MPC505

Advance Information

PowerPC™ MPC505 RISC Microcontroller

The MPC505 is the first implementation of a family of reduced instruction set computer (RISC) microcontrollers based on the PowerPC Architecture™. The MPC505 implements the 32-bit portion of the PowerPC Architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

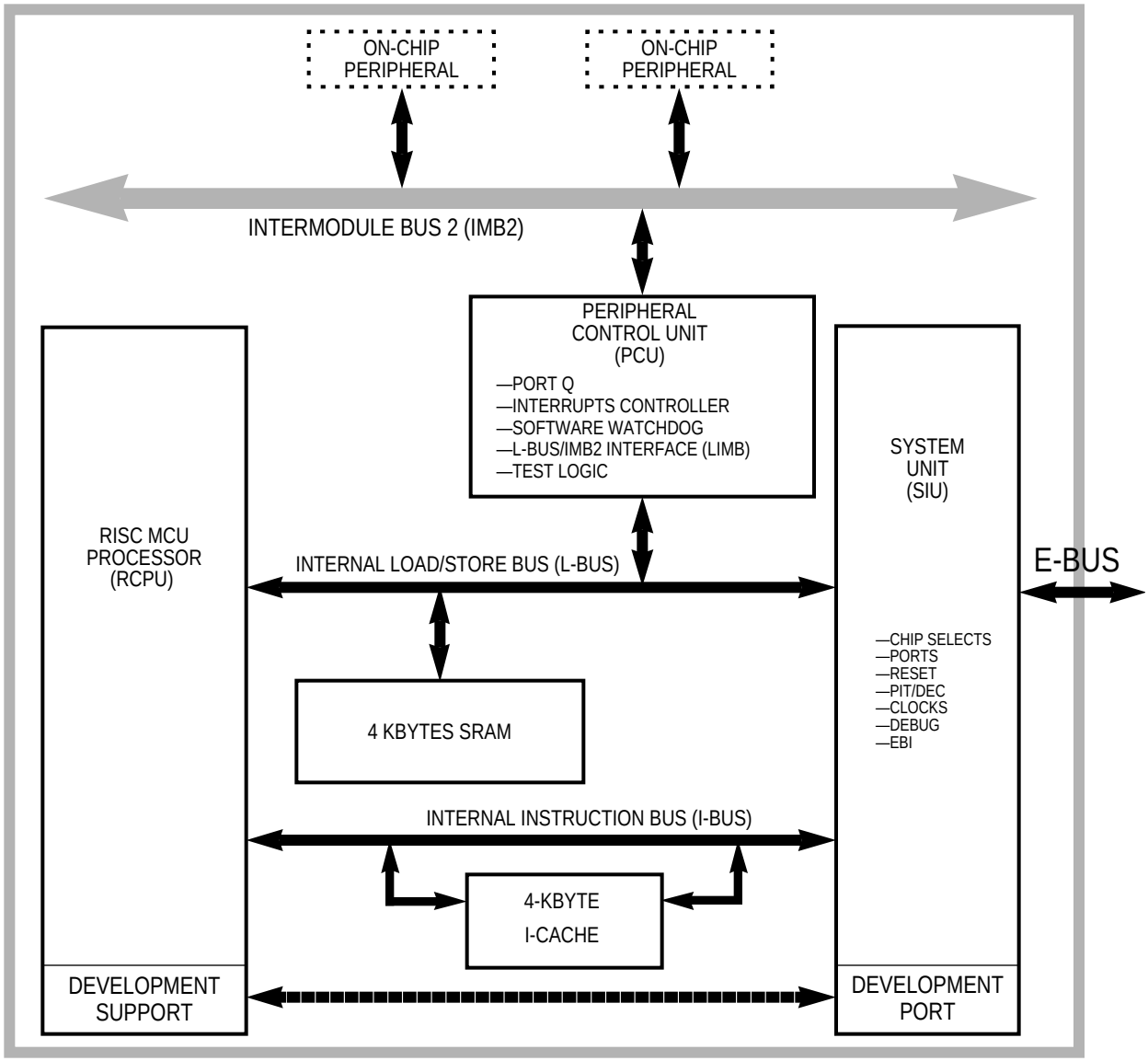
The RISC MCU processor (RCPU) integrates four execution units: an integer unit (IU), a load/store unit (LSU), a branch processing unit (BPU), and a floating-point unit (FPU). The RCPU is capable of issuing one instruction per clock. Instructions can complete out of order for increased performance; however, the MPC505 makes them appear sequential.

The MPC505 includes an on-chip, 4-Kbyte, two-way set associative, physically addressed instruction cache; chip-select logic to reduce or eliminate external decoding logic; 4 Kbytes of static RAM; and extensive processor debugging functionality.

The MPC505 has a high-bandwidth, 32-bit data bus and a 32-bit address bus. The MCU supports 16- and 32-bit memories. Single-beat and burst data memory accesses are supported.

The MPC505 uses an advanced, 3.3-V CMOS process technology.

BLOCK DIAGRAM



FEATURES

- Single-Chip Microcontroller
- RISC MCU Central Processing Unit (RCPU)
  - — 32-Bit PowerPC Architecture
  - — Single-Issue Processor
  - — Integrated Floating-Point Unit
  - — Branch Prediction for Prefetch
  - — Branch Folding
  - — 32 x 32 Bits General-Purpose Register File
  - — 32 x 64 Bits Floating-Point Register File
  - — Precise Exception Model
  - — Internal Harvard Architecture: Load/Store Bus (L-Bus), Instruction Bus (I-Bus)
- System Interface Unit (SIU)
  - — Chip-Select Logic to Reduce or Eliminate External Decoding Logic
  - — Supports a Variety of Memory Types (SRAM, EEPROM)
  - — Supports 16- and 32-bit Devices
  - — System Protection Features Including Bus Monitor, Decrementer, and Periodic Interrupt Timer
  - — On-Chip Phase-Locked Loop (PLL)
  - — Five Dual-Purpose I/O Ports, Two Dual-Purpose Output Ports
- Peripheral Control Unit (PCU)
  - — Software Watchdog
  - — Interrupt Controller to Manage External and Internal Interrupts to the CPU
  - — Dual-Purpose I/O Port
  - — L-bus IMB Interface (LIMB) Connecting L-Bus to Intermodule Bus 2 (IMB2)
- Development Support
  - — Internal Breakpoints
  - — External Watchpoints
  - — Internal Bus Visibility
  - — Program Flow Tracking
  - — Development Port
- 4-Kbyte On-Chip Instruction Cache (I-Cache)
- 4-Kbyte On-Chip Static RAM (SRAM)
- 3.3-V Supply Voltage
- Frequency: dc to 25 MHz (40 MHz in Future Versions)
- Power Consumption: 530 mW @ 25 MHz
- Interrupt Response Time: Less than 1 μs @ 25 MHz

CENTRAL PROCESSING UNIT

The RISC MCU processor (RCPU) integrates four execution units: an integer unit (IU), a load/store unit (LSU), a branch processing unit (BPU), and a floating-point unit (FPU). The use of simple instructions with rapid execution times yields high efficiency and throughput for MPC505-based systems.

Most fixed-point instructions execute in one clock cycle. The FPU is designed to provide cost-effective solutions to most mathematical problems. It includes single- and double-precision multiply-add instructions. Instructions can complete out of order for increased performance; however, the processor makes execution appear sequential.

Major features of the RCPU are as follows:

- High-performance microprocessor
  - — Single clock-cycle execution for many instructions
- Four independent execution units and two register files
  - — Independent load/store unit for load and store operations
  - — Branch-processing unit featuring static branch prediction
  - — A 32-bit integer unit
  - — Fully IEEE 754-compliant floating-point unit for both single- and double-precision operations
  - — Thirty-two general-purpose registers (GPRs) for integer operands
  - — Thirty-two floating-point registers (FPRs) for single- or double-precision operands
- Facilities for enhanced system performance
  - — Programmable big- and little-endian byte ordering
  - — Atomic memory references
- In-system testability and debugging features through boundary-scan capability
- High instruction and data throughput
  - — Condition register (CR) look-ahead operations performed by BPU
  - — Branch-folding capability during execution (zero-cycle branch execution time)
  - — Programmable static branch prediction on unresolved conditional branches
  - — A prefetch queue that can hold up to four instructions, providing look-ahead capability

INSTRUCTION CACHE

The MPC505 instruction cache (I-cache) is a 4-Kbyte, 2-way set associative cache. The cache is organized into 128 sets, with two lines per set and four words per line. Cache lines are aligned on four-word boundaries in memory.

A cache access cycle begins with an instruction request from the CPU instruction unit. In case of a cache hit, the instruction is delivered to the instruction unit. In case of a cache miss, the cache initiates a burst read cycle (four beats per burst, one word per beat) on the instruction bus (I-bus) with the address of the requested instruction. The first word received from the bus is the requested instruction. The cache forwards this instruction to the instruction unit as soon as it is received from the I-bus. A cache line is then selected to receive the data which will be coming from the bus. An LRU (least recently used) replacement algorithm is used to select a line when no empty lines are available.

Each cache line can be used as an SRAM, allowing the application to lock critical code segments that need fast and deterministic execution time.

Major features of the I-cache include the following:

- 4 Kbytes, 2-way set associative, 4 words in a line
- LRU replacement policy
- Lockable SRAM (cache line granularity)
- Critical word first burst access
- Stream hit (allows fetch from the burst buffer and of the word currently on the I-bus)
- Efficiently utilizes the pipeline of the I-bus by initiating a new burst cycle (if miss is detected) while bringing the tail of the previous missed line
- Cache control:
  - — Supports PowerPC invalidate instruction
  - — Supports load & lock (cache line granularity)
- Supports cache inhibit:
  - — as a cache mode of operation (cache disable)
  - — on memory regions (supported by the chip select logic)
- Miss latency is reduced by
  - — sending address to the cache and to the I-bus simultaneously; and
  - — aborting on cache hit before cycle goes external
- Minimum operational power consumption
- Read capability of tags (including all attributes) and data arrays for debugging purposes

SYSTEM INTERFACE UNIT

The system interface unit (SIU) consists of several blocks. These blocks control the buses of the chip, provide the clocks, and provide miscellaneous functions for the system, such as chip selects, test control, reset control, and I/O ports.

The MPC505 has an internal Harvard architecture and a single external bus. The internal buses are the instruction bus (I-bus) and the load/store bus (L-bus). The external bus interface (EBI) connects each of these internal buses with the external bus (E-bus). The chip select block provides user-programmable chip selects to select external memory or peripherals. The clock block controls the generation of the system clocks and such features as programmability of the clocks and low-power modes. The reset control function interfaces to the reset pins and provides a reset status register. The I/O ports provide untimed I/O functions on pins that are not used for their primary function.

External Bus Interface

The external bus interface (EBI) interfaces the external bus (E-bus) with the two internal buses (I-bus and L-bus). The E-bus can perform synchronous, pipeline, or burst transfers. Signals driven onto the E-bus are required to meet the set-up and hold times relative to the bus clock's rising edge. The bus has the ability to support multiple masters, but its protocol is optimized for a single-processor environment.

Major features of the EBI include the following:

- No external glue logic required for a simple system.
- Supports a variety of memory devices (SRAM, EEPROM).
- Fast (one-clock) arbitration possible.
- Bus is synchronous — all signals are referenced to the rising edge of the bus clock.
- 32-bit data bus, 32-bit address bus with byte enables.
- Protocol allows wait states to be inserted before handshaking signals are asserted.
- Supports 16- and 32-bit devices.
- Bus electrical specification minimizes system power consumption.

Chip Selects

Typical microcontrollers require additional hardware to provide external chip-select signals. On the MPC505, the chip-select logic controls the peripheral devices of typical uniprocessor systems. This allows users to implement simple systems without the need to design any external glue logic.

Major features of the chip-select module include the following:

- No external glue logic required for typical systems if the chip-select module is used.
- Modular architecture for ease of expansion.
- Pins are programmable as chip enables, output enables, or write enables.
- Supports multiple regions, with each region having programmable attributes.
- Up to seven programmable wait states for slave devices.
- Programmable address range, block size.

System Protection

The system protection unit within the SIU consists of a reset status register, two interrupt timers, and a bus monitor. System protection features include the following:

- The bus monitor monitors internal-to-external bus accesses. Four selectable response time periods are available, ranging from 16 to 256 system clock cycles. An internal bus error signal is generated if a bus time-out occurs.
- The reset status register distinguishes between all of the possible reset causes.
- A 32-bit decrementer (DEC) and a 16-bit periodic interrupt timer (PIT) generate interrupts. The DEC time period can range from 250 ns to 1073.74 seconds with a 4-MHz source. The PIT time period can range from 1 µs to 65.5 ms with a 4-MHz source.
- A software watchdog prevents system lock-up in case the software becomes trapped in loops with no controlled exit. The software watchdog has a selectable time-out range based on the system clock frequency (167 ns to 2.79 s with a 24-MHz system clock). A reset can be generated if a software watchdog time-out occurs.

Reset

Reset procedures handle system initialization and recovery from catastrophic failure. The MPC505 performs reset with a combination of hardware and software. The SIU determines whether a reset is valid, asserts control signals, performs basic system configuration based on hardware mode-select inputs, and then passes control to the CPU, which performs software initialization.

The following sources can cause reset in the MPC505:

- External reset pin ($\overline{\text{RESET}}$)
- Loss of Clock
- Loss of PLL lock
- Software watchdog reset
- Checkstop reset
- JTAG reset

General-Purpose I/O

External bus interface pins can be used for more than one function. When not used for bus interface signals, these pins can be used as digital I/O pins.

SIU digital I/O pins are grouped into 8-bit ports. The following registers are associated with each I/O port. (Output-only ports do not have a data direction register.)

- Pin assignment register — allows the user to configure a pin for its primary function or digital I/O.
- Data direction register — configures individual pins as input or output pins.
- Data register — allows writes to output pins and reads of input pins

PERIPHERAL CONTROL UNIT

The peripheral control unit (PCU) consists of the following submodules:

- Software watchdog — provides system protection.
- Interrupt controller — controls the interrupts that external peripherals and internal modules send to the CPU.
- Port Q — provides for digital I/O on pins that are not being used as interrupt inputs.
- L-bus/IMB2 interface (LIMB) — provides an interface between the load/store bus and the second generation intermodule bus (IMB2). The IMB2, which is comparable to the IMB in the modular 68300 and M68HC16 families, connects on-chip peripherals to the processor via the LIMB.

Interrupt Controller

The interrupt controller consolidates all the interrupt sources into a single interrupt signal to the processor. The interrupt controller supports up to 32 maskable interrupt levels. Each external interrupt request ($\overline{IRQ}$) input can be made edge-sensitive or level-sensitive. The interrupt controller uses the following registers:

- IRQPEND — Contains a status bit for each of the 32 interrupt levels. Each bit of IRQPEND is a read-only status bit that reflects the current state of the corresponding interrupt signal.
- IRQENABLE — Contains an enable bit for each of the 32 interrupt levels.
- IRQAND — Logical AND of the IRQPEND and IRQENABLE registers. This register reflects which levels are actually causing the $\overline{IRQ}$ input to the processor to be asserted.
- IRQLEVELS — Contains three 5-bit fields that determine the interrupt request levels of the PIT and the external interrupt request signals.

The interrupt controller does not enforce a priority scheme. All interrupt priority is determined by the software. In this way, the system is not limited to a particular interrupt priority scheme.

Software Watchdog

The software watchdog monitors the system software interface and requires the software to take periodic action in order to communicate that it is executing properly. To protect against software error, the following service sequence must be executed on a regular basis:

1. Write 0x556C to the SWSR
2. Write 0xAA39 to the SWSR

This sequence clears the watchdog timer, and the timing process begins again. If this periodic servicing does not occur, the software watchdog issues a reset. If any value other than 0x556C or 0xAA39 is written to the SWSR, the service sequence must start over.

Port Q

When not used as interrupt inputs, interrupt request ($\overline{IRQ}$) pins can be used for digital I/O. The following registers control port Q operation:

- Port Q Pin Assignment Register (PQPAR) — Allows the user to configure each pin as a digital input, digital output, edge- or level-sensitive interrupt request to the CPU, or edge- or level-sensitive interrupt request to the interrupt controller.
- Port Q Data Register (PORTQ) — Monitors or controls the state of its pins, depending on the encoding for each pin in the PQPAR. PORTQ and PORTQE make up the PQEDGDAT register.
- Port Q Edge-Detect Status Register (PORTQE) — Monitors when the proper transition occurs on a port Q or interrupt request pin. PORTQ and PORTQE make up the PQEDGDAT register.

STATIC RAM MODULE

The SRAM module consists of one 4-Kbyte block of static RAM. The SRAM module is accessible to the CPU and other bus masters via the MPC505 L-bus.

The primary function of this module is to serve as fast (one-cycle access), general-purpose RAM for the MCU. The SRAM can be read or written as either bytes, half-words or words.

The bus interface and control logic for the SRAM module are powered by V_{DD}. A separate pin, VDDKAP1, supplies power to the memory array. VDDKAP1 must never fall below V_{DD}. If main power (V_{DD}) is shut off, VDDKAP1 can subsequently be lowered to save power. While VDDKAP1 is reduced, data in the SRAM array remains valid, but access to the array is blocked.

- Fast, One-Cycle Access
- Low-Power Modes
  - — Two-Cycle Access Mode Provides Power Savings while Keeping Memory Active
  - — Stop Mode Disables the SRAM Module while Preserving SRAM Array
  - — Standby Mode Preserves SRAM Array while Main Power is Shut Off
- Programmable Attributes (Supervisor Only, Data Only, Read Only)

DEVELOPMENT SUPPORT

MPC505 development support features include internal breakpoint comparators, internal bus visibility, program flow tracking, and a development port.

- Breakpoints Force Exception-Handling when User-Programmable Conditions Are Met
- Watchpoints Are Reported on External Pins when User-Programmable Conditions are Met
- Show-cycle Features Allow Internal Bus Activity to be Visible Externally
- Program Flow Tracking
  - — Exact program trace can be obtained with minimal decrease in performance.
  - — Instruction execution tracking output signals.
- Hardware and Software Debug Modes
  - — Hardware debug mode supports debugging with an in-circuit emulator. All development support features are protected for use by an in-circuit emulator. Instructions are shifted in and data is shifted in and out through the development port.
  - — Software debug mode supports debugging with a software monitor. All development support features are protected for use by an exception handler (i.e., a software monitor program).
- Development Port
  - — Allows external development system full control over the CPU during debug without using regular bus pins and without placing restrictions on user software.
  - — Uses a three-pin serial interface for both software and hardware debug modes.
  - — Allows external breakpoints in either hardware or software debug mode.
  - — Supports both asynchronous and synchronous serial transmissions.

NOTES

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