Advance Information

MPC7451EC/D
Rev. 0.1, 11/2001

MPC7451 RISC Microprocessor Hardware Specifications

The MPC7451 is a reduced instruction set computing (RISC) microprocessor that implements the PowerPC instruction set architecture. This document describes pertinent electrical and physical characteristics of the MPC7451. For functional characteristics of the processor, refer to the *MPC7450 RISC Microprocessor Family User's Manual*.

This document contains the following topics:

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1.1 Overview

The MPC7451 is the third implementation of the fourth generation (G4) microprocessors from Motorola. The MPC7451 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The MPC7451 consists of a processor core, a 256-Kbyte L2, and an internal L3 tag and controller which support a glueless backside L3 cache through a dedicated high bandwidth interface.

Figure 1 shows a block diagram of the MPC7451. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit. The memory storage subsystem supports the MPX bus interface to main memory and other system resources. The L3 interface supports 1 or 2 Mbytes of external SRAM for L3 cache data.

Note that the MPC7451 is a footprint-compatible, drop-in replacement in a MPC7450 application as long as the core power supply is 1.6 V.

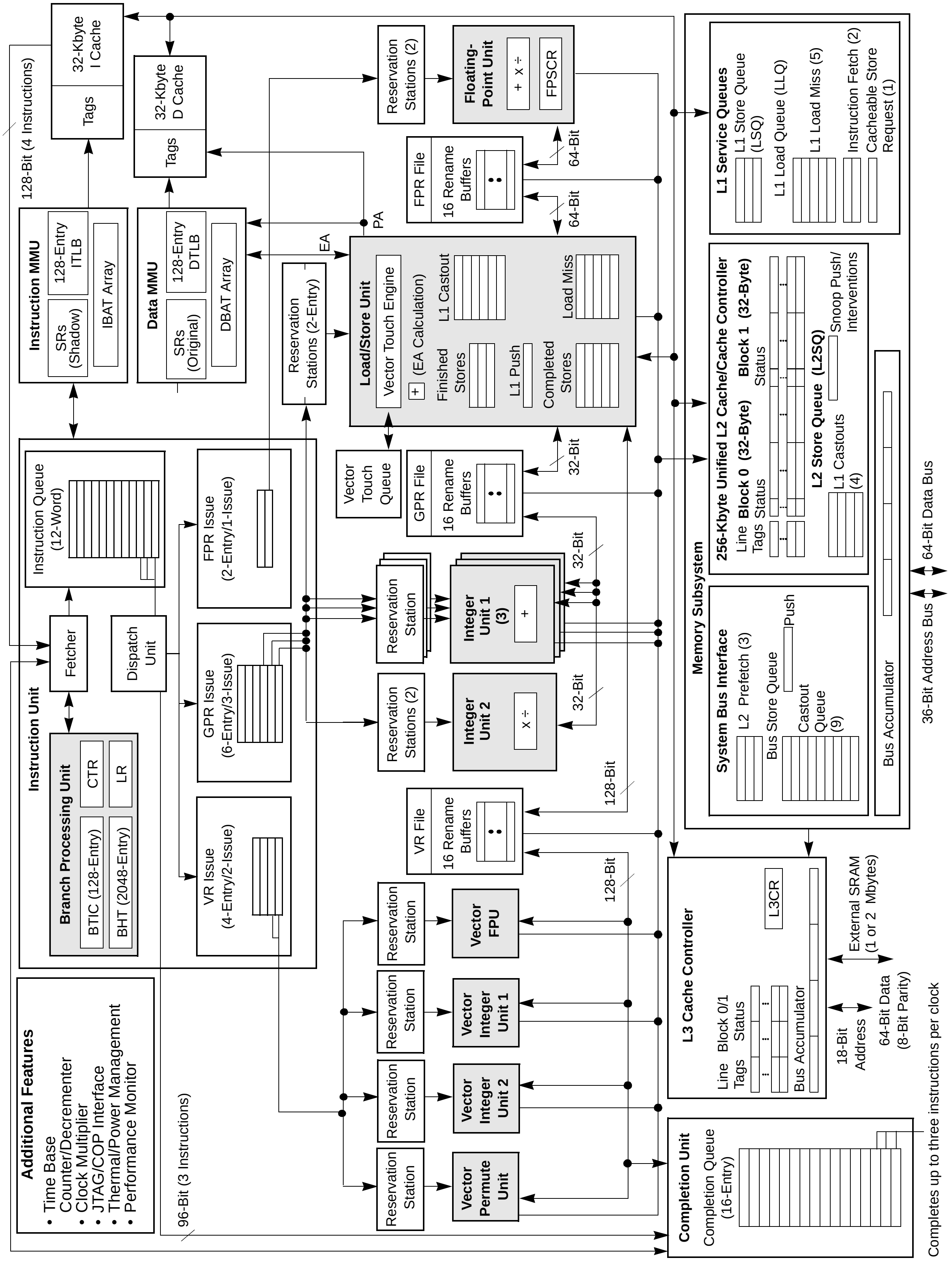


Figure 1. MPC7451 Block Diagram

1.2 Features

This section summarizes features of the MPC7451 implementation of the PowerPC architecture. Major features of the MPC7451 are as follows:

Major features of the MPC7451 are as follows:

- High-performance, superscalar microprocessor
  - As many as 4 instructions can be fetched from the instruction cache at a time
  - As many as 3 instructions can be dispatched to the issue queues at a time
  - As many as 12 instructions can be in the instruction queue (IQ)
  - As many as 16 instructions can be at some stage of execution simultaneously
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history table (BHT) with two bits per entry for four levels of prediction— not-taken, strongly not-taken, taken, strongly taken
    - Up to three outstanding speculative branches
    - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
    - 8-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions.
  - Four integer units (IUs) that share 32 GPRs for integer operands
    - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
    - IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
  - Five-stage FPU and a 32-entry FPR file
    - Fully IEEE 754-1985-compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Hardware support for denormalized numbers
    - Thirty-two 64-bit FPRs for single- or double-precision operands
  - Four vector units and 32-entry vector register file (VRs)
    - Vector permute unit (VPU)

    - Vector integer unit 1 (VIU1) handles short-latency AltiVec integer instructions, such as vector add instructions (**vaddsbs**, **vaddshs**, and **vaddsws**, for example)
    - Vector integer unit 2 (VIU2) handles longer -latency AltiVec integer instructions, such as vector multiply add instructions (**vmhaddshs**, **vmhraddshs**, and **vmladduhm**, for example).
    - Vector floating-point unit (VFPU)
  - Three-stage load/store unit (LSU)
    - Supports integer, floating-point and vector instruction load/store traffic
    - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
    - Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with 1-cycle throughput
    - Four-cycle FPR load latency (single, double) with 1-cycle throughput
    - No additional delay for misaligned access within double-word boundary
    - Dedicated adder calculates effective addresses (EAs)
    - Supports store gathering
    - Performs alignment, normalization, and precision conversion for floating-point data
    - Executes cache control and TLB instructions
    - Performs alignment, zero padding, and sign extension for integer data
    - Supports hits under misses (multiple outstanding misses)
    - Supports both big- and little-endian modes, including misaligned little-endian accesses
- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries—IQ0, IQ1, and IQ2.
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle.
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - The decode/dispatch stage fully decodes each instruction.
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending.
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order

- Tracks unresolved branches and flushes instructions after a mispredicted branch
- Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 256-Kbyte, 8-way set associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total 9-cycle load latency for an L1 data cache miss that hits in L2
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Level 3 (L3) cache interface
  - Provides critical double-word forwarding to the requesting unit
  - Internal L3 cache controller and tags
  - External data SRAMs
  - Support for 1- and 2-Mbyte L3 caches
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte (1 M) or 128-byte (2 M) sectored line size
  - Private memory capability for half (1-Mbyte minimum) or all of the L3 SRAM space
  - Supports MSUG2 dual data rate (DDR) synchronous Burst SRAMs, PB2 pipelined synchronous Burst SRAMs, and pipelined (register-register) Late Write synchronous Burst SRAMs

    - Supports parity on cache and tags
    - Configurable core-to-L3 frequency divisors
    - 64-bit external L3 data bus sustains 64 bits per L3 clock cycle
- Separate memory management units (MMUs) for instructions and data
    - 52-bit virtual address; 32- or 36-bit physical address
    - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
    - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
    - Separate IBATs and DBATs (four each) also defined as SPRs
    - Separate instruction and data translation lookaside buffers (TLBs)
        - Both TLBs are 128-entry, two-way set associative, and use LRU replacement algorithm
        - TLBs are hardware- or software-reloadable (that is, on a TLB miss a page table search is performed in hardware or by system software)
- Efficient data flow
    - Although the VR/LSU interface is 128 bits, the L1/L2/L3 bus interface allows up to 256 bits.
    - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
    - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache.
    - As many as 8 outstanding, out-of-order, cache misses are allowed between the L1 data cache and L2/L3 bus.
    - As many as 16 out-of-order transactions can be present on the MPX bus
    - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
    - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
    - Separate additional queues for efficient buffering of outbound data (such as cast outs and write through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
    - Hardware-enforced, MESI cache coherency protocols for data cache
    - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
    - 1.6-V processor core
    - The following three power-saving modes are available to the system:
        - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
        - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
        - Deep sleep—When the part is in the sleep state, the system can disable the PLL resulting.

The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.

  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7451-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption.
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on L1, L2, and L3 cache arrays

1.3 Comparison with the MPC7400

Table 1 compares the key features of the MPC7451 with the key features of the earlier MPC7400. To achieve a higher frequency, the number of logic levels per cycle is reduced. Also, to achieve this higher frequency, the pipeline of the MPC7451 is extended (compared to the MPC7400), while maintaining the same level of performance as measured by the number of instructions executed per cycle (IPC).

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7451	MPC7400/MPC7410
Basic Pipeline Functions		
Logic Inversions per Cycle	18	28
Pipeline Stages up to Execute	5	3
Total Pipeline Stages (Minimum)	7	4
Pipeline Maximum Instruction Throughput	3 + Branch	2 + Branch
Pipeline Resources		
Instruction Buffer Size	12	6
Completion Buffer Size	16	8
Renames (Integer, Float, Vector)	16, 16, 16	6, 6, 6
Maximum Execution Throughput		
SFX	3	2
Vector	2 (Any 2 of 4 Units)	2 (Permute/Fixed)
Scalar Floating-Point	1	1

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7451	MPC7400/MPC7410
Out-of-Order Window Size in Execution Queues		
SFX Integer Units	1 Entry × 3 Queues	1 Entry × 2 Queues
Vector Units	In Order, 4 Queues	In Order, 2 Queues
Scalar Floating-Point Unit	In Order	In Order
Branch Processing Resources		
Prediction Structures	BTIC, BHT, Link Stack	BTIC, BHT
BTIC Size, Associativity	128-Entry, 4-Way	64-Entry, 4-Way
BHT Size	2K-Entry	512-Entry
Link Stack Depth	8	None
Unresolved Branches Supported	3	2
Branch Taken Penalty (BTIC Hit)	1	0
Minimum Misprediction Penalty	6	4
Execution Unit Timings (Latency-Throughput)		
Aligned Load (Integer, Float, Vector)	3-1, 4-1, 3-1	2-1, 2-1, 2-1
Misaligned Load (Integer, Float, Vector)	4-2, 5-2, 4-2	3-2, 3-2, 3-2
L1 Miss, L2 Hit Latency	6 (9)	9 (11)[1]
SFX (aDd Sub, Shift, Rot, Cmp, Logicals)	1-1	1-1
Integer Multiply (32 × 8, 32 × 16, 32 × 32)	3-1, 3-1, 4-2	2-1, 3-2, 5-4
Scalar Float	5-1	3-1
VSFX (Vector Simple)	1-1	1-1
VCFX (Vector Complex)	4-1	3-1
VFPU (Vector Float)	4-1	4-1
VPER (Vector Permute)	2-1	1-1
MMUs		
MMUs (Instruction and Data)	128-Entry, 2-Way	128-Entry, 2-Way
Tablewalk Mechanism	Hardware + Software	Hardware
L1 I Cache/D Cache Features		
Size	32K/32K	32K/32K
Associativity	8-Way	8-Way
Locking Granularity/Style	4-Kbyte/Way	Full Cache
Parity on I Cache	Word	None
Parity on D Cache	Byte	None
Number of D Cache Misses (Load/Store)	5/1	8 (Any Combination)
Data Stream Touch Engines	4 Streams	4 Streams
On-Chip Cache Features		
Cache Level	L2	None (Except L1)

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7451	MPC7400/MPC7410
Size/Associativity	256-Kbyte/8-Way	N/A
Access Width	256 Bits	N/A
Number of 32-Byte Sectors/Line	2	N/A
Parity	Byte	N/A
Off-Chip Cache Support		
Cache Level	L3	L2
On-Chip Tag Logical Size	1MB, 2MB	0.5MB, 1MB, 2MB
Associativity	8-Way	2-Way
Number of 32-Byte Sectors/Line	2, 4	1, 2, 4
Off-Chip Data SRAM Support	MSUG2 DDR, LW, PB2	LW, PB2, PB3
Data Path Width	64	64
Direct Mapped SRAM Sizes	1 Mbyte, 2 Mbytes	0.5 Mbyte, 1 Mbyte, 2 Mbytes
Parity	Byte	Byte

[1] Numbers in parentheses are for 2:1 SRAM.

1.4 General Parameters

The following list provides a summary of the general parameters of the MPC7451:

Technology	0.18 µm CMOS, six-layer metal
Die size	8.69 mm × 12.17 mm (106 mm^2)
Transistor count	33 million
Logic design	Fully static
Packages	MPC7451: Surface mount 483 ceramic ball grid array (CBGA)
Core power supply	1.6 V ± 50 mV DC nominal
I/O power supply	1.8 V ± 5% DC or 2.5 V ± 5% DC or 1.5 V ± 5% DC (L3 interface only)

1.5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7451.

1.5.1 DC Electrical Characteristics

The tables in this section describe the MPC7451 DC electrical characteristics. Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.95	V	4
PLL supply voltage		AV_{DD}	–0.3 to 1.95	V	4
Processor bus supply voltage	BVSEL = 0	OV_{DD}	–0.3 to 1.95	V	3, 6
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	–0.3 to 2.7	V	3, 7
L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	–0.3 to 1.65	V	3, 8
	L3VSEL = 0	GV_{DD}	–0.3 to 1.95	V	3, 9
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	–0.3 to 2.7	V	3, 10
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3	V	2, 5
	L3 bus	V_{in}	–0.3 to GV_{DD} + 0.3	V	2, 5
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.3	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or GV_{DD} by more than 0.3 V at any time including during power-on reset.
3. **Caution**: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V at any time including during power-on reset.
4. **Caution**: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 0.4 V at any time including during power-on reset.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. BVSEL must be set to 0, such that the bus is in 1.8 V mode.
7. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5 V mode.
8. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5 V mode.
9. L3VSEL must be set to 0, such that the bus is in 1.8 V mode.
10. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5 V mode.

Figure 2 shows the undershoot and overshoot voltage on the MPC7451.

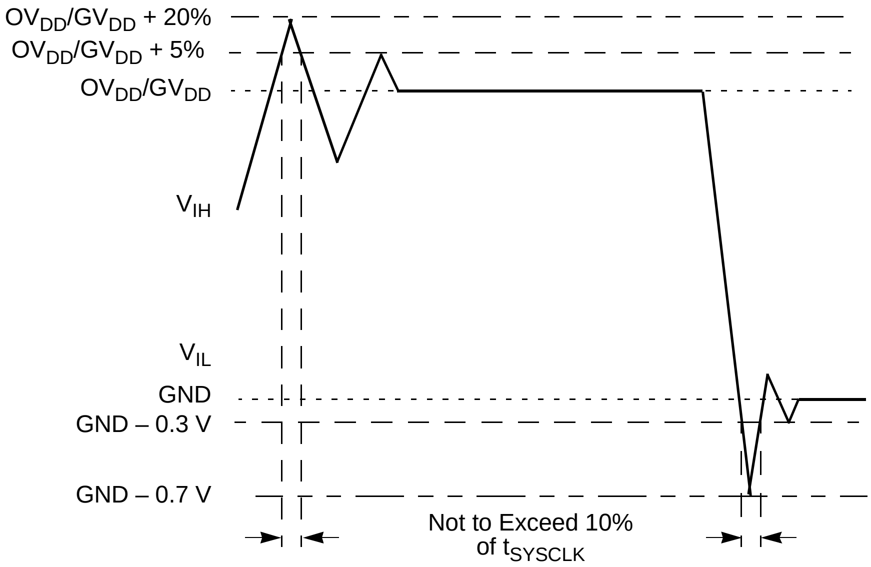


Figure 2. Overshoot/Undershoot Voltage

The MPC7451 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7451 core voltage must always be provided at nominal 1.6 V (see Table 4 for actual recommended core voltage). Voltage to the L3 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 3. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or GV_{DD} power pins.

Table 3. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal	L3 Bus Input Threshold is Relative to:	Notes
0	1.8 V	0	1.8 V	1, 4
¬$\overline{\text{HRESET}}$	Not Available	¬$\overline{\text{HRESET}}$	1.5 V	1, 3
$\overline{\text{HRESET}}$	2.5 V	$\overline{\text{HRESET}}$	2.5 V	1, 2
1	2.5 V	1	2.5 V	1

Notes:

1. **Caution:** The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in Table 2.
2. To select the 2.5-V threshold option for the processor bus, BVSEL should be tied to $\overline{\text{HRESET}}$ so that the two signals change state together. Similarly, to select 2.5 V for the L3 bus, tie L3VSEL to $\overline{\text{HRESET}}$. This is the preferred method for selecting this mode of operation.
3. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.
4. If used, pulldown resistors should be less than 250 Ω.

Table 4 provides the recommended operating conditions for the MPC7451.

Table 4. Recommended[1] Operating Conditions

Characteristic		Symbol	Recommended Value		Unit	Notes
			Min	Max		
Core supply voltage		V_{DD}	1.6 V ± 50 mV		V	
PLL supply voltage		AV_{DD}	1.6 V ± 50 mV		V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 5%		V	
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	2.5 V ± 5%		V	
L3 bus supply voltage	L3VSEL = 0	GV_{DD}	1.8 V ± 5%		V	
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	2.5 V ± 5%		V	
	L3VSEL = $\neg\overline{\text{HRESET}}$	GV_{DD}	1.5 V ± 5%		V	
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	V	
	L3 bus	V_{in}	GND	GV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section 1.9.2, “PLL Power Supply Filtering” and not necessarily the voltage at the AV_{DD} pin which may be reduced from V_{DD} by the filter.

Table 5 provides the package thermal characteristics for the MPC7451.

Table 5. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	<0.1	°C/W
CBGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θ_{JB}	2.2	°C/W

Note: Refer to Section 1.9, “System Design Information,” for more details about thermal management.

Table 6 provides the DC electrical characteristics for the MPC7451.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)		1.5	V_{IH}	$GV_{DD} \times 0.65$	$GV_{DD} + 0.3$	V	6
		1.8	V_{IH}	$OV_{DD}/GV_{DD} \times 0.65$	$OV_{DD}/GV_{DD} + 0.3$	V	
		2.5	V_{IH}	1.7	$OV_{DD}/GV_{DD} + 0.3$	V	
Input low voltage (all inputs except SYSCLK)		1.5	V_{IL}	–0.3	$GV_{DD} \times 0.35$	V	6
		1.8	V_{IL}	–0.3	$OV_{DD}/GV_{DD} \times 0.35$	V	
		2.5	V_{IL}	–0.3	0.7	V	
SYSCLK input high voltage		—	CV_{IH}	1.4	$OV_{DD} + 0.3$	V	
SYSCLK input low voltage		—	CV_{IL}	–0.3	0.4	V	
Input leakage current, $V_{in} = GV_{DD}/OV_{DD} + 0.3$ V		—	I_{in}	—	10	μA	2, 3
High impedance (off-state) leakage current, $V_{in} = GV_{DD}/OV_{DD} + 0.3$ V		—	I_{TSI}	—	10	μA	2, 3, 5
Output high voltage, I_{OH} = –5 mA		1.5	V_{OH}	$OV_{DD}/GV_{DD} - 0.45$	—	V	6
		1.8	V_{OH}	$OV_{DD}/GV_{DD} - 0.45$	—	V	
		2.5	V_{OH}	1.7	—	V	
Output low voltage, I_{OL} = 5 mA		1.5	V_{OL}	—	0.45	V	6
		1.8	V_{OL}	—	0.45	V	
		2.5	V_{OL}	—	0.7	V	
Capacitance, V_{in} = 0 V, f = 1 MHz	L3 interface	—	C_{in}	—	9.5	pF	4
	All other inputs			—	8.0	pF	4

Notes:

1. Nominal voltages; see Table 4 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while GV_{DD} is the reference for the L3 bus signals.
3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
6. Applicable to L3 bus interface only.

Table 7 provides the power consumption for the MPC7451.

Table 7. Power Consumption for MPC7451

	Processor (CPU) Frequency		Unit	Notes
	600 MHz	667 MHz		
Full-Power Mode				
Typical	13.0	14.5	W	1, 3
Maximum	17.5	19.0	W	1, 2
Doze Mode				
Typical	—	—	W	1, 3, 4
Nap Mode				
Typical	1.4	1.7	W	1, 3
Sleep Mode				
Typical	0.7	0.8	W	1, 3
Deep Sleep Mode (PLL Disabled)				
Typical	460	510	mW	1, 3

Notes:

1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically <20% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, with or without AltiVec, maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 4) in a system while running a typical code sequence.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

1.5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7451. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.5.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_EXT and PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 1.11, “Ordering Information.”

1.5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

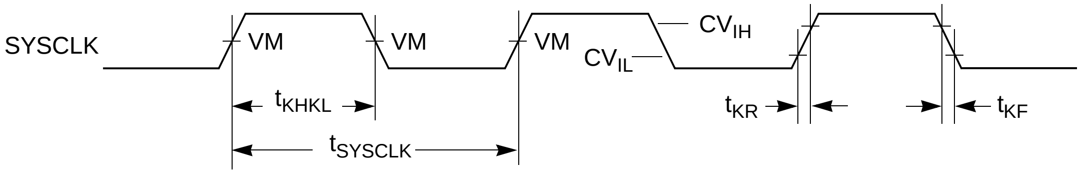
Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency				Unit	Notes
		600 MHz		667 MHz			
		Min	Max	Min	Max		
Processor frequency	f_{core}	500	600	500	667	MHz	1
VCO frequency	f_{VCO}	1000	1200	1000	1333	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	ns	
SYSCLK rise and fall time	t_{KR} and t_{KF}	—	1.0	—	1.0	ns	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	ps	4, 6
Internal PLL relock time		—	100	—	100	µs	5

Notes:
1. **Caution**: The SYSCLK frequency, PLL_EXT and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_EXT, PLL_CFG[0:3] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_EXT and PLL_CFG[0:3] settings.
2. Rise and fall times for the SYSCLK input measured from 0.4 V to 1.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
6. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade connected PLL-based devices to track SYSCLK drivers with the specified jitter.

Figure 3 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 3. SYSCLK Input Timing Diagram

1.5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7451 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 1.5.2.3, “L3 Clock AC Specifications.”

Table 9. Processor Bus AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol[2]	All Speed Grades		Unit	Notes
		Min	Max		
Mode select input setup to HRESET	t_{MVRH}	8	—	t_{sysclk}	3, 4, 5, 6
HRESET to mode select input hold	t_{MXRH}	0	—	ns	3, 5
Input setup times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI, D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], HRESET, INT, MCP, QACK, SMI, SRESET, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	 t_{AVKH} t_{IVKH}	 2.0 2.0	 — —	ns	
Input hold times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI, D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], HRESET, INT, MCP, QACK, SMI, SRESET, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	 t_{AXKH} t_{IXKH}	 0 0	 — —	ns	
Output valid times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI TS D[0:63], DP[0:7] ARTRY/SHD0/SHD1 BR, CKSTP_OUT, DRDY, HIT, PMON_OUT, QREQ]	 t_{KHAV} t_{KHTSV} t_{KHDV} t_{KHARV} t_{KHOV}	 — — — — —	 2.5 2.5 2.5 2.5 2.5	ns	
Output hold times: A[0:35], AP[0:4], GBL, TBST, TSIZ[0:2], WT, CI TS D[0:63], DP[0:7] ARTRY/SHD0/SHD1 BR, CKSTP_OUT, DRDY, HIT, PMON_OUT, QREQ	 t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5 0.5 0.5	 — — — — —	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	
SYSCLK to output high impedance (all except TS, ARTRY, SHD0, SHD1)	t_{KHOZ}	—	3.5	ns	
SYSCLK to TS high impedance after precharge	t_{KHTSPZ}	—	1	t_{sysclk}	5, 7, 10
Maximum delay to ARTRY/SHD0/SHD1 precharge	t_{KHARP}	—	1	t_{sysclk}	5, 8, 9, 10

Table 9. Processor Bus AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol^2	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to ARTRY/SHD0/SHD1 high impedance after precharge	t_{KHARPZ}	—	2	t_{sysclk}	5, 8, 9, 10

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of HRESET (see Figure 5).
4. This specification is for configuration mode select only.
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are: BVSEL, L3VSEL, PLL_CFG[0:3], PLL_EXT, BMODE[0:1].
7. According to the bus protocol, TS is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for TS is $0.5 \times t_{SYSCLK}$, i.e., less than the minimum t_{SYSCLK} period, to ensure that another master asserting TS on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high impedance behavior is guaranteed by design.
8. According to the bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue because any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of AACK. The nominal precharge width for ARTRY is 1.0 t_{sysclk}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
9. According to the MPX bus protocol, SHD0 and SHD1 can be driven by multiple bus masters beginning the cycle of TS. Timing is the same as ARTRY, i.e., the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for SHD0 and SHD1 is 1.0 t_{sysclk}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
10. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7451.

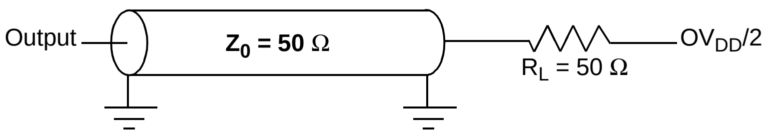
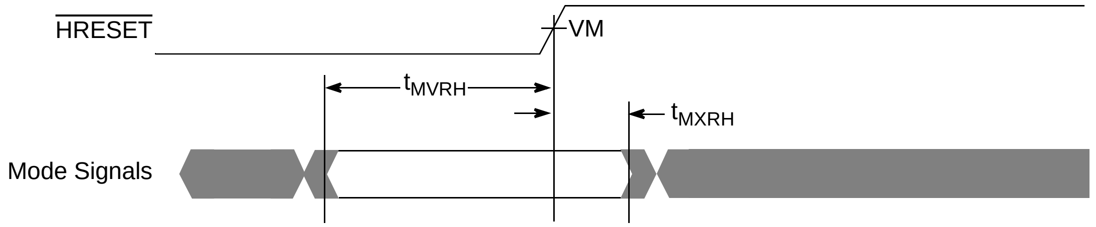


Figure 4. AC Test Load

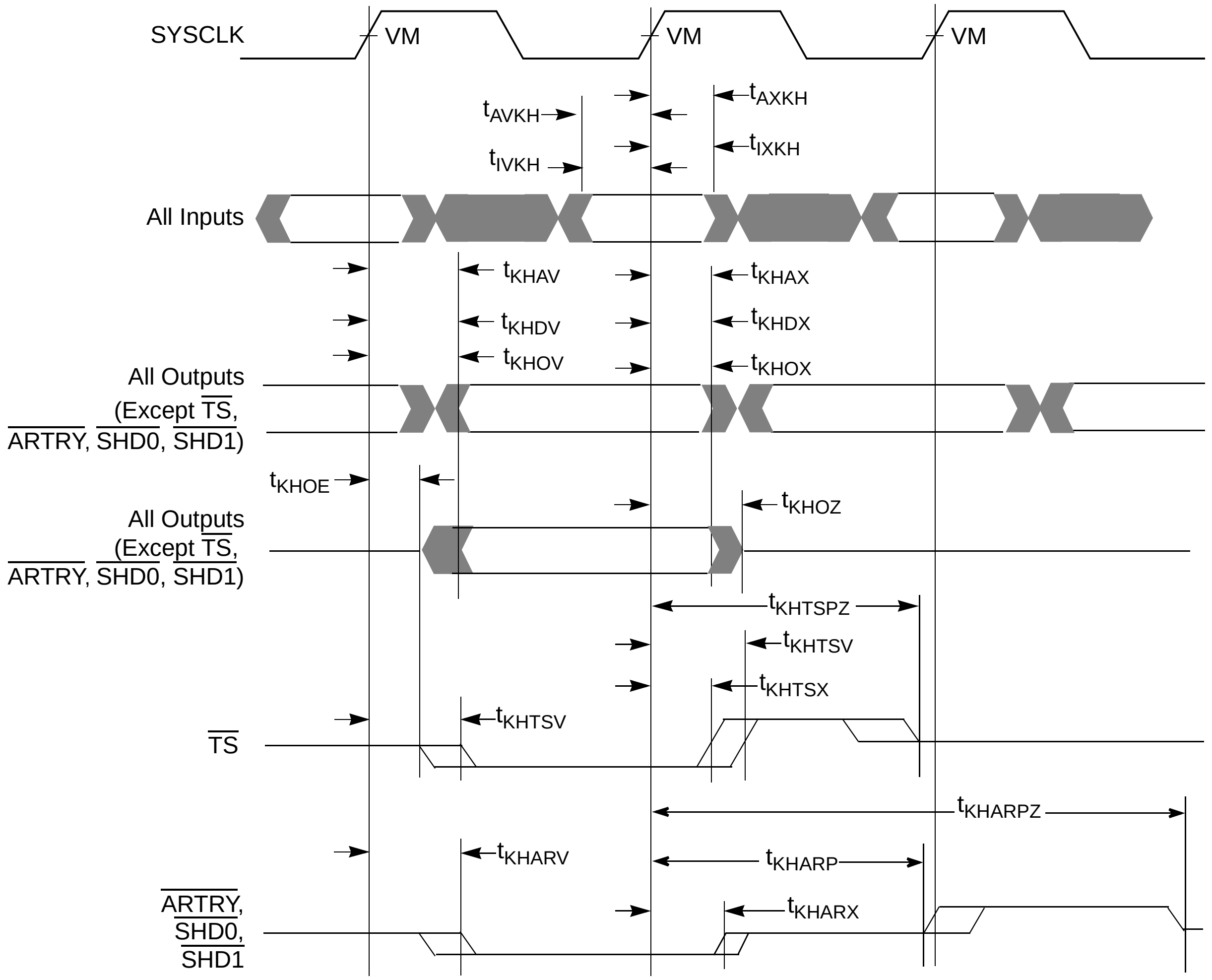
Figure 5 provides the mode select input timing diagram for the MPC7451.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7451.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 6. Input/Output Timing Diagram

1.5.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register (L3CR[6:8]) core-to-L3 divisor ratio. See Table 17 for example core and L3 frequencies at various divisors. Table 10 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7.

The maximum L3_CLK frequency is the core frequency divided by two. However, very few SRAM designs will be able to operate in this mode and most designs will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the maximum L3_CLK frequency shown in Table 10 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the MPC7451 will be a function of the AC timings of the MPC7451, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Motorola is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 10. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 200 MHz or less.

Table 10. L3_CLK Output AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades Min	All Speed Grades Max	Unit	Notes
L3 clock frequency	f_{L3_CLK}	75	266	MHz	1
L3 clock cycle time	t_{L3_CLK}	3.75	13.3	ns	
L3 clock duty cycle	t_{CHCL}/t_{L3_CLK}	50		%	2
L3 clock output-to-output skew (L1_CLK0 to L1_CLK1)	$t_{L3CSKW1}$	—	200	ps	3
L3 clock output-to-output skew (L1_CLK[0:1] to L1_ECHO_CLK[1:3])	$t_{L3CSKW2}$	—	100	ps	4
L3 clock jitter		—	±50	ps	5

Notes:

1. The maximum L3 clock frequency will be system dependent. See Section 1.5.2.3, “L3 Clock AC Specifications” for an explanation that this maximum frequency is not functionally tested at speed by Motorola.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the write data signals which are separately latched onto each SRAM part by these pairs of signals.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This must be accounted for, along with clock skew, in any L3 timing analysis.

The L3_CLK timing diagram is shown in Figure 7.

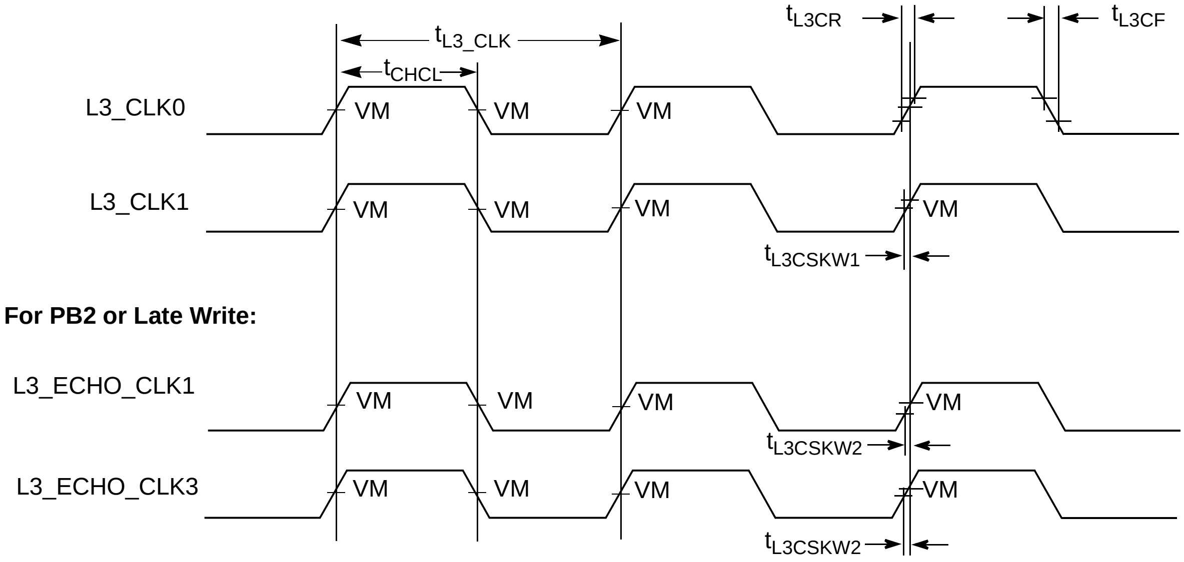


Figure 7. L3_CLK_OUT Output Timing Diagram

1.5.2.4 L3 Bus AC Specifications

The MPC7451 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the MPC7451 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the chip-to-SRAM interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched.
- For a 1-Mbyte L3, use address bits 0:16 (bit 0 is LSB).
- No pull-up resistors are required for the L3 interface.
- For high speed operations, L3 interface address and control signals should be a “T” with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 8 shows the AC test load for the L3 interface.

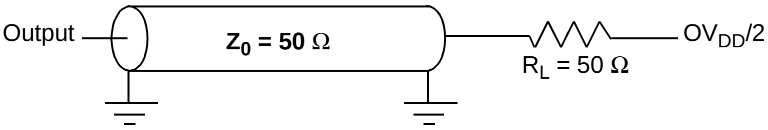


Figure 8. AC Test Load for the L3 Interface

In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the MPC7451 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 12, Table 13, and Table 14), the limitations of functional testers described in Section 1.5.2.3, “L3 Clock AC Specifications,” and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 9 or Figure 11, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 9); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the MPC7451; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The *MPC7450 RISC Microprocessor Family User's Manual* refers to logical settings called "Sample Points" used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the *MPC7450 RISC Microprocessor Family User's Manual*. Three specifications are used in this calculation and are given in Table 11. It is essential that all three specifications are included in the calculations to determine the sample points, as incorrect settings can result in errors and unpredictable behavior. For more information, see the *MPC7450 RISC Microprocessor Family User's Manual.*

Table 11. Sample Points Calculation Parameters

Parameter	Symbol	Max	Unit	Notes
Delay from processor clock to internal_L3_CLK	t_{AC}	3/4	t_{L3_CLK}	1
Delay from internal_L3_CLK to L3_CLK[*n*] output pins	t_{CO}	3	ns	2
Delay from L3_ECHO_CLK[*n*] to receive latch	t_{ECI}	3	ns	3

Notes:

1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[*n*] signals. With proper board routing, this offset ensures that the L3_CLK[*n*] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[*n*] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[*n*] to data valid and ready to be sampled from the FIFO.

1.5.2.4.1 L3 Bus AC Specifications for DDR MSUG2 SRAMs

When using DDR MSUG2 SRAMs at the L3 interface, the parts should be connected as shown in Figure 9.

Outputs from the MPC7451 are actually launched on the edges of an internal clock phase-aligned to SYSCLK (adjusted for core and L3 frequency divisors). L3_CLK0 and L3_CLK1 are this internal clock output with 90° phase delay, so outputs are shown synchronous to L3_CLK0 and L3_CLK1. Output valid times are typically negative when referenced to L3_CLK*n* because the data is launched one-quarter period before L3_CLK*n* to provide adequate setup time at the SRAM after the delay-matched address, control, data, and L3_CLK*n* signals have propagated across the printed wiring board.

Inputs to the MPC7451 are source-synchronous with the CQ clock generated by the DDR MSUG2 SRAMs. These CQ clocks are received on the L3_ECHO_CLK*n* inputs of the MPC7451. An internal circuit delays the incoming L3_ECHO_CLK*n* signal such that it is positioned within the valid data window at the internal receiving latches. This delayed clock is used to capture the data into these latches which comprise the receive FIFO. This clock is asynchronous to all other processor clocks. This latched data is subsequently read out of the FIFO synchronously to the processor clock. The time between writing and reading the data is set by the using the sample point settings defined in the L3CR register.

Table 12 provides the L3 bus interface AC timing specifications for the configuration as shown in Figure 9, assuming the timing relationships shown in Figure 10 and the loading shown in Figure 8.

Table 12. L3 Bus Interface AC Timing Specifications for MSUG2

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR} and t_{L3CF}	—	1.0	ns	1
Setup times:Data and parity	t_{L3DVEH} and t_{L3DVEL}	$-(t_{L3\_ECHO\_CLK}/4 - 0.35)$	—	ns	2, 3, 4
Input hold times:Data and parity	t_{L3DXEH} and t_{L3DXEL}	$t_{L3\_ECHO\_CLK}/4 + 0.35$	—	ns	2, 4
Valid times:Data and parity All other outputs	t_{L3CHDV} and t_{L3CLDV} t_{L3CHOV}	— —	$-t_{L3\_CLK}/4 + 0.5$ $t_{L3\_CLK}/4 + 1.0$	ns	5, 6, 7 5, 7
Output hold times: Data and parity All other outputs	t_{L3CHDX} and t_{L3CLDX} t_{L3CHOX}	$t_{L3\_CLK}/4 - 0.35$ $t_{L3\_CLK}/4 + 0.5$	— —	ns	5, 6, 7 5, 7
L3_CLK to high impedance: Data and parity All other outputs	t_{L3CLDZ} t_{L3CHOZ}	— —	$t_{L3\_CLK}/2$ $t_{L3\_CLK}/4 + 2.0$	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. $t_{L3\_ECHO\_CLK}/4$ is one-fourth the period of L3_ECHO_CLK*n*. This parameter indicates that the MPC7451 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.

Figure 9 shows the typical connection diagram for the MPC7451 interfaced to MSUG2 SRAMs such as the Motorola MCM64E836.

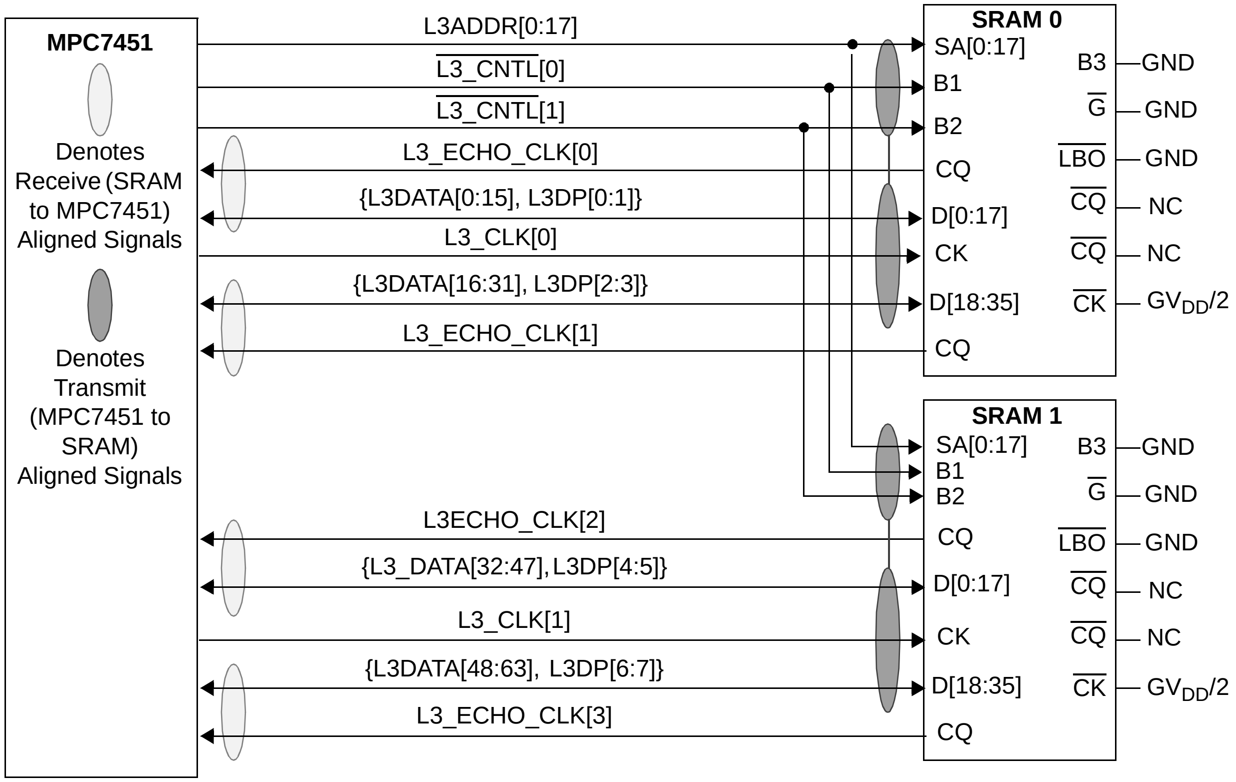
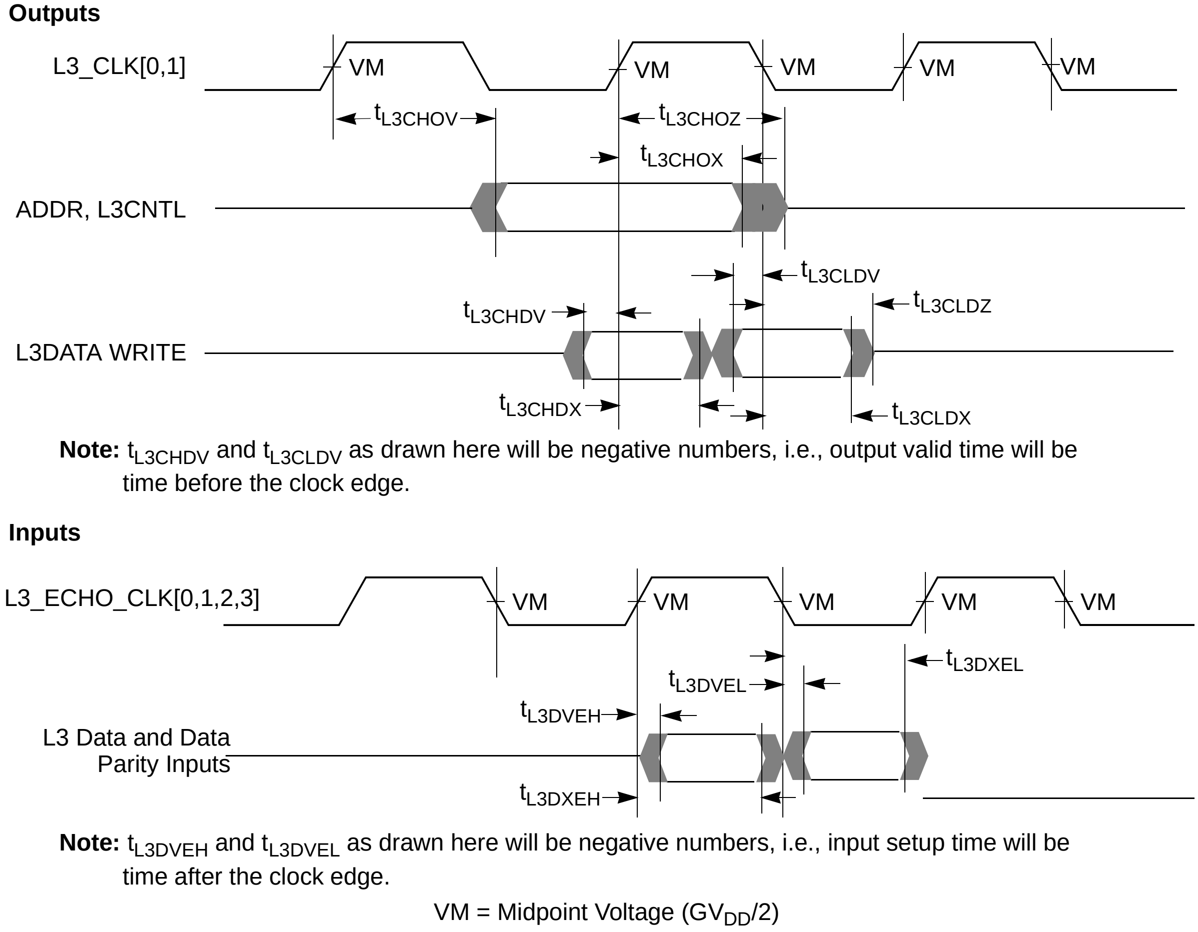


Figure 9. Typical Source Synchronous 2-Mbyte L3 Cache DDR Interface

Figure 10 shows the L3 bus timing diagrams for the MPC7451 interfaced to MSUG2 SRAMs.



Note: t_{L3CHDV} and t_{L3CLDV} as drawn here will be negative numbers, i.e., output valid time will be time before the clock edge.

Note: t_{L3DVEH} and t_{L3DVEL} as drawn here will be negative numbers, i.e., input setup time will be time after the clock edge.

VM = Midpoint Voltage ($GV_{DD}/2$)

Figure 10. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs

1.5.2.4.2 L3 Bus AC Specifications for PB2 and Late Write SRAMs

When using PB2 or Late Write SRAMs at the L3 interface, the parts should be connected as shown in Figure 11. These SRAMs are synchronous to the MPC7451; one L3_CLK*n* signal is output to each SRAM to latch address, control, and write data. Read data is launched by the SRAM synchronous to the delayed L3_CLK*n* signal it received. The MPC7451 needs a copy of that delayed clock which launched the SRAM read data to know when the returning data will be valid. Therefore, L3_ECHO_CLK1 and L3_ECHO_CLK3 must be routed halfway to the SRAMs and then returned to the MPC7451 inputs L3_ECHO_CLK0 and L3_ECHO_CLK2 respectively. Thus, L3_ECHO_CLK0 and L3_ECHO_CLK2 are phase-aligned with the input clock received at the SRAMs. The MPC7451 will latch the incoming data on the rising edge of L3_ECHO_CLK0 and L3_ECHO_CLK2.

Table 13 provides the L3 bus interface AC timing specifications for the configuration shown in Figure 11, assuming the timing relationships of Figure 12 and the loading of Figure 8.

Table 13. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR} and t_{L3CF}	—	1.0	ns	1, 5
Setup times:Data and parity	t_{L3DVEH}	1.5	—	ns	2, 5
Input hold times:Data and parity	t_{L3DXEH}	—	0.5	ns	2, 5
Valid times:Data and parity All other outputs	t_{L3CHDV} t_{L3CHOV}	— —	$t_{L3\_CLK}/4 + 1.0$ $t_{L3\_CLK}/4 + 1.0$	ns	3, 4, 5 4
Output hold times:Data and parity All other outputs	t_{L3CHDX} t_{L3CHOX}	$t_{L3\_CLK}/4 + 0.5$ $t_{L3\_CLK}/4 + 0.5$	— —	ns	3, 4, 5 4, 5
L3_CLK to high impedance:Data and parity All other outputs	t_{L3CHDZ} t_{L3CHOZ}	— —	2.0 2.0	ns	5 5

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
5. Timing behavior and characterization are currently being evaluated.

Figure 11 shows the typical connection diagram for the MPC7451 interfaced to PB2 SRAMs, such as the Motorola MCM63R737, or Late Write SRAMs, such as the Motorola MCM63R836A.

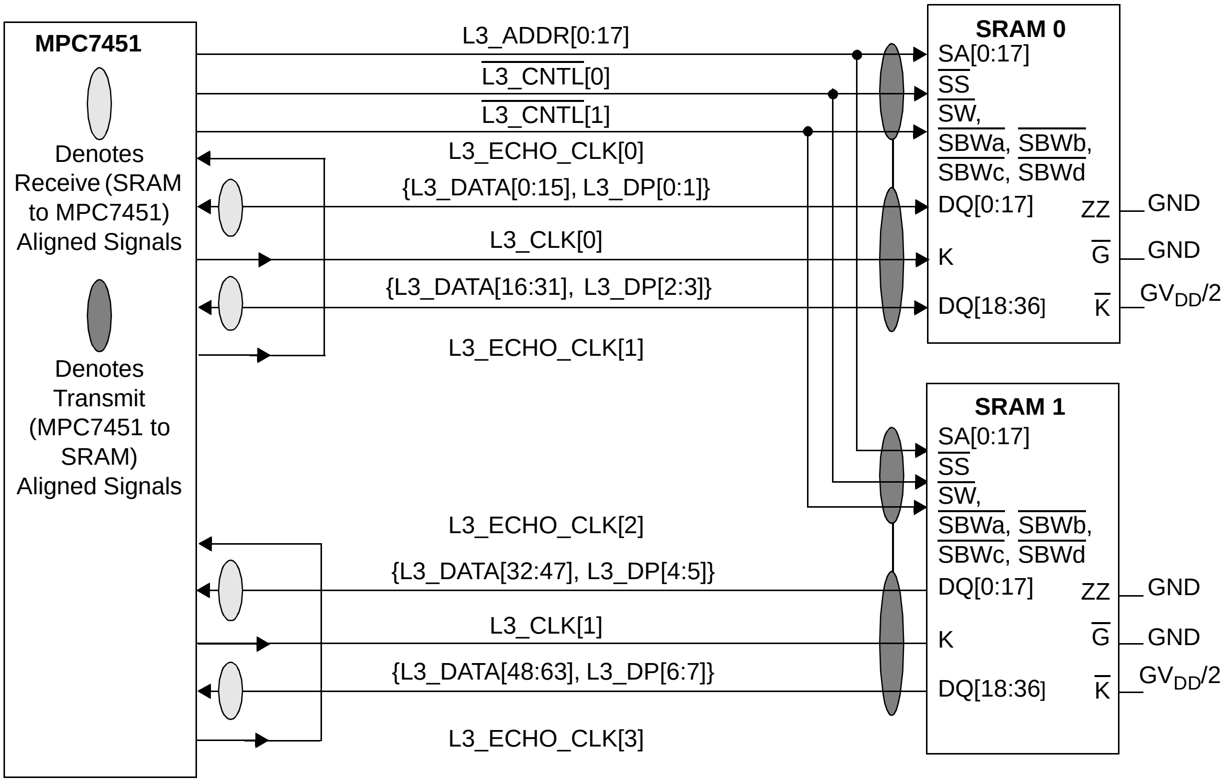


Figure 11. Typical Synchronous 1-MByte L3 Cache Late Write or PB2 Interface

Figure 12 shows the L3 bus timing diagrams for the MPC7451 interfaced to PB2 or Late Write SRAMs.

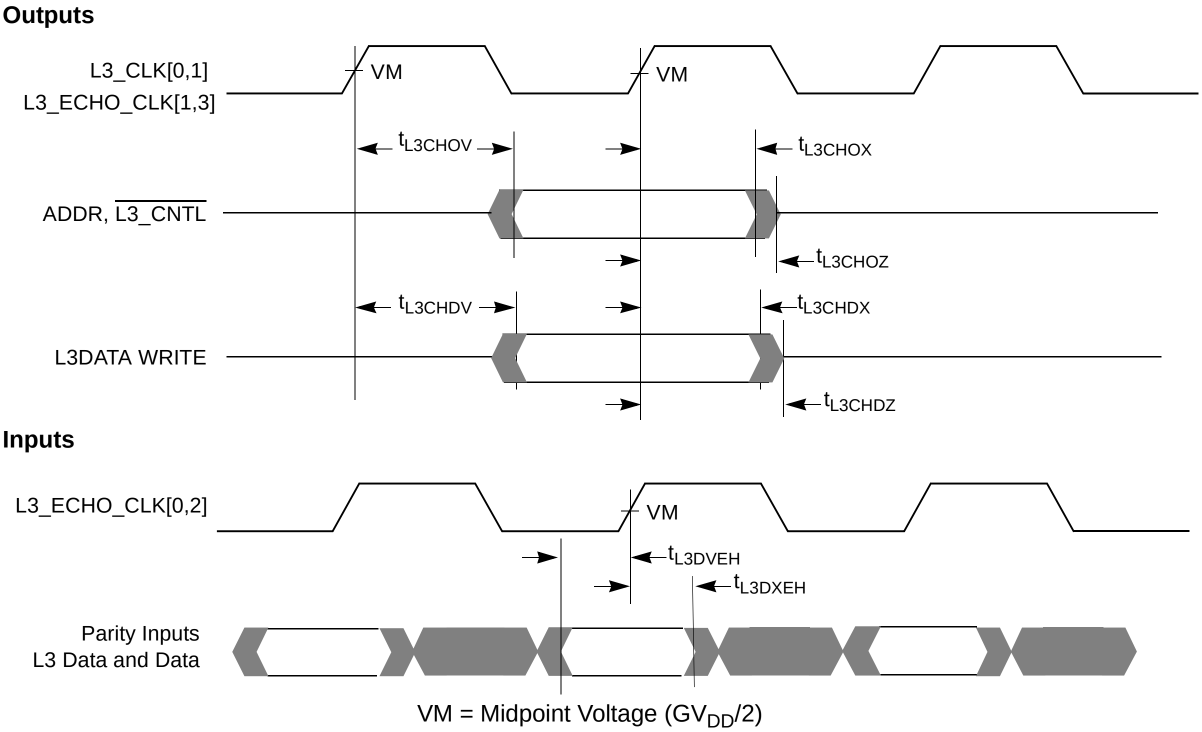


Figure 12. L3 Bus Timing Diagrams for Late Write or PB2 SRAMs

1.5.2.5 IEEE 1149.1 AC Timing Specifications

Table 14 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 14, Figure 15, Figure 16, and Figure 17.

Table 14. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	 3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	 3

Table 14. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times:				ns	
Boundary-scan data	t_{JLDV}	4	20		4
TDO	t_{JLOV}	4	25		
Output hold times:				ns	
Boundary-scan data	t_{JLDX}	TBD	TBD		4
TDO	t_{JLOX}	TBD	TBD		
TCK to output high impedance:				ns	
Boundary-scan data	t_{JLDZ}	3	19		4, 5
TDO	t_{JLOZ}	3	9		5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7451.

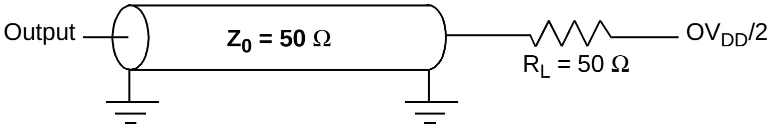


Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

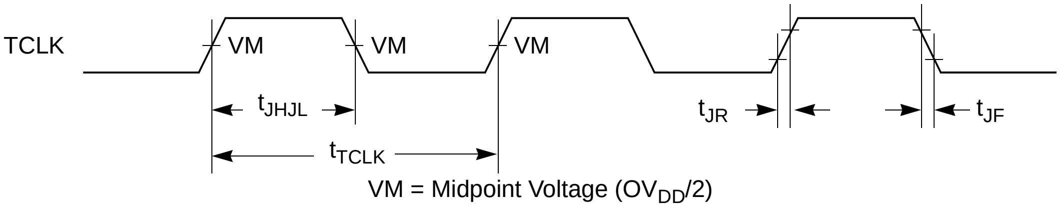


Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{TRST}$ timing diagram.

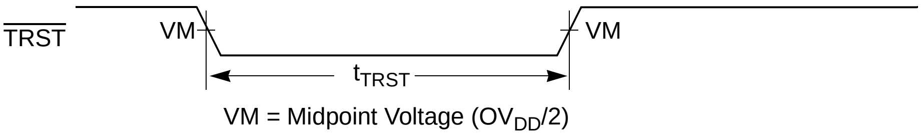


Figure 15. $\overline{TRST}$ Timing Diagram

Figure 16 provides the boundary-scan timing diagram.

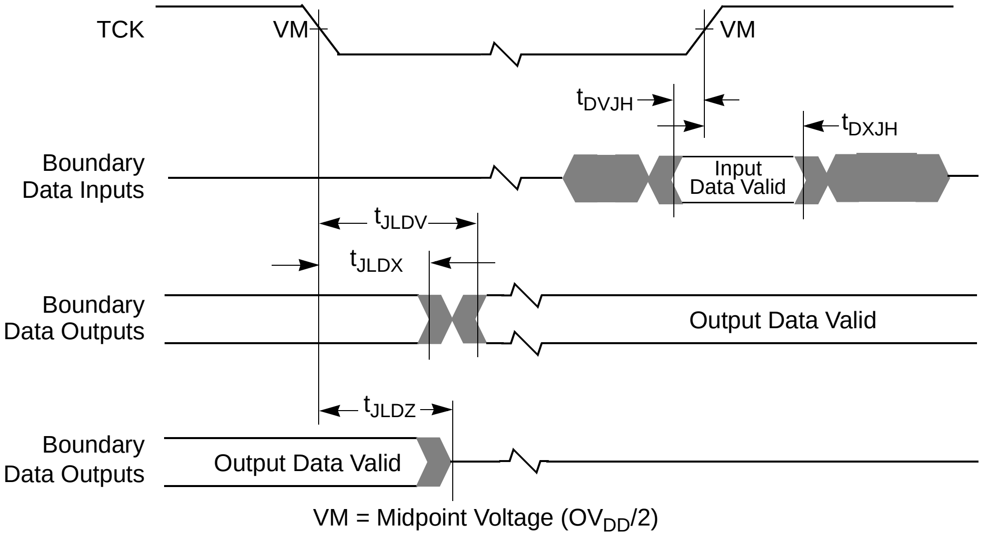


Figure 16. Boundary-Scan Timing Diagram

Figure 17 provides the test access port timing diagram.

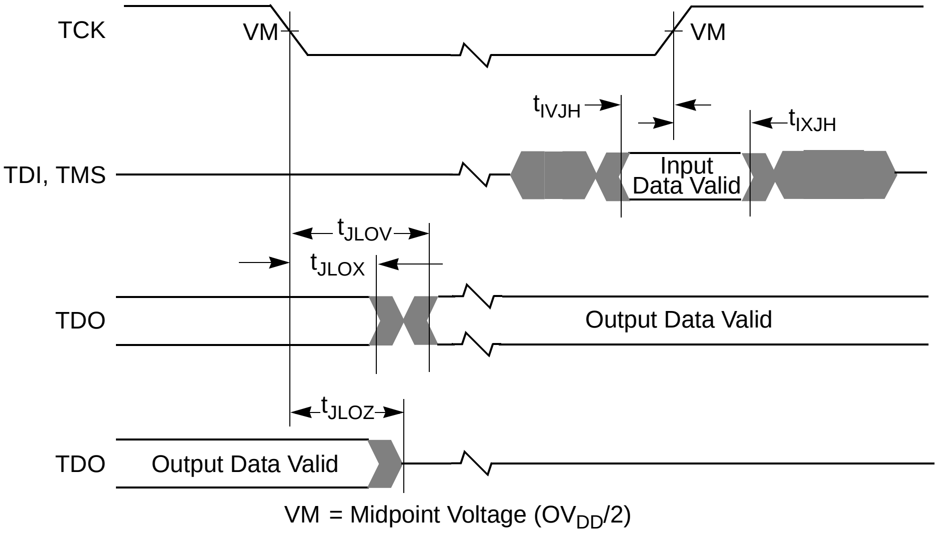
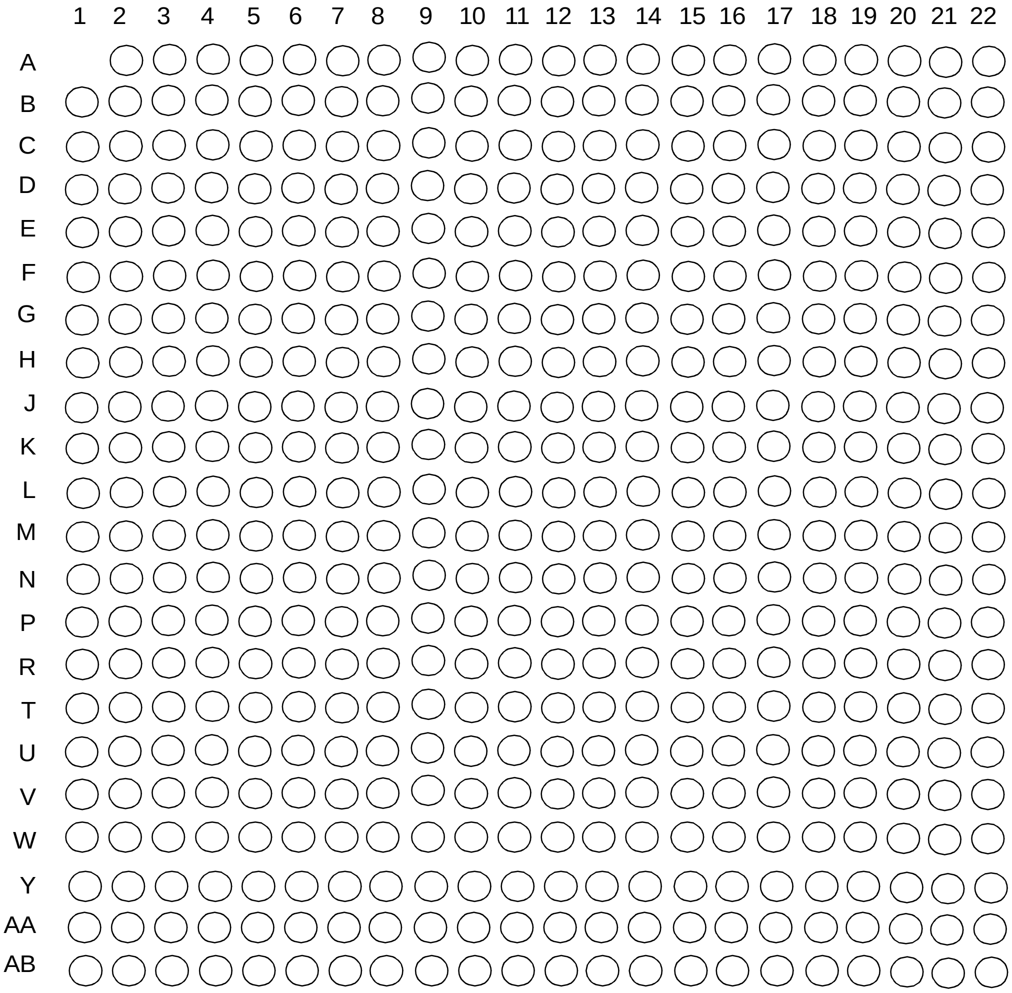


Figure 17. Test Access Port Timing Diagram

1.6 Pin Assignments

Figure 18 (in Part A) shows the pinout of the MPC7451, 483 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Not to Scale

Part B

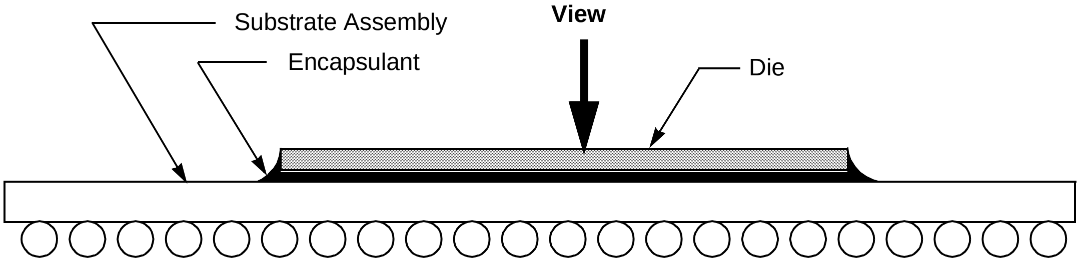


Figure 18. Pinout of the MPC7451, 483 CBGA Package as Viewed from the Top Surface

1.7 Pinout Listings for the 483 CBGA Package

Table 15 provides the pinout listing for the MPC7451, 483 CBGA package.

Table 15. Pinout Listing for the MPC7451, 483 CBGA Package

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
A[0:35]	E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9	High	I/O	BVSEL	11
$\overline{\text{AACK}}$	U1	Low	Input	BVSEL	
AP[0:4]	L5, L6, J1, H2, G5	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	T2	Low	I/O	BVSEL	8
AV$_{DD}$	B2	—	Input	N/A	
$\overline{\text{BG}}$	R3	Low	Input	BVSEL	
$\overline{\text{BMODE0}}$	C6	Low	Input	BVSEL	5
$\overline{\text{BMODE1}}$	C4	Low	Input	BVSEL	6
$\overline{\text{BR}}$	K1	Low	Output	BVSEL	
BVSEL	G6	High	Input	N/A	3, 7
$\overline{\text{CI}}$	R1	Low	Output	BVSEL	8
$\overline{\text{CKSTP\_IN}}$	F3	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	K6	Low	Output	BVSEL	
CLK_OUT	N1	High	Output	BVSEL	
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL	
$\overline{\text{DBG}}$	V1	Low	Input	BVSEL	
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL	
$\overline{\text{DRDY}}$	T6	Low	Output	BVSEL	4
DTI[0:3])	P2, T5, U3, P6	High	Input	BVSEL	4, 13
EXT_QUAL	B9	High	Input	BVSEL	9
$\overline{\text{GBL}}$	M4	Low	I/O	BVSEL	

Table 15. Pinout Listing for the MPC7451, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	—	—	N/A	
GV_{DD}	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	—	—	N/A	15
$\overline{\text{HIT}}$	K2	Low	Output	BVSEL	4
$\overline{\text{HRESET}}$	A3	Low	Input	BVSEL	
$\overline{\text{INT}}$	J6	Low	Input	BVSEL	
L1_TSTCLK	H4	High	Input	BVSEL	9
L2_TSTCLK	J2	High	Input	BVSEL	12
L3VSEL	A4	High	Input	N/A	3, 7
L3ADDR[0:17]	L18, K22, L16, K20, K18, J22, J20, H22, J18, K16, H20, G22, F22, G20, H18, E22, J16, F20	High	Output	L3VSEL	
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL	
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL	
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL	
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL	
L3_ECHO_CLK[0:3]	V18, P20, E18, E14	High	Input	L3VSEL	
$\overline{\text{LSSD\_MODE}}$	F6	Low	Input	BVSEL	2, 7
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL	
No Connect	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G11, G2, H11, H9, J8	—	—	N/A	

Table 15. Pinout Listing for the MPC7451, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	—	—	N/A	
PLL_CFG[0:3]	A2, F7, C2, D4	High	Input	BVSEL	
PLL_EXT	H8	High	Input	BVSEL	
$\overline{\text{PMON\_IN}}$	E6	Low	Input	BVSEL	10
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL	
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL	8
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL	
SYSCLK	D6	—	Input	BVSEL	
$\overline{\text{TA}}$	N8	Low	Input	BVSEL	
TBEN	L3	High	Input	BVSEL	
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL	
TCK	J7	High	Input	BVSEL	
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	2
TEST[6]	A9	—	Input	BVSEL	9
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 14
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	8
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	8

Table 15. Pinout Listing for the MPC7451, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals L3_CNTL[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To program the processor interface I/O voltage, connect BVSEL to either GND (selects 1.8 V) or to $\overline{\text{HRESET}}$ (selects 2.5 V). To program the L3 interface, connect L3VSEL to either GND (selects 1.8 V) or to $\overline{\text{HRESET}}$ (selects 2.5 V) or to $\overline{\text{HRESET}}$ (selects 1.5 V). If used, pulldown resistors should be less than 250 Ω.
4. Ignored in 60x bus mode.
5. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
6. This signal must be negated during reset, by pull-up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
7. Internal pull-up on die.
8. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7451 and other bus masters.
9. These input signals for factory use only and must be pulled down to GND for normal machine operation.
10. This pin can externally enable the performance monitor counters (PMC) if they are internally enabled by the software. If it will not be used to control the PMC, it should be pulled down to GND so that the software can enable the PMC.
11. Unused address pins must be pulled down to GND.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These signals must be pulled down to GND if unused or if the MPC7451 is in 60x bus mode.
14. This signal must be asserted during reset, by pull-down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.

1.8 Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

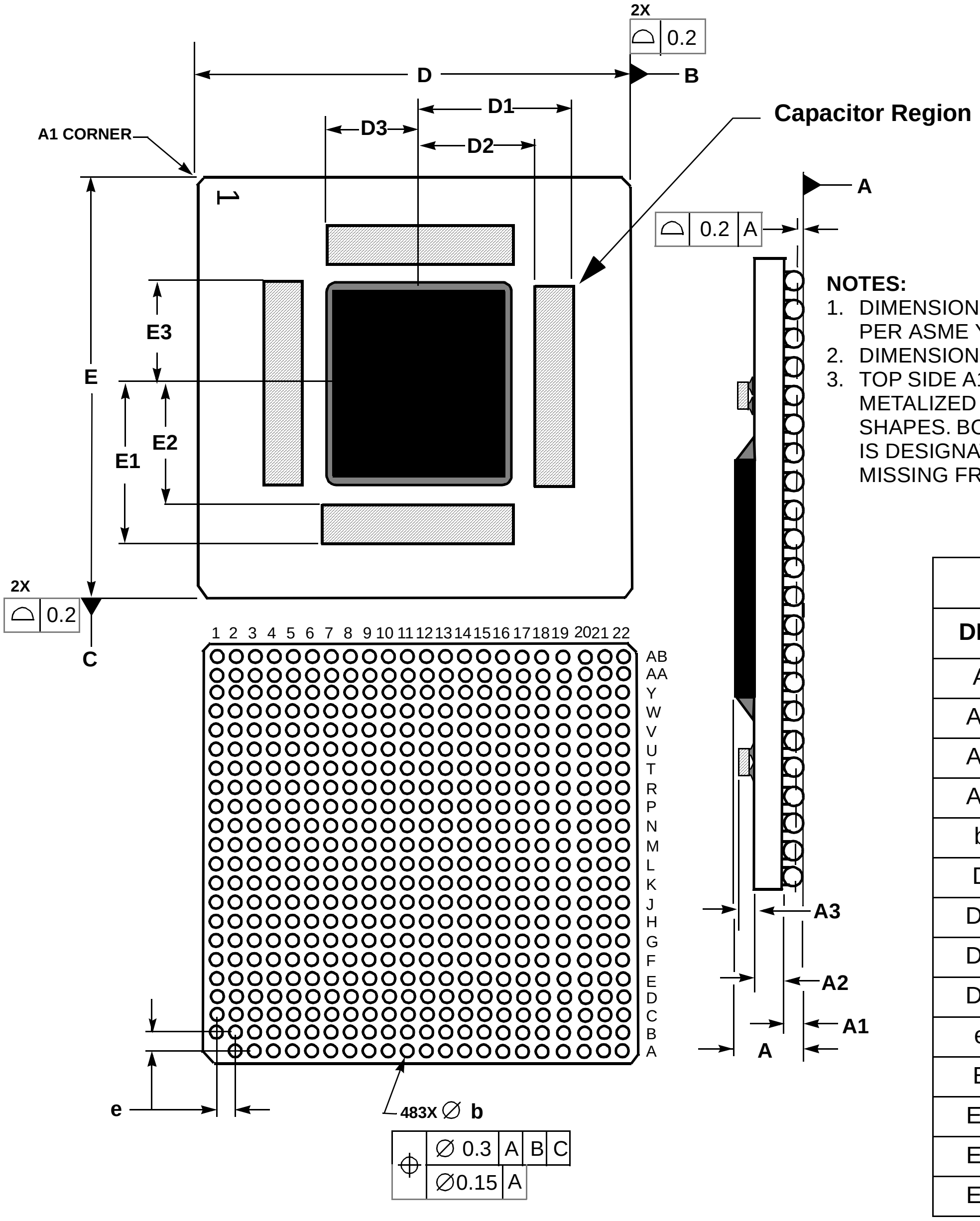
1.8.1 Package Parameters for the MPC7451, 483 CBGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483-lead ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

1.8.2 Mechanical Dimensions for the MPC7451, 483 CBGA

Figure 19 provides the mechanical dimensions and bottom surface nomenclature for the MPC7451, 483 CBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE. A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	MIN	MAX
A	--	3.22
A1	0.80	1.00
A2	1.08	1.32
A3	--	0.60
b	0.82	0.93
D	29.00 BSC	
D1	—	11.6
D2	8.94	—
D3	—	6.9
e	1.27 BSC	
E	29.00 BSC	
E1	—	11.6
E2	8.94	—
E3	—	6.9

Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7451, 483 CBGA

1.9 System Design Information

This section provides system and thermal design recommendations for successful application of the MPC7451.

1.9.1 PLL Configuration

The MPC7451 PLL is configured by the PLL_EXT and PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. PLL_EXT will normally be pulled low but can be asserted for extended modes of operation. The PLL configuration for the MPC7451 is shown in Table 16 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 600-MHz column in Table 8.

Table 16. MPC7451 Microprocessor PLL Configuration Example for 600 MHz Parts

PLL_EXT	PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
		Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83 MHz	Bus 100 MHz	Bus 133 MHz
0	0000	0.5x	2x	16 (33)	25 (50)	33 (66)	37 (75)	47 (83)	50 (100)	66 (133)
0	0100	2x	2x	66 (133)	100 (200)	133 (266)	150 (300)	166 (333)	200 (400)	266 (533)
0	0110	2.5x	2x	83 (166)	125 (250)	166 (333)	187 (375)	208 (415)	250 (500)	333 (666)
0	1000	3x	2x	100 (200)	150 (300)	200 (400)	225 (450)	250 (500)	300 (600)	400 (800)
0	1110	3.5x	2x	116 (233)	175 (350)	233 (466)	262 (525)	291 (581)	350 (700)	466 (933)
0	1010	4x	2x	133 (266)	200 (400)	266 (533)	300 (600)	333 (666)	400 (800)	533 (1066)
0	0111	4.5x	2x	150 (300)	225 (450)	300 (600)	337 (675)	374 (747)	450 (900)	600 (1200)
0	1011	5x	2x	166 (333)	250 (500)	333 (666)	375 (750)	415 (830)	500 (1000)	667 (1333)
0	1001	5.5x	2x	183 (366)	275 (550)	366 (733)	412 (825)	457 (913)	550 (1100)	733 (1466)
0	1101	6x	2x	200 (400)	300 (600)	400 (800)	450 (900)	498 (996)	600 (1200)	
0	0101	6.5x	2x	216 (433)	325 (630)	433 (866)	488 (975)	540 (1080)	650 (1300)	
0	0010	7x	2x	233 (466)	350 (700)	466 (933)	525 (1050)	581 (1162)	700 (1400)	
0	0001	7.5x	2x	250 (500)	375 (750)	500 (1000)	563 (1125)	623 (1245)	750 (1500)	
0	1100	8x	2x	266 (533)	400 (800)	533 (1066)	600 (1200)	664 (1328)		

Table 16. MPC7451 Microprocessor PLL Configuration Example for 600 MHz Parts (continued)

PLL_EXT	PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
		Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83 MHz	Bus 100 MHz	Bus 133 MHz
1	0111	9x	2x	300 (600)	450 (900)	600 (1200)	675 (1350)	747 (1494)		
1	1010	10x	2x	333 (666)	500 (1000)	667 (1333)	750 (1500)			
1	1001	11x	2x	366 (733)	550 (1100)	733 (1466)				
1	1011	12x	2x	400 (800	600 (1200)					
1	0101	13x	2x	433 (866)	650 (1300)					
1	1100	14x	2x	466 (933)	700 (1400)					
1	0001	15x	2x	500 (1000)	750 (1500)					
1	1101	16x	2x	533 (1066)						
0	0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly						
0	1111	PLL off		PLL off, no core clocking occurs						

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7451; see Section 1.5.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7451 regardless of the SYSCLK input.

The MPC7451 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the MPC7451. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC7451 core, and timing analysis of the circuit board routing. Table 17 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 17. Sample Core-to-L3 Frequencies

Core Frequency (MHz)	÷2	÷2.5	÷3	÷3.5	÷4	÷5	÷6
500	250	200	167	143	125	100	83
533	266	213	178	152	133	107	89
550	275	220	183	157	138	110	92
600	300	240	200	171	150	120	100
650[2]	325	260	217	186	163	130	108
666[2]	333	266	222	190	167	133	111
700[2]	350	280	233	200	175	140	117
733[2]	367	293	244	209	183	147	122

Notes:

1. The core and L3 frequencies are for reference only. Some examples may represent core or L3 frequencies which are not useful, not supported, or not tested for the MPC7451; see Section 1.5.2.3, "L3 Clock AC Specifications," for valid L3_CLK frequencies. (Shaded cells do not comply with Table 10.)
2. These core frequencies are not supported by all speed grades; see Table 8.

1.9.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7451 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 20 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint and very close to the periphery of the 483 CBGA footprint, without the inductance of vias.

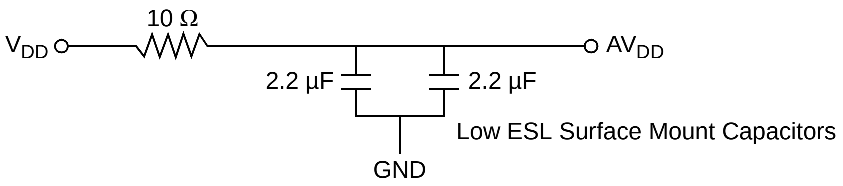


Figure 20. PLL Power Supply Filter Circuit

1.9.3 Power Supply Voltage Sequencing

The notes in Table 2 contain cautions about the sequencing of the external bus voltages and core voltage of the MPC7451 (when they are different). These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes will be forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 21 can be added to meet these requirements. The 30BF10 diodes (see Figure 21) control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

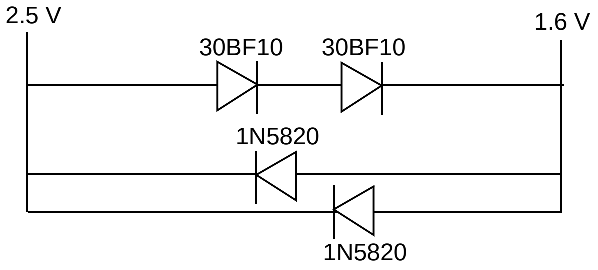


Figure 21. Example Voltage Sequencing Circuit

1.9.4 Decoupling Recommendations

Due to the MPC7451 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7451 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7451 system, and the MPC7451 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pin of the MPC7451. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}/GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Motorola microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, GV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.9.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, GV_{DD}, and GND pins in the MPC7451. If the L3 interface is not used, GV_{DD} should be connected to the OV_{DD} power phase, and L3VSEL should be connected to BVSEL.

1.9.6 Output Buffer DC Impedance

The MPC7451 processor bus and L3 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 22).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

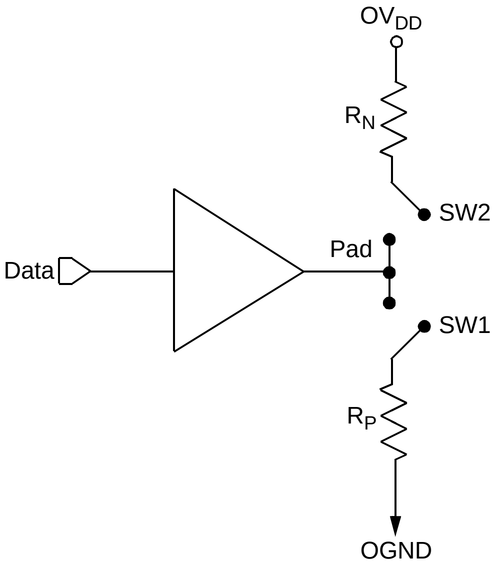


Figure 22. Driver Impedance Measurement

Table 18 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 18. Impedance Characteristics

V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5° –85°C

Impedance		Processor Bus	L3 Bus	Unit
Z_0	Typical	33–42	34–42	Ω
	Maximum	31–51	32–44	Ω

1.9.7 Pull-Up/Pull-Down Resistor Requirements

The MPC7451 requires high-resistive (weak: 4.7 kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7451 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being for factory test must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the MPC7451, 483 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:5]; the pins that must be pulled down are: L1_TSTCLK and TEST[6].

In addition, the MPC7451 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 kΩ–1 kΩ) if it is used by the system. This pin is CKSTP_OUT.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250 Ω (see Table 15).

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7451 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7451 or by other receivers in the system. It is recommended that these signals be pulled up through weak (4.7 kΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], CI, WT, and GBL.

If extended addressing is not used, A[0:3] are unused and must be be pulled low to GND through weak pull-down resistors. If the MPC7451 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors.

1.9.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

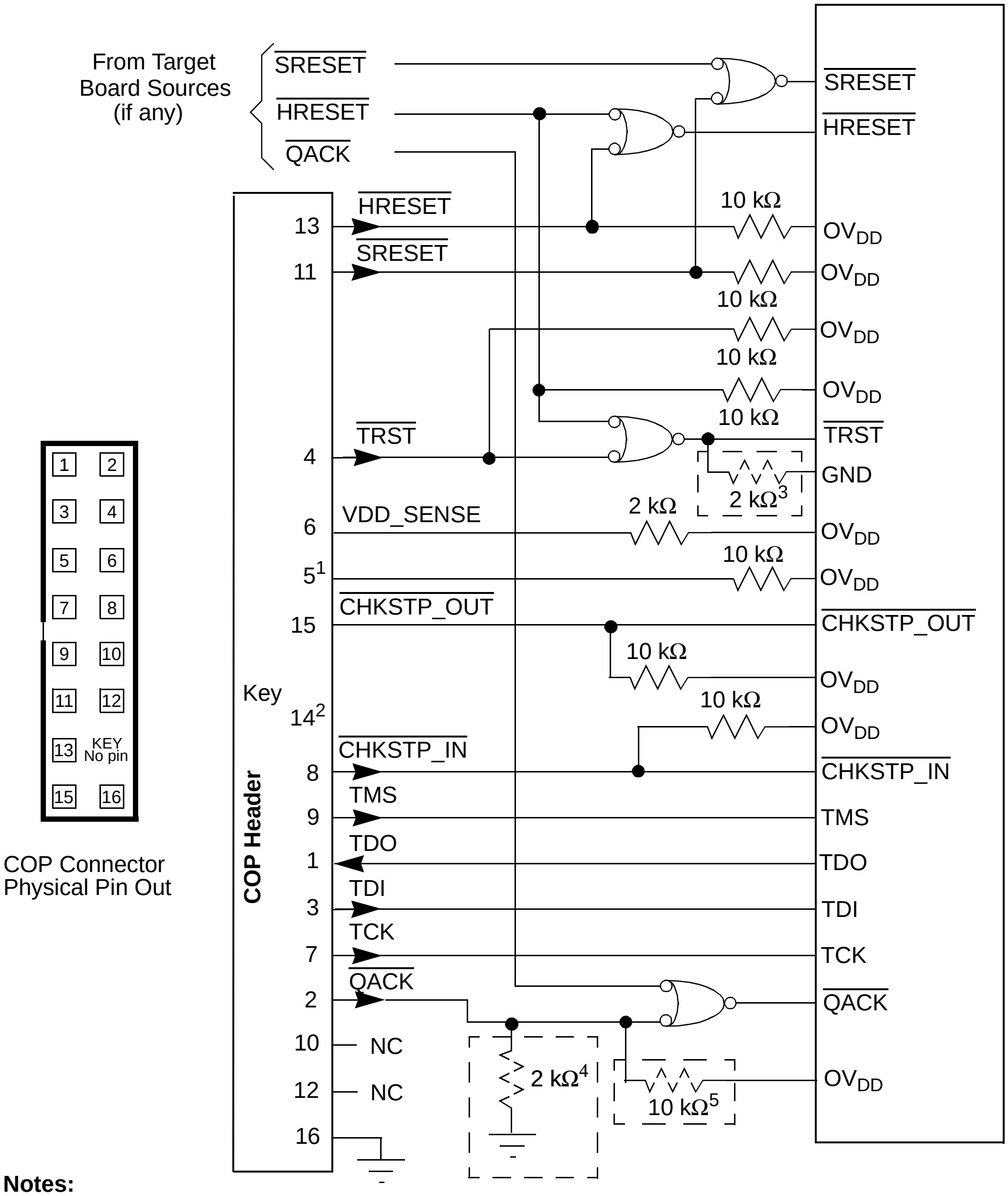
The arrangement shown in Figure 23 allows the COP to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well. An optional pull-down resistor on TRST can be populated to ensure that the JTAG scan chain is initialized during power-on if the JTAG interface and COP header will not be used; otherwise, this resistor should be unpopulated and TRST is asserted when the system reset signal (HRESET) is asserted and the JTAG interface is responsible for driving TRST when needed.

The COP header shown in Figure 23 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 23; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 23 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 23 is usually connected to the PCI bridge chip in a system and is an input to the MPC7451 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7451 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.



Notes:

1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC7450. Connect pin 5 of the COP header to OV_{DD} with a 10 KΩ pull-up resistor.
2. Key location; Pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if JTAG interface is unused.
4. Component not populated. Populate only if debug tool does not drive QACK.
5. Populate only if debug tool uses an open-drain type output and does not actively deassert QACK.

Figure 23. JTAG Interface Connection

1.9.9 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 24); however, due to the potential large mass of the heat sink, attachment through the printed circuit board is suggested. If a spring clip is used, the spring force should not exceed 5.5 pounds.

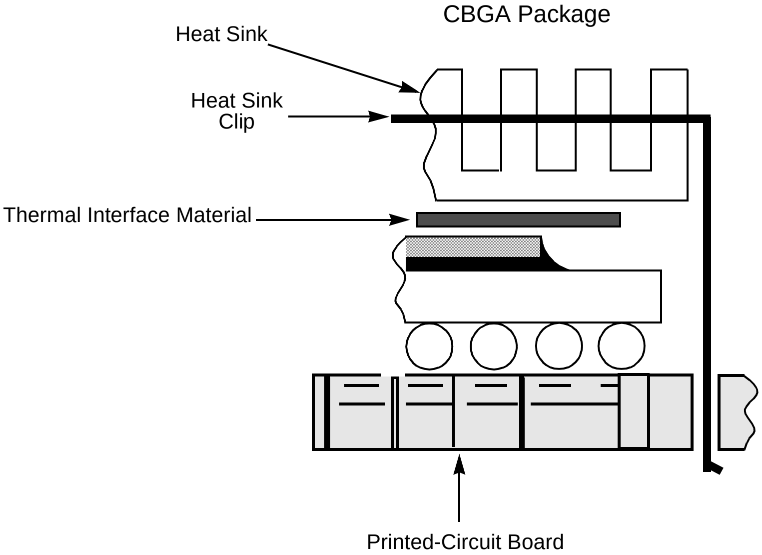


Figure 24. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC7451. There are several commercially available heat sinks for the MPC7451 provided by the following vendors:

Chip Coolers Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979 Internet: www.chipcoolers.com	800-227-0254 (USA/Canada) 401-739-7600
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Thermalloy 2021 W. Valley View Lane Dallas, TX 75234-8993 Internet: www.thermalloy.com	972-243-4321
Wakefield Engineering 100 Cummings Center, Suite 157H Beverly, MA 01915 Internet: www.wakefield.com	781-406-3000

Aavid Engineering 250 Apache Trail Terrell, TX 75160 Internet: www.aavid.com	972-551-7330
Cool Innovations Inc. 260 Spinnaker Way, Unit 8 Concord, Ontario L4K 4P9 Canada Internet: www.coolinnovations.com	905-760-1992

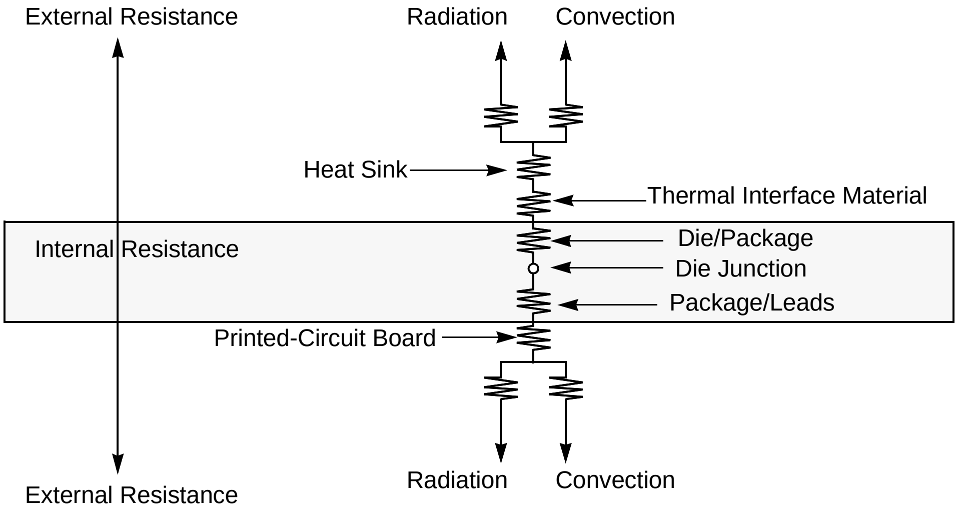
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.9.9.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 25 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 25. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

1.9.9.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 26 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 24). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the MPC7451. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

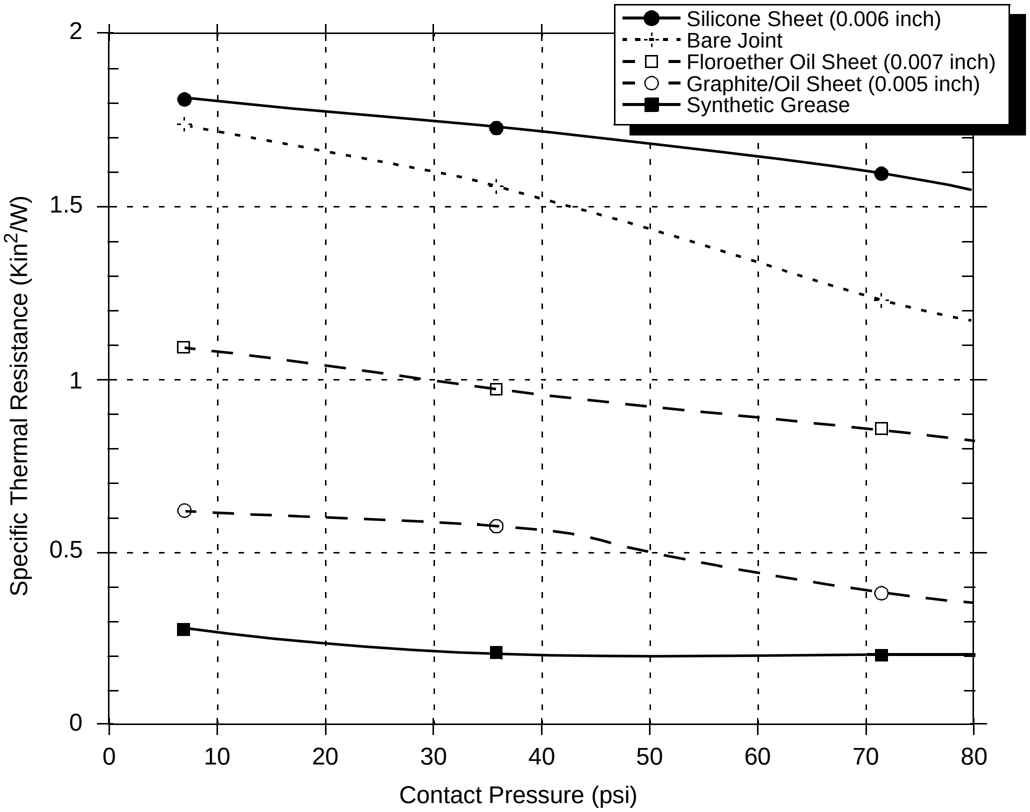


Figure 26. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
PO Box 0997
Midland, MI 48686-0997
Internet: www.dow.com

Chomerics, Inc. 781-935-4850
77 Dragon Court
Woburn, MA 01888-4014
Internet: www.chomerics.com

Thermagon Inc. 888-246-9050
3256 West 25th Street
Cleveland, OH 44109-1668
Internet: www.thermagon.com

Loctite Corporation 860-571-5100
1001 Trout Brook Crossing
Rocky Hill, CT 06067-3910
Internet: www.loctite.com

The following section provides a heat sink selection example using one of the commercially available heat sinks.

1.9.9.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1.5°C/W. For example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $\theta_{jc} = 0.1$, and a typical power consumption (P_d) of 13.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°\text{C} + 5°\text{C} + (0.1°\text{C/W} + 1.5°\text{C/W} + \theta_{sa}) \times 13.0\ \text{W}$

For this example, a θ_{sa} value of 3.7°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

1.10 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Document Revision History

Document Revision	Substantive Change(s)
Rev 0	Initial release.
Rev 0.1	Made final adjustments to document template.
	Changed “Full-on Mode” to “Full-Power Mode” and “Sleep - PLL disabled” to “Deep Sleep Mode” in Table 7 to be consistent with User’s Manual.
	Removed specifcation for Doze mode power since this is not tested (see Table 7, Note 4).
	Lowered t_{KHDV} in Table 9 to 2.5 ns.
	Removed Deep Sleep Mode-Max power specification since this is not tested.

1.11 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.11.1, “Part Numbers Fully Addressed by This Document.” Section 1.11.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.11.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Motorola part numbering nomenclature for the MPC7451. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision level code which refers to the die mask revision number.

Table 20. Part Numbering Nomenclature

XPC	**7451**	**RX**	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Package**	**Processor Frequency**[1]	**Application Modifier**	**Revision Level**
XPC[2]	7451	RX = CBGA	600 667	L: 1.6 V ± 50 mV 0 to 105°C	G: 2.3; PVR = 8000 0210

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by Part Number Specifications may support other maximum core frequencies.
2. The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document; see Table 21.

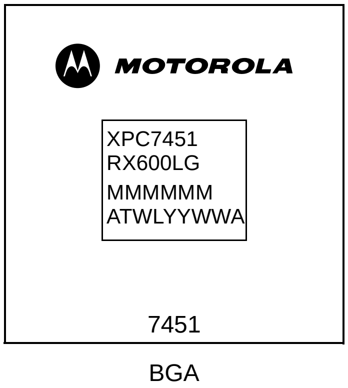
Table 21. Part Numbers with Separate Documentation

Part Number Series	**Operating Conditions**	**Document Order Number of Applicable Specification**
XPC7451RX*nnn*P*x*	1.9 V ± 50 mV, 0 to 65°C	MPC7451RXPXPNS/D

Note: For other differences, see applicable specifications.

1.11.3 Part Marking

Parts are marked as the example shown in Figure 27.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 27. Part Marking for BGA Device

Freescale Semiconductor, Inc.

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81-3-3440-3569

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