Freescale Semiconductor
Advance Information

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MPC7455 RISC Microprocessor Hardware Specifications Addendum for the XPC74*n*5RX*nnnn*LC Series

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7455 RISC Microprocessor Hardware Specifications* (Order No. MPC7455EC). The MPC7455 is a PowerPC™ microprocessor. The devices described in this specification are no longer in production and this document is provided for reference only. For recommended upgrades or replacement devices, contact your Freescale sales office.

Specifications provided in this document supersede those in the *MPC7455 RISC Microprocessor Hardware Specifications*, Rev. 1 or later, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.freescale.com or contact your Freescale sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Freescale Part Numbers Affected:

XPC7455RX600LC
XPC7455RX733LC
XPC7455RX800LC
XPC7455RX867LC
XPC7455RX933LC
PPC7455RX1000LC
XPC7445RX600LC
XPC7445RX733LC
XPC7445RX800LC
XPC7445RX867LC
XPC7445RX933LC
PPC7445RX1000LC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Part numbers addressed in this document are listed in Table A.

Table A. Part Numbers Addressed by This Data Sheet

Freescale Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency (MHz)	V_{DD}	T_J (°C)	
XPC7455RX600LC	600	1.6 V ± 50 mV	0 to 105	Modified core voltage, core and VCO frequency, and power specifications; modified PLL_CFG settings. This document describes all XPC74*n*5RX*nnnn*LC devices. Rev. 0 of the *MPC7455 RISC Microprocessor Hardware Specifications* originally described these devices but later revisions of that document describe only later devices.
XPC7455RX733LC	733			
XPC7455RX800LC	800			
XPC7455RX867LC	867			
XPC7455RX933LC	933			
PPC7455RX1000LC	1000			
XPC7445RX600LC	600			
XPC7445RX733LC	733			
XPC7445RX800LC	800			
XPC7445RX867LC	867			
XPC7445RX933LC	933			
PPC7445RX1000LC	1000			

Note: The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.1 Features

This section summarizes changes to the features of the MPC7455 described in the *MPC7455 RISC Microprocessor Hardware Specifications*.

- Power management
  - 1.6-V processor core

1.4 General Parameters

- Core power supply: 1.6 V ± 50 mV DC nominal

1.5.1 DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7455 part numbers described herein.

Table 4. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage	V_{DD}	1.6 V ± 50 mV	V
PLL supply voltage	AV_{DD}	1.6 V ± 50 mV	V

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption for the MPC7455 part numbers described herein.

Table 7. Power Consumption for MPC7455

	Processor (CPU) Frequency						Unit	Notes
	600 MHz	733 MHz	800 MHz	867 MHz	933 MHz	1 GHz		
Full-Power Mode								
Typical	13.0	15.6	17.0	18.5	19.9	21.3	W	1, 3
Maximum	17.5	22.0	24.0	26.0	28.0	30.0	W	1, 2
Doze Mode								
Typical	—	—	—	—	—	—	W	1, 3, 4
Nap Mode								
Typical	1.4	1.7	1.8	1.9	2.0	2.2	W	1, 3
Sleep Mode								
Typical	0.85	0.90	0.90	0.95	1.00	1.00	W	1, 3
Deep Sleep Mode (PLL Disabled)								
Typical	500	500	510	570	610	640	mW	1, 3

Notes:
1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} and GV_{DD} power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, with or without AltiVec™, maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 4) and 65°C in a system while running a typical code sequence.
4. Doze mode is not a user-definable state; it is an intermediate state between Full-Power and either Nap or Sleep mode. As a result, power consumption for this mode is not tested.

Table 8 provides the clock AC timing specificatons for the MPC7455 part numbers described herein.

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency												Unit	Notes
		600 MHz		733 MHz		800 MHz		867 MHz		933 MHz		1 GHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	500	600	500	733	500	800	500	867	500	933	500	1000	MHz	1
VCO frequency	f_{VCO}	1000	1200	1000	1466	1000	1600	1000	1734	1000	1866	1000	2000	MHz	1

Notes:

1. **Caution**: The SYSCLK frequency, PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies (see Table 4 in the *MPC7455 RISC Microprocessor Hardware Specifications*). Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.

Table 12 provides the L3 bus interface AC timing specifications for MSUG2 for the MPC7455 part numbers described herein.

Table 12. L3 Bus Interface AC Timing Specifications for MSUG2

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades				Unit	Notes
		L2CR[12] = 0 and L3CR[12] = 0[8]		L2CR[12] = 1 and L3CR[12] = 1[8]			
		Min	Max	Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	1.0	—	1.0	ns	1
Setup times: Data and parity	t_{L3DVEH}, t_{L3DVEL}	– 0.1	—	– 0.1	—	ns	2, 3, 4
Input hold times: Data and parity	t_{L3DXEH}, t_{L3DXEL}	$t_{L3\_ECHO\_CLK}/4$ + 0.6	—	$t_{L3\_ECHO\_CLK}/4$ + 0.6	—	ns	2, 4
Valid times: Data and parity	t_{L3CHDV}, t_{L3CLDV}	—	$(-t_{L3\_CLK}/4)$ + 0.4	—	$(-t_{L3\_CLK}/4)$ + 0.8	ns	5, 6, 7
Valid times: All other outputs	t_{L3CHOV}	—	$t_{L3\_CLK}/4$ + 1.0	—	$t_{L3\_CLK}/4$ + 1.2	ns	5, 7
Output hold times: Data and parity	t_{L3CHDX}, t_{L3CLDX},	$t_{L3\_CLK}/4$ – 0.4	—	$t_{L3\_CLK}/4$ – 0.2	—	ns	5, 6, 7
Output hold times: All other outputs	t_{L3CHOX}	$t_{L3\_CLK}/4$ – 0.5	—	$t_{L3\_CLK}/4$ – 0.3	—	ns	5, 7
L3_CLK to high impedance: Data and parity	t_{L3CLDZ}	—	$t_{L3\_CLK}/2$	—	$t_{L3\_CLK}/2$	ns	

Table 12. L3 Bus Interface AC Timing Specifications for MSUG2 (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades				Unit	Notes
		L2CR[12] = 0 and L3CR[12] = 0[8]		L2CR[12] = 1 and L3CR[12] = 1[8]			
		Min	Max	Min	Max		
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	$t_{L3\_CLK}/4 + 2.0$	—	$t_{L3\_CLK}/4 + 2.0$	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10 in the *MPC7455 RISC Microprocessor Hardware Specifications*). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10 in the *MPC7455 RISC Microprocessor Hardware Specifications*. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. $t_{L3\_ECHO\_CLK}/4$ is one-fourth the period of L3_ECHO_CLK*n*. This parameter indicates that the MPC7455 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8 in the *MPC7455 RISC Microprocessor Hardware Specifications*).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10 in the *MPC7455 RISC Microprocessor Hardware Specifications*. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. These configuration bits allow the AC timing of the L3 interface to be altered via software. They must be both set or both cleared; other configurations will increase $t_{L3CSKW1}$, which may cause unreliable L3 operation.

Table 13 provides the L3 bus AC timing specifications for PB2 and Late Write SRAMs for the MPC7455 part numbers described herein.

Table 13. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades				Unit	Notes
		L2CR[12]=0 and L3CR[12]=0 [6]		L2CR[12]=1 and L3CR[12]=1 [6]			
		Min	Max	Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	1.0	—	1.0	ns	1, 5
Setup times: Data and parity	t_{L3DVEH}	1.5	—	1.5	—	ns	2, 5
Input hold times: Data and parity	t_{L3DXEH}	—	0.5	—	0.5	ns	2, 5

Table 13. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Speed Grades				Unit	Notes
		L2CR[12]=0 and L3CR[12]=0 [6]		L2CR[12]=1 and L3CR[12]=1 [6]			
		Min	Max	Min	Max		
Valid times: Data and parity	t_{L3CHDV}	—	$t_{L3\_CLK}/4 + 1.0$	—	$t_{L3\_CLK}/4 + 1.2$	ns	3, 4, 5
Valid times: All other outputs	t_{L3CHOV}	—	$t_{L3\_CLK}/4 + 1.0$	—	$t_{L3\_CLK}/4 + 1.2$	ns	4
Output hold times: Data and parity	t_{L3CHDX}	$t_{L3\_CLK}/4 - 0.4$	—	$t_{L3\_CLK}/4 - 0.2$	—	ns	3, 4, 5
Output hold times: All other outputs	t_{L3CHOX}	$t_{L3\_CLK}/4 - 0.4$	—	$t_{L3\_CLK}/4 - 0.2$	—	ns	4, 5
L3_CLK to high impedance: Data and parity	t_{L3CHDZ}	—	2.0	—	2.0	ns	5
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	2.0	—	2.0	ns	5

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10 in the *MPC7455 RISC Microprocessor Hardware Specifications*). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10 in the *MPC7455 RISC Microprocessor Hardware Specifications*).
4. $t_{L3\_CLK}/4$ is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock prior to the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
5. Timing behavior and characterization are currently being evaluated.
6. These configuration bits allow the AC timing of the L3 interface to be altered via software. They must be both set or both cleared; other configurations will increase $t_{L3CSKW1}$ and $t_{L3CSKW2}$, which may cause unreliable L3 operation.

1.9.1 PLL Configuration

The MPC7455 PLL is configured by the PLL_CFG[0:4] signals; note that PLL_CFG[4] was formerly called PLL_EXT in earlier documentation. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. PLL_CFG[4] will normally be pulled low but can be asserted for extended modes of operation. The PLL configuration for the MPC7455 is shown in Table 17 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1-GHz column in Table 8. Note that the settings for Rev. C devices are different than those for subsequent devices.

Table 17. MPC7455 Microprocessor PLL Configuration Example for 1 GHz Parts

PLL_CFG [0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83 MHz	Bus 100 MHz	Bus 133 MHz
00000	0.5x	2x							
01000	2x	2x							
01100	2.5x	2x							
10000	3x	2x							
11100	3.5x	2x							
10100	4x	2x							533 (1066)
01110	4.5x	2x							600 (1200)
10110	5x	2x						500 (1000)	667 (1333)
10010	5.5x	2x						550 (1100)	733 (1466)
11010	6x	2x						600 (1200)	800 (1600)
01010	6.5x	2x					540 (1080)	650 (1300)	866 (1730)
00100	7x	2x				525 (1050)	580 (1160)	700 (1400)	933 (1866)
00010	7.5x	2x			500 (1000)	563 (1125)	623 (1245)	750 (1500)	1000 (2000)
11000	8x	2x			533 (1066)	600 (1200)	664 (1328)	800 (1600)	
01111	9x	2x			600 (1200)	675 (1350)	747 (1494)	900 (1800)	
10101	10x	2x		500 (1000)	667 (1333)	750 (1500)	830 (1660)	1000 (2000)	
10011	11x	2x		550 (1100)	733 (1466)	825 (1650)	913 (1826)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)		

Table 17. MPC7455 Microprocessor PLL Configuration Example for 1 GHz Parts (continued)

PLL_CFG [0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83 MHz	Bus 100 MHz	Bus 133 MHz
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)			
11001	14x	2x		700 (1400)	933 (1866)				
00011	15x	2x	500 (1000)	750 (1500)	1000 (2000)				
11011	16x	2x	533 (1066)	800 (1600)					
00110	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly						
11110	PLL off		PLL off, no core clocking occurs						

1.11 Ordering Information

1.11.1 Part Numbers Addressed by This Specification

Table 21 provides the ordering information for the MPC7455 parts described in this document.

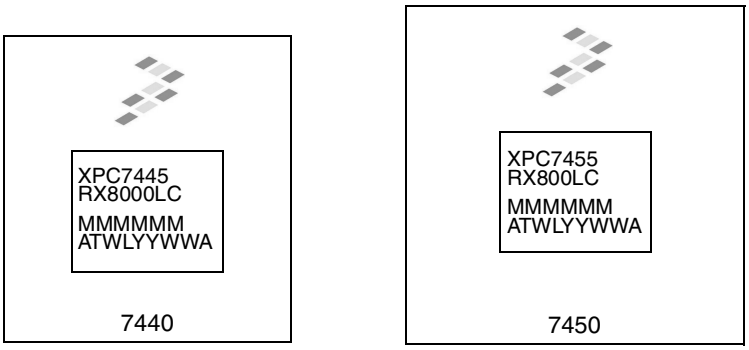
Table 21. Part Marking Nomenclature

XPC	74*n*5	RX	*nnnn*	*x*	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency [1]**	**Application Modifier**	**Revision Level**
XPC [2]	7455 7445	RX = CBGA	600 733 800 867 933	L: 1.6 V ± 50 mV 0 to 105°C	C: 2.1; PVR = 8001 0201
PPC [3]			1000		

Notes:
1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
3. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.11.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Freescale Part Marking for CBGA Device

Document Revision History

Table B provides a revision history for this hardware specification addendum.

Table B. Document Revision History

Rev. No.	Date	Editor/ Writer	Substantive Change(s)
0.1	07/19/2005	NB	Changed document order number (was MPC7455RXLCPNS, Rev. 0). Updated to Freescale template.
0	01/2003	NB/ME	Initial release.

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