DC ELECTRICAL CHARACTERISTI

MOTOROLA

CHARACTERISTIC
Input High Voltage (for JTAG and GPIO)
Input High Voltage (all other pins)
Input Low Voltage
EXTAL and EXTCLK Input High Voltage
Input Leakage Current, V_{IN} = 5.5 V
Hi-z (Off State) Leakage Current, V_{IN} = 3.5V
Signal Low Input Current, V_{IL} = 0.8 V
Signal High Input Current, V_{IH} = 2.0 V
Output High Voltage, I_{OH} = –2.0 mA, V_{DDH} = 3.0V Except XTAL, XFC, and Open-Drain Pins
Output Low Voltage IOL = 2.0 mA CLKOUT IOL = 3.2 mAA[6:31], TSIZ0/REG, TSIZ1, D(0:31), DP[(RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IF VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, USBRXD/PA1 PA13, SMRXD2/L1TXDA/PA9, SMTXD2/L1RXDA/PA8 SPKROUT, TIN1/L1RCLKA/BRGO1/CLK1/PA7, TIN3/ CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TIN4/T PA4, LCD_A/SPISEL/PB31, SPICLK/TXD3/PB30, SPII PB29, BRGO3/SPIMISO/PB28, BRGO1/I2CSDA/PB27 I2CSCL/PB26, SMTXD1/TXD3/PB25, SMRXD1/RXD3/ SMSYN1/SDACK1/CTS3/PB23, SMSYN2/SDACK2/PB L1ST1/PB19, L1ST2/RTS2/PB18, LCD_C/L1ST3/PB17 L1RQA/PB16, L1ST5/DREQ1/PC15, L1ST6/RTS2/DRI L1ST7/RTS3/PC13, L1ST8/L1RQA/PC12, USBRXP/PC USBRXN/TGATE1/PC10, CTS2/PC9, TGATE1/CD2/PC PC7, USBTXN/PC6, SDACK1/L1TSYNCA/PC5, L1RS PC4, LD8/VD7/PD15, LD7/VD6/PD14, LD6/VD5/PD13 PD12, LD4/VD3/PD11, LD3/VD2/PD10, LD2/VD1/PD9 PD8, FRAME/VSYNC/PD5, LCD_AC/LOE/BLANK/PD6 FIELD/PD7, LOAD/HSYNC/PD4, SHIFT/CLK/PD3
IOL = 5.3 mABDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0 CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_A WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/(GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UP GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DS OP2/MODCK1/STS, OP3/MODCK2/DSDO IOL = 7.0 mA USBOE/PA14, TXD2/PA12 IOL = 8.9 mATS, TA, TEA, BI, BB, HRESET, SRESET

NOTE: Input pin voltage specifications are V_{CC} = +4 V
AC timings are based on a 50 pf load.
If you are using Mask Revision Base #F98S, a

MPC823 Electrical Specif

This document contains detailed information
characteristics, and AC timing specifications

Note: Visit our website at www.m
than 25, 40, or 50MHz. Ou
calculate the timing for you

This device contains circuitry protecting agai
fields. However, it is advised that precaution
higher than the maximum-rated voltages to th
is enhanced if unused inputs are tied to an a

MAXIMUM RATINGS (GND = 0V)

RATING
Supply Voltage
Input Voltage (JTAG and GPIO)
Input Voltage (All other pins)
Operating Temperature
Storage Temperature Range

NOTES:

1. Functional operating conditions are **= 3.0 - 3.6 V)**. Absolute maximum r at the maxima is not guaranteed. S cause permanent damage to the d
2. **CAUTION**: The JTAG and GPIO inp supply voltage, this restriction appl
3. 5 Volt friendly inputs are inputs tha
4. If you are using Mask Revision Base are 5V tolerant inputs.

THERMAL CHARACTERISTICS

CHARACTERISTIC
Thermal Resistance for BGA

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in

$$T_J = T_A + (P_D \bullet q_{JA}) \qquad (1)$$

where

T_A = Ambient Temperature, ∞
q_{JA} = Package Thermal Resis
P_D = $P_{INT} + P_{I/O}$
P_{INT} = I_{DD} x V_{DD}, Watts—Chip I
$P_{I/O}$ = Power Dissipation on In

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can relationship between P_D and T_J is:

$$P_D = K \prod (T_J + 273 \infty C) \qquad (2)$$

Solving equations (1) and (2) for K gives

$$K = P_D \bullet (T_A + 273 \infty C) + q_{JA}$$

where K is a constant pertaining to the partic by measuring P_D (at equilibrium) for a known can be obtained by solving equations (1) and

Layout Practices

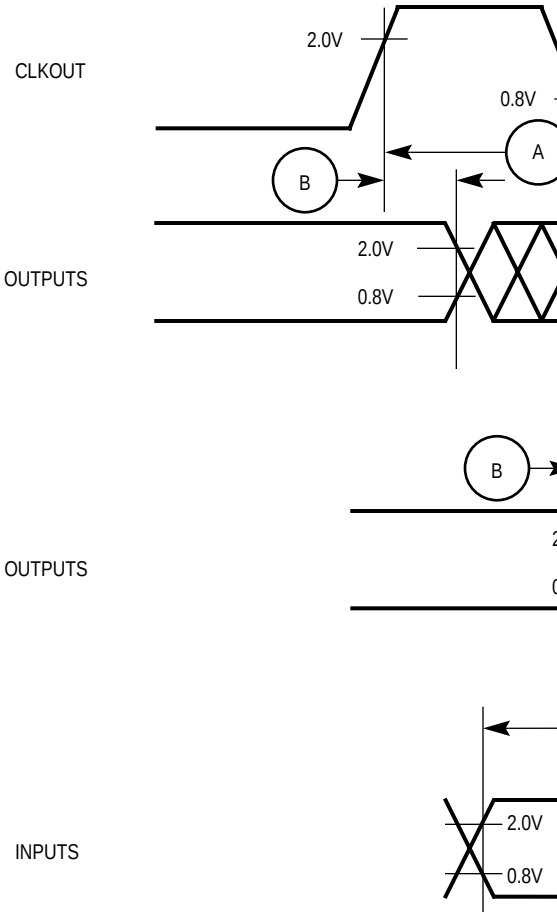
Each V_{CC} pin on the MPC823 should be prov supply. Each GND pin should be provided w supply pins drive distinct groups of logic on c ground using at least four 0.1 µF bypass cap sides of the package. The capacitor leads ar chip V_{CC} and GND should be kept to less tha board that employs two inner layers as V_{CC} a

All output pins on the MPC823 have fast rise interconnection length should be minimized caused by these fast output switching times. address and data busses. Maximum PC trac Capacitance calculations should consider all due to the PC traces. Attention to proper PCB in systems with higher capacitive loads beca in the V_{CC} and GND circuits. Pull up all unuse Special care should be taken to minimize the

Table 1. Bus Opera

NUM	CHARACTERISTIC
B28c	CLKOUT Falling Edge to $\overline{WE}$(0:3) Negated -GPCM Access TRLX = '0', CSNT = '1', EBDF=1
B28d	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Wri TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', E
B29	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM Access, CSNT = '0'
B29a	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM Access, TRLX = '0', CSNT = '1', EBDF = 0
B29b	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Writ ACS = '00', TRLX = '0' & CSNT = '0'
B29c	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Writ TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', E
B29d	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM Access, TRLX = '1', CSNT = '1', EBDF = 0
B29e	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Writ TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', E
B29f	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM Access, TRLX = '0', CSNT = '1', EBDF = 1
B29g	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Writ TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', E
B29h	$\overline{WE}$(0:3) Negated to D(0:31), DP(0:3) Hi Z -GPCM Access, TRLX = '1', CSNT = '1', EBDF = 1
B29i	$\overline{CS}$ Negated to D(0:31), DP(0:3) Hi Z -GPCM- Writ TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', E
B30	$\overline{CS}$, $\overline{WE}$(0:3) Negated to A(6:31) invalid -GPCM- V Access.
B30a	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write TRLX='0', CSNT = '1', CS Negated to A(6:31) Inval Write Access, TRLX='0', CSNT = '1', ACS = 10,AC EBDF = 0
B30b	$\overline{WE}$(0:3) Negated to A(6:31)Invalid -GPCM- Write TRLX='1', CSNT = '1', CS Negated to A(6:31)Inval Write Access, TRLX='1', CSNT = '1', ACS = 10,AC EBDF = 0
B30c	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write TRLX='0', CSNT = '1', CS Negated to A(6:31) Inval Write Access, TRLX='0', CSNT = '1', ACS = 10 ,AC EBDF = 1
B30d	$\overline{WE}$(0:3) Negated to A(6:31) Invalid -GPCM- Write TRLX='1', CSNT = '1', CS Negated to A(6:31) Inval Write Access, TRLX='1', CSNT = '1', ACS = 10,AC EBDF = 1
B31	CLKOUT Falling Edge to $\overline{CS}$ valid as requested by the corresponding word of the UPM

AC ELECTRICAL CHARACTERISTIC



A = MAXIMUM OUTPUT DELAY SPECIFICATION
B = MINIMUM OUTPUT HOLD TIME

EXTERNAL BUS ELECTRICAL CHA

Table 1. Bus

NUM	CHARACTERISTIC
B1	CLKOUT Period
B1a	EXTCLK to CLKOUT Phase Skew (EXTCLK>15M MF ≤ 2)
B1b	EXTCLK to CLKOUT Phase Skew (EXTCLK>10M MF ≤ 10)
B1c	CLKOUT Phase Jitter (EXTCLK>15MHz and MF≤
B1d	CLKOUT Phase Jitter (EXTCLK>10MHz and MF≤
B1e	CLKOUT Frequency Jitter (MF<10)
B1f	CLKOUT Frequency Jitter (10<MF<500)
B1g	CLKOUT Frequency Jitter (MF>500)
B1h	Frequency Jitter on EXTCLK
B2	Clock Pulse Width Low
B3	Clock Pulse Width High
B4	CLKOUT Rise Time
B5	CLKOUT Fall Time
B6	N/A (Used on Interactive Spreadsheet)
B7	CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP Invalid
B7a	CLKOUT to TSIZ(0:1),REG, RSV, AT(0:3),BDIP, P
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2), IW LWP(0:1), STS Invalid
B8	CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP
B8a	CLKOUT to TSIZ(0:1),REG, RSV, AT(0:3), BDIP,
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2) LWP(0:1), STS Valid
B9	CLKOUT to A(6:31), RD/WR, BURST, D(0:31), DP TSIZ(0:1),REG, RSV, AT(0:3), PTR Hi Z
B10	N/A
B11	CLKOUT to TS, BB Assertion
B11a	CLKOUT to TA, BI Assertion (when driven by the Memory Controller or PCMCIA Interface)
B12	CLKOUT to TS, BB Negation
B12a	CLKOUT to TA, BI Negation (when driven by the Memory Controller or PCMCIA Interface)
B13	CLKOUT to TS, BB Hi Z

Table 1. Bus Opera

NUM	CHARACTERISTIC
B13a	CLKOUT to TA, BI Hi Z (When Driven by the Mem Controller or PCMCIA Interface)
B14	CLKOUT to TEA Assertion
B15	CLKOUT to TEA Hi Z
B16	TA, BI Valid to CLKOUT (Setup Time)
B16a	TEA, KR, RETRY Valid to CLKOUT (Setup Time)
B16b	BB, BG, BR Valid to CLKOUT (Setup Time)
B17	CLKOUT to TA, TEA, BI , BB, BG, BR Valid (Hold
B17a	CLKOUT to KR, RETRY Valid (Hold Time)
B18	D(0:31), DP(0:3) Valid to CLKOUT Rising Edge (S
B19	CLKOUT Rising Edge to D(0:31), DP(0:3) Valid (H
B20	D(0:31), DP(0:3) Valid to CLKOUT Falling Edge (Se
B21	CLKOUT Falling Edge to D(0:31), DP(0:3) Valid (H
B22	CLKOUT Rising Edge to CS Asserted -GPCM- AC
B22a	CLKOUT Falling Edge to CS Asserted -GPCM- AC TRLX = 0
B22b	CLKOUT Falling Edge to CS Asserted -GPCM- AC TRLX = 0, EBDF = 0
B22c	CLKOUT Falling Edge to CS Asserted -GPCM- AC TRLX = 0, EBDF = 1
B23	CLKOUT Rising Edge to CS Negated -GPCM-Rea GPCM-Write Access, ACS=00, TRLX=0, CSNT=0
B24	A(6:31) to CS Asserted -GPCM- ACS = 10, TRLX
B24a	A(6:31) to CS Asserted -GPCM- ACS = 11, TRLX
B25	CLKOUT Rising Edge to OE, WE(0:3) Asserted
B26	CLKOUT Rising Edge to OE Negated
B27	A(6:31) to CS Asserted -GPCM- ACS = 10, TRLX
B27a	A(6:31) to CS Asserted -GPCM- ACS = 11, TRLX
B28	CLKOUT Rising Edge to WE(0:3) Negated -GPCM Access CSNT = '0'
B28a	CLKOUT Falling Edge to WE(0:3) Negated -GPCM Access TRLX = '0', CSNT = '1', EBDF=0
B28b	CLKOUT Falling Edge to CS Negated -GPCM-Wri TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', E

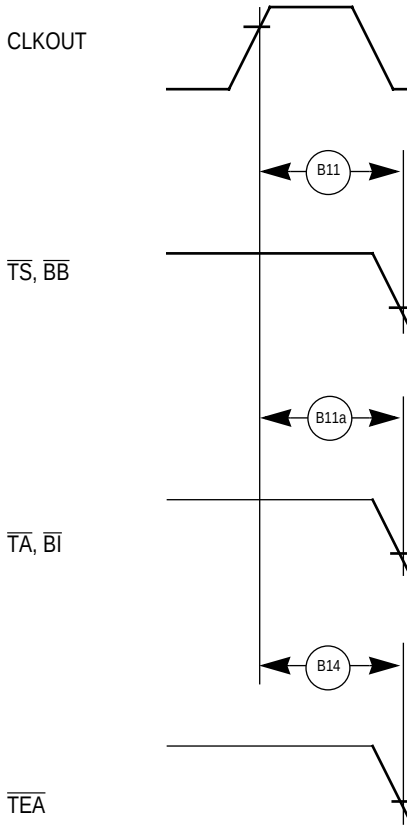


Figure 3. Synchronous A Outputs Signa

Table 1. Bus Opera

NUM	CHARACTERISTIC
B31a	CLKOUT Falling Edge to CS valid as requested by the corresponding word of the UPM, EBDF = 0
B31b	CLKOUT Rising Edge to CS valid as requested by the corresponding word of the UPM
B31c	CLKOUT Rising Edge to CS valid as requested by the corresponding word of the UPM
B31d	CLKOUT Falling Edge to CS valid as requested by the corresponding word of the UPM, EBDF = 1
B32	CLKOUT Falling Edge to BS valid as requested by the corresponding word of the UPM
B32a	CLKOUT Falling Edge to BS valid as requested by the corresponding word of the UPM, EBDF = 0
B32b	CLKOUT Rising Edge to BS valid as requested by E corresponding word of the UPM
B32c	CLKOUT Rising Edge to BS valid as requested by E corresponding word of the UPM
B32d	CLKOUT Falling Edge to BS valid as requested by the corresponding word of the UPM, EBDF = 1
B33	CLKOUT Falling Edge to GPL valid as requested b the corresponding word of the UPM
B33a	CLKOUT Rising Edge to GPL valid as requested b the corresponding word of the UPM
B34	A(6:31) and D(0:31) to CS valid as requested by C corresponding word of the UPM
B34a	A(6:31) and D(0:31) to CS valid as requested by C corresponding word of the UPM
B34b	A(6:31) and D(0:31) to CS valid as requested by C corresponding word of the UPM
B35	A(6:31) and D(0:31) to BS valid as requested by B corresponding word of the UPM
B35a	A(6:31) and D(0:31) to BS valid as requested by B corresponding word of the UPM
B35b	A(6:31) and D(0:31) to BS valid as requested by B corresponding word of the UPM
B36	A(6:31) and D(0:31) to GPL valid as requested by C corresponding word of the UPM
B37	UPWAIT Valid to CLKOUT Falling Edge
B38	CLKOUT Falling Edge to UPWAIT Valid
B39	AS Valid to CLKOUT Rising Edge

Table 1. Bus Opera

NUM	CHARACTERISTIC
B40	A(6:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, Valid to CLKC Edge
B41	$\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)
B42	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time)
B43	$\overline{AS}$ Negation to Memory Controller Signals Negati

NOTES:

1. The timing for $\overline{BR}$ output is relevant when th
   The timing for $\overline{BG}$ output is relevant when th
2. The setup times required for $\overline{TA}$, $\overline{TEA}$ and $\overline{B}$
   (and not when the memory controller or the
3. The timing required for $\overline{BR}$ input is relevant v
   The timing for $\overline{BG}$ input is relevant when the
4. The D(0:31) and DP(0:3) input timings B18
   input signal is asserted.
5. The D(0:31) and DP(0:3) input timings B20
   valid only under control of the UPM in the m
6. The timing B30 refers to $\overline{CS}$ when ACS = ‘0
7. The signal UPWAIT is considered asynchro
   specified in B37 and B38 are specified to en
8. The $\overline{AS}$ signal is considered asynchronous

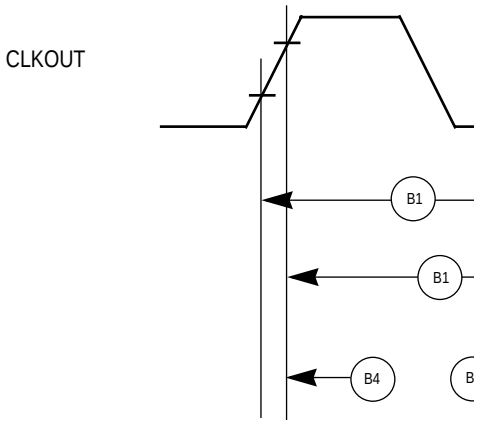


Figure 1. External

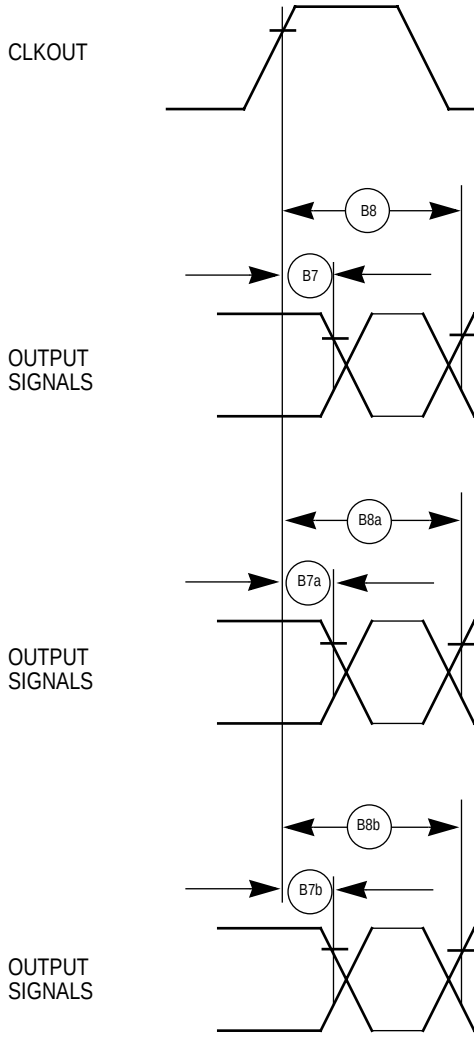


Figure 2. Synchronous O

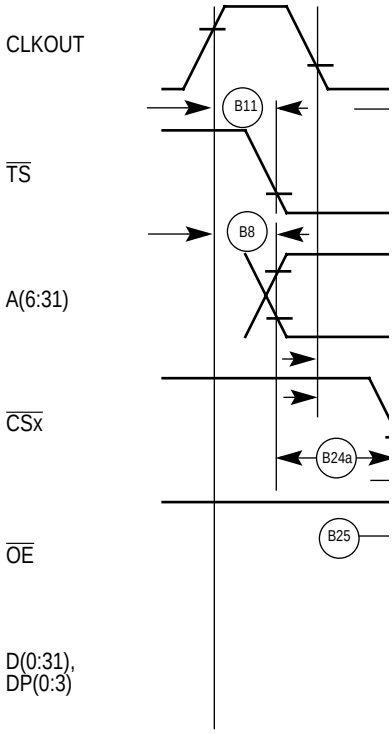


**Figure 9. External B
(GPCM Controlled-**

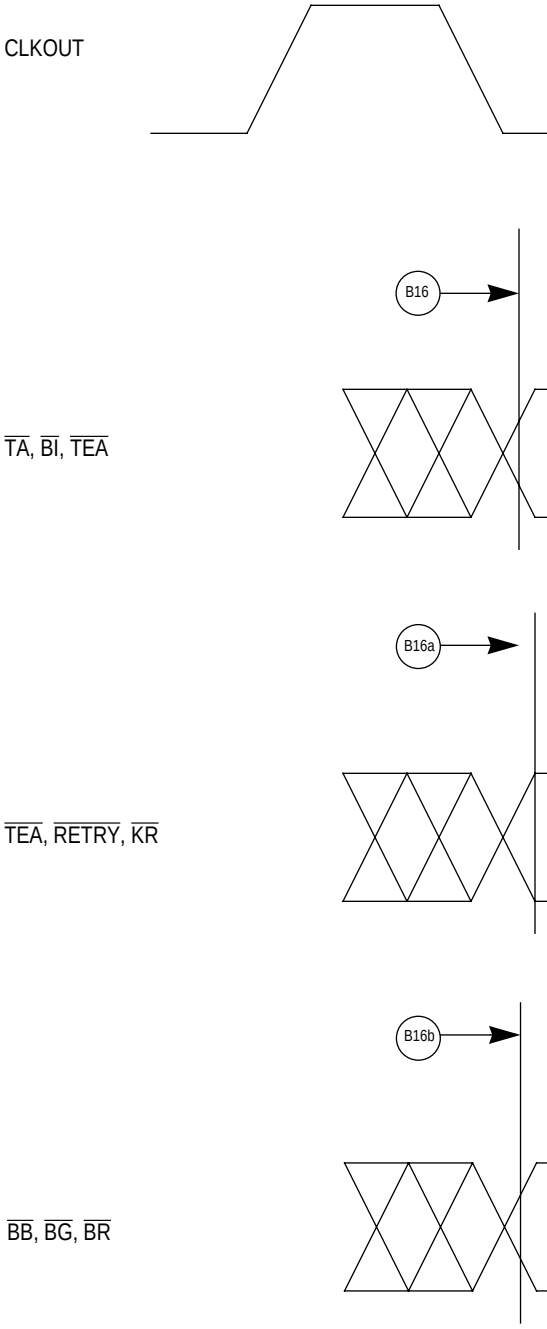


Figure 4. Synchronous I

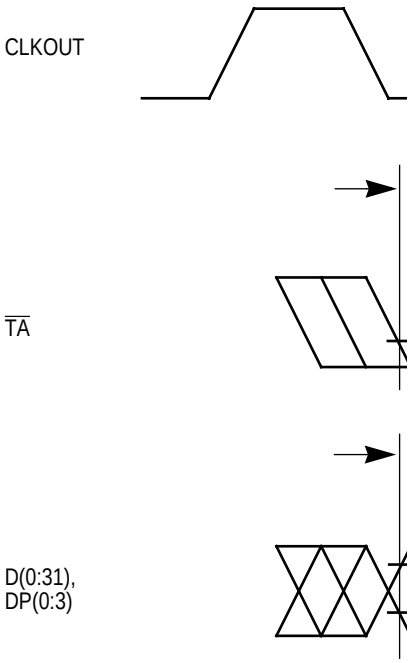


Figure 5. Input Data In N

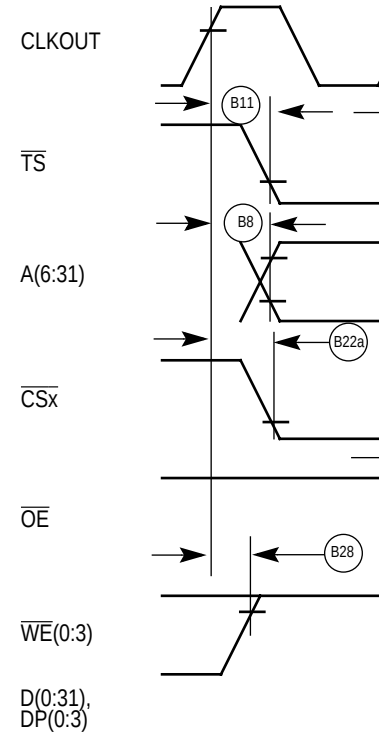


Figure 7. External Bus Read Timing

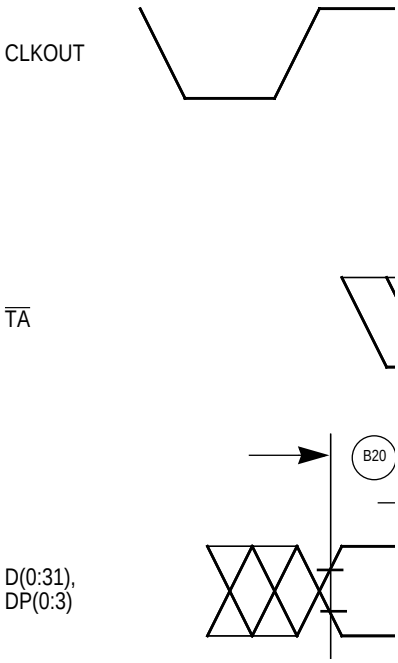


Figure 6. Input Data When Con

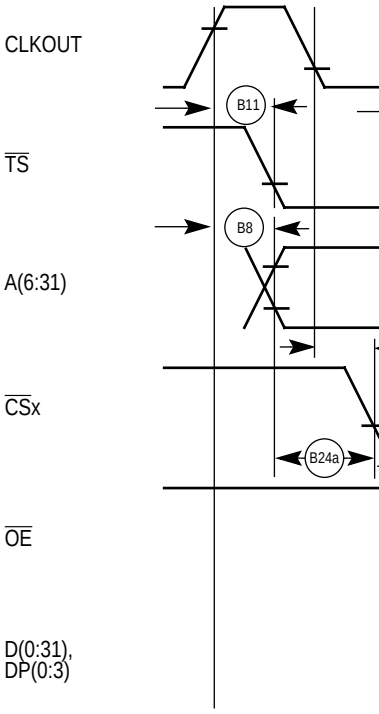


Figure 8. External Bus Read Timing Diagr

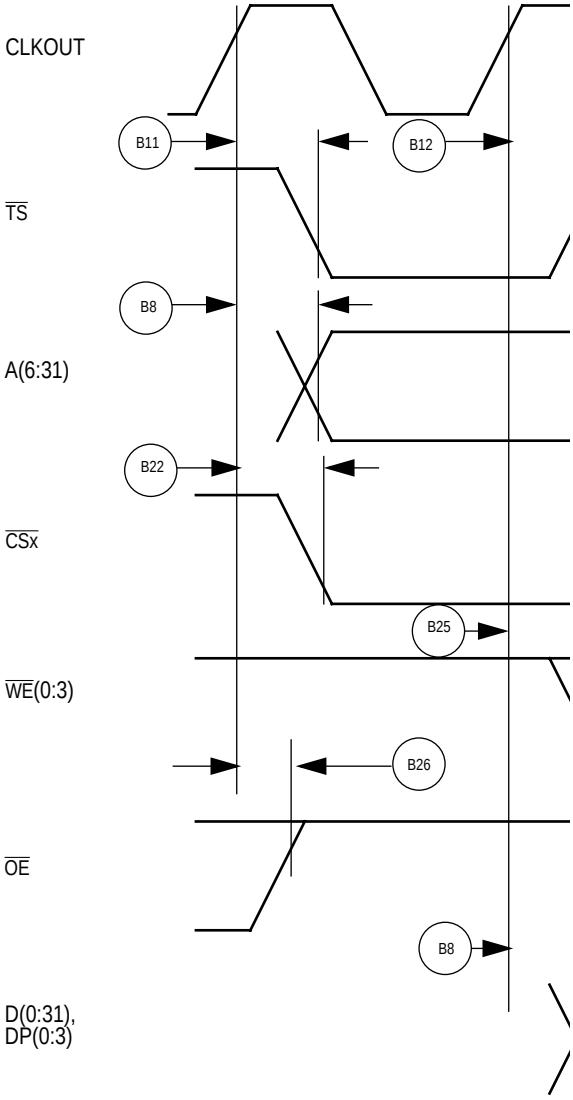


Figure 13. External B
(GPCM Controlled-

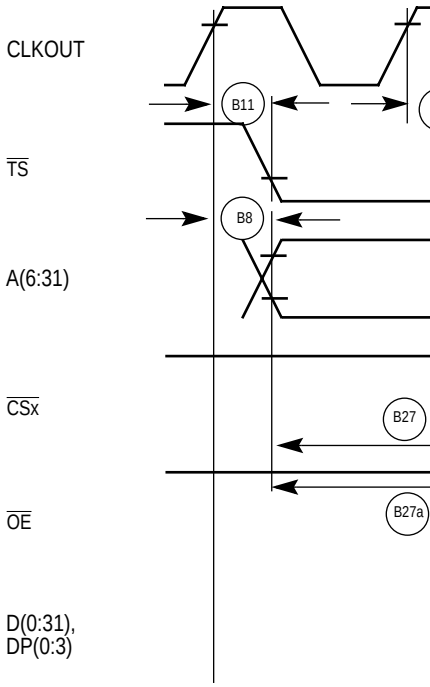


Figure 10. External B
(GPCM Controlled–TRLX

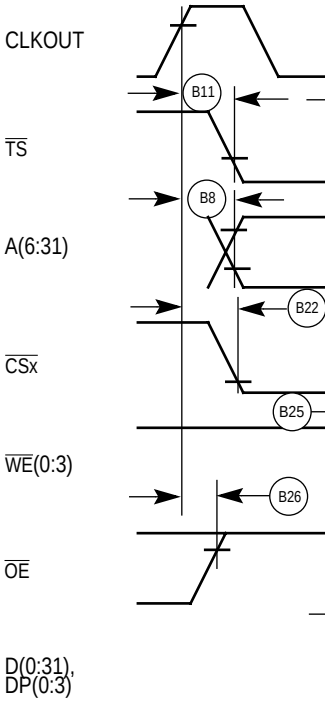


Figure 11. External B
(GPCM Controlled-

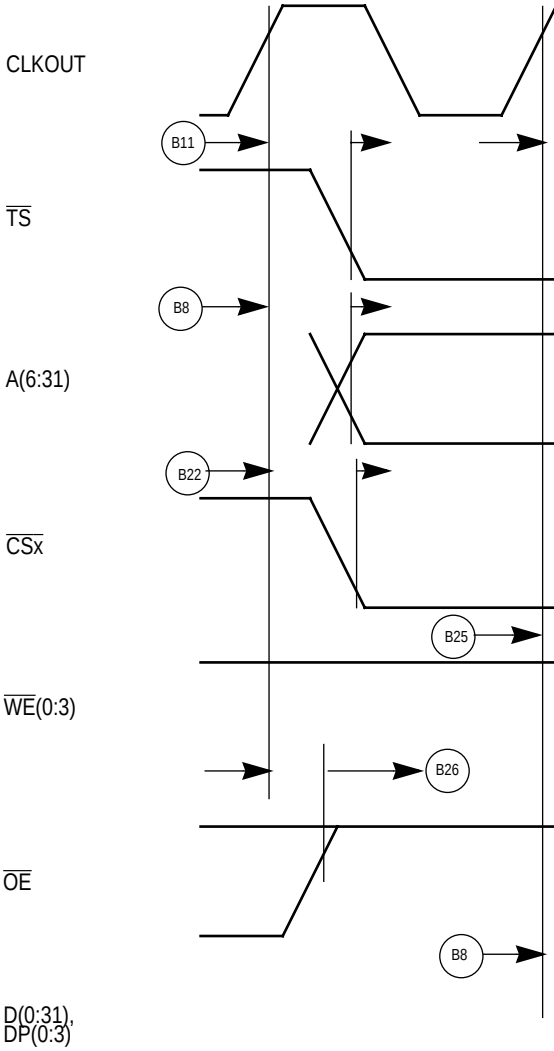


Figure 12. External B
(GPCM Controlled-

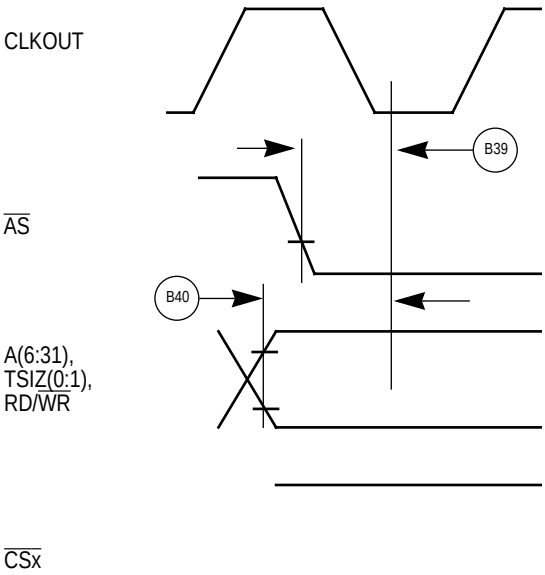


Figure 18. Asynchronous External I (GPCM Contr

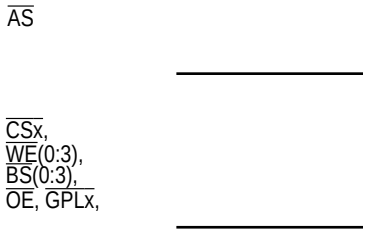


Figure 19. Asynchronous E (Control Signa

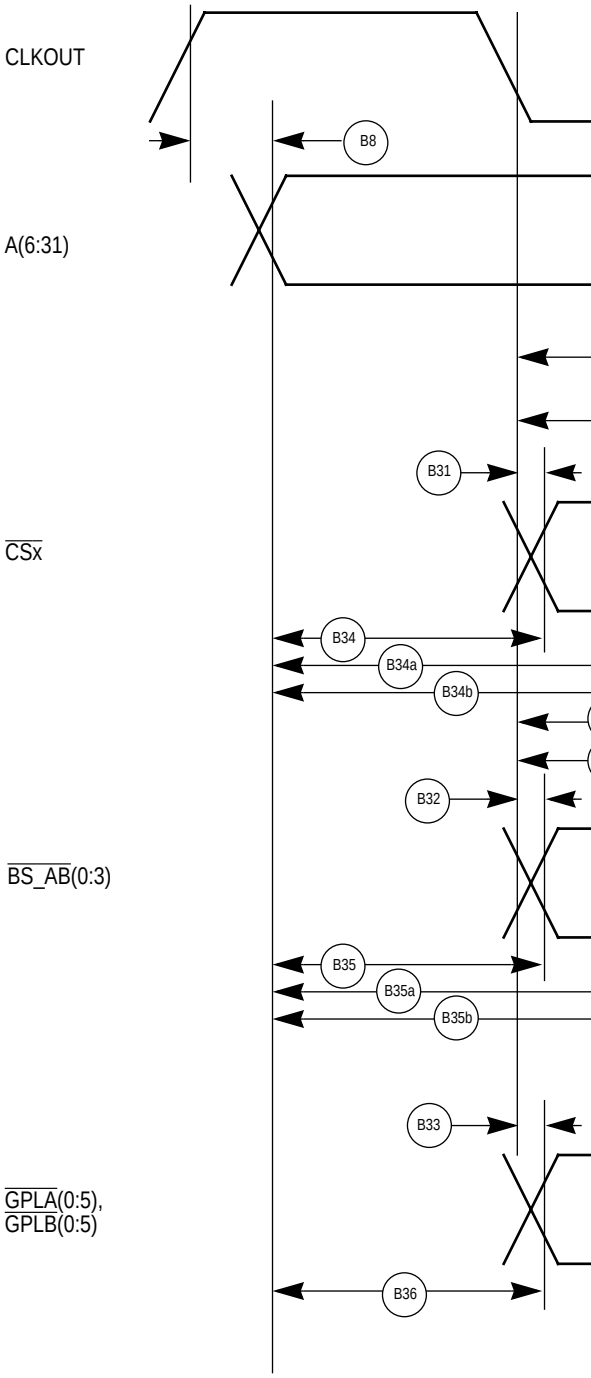


Figure 14. External Bus Timing

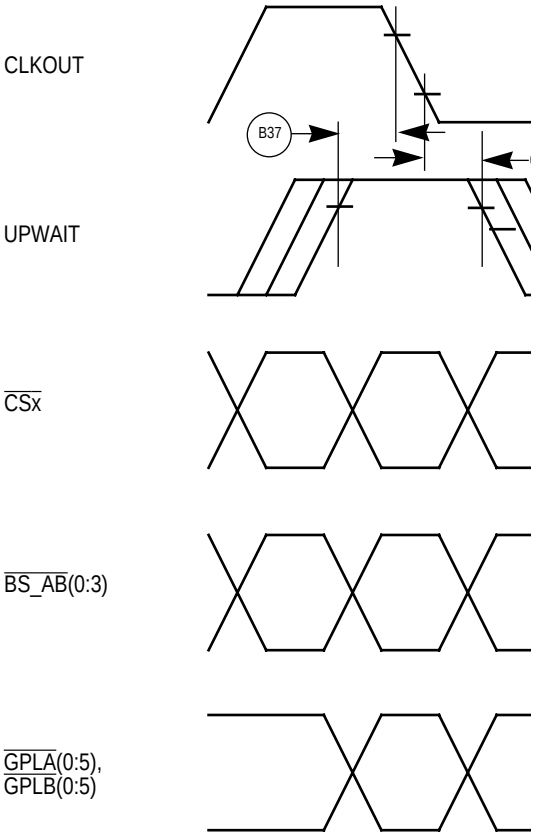


Figure 15. Asynchronous UP Handled Cycl

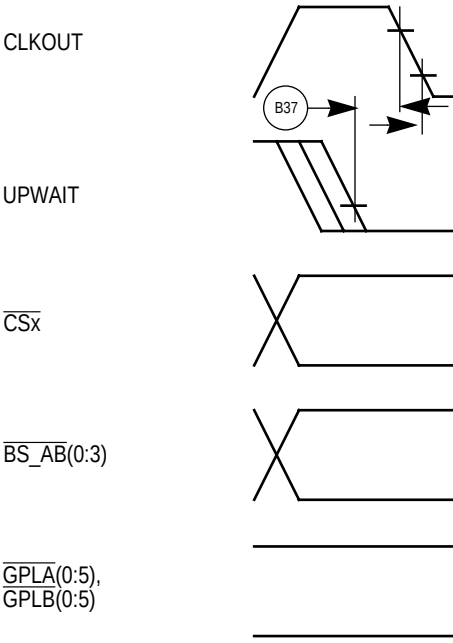


Figure 16. Asynchronous UP Handled Cycl

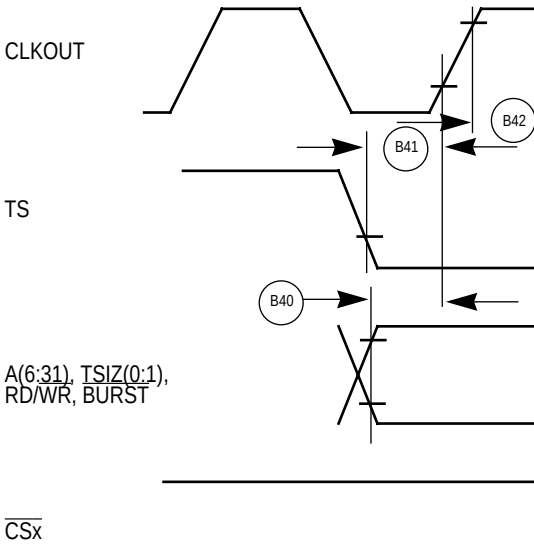


Figure 17. Synchronous Exter (GPCM Han

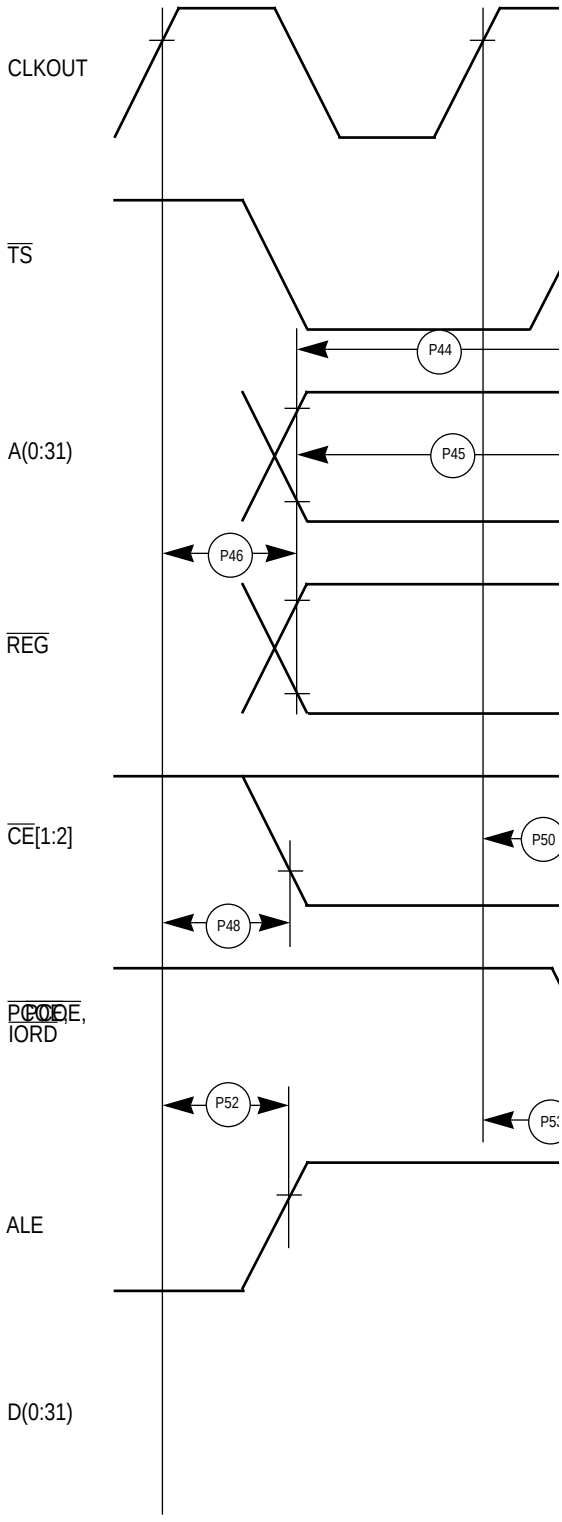


Figure 22. PCMCIA Access Cycles

Table 2. In

NUM	CHARACTERISTIC
I39	IRQx valid to CLKOUT rising edge (setup time)
I40	IRQx hold time after CLKOUT
I41	IRQx pulse width low
I42	IRQx pulse width high
I43	IRQx edge to edge time

NOTES:

1. The timings I39 and I40 describe the testing level sensitive. The IRQ lines are synchroni reference to the CLKOUT.
2. The timings I41 and I42 are specified to allo no direct relation with the total system inter

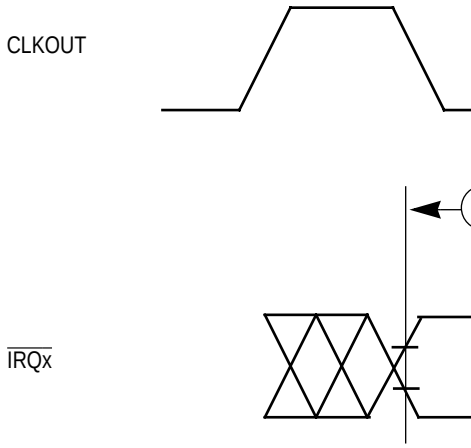


Figure 20. Interrupt D for External Le

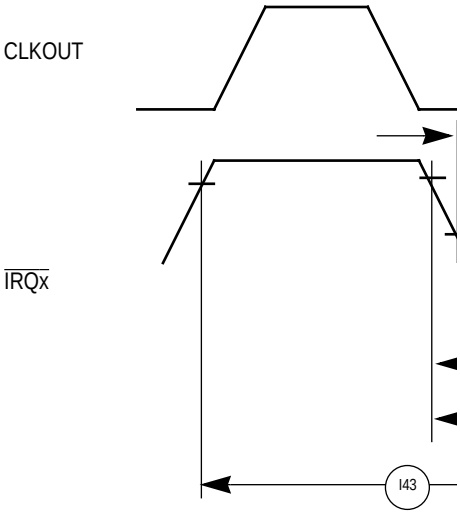


Figure 21. Interrupt D for External Ec

Table 3. P

NUM	CHARACTERISTIC
P44	A(6:31), REG valid to PCMCIA strobe asserted
P45	A(6:31), REG valid to ALE negation
P46	CLKOUT to REG valid
P47	CLKOUT to REG invalid
P48	CLKOUT to CE1, CE2 asserted
P49	CLKOUT to CE1, CE2 negated
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time
P52	CLKOUT to ALE assert time
P53	CLKOUT to ALE negate time
P54	PCWE, IOWR negated to D(0:31) invalid
P55	WAIT_B valid to CLKOUT rising edge
P56	CLKOUT rising edge to WAIT_B invalid

NOTES:

1. PSST = 1. Otherwise, add PSST times cycl
2. PSHT = 0. Otherwise, add PSHT times cyc
3. These synchronous timings define when th PCMCIA current cycle. The WAIT_B asserti timer expiration.

Table 5. De

NUM	CHARACTERISTIC
D61	DSCK cycle time
D62	DSCK clock pulse width
D63	DSCK rise and fall times
D64	DSDI input data setup time
D65	DSDI data hold time
D66	DSCK low to DSDO data valid
D67	DSCK low to DSDO invalid

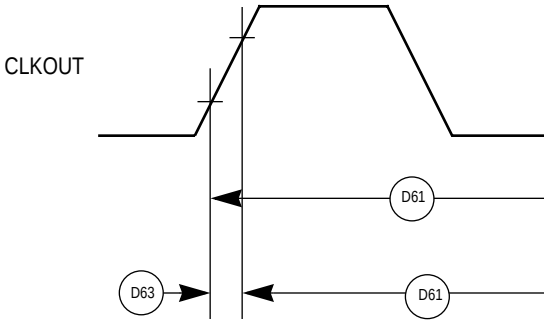


Figure 28. Debug Port

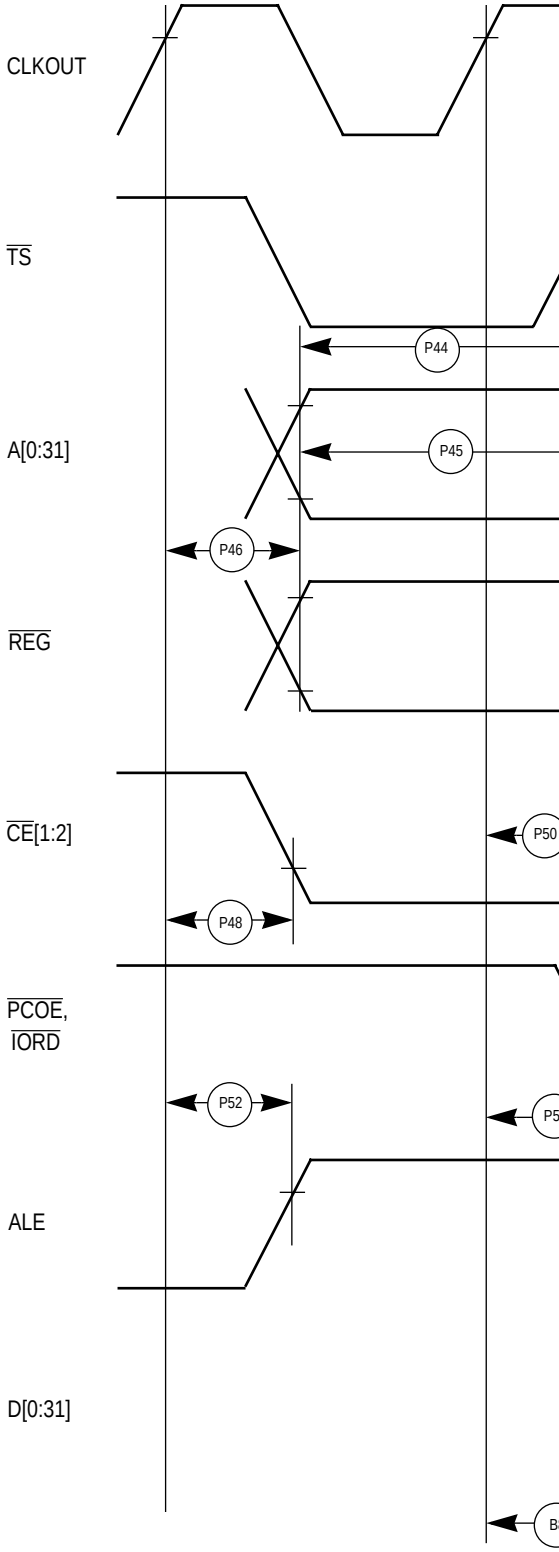


Figure 23. PCMCIA Access Cycles

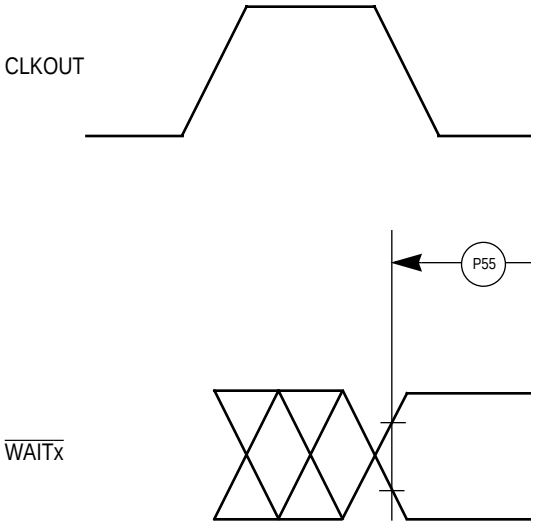


Figure 24. PCMCIA Wait Sig

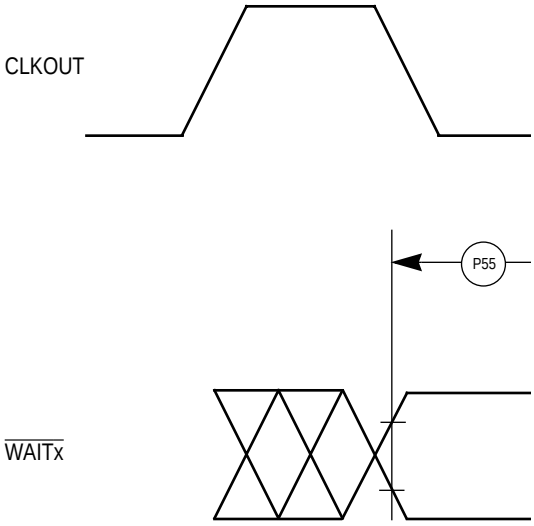


Figure 25. PCMCIA Wait Sig

Table 4. PCM

NUM	CHARACTERISTIC
P57	CLKOUT to OPx Valid
P58	HRESET negated to OPx drive
P59	IP_Bx valid to CLKOUT Rising Edge
P60	CLKOUT Rising Edge to IP_Bx invalid

NOTE: *OP2 and OP3 only.

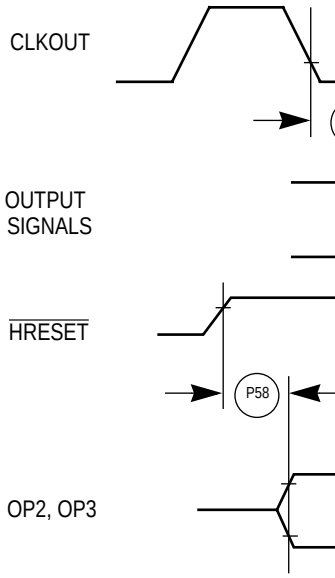


Figure 26. PCMCIA Ou

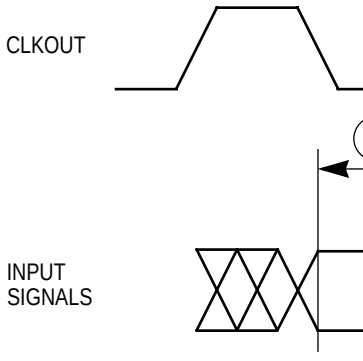


Figure 27. PCMCIA In

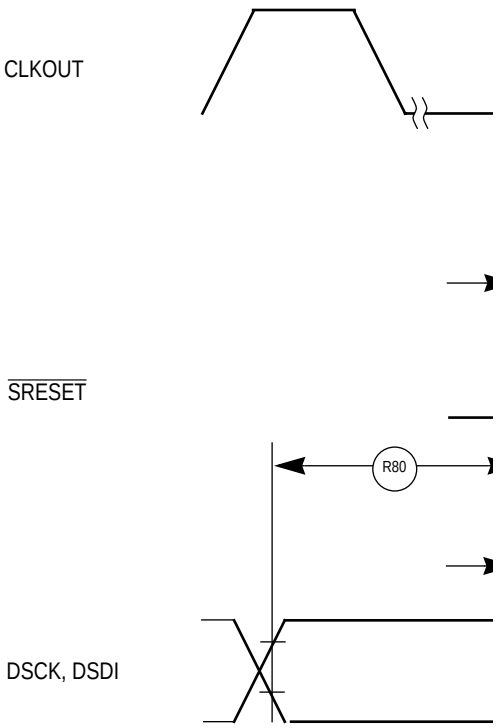


Figure 32. Reset Timing Dia

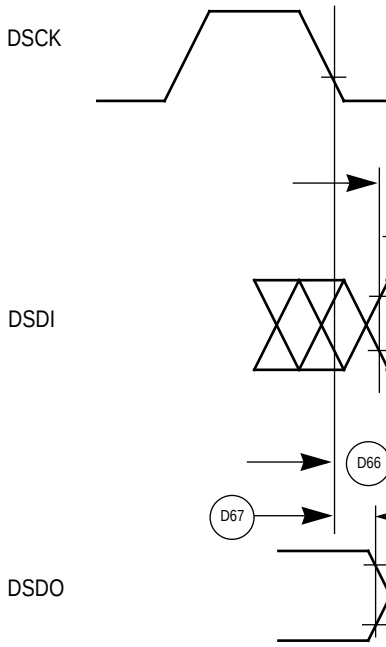


Figure 29. Debug

Table 6.

NUM	CHARACTERISTIC
R68	CLKOUT to HRESET high impedance
R69	CLKOUT to SRESET high impedance
R70	RSTCONF pulse width
R71	N/A
R72	Configuration data to HRESET rising edge setup time
R73	Configuration data to RSTCONF rising edge setu time
R74	Configuration data hold time after RSTCONF negation
R75	Configuration data hold time after HRESET nega
R76	HRESET and RSTCONF asserted to data out dri
R77	RSTCONF negated to data out high impedance
R78	CLKOUT of last rising edge before chip three-sta HRESET to data out high impedance
R79	DSDI and DSCK setup
R80	DSDI and DSCK hold time
R81	SRESET negated to CLKOUT rising edge for DS and DSCK sample

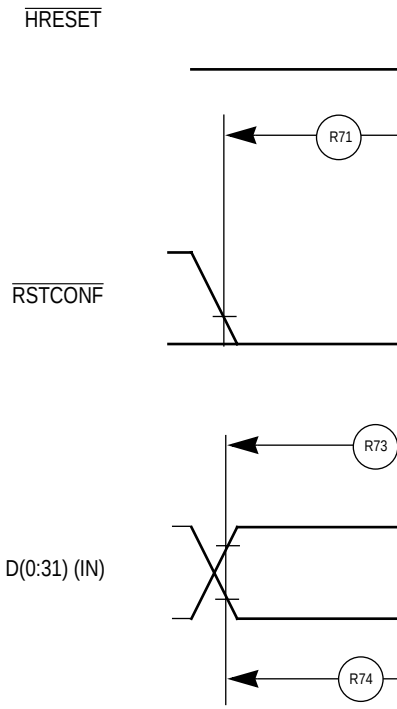


Figure 30. Reset Timing Diagr

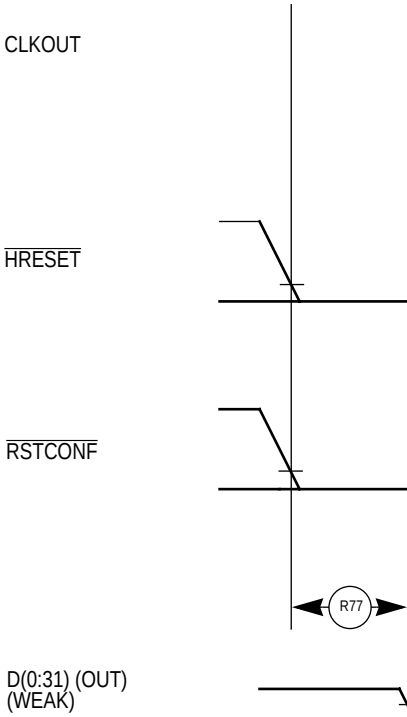


Figure 31. Reset Timing Diagram–MPC82

COMMUNICATION ELECTRICAL CH

Table 8. Parallel In

NUM	CHARACTERISTIC	MI
29	Data-in setup time to clock high	2
30	Data-in hold time from clock high	1
31	Clock high to data-out valid (CPU writes data, control, or direction)	–

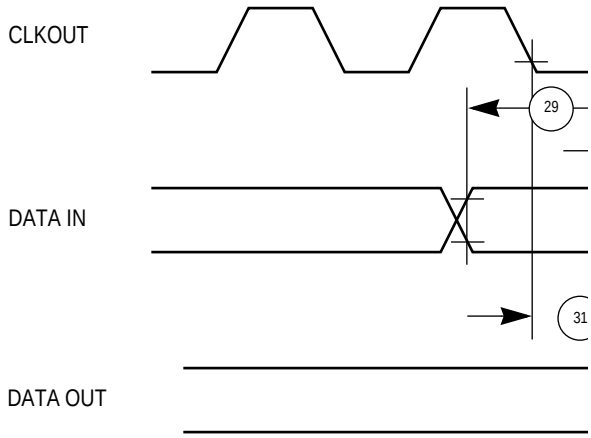


Figure 37. Parallel Input/Outpu

Table 7.

NUM	CHARACTERISTIC
J82	TCK cycle time
J83	TCK clock pulse width measured at 1.5V
J84	TCK rise and fall times
J85	TMS, TDI data setup time
J86	TMS, TDI data hold time
J87	TCK low to TDO data valid
J88	TCK low to TDO data invalid
J89	TCK low to TDO high impedance
J90	$\overline{\text{TRST}}$ assert time
J91	$\overline{\text{TRST}}$ setup time to TCK low
J92	TCK falling edge to output valid
J93	TCK falling edge to ouput valid out of high impeda
J94	TCK falling edge to output high impedance
J95	Boundary scan input valid to TCK rising edge
J96	TCK rising edge to boundary scan input invalid

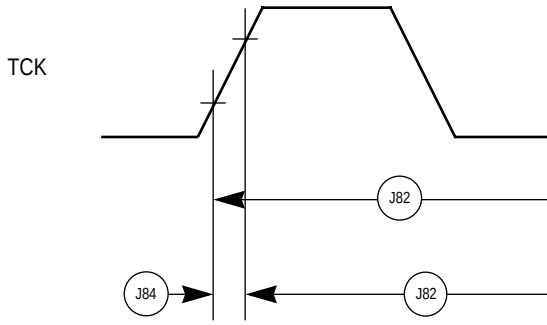


Figure 33. JTAG Test C

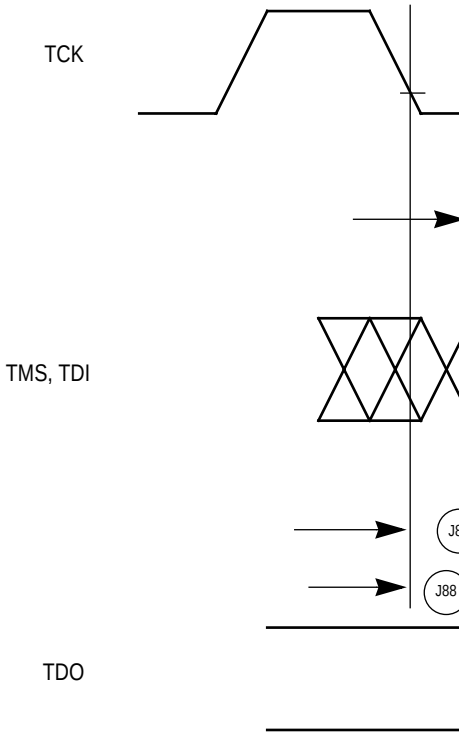


Figure 34. JTAG–Test A

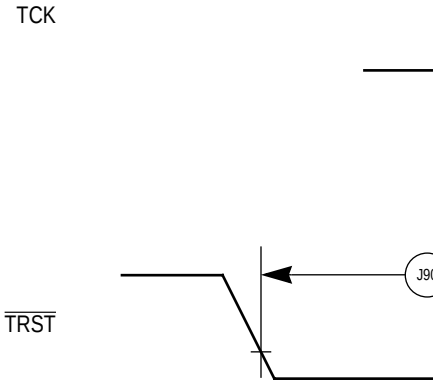


Figure 35. JTAG–

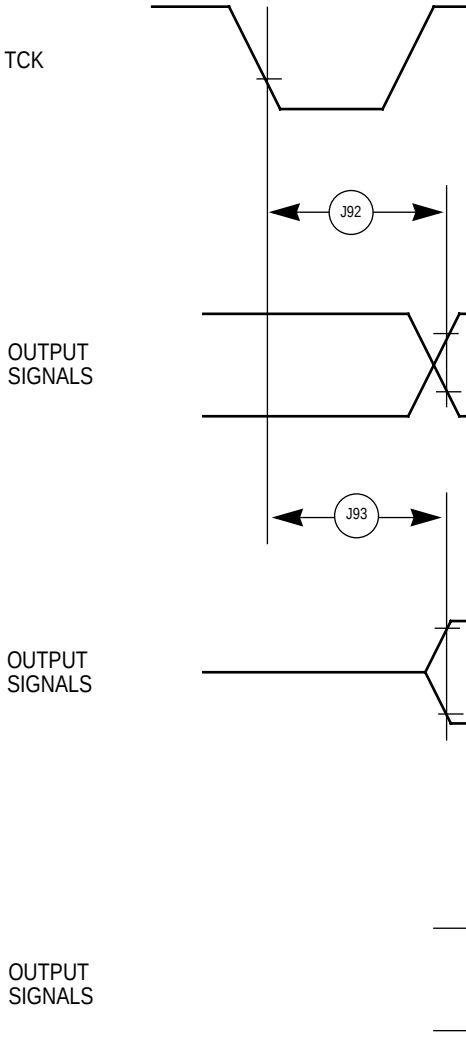


Figure 36. Boundary Sc

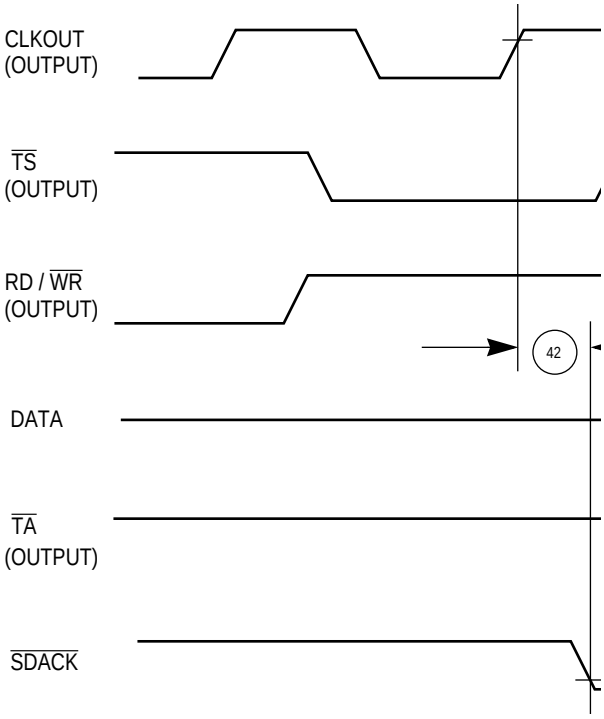


Figure 41. SDACK Timi

Table 9.

NUM	CHARACTERISTIC	M
40	DREQ setup time to clock high	1
41	DREQ hold time from clock high	5
42	SDACK assertion delay from clock high	–
43	SDACK negation delay from clock low	–
44	SDACK negation delay from TA low	–
45	SDACK negation delay from clock high	–
46	TA assertion to falling edge of the clock setup time	1

NOTE: Applies to external TA.

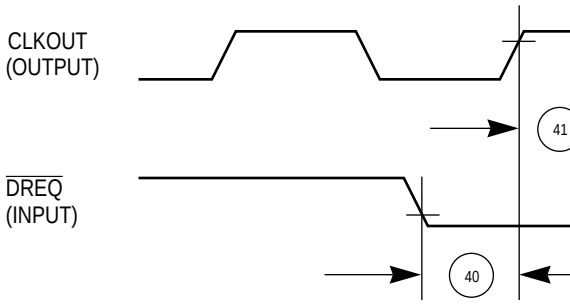


Figure 38. IDMA Externa

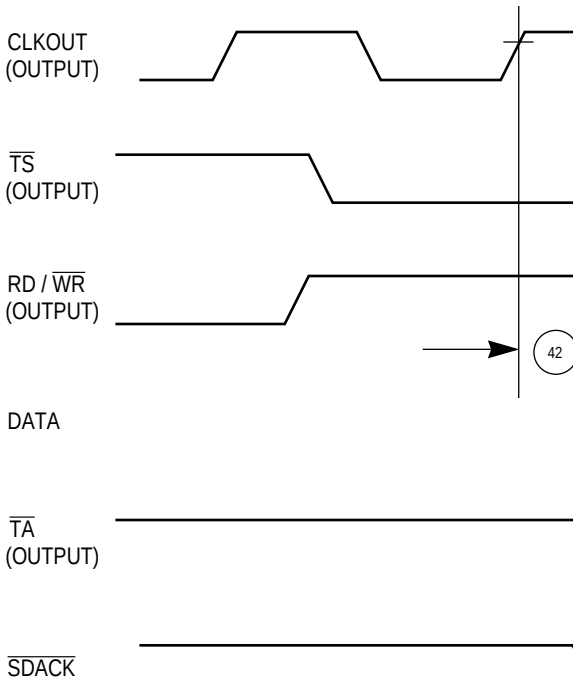


Figure 39. SDACK Timing Diagra at the Falling

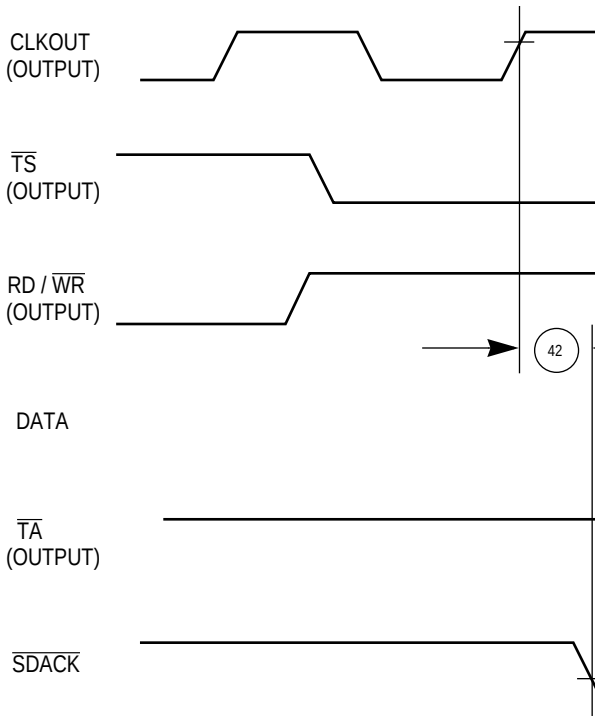


Figure 40. SDACK Timing Diagra at the Falling

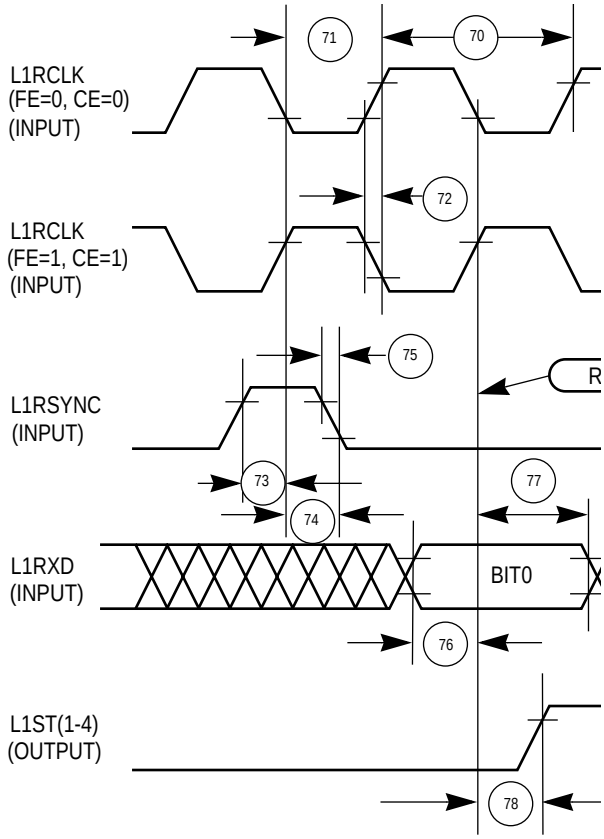


Figure 44. Serial Interface Receive Timi

Table 10. Baud R

NUM	CHARACTERISTIC	MI
50	BRGO rise and fall times	–
51	BRGO duty cycle	4
52	BRGO cycle	4

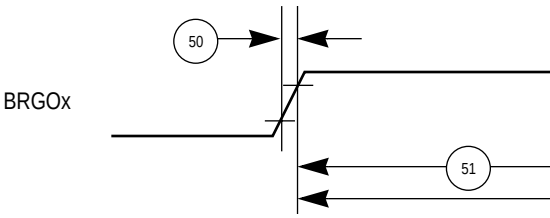


Figure 42. Baud Rate

Table 11. General-

NUM	CHARACTERISTIC	MIN
61	TIN/$\overline{\text{TGATE}}$ rise and fall times	12
62	TIN/$\overline{\text{TGATE}}$ low time	5
63	TIN/$\overline{\text{TGATE}}$ high time	—
64	TIN/$\overline{\text{TGATE}}$ cycle time	—
65	CLKO low to $\overline{\text{TOUT}}$ valid	—

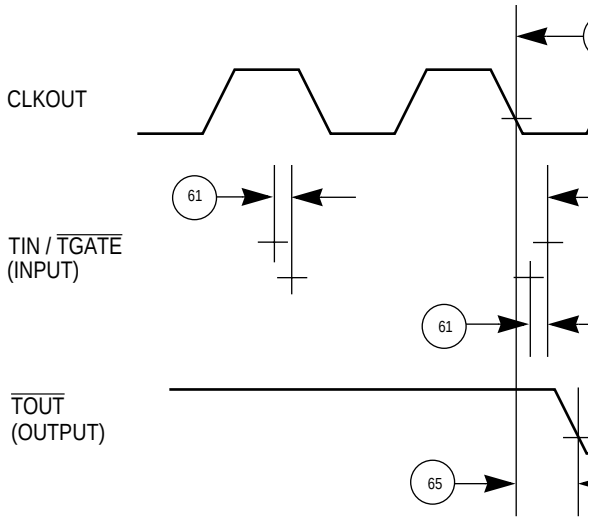


Figure 43. General-Purp

Table 12. Seri

NUM	CHARACTERISTIC
70	L1RCLK and L1TCLK frequency (DSC=0)[1,3]
71	L1RCLK and L1TCLK width low (DSC=0)[3]
71a	L1RCLK and L1TCLK width high (DSC=0)[2]
72	L1TXD, L1ST(1–8), L1RQ, L1CLKO rise and fall times
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)
74	L1CLK edge to L1RSYNC and L1TSYNC invalid (SYNC hold time)
75	L1RSYNC and L1TSYNC rise and fall times
76	L1RXD valid to L1CLK edge (L1RXD setup time)
77	L1CLK edge to L1RXD invalid (L1RXD hold time)
78	L1CLK edge to L1ST(1–8) valid
78a	L1SYNC valid to L1ST(1–8) valid[4]
79	L1CLK edge to L1ST(1–8) invalid
80	L1CLK edge to L1TXD valid
80a	L1TSYNC valid to L1TXD valid[4]
81	L1CLK edge to L1TXD high impedance
82	L1RCLK and L1TCLK frequency (DSC=1)
83	L1RCLK and L1TCLK width low (DSC=1)
83a	L1RCLK and L1TCLK width high (DSC=1)[2]
84	L1CLK edge to L1CLKO valid (DSC=1)
85	L1RQ valid before falling edge of L1TSYNC[3]
86	L1GR setup time[3]
87	L1GR hold time[3]
88	L1CLK edge to L1SYNC valid (FSD = 00, CNT = 0000, BYT = 0, DSC=0)

NOTES:

1. The ratio SyncCLK/L1RCLK must be greate
2. Where P=1/CLKO1. For a 25MHz CLKO1 r
3. These electrical specifications are only vali
4. The strobes and TXD2 on the first bit of the is later.

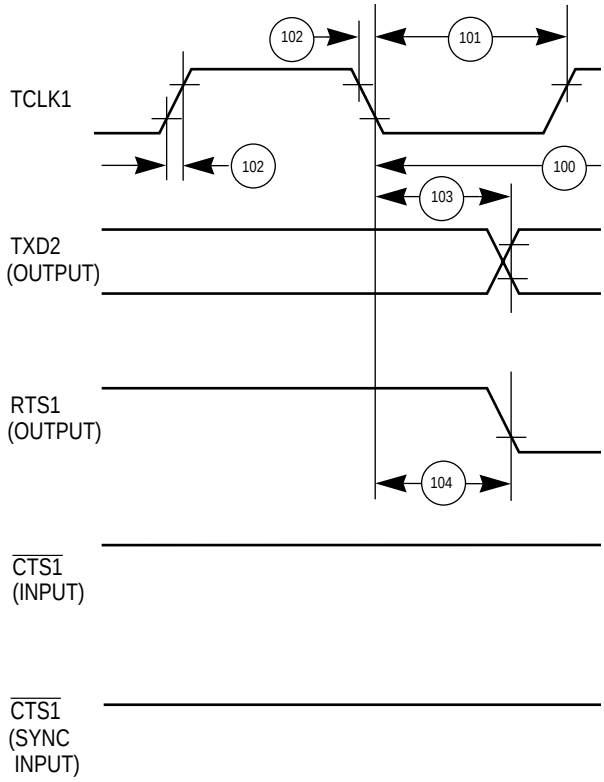


Figure 47. SCC NMSI

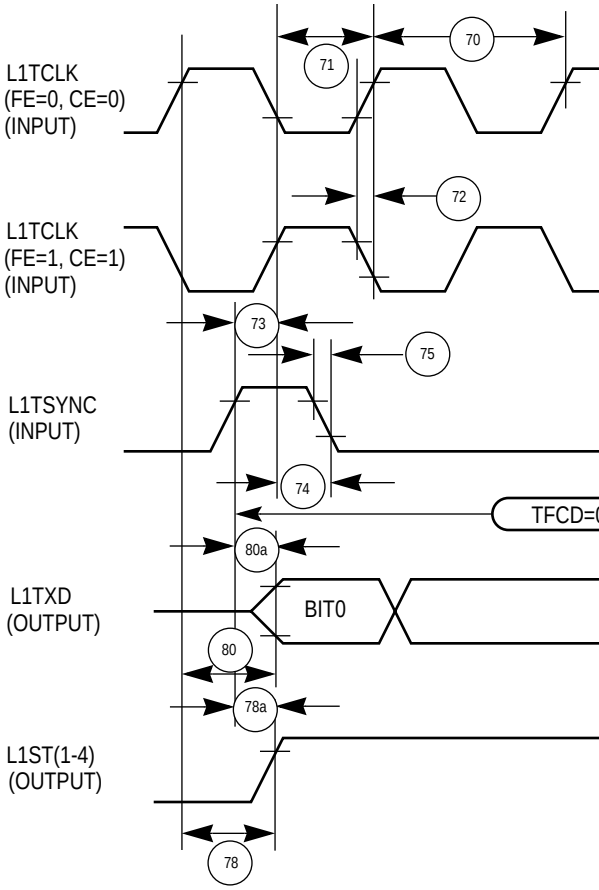


Figure 45. Serial Interfa

Table 13. Serial Communicatior

NUM	CHARACTERISTIC	2
		MIN
100	RCLK1 and TCLK1 width high[1]	CLKOUF
101	RCLK1 and TCLK1 width low	CLKOU +5ns
102	RCLK1 and TCLK1 rise and fall times	—
103	TXD2 active delay (from TCLK1 falling edge)	0
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5
106	RXD2 setup time to RCLK1 rising edge	5
107	RXD2 hold time from RCLK1 rising edge2	5
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	5

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/T
2. Applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they

Table 14. Serial Communicatio

NUM	CHARACTERISTIC	
		MI
100	RCLK1 and TCLK1 frequency[1]	0
102	RCLK1 and TCLK1 rise and all times	–
103	TXD2 active delay (from TCLK1 falling edge)	0
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	4
106	RXD2 setup time to RCLK1 rising edge	4
107	RXD2 hold time from RCLK1 rising edge[2]	0
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	4

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/T
2. Applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they

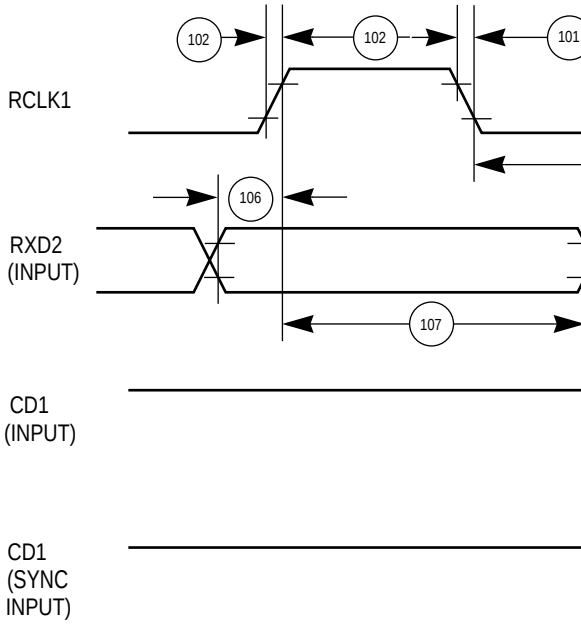
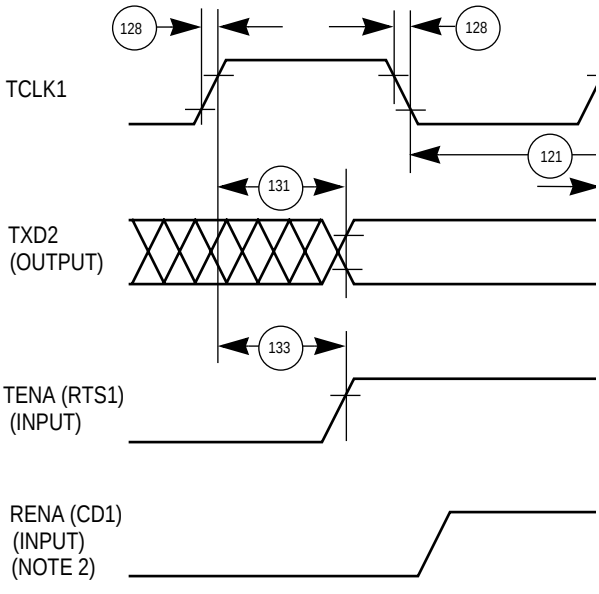


Figure 46. SCC NMSI



NOTES: 1. TRANSMIT CLOCK INVERT (TCI) BIT IN THE GSMF
2. IF RENA IS DEASSERTED BEFORE TENA, OR REN
TRANSMIT, THEN THE CSL BIT IS SET IN THE BUI

Figure 51. Ethernet T

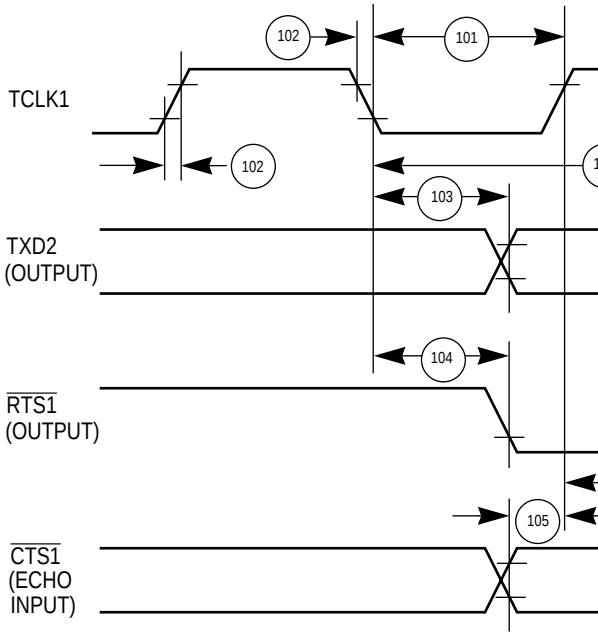


Figure 48. HDLC

Table 15. E

NUM	CHARACTERISTIC	M
120	CLSN (CTS2) width high	4
121	RCLK1 rise and fall times	–
122	RCLK1 width low	4
123	RCLK1 clock period[1]	8
124	RXD2 setup time	2
125	RXD2 hold time	5
126	RENA (CD2) active delay (from RCLK1 rising edge of the last data bit)	1
127	RENA (CD2) width low	1(
128	TCLK1 rise and fall times	–
129	TCLK1 width low	4
130	TCLK1 clock period[1]	9
131	TXD2 active delay (from TCLK1 rising edge)	1
132	TXD2 inactive delay (from TCLK1 rising edge)	1
133	TENA (RTS2) active delay (from TCLK1 rising edge)	1
134	TENA (RTS2) inactive delay (from TCLK1 rising edge)	1
135	N/A	
136	N/A	
137	N/A	
138	CLKx low to $\overline{\text{SDACK}}$ asserted[2]	–
139	CLKx low to $\overline{\text{SDACK}}$ negated[3]	–

NOTES:

1. The ratio SyncCLK/RCLK1 and SyncCLK/T
2. $\overline{\text{SDACK}}$ is asserted when the SDMA writes

Figure 49. Ethernet C

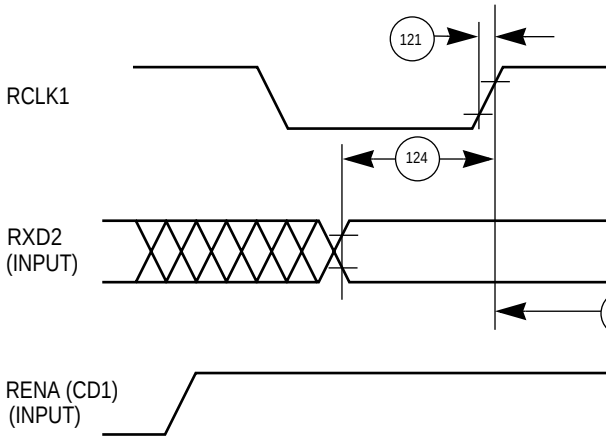


Figure 50. Ethernet

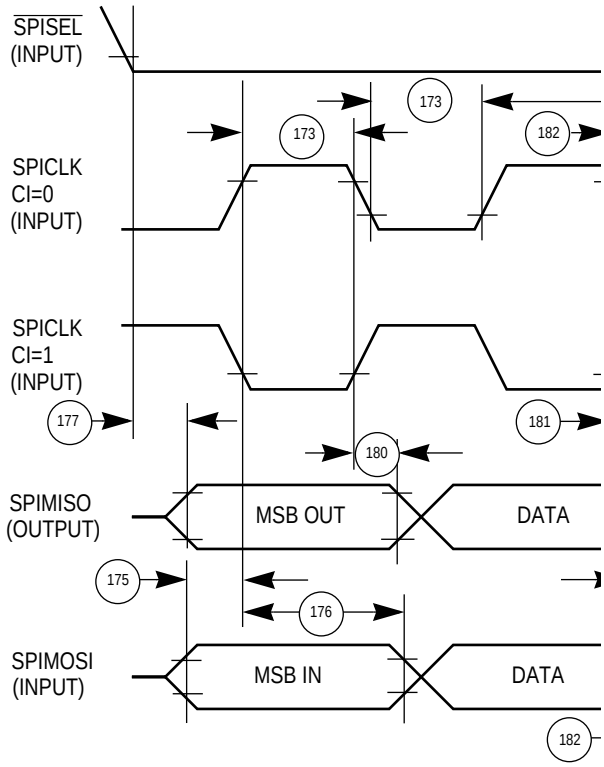


Figure 54. SPI Slave

Table 16. Serial Periphe

NUM	CHARACTERISTIC	MIN
160	Master cycle time	4
161	Master clock (SCK) high or low time	2
162	Master data setup time (inputs)	50
163	Master data hold time (inputs)	0
164	Master data valid (after SCK edge)	—
165	Master data hold time (outputs)	0
166	Rise time output	—
167	Fall time output	—

NOTE: The ratio SyncCLK/SMCLK must be greater tha

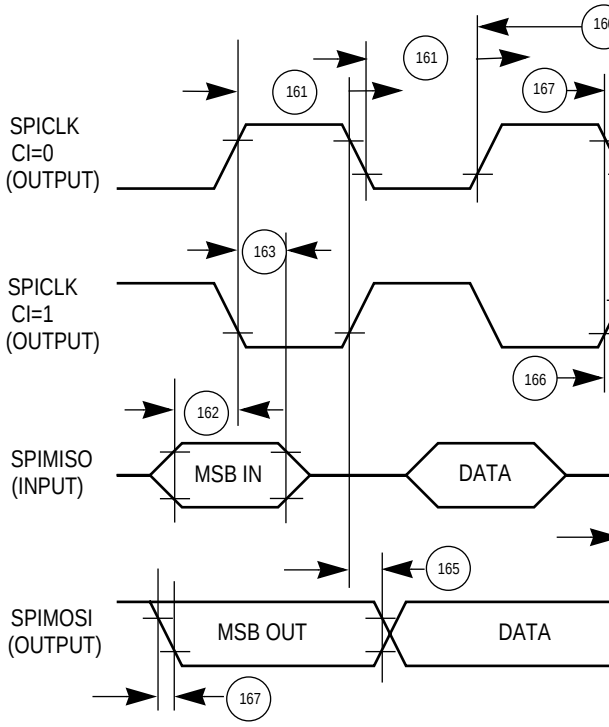


Figure 52. SPI Maste

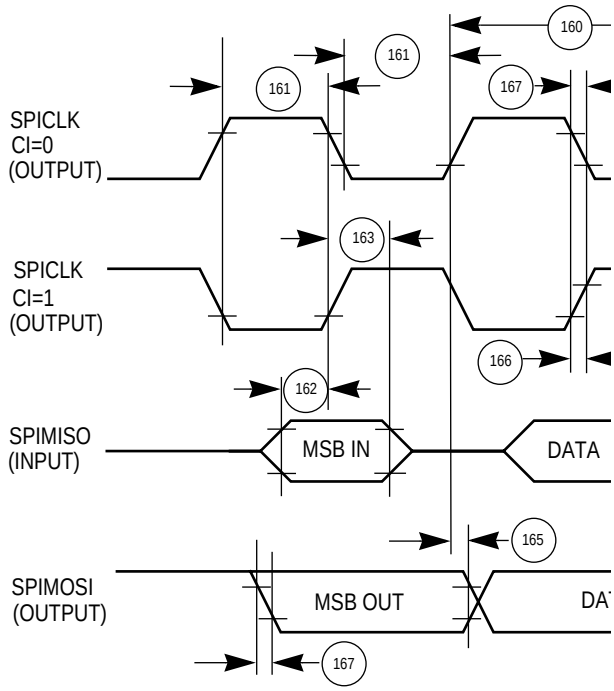


Figure 53. SPI Maste

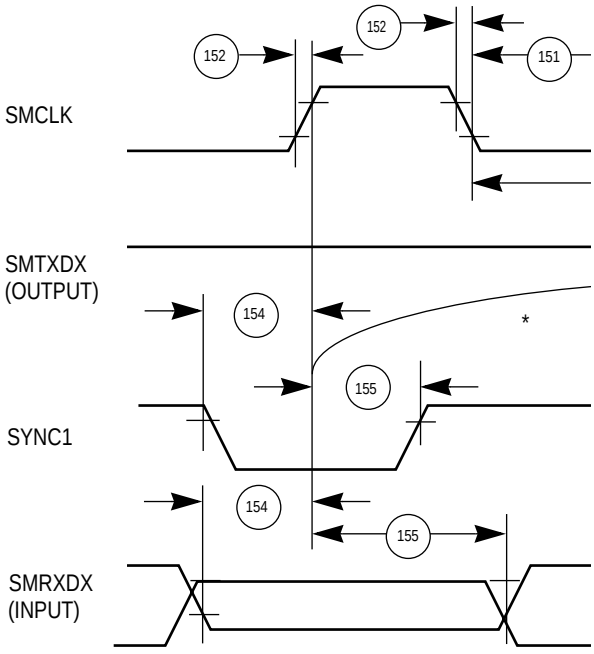
Table 17. Serial Periph

NUM	CHARACTERISTIC	MI
170	Slave cycle time	2
171	Slave enable lead time	1
172	Slave enable lag time	1
173	Slave clock (SPICLK) high or low time	1
174	Slave sequential transfer delay (does not require deselect)	1
175	Slave data setup time (inputs)	2
176	Slave data hold time (inputs)	2
177	Slave access time	–
178	Slave SPI MISO disable time	–
179	Slave data valid (after SPICLK edge)	–
180	Slave data hold time (outputs)	0
181	Rise time (input)	–
182	Fall time (input)	–

Table 20. Serial Mana

NUM	CHARACTERISTIC	M
150	CLK1 clock period	1(
151	CLK1 width low	5
151A	CLK1 width high	5
152	CLK1 rise and fall times	–
153	SMTXDx active delay (from CLK1 falling edge)	1
154	SMRXDx/SYNC1 setup time	2
155	SMRXDx/SYNC1 hold time	5

NOTE: The ratio SyncCLK/SMCLK must be greater than



NOTE: * THIS DELAY IS EQUAL TO AN INTEGER NUMBER OF

Figure 57. SMC Trar

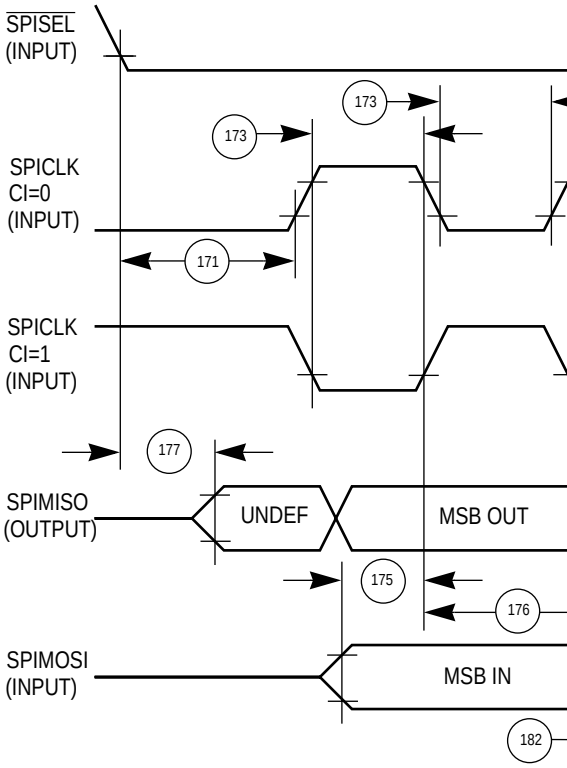


Figure 55. SPI Slave

Table 18. I²C Tim

NUM	CHARACTERISTIC	MIN
200	SCL clock frequency (slave)	0
200	SCL clock frequency (master)	1.5
202	Bus free time between transmissions	4.7
203	Low period of SCL	4.7
204	High period of SCL	4.0
205	Start condition setup time	4.7
206	Start condition hold time	4.0
207	Data hold time	0
208	Data setup time	250
209	SDL/SCL rise time	—
210	SDL/SCL fall time	—
211	STOP condition setup time	4.7

NOTE: SCL frequency is given by SCL = BRGCLK_fre
The ratio SyncClk/(BRGCLK/pre_scaler) must b

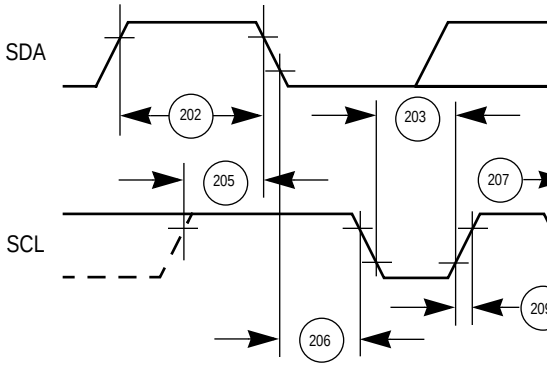


Figure 56. I²C B

Table 19. I²C Tim

NUM	CHARACTERISTIC
200	SCL clock frequency (slave)
200	SCL clock frequency (master)
202	Bus free time between transmissions
203	Low period of SCL
204	High period of SCL
205	Start condition setup time
206	Start condition hold time
207	Data hold time
208	Data setup time
209	SDL/SCL rise time
210	SDL/SCL fall time
211	Stop condition setup time

Table 22. Vide

NUM	CHARACTERISTIC	MIN
240	Clock cycle time	32
241	Clock high time	13
242	CLK/HSYNC/VSYNC/BLANK/FIELD rise and fall times	—
243	Clock high to data valid	10

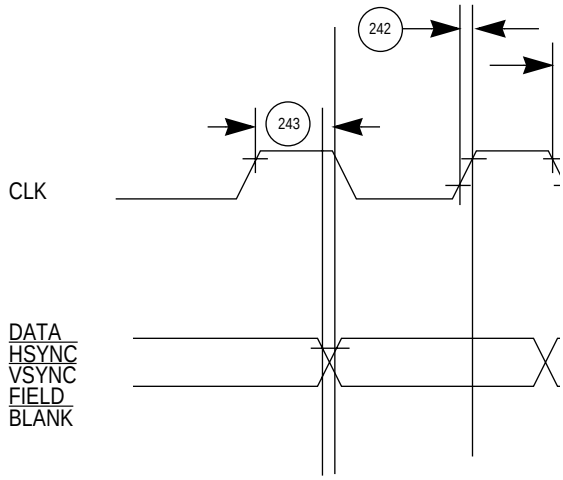


Figure 60. Vide

Table 21. LCD

NUM	CHARACTERISTIC	MI
220	Shift clock cycle time	4
221	Shift clock high time	2
223	CLOCK/HSYNC/VSYNC/OE rise and fall times	–
224	Data valid delay from shift clock high	–
225	VSYNC to HSYNC setup time[1]	5
226	VSYNC hold time	1
227	HSYNC pulse width	4
228	Time from clock falling edge to HSYNC rising edge	4.
229	Time from HSYNC falling edge to clock rising edge[2]	4
230	AC active delay	–
231	VSYNC pulse width (TFT)	1
232	HSYNC to OE delay[3]	4
233	OE to HSYNC delay	4
234	VSYNC to OE delay (TFT)	0
235	VSYNC/HSYNC/OE active delay (TFT)	–
236	Wait between frames[4]	WI

NOTES:

1. T = shift clock cycle (220).
2. This number is given for wbl(wait between l
3. This number is given for wbl(wait between li
4. Wait Between Frames (WBF) is a programm

Tcyc is the cycle time of the LCD clock (shift the AC electrical specifications. 1–16 lines is and 16, depending on how the LCD controlle 0–1,023 lines is a time period that can vary b the LCVCR.

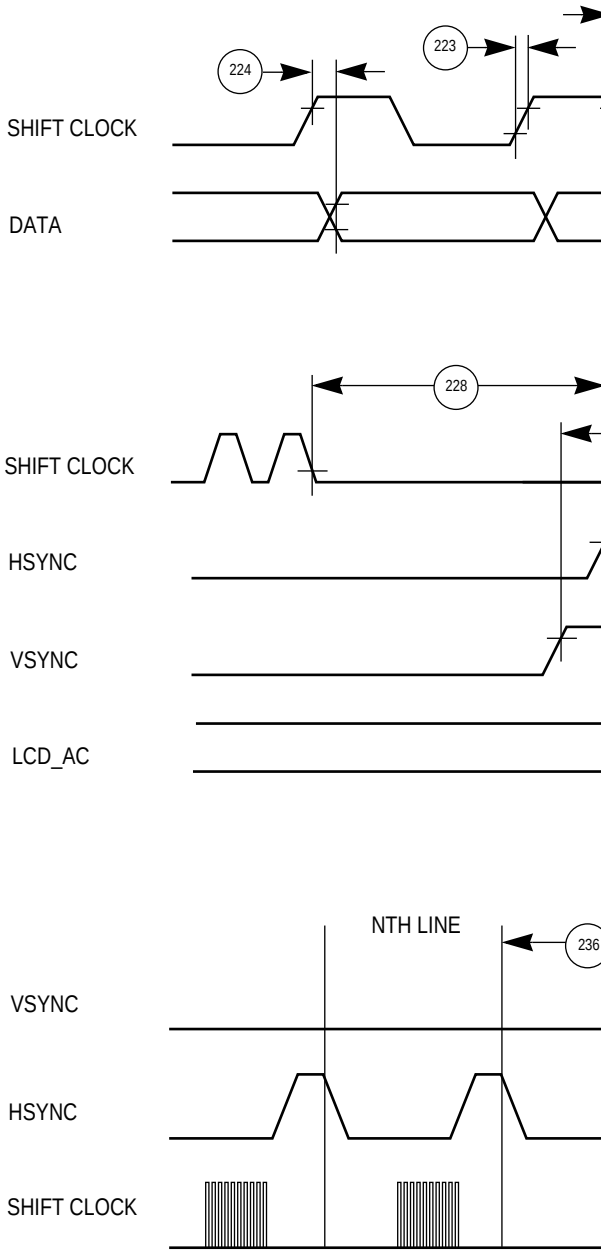


Figure 58. Passive

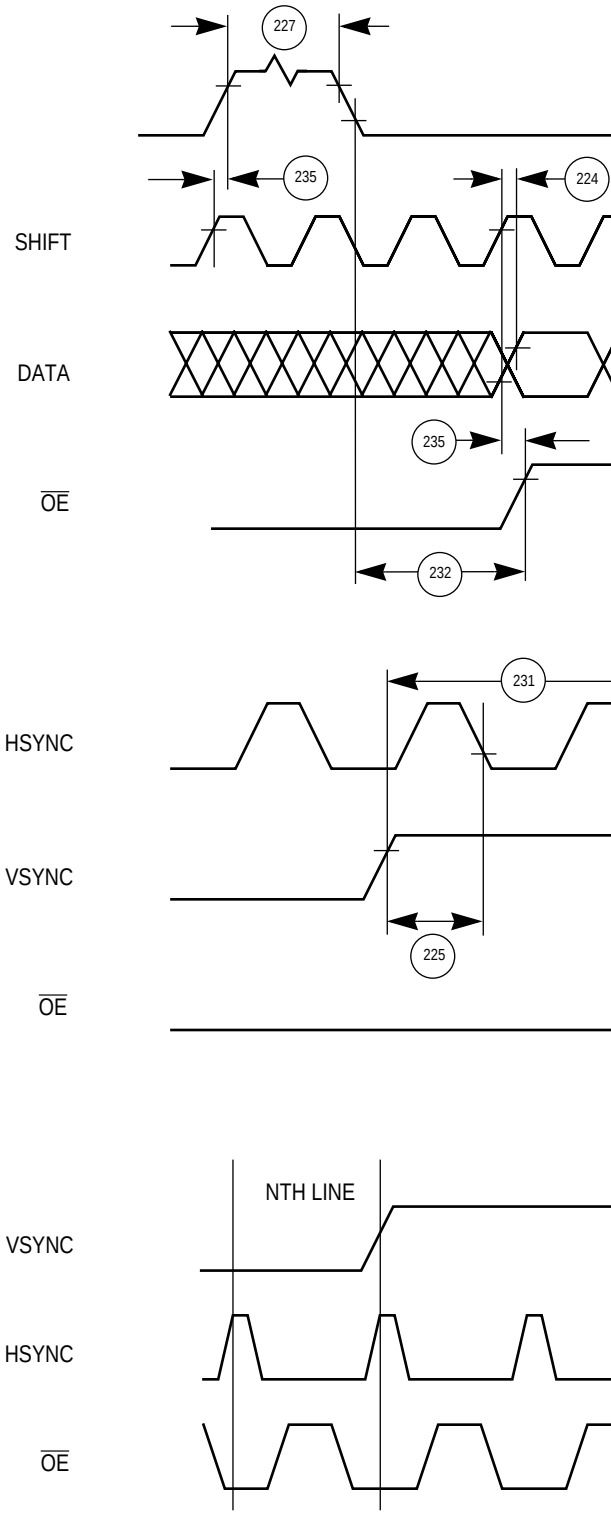


Figure 59. TFT P

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, A
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-k
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbou
Tai Po, N.T., Hong Kong.