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PowerPC™

*Advance Information*

# EC603e™ Embedded RISC Microprocessor (PID7t) Hardware Specifications

The EC603e microprocessor from Motorola is an implementation of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. The EC603e microprocessor for embedded systems is functionally equivalent to the MPC603e with the exception of the floating-point unit which is not supported on the EC603e microprocessor.

The EC603e is implemented in several semiconductor fabrication processes. Different processes may require different supply voltages and may have other electrical differences but will have the same functionality. As a technical designator to distinguish between EC603e implementations in various processes, an abbreviation composed of the processor version register (PVR) value and a process identifier (PID) is assigned to the various implementations as shown below:

**EC603e Microprocessors from Motorola**

| Technical Designator | Process | Core Voltage | I/O Voltage | 5-Volt Tolerant | Part Number |
|---|---|---|---|---|---|
| PID6 | 0.5 μm CMOS, 4LM | 3.3 V | 3.3 V | Yes | MPE603e |
| PID7v | 0.35 μm CMOS, 5LM | 2.5 V | 3.3 V | Yes | MPE603p |
| PID7t | 0.29 μm CMOS, 5LM | 2.5 V | 3.3 V | Yes | MPE603r |

This document describes the pertinent physical characteristics of the PID7t. For functional characteristics of the processor, refer to the *MPC603e & EC603e RISC Microprocessors User's Manual*.

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## 1.1 Overview

This section describes the features of the PID7t and describes briefly how those units interact.

The PID7t is a low-power implementation of the PowerPC microprocessor family of reduced instruction set computing (RISC) microprocessors. The PID7t implements the 32-bit portion of the PowerPC architecture specification, which provides 32-bit effective addresses and integer data types of 8, 16, and 32 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The PID7t provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the PID7t to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The PID7t is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the PID7t makes completion appear sequential.

The PID7t integrates four execution units—an integer unit (IU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for PID7t-based systems. Most integer instructions execute in one clock cycle.

The PID7t provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least-recently used (LRU) replacement algorithm. The PID7t also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The PID7t has a selectable 32- or 64-bit data bus and a 32-bit address bus. The PID7t interface protocol allows multiple masters to compete for system resources through a central external arbiter. The PID7t

provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The PID7t supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The PID7t uses an advanced, 2.5/3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

## 1.2 Features

This section summarizes features of the PID7t's implementation of the PowerPC architecture. Major features of the PID7t are as follows:

- High-performance, superscalar microprocessor
  - As many as three instructions issued and retired per clock
  - As many as five instructions in execution per clock
  - Single-cycle execution for most instructions
- Four independent execution units and two register files
  - BPU featuring static branch prediction
  - A 32-bit IU
  - LSU for data transfer between data cache and GPRs
  - SRU that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
  - Thirty-two GPRs for integer operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16-Kbyte data cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - 16-Kbyte instruction cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 64-entry, two-way set-associative ITLB
  - A 64-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions

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- Integrated power management
  - Low-power 2.5/3.3-volt design
  - Internal processor/bus clock multiplier that provides 2/1, 2.5/1, 3/1, 3.5/1, 4/1, 4.5/1, 5/1, 5.5/1, and 6/1 ratios
  - Three power saving modes: doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

# 1.3 General Parameters

The following list provides a summary of the general parameters of the PID7t:

| | |
|---|---|
| Technology | 0.25 $\mu$m CMOS, five-layer metal |
| Die size | 5.65 mm x 7.7 mm (44 $mm^2$) |
| Transistor count | 2.6 million |
| Logic design | Fully-static |
| Package | 255 ceramic ball grid array (CBGA) |
| Core power supply | 2.5 ± 5% V dc |
| I/O power supply | 3.3 ± 5% V dc |

# 1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PID7t.

## 1.4.1 DC Electrical Characteristics

The tables in this section describe the PID7t DC electrical characteristics. Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | Vdd | –0.3 to 2.75 | V |
| PLL supply voltage | AVdd | –0.3 to 2.75 | V |
| I/O supply voltage | OVdd | –0.3 to 3.6 | V |
| Input voltage | $V_{in}$ | –0.3 to 5.5 | V |
| Storage temperature range | $T_{stg}$ | –55 to 150 | °C |

**Notes**:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: $V_{in}$ must not exceed OVdd by more than 2.5 V at any time, including during power-on reset.
3. **Caution**: OVdd must not exceed Vdd/AVdd by more than 1.2 V at any time, including during power-on reset.
4. **Caution**: Vdd/AVdd must not exceed OVdd by more than 0.4 V at any time, including during power-on reset.


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Table 2 provides the recommended operating conditions for the PID7t.

**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | Vdd | 2.375 to 2.625 | V |
| PLL supply voltage | AVdd | 2.375 to 2.625 | V |
| I/O supply voltage | OVdd | 3.135 to 3.465 | V |
| Input voltage | $V_{in}$ | GND to 5.5 | V |
| Die-junction temperature | Tj | 0 to 105 | °C |

**Note:** These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3 provides the package thermal characteristics for the PID7t.

**Table 3. Package Thermal Characteristics**

| Characteristic | Symbol | Value | Rating |
|---|---|---|---|
| CBGA package die junction-to-case thermal resistance (typical) | $\theta_{JC}$ | 0.095 | °C/W |
| CBGA package die junction-to-ball thermal resistance (typical) | $\theta_{JB}$ | 3.5 | °C/W |

**Note:** Refer to Section 1.8, “System Design Information,” for more details about thermal management.

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Table 4 provides the DC electrical characteristics for the PID7t.

**Table 4. DC Electrical Specifications**

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage (all inputs except SYSCLK) | $V_{IH}$ | 2.0 | 5.5 | V | |
| Input low voltage (all inputs except SYSCLK) | $V_{IL}$ | GND | 0.8 | V | |
| SYSCLK input high voltage | $CV_{IH}$ | 2.4 | 5.5 | V | |
| SYSCLK input low voltage | $CV_{IL}$ | GND | 0.4 | V | |
| Input leakage current, $V_{in}$ = 3.465 V | $I_{in}$ | — | 30 | μA | 1,2 |
| $V_{in}$ = 5.5 V | $I_{in}$ | — | 300 | μA | 1,2 |
| Hi-Z (off-state) leakage current, $V_{in}$ = 3.465 V | $I_{TSI}$ | — | 30 | μA | 1,2 |
| $V_{in}$ = 5.5 V | $I_{TSI}$ | — | 300 | μA | 1,2 |
| Output high voltage, $I_{OH}$ = –7 mA | $V_{OH}$ | 2.4 | — | V | |
| Output low voltage, $I_{OL}$ = 7 mA | $V_{OL}$ | — | 0.4 | V | |
| Capacitance, $V_{in}$ = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | $C_{in}$ | — | 10.0 | pF | 3 |
| Capacitance, $V_{in}$ = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | $C_{in}$ | — | 15.0 | pF | 3 |

**Notes**:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. The leakage is measured for nominal OVdd and Vdd or both OVdd and Vdd must vary in the same direction (for example, both OVdd and Vdd vary by either +5% or -5%).
3. Capacitance is periodically sampled rather than 100% tested.

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Table 5 provides the power consumption for the PID7t.

**Table 5. Power Consumption**

| | Processor (CPU) Frequency | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 100 MHz | 133 MHz | 166 MHz | 200 MHz | 233 MHz | 266 MHz | 300 MHz | |
| **Full-On Mode (DPM Enabled)** | | | | | | | | |
| Typical | 1.1 | 1.6 | 2.1 | 2.5 | 3.1 | 3.5 | 4.0 | W |
| Maximum | 1.6 | 2.4 | 3.2 | 4.0 | 4.6 | 5.4 | 6.1 | W |
| **Doze Mode** | | | | | | | | |
| Typical | 0.55 | .7 | .9 | 1.1 | 1.3 | 1.5 | 1.8 | W |
| **Nap Mode** | | | | | | | | |
| Typical | 50 | 60 | 75 | 85 | 100 | 120 | 130 | mW |
| **Sleep Mode** | | | | | | | | |
| Typical | 45 | 50 | 55 | 65 | 75 | 90 | 100 | mW |
| **Sleep Mode—PLL Disabled** | | | | | | | | |
| Typical | 40 | 40 | 40 | 40 | 40 | 40 | 40 | mW |
| **Sleep Mode—PLL and SYSCLK Disabled** | | | | | | | | |
| Typical | 15 | 15 | 15 | 15 | 15 | 15 | 25 | mW |
| Maximum | 25 | 25 | 25 | 25 | 25 | 80 | 100 | mW |

**Notes**:

1. These values apply for all valid PLL_CFG[0–3] settings and do not include output driver power (OVdd) or analog supply power (AVdd). OVdd power is system dependent but is typically ≤ 10% of Vdd. Worst-case AVdd = 15 mW.
2. Typical power is an average value measured at Vdd = AVdd = 2.5 V, OVdd = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at 2.625 V using a worst-case instruction mix.

### 1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PID7t. These specifications are for 200, 266, and 300 MHz processor speed grades. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. All timings are specified respective to the rising edge of SYSCLK. PLL_CFG signals should be set prior to power up and not altered afterwards.

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### 1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. Parts are sold by maximum processor core frequency; see Section 1.9, “Ordering Information.”

**Table 6. Clock AC Timing Specifications**

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C

| Num | Characteristic | 200 MHz | | 266 MHz | | 300 MHz | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| | Processor frequency | 80 | 200 | 150 | 266 | 180 | 300 | MHz | 1,6 |
| | VCO frequency | 300 | 400 | 300 | 532 | 360 | 600 | MHz | 1 |
| | SYSCLK frequency | 25 | 66.7 | 25 | 75 | 33.3 | 75 | MHz | 1 |
| 1 | SYSCLK cycle time | 13.3 | 40 | 13.3 | 40 | 13.3 | 30 | ns | |
| 2,3 | SYSCLK rise and fall time | — | 2.0 | — | 2.0 | — | 2.0 | ns | 2 |
| 4 | SYSCLK duty cycle measured at 1.4 V | 40.0 | 60.0 | 40.0 | 60.0 | 40.0 | 60.0 | % | 3 |
| | SYSCLK jitter | — | ±150 | — | ±150 | — | ±150 | ps | 4 |
| | PID7t internal PLL-relock time | — | 100 | — | 100 | — | 100 | µs | 3,5 |

**Notes**:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8, “System Design Information,” for valid PLL_CFG[0–3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Cycle-to-cycle jitter, and is guaranteed by design. The total input jitter (short term and long term combined) must be under ±150 ps to guarantee the input/output timing of Section 1.4.2.2, “Input AC Specifications,” and Section 1.4.2.3, “Output AC Specifications.”
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum time required for PLL lock after a stable Vdd, OVdd, AVdd, and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 µs) during the power-on reset sequence.
6. Operation below 150 MHz is supported only by PLL_CFG[0–3] = 0b0101. Refer to Section 1.8.1, “PLL Configuration” for additional information.

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Figure 1 provides the SYSCLK input timing diagram.

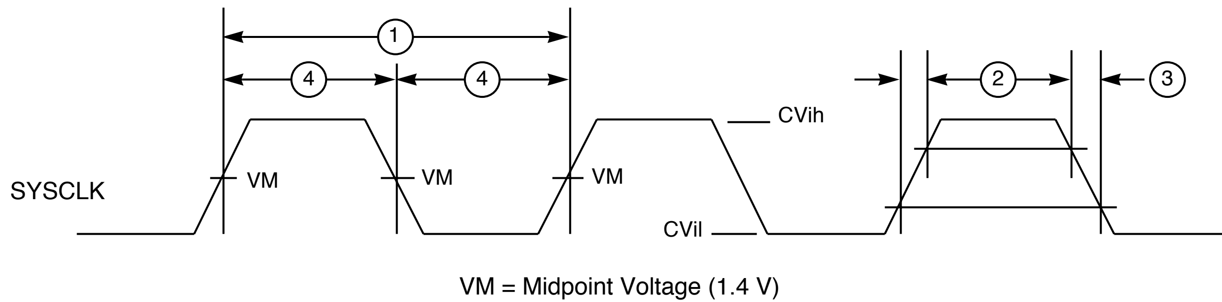


**Figure 1. SYSCLK Input Timing Diagram**

### 1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the PID7t as defined in Figure 2 and Figure 3.

**Table 7. Input AC Timing Specifications[1]**

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ Tj ≤105° C

| Num | Characteristic | 200, 266, 300 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| 10a | Address/data/transfer attribute inputs valid to SYSCLK (input setup) | 2.5 | — | ns | 2 |
| 10b | All other inputs valid to SYSCLK (input setup) | 3.5 | — | ns | 3 |
| 10c | Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$) | 8 | — | $t_{sysclk}$ | 4, 5, 6, 7 |
| 11a | SYSCLK to address/data/transfer attribute inputs invalid (input hold) | 1.0 | — | ns | 2 |
| 11b | SYSCLK to all other inputs invalid (input hold) | 1.0 | — | ns | 3 |
| 11c | $\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$) | 0 | — | ns | 4, 6, 7 |

**Notes**:

1. Input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Address/data/transfer attribute input signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TC[0–1], $\overline{\text{TBST}}$, TSIZ[0–2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].
3. All other input signals are composed of the following—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
5. $t_{sysclk}$ is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.


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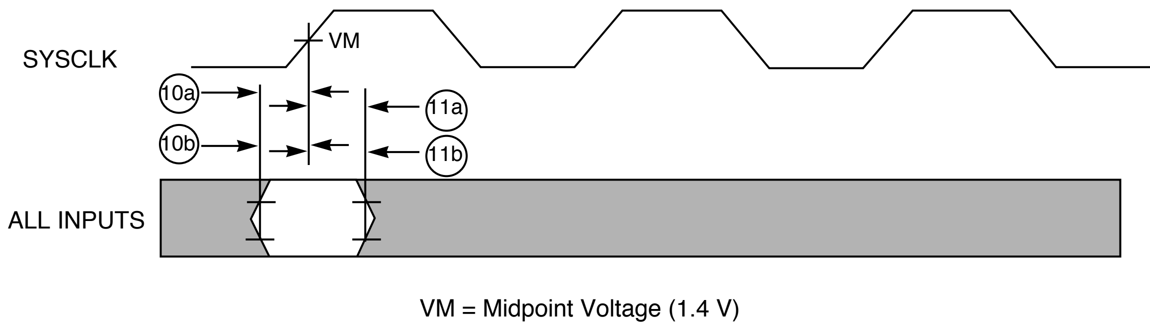
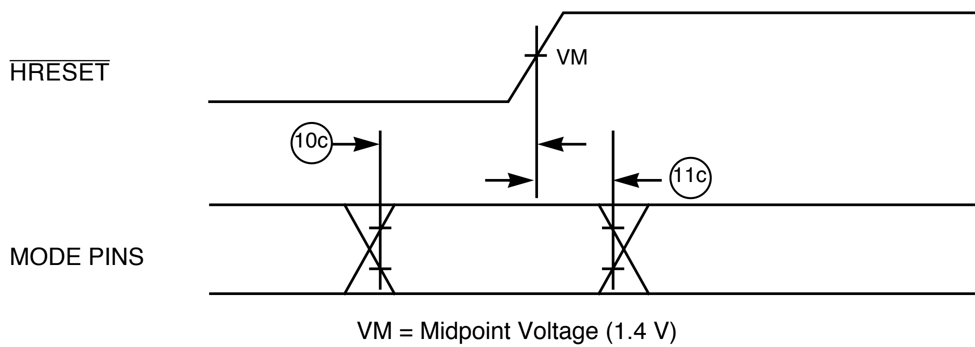
Figure 2 provides the input timing diagram for the PID7t.




VM = Midpoint Voltage (1.4 V)

**Figure 2. Input Timing Diagram**

Figure 3 provides the mode select input timing diagram for the PID7t.




VM = Midpoint Voltage (1.4 V)

**Figure 3. Mode Select Input Timing Diagram**

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### 1.4.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for the PID7t as defined in Figure 4.

**Table 8. Output AC Timing Specifications[1]**

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, 0 ≤ Tj ≤ 105 °C, $C_L$ = 50 pF (unless otherwise noted)

| Num | Characteristic | 200, 266, 300 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| 12 | SYSCLK to output driven (output enable time) | 1.0 | — | ns | |
| 13a | SYSCLK to output valid (5.5 V to 0.8 V—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$) | — | 9.0 | ns | 3 |
| 13b | SYSCLK to output valid ($\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$) | — | 8.0 | ns | 5 |
| 14a | SYSCLK to output valid (5.5 V to 0.8 V—all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$) | — | 11.0 | ns | 3 |
| 14b | SYSCLK to output valid (all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$) | — | 9.0 | ns | 5 |
| 15 | SYSCLK to output invalid (output hold) | 1.0 | — | ns | 2 |
| 16 | SYSCLK to output high impedance (all except $\overline{\text{ARTRY}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$) | — | 8.0 | ns | |
| 17 | SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, high impedance after precharge | — | 1.0 | $t_{sysclk}$ | 4, 6 |
| 18 | SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge | — | 7.5 | ns | |
| 19 | SYSCLK to $\overline{\text{ARTRY}}$ precharge enable | 0.2 * $t_{sysclk}$ + 1.0 | — | ns | 2, 4, 7 |
| 20 | Maximum delay to $\overline{\text{ARTRY}}$ precharge | — | 1.0 | $t_{sysclk}$ | 4, 7 |
| 21 | SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge | — | 2.0 | $t_{sysclk}$ | 5,7 |

**Notes**:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 4).
2. This minimum parameter assumes $C_L$ = 0 pF.
3. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
4. $t_{sysclk}$ is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
5. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
6. Nominal precharge width for $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ is 0.5 $t_{sysclk}$.
7. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 $t_{sysclk}$.

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Figure 4 provides the output timing diagram for the PID7t.

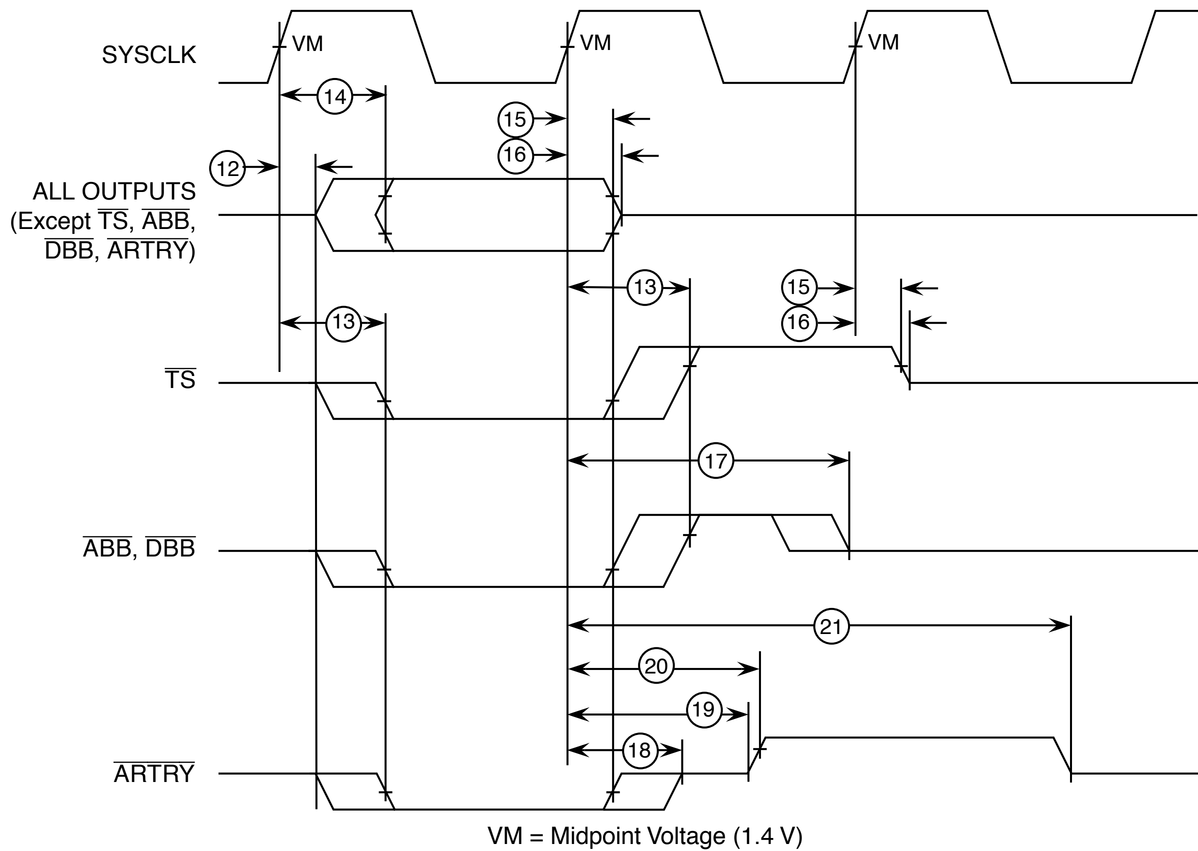


**Figure 4. Output Timing Diagram**


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### 1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications as defined in Figure 5 through Figure 8.

**Table 9. JTAG AC Timing Specifications**

Vdd = AVdd = 2.5 ± 5% V dc, OVdd = 3.3 ± 5%, GND = 0 V dc, 0 ≤ Tj ≤ 105° C, $C_L$ = 50 pF

| Num | Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| | TCK frequency of operation | 0 | 16 | MHz | |
| 1 | TCK cycle time | 62.5 | — | ns | |
| 2 | TCK clock pulse width measured at 1.4 V | 25 | — | ns | |
| 3 | TCK rise and fall times | 0 | 3 | ns | |
| 4 | $\overline{\text{TRST}}$ setup time to TCK rising edge | 13 | — | ns | 1 |
| 5 | $\overline{\text{TRST}}$ assert time | 40 | — | ns | |
| 6 | Boundary scan input data setup time | 6 | — | ns | 2 |
| 7 | Boundary scan input data hold time | 27 | — | ns | 2 |
| 8 | TCK to output data valid | 4 | 25 | ns | 3 |
| 9 | TCK to output high impedance | 3 | 24 | ns | 3 |
| 10 | TMS, TDI data setup time | 0 | — | ns | |
| 11 | TMS, TDI data hold time | 25 | — | ns | |
| 12 | TCK to TDO data valid | 4 | 24 | ns | |
| 13 | TCK to TDO high impedance | 3 | 15 | ns | |

**Notes**:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.

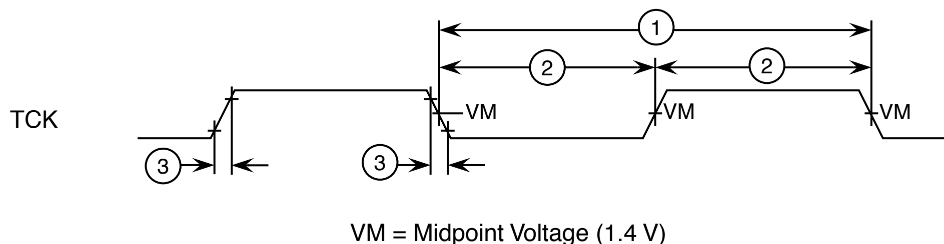


**Figure 5. JTAG Clock Input Timing Diagram**

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

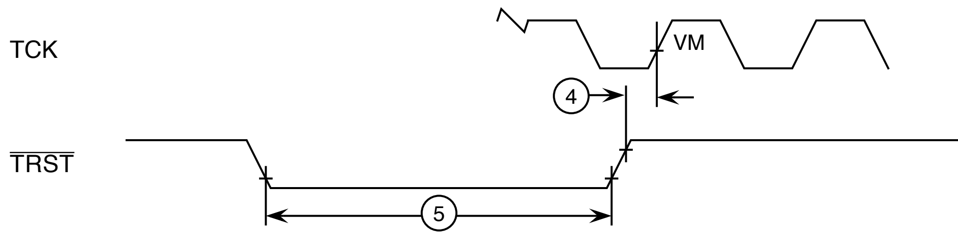


**Figure 6. $\overline{\text{TRST}}$ Timing Diagram**

Figure 7 provides the boundary-scan timing diagram.

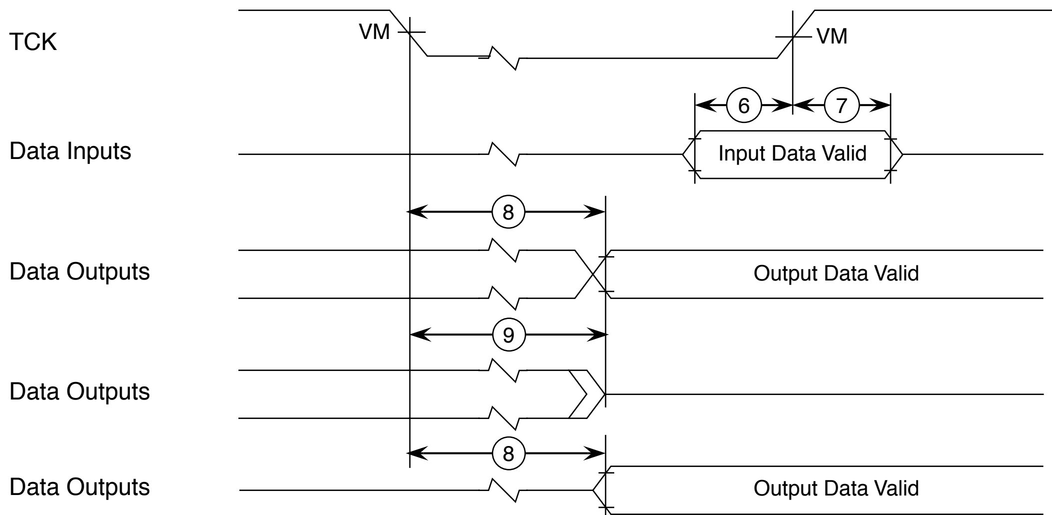


**Figure 7. Boundary-Scan Timing Diagram**

Figure 8 provides the test access port timing diagram.

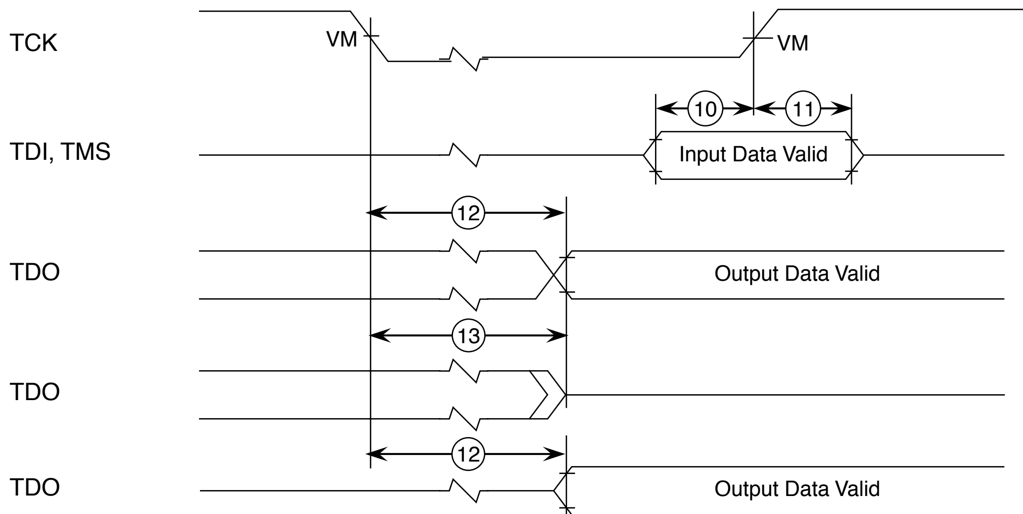


**Figure 8. Test Access Port Timing Diagram**


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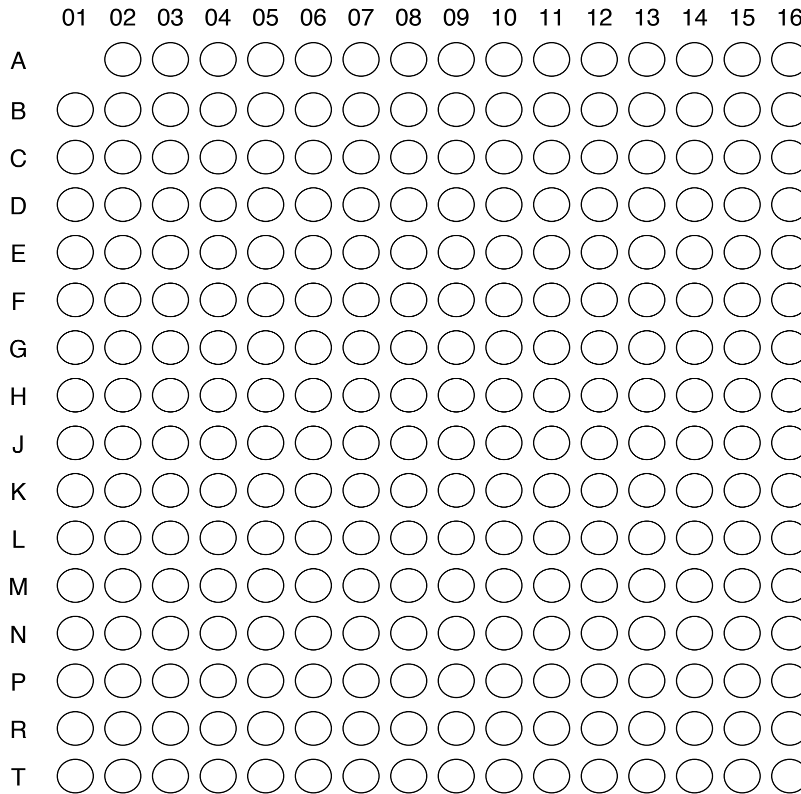
## 1.5 Pin Assignments

Figure 9 (in part A) shows the pinout of the CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

**Part A**




**Part B**

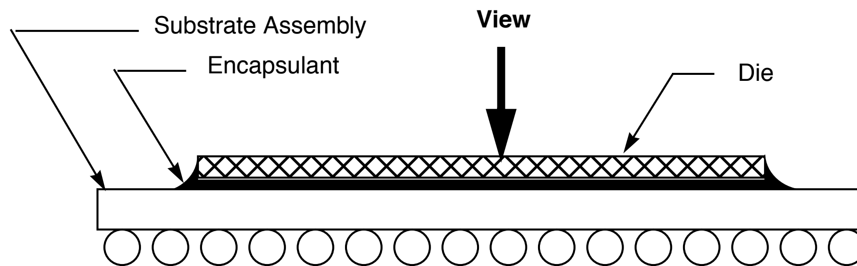



**Figure 9. Pinout of the CBGA Package as Viewed from the Top Surface**

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# 1.6 Pinout Listings

Table 10 provides the pinout listing for the PID7t CBGA package.

**Table 10. Pinout Listing for the 255-Pin CBGA Package**

| Signal Name | Pin Number | Active | I/O |
|---|---|---|---|
| A[0–31] | C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01 | High | I/O |
| $\overline{AACK}$ | L02 | Low | Input |
| $\overline{ABB}$ | K04 | Low | I/O |
| AP[0–3] | C01, B04, B03, B02 | High | I/O |
| $\overline{APE}$ | A04 | Low | Output |
| $\overline{ARTRY}$ | J04 | Low | I/O |
| AVDD | A10 | — | — |
| $\overline{BG}$ | L01 | Low | Input |
| $\overline{BR}$ | B06 | Low | Output |
| $\overline{CI}$ | E01 | Low | Output |
| $\overline{CKSTP_IN}$ | D08 | Low | Input |
| $\overline{CKSTP_OUT}$ | A06 | Low | Output |
| CLK_OUT | D07 | — | Output |
| CSE[0–1] | B01, B05 | High | Output |
| $\overline{DBB}$ | J14 | Low | I/O |
| $\overline{DBG}$ | N01 | Low | Input |
| $\overline{DBDIS}$ | H15 | Low | Input |
| $\overline{DBWO}$ | G04 | Low | Input |
| DH[0–31] | P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04 | High | I/O |
| DL[0–31] | K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04 | High | I/O |
| DP[0–7] | M02, L03, N02, L04, R01, P02, M04, R02 | High | I/O |
| $\overline{DPE}$ | A05 | Low | Output |
| $\overline{DRTRY}$ | G16 | Low | Input |
| $\overline{GBL}$ | F01 | Low | I/O |



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Table 10. Pinout Listing for the 255-Pin CBGA Package (Continued)

| Signal Name | Pin Number | Active | I/O |
|---|---|---|---|
| GND | C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12 | — | — |
| HRESET | A07 | Low | Input |
| INT | B15 | Low | Input |
| L1_TSTCLK [1] | D11 | — | Input |
| L2_TSTCLK [1] | D12 | — | Input |
| LSSD_MODE [1] | B10 | Low | Input |
| MCP | C13 | Low | Input |
| NC (No-Connect) | B07, B08, C03, C06, C08, D05, D06, H04, J16 | — | — |
| OVDD | C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10 | — | — |
| PLL_CFG[0–3] | A08, B09, A09, D09 | High | Input |
| QACK | D03 | Low | Input |
| QREQ | J03 | Low | Output |
| RSRV | D01 | Low | Output |
| SMI | A16 | Low | Input |
| SRESET | B14 | Low | Input |
| SYSCLK | C09 | — | Input |
| TA | H14 | Low | Input |
| TBEN | C02 | High | Input |
| TBST | A14 | Low | I/O |
| TC[0–1] | A02, A03 | High | Output |
| TCK | C11 | — | Input |
| TDI | A11 | High | Input |
| TDO | A12 | High | Output |
| TEA | H13 | Low | Input |
| TLBISYNC | C04 | Low | Input |
| TMS | B11 | High | Input |
| TRST | C10 | Low | Input |
| TS | J13 | Low | I/O |


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**Table 10. Pinout Listing for the 255-Pin CBGA Package (Continued)**

| Signal Name | Pin Number | Active | I/O |
|---|---|---|---|
| TSIZ[0–2] | A13, D10, B12 | High | Output |
| TT[0–4] | B13, A15, B16, C14, C15 | High | I/O |
| $\overline{\text{WT}}$ | D02 | Low | Output |
| VDD [2] | F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11 | — | — |
| VOLTDETGND [3] | F03 | Low | Output |

**Notes:**

1. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
3. NC (no-connect) in the PID6; internally tied to GND in the PID7v and PID7t CBGA package to indicate to the power supply that a low-voltage processor is present.

# 1.7 Package Descriptions

The following sections provide the package parameters and the mechanical dimensions for the PID7t. Note that the PID7t is currently offered only in the ceramic ball grid array (CBGA) package.

## 1.7.1 CBGA Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

### 1.7.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm x 21 mm, 255-lead ceramic ball grid array (CBGA).

| | |
|---|---|
| Package outline | 21 mm x 21 mm |
| Interconnects | 255 |
| Pitch | 1.27 mm (50 mil) |
| Package height | Minimum: 2.45 mm<br>Maximum: 3.00 mm |
| Ball diameter | 0.89 mm (35 mil) |
| Maximum heat sink force | 10 lbs |

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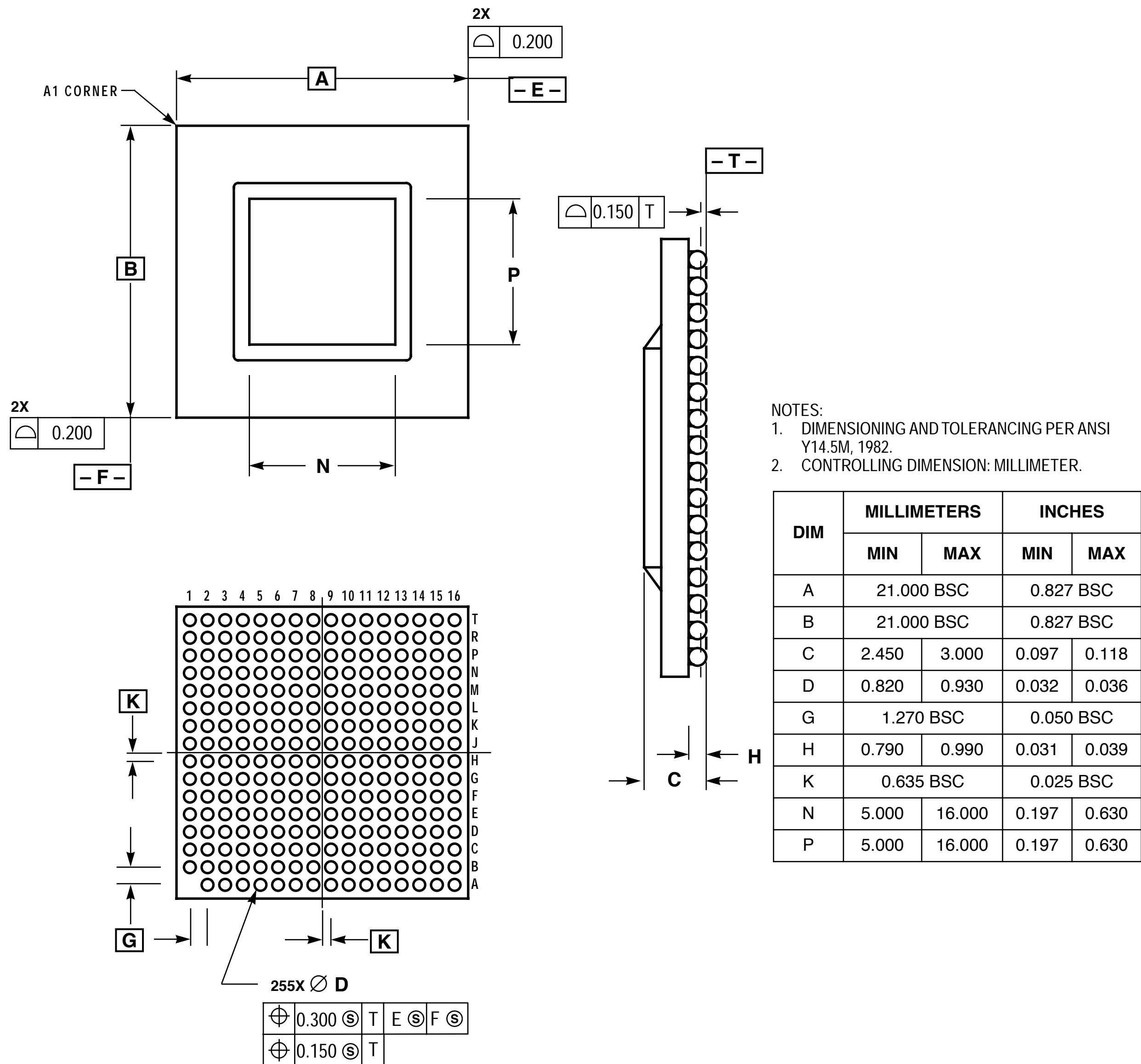
### 1.7.1.2 Mechanical Dimensions of the CBGA Package

Figure 10 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 21.000 BSC | | 0.827 BSC | |
| B | 21.000 BSC | | 0.827 BSC | |
| C | 2.450 | 3.000 | 0.097 | 0.118 |
| D | 0.820 | 0.930 | 0.032 | 0.036 |
| G | 1.270 BSC | | 0.050 BSC | |
| H | 0.790 | 0.990 | 0.031 | 0.039 |
| K | 0.635 BSC | | 0.025 BSC | |
| N | 5.000 | 16.000 | 0.197 | 0.630 |
| P | 5.000 | 16.000 | 0.197 | 0.630 |

**Figure 10. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package**

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## 1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the PID7t.

### 1.8.1 PLL Configuration

The PID7t PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PID7t is shown in Table 11 for nominal frequencies.

**Table 11. PLL Configuration**

| PLL_CFG[0–3] | CPU Frequency in MHz (VCO Frequency in MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to VCO Multiplier | Bus 25 MHz | Bus 33.33 MHz | Bus 40 MHz | Bus 50 MHz | Bus 60 MHz | Bus 66.67 MHz | Bus 75 MHz |
| 0100 | 2x | 2x | — | — | — | — | — | ) | 150 (300) |
| 0101 | 2x | 4x | — | — | 80 (320) | 100 (400) | 120 (480) | 133 (532) | 150 (600) |
| 0110 | 2.5x | 2x | — | — | — | — | 150 (300) | 166 (333) | 187 (375) |
| 1000 | 3x | 2x | — | — | — | 150 (300) | 180 (360) | 200 (400) | 225 (450) |
| 1110 | 3.5x | 2x | — | — | | 175 (350) | 210 (420) | 233 (466) | 263 (525) |
| 1010 | 4x | 2x | — | | 160 (320) | 200 (400) | 240 (480) | 267 (533) | 300 (600) |
| 0111 | 4.5x | 2x | — | 150 (300) | 180 (360) | 225 (450) | 270 (540) | 300 (600) | — |
| 1011 | 5x | 2x | — | 166 (333) | 200 (400) | 250 (500) | 300 (600) | — | — |
| 1001 | 5.5x | 2x | — | 183 (366) | 220 (440) | 275 (550) | — | — | — |
| 1101 | 6x | 2x | 150 (300) | 200 (400) | 240 (480) | 300 (600) | — | — | — |
| 0011 | PLL bypass | | | | | | | | |
| 1111 | Clock off | | | | | | | | |

**Notes**:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not supported; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   **Note**: The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the PID7t regardless of the SYSCLK input.

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### 1.8.2 PLL Power Supply Filtering

The AVdd power signal is provided on the PID7t to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 11. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible. The 0.1 $\mu$F capacitor should be closest to the AVdd pin, followed by the 10 $\mu$F capacitor, and finally the 10 Ω resistor to Vdd. These traces should be kept short and direct.

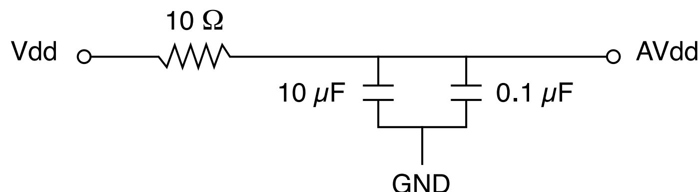


**Figure 11. PLL Power Supply Filter Circuit**

### 1.8.3 Decoupling Recommendations

Due to the PID7t's dynamic power management feature, large address and data buses, and high operating frequencies, the PID7t can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PID7t system, and the PID7t itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd and OVdd pin of the PID7t. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd or OVdd pin. Suggested values for the Vdd pins—220 pF (ceramic), 0.01 $\mu$F (ceramic), and 0.1 $\mu$F (ceramic). Suggested values for the OVdd pins—0.01 $\mu$F (ceramic), 0.1 $\mu$F (ceramic), and 10 $\mu$F (tantalum). Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 $\mu$F (AVX TPS tantalum) or 330 $\mu$F (AVX TPS tantalum).

### 1.8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, and GND pins of the PID7t.

### 1.8.5 Pull-up Resistor Requirements

The PID7t requires high-resistive (weak: 10 KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PID7t or other bus master. These signals are—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, and $\overline{\text{ARTRY}}$.


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In addition, the PID7t has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 KΩ–10 KΩ) if they are used by the system. These signals are—$\overline{\text{APE}}$, $\overline{\text{DPE}}$, and $\overline{\text{CKSTP_OUT}}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the PID7t must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PID7t. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are—A[0–31], AP[0–3], TT[0–4], $\overline{\text{TBST}}$, and $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

## 1.8.6 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (CBGA package); see Figure 12. This spring force should not exceed 5.5 pounds of force.

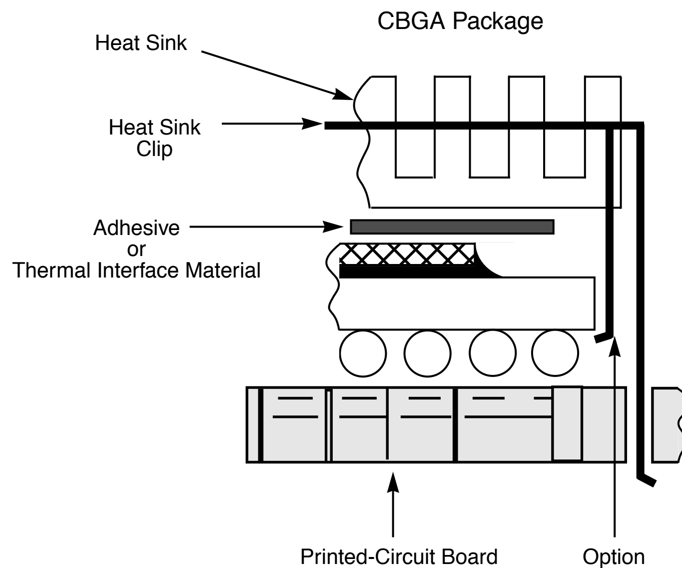


**Figure 12. Package Exploded Cross-Sectional View with Several Heat Sink Options**



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The board designer can choose between several types of heat sinks to place on the PID7t. There are several commercially-available heat sinks for the PID7t provided by the following vendors:

| | |
|---|---|
| Chip Coolers Inc.<br>333 Strawberry Field Rd.<br>Warwick, RI 02887-6979 | 800-227-0254 (USA/Canada)<br>401-739-7600 |
| International Electronic Research Corporation (IERC)<br>135 W. Magnolia Blvd.<br>Burbank, CA 91502 | 818-842-7277 |
| Thermalloy<br>2021 W. Valley View Lane<br>P.O. Box 810839<br>Dallas, TX 75731 | 214-243-4321 |
| Wakefield Engineering<br>60 Audubon Rd.<br>Wakefield, MA 01880 | 617-245-5900 |
| Aavid Engineering<br>One Kool Path<br>Laconia, NH 03247-0440 | 603-528-3400 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

### 1.8.6.1 Internal Package Conduction Resistance

For this packaging technology the intrinsic thermal conduction resistance (shown in Table 3) versus the external thermal resistance paths are shown in Figure 13 for a package with an attached heat sink mounted to a printed-circuit board.

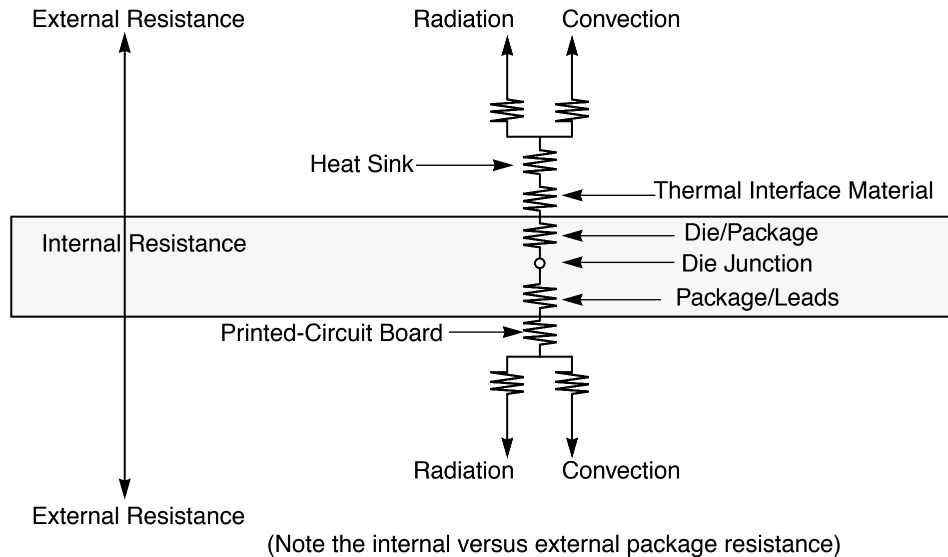


**Figure 13. Package with Heat Sink Mounted to a Printed-Circuit Board**



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### 1.8.6.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 14 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 12). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

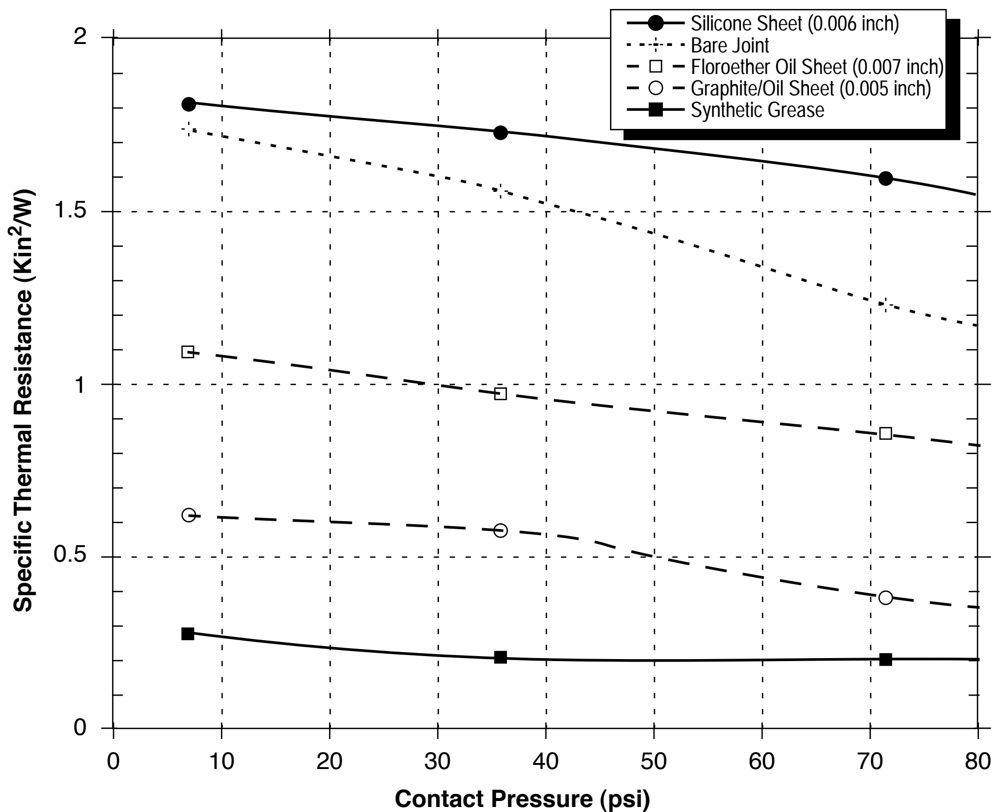


**Figure 14. Thermal Performance of Select Thermal Interface Material**

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The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

| | |
|---|---|
| Dow-Corning Corporation<br>Dow-Corning Electronic Materials<br>PO Box 0997<br>Midland, MI 48686-0997 | 517-496-4000 |
| Chomerics, Inc.<br>77 Dragon Court<br>Woburn, MA 01888-4850 | 617-935-4850 |
| Thermagon Inc.<br>3256 West 25th Street<br>Cleveland, OH 44109-1668 | 216-741-7659 |
| Loctite Corporation<br>1001 Trout Brook Crossing<br>Rocky Hill, CT 06067 | 860-571-5100 |
| AI Technology (e.g., EG7655)<br>1425 Lower Ferry Rd.<br>Trent, NJ 08618 | 609-882-2332 |

The following section provides a heat sink selection example using one of the commercially available heat sinks.

### 1.8.6.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

**Where**:

$T_j$ is the die-junction temperature
$T_a$ is the inlet cabinet ambient temperature
$T_r$ is the air temperature rise within the computer cabinet
$\theta_{jc}$ is the die junction-to-case thermal resistance
$\theta_{int}$ is the adhesive or interface material thermal resistance
$\theta_{sa}$ is the heat sink base-to-ambient thermal resistance
$P_d$ is the power dissipated by the device

During operation the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 2. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_a$) may range from 30 to 40 °C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5 to 10 °C. The thermal resistance of the thermal interface material ($\theta_{int}$) is typically about 1 °C/W. Assuming a $T_a$ of 30 °C, a $T_r$ of 5 °C a CBGA package $\theta_{jc}$ = 0.095, and a power consumption ($P_d$) of 3.0 Watts, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j$ = 30 °C + 5 °C + (0.095 °C/W + 1.0 °C/W + $R_{sa}$) * 3.0 W



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For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($R_{sa}$) versus airflow velocity is shown in Figure 15.

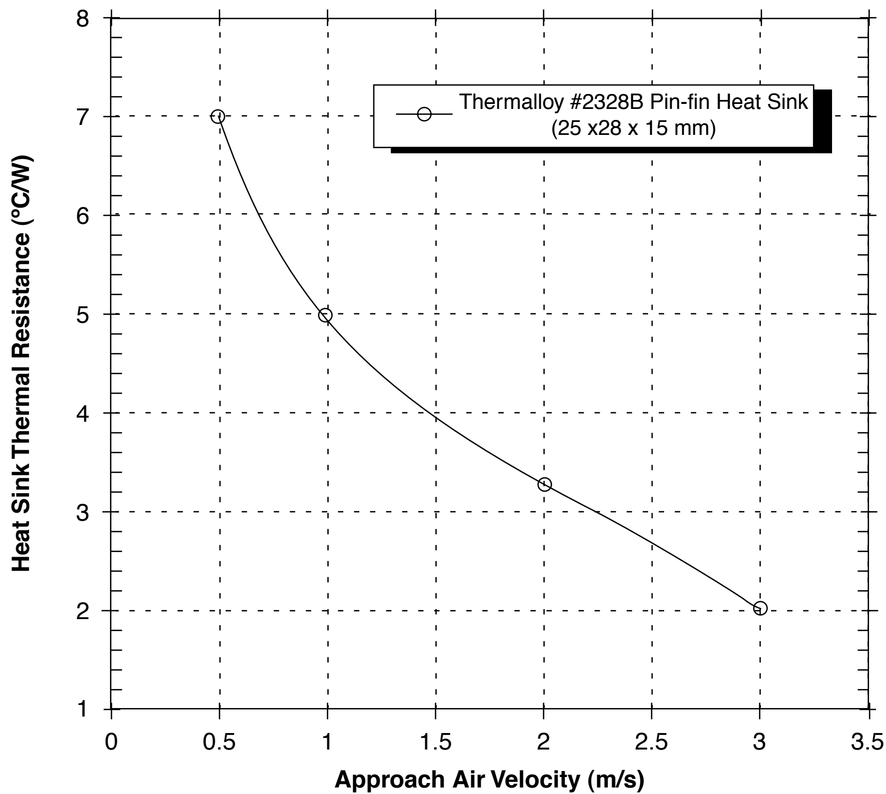


**Figure 15. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

Assuming an air velocity of 0.5 m/s, we have an effective $R_{sa}$ of 7 °C/W, thus

$$T_j = 30°C + 5°C + (0.095\ °C/W + 1.0\ °C/W + 7\ °C/W) * 3.0\ W,$$

resulting in a die-junction temperature of approximately 60 °C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.


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## 1.9 Ordering Information

Figure 16 provides the part numbering nomenclature for the PID7t. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office.

In addition to the processor frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancement(s) in the part from the original design. The application modifier may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

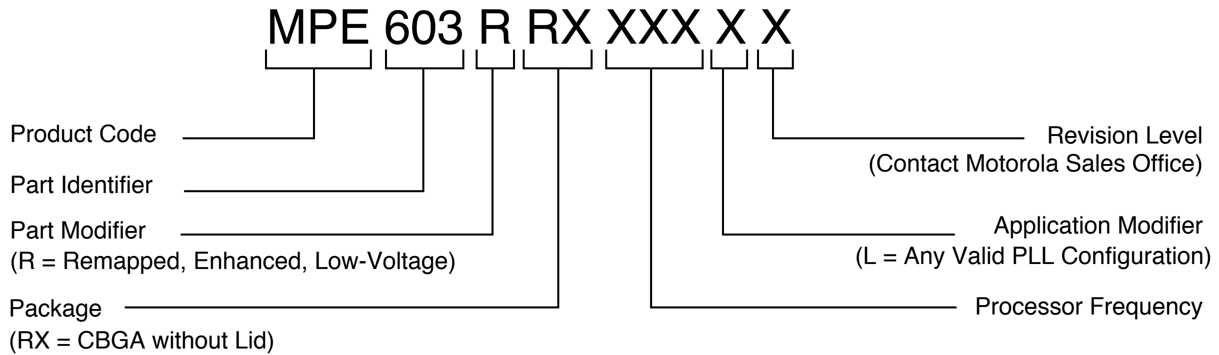


**Figure 16. Part Number Key**

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