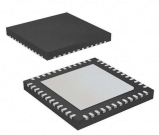


PF7100_BA2 — NXP Standard

Configuration report for PF7100 OTP program ID: A2 rev B

Rev. 1.1 — 28 July 2020 **Report**

1 General description

The PF7100 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 processors. It features five high efficiency buck converters and two linear regulators for powering the processor, memory and miscellaneous peripherals.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

Electrical characteristics are mantained in the PF7100 data sheet

2 Features and benefits

- Up to five high efficiency buck converters
- Two linear regulators with load switch options
- Independent OV/UV monitoring circuits
- Dual always-on RTC supply
- Watchdog timer/monitor
- AEC-Q100 grade 2 qualified
- Safety mechanisms to fit ASIL B applications
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 48-pin 7 x 7 mm QFN Package (Automotive and Industrial grades available)

3 Applications

- Automotive infotainment
- V2X
- High-end consumer and industrial

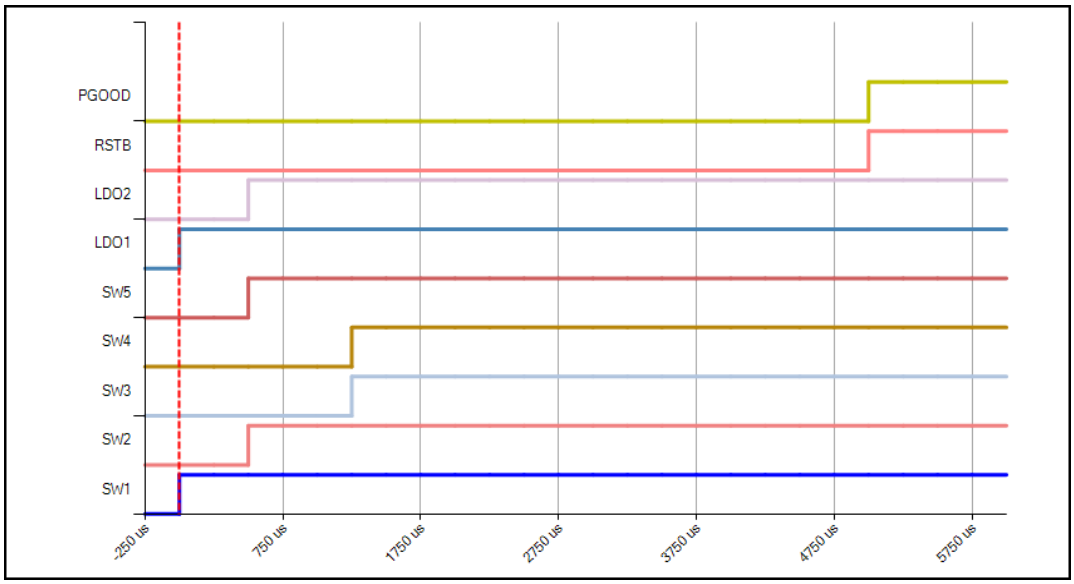
4 Ordering information

Table 1. Ordering information

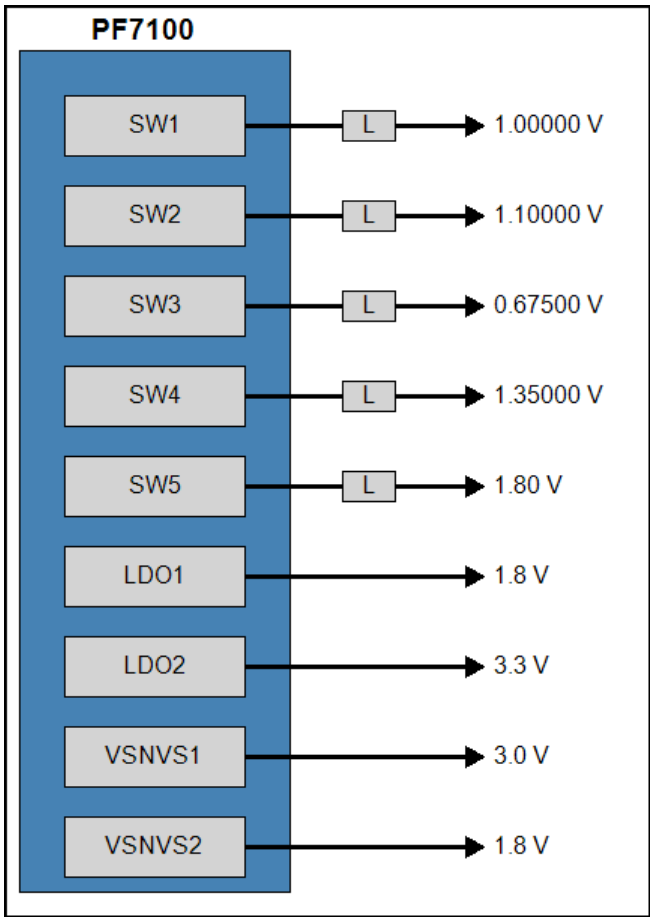
Type number[1]	Package		
	Name	Description	Version
MPF7100BVBA2ES	WF-Type QFN48 ES	QFN48 plastic thermally enhanced very thin quad flat non-leaded package. Wettable flanks; 48 terminals; 0.5mm pitch; 7 mm x 7 mm x 0.85 mm body	SOT619-27(D)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



6 Hardware configuration diagram



7 System OTP configuration

See PF7100 datasheet for parametric details. The OTP configuration summary for A2 sequence ID is provided in Tables below.

Table 2. System configuration

Functional block	Feature	OTP selection
System configuration	I2C address	0x08
	I2C CRC	Enabled
	I2C Secure write	Secure write disabled
	VIN OVLO monitor	Enabled
	VIN OVLO debounce	100 µs
	VIN OVLO shutdown	Disabled
	Maximum fault count	Disabled
	Fault timer	Disabled
	Fail-safe state	Disabled
	Fail-safe maximum count	16
	Fail-safe OK timer	60 min
Watchdog monitoring	WDI mode	Hard WD reset
	WDI polatiry	Rising edge detection
	WDI in standby	WDI disabled in standby
	WD counter	WD counter disabled
	WD counter in standby	WD counter disabled
	WD clear window	100% window
	Maximum time-out steps	8 steps
	WD duration	1024 ms
	Maximum WD events	16 events
Clock management	Switching frequency	2.5 MHz
	SYNCIN range	2000 KHz to 3000 KHz
	SYNCIN operation	SYNCIN disabled
	SYNCOUT operation	SYNCOUT disabled
	Frequency spread spectrum	FSS disabled
	FSS range	FSS Range set to 5%

Table 3. I/Os configuration

Functional block	Feature	OTP selection
I/O Configuration	PWRON mode	Level sensitive
	PWRON debounce	32 ms
	PWRON reset mode	Shutdown on TRESET
	TRESET delay	2 seconds
	STANDBY polarity	STANDBY Active high
	PGOOD pin mode	PGOOD indicator
	OV/UV check on power-up	No OV/UV checked at power-up
	XFAILB operation	XFAILB pin disabled
	EWARN time	0.1 ms
	FSOB soft fault event	FSOB ignores soft faults
	FSOB hard fault event	FSOB ignores hard faults
	FSOB WDI event	FSOB ignores WDI faults
	FSOB WDC event	FSOB ignores WD counter faults
	FSOB operating mode	Fault safe state mode

Table 4. Sequencer configuration

Functional block	Feature	OTP selection
SW configurations	SW1 multi-phase selector	SW1 & SW2 single phase
	SW4 multi-phase selector	SW3 & SW4 single phase
	Default SW operation	PWM mode
	SW3 VTT mode	VTT mode enabled
	VTT discharge mode	High impedance
	Bandgap monitor reaction	Power stage disabled
Power-up sequence	Sequencer time base	250 µs
	SW1 sequence	Slot 0
	SW2 sequence	Slot 2
	SW3 sequence	Slot 5
	SW4 sequence	Slot 5
	SW5 sequence	Slot 2
	LDO1 sequence	Slot 0
	LDO2 sequence	Slot 2
	RESETBMCU sequence	Slot 20
	PGOOD sequence	Slot 20
Power down sequence	Power down mode	Mirror power down
	SW1 power down group	Group 4 (1st)
	SW2 power down group	Group 4 (1st)
	SW3 power down group	Group 4 (1st)
	SW4 power down group	Group 4 (1st)
	SW5 power down group	Group 4 (1st)
	LDO1 power down group	Group 4 (1st)
	LDO2 power down group	Group 4 (1st)
	PGOOD power down group	Group 4 (1st)
	RESETBMCU power down group	Group 4 (1st)
Power down delays	GRP1 delay	120 µs
	GRP2 delay	120 µs
	GRP3 delay	120 µs
	GRP4 delay	120 µs
	RESETBMCU delay	No delay
	Power down delay	5.0 ms

Table 5. Switching regulators

Functional block	Feature	OTP selection
SW1	SW1 output voltage	1.00000 V
	SW1 DVS ramp	7.81 / 5.21 mV/µs
	SW1 UV threshold	93%
	SW1 OV threshold	107%
	SW1 current limit	4.6 A
	SW1 inductor	1.0 µH
	SW1 phase	45°
	SW1 PGOOD control	PGOOD control enabled
	SW1 WD bypass	Reset on soft WD
	SW1 OV bypass	OV active
	SW1 UV bypass	UV active
	SW1 ILIM bypass	ILIM bypassed
SW2	SW2 output voltage	1.10000 V
	SW2 DVS ramp	7.81 / 5.21 mV/µs
	SW2 UV threshold	93%
	SW2 OV threshold	107%
	SW2 current limit	4.6 A
	SW2 inductor	1 µH
	SW2 phase	90°
	SW2 PGOOD control	PGOOD control enabled
	SW2 WD bypass	Reset on soft WD
	SW2 OV bypass	OV active
	SW2 UV bypass	UV active
	SW2 ILIM bypass	ILIM bypassed
SW3	SW3 output voltage	0.67500 V
	SW3 DVS ramp	7.81 / 5.21 mV/µs
	SW3 UV threshold	93%
	SW3 OV threshold	107%
	SW3 current limit	4.6 A
	SW3 inductor	1 µH
	SW3 phase	135°
	SW3 PGOOD control	PGOOD control enabled
	SW3 WD bypass	Reset on soft WD
	SW3 OV bypass	OV active
	SW3 UV bypass	UV active
	SW3 ILIM bypass	ILIM bypassed

Table 5. Switching regulators(cont)

Functional block	Feature	OTP selection
SW4	SW4 output voltage	1.35000 V
	SW4 DVS ramp	7.81 / 5.21 mV/µs
	SW4 UV threshold	93%
	SW4 OV threshold	107%
	SW4 current limit	4.6 A
	SW4 inductor	1 µH
	SW4 phase	180°
	SW4 PGOOD control	PGOOD control enabled
	SW4 WD bypass	Reset on soft WD
	SW4 OV bypass	OV active
	SW4 UV bypass	UV active
	SW4 ILIM bypass	ILIM bypassed
SW5	SW5 output voltage	1.80 V
	SW5 UV threshold	93%
	SW5 OV threshold	107%
	SW5 current limit	4.6 A
	SW5 inductor	1 µH
	SW5 phase	0°
	SW5 PGOOD control	PGOOD control enabled
	SW5 WD bypass	Reset on soft WD
	SW5 OV bypass	OV active
	SW5 UV bypass	UV active
	SW5 ILIM bypass	ILIM bypassed

Table 6. LDO regulators

Functional block	Feature	OTP selection
LDO1	LDO1 output voltage	1.8 V
	LDO1 UV threshold	93%
	LDO1 OV threshold	107%
	LDO1 PGOOD control	PGOOD control enabled
	LDO1 WD bypass	Reset on soft WD
	LDO1 mode	LDO mode
	LDO1 OV bypass	OV active
	LDO1 UV bypass	UV active
	LDO1 ILIM bypass	ILIM bypassed
LDO2	LDO2 Output voltage	3.3 V
	LDO2 UV threshold	89%
	LDO2 OV threshold	111%
	LDO2 PGOOD control	PGOOD control enabled
	LDO2 WD bypass	Reset on soft WD
	LDO2 mode	LDO mode
	LDO2EN hardware control	I2C control only
	VSELECT hardware control	VLDO2 set by VSELECT pin
	LDO2 OV BYPASS	OV active
	LDO2 UV BYPASS	UV active
	LDO2 ILIM BYPASS	ILIM bypassed
VSNVS	VSNVS1 output voltage	3.0 V
	VSNVS2 output voltage	1.8 V

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