Document Number: MRF19030-2
Rev. 14, 10/2008

RoHS

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for class AB PCN and PCS base station applications with frequencies from 1800 to 2000 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

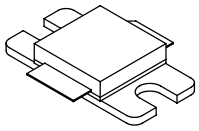
- CDMA Performance @ 1930 MHz, 26 Volts
  IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
  885 kHz — -47 dBc in 30 kHz BW
  1.25 MHz — -55 dBc in 12.5 kHz BW
  2.25 MHz — -55 dBc in 1 MHz BW
  Output Power — 4.5 Watts Avg.
  Power Gain — 13.5 dB
  Efficiency — 17%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1960 MHz, 30 Watts CW Output Power

Features

- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40μ″ Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF19030LR3

1930-1990 MHz, 30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFET



CASE 465E-04, STYLE 1
NI-400

ARCHIVE INFORMATION

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

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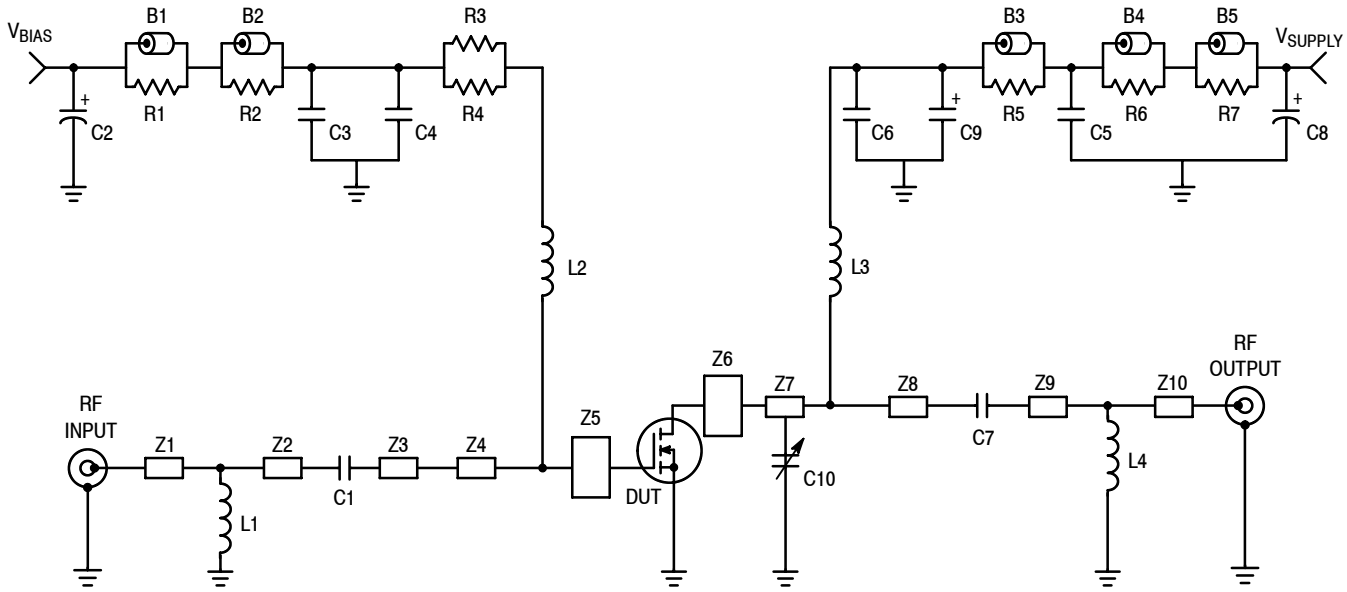
Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 300 mA)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
Dynamic Characteristics					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.3	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	G_{ps}	—	13	—	dB
Two-Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	η	—	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IMD	—	-31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IRL	—	-13	—	dB
Two-Tone Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	12	13	—	dB
Two-Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	-31	-28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	-13	-9	dB

1. Part is internally matched both on input and output.

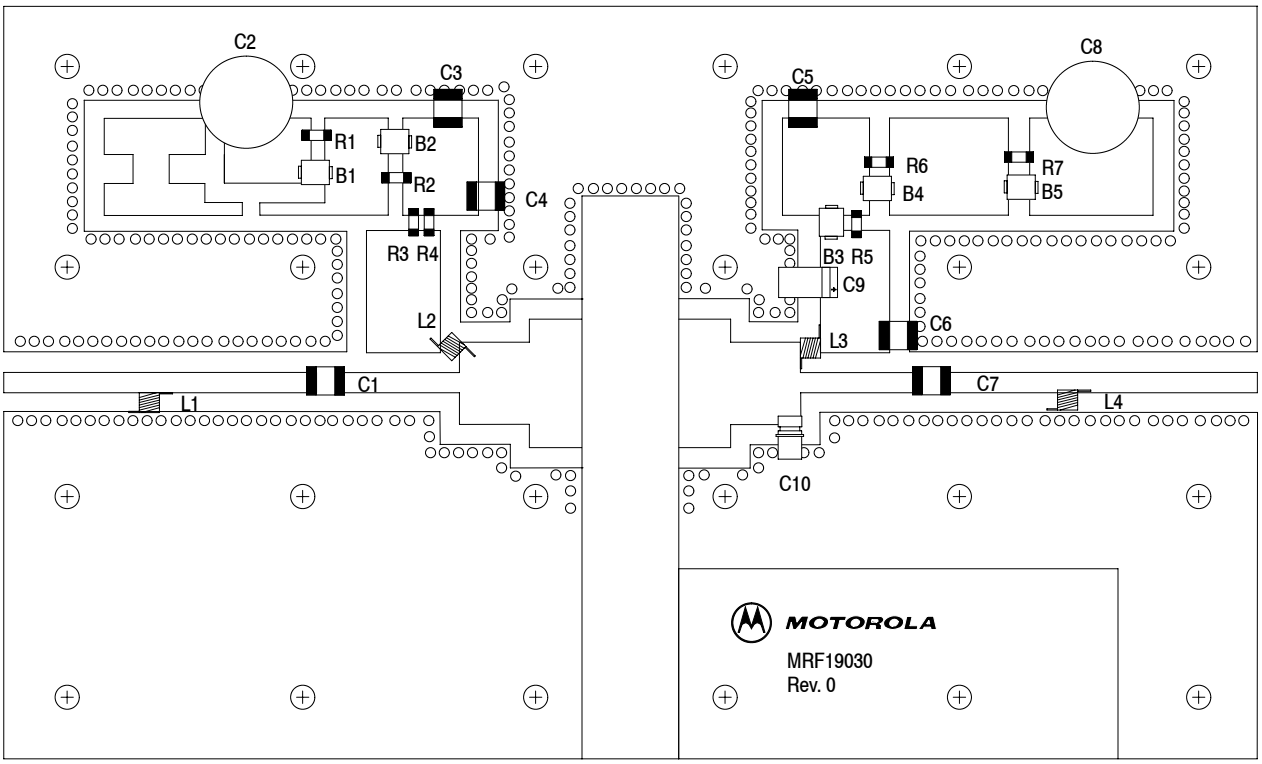
ARCHIVE INFORMATION



B1 – B5	Short Ferrite Beads	Z3	0.080″ x 0.480″ Microstrip
C1, C7	10 pF Chip Capacitors	Z4	0.325″ x 0.280″ Microstrip
C2, C8	470 μF, 35 V Electrolytic Capacitors	Z5	0.510″ x 0.200″ Microstrip
C3, C5	0.1 μF Chip Capacitors	Z6	0.510″ x 0.200″ Microstrip
C4, C6	5.1 pF Chip Capacitors	Z7	0.325″ x 0.280″ Microstrip
C9	22 μF Tantalum Chip Capacitor	Z8	0.080″ x 0.480″ Microstrip
C10	0.4 – 2.5 pF Variable Capacitor	Z9	0.080″ x 0.530″ Microstrip
L1 – L4	12.5 nH Inductors	Z10	0.080″ x 0.671″ Microstrip
R1 – R7	12 Ω Chip Resistors (0805)	Substrate	0.030″ x 3.00″ x 5.00″ Glass Teflon®, Arlon
Z1	0.080″ x 0.595″ Microstrip		
Z2	0.080″ x 0.600″ Microstrip		

Figure 1. MRF19030LR3 Test Circuit Schematic

ARCHIVE INFORMATION



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/-logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF19030LR3 Test Circuit Component Layout

ARCHIVE INFORMATION

TYPICAL CHARACTERISTICS

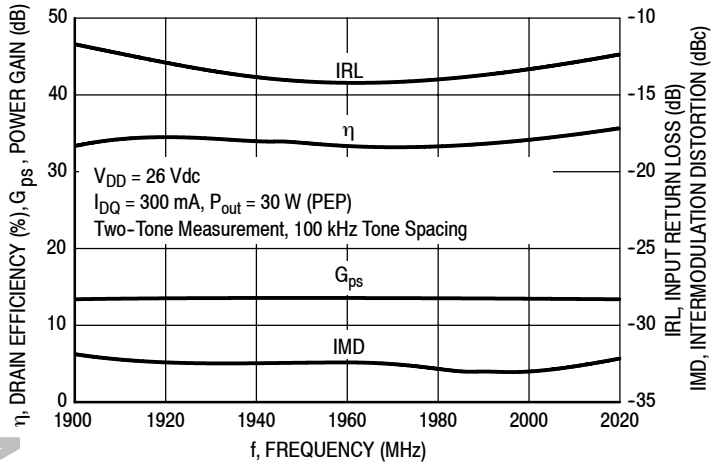


Figure 3. Class AB Broadband Circuit Performance

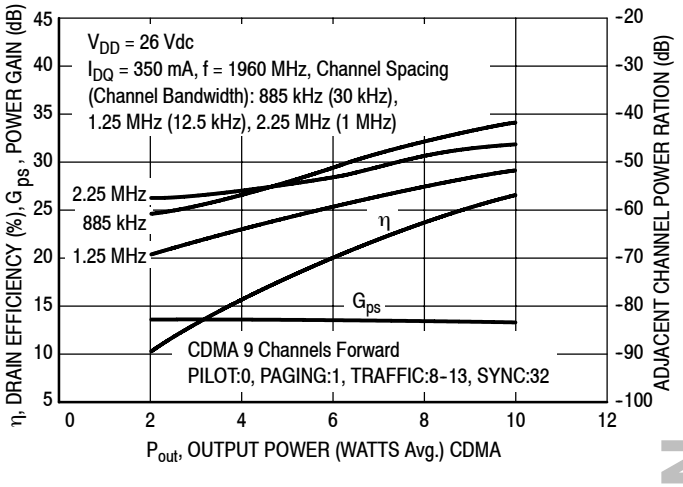


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

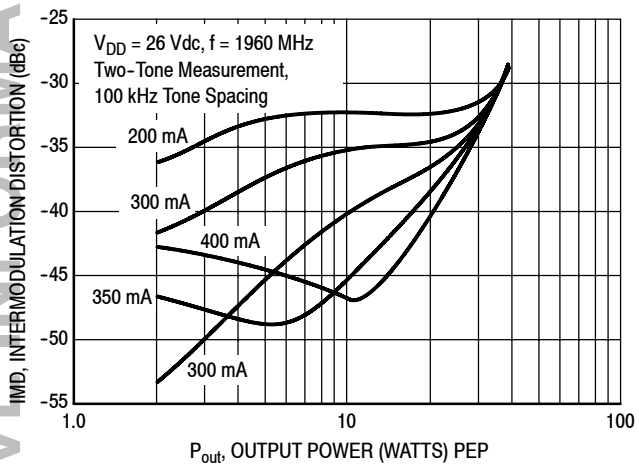


Figure 5. Intermodulation Distortion versus Output Power

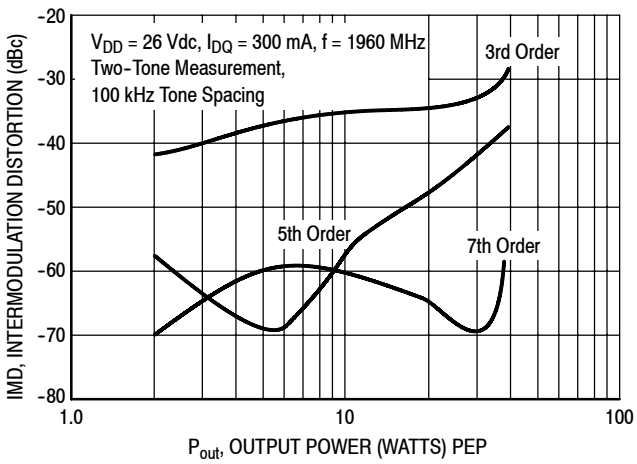


Figure 6. Intermodulation Distortion Products versus Output Power

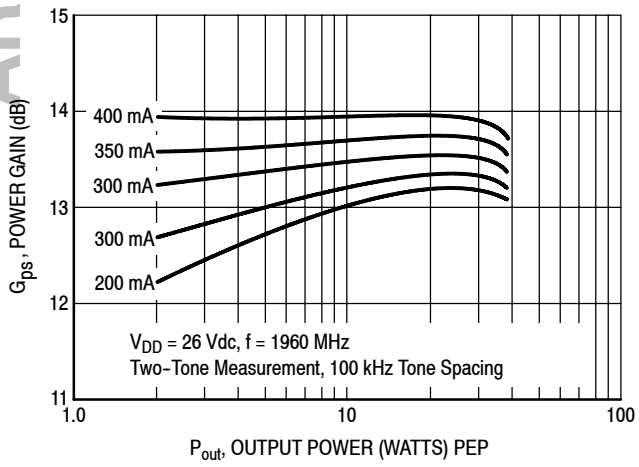


Figure 7. Power Gain versus Output Power

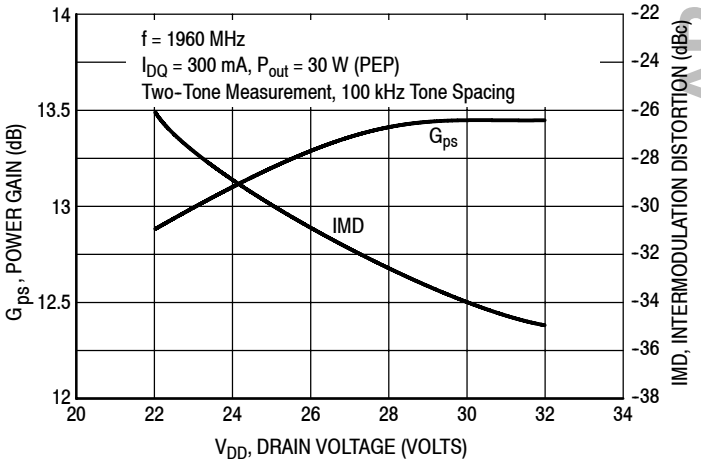


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

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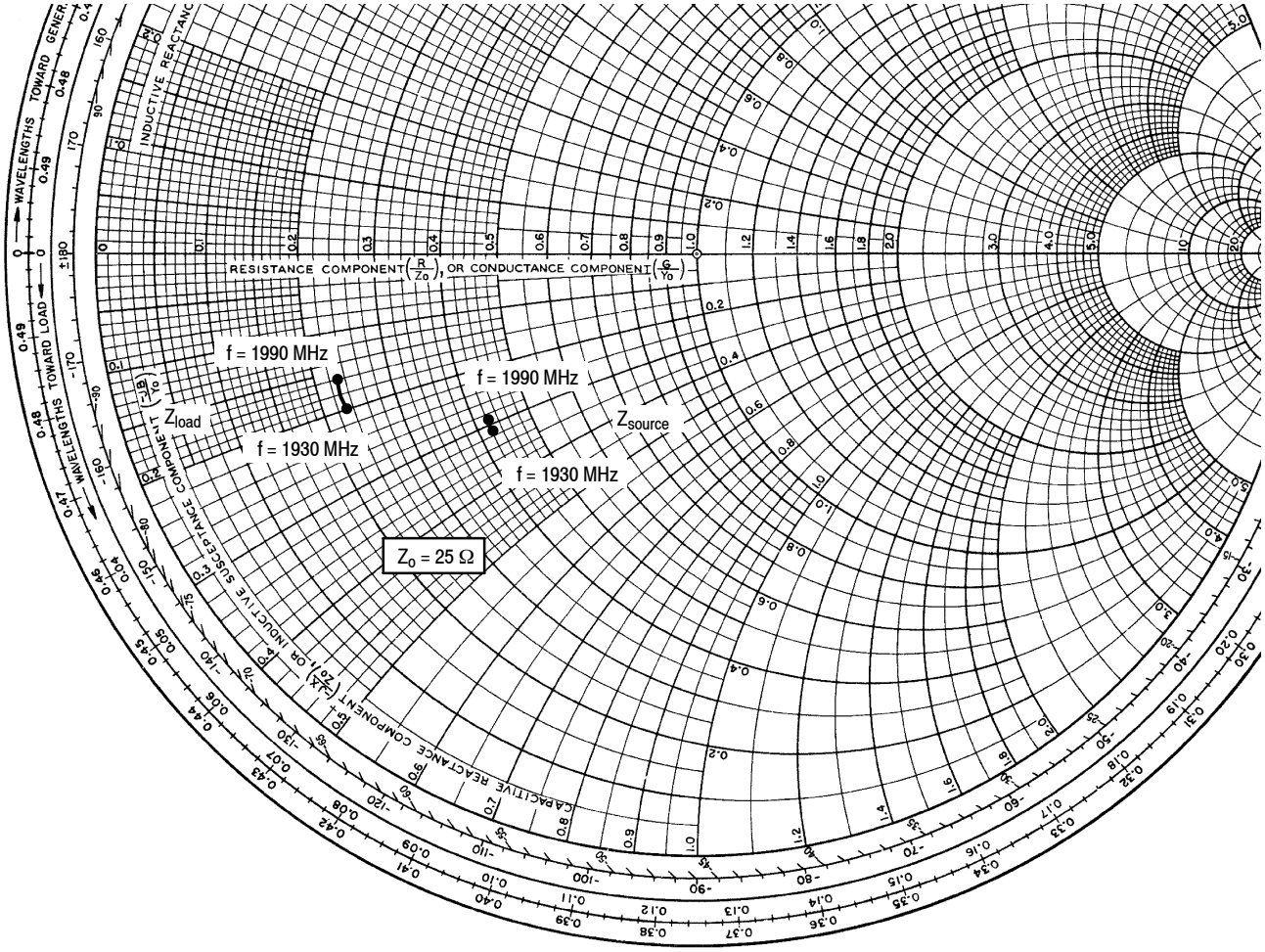


V_{DD} = 26 V, I_{DQ} = 300 mA, P_{out} = 30 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
1930	10.57 – j7.69	5.81 – j5.01
1960	10.54 – j7.43	5.84 – j4.67
1990	10.47 – j7.21	5.84 – j4.35

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

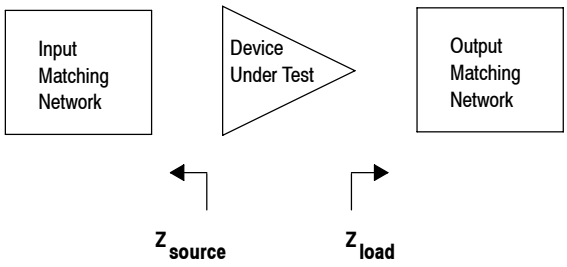
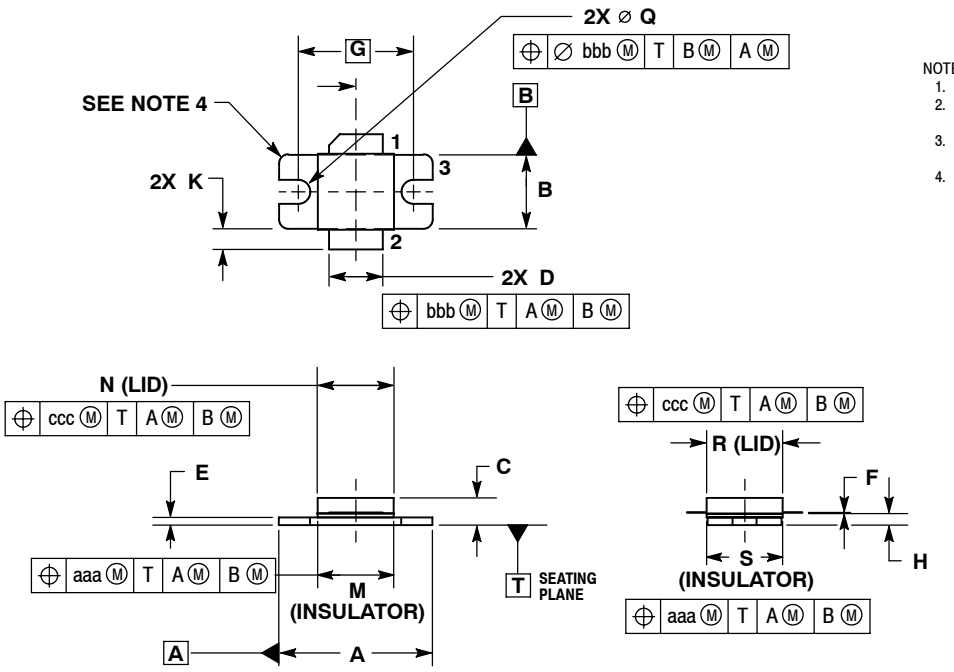


Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. INFORMATION ONLY: CORNER BREAK (4X) TO BE .060±.005 (1.52±0.13) RADIUS OR .06±.005 (1.52±0.13) x 45° CHAMFER.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	⌀ .120	⌀ .130	⌀ 3.05	⌀ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E-04
ISSUE F
NI-400
MRF19030LR3

ARCHIVE INFORMATION

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
14	Oct. 2008	• Data sheet revised to reflect part status change, p. 1, 3–4, including use of applicable overlay. • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2 • Added Product Documentation and Revision History, p. 8 • Data sheet split due to change in part life cycle (–1, –2 added to enable visibility on web).
	Dec. 2010	• MRF19030–2 Rev. 14 (MRF19030LR3) data sheet archived. Part no longer manufactured. See MRF19030–1 Rev. 13 for MRF19030LSR3.

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Freescale Semiconductor, Inc.
Technical Information Center, EL516
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Tempe, Arizona 85284
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Europe, Middle East, and Africa:
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+46 8 52200080 (English)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
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China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
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Document Number: MRF19030-2
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