

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1900 to 2000 MHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

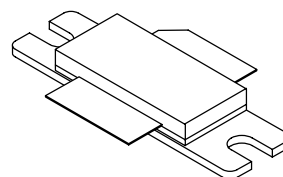
- Typical CDMA Performance: 1960 MHz, 26 Volts
 IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
 Output Power — 7.5 Watts
 Power Gain — 12.5 dB
 Adjacent Channel Power —
 885 kHz: -47 dBc @ 30 kHz BW
 1.25 MHz: -55 dBc @ 12.5 kHz BW
 2.25 MHz: -55 dBc @ 1 MHz BW
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1960 MHz, 60 Watts CW Output Power

Features

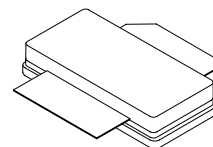
- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF19060LR3
MRF19060LSR3

1930-1990 MHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF19060LR3



CASE 465A-06, STYLE 1
NI-780S
MRF19060LSR3

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

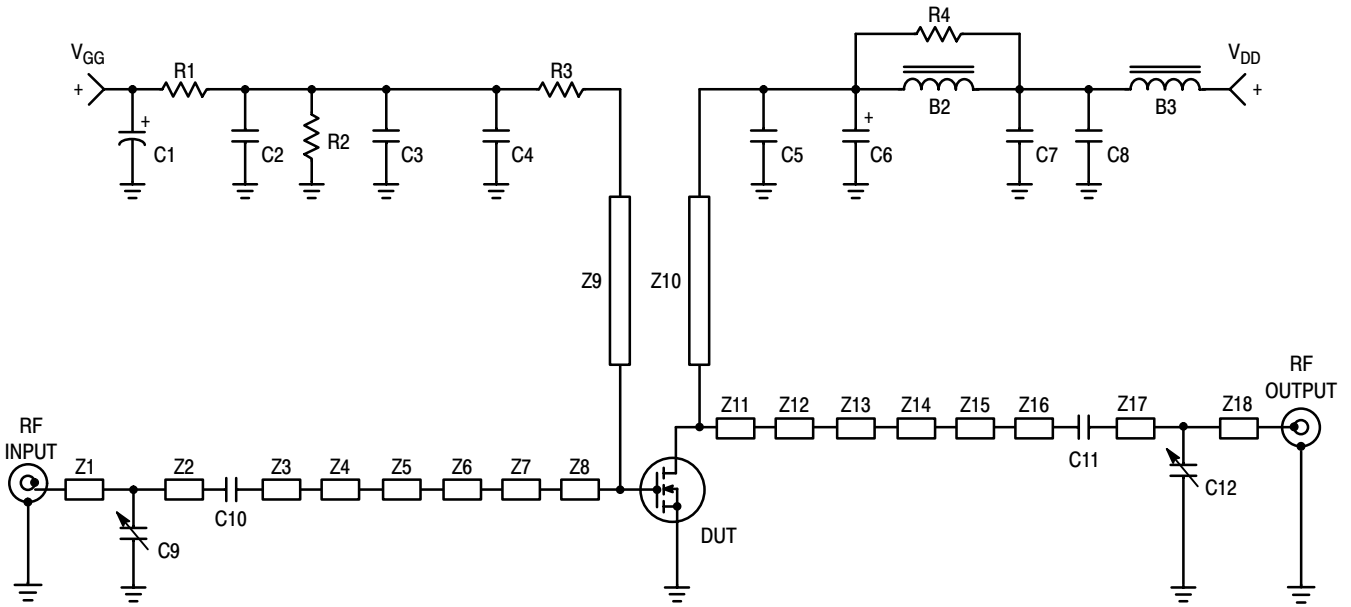
Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

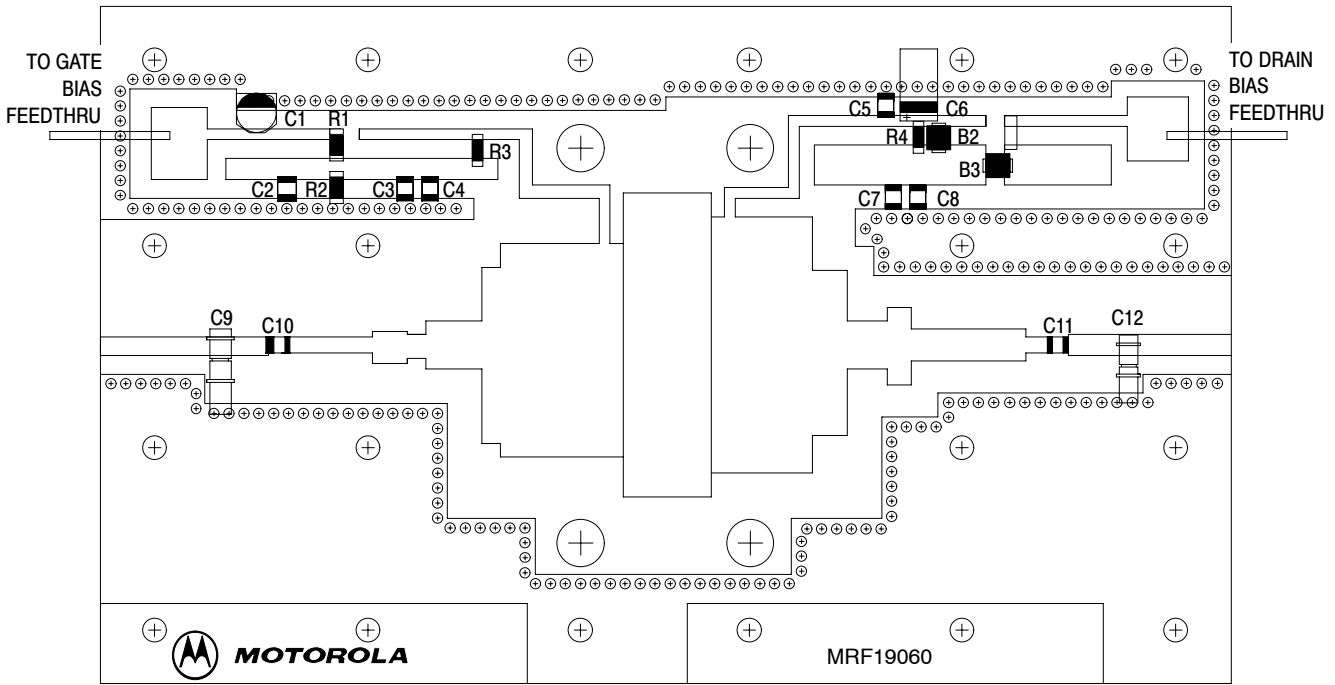
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\ \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	6	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$)	$V_{GS(th)}$	2	—	4	V
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 500\text{ mAdc}$)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	$V_{DS(on)}$	—	0.27	—	V
Dynamic Characteristics					
Reverse Transfer Capacitance (1) ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	2.7	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IRL	—	-12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W CW}$, $f = 1990\text{ MHz}$)	P1dB	—	60	—	W

1. Part is internally matched both on input and output.



B2 - B3	Ferrite Beads, Fair Rite, 2743019447	Z4	0.152" x 0.140" Microstrip
C1	10 μ F, 50 V Electrolytic Capacitor, Panasonic #ECEV1HV100R	Z5	0.090" x 0.102" Microstrip
C2, C7	1000 pF Chip Capacitors, ATC #100B102JCA500X	Z6	0.245" x 0.217" Microstrip
C3, C8	0.10 μ F Chip Capacitors, Kemet #CDR33BX104AKWS	Z7	0.090" x 0.737" Microstrip
C4	5.1 pF Chip Capacitor, ATC #100B5R1JCA500X	Z8	0.530" x 0.941" Microstrip
C5	6.2 pF Chip Capacitor, ATC #100B6R2JCA500X	Z9	1.010" x 0.050" Microstrip
C6	22 μ F, 35 V Tantalum Capacitor, SMT, Sprague	Z10	1.060" x 0.050" Microstrip
C9	0.8 pF - 8.0 pF Variable Capacitor, Johanson Gigatrim	Z11	0.446" x 1.137" Microstrip
C10, C11	10 pF Chip Capacitors, ATC #100B100JCA500X	Z12	0.152" x 0.567" Microstrip
C12	0.4 pF - 2.5 pF Variable Capacitor, Johanson Gigatrim	Z13	0.183" x 0.220" Microstrip
R1	1 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z14	0.100" x 0.338" Microstrip
R2	560 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z15	0.480" x 0.142" Microstrip
R3	15 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z16	0.140" x 0.080" Microstrip
R4	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z17	0.173" x 0.080" Microstrip
Z1	0.580" x 0.074" Microstrip	Z18	0.420" x 0.080" Microstrip
Z2	0.100" x 0.074" Microstrip	Board	0.030" Glass Teflon [®] Arlon GX-0300-55-22, 2 oz Cu
Z3	0.384" x 0.074" Microstrip		

Figure 1. MRF19060L Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF19060L Test Circuit Component Layout

TYPICAL CHARACTERISTICS

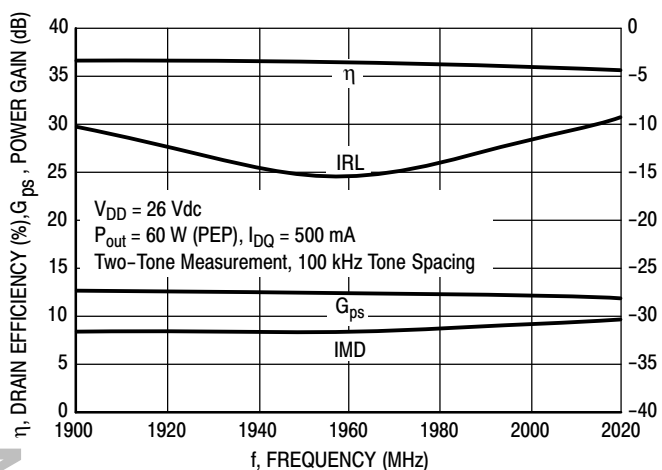


Figure 3. Class AB Broadband Circuit Performance

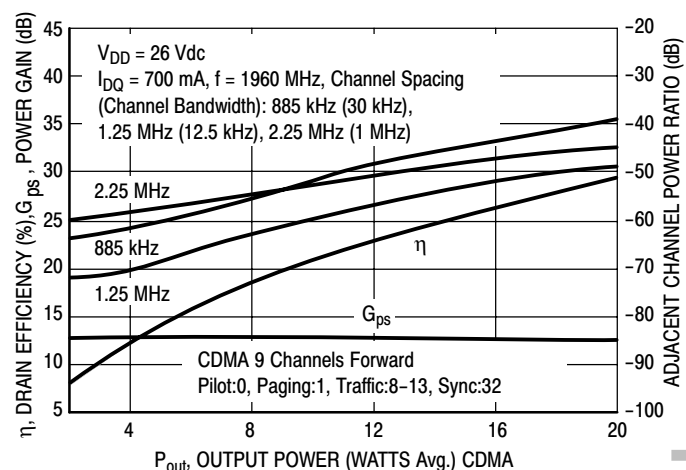


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

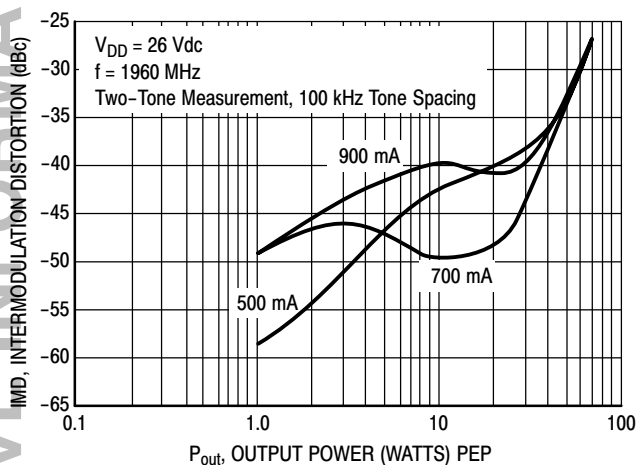


Figure 5. Intermodulation Distortion versus Output Power

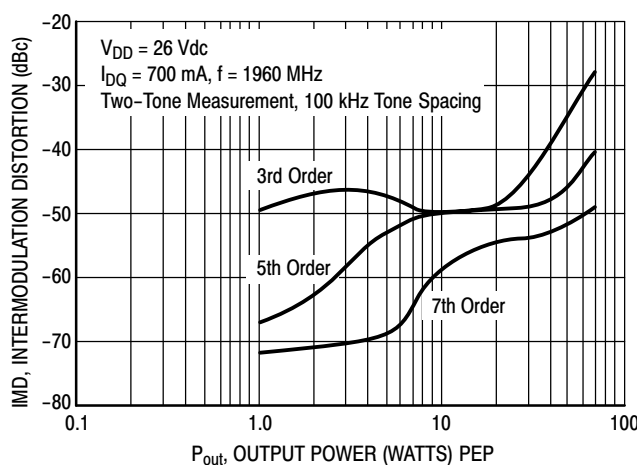


Figure 6. Intermodulation Products versus Output Power

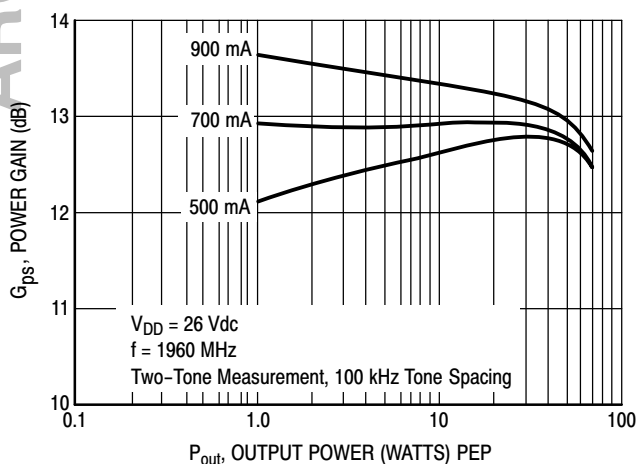


Figure 7. Power Gain versus Output Power

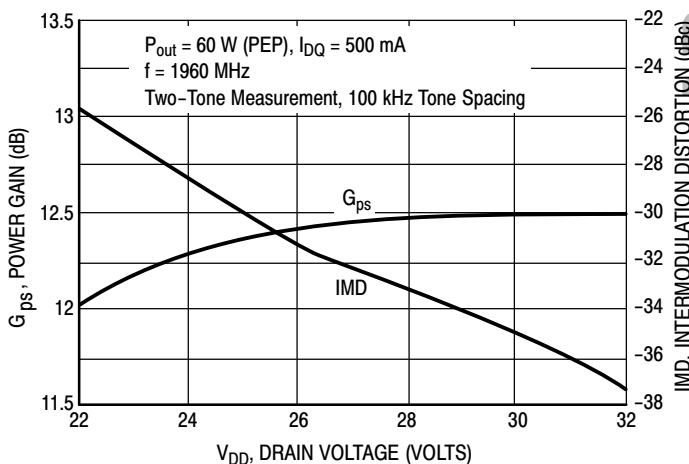
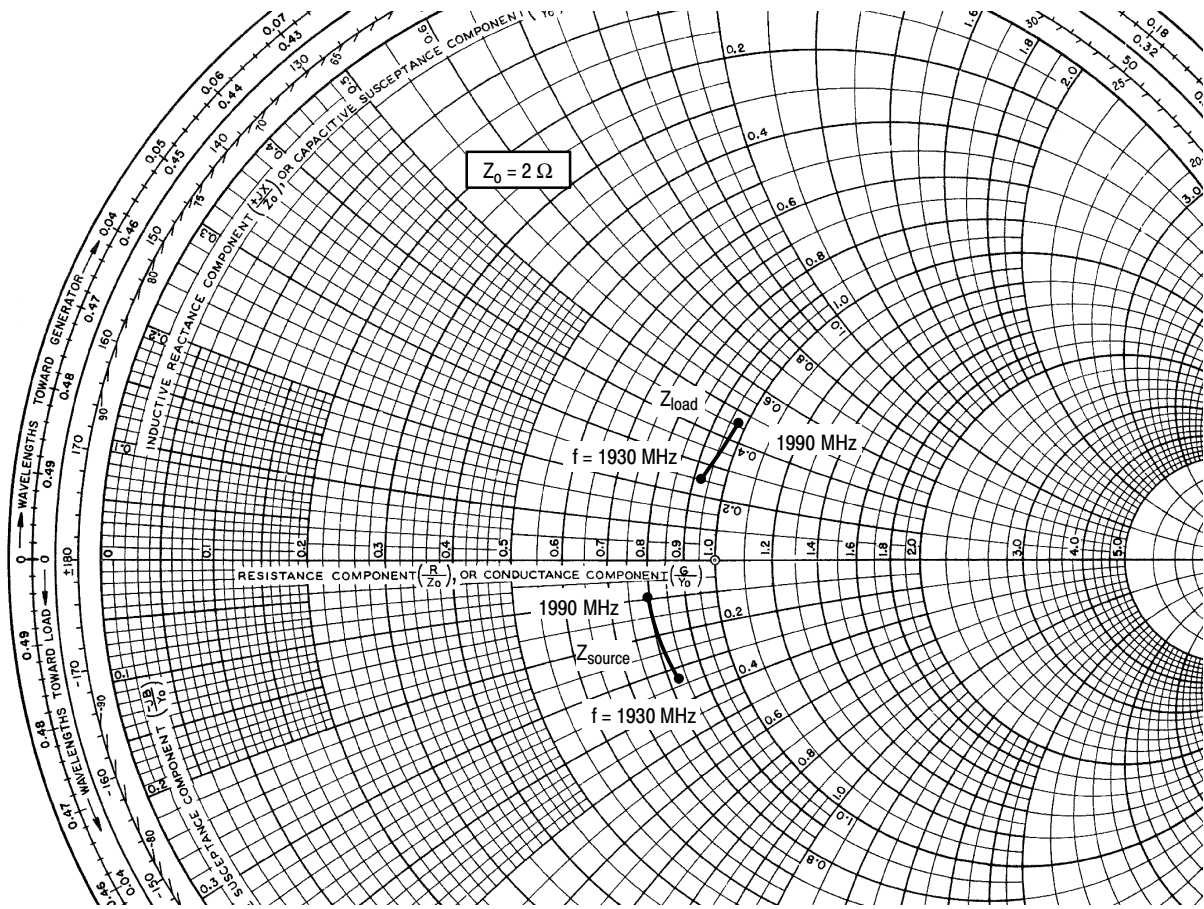


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

ARCHIVE INFORMATION

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$V_{DD} = 26\text{ V}$, $I_{DQ} = 500\text{ mA}$, $P_{out} = 60\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$1.65 - j0.67$	$1.85 + j0.50$
1960	$1.64 - j0.45$	$1.89 + j0.74$
1990	$1.60 - j0.20$	$1.96 + j0.94$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

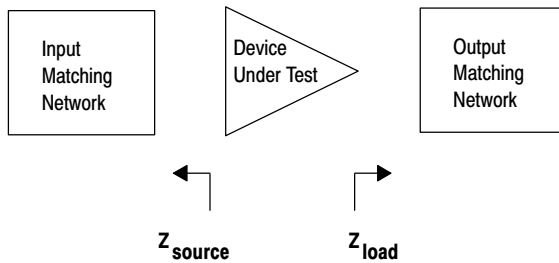
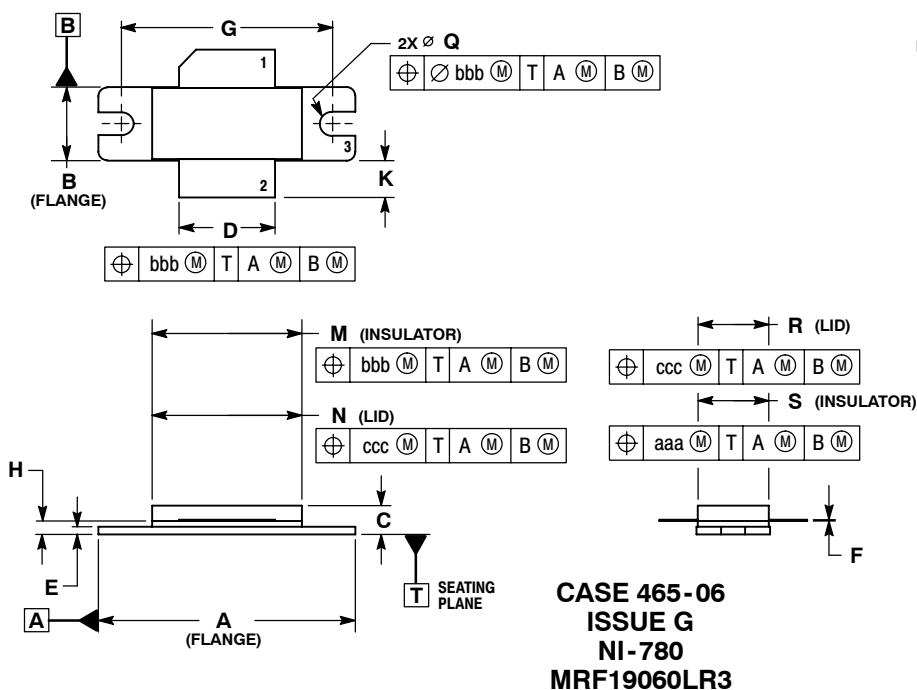


Figure 9. Series Equivalent Source and Load Impedance

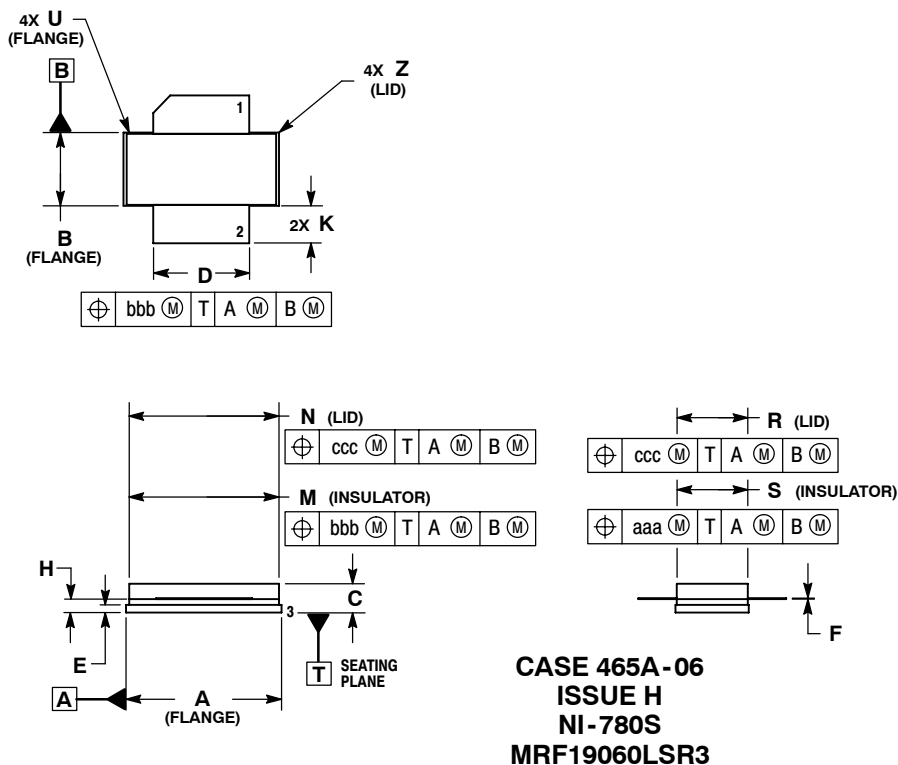
PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

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