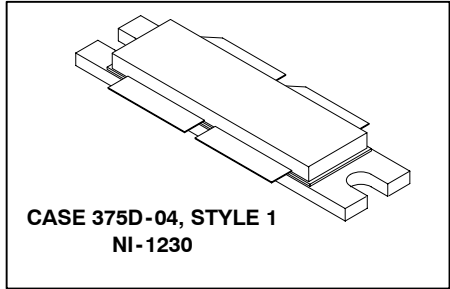


The RF MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

MRF19120

**1990 MHz, 120 W, 26 V
 LATERAL N-CHANNEL
 RF POWER MOSFET**



Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- CDMA Performance @ 1990 MHz, 26 Volts
 - IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
 - 885 kHz — -47 dBc @ 30 kHz BW
 - 1.25 MHz — -55 dBc @ 12.5 kHz BW
 - 2.25 MHz — -55 dBc @ 1 MHz BW
 - Output Power — 15 Watts (Avg.)
 - Power Gain — 11.7 dB
 - Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency, High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1990 MHz, 120 Watts (CW) Output Power
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	389 2.22	Watts W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.8	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V _{DS} = 26 V, I _D = 500 mA)	V _{GS(Q)}	3	3.9	5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 V, I _D = 2 A)	V _{DS(on)}	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	G _{ps}	10.7	11.7	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	η	30	34	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	IMD	—	-31	-28	dB
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	IRL	—	-12	-9	dB
Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	G _{ps}	—	11.7	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	η	—	34	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	IMD	—	-31	—	dB
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	IRL	—	-14	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 26 Vdc, CW, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz)	P _{1dB}	—	120	—	Watts
Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W CW, I _{DQ} = 2 × 500 mA, f ₁ = 1990.0 MHz)	G _{ps}	—	11	—	dB

(1) Each side of device measured separately.

(2) Device measured in push-pull configuration.

(continued)

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ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 120 \text{ W CW}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $f_1 = 1990.0 \text{ MHz}$)	η	—	45	—	%
Output Mismatch Stress ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 120 \text{ W CW}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $f = 1990 \text{ MHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

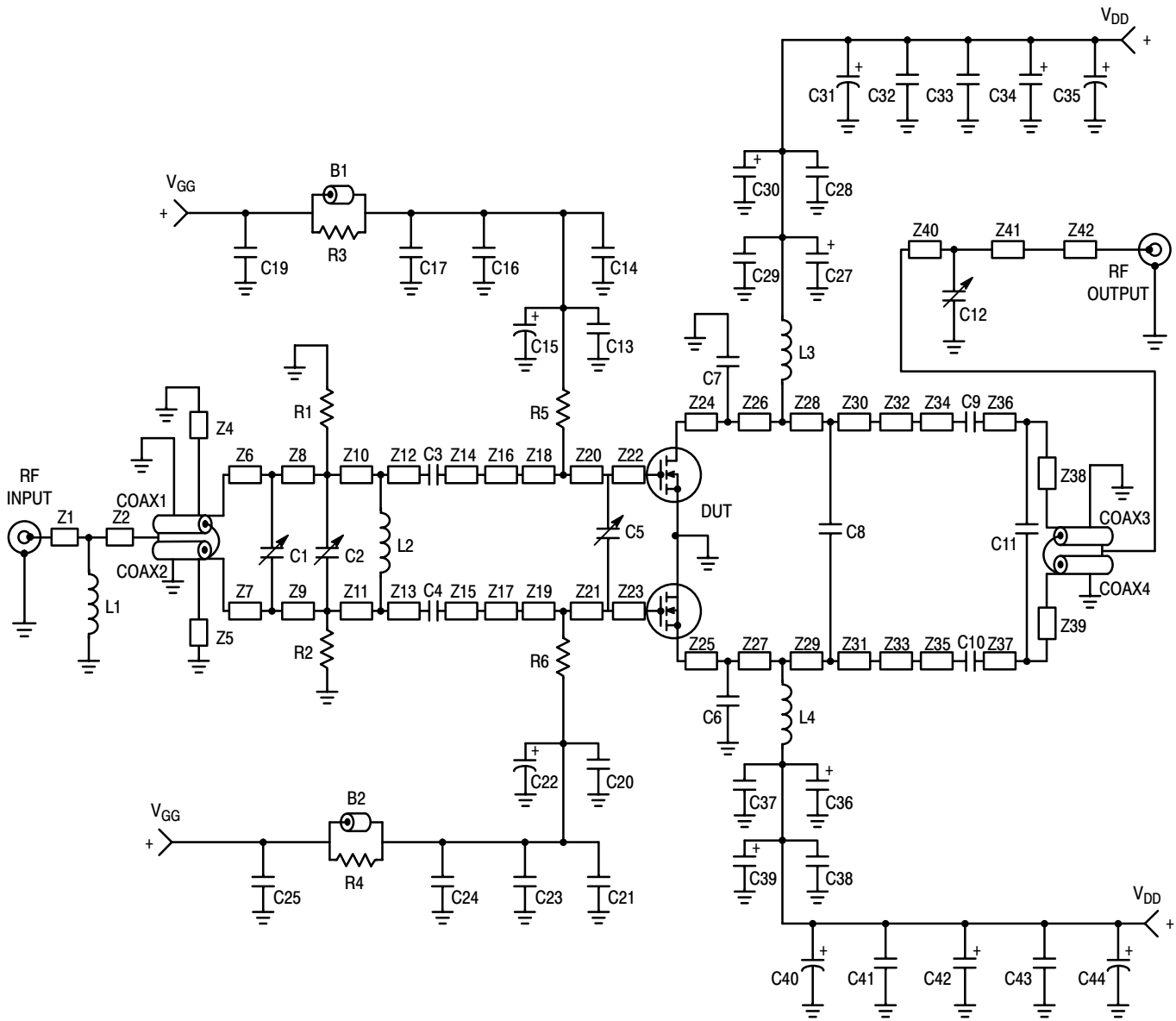
(2) Device measured in push-pull configuration.

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- B1, B2 Ferrite Beads, Fair Rite
- C1, C2 0.6 - 4.5 pF Variable Capacitors, Johanson Gigatrim
- C3, C4, C9, C10 10 pF Chip Capacitors, B Case, ATC
- C5, C12 0.4 - 2.5 pF Variable Capacitors, Johanson Gigatrim
- C6, C7 2.0 pF Chip Capacitors, B Case, ATC
- C8 1.1 pF Chip Capacitor, B Case, ATC
- C11 0.1 pF Chip Capacitor, B Case, ATC
- C13, C20, C29, C37 5.1 pF Chip Capacitors, B Case, ATC
- C14, C21, C28, C38 91 pF Chip Capacitors, B Case, ATC
- C15, C22, C31, C40 100 μF, 50 V Electrolytic Capacitors, Sprague
- C16, C23, C33, C43 0.039 μF Chip Capacitors, B Case, ATC
- C17, C24, C32, C41 1000 pF Chip Capacitors, B Case, ATC
- C19, C25 0.020 μF Chip Capacitors, B Case, ATC
- C27, C34, C36, C42 22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
- C30, C39 1.0 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
- C35, C44 470 μF, 63 V Electrolytic Capacitors, Sprague
- Coax1, Coax2 25 Ω, Semi Rigid Coax, 70 mil OD, 1.05" Long
- Coax3, Coax4 50 Ω, Semi Rigid Coax, 85 mil OD, 1.05" Long
- L1 5.0 nH, Minispring Inductor, Coilcraft
- L2 8.0 nH, Minispring Inductor, Coilcraft
- L3, L4 5.60 nH, Microspring Inductors, Coilcraft
- R1, R2 1 kΩ, 1/2 W Fixed Metal Film Resistors, Dale
- R3, R4 270 Ω, 1/8 W Fixed Film Chip Resistors, Dale
- R5, R6 1.0 kΩ, 1/8 W Fixed Film Chip Resistors, Dale
- Z1 0.150" x 0.080" Microstrip

- Z2 0.320" x 0.080" Microstrip
- Z4, Z5 1.050" x 0.080" Microstrip
- Z6, Z7 0.120" x 0.080" Microstrip
- Z8, Z9 0.140" x 0.080" Microstrip
- Z10, Z11 0.610" x 0.080" Microstrip
- Z12, Z13 0.135" x 0.080" Microstrip
- Z14, Z15 0.130" x 0.080" Microstrip
- Z16, Z17 0.300" x 0.350" Microstrip
- Z18, Z19 0.150" x 0.500" Microstrip
- Z20, Z21 0.075" x 0.500" Microstrip
- Z22, Z23 0.330" x 0.500" Microstrip
- Z24, Z25 0.100" x 0.550" Microstrip
- Z26, Z27 0.175" x 0.550" Microstrip
- Z28, Z29 0.045" x 0.550" Microstrip
- Z30, Z31 0.190" x 0.325" Microstrip
- Z32, Z33 0.080" x 0.325" Microstrip
- Z34, Z35 0.515" x 0.080" Microstrip
- Z36, Z37 0.020" x 0.080" Microstrip
- Z38, Z39 0.565" x 0.080" Microstrip
- Z40 0.100" x 0.080" Microstrip
- Z41 0.470" x 0.080" Microstrip
- Z42 0.100" x 0.080" Microstrip
- Board Material 0.03" Teflon®, ε_r = 2.55 Copper Clad, 2 oz. Cu
- Connectors N-Type Panel Mount, Stripline

Figure 1. 1.93 - 1.99 GHz Broadband Test Circuit Schematic

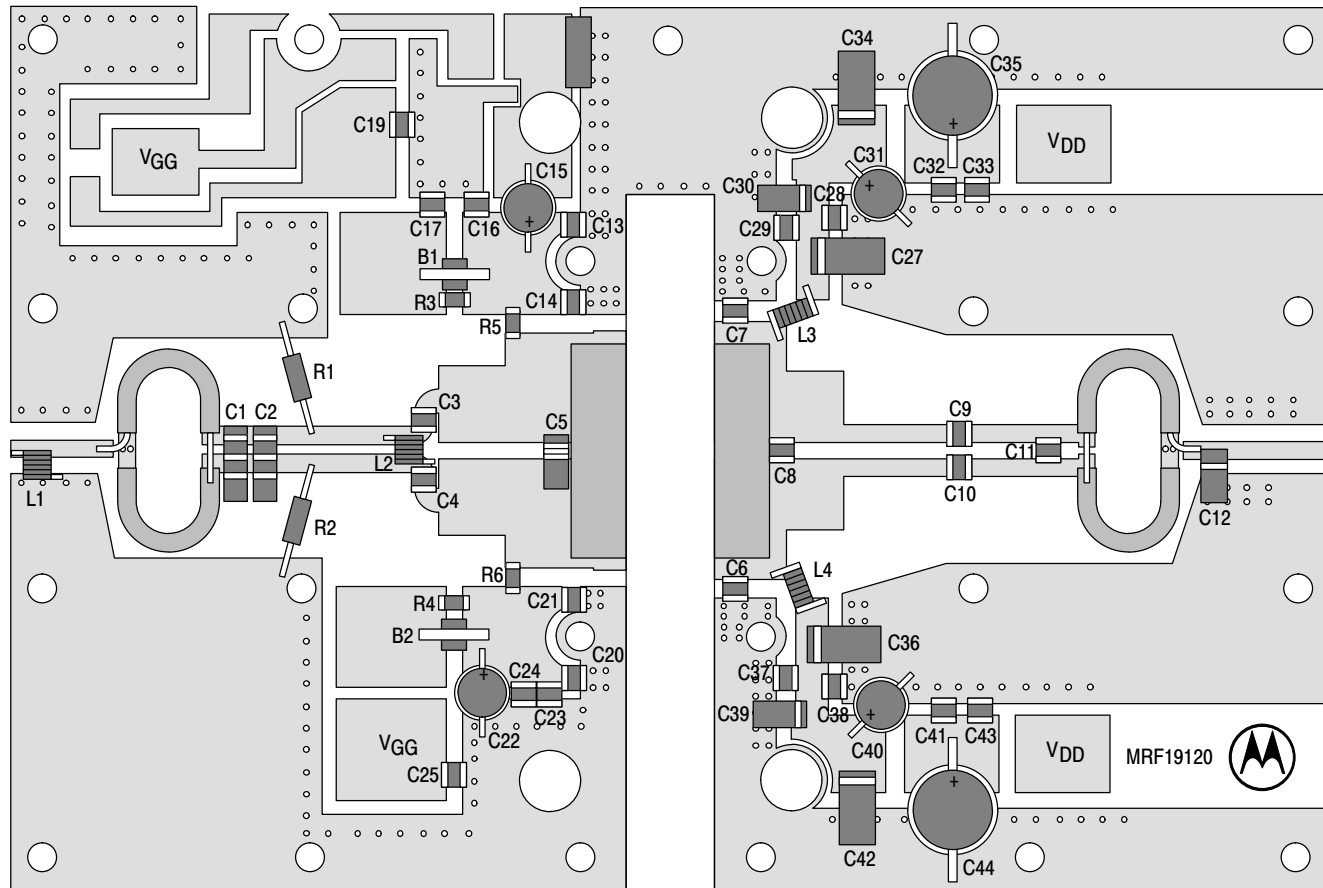


Figure 2. MRF19120 Test Circuit Component Layout

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TYPICAL CHARACTERISTICS

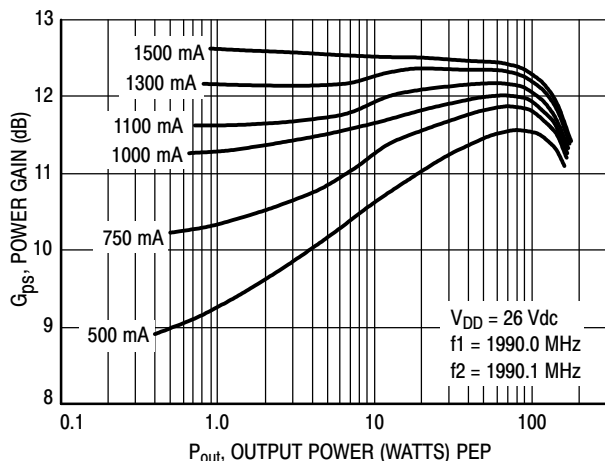


Figure 3. Power Gain versus Output Power

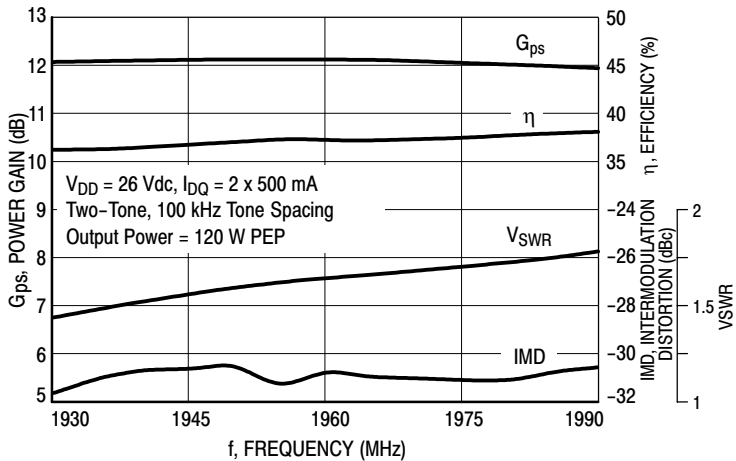


Figure 4. Class AB Broadband Circuit Performance

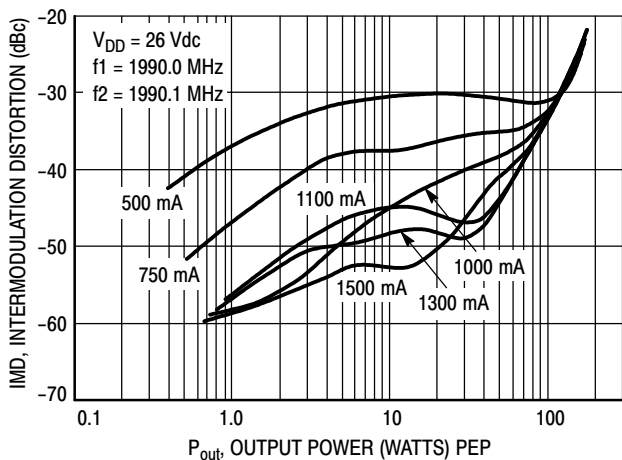


Figure 5. Intermodulation Distortion versus Output Power

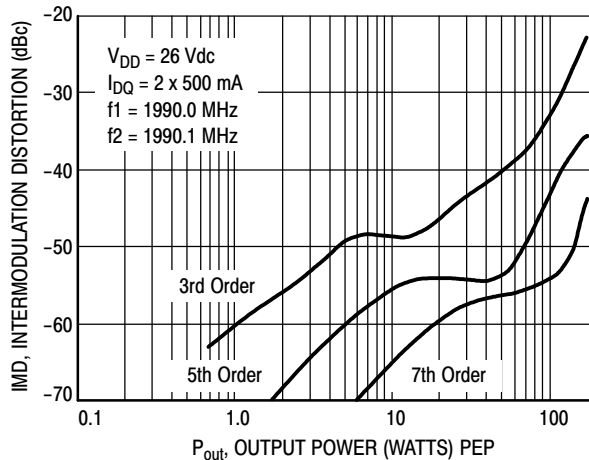


Figure 6. Intermodulation Distortion Products versus Output Power

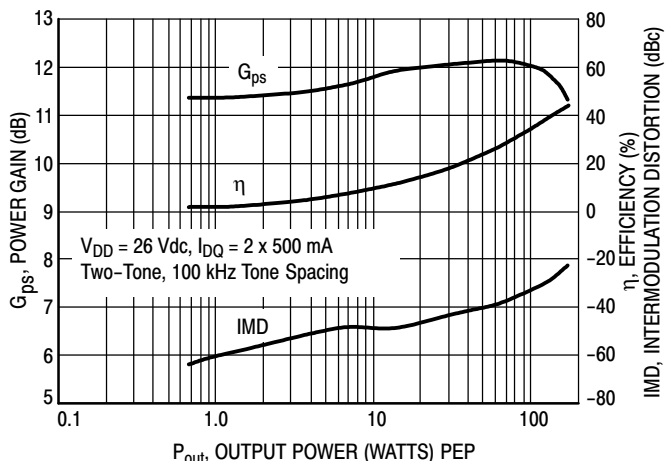


Figure 7. Power Gain, Efficiency, and IMD versus Output Power

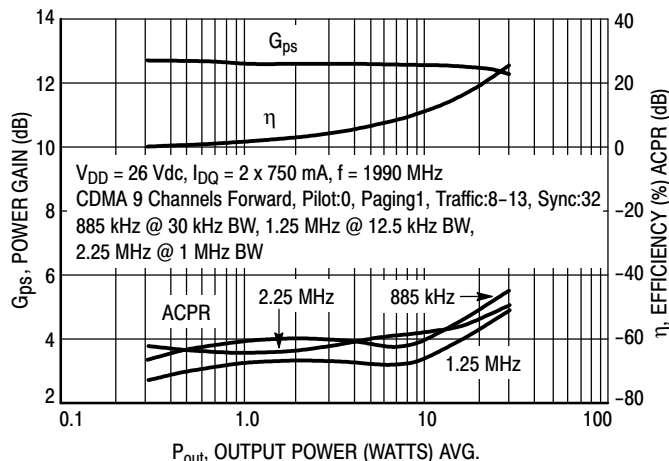
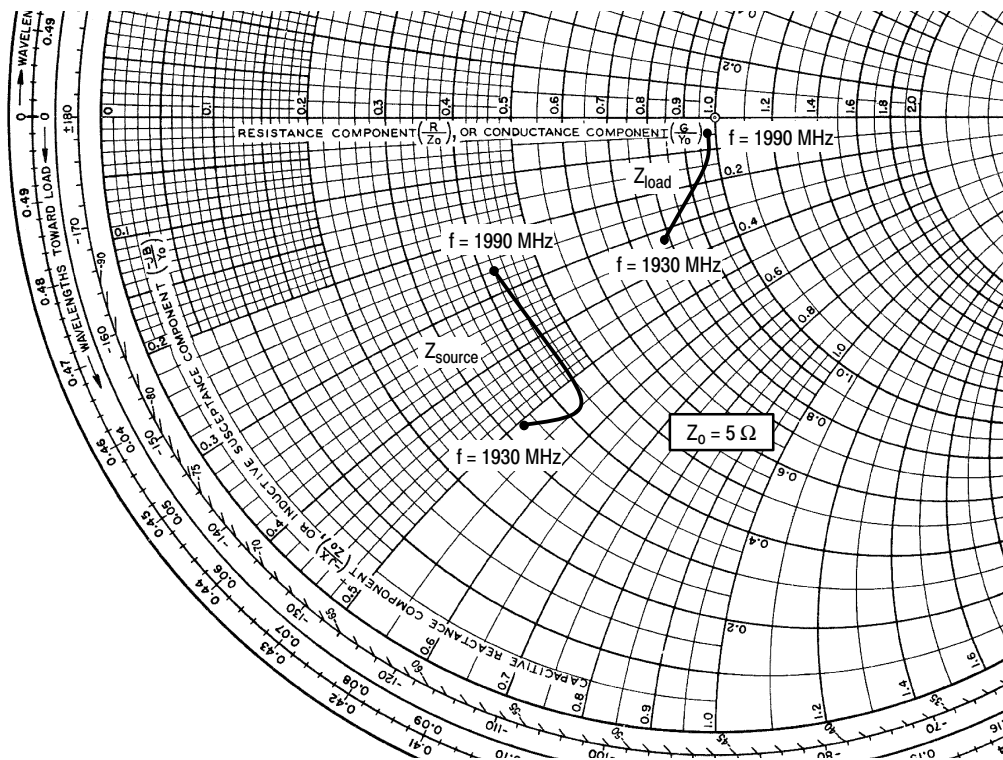


Figure 8. Power Gain, Efficiency, and ACPR versus Output Power

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$V_{DD} = 26 \text{ V}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $P_{out} = 120 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$1.64 - j2.6$	$3.9 - j1.7$
1960	$2.10 - j2.8$	$4.8 - j0.8$
1990	$2.10 - j1.4$	$4.9 - j0.3$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

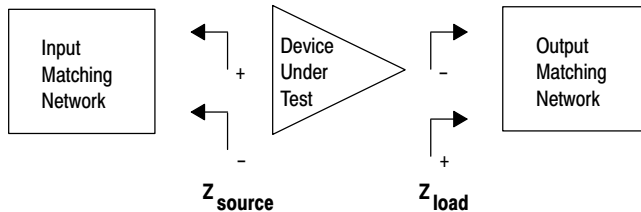
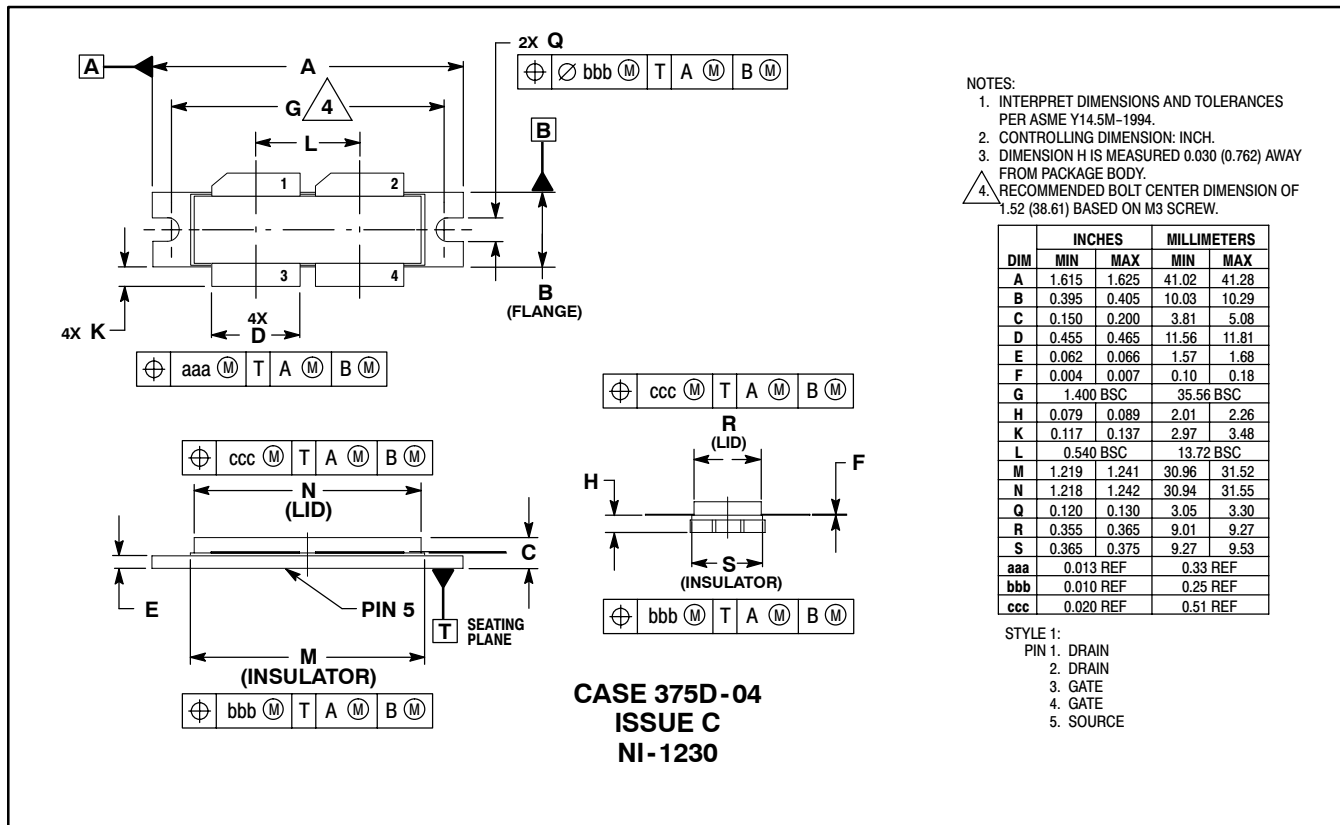


Figure 9. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS



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