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MOTOROLA

MRFIC1854A

Advance Information

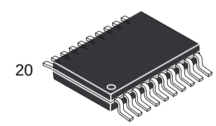
1.9 GHz CDMA Upmixer/Exciter

The MRFIC1854A is an integrated upmixer and exciter amplifier designed specifically for PCS CDMA digital cellular radios. The exciter amplifier incorporates a temperature compensated linear gain control and selectable bias to reduce power consumption. The design utilizes Motorola's RF BiCMOS1 process to yield superior performance in a cost effective monolithic device.

- Total Supply Current CDMA Mode = 55 mA Typical
- 65 dB Dynamic Range Gain Control
- Upmixer Output IP3 = 6.0 dBm Typical
- Exciter Output IP3 = 22 dBm Typical
- Supply Voltage Range = 2.7 to 3.6 V
- Adjacent Channel Power (ACPR) @ 1.25 MHz Offset (P_{out} = 3.0 dBm) = –58 dBc Typical

1.9 GHz CDMA UPMIXER/EXCITER

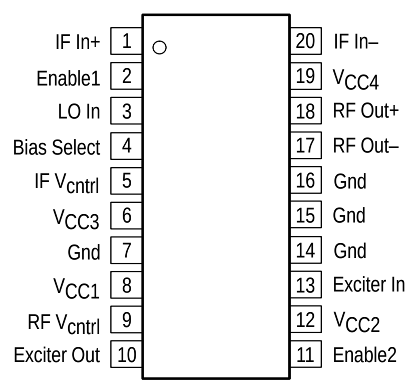
SEMICONDUCTOR TECHNICAL DATA



(Scale 2:1)

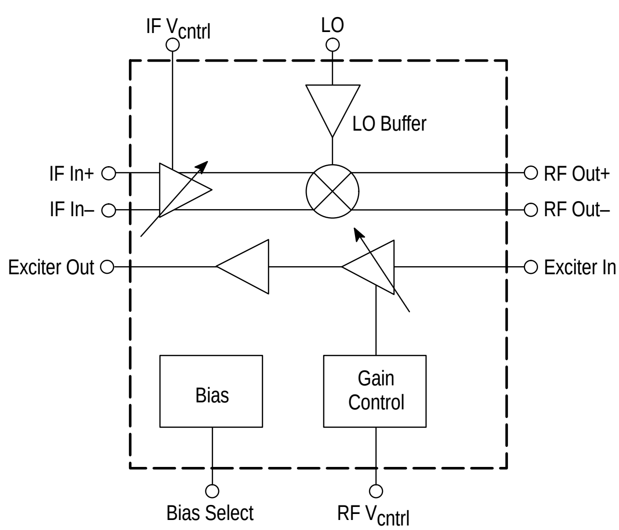
PLASTIC PACKAGE
CASE 948M
(TSSOP–20EP, Tape & Reel Only)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



This device contains 305 active transistors.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1854AR2	T_A = –40 to 85°C	TSSOP–20EP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Rev 0

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0	V
IF Input	IF In+, IF In–	10	dBm
LO Input	LO	10	dBm
Operating Temperature	T_A	–40 to 85	°C
Storage Temperature	T_{stg}	–65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables or Pin Descriptions section.
2. Meets Human Body Model (HBM) ≤50 V and Machine Model (MM) ≤40 V. This device is rated Moisture Sensitivity Level (MSL) 4. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	–	3.6	V
RF Frequency Range	f_{RF}	1700	–	2000	MHz
IF Frequency Range	f_{IF}	70	–	250	MHz
LO Frequency Range	f_{LO}	1500	–	2100	MHz
Gain Control Voltage Range	IF V_{cntrl}, RF V_{cntrl}	0.1	–	1.7	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, P_{LO} = –13 dBm @ 2010 MHz, P_{IF} = –27 dBm (differential) @ 130 MHz, $V_{Enable1}$ = $V_{Enable2}$ = 2.4 V, T_A = –40 to 85°C, Test Circuit in Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CASCADE PERFORMANCE (Filter included between RF Out and Exciter input. Filter insertion loss is 4.0 dB)					
Output Power V_{ctrl} = 1.7 V V_{ctrl} = 1.3 V	P_{out}	 3.0 2.0	 5.0 3.8	 – –	dBm
Dynamic Range (V_{ctrl} = 0.1 to 1.7 V)	DR	50	65	–	dB
Adjacent Channel Power @ 1.25 MHz Offset High Current (Bias Select = 0.4 V, P_{out} = 3.0 dBm (set by V_{ctrl}))	ACPR	 –52	 –58	 –	dBc
Supply Current High Current (Bias Select = 0.4 V) Low Current (Bias Select = 2.4 V)	I_{CC}	 – –	 55 35	 80 50	mA
MIXER SECTION					
Conversion Gain	G_C	–	16	–	dB
Noise Figure	NF	–	12	–	dB
Output Third Order Intercept Point	OIP3	–	6.0	–	dBm
IF AGC Dynamic Range	DR_{IF}	25	38	–	dB
EXCITER SECTION					
Gain (No Attenuation)	G	–	24	–	dB
Noise Figure	NF	–	5.0	–	dB
Output Third Order Intercept Point	OIP3	–	22	–	dBm
RF AGC Dynamic Range	DR_{RF}	25	38	–	dB

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PIN FUNCTION DESCRIPTION

Pin	Function	Description	Voltage On (V)	Voltage Off (V)
1	IF In+	Mixer IF input pin. Input impedance is 500 Ω.	–33 dBm (Typ)	
2	Enable 1 (See Table 1)	Enable pin. A logic ″High″ (>2.4 V) enables entire chip and ″Low″ (<0.4 V) **disables chip.**	2.4 to 3.6	0 to 0.4
3	LO In	Mixer LO input pin.	–13 dBm (Typ)	
4	Bias Select	Bias select pin. Logic ″Low″ (<0.4 V) selects higher current bias for increased linearity and output power. ″High″ (>2.4 V) selects lower bias for reduced current consumption.		
5	IF AGC Control Voltage	IF AGC gain control pin. A 30 dB dynamic range can be acheived by adjusting voltage from 0.1 V (low gain) to 1.7 V (high gain).	0.1 to 1.7	
6	V_{CC3}	Supply Voltage.	2.7 to 3.6	
7	Gnd	Ground connection.	–	
8	V_{CC1}	Supply Voltage	2.7 to 3.6	
9	RF AGC Control Voltage	RF AGC control pin. A 30 dB dynamic range can be acheived by adjusting voltage from 0.1 V (low gain) to 1.7 V (high gain).	0.1 to 1.7	
10	Exciter Out	RF exciter amplifier output pin.	–	
11	Enable 2 (See Table 1)	Tx Enable pin. A logic ″High″ (>2.4 V) enables Tx path and ″Low″ (<0.4 V) **disables Tx path except LO Buffer**.	2.4 to 3.6	0 to 0.4
12	V_{CC2}	Supply Voltage	2.7 to 3.6	
13	Exciter In	RF exciter amplifier input pin.	–	
14	Gnd	Ground connection.	–	
15	Gnd	Ground connection.	–	
16	Gnd	Ground connection.	–	
17	RF Out–	Mixer RF output pin.		
18	RF Out+	Mixer RF output pin.		
19	V_{CC4}	Supply Voltage	2.7 to 3.6	
20	IF In–	Mixer IF input pin. Input impedance is 500 Ω.	–33 dBm (Typ)	

Table 1. Enable Truth Table

Enable 1	Enable 2	Mode
0	0	Disabled
0	1	Not Applicable
1	0	Standby Mode: Disables mixer/exciter, except LO buffer
1	1	Tx Enabled

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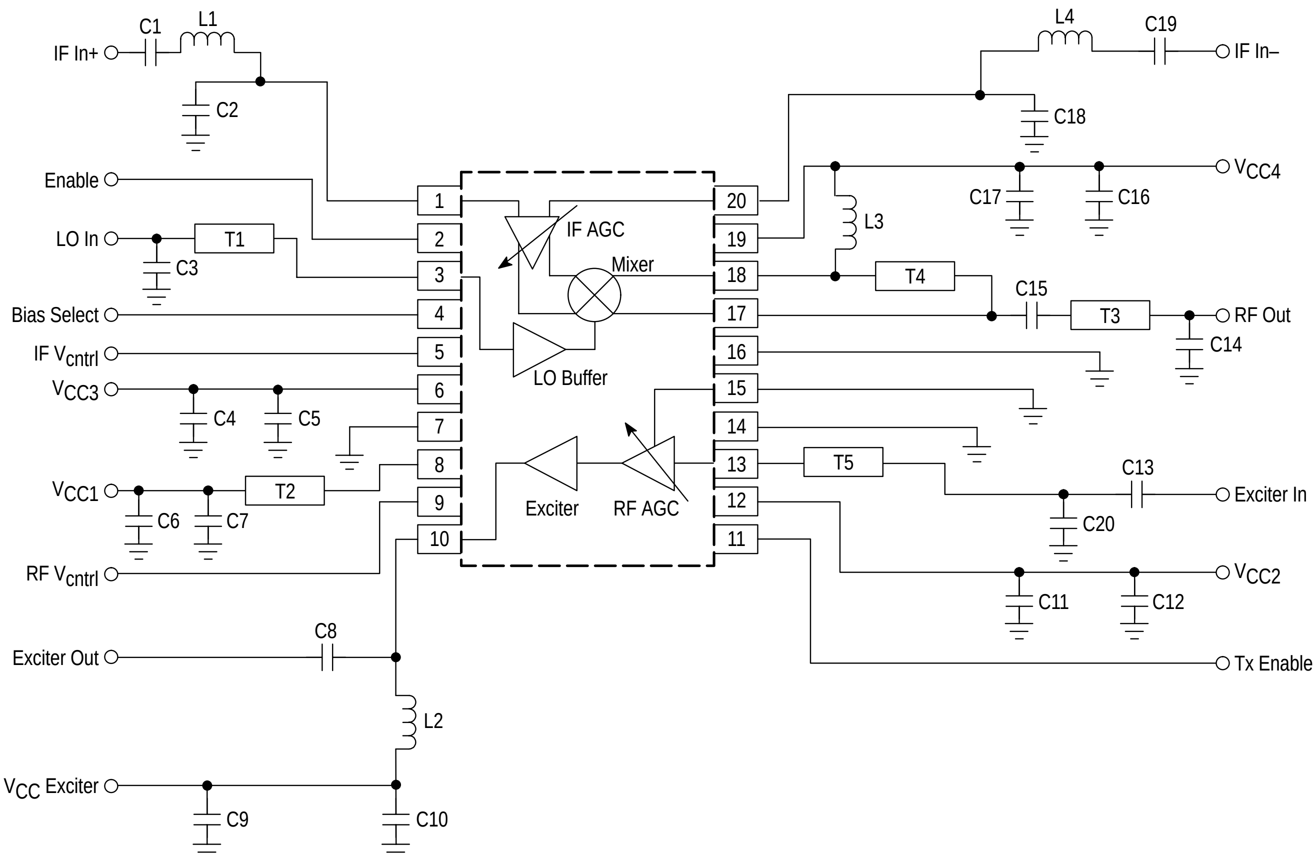
Figure 1. Application Circuit



C1, C19	1.0 nF	L1, L4	220 nH
C2, C18	4.7 pF	L2	10 nH
C3	1.7 pF	L3	18 nH
C4, C6, C9, C12, C16	10 nF	T1	50 Ω Microstrip, L = 670 mils
C5, C8, C10, C11, C13, C15, C17	30 pF	T2	50 Ω Microstrip, L = 150 mils
C7	47 pF	T3	50 Ω Microstrip, L = 400 mils
C14	3.6 pF	T4	50 Ω Stripline, L = λ/2 @ 1880 MHz
C20	1.0 pF	T5	50 Ω Microstrip, L = 350 mils

NOTES: 1. IF ports matched to 50 Ω for testing purposes.
2. Microstrip line and C7 form part of RF AGC/Exciter interstage match.
3. Er = 4.45 and board thickness = 18 mils.

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Figure 2. Gain versus Frequency (Low Current Mode)

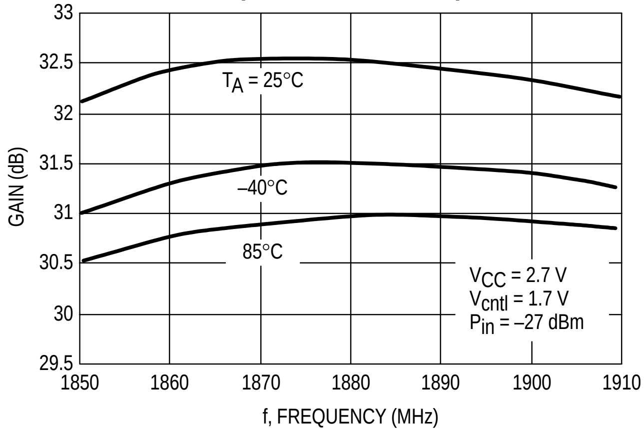

Figure 3. Gain versus Frequency (High Current Mode)

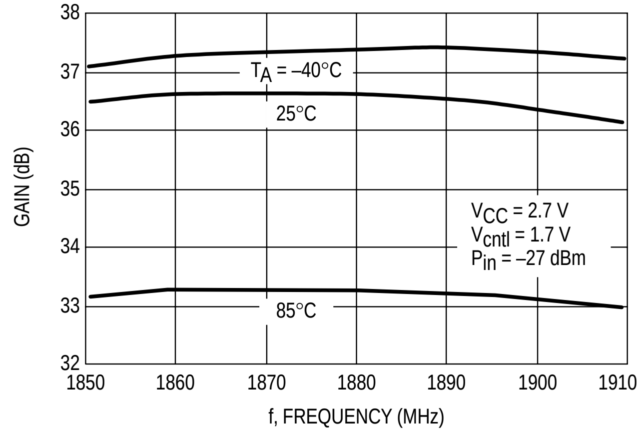

Figure 4. Gain versus LO Power (Low Current Mode)

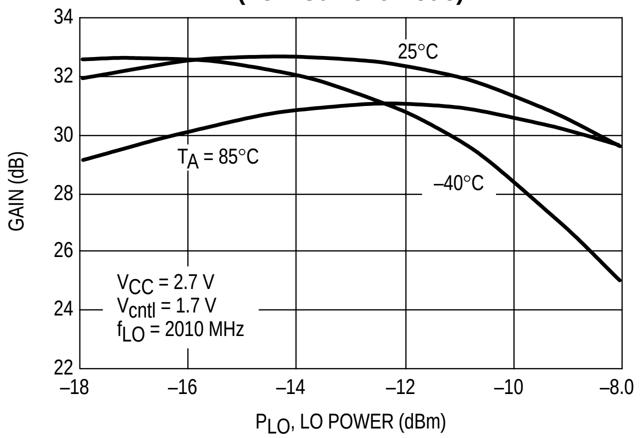

Figure 5. Gain versus LO Power (High Current Mode)

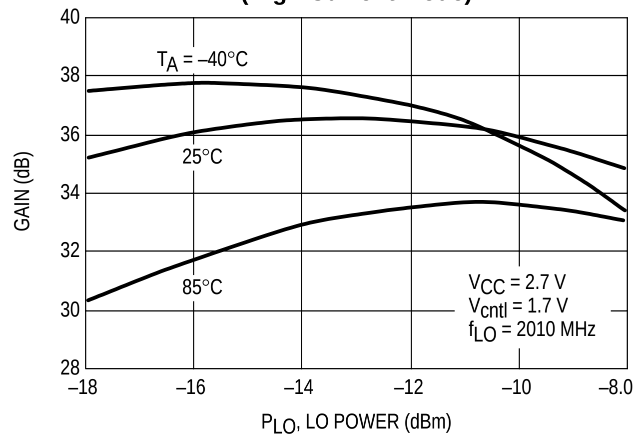

Figure 6. LO Feedthrough versus Control Voltage (Low Current Mode)

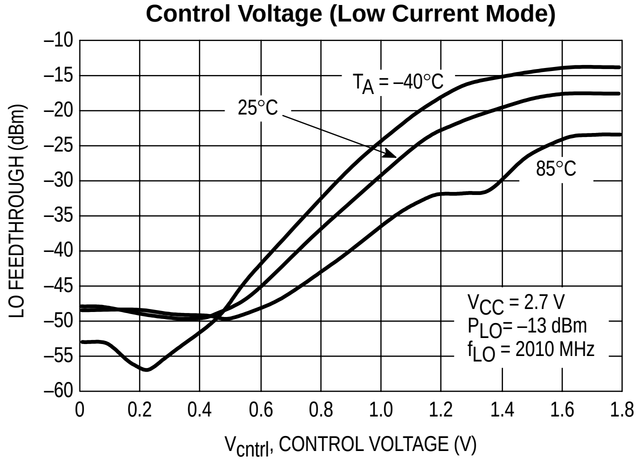

Figure 7. LO Feedthrough versus Control Voltage (High Current Mode)

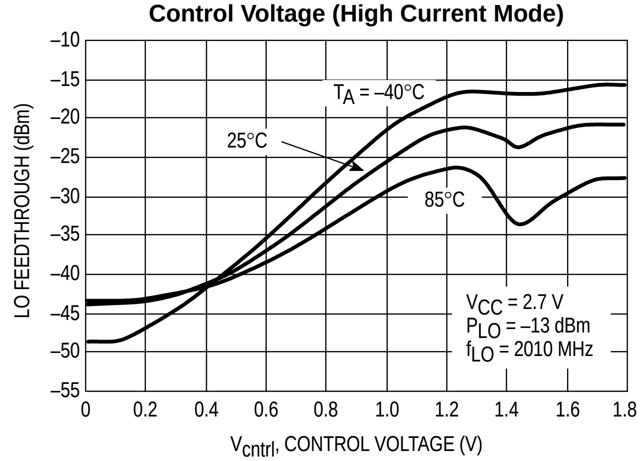

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Figure 8. Output Power versus Control Voltage (Low Current Mode)

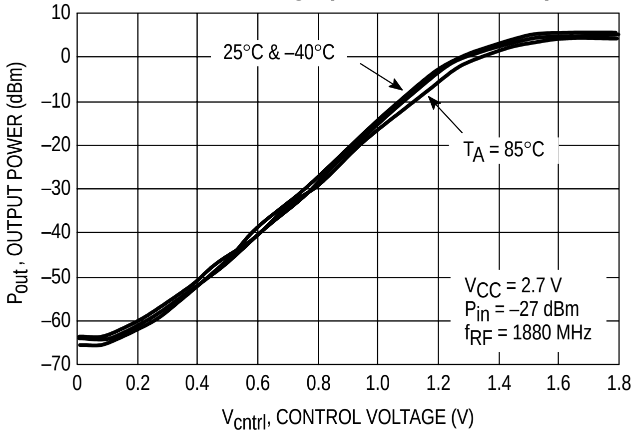


Figure 9. Output Power versus Control Voltage (High Current Mode)

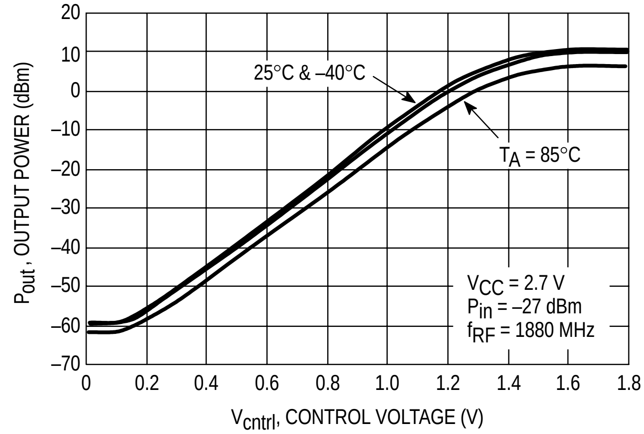
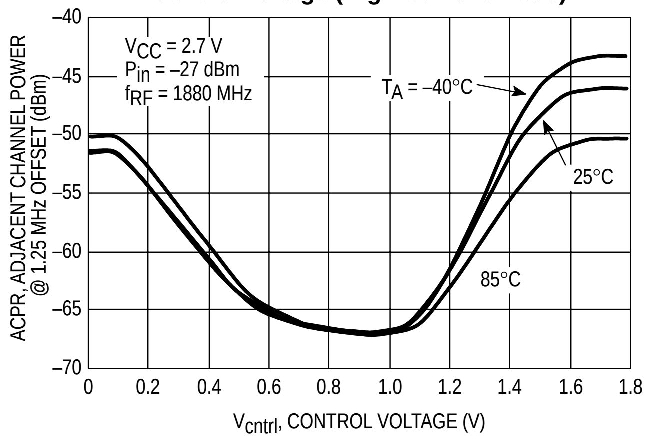


Figure 10. Adjacent Channel Power versus Control Voltage (High Current Mode)



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APPLICATION INFORMATION

Design Philosophy

The MRFIC1854A has three operating states, enable, standby, and disable. These states are controlled by the truth table shown in Table 1. The device is fully operational during the enable state and the bias level can be selected. A high bias current for maximum power CDMA or a lower bias current for CDMA at lower powers can be selected via the Bias Select pin. In the high current CDMA mode, the quiescent current is increased to maximize the linearity of the device. In the lower current bias state, the quiescent current is reduced to save current during lower power CDMA operation. The standby mode can be used to reduce current consumption during Voice Activity Factoring. In the standby mode, the LO buffer remains on to prevent VCO pulling and the bandgap reference bias circuit remains on to assure rapid device turn on. Current consumption in standby mode is 10 mA typical. The disable mode is used to turn the MRFIC1854A completely off. Leakage current in this mode is only a few microamps.

The mixer is a double–balanced “Gilbert–cell” design with a balanced LO buffer amplifier. The input and output of the mixer are differential. The IF AGC is a differential amplifier that uses the “current steering” method for gain control. The IF AGC/mixer combination has 16 dB of gain and typically draws 20 mA quiescent current in the CDMA mode. An external filter is required between the mixer and RF AGC amplifier to reduce RX band noise.

Figure 1 shows the applications circuit for the MRFIC1854A. In this circuit, the IF ports of the IF AGC have been matched to 50 Ω for testing purposes. In the actual application, the differential IF ports of the mixer would be impedance matched to an IF SAW filter. The differential impedance of the IF ports is 1600 ohms. The RF output of the mixer is configured as a differential output. A stripline balun is used to convert the RF output to single ended. DC current to the open collector output of the mixer is provided by inductor, L3 (18 nH) and transmission line, T4. Transmission lines T3 and T4, and capacitors C15 (30 pF) and C14 (3.6 pF) form the balun/output match for the mixer.

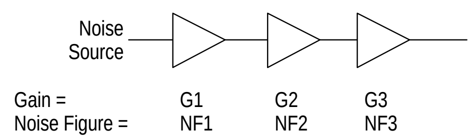
The RF AGC amplifier is a single–ended cascode design employing the standard “current steering” method of gain control. It’s ground is brought out through pin number 15 so inductance can be added to degenerate the gain for a lower noise floor. The maximum gain is around 13 dB. It typically draws 9.0 mA quiescent current in CDMA mode. The RF V_{cntrl} signal is buffered with an on–chip OpAmp then preconditioned with temperature compensation and dB/V linearization before being applied to the RF AGC amplifier.

Transmission line T2 and capacitor C7 (47 pF) are for the interstage match between the RF AGC and the exciter amplifier.

The exciter amplifier is a simple common emitter design. It is grounded directly to the exposed pad which results in 12 dB of gain. It typically draws 24 mA bias current in CDMA. Inductor L2 (10 nH), capacitor C8 (30 pF), and C10 (30 pF) provide the output matching. L2 also provides a DC current path for the open collector output.

Noise Power Considerations

In CDMA systems, the handset is required to dynamically adjust its output power to specific levels. This requires a dynamic range of as much as 90 dB from the transmitter. Another key performance specification in CDMA systems is the output noise power, both in band and out of band. Noise power specifications has caused the noise figure of the transmitter to become an important system consideration. The cascaded noise figure of the transmitter can be analyzed with the same equation used in receiver analysis. The only difference is the noise source is from the transmitter (modulator) instead of the atmosphere.



$$NF_{cascaded} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2}$$

This equation above shows that the cascaded noise figure is better if the gain is higher and the noise figure is lower for the stages close to the noise source. For this reason, it is advantageous to implement some of the gain control of a CDMA transmitter in the RF section. The MRFIC1854A integrates a RF AGC amplifier after the upmixer to improve the overall noise figure of the transmitter.

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Table 2. Scattering Parameters for Exciter Amplifier
(V_{DD} = 2.7 V, T_A = 25°C, RF V_{cntrl} = 1.8 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11} \rvert$	∠ ϕ	$\lvert S_{21} \rvert$	∠ ϕ	$\lvert S_{12} \rvert$	∠ ϕ	$\lvert S_{22} \rvert$	∠ ϕ
1700	0.319	–121.64	15.566	84.09	0.00476	–139.21	0.219	–12.29
1725	0.315	–123.78	16.291	76.55	0.00415	–126.71	0.222	–24.12
1750	0.310	–126.93	16.975	68.23	0.00406	–143.61	0.223	–35.58
1775	0.309	–130.34	17.590	56.64	0.00336	–143.09	0.237	–51.49
1800	0.304	–132.64	17.834	47.84	0.00406	–144.41	0.248	–64.80
1825	0.294	–137.08	17.944	35.98	0.00268	–141.85	0.271	–82.53
1850	0.286	–139.92	17.871	26.91	0.00411	–127.38	0.278	–94.74
1875	0.274	–141.87	17.591	17.93	0.00286	–132.49	0.298	–104.71
1900	0.261	–143.08	17.141	9.25	0.00351	–136.62	0.308	–114.83
1925	0.249	–145.61	16.374	–1.69	0.00447	–139.69	0.324	–128.42
1950	0.242	–146.86	15.738	–9.57	0.00322	–153.09	0.335	–137.57
1975	0.233	–148.86	15.046	–17.01	0.00411	–139.41	0.346	–146.12
2000	0.225	–149.74	14.132	–26.57	0.00490	–139.12	0.350	–155.24

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Table 3. Scattering Parameters for Upmixer
(V_{DD} = 2.7 V, T_A = 25°C, IF V_{cntrl} = 1.8 V, 50 Ω System)

f	IF In+		IF In–		f	RF Out (Pin 17)	
(MHz)	|S11|	∠ ϕ	|S11|	∠ ϕ	(MHz)	|S11|	∠ ϕ
70	0.830	–2.07	0.832	–2.24	1700	0.815	–55.16
80	0.828	–2.73	0.830	–2.71	1725	0.814	–55.65
90	0.826	–3.01	0.828	–2.95	1750	0.814	–56.29
100	0.826	–3.21	0.827	–3.22	1775	0.817	–56.98
110	0.822	–3.57	0.825	–3.67	1800	0.820	–57.45
120	0.821	–3.74	0.823	–3.93	1825	0.823	–58.68
130	0.821	–3.93	0.823	–4.08	1850	0.825	–59.57
140	0.818	–4.25	0.820	–4.42	1875	0.826	–60.85
150	0.818	–4.54	0.821	–4.57	1900	0.825	–62.07
160	0.818	–4.61	0.820	–4.76	1925	0.815	–63.81
170	0.817	–4.85	0.819	–5.06	1950	0.807	–64.79
180	0.815	–5.12	0.819	–5.29	1975	0.794	–65.64
190	0.815	–5.26	0.819	–5.50	2000	0.782	–66.58
200	0.813	–5.45	0.816	–5.76			
210	0.815	–5.71	0.818	–6.15			
220	0.812	–5.82	0.816	–6.13			
230	0.811	–6.38	0.817	–6.54			
240	0.812	–6.54	0.814	–6.72			
250	0.810	–6.76	0.815	–6.98			

f	LO In		f	LO In		f	LO In	
(MHz)	|S11|	∠ ϕ	(MHz)	|S11|	∠ ϕ	(MHz)	|S11|	∠ ϕ
1500	0.708	–47.83	1725	0.677	–54.36	1950	0.624	–58.20
1525	0.704	–48.38	1750	0.670	–55.34	1975	0.623	–59.40
1550	0.702	–49.02	1775	0.654	–56.33	2000	0.612	–60.59
1575	0.696	–49.55	1800	0.641	–56.34	2025	0.605	–61.04
1600	0.694	–50.11	1825	0.636	–56.65	2050	0.599	–61.70
1625	0.691	–50.83	1850	0.631	–56.59	2075	0.592	–62.19
1650	0.688	–51.47	1875	0.630	–57.04	2100	0.588	–62.99
1675	0.691	–52.18	1900	0.626	–57.38			
1700	0.681	–53.42	1925	0.622	–57.84			

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OUTLINE DIMENSIONS

PLASTIC PACKAGE
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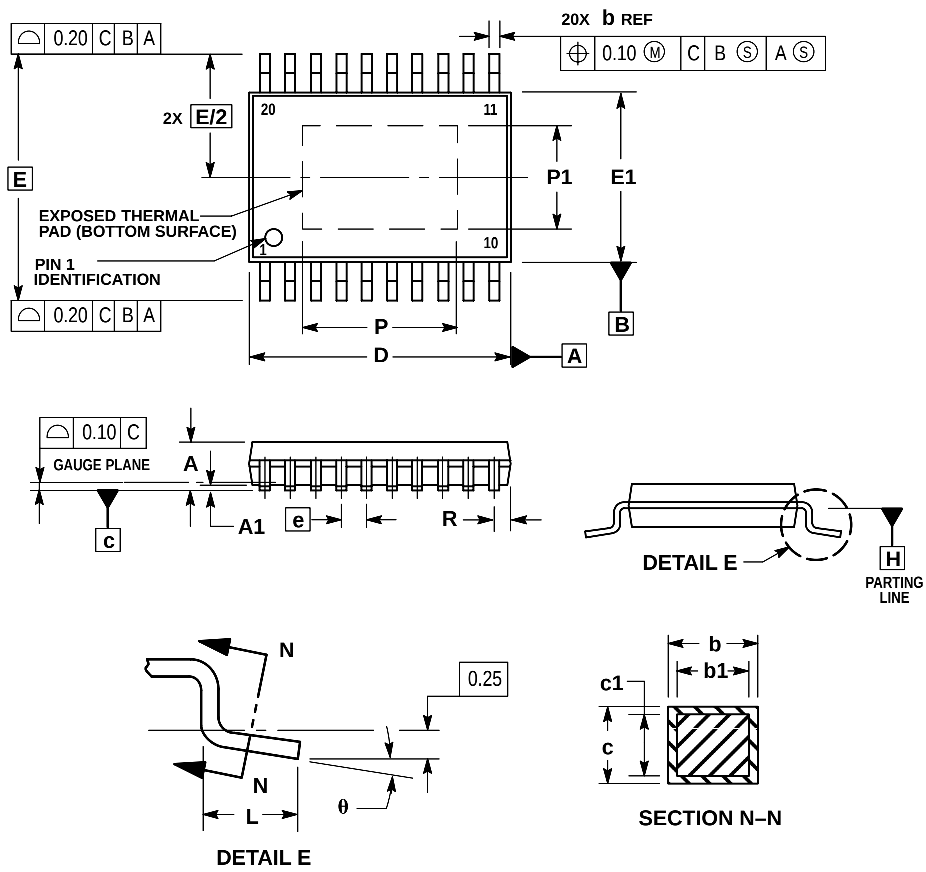
(TSSOP–20EP)
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.20
A1	0.00	0.10
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	6.40	6.60
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
P	—	4.80
P1	—	3.00
R	0.27	0.37
θ	0 °	8 °

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