Freescale Semiconductor
Data Sheet

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MWCT1200DS

Features

- Low power (5 W) solution for Wireless Power Consortium (WPC) compliant transmitter design
- Conforms to the V1.1 low power WPC specifications
- Supports wide DC input voltage range starting from 4.5 V, typically 5 V, 12 V
- Integrated digital demodulation on chip
- Supports all types of receiver modulation strategies (AC capacitor, AC resistor and DC resistor)
- Supports power loss Foreign Object Detection (FOD)
- Supports resonance shift FOD before the power transfer action.
- Dynamic input power limit for power limited power supply input, like USB power
- Super low standby power (less than 40 mW) by Freescale GPIO Touch Sensing technology
- Supports any free positioning multiple coils power transmitter solutions using frequency and duty cycle control
- LEDs for system status indication
- Over-voltage/current/temperature protection
- Software based solution to provide maximum design freedom and product differentiation
- FreeMASTER GUI tool to enable configuration, calibration, and debugging

Applications

- Low Power Wireless Power Transmitter
  Any free positioning multiple coils solution with frequency & duty cycle control (WPC types or customer properties)

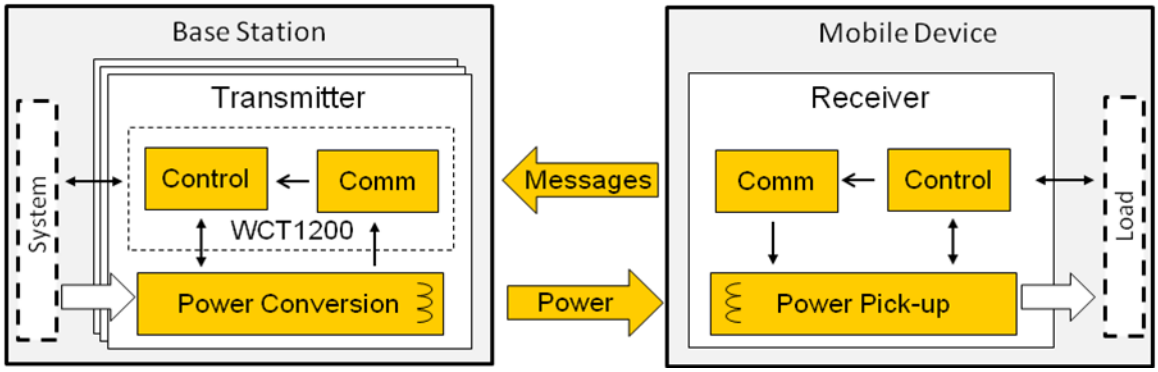
Overview Description

The WCT1200 is a wireless power transmitter controller that integrates all required functions for WPC “Qi” compliant wireless power transmitter design. It’s an intelligent device to work with Freescale touch sensing technology or use periodically analog PING (configurable by user) to detect a mobile device for charging while gaining super low standby power. Once the mobile device is detected, the WCT1200 controls the power transfer by adjusting the operation frequency of the power stage according to message packets sent by the mobile device.

In order to maximize the design freedom and product differentiation, WCT1200 supports any low power free positioning multiple coils power transmitter design (WPC types or customization) using operation frequency and duty cycle control by software based solutions. Besides, easy-to-use FreeMASTER GUI tool with configuration, calibration and debugging functions provides user-friendly design experience and speed time-to-market.

The WCT1200 includes digital demodulation module to reduce external components, dynamic input power limit function for power limited power supply input, over-voltage/current/temperature protection and FOD method to protect from overheating by misplaced metallic foreign objects. It also handles any abnormal condition and operational status, and provides comprehensive indicator outputs for robust system design.

Wireless Charging System Functional Diagram



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1 Absolute Maximum Ratings

1.1 Electrical operating ratings

Table 1 Absolute maximum electrical ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min.	Max.	Unit
Supply Voltage Range	V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	–0.3	5.5	V
RESET Input Voltage Range	V_{IN_RESET}	Pin Group 2	–0.3	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		–	–5.0	mA
Output clamp current, per pin[4]	V_{OC}		–	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		–25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1,2	–0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	–0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	–0.3	4.0	V
Ambient Temperature	T_A		–40	85	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		–55	150	°C

1. Default Mode:
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. Continuous clamp current.
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through an ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (= VSS–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

1.2 Thermal handling ratings

Table 2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	–	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

1.3 ESD handling ratings

Table 3 ESD handling ratings

Characteristic[1]	Min.	Max.	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

1.4 Moisture handling ratings

Table 4 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

2 Electrical Characteristics

2.1 General characteristics

Table 5 General electrical characteristics

Recommended operating conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)							
Characteristic	**Symbol**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test conditions**
Supply Voltage[2]	V_{DD} ,V_{DDA}		2.7	3.3	3.6	V	-
ADC Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA} -0.6		V_{DDA}	V	-
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V	-
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		-0.1	0	0.1	V	-
Input Voltage High (digital inputs)	V_{IH}	1 (Pin Group 1)	0.7×V_{DD}		5.5	V	-
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	1 (Pin Group 2)	0.7×V_{DD}	-	V_{DD}	V	-
Input Voltage Low (digital inputs)	V_{IL}	1 (Pin Group 1,2)			0.35×V_{DD}	V	-
Output Source Current High (at V_{OH} min.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 1 (Pin Group 1) 1 (Pin Group 1)	 - -		 -2 -9	mA	
Output Source Current High (at V_{OL} max.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 1 (Pin Group 1,2) 1 (Pin Group 1,2)	 - -		 2 9	mA	-
Output Voltage High	V_{OH}	1 (Pin Group 1)	V_{DD} -0.5	-	-	V	I_{OH} = I_{OHmax}
Output Voltage Low	V_{OL}	1 (Pin Group 1,2)	-	-	0.5	V	I_{OL} = I_{OLmax}
Digital Input Current High pull-up enabled or disabled	I_{IH}	1 (Pin Group 1)	-	0	+/-2.5	µA	V_{IN} = 2.4V to 5.5V
		1 (Pin Group 2)					V_{IN} = 2.4V to V_{DD}

Comparator Input Current High	I_{IHC}	1 (Pin Group 3)		0	+/-2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	-	50	kΩ	-
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	-	50	kΩ	-
Comparator Input Current Low	I_{ILC}	1 (Pin Group 3)	-	0	+/-2	µA	V_{IN} = 0V
Output Current[1] High Impedance State	I_{OZ}	1 (Pin Group 1,2)	-	0	+/-1	µA	-
Schmitt Trigger Input Hysteresis	V_{HYS}	1 (Pin Group 1,2)	0.06×V_{DD}	-	-	V	-
Input capacitance	C_{IN}		-	10	-	pF	-
Output capacitance	C_{OUT}		-	10	-	pF	-
GPIO pin interrupt pulse width[5]	T_{INT_Pulse}	6	1.5	-	-	Bus clock	-
Port rise and fall time (high drive strength). Slew disabled.	$T_{Port\_H\_DIS}$	7	5.5	-	15.1	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (high drive strength). Slew enabled.	$T_{Port\_H\_EN}$	7	1.5	-	6.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew disabled.	$T_{Port\_L\_DIS}$	8	8.2	-	17.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew enabled.	$T_{Port\_L\_EN}$	8	3.2	-	9.2	ns	2.7 ≤ VDD ≤ 3.6V
Device (system and core) clock frequency	f_{SYSCLK}		0.001	-	100	MHz	-
Bus clock	f_{BUS}		-	-	50	MHz	-

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. ADC specifications are not guaranteed when VDDA is below 3.0 V.
3. Total chip source or sink current cannot exceed 75mA.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25mA.
5. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
6. The greater synchronous and asynchronous timing must be met.
7. 75 pF load
8. 15 pF load

2.2 Device characteristics

Table 6 General device characteristics

Power mode transition behavior					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
T_{S2R}	STOP mode to RUN mode	6.79	7.27	µs	1
$T_{LPS2LPR}$	LPS mode to LPRUN mode	240.9	551	µs	2
Reset and interrupt timing					
Symbol	**Characteristic**	**Min.**	**Max.**	**Unit**	**Notes**
t_{RA}	Minimum $\overline{\text{RESET}}$ Assertion Duration	16	-	ns	3
t_{RDA}	$\overline{\text{RESET}}$ desertion to First Address Fetch	865 × T_{OSC} + 8 × T_{SYSCLK}	-	ns	4
t_{IF}	Delay from Interrupt Assertion to Fetch of first instruction (exiting STOP mode)	361.3	570.9	ns	
PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{POR_A}	POR Assert Voltage[5]	-	2.0	-	V
V_{POR_R}	POR Release Voltage[6]	-	2.7	-	V
V_{LVI_2p7}	LVI_2p7 Threshold Voltage	-	2.73	-	V
V_{LVI_2p2}	LVI_2p2 Threshold Voltage	-	2.23	-	V
JTAG timing					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
f_{OP}	TCK frequency of operation	DC	f_{SYSCLK}/8	MHz	
t_{PW}	TCK clock pulse width	50	-	ns	
t_{DS}	TMS, TDI data set-up time	5	-	ns	
t_{DH}	TMS, TDI data hold time	5	-	ns	
t_{DV}	TCK low to TDO data valid	-	30	ns	
t_{TS}	TCK low to TDO tri-state	-	30	ns	
Regulator 1.2 V parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**

V_{CAP}	Output Voltage[7]	-	1.22	-	V
I_{SS}	Short Circuit Current[8]	-	600	-	mA
T_{RSC}	Short Circuit Tolerance (VCAP shorted to ground)	-	-	30	Mins
V_{REF}	Reference Voltage (after trim)	-	1.21	-	V

Phase-locked loop timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{Ref_PLL}	PLL input reference frequency[9]	8	8	16	MHz
f_{OP_PLL}	PLL output frequency[10]	200	-	400	MHz
t_{Lock_PLL}	PLL lock time[11]	35.5	-	73.2	µs
t_{DC_PLL}	Allowed Duty Cycle of input reference	40	50	60	%

Relaxation oscillator electrical specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{ROSC_8M}	8 MHz Output Frequency[12] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C	 7.84 7.76 -	 8 8 405	 8.16 8.24 -	 MHz MHz kHz
$f_{ROSC\_8M\_Delta}$	8 MHz Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
f_{ROSC_200k}	200 kHz Output Frequency[13] RUN Mode • -40°C to 105°C	 194	 200	 206	 kHz
$f_{ROSC\_200k\_Delta}$	200 kHz Output Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 85°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
t_{Stab}	Stabilization Time • 8 MHz output[14] • 200 kHz output[15]	 - -	 0.12 10	 - -	 µs µs
t_{DC_ROSC}	Output Duty Cycle	48	50	52	%

Flash specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{hvpgm4}	Longword Program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector Erase high-voltage time[16]	-	13	113	ms
$t_{hversall}$	Erase All high-voltage time[16]	-	52	452	ms

$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)[17]	-	-	60	µs
t_{pgmchk}	Program Check execution time[17]	-	-	45	µs
t_{rdrsrc}	Read Resource execution time[17]	-	-	30	µs
t_{pgm4}	Program Longword execution time	-	65	145	µs
t_{ersscr}	Erase Flash Sector execution time[18]	-	14	114	ms
t_{rd1all}	Read 1s All Blocks execution time	-	-	0.9	ms
t_{rdonce}	Read Once execution time[17]	-	-	25	µs
$t_{pgmonce}$	Program Once execution time	-	65	-	µs
t_{ersall}	Erase All Blocks execution time[18]	-	70	575	ms
t_{vfykey}	Verify Backdoor Access Key execution time[17]	-	-	30	µs
$t_{flashretp10k}$	Data retention after up to 10 K cycles	5	50[19]	-	years
$t_{flashretp1k}$	Data retention after up to 1 K cycles	20	100[19]	-	years
$n_{flashcyc}$	Cycling endurance[20]	10 K	50 K[19]	-	cycles

12-bit ADC electrical specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage[21]	3	3.3	3.6	V
f_{ADCCLK}	ADC conversion clock[22]	0.1	-	10	MHz
R_{ADC}	Conversion range with single-ended/unipolar[23]	V_{REFL}	-	V_{REFH}	V
V_{ADCIN}	Input voltage range (per input) with internal reference[24]	0	-	V_{DDA}	V
t_{ADC}	Conversion time[25]	-	8	-	t_{ADCCLK}
t_{ADCPU}	ADC power-up time (from adc_pdn)	-	13	-	t_{ADCCLK}
I_{ADCRUN}	ADC RUN current (per ADC block)	-	1.8	-	mA
INL_{ADC}	Integral non-linearity[26]	-	+/- 1.5	+/- 2.2	LSB[27]
DNL_{ADC}	Differential non-linearity[26]	-	+/- 0.5	+/- 0.8	LSB[27]
E_{GAIN}	Gain Error	-	0.996 to 1.004	0.99 to 1.101	-
ENOB	Effective number of bits	-	10.6	-	bits
I_{INJ}	Input injection current[28]	-	-	+/-3	mA
C_{ADCI}	Input sampling capacitance	-	4.8	-	pF

Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	-	3.6	V
I_{DDHS}	Supply current, High-speed mode(EN=1, PMODE=1)	-	300	-	µA
I_{DDLS}	Supply current, Low-speed mode(EN=1, PMODE=0)	-	36	-	µA
V_{AIN}	Analog input voltage	V_{ss}	-	V_{DD}	V

V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[29] • CR0[HYSTCTR]=00 • CR0[HYSTCTR]=01 • CR0[HYSTCTR]=10 • CR0[HYSTCTR]=11	- - - -	5 25 55 80	13 48 105 148	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} -0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode(EN=1, PMODE=1)[30]	-	25	50	ns
t_{DLS}	Propagation delay, low-speed mode(EN=1, PMODE=0) [30]	-	60	200	ns
t_{DInit}	Analog comparator initialization delay[31]	-	40	-	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
R_{DAC6b}	6-bit DAC reference inputs	V_{DDA}	-	V_{DD}	V
INL_{DAC6b}	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[32]
DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB

PWM timing parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{PWM}	PWM clock frequency[33,34]	-	100	-	MHz
S_{PWMNEP}	NanoEdge Placement (NEP) step size	-	312	-	ps
t_{DFLT}	Delay for fault input activating to PWM output deactivated	1	-	-	ns
t_{PWMPU}	Power-up time[35]	-	25	-	µs

Timer timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
P_{IN}	Timer input period	$2T_{timer}$ + 6	-	ns	36
P_{INHL}	Timer input high/low period	$1T_{timer}$ + 3	-	ns	36
P_{OUT}	Timer output period	$2T_{timer}$ - 2	-	ns	36
P_{OUTHL}	Timer output high/low period	$1T_{timer}$ - 2	-	ns	36

SCI timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{SCI}	Baud rate	-	(f_{MAX_SCI} /16)	Mbit/s	37
PW_{RXD}	RXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	
PW_{TXD}	TXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	

IIC timing							
Symbol	**Characteristic**	**Min.**		**Max.**		**Unit**	**Notes**
		Min.	**Max.**	**Min.**	**Max.**		
f_{SCL}	SCL clock frequency	0	100	0	400	kHz	
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs	
t_{SCL_LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs	
t_{SCL_HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs	
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs	
t_{HD_DAT}	Data hold time for IIC bus devices	0[38]	3.45[39]	0[40]	0.9[38]	µs	
t_{SU_DAT}	Data set-up time	250[41]	-	100[42]	-	ns	
t_r	Rise time of SDA and SCL signals	-	1000	20 + 0.1C_b	300	ns	43
t_f	Fall time of SDA and SCL signals	-	300	20 + 0.1C_b	300	ns	42, 43
t_{SU_STOP}	Set-up time for STOP condition	4	-	0.6	-	µs	
t_{BUS_Free}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	ns	

1. Clock configuration: CPU and system clocks= 100 MHz; Bus Clock = 100 MHz.
2. CPU clock = 200 kHz and 8 MHz IRC on standby.
3. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.
4. TOSC means oscillator clock cycle; TSYSCLK means system clock cycle.
5. During 3.3 V VDD power supply ramp down
6. During 3.3 V VDD power supply ramp up (gated by LVI_2p7)
7. Value is after trim
8. Guaranteed by design
9. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
10. The frequency of the core system clock cannot exceed 50 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
11. This is the time required after the PLL is enabled to ensure reliable operation.
12. Frequency after application of 8 MHz trimmed.
13. Frequency after application of 200 kHz trimmed.
14. Standby to run mode transition.
15. Power down to run mode transition.
16. Maximum time based on expectations at cycling end-of-life.
17. Assumes 25 MHz flash clock frequency.
18. Maximum times for erase parameters based on expectations at cycling end-of-life.
19. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
20. Cycling endurance represents number of program/erase cycles at -40°C ≤ Tj ≤ 125°C.
21. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed.
22. ADC clock duty cycle is 45% ~ 55%.
23. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
24. In unipolar mode, positive input must be ensured to be always greater than negative input.
25. First conversion takes 10 clock cycles.

26. INLADC/DNLADC is measured from VADCIN = VREFL to VADCIN = VREFH using Histogram method at x1 gain setting.
27. Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 gain setting.
28. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC.
29. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD-0.6V.
30. Signal swing is 100 mV.
31. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
32. 1 LSB = Vreference/64.
33. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
34. Temperature and voltage variations do not affect NanoEdge Placement step size.
35. Powerdown to NanoEdge mode transition.
36. Ttimer = Timer input clock cycle. For 100 MHz operation, Ttimer = 10 ns.
37. fMAX_SCI is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 50 MHz depending on part number) or 2x bus clock (max. 100 MHz) for the device.
38. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
39. The maximum tHD_DAT must be met only if the device does not stretch the LOW period (tSCL_LOW) of the SCL signal.
40. Input signal Slew = 10 ns and Output Load = 50 pF
41. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
42. A Fast mode IIC bus device can be used in a Standard mode IIC bus system, but the requirement tSU_DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU_DAT = 1000 + 250 = 1250ns (according to the Standard mode I2C bus specification) before the SCL line is released.
43. Cb = total capacitance of the one bus line in pF.

2.3 Thermal operating characteristics

Table 7 General thermal characteristics

Symbol	Description	Min	Max	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	85	°C

3 Typical Performance Characteristics

3.1 System efficiency

The typical maximum system efficiency (RX output power vs. TX input power) on the WCT1200 solution with the standard receiver (RX for short, bq51013B based) is more than 71%.

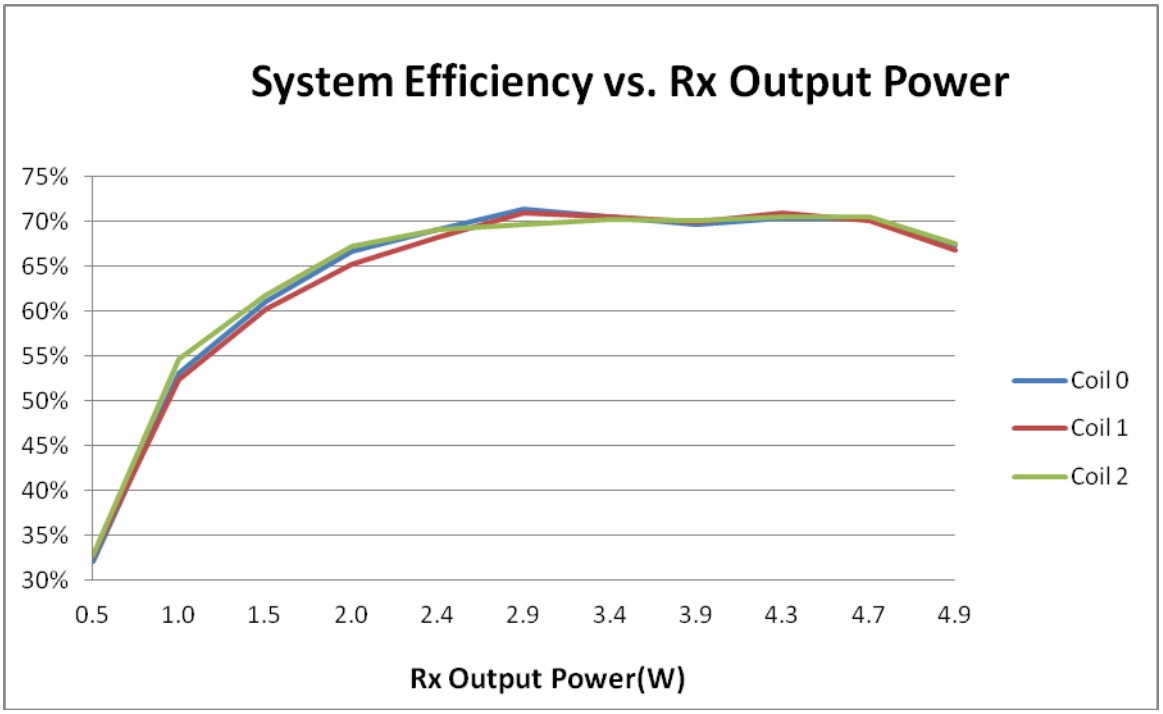

Figure 1 System efficiency on the WCT1200 solution

Note: Power components are the main factor to determine the system efficiency, such as drivers and MOSFETs. The efficiency data in Figure 1 is obtained on Freescale reference solution with A28 configuration.

Figure 2 shows the active charging area of the Freescale WCT1200 A28 transmitter reference solution — transmitter well charges receiver at different X/Y offsets. For this test, the receiver is tested with constant 700 mA loading and 3 mm Z gap between transmitter surface and receiver surface.

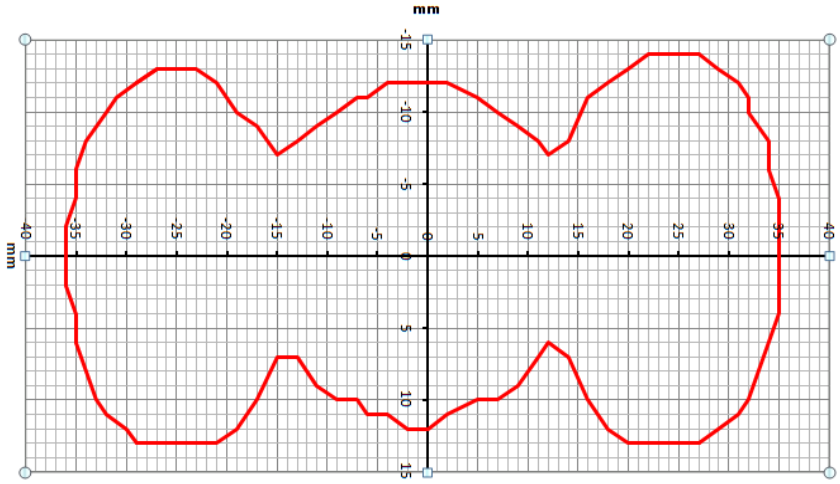

Figure 2 Active charging area on the WCT1200 A28 transmitter reference solution

3.2 Standby power

WCT1200 solution only consumes the very low standby power with the special low power control method, and can further achieve ultra low standby power by using the Freescale Touch Sensing technology. (Freescale reference solution with A28 configuration uses Freescale GPIO Touch Sensing Software technology).

Transmitter (TX for short) power consumption in standby mode: < 11 mA (55 mW with 5 V DC input)

Transmitter power consumption in standby mode with GPIO Touch Sensing technology: < 8 mA (40 mW with 5 V DC input)

3.3 Digital demodulation

WCT1200 solution employs digital demodulation algorithm to communicate with RX. This method can achieve high performance, low cost, very simple coil signal sensing circuit with less component number.

3.4 Foreign object detection

WCT1200 solution uses flexible, intelligent, and easy-to-use FOD algorithm to assure accurate foreign metal objects detection. With Freescale FreeMASTER GUI tool, FOD algorithm can be easily calibrated to get accurate power loss information especially for very sensitive foreign objects. On the Freescale reference solution, the calculated power loss resolution between transmitted power and received power is less than 100 mW.

The WCT1200 solution also supports the Resonance Shift FOD. When the FO is present on the active charging surface without the RX, the system detects this FO and enters the fault state.

3.5 Dynamic input power limit

When TX is powered by a power limited power supply, such as USB power, WCT1200 can limit the TX output power and provide necessary margin relative to the input power supply capability. By monitoring the input voltage and input current of TX, when it drops to a specified level and still positive Control Error Packet (CEP) is received, WCT1200 will stop increasing output power and control TX operating in input power limit state. User can know the system is in DIPL control mode by LED indication, LED1 and LED2 will be in fast blinking mode when input power is limited. When the WCT1200 enters DIPL mode, it will not exit from this state until the RX is moved away. The input voltage level for DIPL control can be configured in the WCT1200 example project.

4 Device Information

4.1 Functional block diagram

From Figure 3, the low power feature with Freescale Touch Sensing technology is optional according to user requirements for minimizing standby power. When this function is not deployed, its pins can be configured for other purpose of use. Besides, 10 pins (dashed) are also configurable for different design requirements to provide design freedom and differentiation.

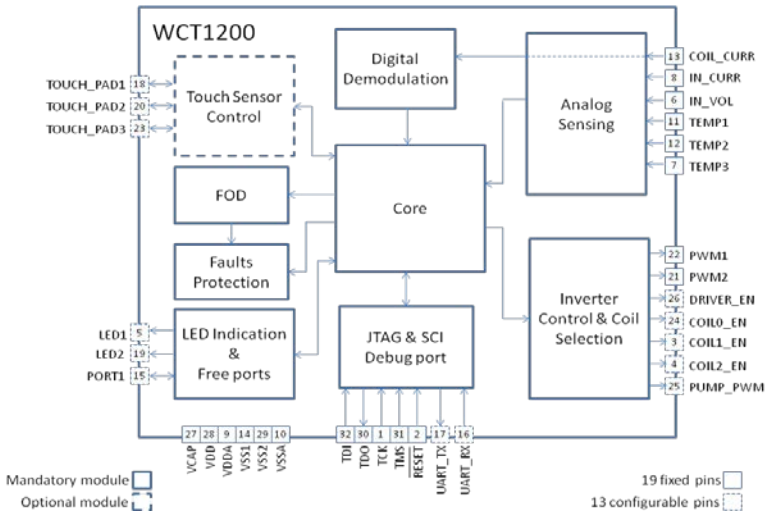

Figure 3 WCT1200 function block diagram

4.2 Pinout diagram

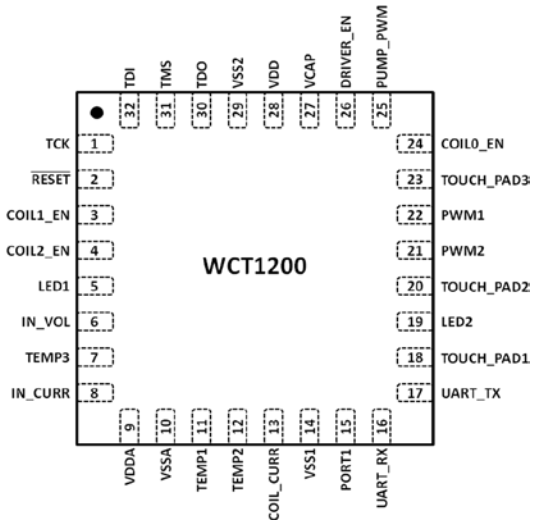

Figure 4 WCT1200 pin configuration (32-pin QFN)

4.3 Pin function description

By default, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the FreeMASTER GUI tool.

Table 8 Pin signal descriptions

Signal name	Pin No.	Type	Function description
TCK	1	Input	Test clock input, connected internally to a pull-up resistor
$\overline{\text{RESET}}$	2	Input	A direct hardware reset, when RESET is asserted low, device is initialized and placed in the reset state. Connect a pull-up resistor and decoupling capacitor
COIL1_EN	3	Output	Primary coil1 enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
COIL2_EN	4	Output	Primary coil2 enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
LED1	5	Output	LED1 drive output for system status indicator
		Input/Output	General purpose input/output pin
IN_VOL	6	Input	Input voltage detection, analog input pin
TEMP3	7	Input	Temperature detection input 3, analog input pin
IN_CURR	8	Input	Input current detection, analog input pin
VDDA	9	Supply	Analog power to on-chip analog module
VSSA	10	Supply	Analog ground to on-chip analog module
TEMP1	11	Input	Temperature detection input 1, analog input pin
TEMP2	12	Input	Temperature detection input 2, analog input pin
COIL_CURR	13	Input	Primary coil current detection, analog input pin
VSS1	14	Supply	Digital ground to on-chip digital module
PORT1	15	Input/Output	General purpose input/output pin
UART_RX	16	Input	UART receive data input
		Input/Output	General purpose input/output pin
UART_TX	17	Output	UART transmit data output
		Input/Output	General purpose input/output pin
TOUCH_PAD1	18	Input/Output	Touch pad detection interface 1
			General purpose input/output pin
LED2	19	Output	LED drive output for system status indicator

		Input/Open-drain output	IIC serial clock
TOUCH_PAD2	20	Input/Output	Touch pad detection interface 2
		Input/Open-drain output	IIC serial data line
PWM2	21	Output	PWM output 2, control one half of inverter bridge
PWM1	22	Output	PWM output 1, control another half of inverter bridge
TOUCH_PAD3	23	Input/Output	Touch pad detection interface 3
			General purpose input/output pin
COIL0_EN	24	Output	Primary coil0 enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
PUMP_PWM	25	Output	PWM output for charger pump
		Input/Output	General purpose input/output pin
DRIVER_EN	26	Output	Pre-driver chip output and auxiliary power enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
VCAP	27	Supply	Connect a 2.2μF or greater capacitor between this pin and VSS
VDD	28	Supply	Digital power to on-chip digital module
VSS2	29	Supply	Digital ground to on-chip digital module
TDO	30	Output	Test data output
TMS	31	Input	Test mode select input, connect a pull-up resistor to VDD
TDI	32	Input	Test data input, connected internally to a pull-up resistor

4.4 Ordering information

Table 9 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order this device.

Table 9 WCT1200 ordering information

Device	Supply voltage	Package type	Pin count	Ambient temp.	Order number
MWCT1200	2.7 to 3.6V	Quad Flat No-leaded (QFN)	32	-40 to +85℃	MWCT1200CFM

4.5 Package outline drawing

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number of 98ASA00473D.

5 Wireless Charging System Operation Principle

5.1 Fundamentals

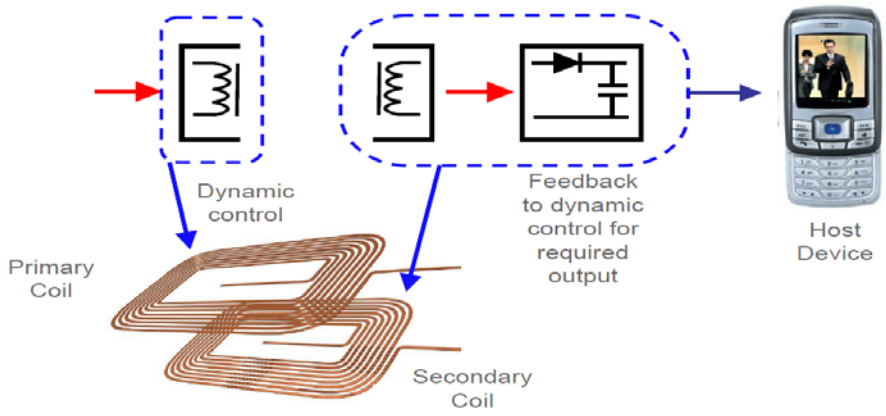

Figure 5 Working principle of Wireless Charging System

The Wireless Charging system works as the digital switched mode power supply with the transformer, which is separated into two parts: The transformer primary coil is on the transmitter, working as the TX coil, and the transformer secondary coil is on the receiver side as the RX coil. The basic system working principle diagram is shown in Figure 5. As this system works based on magnetic induction, the better coupling between the TX coil and RX coil gain better system efficiency, so the RX coil should be closely and center aligned with the TX coil as possible. After the RX coil receives the power from the TX coil by magnetic field, it regulates the received voltage to power the load, and send its operational information to TX according to specific protocol by the communication link. Then the system can achieve the closed-loop control, and power the load stably and wirelessly.

5.2 Power transfer

When the wireless charging receiver is placed on the transmitter coils and the required conditions are met, the power transfer starts.

- The TX coil and RX coil meet proper specifications, such as the inductance, coil dimensions, coil materials, and magnets shielding.
- The distance is in suitable range (less than 6 mm for Z axis) between the TX coil and RX coil.
- The RX coil should be in the active area of the TX charging surface, which still means that the TX coil and RX coil should be coupled well. Coil coupling highly impacts the power transfer efficiency, and good coupling can achieve high efficiency.

The coil shielding is also important, because the magnetic field leaking into the air will not transfer the power from TX to RX, and the shielding can contain the magnetic field as much as possible to improve the system efficiency and avoid bad effect of the nearby objects from interference. The shielding should be designed to place at the back of the TX coil and RX coil.

The power transfer must function correctly under the conditions when the RX coil is on the TX charging area during the overall system operational phases. To facilitate power transfer control, set the system operating frequency on the right side of resonant frequency of resonant network (because resonant converter works in a soft-switching mode when its operational frequency is over the resonant frequency and its output power changes monotonously with the adjustment of the operational frequency).

For WPC specification, the “Qi” defines the coil inductance and resonant capacitance, the resonant frequency is fixed as 100 kHz, then power transfer can work normally by adjusting the TX operating frequency from 110 kHz to 205 kHz with fixed 50% duty cycle. The higher operating frequency means lower power transferred to RX, and lower operating frequency means higher power transferred to RX. The duty cycle will decrease when the operating frequency reaches to 205 kHz. Figure 6 shows the voltage gain (voltage on resonant inductor vs. the input voltage) change with operating frequency, as we can see voltage gain will increase when the operating frequency decreases.

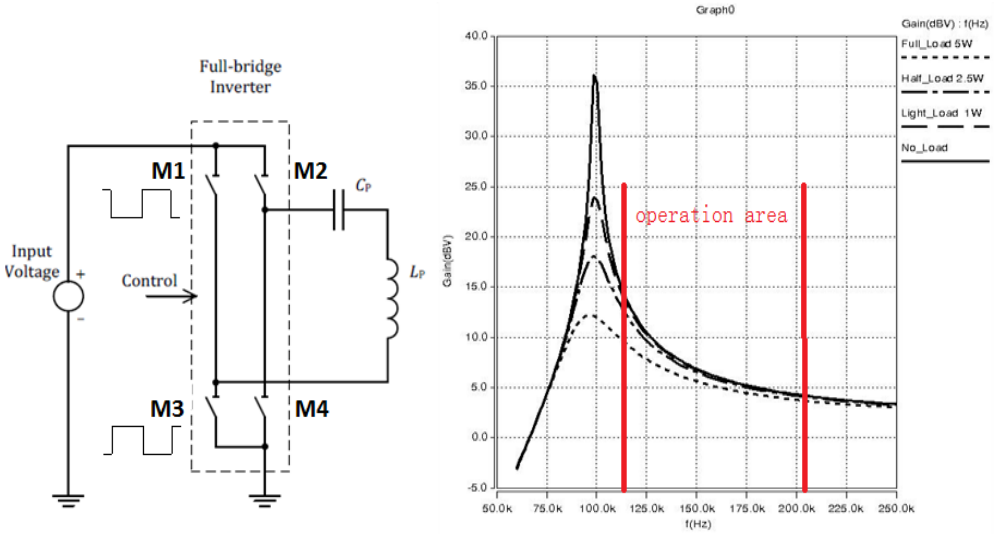

Figure 6 LC Parallel resonant converter control principle

5.3 Communication

5.3.1 Modulator

In low power wireless charging application, there is only one-way communication link between the receiver and the transmitter, and the receiver sends the information to transmitter by communication packages. The information includes the power requirements, received power, receiver ID and version, receiver power ratings, and charging end command.

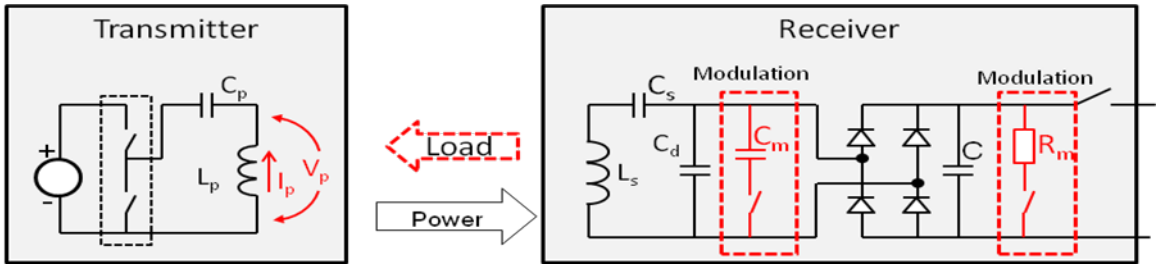

Figure 7 Load modulation scheme

Figure 7 shows the modulation technologies at the RX side. RX modulates load by switching modulation resistor (R_m, AC side or DC side), or modulation capacitor (C_m, AC side). The amplitude of voltage/current on RX coil is modulated through connecting or disconnecting modulation load (resistor or capacitor). The amplitude of voltage/current on TX coil is also modulated to reflect load switching through magnetic induction. Then TX demodulates the sensed amplitude change of current (ΔI_p > 15mA), or voltage (ΔV_p > 200mV) on TX coil. Figure 8 shows how the RX switching modulation capacitor affects the TX resonant characteristics (Gain vs. Frequency characteristics).

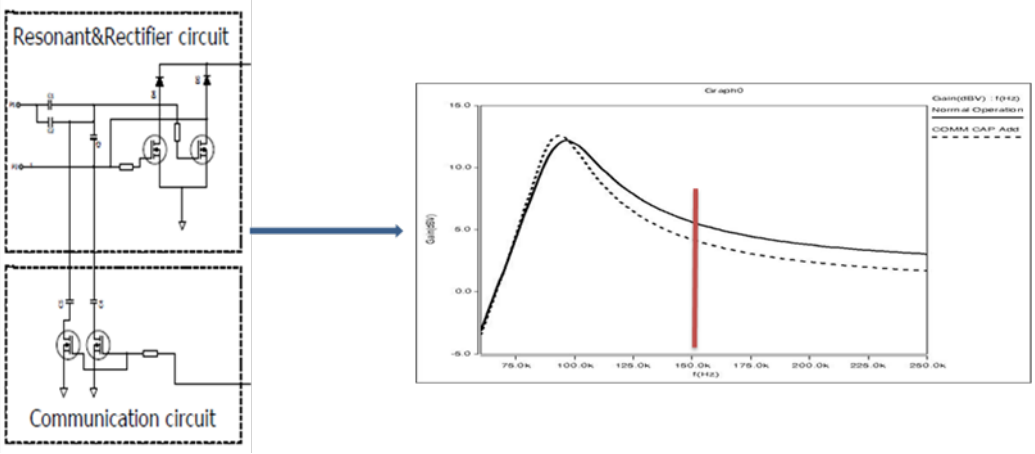

Figure 8 Load modulation principle

The Bode diagram in Figure 8 shows that the voltage amplitude on the TX coil will decrease when the modulation capacitor is connected on the RX side. The RX couples the communication signal onto the power signal through modulating power signal directly. The WPC defines the modulation baud rate to 2 kbps.

5.3.2 Demodulator

As the RX modulates the communication signal on the power signal, the TX has to demodulate communication signal from the power signal to get the correct information sent by RX, and further control the whole system operation. Figure 9 shows the power signal (voltage) waveform coupled with the communication signal on the TX coil.

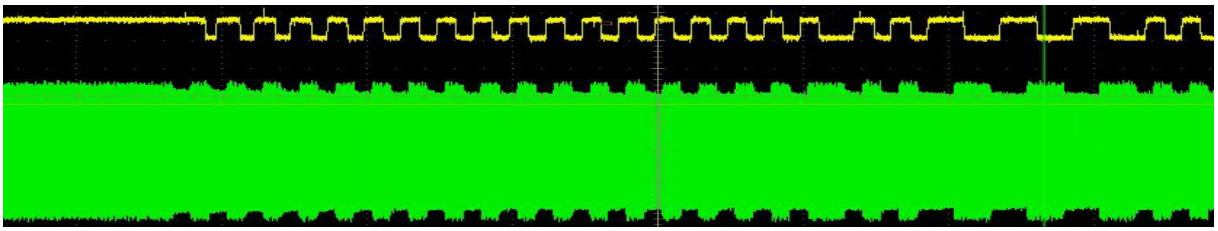

Figure 9 TX coil voltage profile with RX modulation

The WCT1200 employs the software solution to implement demodulator, also called digital demodulation technology. The WCT1200 directly senses the voltage on resonant capacitor through the very simple, low cost RC circuit (Figure 10), and the high speed 12-bit cyclic ADC is capable of handling the maximum 205 kHz signal in time to assure accurate signal sampling. After the resonant capacitors voltage value is obtained, the equivalent resonant current in the coil can be calculated, and this coil current is used for the digital demodulation algorithm. After that, WCT1200 decodes the demodulated information to get the accurate communication message. Besides, the calculated coil current is also used for the FOD algorithm.

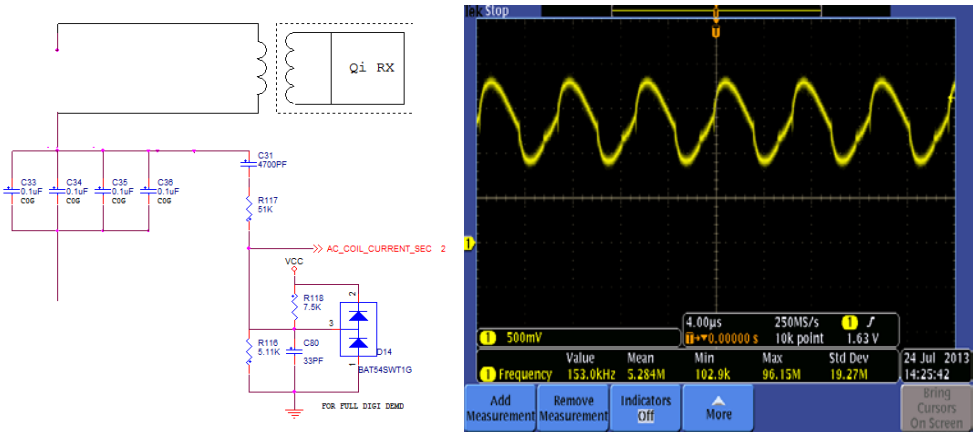

Figure 10 Sensing circuit and waveform of TX resonant capacitor voltage

With Freescale digital demodulation algorithm, the WCT1200 can support all available modulation methods on the RX, such AC resistor, DC resistor, or AC capacitor, and pass all compliance tests defined in the WPC specifications.

5.3.3 Message encoding scheme

The WCT1200 demodulates and decodes the message sent from RX that is encoded by the differential bi-phase scheme. A logic ONE bit is encoded using two transitions in the 2 kHz clock period (500 us), and a logic ZERO bit using one transition. One 8-bit data, one Start bit, one Parity bit and one Stop bit

compose one message byte. A typical packet consists of four parts, namely a preamble ($\geq$ 11 bits), a header (1 byte), a message (1 to 27 bytes), and a checksum (1 byte). Figure 11 shows the detailed message encoding scheme that WPC defines. Digital demodulation module in WCT1200 extracts the digital encoded communication signal from the analog power signal. The decoding module packs up the demodulated bits into message byte, and then message packet, which is processed by the system State Machine.

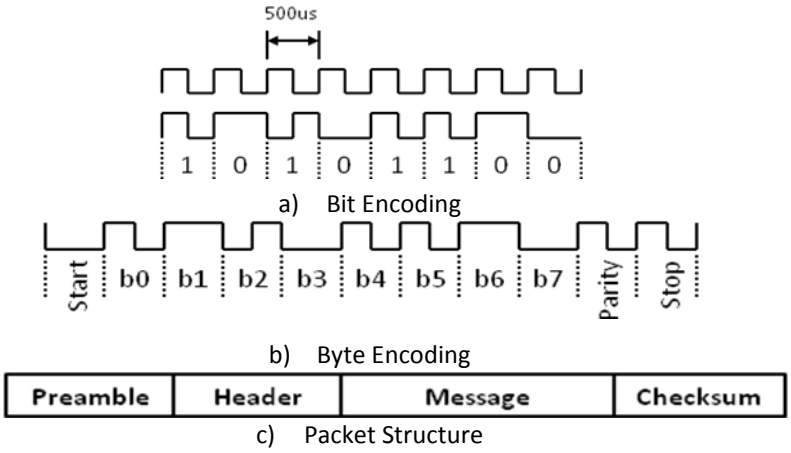

Figure 11 WPC communication message encoding scheme

5.4 System control state machine

WCT1200 embeds a WPC "Qi" State Machine to process received communication message from RX and control power transfer to RX. The overall system behavior between transmitter and receiver is controlled by the State Machine shown in Figure 12.

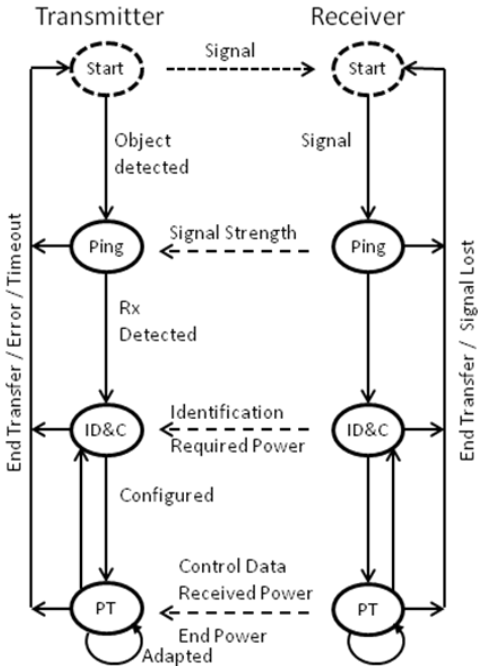

Figure 12 WPC Wireless Charging System state machine

5.4.1 Start phase

In the Start phase, the TX system runs in low power mode to judge whether an object is placed on the TX coil surface. The PING operation runs every 400 ms, and during the PING interval, the system is in the

Start phase. If the touch sensing function is enabled, the WCT1200 enters deep low power mode as described in the Standby Power section.

5.4.2 PING phase

In the PING phase, the TX system works on both analog PING and digital PING to detect a receiver placed on the TX charging area. The analog PING time is far shorter than the digital PING for power-saving purposes. The analog PING enables a very short AC pulse on the TX coil, WCT1200 reads back the coil current and compares it with the predefined current change threshold to judge whether an object is put on. The default coil current change threshold is 5%, which the user can set in FreeMASTER GUI to get good sensitivity.

For digital PING, the TX system applies a power signal at 175 kHz with 50% duty cycle to attempt to set up communication with RX. In response, RX must send out the Signal Strength packet. Signal Strength message indicates the degree of coupling between TX coil and RX coil, and is the percentage of rectifier output signal against the possible maximum PING signal.

$$\text{Signal Strength Value} = \frac{U}{U_{max}} \times 256$$

In this formula, U is the monitored variable, and U_{max} is the maximum value, which the RX expects for during digital PING.

When the Signal Strength packet is received in the PING phase, the system enters the Identification & Configuration phase.

5.4.3 Identification & Configuration phase

In the Identification & Configuration phase, the TX system continues to identify the receiver device and collects the configuration information for a power transfer setup.

Required packets in the Identification & Configuration phase:

- Identification packet (0x71)
- Extended Identification packet (0x81)*
- Configuration packet (0x51)

* If Ext bit of Identification packet is set to 1.

The system must receive these packets in order:

- Identification packet (0x71)
- Extended Identification packet (0x81)
- Up to 7 optional configuration packets (0x51)
    - Power Control Hold-off Packet (0x06)
    - Proprietary Packet (0x18 – 0xF2)

- Configuration Packet (0x51)

If the Identification & Configuration packets are received in right timing and format according to specifications, the TX system enters power transfer phase.

5.4.4 Power transfer phase

During the Power Transfer phase, the TX system receives the Control Error packet from the RX and controls the amount of output power by adjusting the PWM frequency in 110 kHz – 205 kHz range with 50% duty cycle. If the PWM frequency reaches 110 kHz and the positive Control Error value is still received (more output power required), the TX system keeps the current power output. If the PWM frequency reaches 205 kHz and the negative Control Error value is still received, the TX system decreases PWM duty cycle in the range from 50% to 10%.

During the power transfer, the TX system also executes the FOD algorithm by using the power packet received from the RX.

Required packets in the Power Transfer phase:

- Control Error packet (0x03)
- Received Power packet (0x04)

When the TX system receives the following packets, it ends power transfer in the Power Transfer phase:

- Charge Status packet (0x05) *
- End Power Transfer packet (0x02)

* If the Charge Status packet value is set to 0xFF.

In the Power Transfer phase, the TX system always checks the timing of the Control Error packet and the Received Power packet, and whether it complies with specifications. If any violation happens, the TX system ends the power transfer.

5.5 Standby power

When there is no charging activity, the TX system enters the standby (Start phase) mode. In standby mode, all analog parts on a board are powered down by the WCT1200, and the WCT1200 itself runs in low power state during the PING interval. The WCT1200 can enter deep sleep state if Freescale GPIO Touch Sensing technology is supported in TX system. In this case, WCT1200 is in LPSTOP (low power STOP) state, only three GPIO touch pads, timer and CPU are periodically activated to sense the electrode capacitance change to know if an object is placed on TX charging area. By the Freescale Touch Sensing technology, the standby current of the overall TX system can be as low as 8 mA under 5 volts input voltage condition.

5.6 Foreign object detection

Following the latest WPC “Qi” specifications, WCT1200 supports the Foreign Object Detection (FOD) function. The WCT1200 detects foreign objects on the TX charging area by using a power loss method

during the Power Transfer phase. TX power loss is calculated by using these equations. When the power loss is greater than a predefined threshold, the system FOD protection is activated. For a “Qi” v1.1 or later version compliant RX, it should send Received Power packet to TX, which equals the RX output power plus RX power loss. But for a “Qi” v1.0 compliant RX, it sends only rectifier output power to TX. The FOD function in WCT1200 is only active when a “Qi” v1.1 or later version compliant RX is detected.

To get an accurate power loss on the TX, the user must calibrate the analog sensing modules on the TX system to get accurate input power value and transmitted power value. As a part of the FOD solution, Freescale provides an easy-to-use and user-friendly FreeMASTER GUI tool for input voltage, input current and power loss calibration on the TX board. FOD parameters are burned in the WCT1200 internal Flash, about how to tune FOD related parameters, like power loss threshold, see the *WCT Runtime Debug User Guide* (WCT1XXXRTDUG).

$$P_{loss} = P_{transmitted} - P_{received}$$
$$P_{transmitted} = P_{Tx\_in} - P_{Tx\_losses}$$
$$P_{received} = P_{Rx\_out} + P_{Rx\_losses}$$
$$P_{Tx\_losses} = C_2 I_{coil}^2 + C_1 I_{coil} + C_0$$

Where:

- P_{loss} — Wireless charging system power loss
- $P_{transmitted}$ — Transmitted power from TX coil
- $P_{received}$ — Received power from RX coil
- P_{Tx_in} — TX input power from power source
- P_{Tx_losses} — Total TX power losses for producing transmitted power
- P_{Rx_out} — RX output power to load
- P_{Rx_losses} — Total RX power losses for producing output power
- C_2, C_1, C_0 — Coefficients to estimate the total TX power losses by coil current
- I_{coil} — TX coil current

Besides, Resonance Shift FOD method is also supported by WCT1200, the system will detect the object by feedback signal during analog PING, and check if it is valid RX. If it is the FO, the system enters the fault state and avoids entering the power transfer state.

6 Application Information

6.1 On-board regulator

The auxiliary power supply provides supply source for control, sensing, communication and driving circuits. In transmitter design, 3.3 V is required for WCT1200, ADC conditioning circuits, and communication demodulation circuits. And 5 V input voltage is supplied for inverter pre-driver circuit. LDO GS7108 is selected to generate 3.3 V power, this IC can provide 100 mA output current capacity to the load. At the same time, other type LDO can be used to meet the requirements, and the below parameters must be considered for the regulator selection.

- Maximum input voltage: > 6 V
- Maximum output current: > 100 mA
- Output voltage accuracy: < 1%

6.2 Inverter and driver control

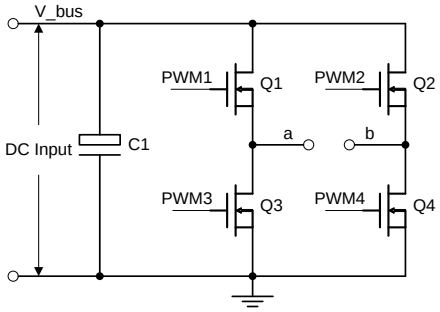

Figure 13 Schematic full-bridge inverter topology

Figure 13 shows the schematic full-bridge inverter. The input voltage range of this application is from 4.5 to 5.5 volts, and the input current range is from 0 to 2 amps. LC resonant network is connected between the middle point (a) of bridge leg 1 and the middle point (b) of bridge leg 2. N-channel MOSFETs of Q1–Q4 are controlled by PWMs generated from WCT1200, and the operating frequency range of MOSFETs is 110 kHz to 205 kHz. To meet the system efficiency and power transfer requirements, these are some suggestions for the MOSFETs and driver IC selection.

- Full-bridge inverter MOSFETs: V_{ds} >= 20 V, $R_{ds(on)}$ < 20 mΩ for power switching application MOSFET is recommended. The MOSFET is the critical component for the system efficiency, AON7400A from AOS is selected as the main power switch, and AON7400A is a 30 V, 40 A, $R_{ds(on)}$ < 10.5 mΩ (V_{gs} = 4.5 V), N-channel power MOSFET.
- Driver: the synchronous BUCK driver IC or bridge driver IC can meet the requirements for the full-bridge inverter. The driver IC should handle 8 V voltage input for some de-rating applications. The synchronous BUCK driver IC is recommended for this application because of good cost advantage, so NCP3420DR2G is selected on this design. This driver IC has the following features:

- Supporting low voltage power supply down to 4.6 V.
- Very short propagation delay from input to output (less than 30 ns).
- 2 channels PWM can be controlled by WCT1200 independently.
- Safety Timer and Overlap protection circuit.

6.3 Primary coil and resonant capacitor

The resonant network is shown in Figure 14, which is the basic LC series resonant network circuit. The section of “Power Transfer” in chapter of “Wireless Charging System Operation Principle” describes the basic operation process of LC resonant inverter. For the design principles of resonant components parameters, consider two points:

- Set a fixed resonant frequency (WPC defines it as 100 kHz)
- Configure a suitable Q (quality factor) value to output required power in specific operational range

Meanwhile, all specifications define the specific resonant network parameters for available TX types.

Like WPC A28 TX type, C_r = 400 nF (for coils furthest from the shielding) or 357 nF (for coils closest to the shielding), L_p = 6.4 uH (for coils furthest from the shielding) or 6.9 uH (for coils closest to the shielding), this resonant network parameters can meet the low power (5 W) wireless charger requirements under defined operational conditions.

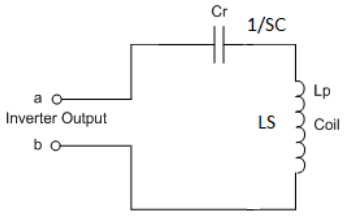

Figure 14 Schematic resonant network circuit

L_p and C_r are connected in series, the resonant frequency of A28 resonant network can be obtained:

$$f_r = \frac{1}{2\pi\sqrt{L_p C_r}} = \frac{1}{2\pi\sqrt{6.4\times10^{-6}\times400\times10^{-9}}} = 100\text{kHz}$$

The electrical and mechanical features of the TX coils are defined in details in specifications. Figure 15 shows the mechanical features of A28 type coil, which are the two types out of the WCT1200 supporting WPC TX coils.

- Number of turns per layer: N = 9
- Number of layer = 1
- Inductance:
  - Lp = 6.9 ± 10% uH for coils closest to the shielding

- Lp = 6.4 ± 10% uH for coils furthest from the shielding

- Wire: type 2 litz wire having 105 strands of No. 40 AWG (0.08 mm diameter) or equivalent

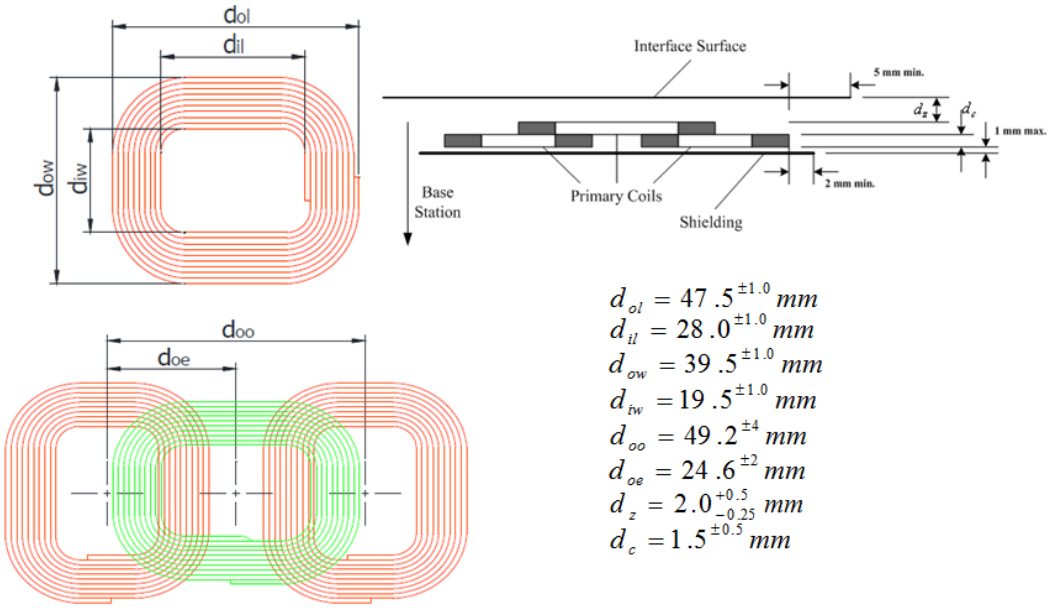

Figure 15 Example of A28 3 coils specification

Typically, the A28 coil has three coils. The inductance is different, so the system should change the resonant capacitor value for different coil to keep the resonant frequency to be about 100 kHz. In addition, different manufacturers provide the same type of coil, such as TDK, Sumida, E&E, and Mingstar. The system is also required to work well with these coils.

For resonant capacitor, COG ceramic capacitor is selected to meet the critical system requirements, because the capacitance affects the resonant frequency of the resonant network, and 5% tolerance is allowed for the whole system operation. This capacitance with the A28 type coil can achieve 100 kHz resonant frequency. Two types of capacitors are recommended:

- Murata: GRM31C5C1H104JA01L – 1206 – 50 V – 100 nF
- TDK: C3225C0G1H104JT – 1210 – 50 V – 100 nF

6.4 Primary coil selection switches and charge pump circuits

As the WCT1200 supports the multi-coil topology, the coil switches circuit is used to select the proper coil to activate. Figure 16 shows the system block diagram and the details of the selection switches circuit for the A28 type coil.

To achieve the switch function, the VCC_SW should be about 8 – 15 V DC in the system. On the A28 reference design, the WCT1200 PUMP_PWM (20 kHz frequency & 50% duty cycle PWM) pin is used to drive the charge pump circuit to achieve the 2X input voltage source.

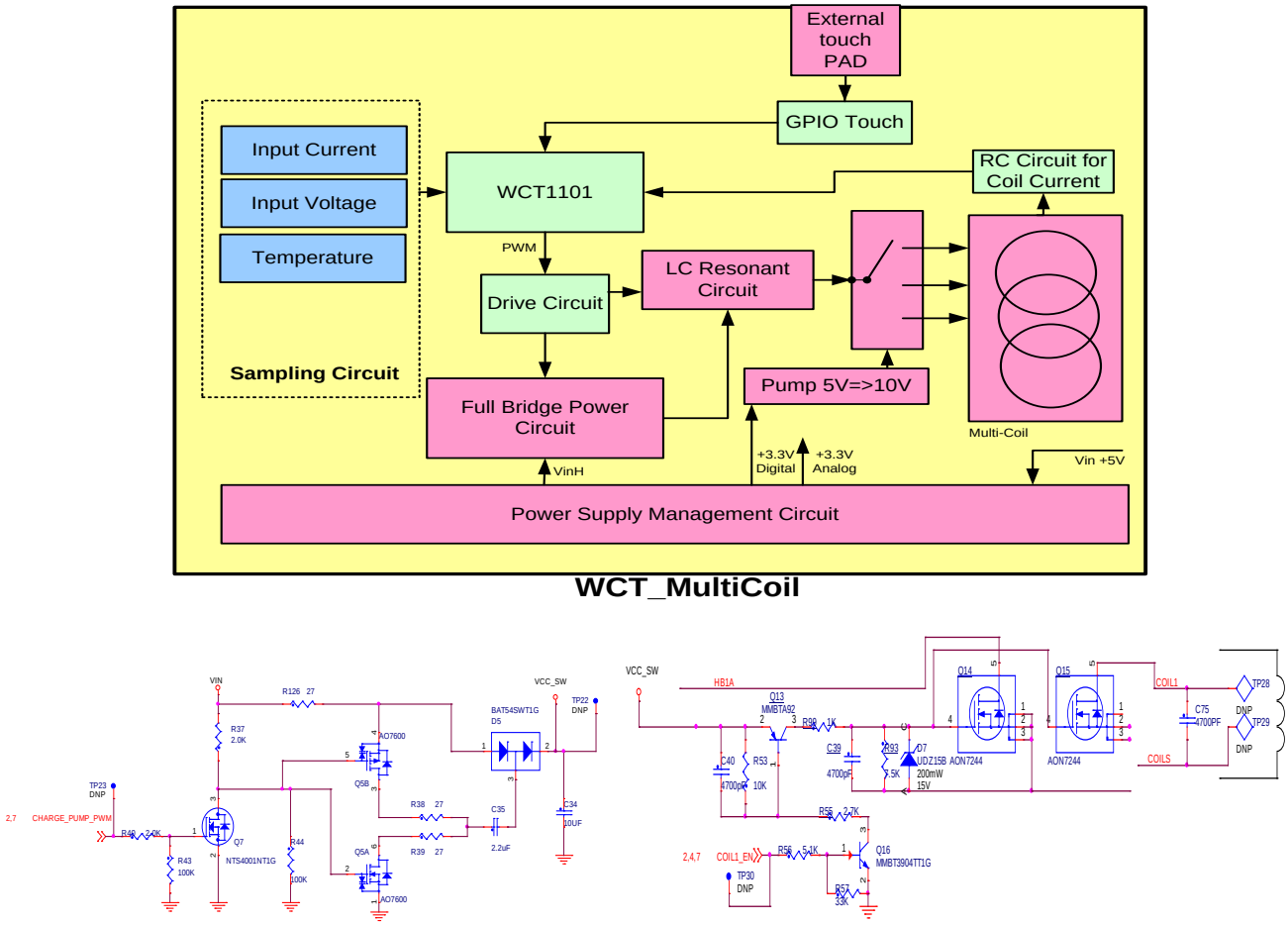

Figure 16 WCT-5WTXMULTI block diagram, charge pump and coil selection switches circuits

Low $R_{ds(on)}$, 60 V V_{ds} MOSFET is recommended for the A28 solution.

6.5 Low power control

To achieve low power consumption, the driver and analog circuits power are shut down when the system is in standby mode or interval time between the PINGs. The DRV_EN_AUX_P signal is designed to achieve this target. Figure 17 is the typical application circuit to control VCCH on or off.

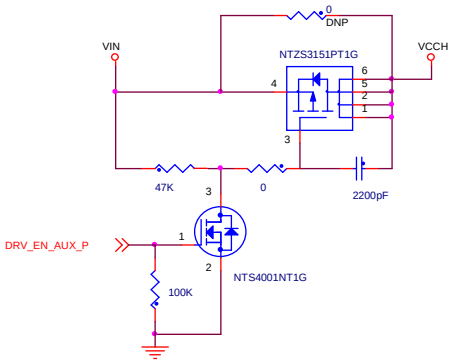

Figure 17 Auxiliary Power Enable Circuit

The power source of the full-bridge drivers and current sensor can be controlled by the above circuit. This circuit is still benefited from the Touch Sensor technology. When the TX goes to the standby mode, the WCT1200 enters deep sleep mode, and the power of the driver and analog circuits is shut down by the DRV_EN_AUX_P signal. If this feature is not used, leave this pin (DRIVER_EN) open.

6.6 GPIO touch sensing

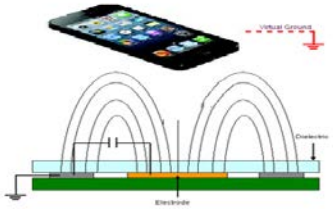

Figure 18 Basic Theory of Capacitive Touch Sensor

Capacitive touch sensor is selected in this design, and three additional electrode touch pads are designed to sense the placement of mobile device. When the mobile device is put on the TX active charging area, GPIO Touch Sensing will detect the capacitance change on the pad, and then enter digital PING phase for device identification. Figure 18 shows the basic theory for this method, and TOUCH_PAD1, TOUCH_PAD2, TOUCH_PAD3 pins for this feature.

Because of FOD function, these electrode touch pads should not be placed on the top of the TX coils, and 5 mm XY (horizontal) distance is required between the TX coil and the electrode touch pad.

6.7 ADC input channels

To sense the necessary analog signals in the TX system, all ADC input channels are designed for these analog signals. This list describes the design details of these analog signals in the default setting. For the specific circuits, see the system example design schematics.

- Input voltage: 154 kΩ and 20 kΩ resistors to divide the input voltage.
- Input current: 15 mΩ current sensing resistor and 1:100 current sensor (CS30CL) are recommended.

- Temperature: 100 kΩ NTC (NCP15WL104E03RC) and 51 kΩ resistors are recommended to sense the temperature of board or coil (over-temperature protection point: 60°C @ 0.94 V ADC input, below this voltage the system will enter over-temperature fault state).
- Coil current: 51 kΩ and 5.11 kΩ to divide the resonant capacitor voltage. The 5.1 kΩ pull-up resistor and 33 pF filter capacitor are recommended.

6.8 Faults handling/recovery

WCT1200 supports several types of fault protections during the TX system operation, including FOD fault, TX system fault, and RX device fault. According to the fault severity, the faults are divided into several rates: fatal fault, immediate retry fault, and retry fault after several minutes. The fault thresholds and time limits are described in the *WCT Runtime Debug User's Guide*. Table 10 lists all the available fault types and their corresponding fault handlings.

Table 10 System faults handling

Types	Name	Handling	Recovery wait time	Conditions	Description
FOD Fault	FOD fault	TX system shuts off after fault lasts 1 second	Wait 5 minutes or RX removed	1, Power loss base threshold 2, Power loss indication to power cessation 3, Power loss fault retry times	Foreign object is detected and lasts for the defined time. The system shuts off, and waits for recovery time or RX removed to enable power transfer. The time limit can be configured by user.
TX System Fault	Hardware fault (ADC, Chip)	TX system shuts off immediately	No retry any more	-	Once hardware fault happens, the TX system shuts off forever.
	EEPROM corruption fault	TX system shuts off immediately	No retry any more	-	The WCT1200 checks data validity of EEPROM after power on, stop running forever if EEPROM is corrupted.
	Input over-voltage	TX system shuts off immediately	No retry any more	Safety input threshold	When input voltage exceeds the threshold, the TX system shuts off forever.
	Input over-power	TX system shuts off immediately	Wait for 5 minutes or RX removed	Input power threshold	When input power exceeds the threshold, the TX system shuts off immediately and waits for recovery time to enable power transfer.
	Coil over-current	TX system shuts off immediately	Retry immediately	Coil current threshold	When coil current exceeds the threshold, the TX system shuts off immediately and tries PING again.

	TX over-temperature	TX system shuts off immediately	Wait for 5 minutes or RX removed	Temperature threshold	When the temperature on the board or the coil exceeds the threshold during power transfer, the TX system shuts off immediately and waits for recovery time or RX removed to enable power transfer.
	Analog PING fault	TX system shuts off immediately	No retry any more	-	When coil current in analog PING exceeds the threshold, the TX system shuts off forever.
	Received Power packet timeout	TX system shuts off immediately	Wait for 5 minutes or RX removed	-	When Received Power packet timeout, the TX system shuts off immediately and waits for recovery time to enable power transfer.
	Select fault coil	TX system shuts off immediately	Wait for 5 minutes or RX removed	-	When fault coil selected, the TX system shuts off immediately and waits for recovery time to enable power transfer.
RX Device Fault	RX internal fault (EPT-02)	TX system shuts off immediately	No retry any more	-	The TX system shuts off forever if End Power packet is received and End Power code is internal fault.
	RX over-temperature (EPT-03)	TX system shuts off immediately	Wait for 5 minutes or RX removed	-	The TX system shuts off and waits for recovery time to enable power transfer if End Power packet is received and End Power code is over temperature.
	RX over-voltage (EPT-04)	TX system shuts off immediately	Wait for 5 minutes or RX removed	-	The TX system shuts off and tries PING again if End Power packet is received and End Power code is over voltage.
	RX over-current (EPT-05)	TX system shuts off immediately	Retry immediately	-	The TX system shuts off and tries PING again if End Power packet is received and End Power code is over current.
	RX battery failure (EPT-06)	TX system shuts off immediately	No retry any more	-	The TX system shuts off forever if End Power packet is received and End Power code is battery failure.
	No response (EPT-08)	TX system shuts off immediately	Retry immediately	-	The TX system shuts off and tries PING again if End Power packet is received and End Power code is no response.

6.9 LEDs function

Two pins (user can re-configure them to different configuration ports) on WCT1200 are used to drive LEDs for different system status indication in this design, such as charging, standby and fault status, etc. The LEDs can work on different functions using software configuration. WCT1200 controls the LEDs on/off and blink according to the parameters configuration under different system status. For how to configure LED functions by the FreeMASTER GUI tool, see the *WCT Runtime Debug User's Guide* (WCT1XXXRTDUG). The suggested LED functions are listed in Table 11 for different system status indication.

Table 11 System LED modes

LED configuration option	Description	LED #	LED operation state						
			Standby	Charging	Charge complete	Power limit	FOD fault	TX fault	RX fault
Default	Default choice	LED 1	Off	Blink slow	Off	Blink fast	On	On	On
		LED 2	Blink slow	On	On	Blink fast	Off	Off	Off
Option 1	Choice 1	LED 1	Off	Blink slow	On	Off	Off	Off	Off
		LED 2	Off	Off	Off	Blink fast	Blink fast	Blink fast	Blink fast
Option 2	Choice 2	LED 1	Off	On	Off	Blink fast	Off	Off	Off
		LED 2	Off	Off	Off	Blink fast	On	Blink slow	Blink slow
Option 3	Choice 3	LED 1	Off	Blink slow	On	Blink fast	Blink fast	Blink fast	Blink fast
		LED 2	-	-	-	-	-	-	-

6.10 Configurable pins

The WCT1200 supports pin multiplexer, which means that one pin can be configured to different functions. If the default on-chip functions are not used in your applications, such as Touch Sensing ports, and ultra low power control, these pins can be configured for other functions. Table 12 lists the pin multiplexer for WCT1200 configurable pins.

Table 12 Configurable pins multiplexer

Pin No.	Default Function	Alternative Function
3	COIL1_EN	GPIO
4	COIL2_EN	GPIO
5	LED1	GPIO
15	GPIO	-
16	UART_RX	GPIO
17	UART_TX	GPIO

18	TOUCH_PAD1	GPIO
19	LED2	SCL
20	TOUCH_PAD2	SDA
23	TOUCH_PAD3	GPIO
24	COIL0_EN	GPIO
25	PUMP_PWM	GPIO
26	DRIVER_EN	GPIO

6.11 Unused pins

All unused pins can be left open unless otherwise indicated. For better system EMC performance, it is recommended that all unused pins are tied to system digital ground and flooded with copper to improve ground shielding.

6.12 Power-on reset

WCT1200 can handle the whole system power on sequence with integrated POR mechanism, so no more action and hardware is needed for the whole system powered on.

6.13 External reset

WCT1200 can be reset when the $\overline{\text{RESET}}$ pin is pull down to logic low (digital ground). A 4.7 kΩ pull-up resistor to 3.3 V digital power and a 0.1uF filter capacitor to digital ground are recommended for the reliable operation. This pin is used for the JTAG debug and programming purpose in this design.

6.14 Programming & Debug interface

One JTAG and one UART communication ports are designed for the communication with the PC. JTAG is used for the system debug, calibration, and programming. And UART is used for the communication with the PC to display the system information, such as input voltage, input current, coil current, and operating frequency. For the hardware design, see the system example design schematics.

6.15 Software module

The software in WCT1200 is matured and tested for production ready. Freescale provides a Wireless Charging Transmitter (WCT) software library for speeding user designs. In this library, low level drivers of HAL (Hardware Abstract Layer), callback functions for library access are open to user. About the software API and library details, see the *WCT1200 TX Library User Guide*.

6.15.1 Memory map

The WCT1200 has 32 Kbytes on-chip Flash memory and 6 Kbytes program/data RAM. Besides for wireless transmitter library code, the user can develop private functions and link it to library through predefined APIs.

Table 13 WCT1200 memory footprint (CodeWarrior V10.6, Code Size Optimization Level 4)

Memory	Total size	Example code size	Library size	FreeMASTER size	Free size
Flash	32 Kbytes	31.8 Kbytes	19 Kbytes	3.5 Kbytes	0.2 Kbytes
RAM	6 Kbytes	5.5 Kbytes	4.3 Kbytes	0.1 Kbytes	0.5 Kbytes

6.15.2 Software library

The WCT software library provides the complete wireless charging function which is compliant with the latest version WPC “Qi” specifications. This library includes the “Qi” communication protocol, power transfer control program, FOD algorithm using power loss method, system status indication module, and fault protection module. Figure 19 shows the complete software structure of this library. A data structure in the software library can be accessed by user code, which contains runtime data like input current, input voltage, coil current, PWM frequency and duty cycle. For the details of how to use this library, the API definitions, and the data structure, see the *WCT1200 TX Library User Guide*. Besides, a FreeMASTER calibration module is integrated into this library, which enables the end product customization and FOD calibration through the SCI port.

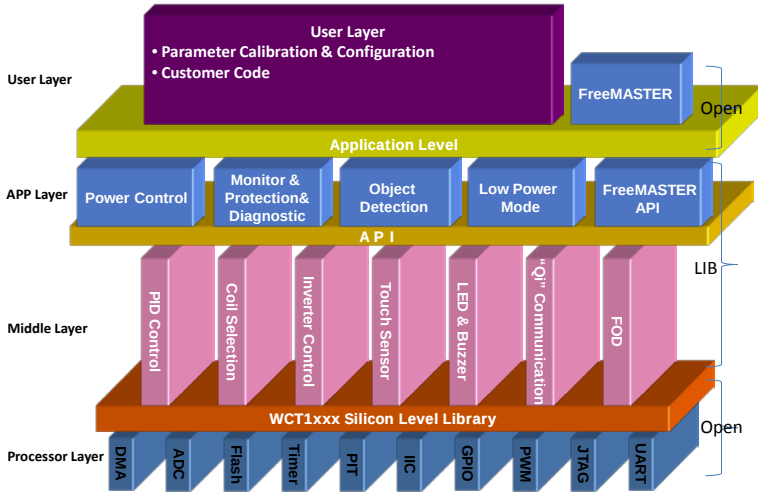

Figure 19 Software Structure of WCT Library

6.15.3 API description

Through WCT library APIs, the user can easily get the typical signals on TX system, such as the input voltage, input current, coil current, and PWM frequency. The user can conveniently know WCT1200

operational status by watching variables through the FreeMASTER GUI tool. For more information about API definitions, see *WCT1200 TX Library User Guide*.

6.16 Example design schematics

Please go to freescale website freescale.com and search “WCT1200” to find the schematic details and the A28 user guide.

6.17 Guideline to other solutions configuration

WCT1200 supports any free positioning multiple coils power transmitter solutions by using frequency and duty cycle control. Based on the example design schematics of Freescale wireless transmitter system with A28 configuration, you can easily develop other solutions according to the following guidelines from both hardware and software perspectives.

- For higher input voltage solutions (Such as A6, A14, A19, A21)
  1. Replace LDO (U1) with BUCK converter for 3.3V voltage generation from the input voltage.
  2. Change the full bridge power stage to half bridge power stage if half bridge topology is used.
  3. Use corresponding primary coils and resonant capacitor.
  4. Use new coil current calibration formula in the software. Adjust the coil current sensing circuits to make the “AC_COIL_CURRET” signal in the range of 0 V DC – 3.3 V DC, and change the mapping parameters in the software.
- For same input voltage solutions

  Replace the corresponding primary coils and resonant capacitor only.

7 Design Considerations

7.1 Electrical design considerations

Use the following list of considerations to assure correct operation of the device and system:

- The minimum bypass requirement is to place 0.01 – 0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the VDD/VSS pairs, including VDDA/VSSA. Ceramic and tantalum capacitors tend to provide better tolerances.
- Bypass the VDD and VSS with approximately 10 µF, plus the number of 0.1 µF ceramic capacitors.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the VDD and VSS circuits.
- Take special care to minimize noise levels on the VDDA, and VSSA pins.
- Using separate power planes for VDD and VDDA and separate ground planes for VSS and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with VDDA traces.
- If desired, connect an external RC circuit to the RESET pin. The resistor value should be in the range of 4.7 kΩ – 10 kΩ; and the capacitor value should be in the range of 0.1 µF – 4.7 µF.
- Add a 2.2 kΩ external pull-up on the TMS pin of the JTAG port to keep device in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input mode with internal weak pull-up.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF/10 Ω RC filter.
- Need some optional circuits for the power saving function, those circuit can be removed when the design is not sensitive for this requirements, so the touch sensor IC and AUXP_CTRL can be removed.
- The system with A28 coil can pass the EMI test with the qualified adaptor and without additional filter. The margin should be more than 6 dB, and the following design items should be considered:
    - The full bridge MOSFET driver resistor can be adjusted. For AOS7400A, the driver resistor is 27 Ω.

- The MOSFET Snubber circuit should be added to decrease the spike on the MOSFET during switching. At present, the Snubber circuit is a 4700 pF ceramic capacitor. This circuit is shown on the example schematic.
- A parallel 4.7 nF 50 V capacitor for the each coil is recommended to add, which will solve the additional unexpected resonance (disabled coil and some parasitical capacitors on the coil switch MOSFET) effect for the CE testing.

7.2 PCB layout considerations

- Provide a low-impedance path from the board power supply to each VDD pin on the device and from the board ground to each VSS pin.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip VDD and VSS pins are as short as possible.
- PCB trace lengths should be minimal for high-frequency signals.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- The decoupling capacitors of 0.1 μF must be placed on the VDD pins as close as possible, and place those ceramic capacitors on the same PCB layer with the WCT1200 device. VIA is not recommend between the VDD pins and decoupling capacitors.
- The WCT1200 bottom EP pad should be soldered to the ground plane, which will make the system more stable, and VIA matrix method can be used to connect this pad to the ground plane.
- As the wireless charging system functions as a switching-mode power supply, the power components layout is very important for the whole system power transfer efficiency and EMI performance. The power routing loop should be small and short as can as possible, especially for the resonant network, the traces of this circuit should be short and wide, and the current loop should be optimized smaller for the MOSFETs, resonant capacitor and primary coil. Another important thing is that the control circuit and power circuit should be separated.

7.3 Thermal design considerations

WCT1200 power consumption is not so critical, so there is not additional part needed for power dissipation. But the full-bridge inverter needs the additional PCB Cu copper to dissipate the heat, so good thermal package MOSFET is recommended to select, such as DFN package, and for the resonant capacitor, COG material, and 1206 or 1210 package are recommended to meet the thermal requirement. The transmitter system internal power loss is about 0.4 W with full 5 W loads, and the worst case is on the inverter, so the user should make some special action to dissipate those heat. Figure 20 shows one thermal strategy for the inverter.

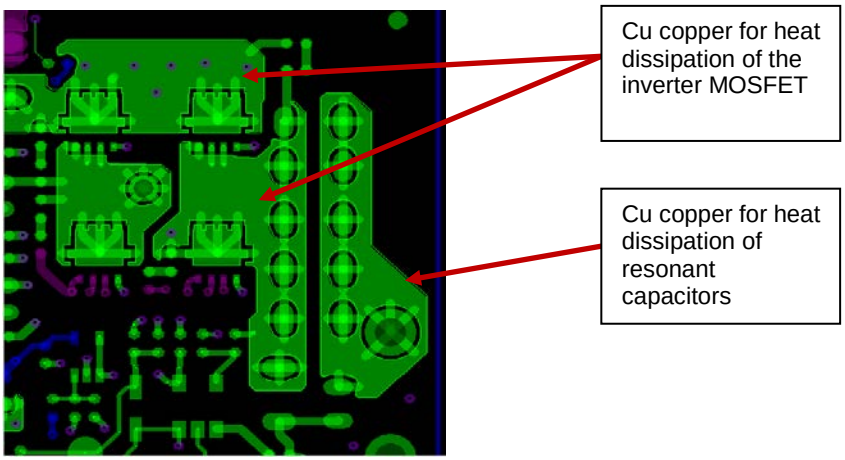

Figure 20 Thermal Design Strategy for Inverter

8 References and Links

8.1 References

- *WCT1200 A28 Reference Design System User Guide* (WCT1200SYSUG)
- *WCT1200 TX Library User Guide* (WCT1200LIBUG)
- *WCT Runtime Debug User Guide* (WCT1XXXRTDUG)
- *WCT1200 A28 Reference Design Calibration User Guide* (WCT1200CALUG)
- *WPC Low Power Wireless Transfer System Description*, Part 1: Interface Definition

8.2 Useful Links

- freescale.com
- freescale.com\wirelesscharging
- www.wirelesspowerconsortium.com
- www.powermatters.org

How to Reach Us:

Home Page:
freescale.com

Web Support:
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