NXQ1TXA1

Qi-standard conforming charger controller

Rev. 2 — 2 July 2015 Objective data sheet

1. General description

The NXQ1TXA1 is a state of the art digital control controller for Qi-standard conforming wireless charger base stations. The controller supports type A1 or A10 single coil base stations.

The NXQ1TXA1 offers wireless power transfer, WPC 1.1 - Qi low-power standard-compliant communication and safety functions including Foreign Object Detection (FOD), temperature monitoring and more. The controller supports the conventional WPC pinging mode during standby to identify potential receivers. The controller can also work with the trigger function of the NXP NTAG I^2C product. This feature enables wake up from a phone its NFC field while having zero power consumption of the charger during standby. The controller also offers a flexible User Interface (UI) with up to two LEDs and one buzzer for feedback and control.

Depending on the required charging pad area, coil configurations such as A1 (single coil with magnet) and A10 (single coil without magnet) are supported.

2. Features and benefits

- Qi conforming wireless charger controller and communication:
  - Integrated Foreign Object Detection (FOD)
  - Using frequency and duty cycle control
  - ASK demodulation
  - One NTC input for coil or surface temperature monitoring
- Two LED outputs for optical user feedback
- Buzzer output for acoustical user feedback
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep and power-down modes using tap to power on
- Tap to power on option in combination with NT3H1201 (NFC TAG)
- Temperature range −40 °C to +85 °C
- HVQFN33 package, 7 × 7 × 0.85 mm

3. Applications

- Wireless Power Consortium version 1.1 (Qi) conforming base station for charging of mobile devices

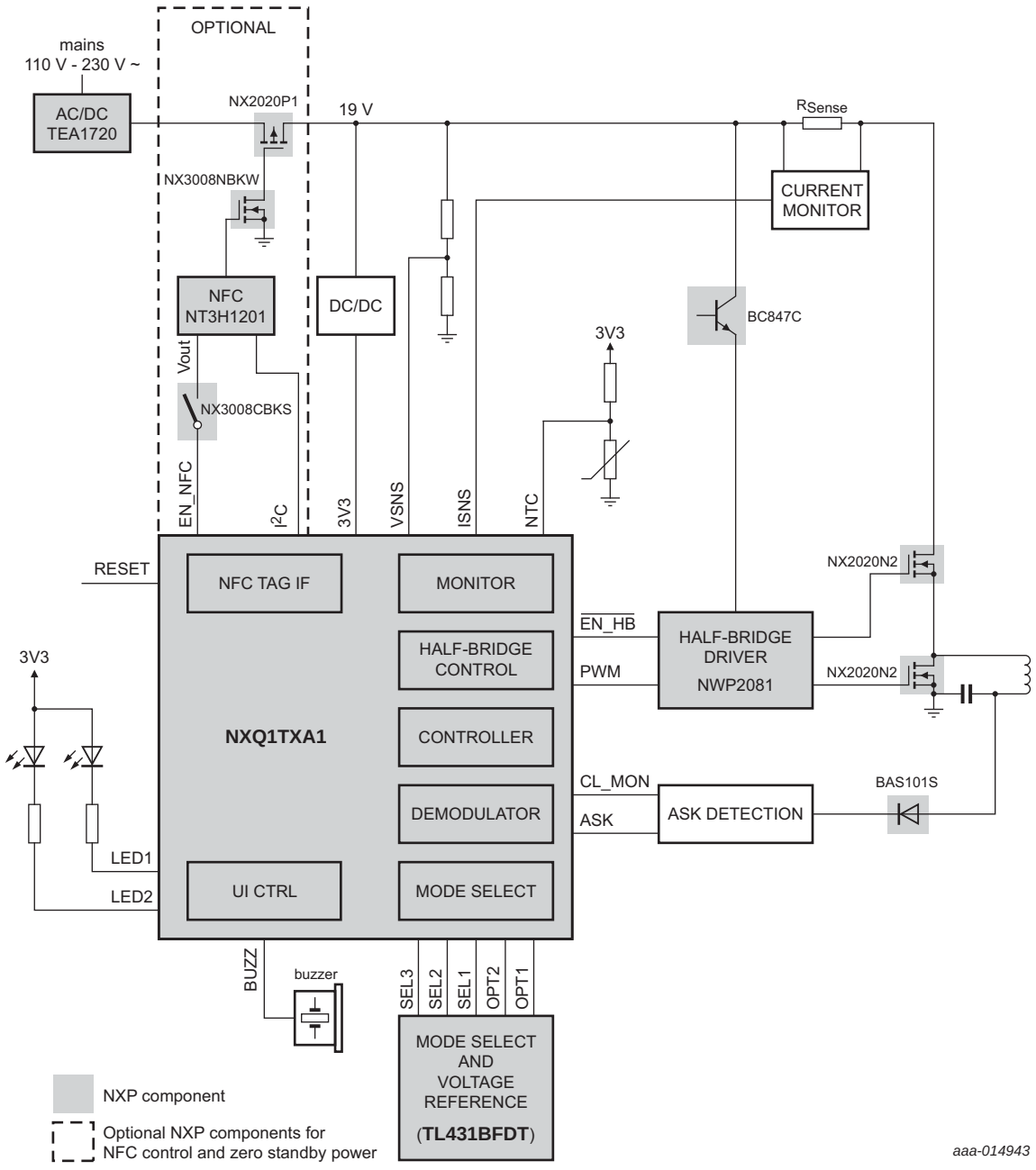
4. Ordering information

The NXP WPC/Qi charging transmitter application uses NXP and non-NXP components to offer an optimized system solution in terms of performance and cost.

Table 1. Ordering information

Type number	Package			
	Name	Description	Order information 12NC	Version
NXQ1TXA1/001	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	9353 039 25551	-

5. Block diagram



The block diagram does not depict all semiconductor components used to build the system. Refer to the related application note for details.

The NXQ1TXA1/001 supports A1 or A10 single coil chargers only.

Fig 1. NXQ1TXA1 based Qi compliant charger block diagram, A1/A10 (1-coil) design with NFC wake-up

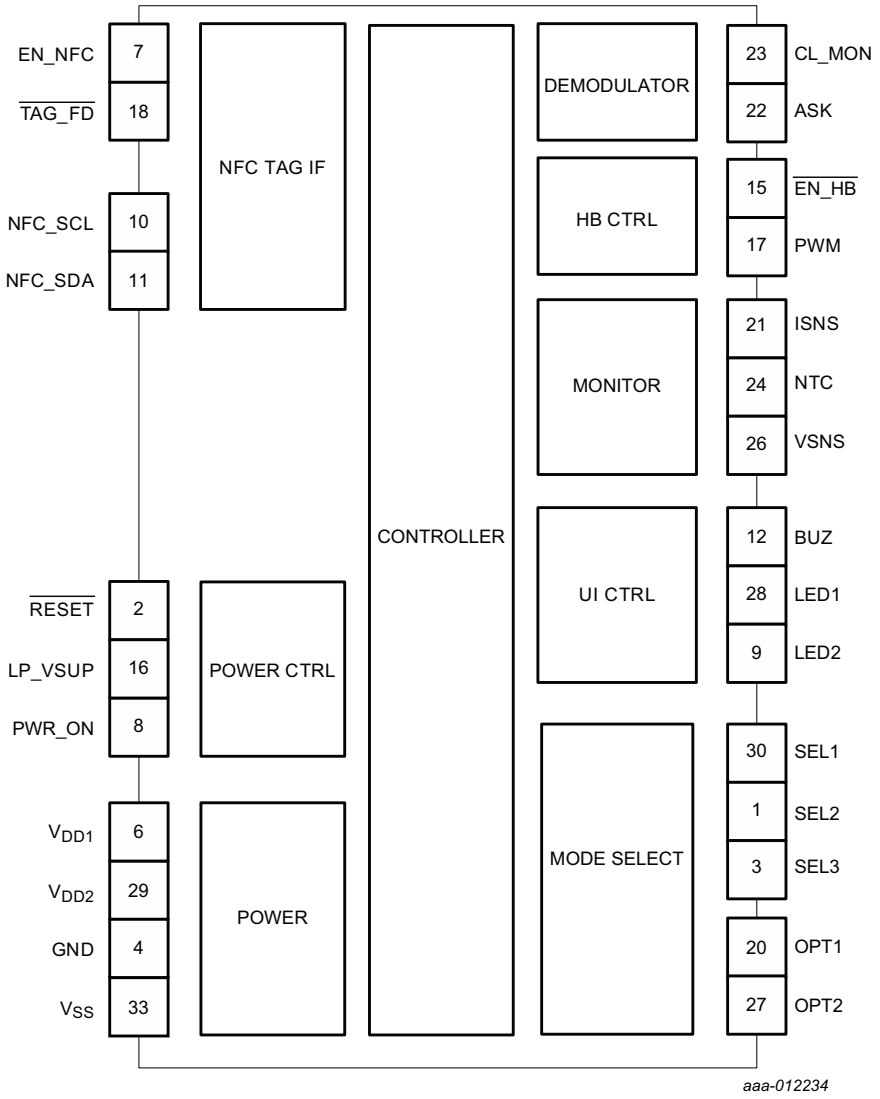


Fig 2. NXQ1TXA1/001 internal block diagram

6. Pinning information

6.1 Pinning

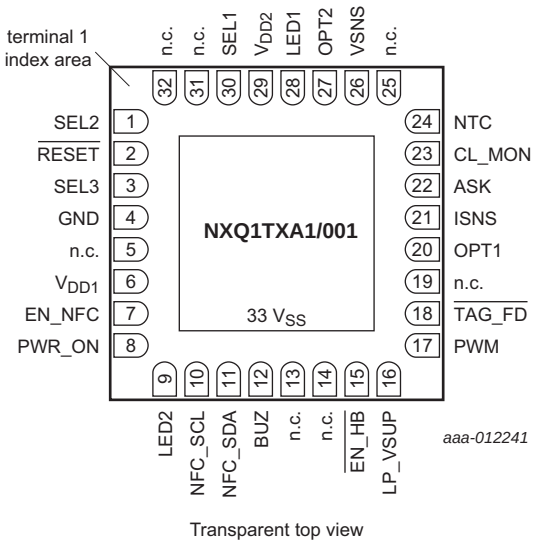


Fig 3. NXQ1TXA1 controller pin configuration HVQFN33 package

6.2 Pin description

Table 2. NXQ1TXA1 pin description table

Symbol	Pin	Description
$\overline{\text{RESET}}$	2	**$\overline{\text{RESET}}$ —** external reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device.
PWR_ON	8	**PWR_ON —** power on signal
NFC_SCL	10	**NFC_SCL —** NFC Tag I^2C-bus, open-drain clock input/output
NFC_SDA	11	**NFC_SDA —** NFC Tag I^2C-bus, open-drain data input/output
$\overline{\text{TAG\_FD}}$	18	**$\overline{\text{TAG\_FD}}$ —** field detect
EN_NFC	7	**EN_NFC —** NFC tag enable control output
$\overline{\text{EN\_HB}}$	15	**$\overline{\text{EN\_HB}}$ —** half-bridge enable control
LP_VSUP	16	**LP_VSUP —** switched low-power voltage supply
PWM	17	**PWM —** half-bridge PWM control
VSNS	26	**VSNS —** supply voltage monitor input
ISNS	21	**ISNS —** current sense monitor input. Power stage current measured over 22 mΩ with a gain of 100 V/V.
ASK	22	**ASK —** ASK demodulator signal input
CL_MON	23	**CL_MON —** coil voltage monitor
NTC	24	**NTC —** NTC input pin
OPT1	20	**OPT1 —** option select input 1
OPT2	27	**OPT2 —** option select input 2 and voltage reference input
SEL1	30	**SEL1 —** select 1 pin
SEL2	1	**SEL2 —** select 2 pin
SEL3	3	**SEL3 —** select 3 pin
LED1	28	**LED1 —** LED 1 open-drain pull-down pin
LED2	9	**LED2 —** LED 2 open-drain pull-down
BUZ	12	**BUZ —** Buzzer open-drain driver input/output pin
V_{DD}	6; 29	**V_{DD} —** 3.3 V supply voltage input
V_{SS}	33	**V_{SS} —** GND and thermal pad; connect to GND
GND	4	reserved - connect to GND
n.c.	5, 13, 14, 19, 25, 31, 32	**n.c. —** not connected; do NOT connect to GND

7. Functional description

7.1 Functional overview

The NXQ1TXA1 is a wireless charging controller for usage in a base station with a single primary coil. It is intended to create a type A1 or type A10 power transmitter as defined by the Qi low-power specification v.1.1.2 of the Wireless Power Consortium.

Figure 1 shows that using the NXQ1TXA1 IC in combination with a power stage, creates a magnetic coupled power transmitter. The power stage comprises a half-bridge driver (NWP2081T) and two MOSFETs (NX2020N2).

The charging controller takes care of all intelligence involved to create a wireless charging transmitter. It includes the control signals PWM and EN_HB to drive a power stage, and the analog inputs ASK and CL_MON for detection and communication. An optional NTC input is used for over temperature protection.

A separate current monitor is used to enable foreign object detection. A discrete envelope detector circuit is used to reconstruct the 2 kHz ASK communication waveform as used by Qi.

At start-up, the controller senses the OPTx inputs to determine the functionality of the connected LEDs and Buzzer. The SELx pins are driven to select the settings for Foreign Object Detection. The transmitter implements four phases, as defined by the Qi standard, for power transfer from a base station to a mobile device: selection, ping, identification and configuration, and power transfer. The transitions between these four phases are done according to the Qi specification.

7.2 Configuration options

The NXQ1TXA1 supports multiple modes of operation for the user interface, comprised of two LEDs and one Buzzer. It supports several blinking code variations for the LEDs in combination with buzzer tones. The voltage level at pin OPT1, sets the UI mode of operation at start-up. To set the level at the pin OPT1, a voltage divider can be used as depicted in Figure 4.

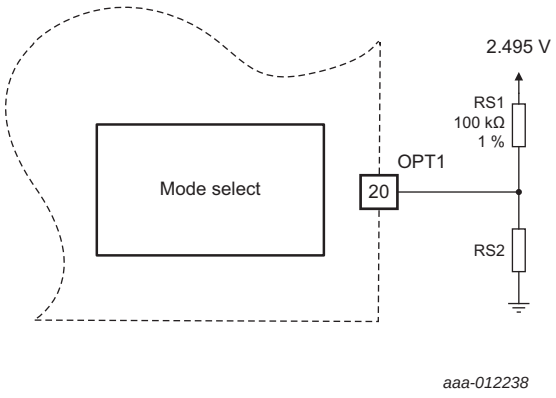


Fig 4. UI behavior mode/option selection

The various settings possible are summarized in Table 3

Table 3. UI behavior selection

RS1 (kΩ, 1 %)	RS2 (kΩ, 1 %)	Mode number	LED	Standby	Charging	Charge complete	FOD	Temp. error	Receiver indicator error
100.0	6.7	1	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	14.3	2	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	23.2	3	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	33.2	4	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	45.3	5	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	60.4	6	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	78.7	7	reserved	reserved	reserved	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved
100.0	100.0	8	LED1	Off	Off	Off	3 Hz blink	3 Hz blink	3 Hz blink
			LED2	Off	1 Hz blink	On	Off	Off	Off
100.0	n.c.	16	LED1	Off	Off	Off	Off	Off	Off
			LED2	Off	On	Off	3 Hz blink	3 Hz blink	3 Hz blink

7.3 Safety features

The NXQ1TXA1 contains three different safety functions to protect the user, the charger itself and also the mobile device to be charged.

The foreign object detection regularly evaluates whether significant amounts of power are absorbed by devices not related to the power receiver used for charging. Thermal protection is used to monitor the base station and the coil temperature. Additionally, if the receiver indicates an error condition or an end-of-charge, the controller stops the power transfer.

7.3.1 Foreign Object Detection

The Foreign Object Detection (FOD) implemented in the NXQ1TXA1 regularly compares the base station input power with the mobile side received power packet information. It calculates additional losses to foreign objects that are not accounted for in the transmitter or receiver. Once the power transfer is stopped due to a foreign object being detected, the base station waits until the receiver is removed.

When the mobile device is placed back on the power transmitter unit, the NXQ1TXA1 resumes normal operation. In case the power consuming foreign object is still present (or e.g. a mobile device is malfunctioning), the procedure is executed again. RS4 sets the FOD threshold.

The OPT2 input is being multiplexed and a voltage divider as depicted in Figure 5 can be used.

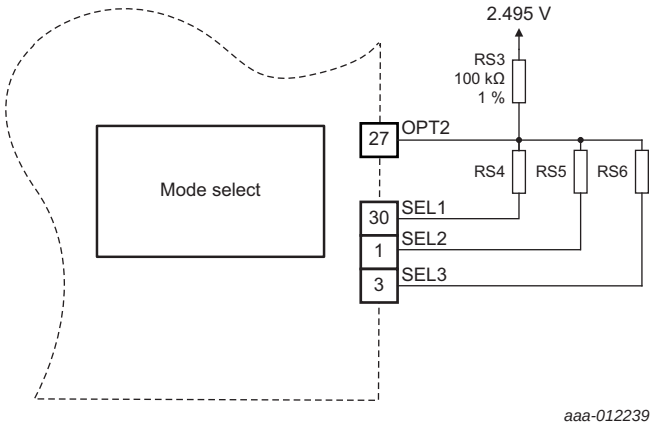


Fig 5. FOD threshold selection

The resistors RS3 and RS4 are used with the SEL1 signal to determine the FOD threshold. The resistor settings are as in Table 4.

Table 4. FOD level selection

RS3 (kΩ, 1 %)	RS4 (kΩ, 1 %)	Foreign Object Detection threshold (mW)
100.0	0	100
100.0	6.7	150
100.0	14.3	200
100.0	23.2	250
100.0	33.2	300
100.0	45.3	350
100.0	60.4	400
100.0	78.7	450
100.0	100.0	500
100.0	127.0	550
100.0	165.0	600
100.0	221.0	650
100.0	301.0	700
100.0	432.0	750
100.0	698.0	800
100.0	1500.0	850
100.0	n.c.	disabled

For FOD accuracy, a voltage of 2.495 V accurate to 0.5 % or better, must be present at the OPT2 input line when the SEL1, SEL2 and SEL3 outputs are high impedance. Resistors RS5 and RS6 are used to set the operational parameters for foreign object detection.

7.3.2 Thermal protection

The voltage at pin NTC is sensed to enable the over-temperature protection. If the voltage at pin NTC drops below the high temperature threshold value, the transmitter stops the power transfer phase. It resumes when the NTC pin voltage is above the low temperature threshold value. When the transmitter resumes, it starts with the Qi selection phase again. The voltage to pin NTC can be created as shown in Figure 6.

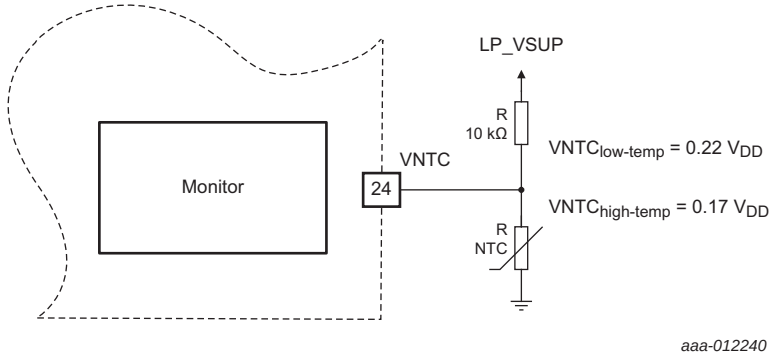


Fig 6. NTC biasing and connection

7.3.3 Receiver end power transfer

If the active Qi receiver signals a valid end of power transfer packet, the transmitter responds according to Table 5.

Table 5. End of power transfer packet value

Reason	Value	base station response
Unknown	0x00	enters selection phase
Charge Complete	0x01	stop power transfer
Internal Fault	0x02	stop power transfer and waits for device removal
Over Temperature	0x03	stop power transfer and waits for device removal
Over Voltage	0x04	enters selection phase
Over Current	0x05	enters selection phase
Battery Failure	0x06	stop power transfer and waits for device removal
Reconfigure	0x07	enters identification phase
No Response	0x08	enters selection phase
Reserved	0x09 ... 0xFF	stop power transfer and waits for device removal

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present [2]	–0.5	+5.5	V
		5 V tolerant open-drain pins [2][3]	–0.5	+5.5	V
V_{IA}	analog input voltage	pins ISNS, VSNS, NTC, ASK, CL_MON, OPTx [2]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground current	per ground pin	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature	non-operating [4]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	150	°C
P_{tot}	total power dissipation	per package based on package heat transfer, not device power consumption	-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins [5]	-	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are concerning V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[4] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Refer to the JEDEC specification (J-STD-033B.1) for further details.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C)
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible.

Table 7. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 8. NXQ1TXA1 Thermal resistance value (C/W): ±15 %

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.

HVQFN33	
θ_{j-a}	
JEDEC (4.5 in × 4 in)	
0 m/s	40.4
1 m/s	32.7
2.5 m/s	28.3
Single-layer (4.5 in × 3 in)	
0 m/s	84.8
1 m/s	61.6
2.5 m/s	53.1
θ_{j-c}	20.3
θ_{j-b}	1.1

10. Static characteristics

Table 9. Static characteristics

3.0 V ≤ V_{DD} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)		3.0	3.3	3.6	V
I_{DD}	supply current	Active mode; average current drawn by controller during power transfer excluding output driving currents (LP_VSUP)	-	14	-	mA
		Standby mode; average pinging current during standby	-	5	-	mA
All pins except VNTC, LP_VSUP, SCL, SDA						
I_{IL}	LOW-level input current	V_I = 0 V	-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$	-	0.5	10	nA
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [3]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [3]	-	-	50	mA
VNTC (pin 24)						
V_{sw}	switch voltage	NTC low temperature	-	$0.22V_{DD}$	-	V
		NTC high temperature	-	$0.17V_{DD}$	-	V
LP_VSUP (pin 16)						
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$;	-	0.5	10	nA
V_O	output voltage	output active	0	-	V_{DD}	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [3]	-	-	50	mA
NFC_I²C-bus pins (pin 10, pin 11)						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V

Table 9. Static characteristics *...continued*

3.0 V ≤ V_{DD} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; *unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{hys}	hysteresis voltage		-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3.5	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ [4]	-	2	4	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[4] To V_{SS}.

11. Dynamic characteristics

11.1 Power-up ramp conditions

Table 10. Power-up characteristics

3.0 V ≤ V_{DD} ≤ 3.6 V; T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 400 mV [1]	0	-	500	ms
t_{wait}	wait time	[1] [2]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	0	-	400	mV

[1] See Figure 7.

[2] The wait time specifies the time the power supply levels must be at below 400 mV before ramping up.

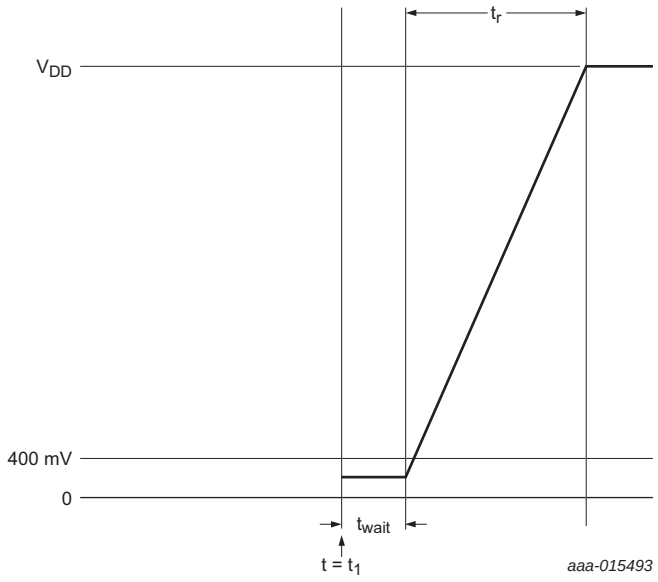


Fig 7. Power-up ramp

11.2 Output pins

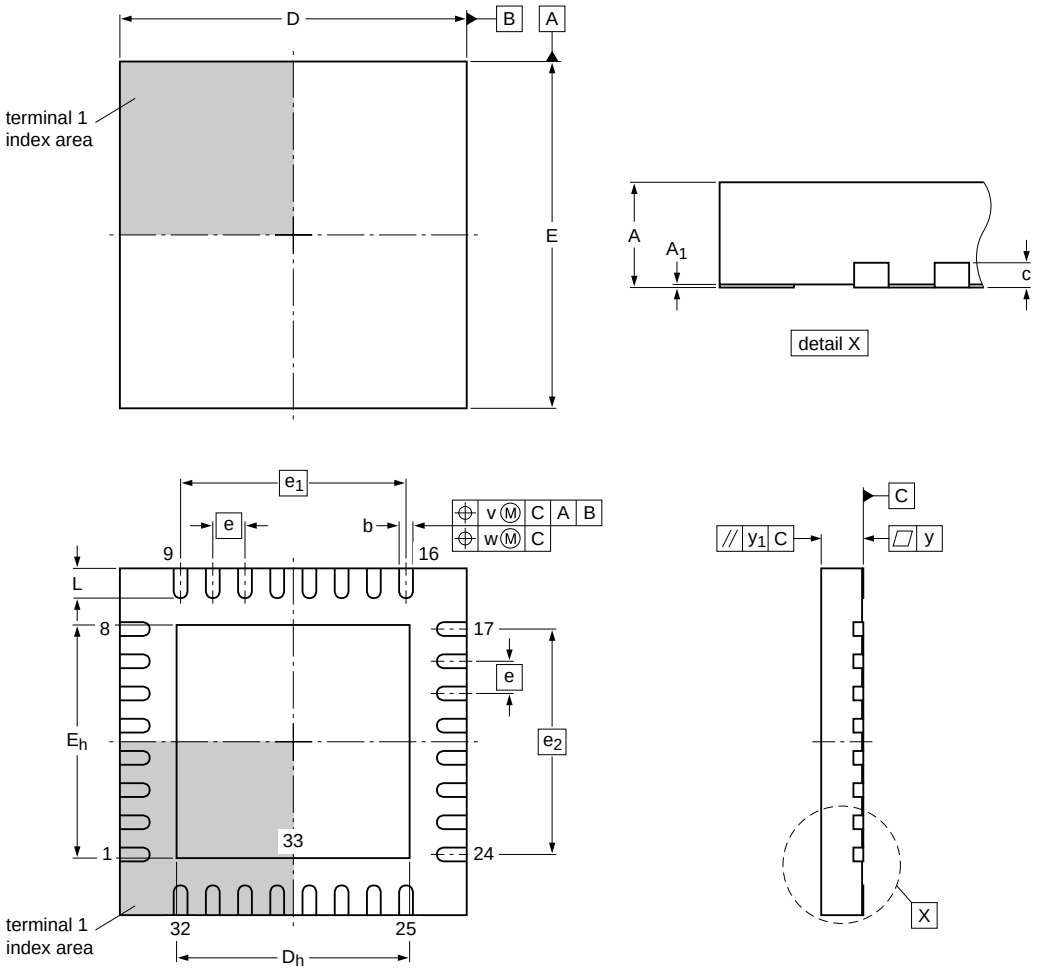
Table 11. Output pins

3.0 V ≤ V_{DD} ≤ 3.6 V; *T_{amb} = −40 °C to +105 °C.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		- - -				~~09-03-17~~ 09-03-23

Fig 8. Package outline HVQFN33

13. Soldering

Footprint information for reflow soldering of HVQFN33 package

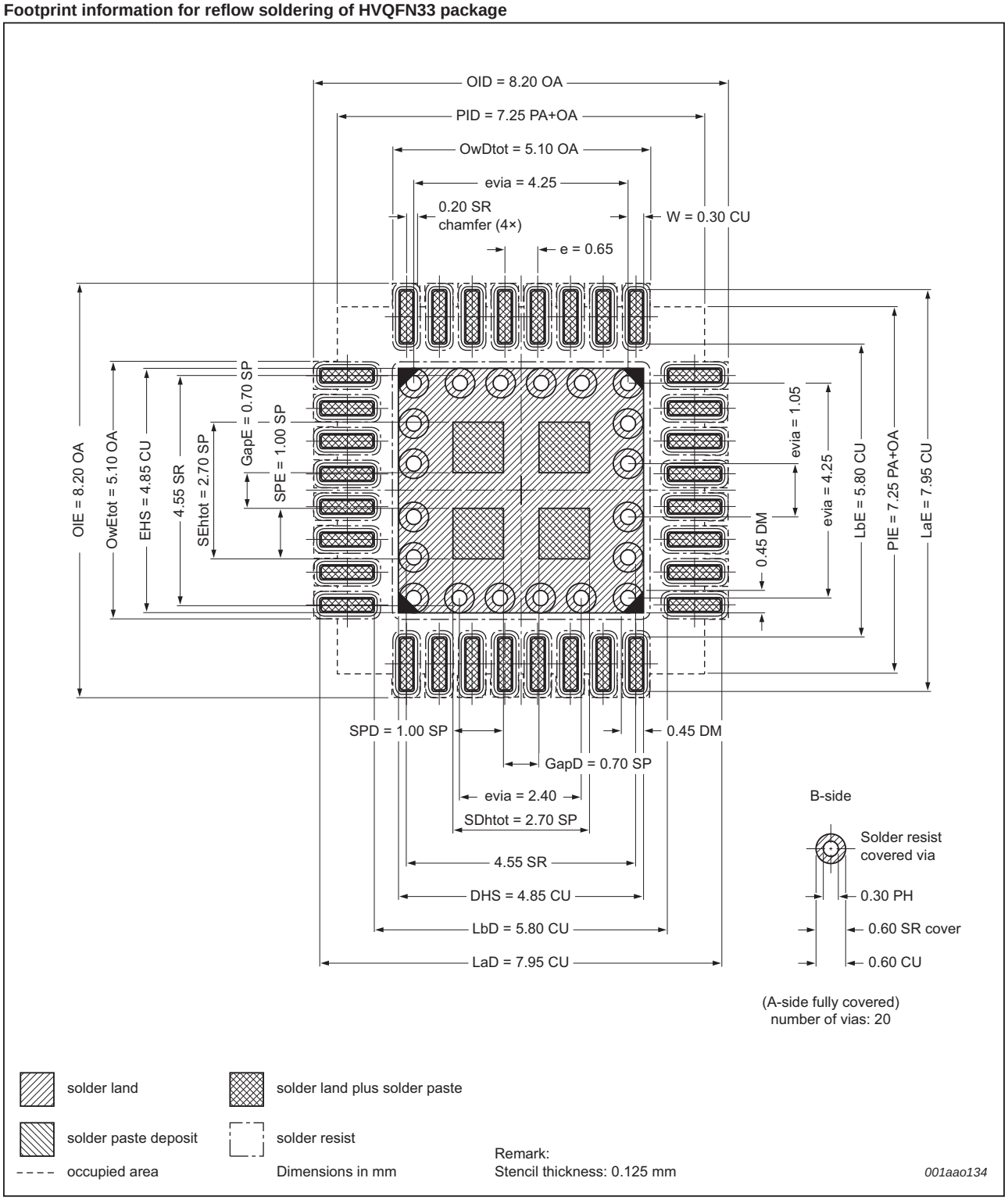


Fig 9. Reflow soldering of the HVQFN33 package

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASK	Amplitude Shift Keying
FOD	Foreign Object Detection
RC	Resistor-Capacitor
WPC	Wireless Power Consortium
HB	Half Bridge
NFC	Near Field Communication
PWM	Pulse Width Modulation
OTP	OverTemperature Protection
NTC	Negative Temperature Coefficient (Thermistor)

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXQ1TXA1 v.2	20150702	Objective data sheet	-	NXQ1TXA1 v.1
Modifications:	• Characteristic values updated • Table 6, “WPC1.0 receiver power threshold” removed • Data sheet reverted to Objective status			
NXQ1TXA1 v.1	20140313	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

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17. Contact information

For more information, please visit: **http://www.nxp.com**

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