PM823

Dual Synchronous 1.5A/1.5A Step-down Buck Regulators with 525 mA LDO

Rev. 4 — 23 June 2022

Product data sheet
PUBLIC

1 Product overview

The PM823 is an efficient low-cost power regulator. It consists of two 1.5 A buck regulators and one 525 mA LDO. The LDO can be powered by the buck converter output (≥1.6 V) to minimize the power loss and simplify the system thermal de-sign.

The PM823 is optimized for module applications. It minimizes the PCB footprint and BOM cost. The PM823 12-bump WLCSP package provides the smallest footprint for the state-of-the-art module applications. For general purpose applications, the 24-pin QFN package can meet the low-cost PCB requirements. The QFN package also provides additional functions such as power good outputs.

The PM823 Dynamic Voltage Scaling (DVS) feature supports the latest SoC and processor power control scheme. The PM823 also supports Adaptive Voltage Scaling (AVS). The serial interface can be used to program the device to meet different application requirements.

Features

- Supports 2.7 V~5.5 V operating voltage
- Two 1.5 A synchronous buck converters
- Single LDO supports up to 525 mA
- Ultra low 15 µA sleep current
- 3 MHz switching frequency
- High output voltage accuracy
- Supports both DVS and AVS
- Single wire proprietary serial interface

Package options

- WLCSP-12 lead (0.35 mm ball pitch)
- QFN-24 lead (0.5 mm pin pitch)

Applications

- IoT devices
- Wi-Fi modules
- Smart home devices
- Cameras, printers
- Smart appliances
- Wi-Fi hubs, Access Points (APs)
- Set top boxes

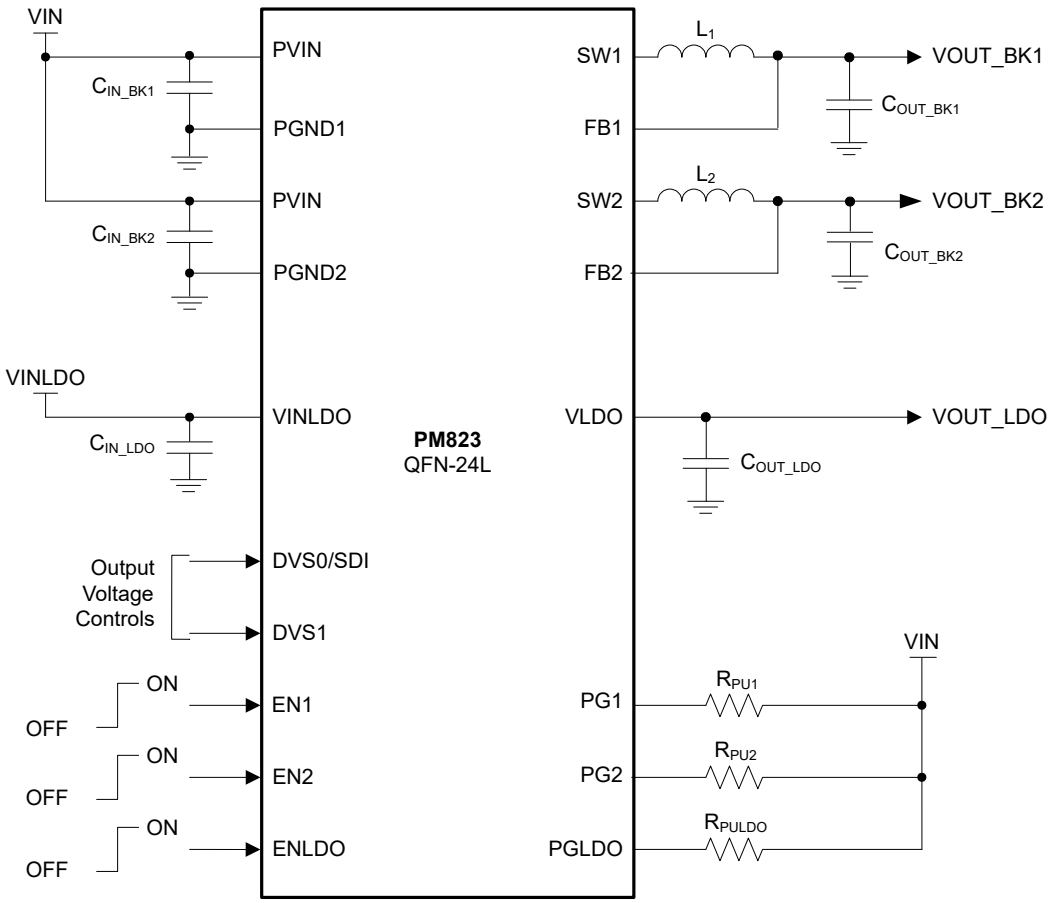

Figure 1. PM823 typical application-QFN package option

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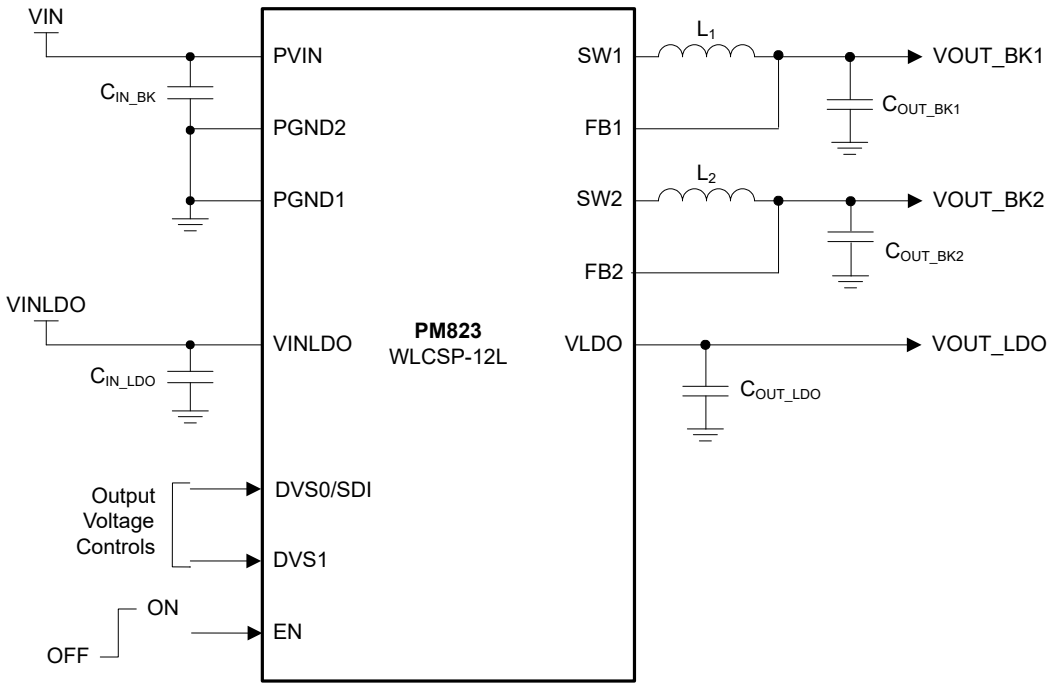

Figure 2. PM823 typical application-WLCSP package option

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2 Ordering information

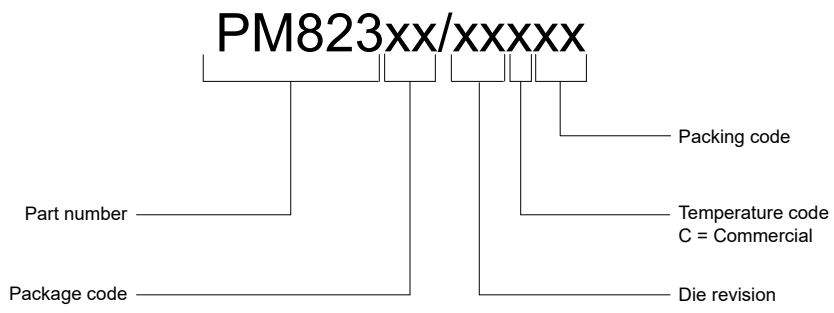

Figure 3. Part numbering scheme

The standard ordering part numbers for the respective solutions are the following:

Table 1. Part order options

Part order number	Buck1 output voltage	Buck2 output voltage	LDO output voltage	Package type
PM823UK/A0CZ (Tape and Reel)	1.1V	2.2V	1.8V	12-pad WLCSP
PM823HN/A0CHP (Tape and Reel)	1.1V	2.2V	1.8V	24-pin QFN

Note: *Based on Marvell's 88PG823 RMA history, no RMA will be accepted except manufacturing defects. Device provided AS-IS and support limited to NXP Wi-Fi/ Bluetooth system related questions.*

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3 Signal description

3.1 Pin configuration

3.1.1 12-lead WLCSP configuration

Figure 4 shows PM823 12-lead WLCSP configuration diagram.

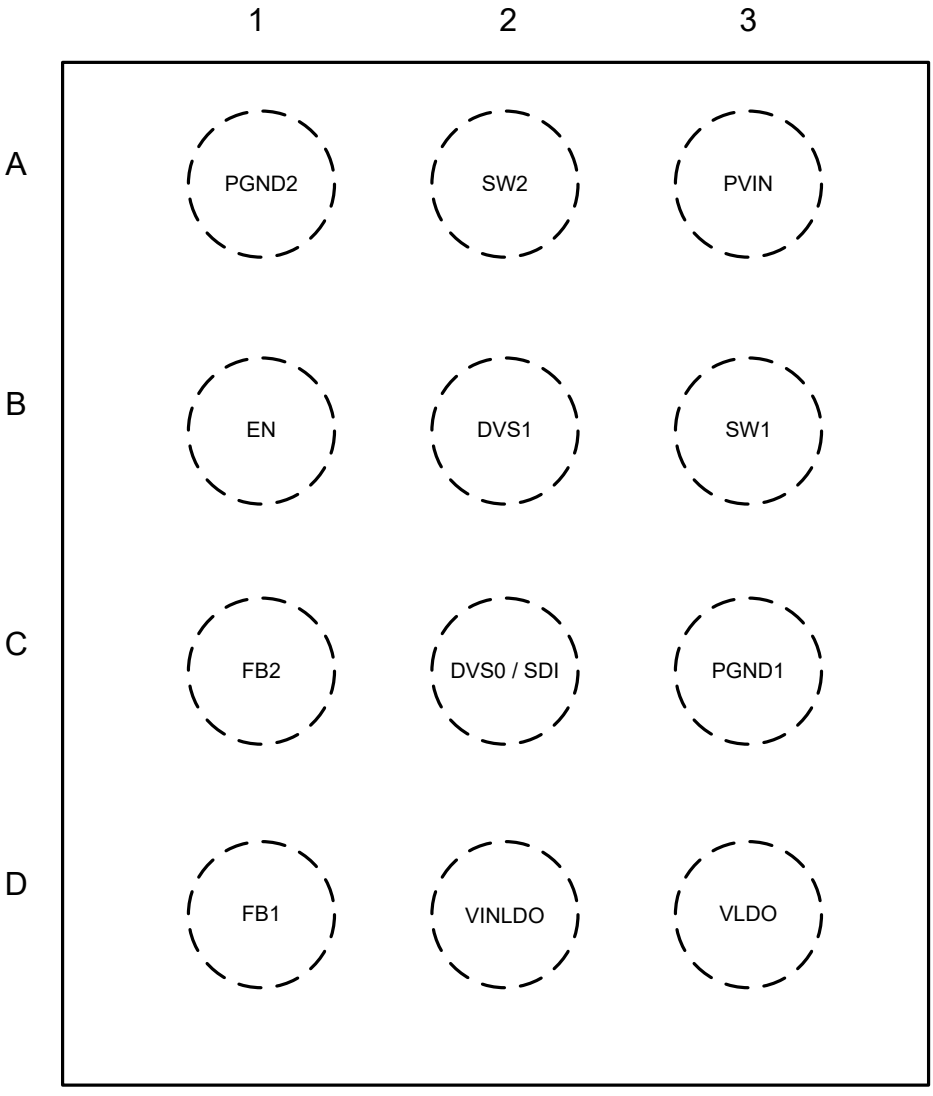

Figure 4. 1.26 mm x 1.545 mm WLCSP-12 lead, pop (see through) view

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3.1.2 24-pin QFN configuration

Figure 5 shows PM823 24-pin QFN configuration diagram.

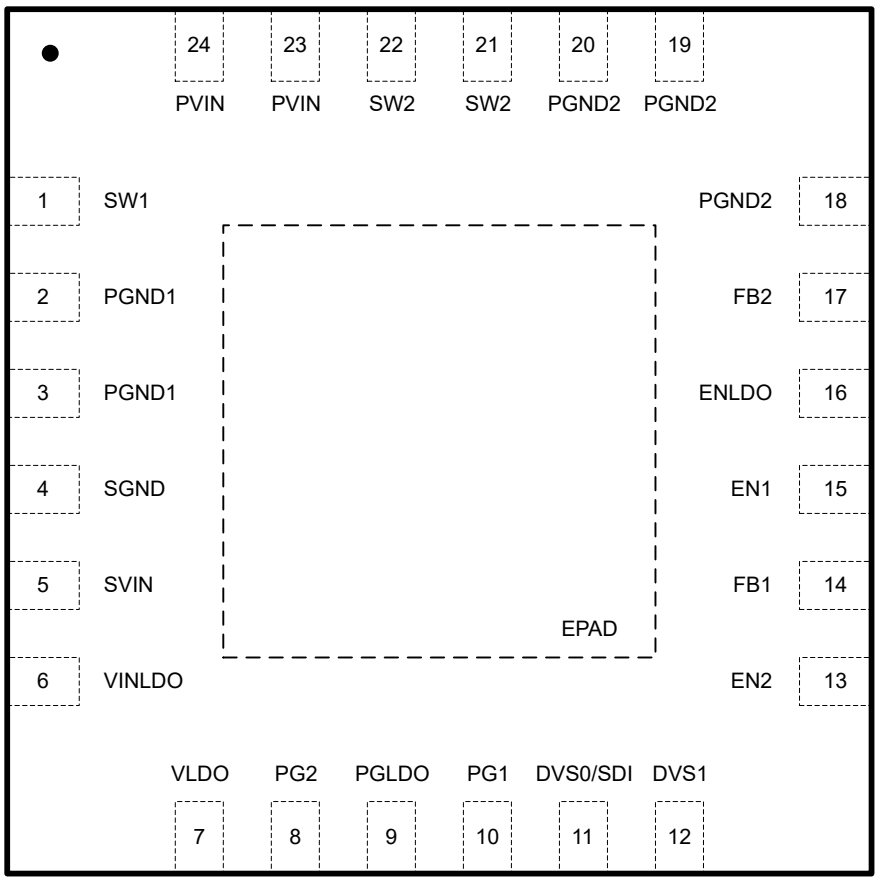

Figure 5. 4 mm x 4 mm QFN-24 in 0.5 mm pitch pin configuration, top (see through) view

3.2 Pin descriptions

Table 3 shows the pin description details for PM823.

Table 2. Pin types

Pin type	Description
I	Input
I/O	Input / Output
GND	Ground
NC	No Connection
S	Supply
O	Output

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Table 3. Pin description

Pin number		Pin name	Pin type	Function
WLCSP	QFN			
A1	18, 19, 20	PGND2	GND	Power ground for Buck2 regulator • It must be connected to the negative terminals of the input and output capacitors • All PGND pins must be connected to SGND, EPAD, and make a star connection to system ground • **Do not float any PGND pin**
A2	21, 22	SW2	O	Switch node for Buck2 regulator • Internally connected to the drains of the high side and low side MOSFETs • Connect to the external inductor • When the switching regulator is disabled, the SW node is high impedance • If step-down regulator 2 is not in use, float this pin
A3	23, 24	PVIN	S	Switching regulator power input • Power input voltage. Internally connected to the source of the high side MOSFET • Connect a ceramic input capacitor or an equivalent low ESR input capacitor between PVIN and PGND. Place it as close as possible to PVIN and PGND pins. See Section 8 "Application information". • The voltage between SVIN and PVIN should be equal to 50mV or less • All PVIN pins must be connected to the same voltage source • **Do not float any PVIN pin**
B1	N/A	EN	I	Enable Input for all regulators • Logic high enables regulators and logic low disables regulators • See Section 4 "Electrical specifications" for detailed logic high and logic low specifications • When not in use, connect this pin to GND or connect a 0Ω resistor to GND • **Do not float this pin**
B2	12	DVS1	I	Dynamic voltage scaling control 1 • This digital input is used to select one of the three operating modes. See Section 5.6 "Operating modes" output voltage settings for mode selection. • **Do not float this pin**
B3	1	SW1	O	Switch node for buck1 regulator • Internally connected to the drains of the high side and low side MOSFETs • Connect to the external inductor • When the switching regulator is disabled, the SW node is high impedance • If Step-down Regulator 1 is not in use, float this pin
C1	17	FB2	I	Buck2 regulator output voltage sense feedback • Connect this pin to the output capacitor • This pin senses the output voltage of the switching regulator • **Do not float this pin**

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Table 3. Pin description...*continued*

Pin number		Pin name	Pin type	Function
WLCSP	QFN			
C2	11	DVS0/SDI	I	Dynamic voltage scaling control 0 / serial data input • This digital input pin has two functions • If DVS1=0, this pin is used as DVS0 input • If DVS1=1, this pin becomes the one wire serial interface input • Input data into this pin is used to program the output voltage (see Section 5.2 "Serial interface (1-wire)") • When not in use, connect this pin to GND or connect a 0Ω resistor to GND • See Section 5.7 "DVS output voltage settings" for mode selection • **Do not share this pin with other serial interface pins** **Do not float this pin**
C3	2, 3	PGND1	GND	Power ground for Buck1 regulator • This pin must be connected to the negative terminals of the input and output capacitors • All PGND pins must be connected to SGND, EPAD, and make a star connection to system ground • **Do not float this pin**
D1	14	FB1	I	Buck1 regulator output voltage sense feedback • Connect this pin to the output capacitor • This pin senses the output voltage of the switching regulator • **Do not float this pin**
D2	6	VIN-LDO	S	LDO power supply • This is the power supply input for the LDO Regulator • Connect a ceramic input capacitor or an equivalent low ESR input capacitor between this pin and the ground plane. Place it as close as possible to this pin and the ground plane. See Section 8 "Application information".
D3	7	VLDO	O	LDO output • This pin is the output of the LDO • Connect a ceramic output capacitor or an equivalent low ESR output capacitor between this pin and the ground plane. Place it as close as possible to this pin and the ground plane. See Section 8 "Application information".
N/A	4	SGND	GND	Signal ground • This pin must be connected to SGND, all PGNDx pins, and make a star connection to system ground • **Do not float this pin**
N/A	5	SVIN	S	Signal input voltage • This is the input voltage pin to the internal circuitry. See Section 4.4 "Electrical characteristics " for input voltage range. • Connect a decoupling ceramic capacitor or an equivalent low ESR decoupling capacitor between SVIN and SGND and position it as close as possible to the IC. See Section 8 "Application information". • The voltage between SVIN and PVIN should be equal to 50mV or less • **Do not float this pin**

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Table 3. Pin description...*continued*

Pin number		Pin name	Pin type	Function
WLCSP	QFN			
N/A	8	PG2	O	Buck2 regulator power good output • This pin is an open-drain output • Connect a 100kΩ pull-up resistor from this pin to VOUT or a logic rail that is equal to or less than SVIN • The PG is held low when the output voltage is outside its regulation band and goes high after the output voltage is within regulation • When not in use, float this pin • **In shutdown, the PG will be actively low**
N/A	9	PGLDO	O	LDO power good • This pin is an open-drain output • Connect a 100kΩ pull-up resistor from this pin to VOUT or a logic rail that is equal to or less than SVIN • The PG is held low when the output voltage is outside its regulation band and goes high after the output voltage is within regulation • When not in use, float this pin • **In shutdown, the PG will be actively low**
N/A	10	PG1	O	Buck1 regulator power good output • This pin is an open-drain output • Connect a 100kΩ pull-up resistor from this pin to VOUT or a logic rail that is equal to or less than SVIN • The PG is held low when the output voltage is outside its regulation band and goes high after the output voltage is within regulation • When not in use, float this pin • **In shutdown, the PG will be actively low**
N/A	13	EN2	I	Buck2 enable input • See Section 5.4 "Power-up sequence" to determine which part numbers have power sequences versus those that do not • For part numbers with a power sequence in the QFN-24 package, EN1, EN2, and ENLDO pins need to be connected together. Any logic high from EN1, EN2, and ENLDO pins enables all regulators. EN1, EN2, and ENLDO need to have logic low to disable all regulators. User can not individually enable or disable each step-down regulator for parts with a power sequence • For part numbers without a power sequence, logic high for this pin enables Step-down Regulator 2. Logic low for this pin disables Step-down Regulator 2 • When not in use, connect this pin to GND or connect a 0Ω resistor to ground • **Do not float this pin**

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Table 3. Pin description...*continued*

Pin number		Pin name	Pin type	Function
WLCSP	QFN			
N/A	15	EN1	I	Buck1 enable input • See Section 5.4 "Power-up sequence" to determine which part numbers have power sequences versus those that do not • For part numbers with a power sequence in the QFN-24 package, EN1, EN2, and ENLDO pins need to be connected together. Any logic high from EN1, EN2, and ENLDO pins enables all regulators. EN1, EN2, and ENLDO need to have logic low to disable all regulators. User can not individually enable or disable each step-down regulator for parts with a power sequence • For part numbers without a power sequence, logic high for this pin enables Step-down Regulator 1. Logic low for this pin disables Step-down Regulator 1 • When not in use, connect this pin to GND or connect a 0Ω resistor to ground • **Do not float this pin**
N/A	16	ENLDO	I	LDO enable input • See Section 5.4 "Power-up sequence" to determine which part numbers have power sequences versus those that do not • For part numbers with a power sequence in the QFN-24 package, EN1, EN2, and ENLDO pins need to be connected together. Any logic high from EN1, EN2, and ENLDO pins enables all regulators. EN1, EN2, and ENLDO need to have logic low to disable all regulators. User can not individually enable or disable each step-down regulator for parts with a power sequence • For part numbers without a power sequence, logic high for this pin enables the LDO Regulator. Logic low for this pin disables the LDO Regulator • When not in use, connect this pin to GND or connect a 0Ω resistor to ground • The voltage on this pin must never be higher than the voltage on the SVIN pin + 0.3V for all conditions • **Do not float this pin**
N/A	25	EPAD	GND	Exposed thermal pad • This pin must be connected to SGND, all PGND pins, and make a star connection to system ground. See Section 8 "Application information". • **Do not float this pin**

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4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings[1]

Parameter	Range	Unit
V_{SVIN} to SGND	-0.3 to +6.0	V
S_{VIN}	V_{PVINx} -0.3 to V_{PVINx} +0.3	V
V_{PVINx} to PGNDx	-0.3 to +6.0	V
V_{SWx} to PGNDx[2]	-0.3 to (V_{PVINx} +0.3)	V
SGND to PGNDx	-0.3 to +0.3	V
V_{EN}, V_{EN_LDO}, V_{EN1}, V_{EN2}	-0.3 to (V_{SVIN} +0.3)	V
$V_{DVS0/SDI}$, V_{DVS1}	-0.3 to +6.0	V
Maximum junction temperature	150	°C
Storage temperature range	-65 to 150	°C

[1] Exceeding the absolute maximum rating may damage the device.
[2] SWx is capable of sustaining -1.0V for less than 50 ns.

4.2 Recommended operating conditions

Table 5. Recommended operating conditions[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{PVIN}	Buck input power voltage	2.7		5.5	V
V_{INLDO}	LDO input power voltage	1.6		5.5	V
T_{JMAX}	Maximum operating junction temperature			125	°C
Θ_{JA}	Package thermal resistance (WLCSP-22L)		40		°C/W
Θ_{JA}	Package thermal resistance (QFN-24L)		50		°C/W
T_A	Operating ambient temperature range	-40		85	°C

[1] Specifications over the –40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.

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4.3 External passive components

Table 6. External passive components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN1_BK} (WLCSP), C_{IN1_BK1}, C_{IN1_BK2},	External components	The distance between this capacitor to PVINx and PGNDx must be less than 1 mm. The maximum case size is 0201 (0603 metric). Use capacitor with ±30% tolerance or better.	0.10	0.22		µF
C_{IN2_BK}		WLCSP package: Use capacitor with ±30% tolerance or better.	2 x 10			µF
C_{IN2_BK1}, C_{IN2_BK2}		QFN package: Use capacitor with ±30% tolerance or better.	10			µF
C_{OUT_BK1}, C_{OUT_BK2}		Use capacitor with ±30% tolerance or better.	22			µF
L_{BK1}, L_{BK2}		Use capacitor with ±30% tolerance or better.		1.0		µH
LC_{BK1}, LC_{BK2}		The nominal L_{BUCKx} x the TOTAL nominal C_{OUT_BUCKx} must not exceed this maximum specification. Use inductor and capacitor with ±30% tolerance or better.			60	µH x µF
C_{IN_LDO}		Use capacitor with ±30% tolerance or better.	10			µF
C_{OUT_LDO}			4.7		20	

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4.4 Electrical characteristics

Table 7. Electrical characteristics

The following applies unless otherwise noted: Refer to the schematics shown in Section 8.2 "PCB schematics". V_{IN} = 3.6V, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply current						
I_{Q_MODE1} / I_{Q_MODE2}	Active modes quiescent current	Active Mode 1 and Mode 2: Buck1 and Buck2 are in PFM mode and LDO is on. V_{IN}=5V. No load.		170		µA
		Active mode 1 and mode 2: Buck1 and Buck2 are in PWM mode and LDO is on. V_{IN}=5V. No load.		20		mA
I_{Q_MODE3}		Active mode 3: Buck1 and Buck2 are in PFM mode and LDO is on. V_{IN} = 5V. No load.		75		µA
		Active mode 3: Buck1 and Buck2 are in PWM mode and LDO is on. V_{IN} = 5V. No load.		20		mA
I_{Q_SLP}	Sleep mode quiescent current	V_{DVS0} = V_{DVS1} = 0V. V_{IN} = 5V. No load.		15		µA
I_{SHDN}	Shutdown current	V_{ENx} = 0V. V_{IN} = 5V		1		µA
Buck1 and Buck2						
V_{PVIN}	Power supply input		2.7		5.5	V
I_{OUT_BK1} / I_{OUT_BK2}	Maximum output current in full power mode		1.5	--	--	A
$I_{OUT_BK1_SLP}$ / $I_{OUT_BK2_SLP}$	Maximum output current in sleep mode	--	10	--	--	mA
V_{OUT_BK1} / V_{OUT_BK2}	Nominal output voltage	Programmable	0.6	--	3.3	V
RDS_{PMOS}	High-side (PMOS) on-resistance	V_{IN} = 3.6V	--	80	--	mΩ
RDS_{NMOS}	Low-side (NMOS) on-resistance	V_{IN} = 3.6V	--	40	--	mΩ
F_{SW}	Switching frequency	--	--	3	--	MHz
$DUTY_{MAX}$	Maximum duty cycle	--	--	--	100	%
V_{DC_ACCY}	V_{OUT} DC accuracy	--	--	±2	--	%
V_{LN_REG}	Line regulation	V_{IN} = 2.7 V to 5.5 V at I_{OUT} = 500 mA	--	0.1	--	%/V

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Table 7. Electrical characteristics...*continued*

The following applies unless otherwise noted: Refer to the schematics shown in Section 8.2 "PCB schematics". V_{IN} = 3.6V, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LD_REG}	Load regulation	I_{OUT} = 100 mA to 1500 mA	--	0.2	--	%/A
PGx_{VTH}	BUCKx PG rising threshold	--	--	95	--	$\%/V_{OUT}$
PGx_{HYS}	BUCKx PG hysteresis	--	--	5	--	$\%/V_{OUT}$
DV_{RAMP_RATE}	V_{OUT} dynamic voltage ramp rate	--	--	7	--	mV/µs
LDO						
V_{IN_LDO}	Power supply input	--	1.6	--	5.5	V
$I_{OUT_LDO_MAX}$	Maximum output current in full power mode	--	525	--	--	mA
$I_{OUT_LDO_MIN}$	Minimum LDO load current	--	5	--	--	µA
$I_{OUT_LDO_SLP}$	Maximum output current in sleep mode	--	10	--	--	mA
V_{OUT_LDO}	Nominal output voltage	Programmable (device part number dependent)	1.2	--	3.3	V
$V_{LDO_DC_ACCY}$	LDO output accuracy	--	--	±2	--	%
V_{DROP}	Dropout voltage	V_{OUT} = 1.8 V; I_{OUT} = 100 mA	--	100	--	mV
$V_{LDO_LN_REG}$	Line regulation	V_{IN} = 2.7 V to 5.5 V at I_{OUT} = 100 mA	--	0.05	--	%/V
$V_{LDO_LD_REG}$	Load Regula-tion	I_{OUT} = 100 mA to 500 mA	--	1	--	%
$PGLDO_{VTH}$	LDO PG rising threshold	--	--	95	--	$\%/V_{OUT}$
$PGLDO_{HYS}$	LDO PG hysteresis	--	--	5	--	
Fault protection						
V_{UVLO}	VIN under Vvltage lock-out	VIN increasing	--	2.35	--	V
		Hysteresis	--	0.1		
V_{OVP}	VIN over voltage protection	VIN increasing	--	5.7	--	V
		Hysteresis	--	0.1		
T_{OTS}	Over-temperature thermal shutdown	Temperature rising		145	--	°C
		Hysteresis		20	--	
Digital input thresholds						
V_{IH}	High level input voltage threshold (EN, EN1, EN2, ENLDO, DVS0/ SDI, DVS1)	V_{SVIN} = 2.5V to 5.5V	1.2	--	--	V

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Table 7. Electrical characteristics...*continued*

The following applies unless otherwise noted: Refer to the schematics shown in Section 8.2 "PCB schematics". V_{IN} = 3.6V, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Low level input voltage threshold (EN, EN1, EN2, ENLDO, DVS0/ SDI, DVS1)	V_{SVIN} = 2.5V to 5.5V	--	--	0.4	V

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5 Functional description

5.1 Overview

The PM823 is a performant power management regulator as well as a general purpose power management regulator for portable applications. The PM823 includes two step-down switching (Buck) regulators and one Low Dropout (LDO) regulator. The switching step-down regulators utilize a proprietary internally compensated PWM control to regulate its respective output voltages that require no additional external compensation. The PM823 operates from an input voltage range of 2.7V to 5.5V. The LDO regulator can operate with an input voltage ranging from 100 mV above its regulation point to 5.5V. Each of the two switching regulators can deliver a maximum continuous load of 1.5A at 3 MHz switching frequency; while the LDO can deliver a continuous load current of up to 525 mA. Figure 6 shows the PM823 block diagram.

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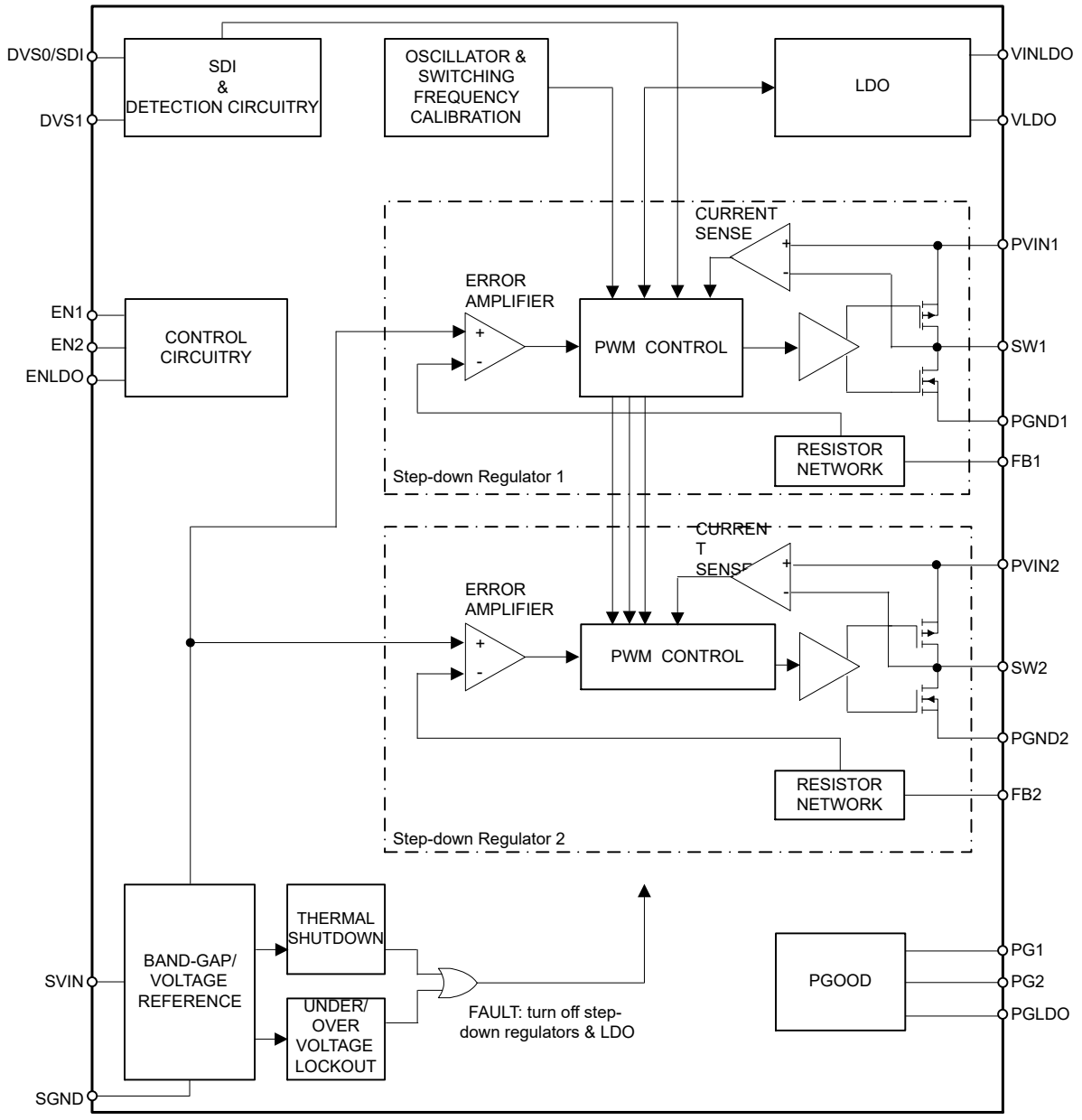

Figure 6. Block diagram

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5.2 Serial interface (1-wire)

The PM823 uses the 1-wire interface. The input for the serial interface is the DVS0 pin, but this functionality is only enabled when the DVS1 pin is set to a high state. Please note SDI capability is not available in sleep mode as this mode requires DVS0=DVS1=Low. The frequency of the SDI interface is 781.25kHz, and has a 20% tolerance. Figure 7 illustrates the serial interface pulse setup.

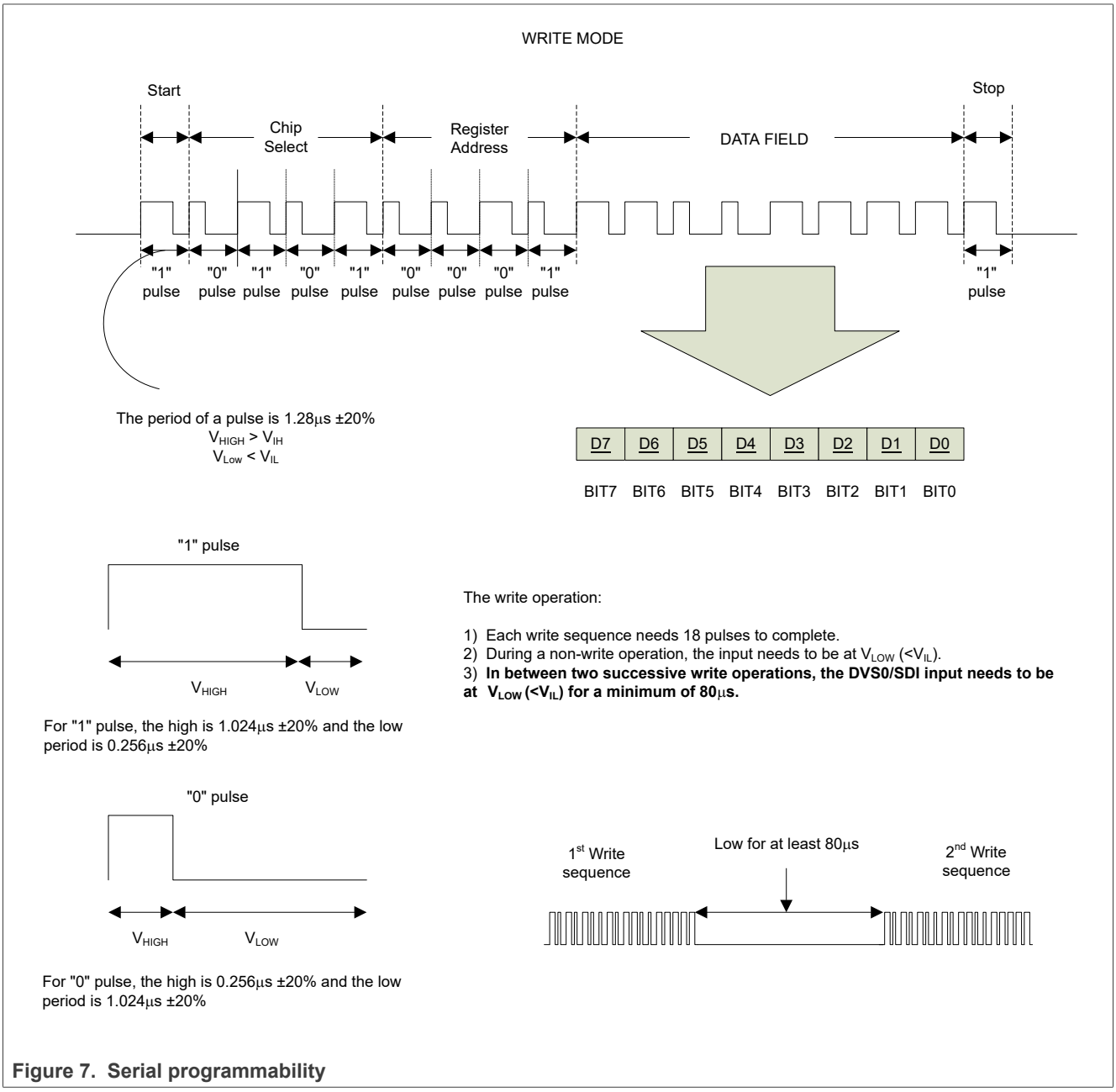

Figure 7. Serial programmability

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5.3 Soft start

The PM823 internally controls the inrush current when the regulator is enabled. This is accomplished by ramping up the desired output voltage based on steps for a predetermined amount of time. Allowing the output voltage to ramp up in this fashion minimizes the current required to charge the output capacitance, therefore limiting the inrush current.

The LDO typical soft start current limit is 50 mA. After the soft start timer has expired (~1 ms), the LDO outputs the full current.

5.4 Power-up sequence

For PM823 with WLCSP package, the EN pin controls the output sequence for all 3 regulators.

For PM823 with QFN package, it is recommended that EN1, EN2 and ENLDO are connected together. Once the part is enabled, Buck2 initializes. After Buck2 completes its start-up, the LDO initializes, followed by Buck1.

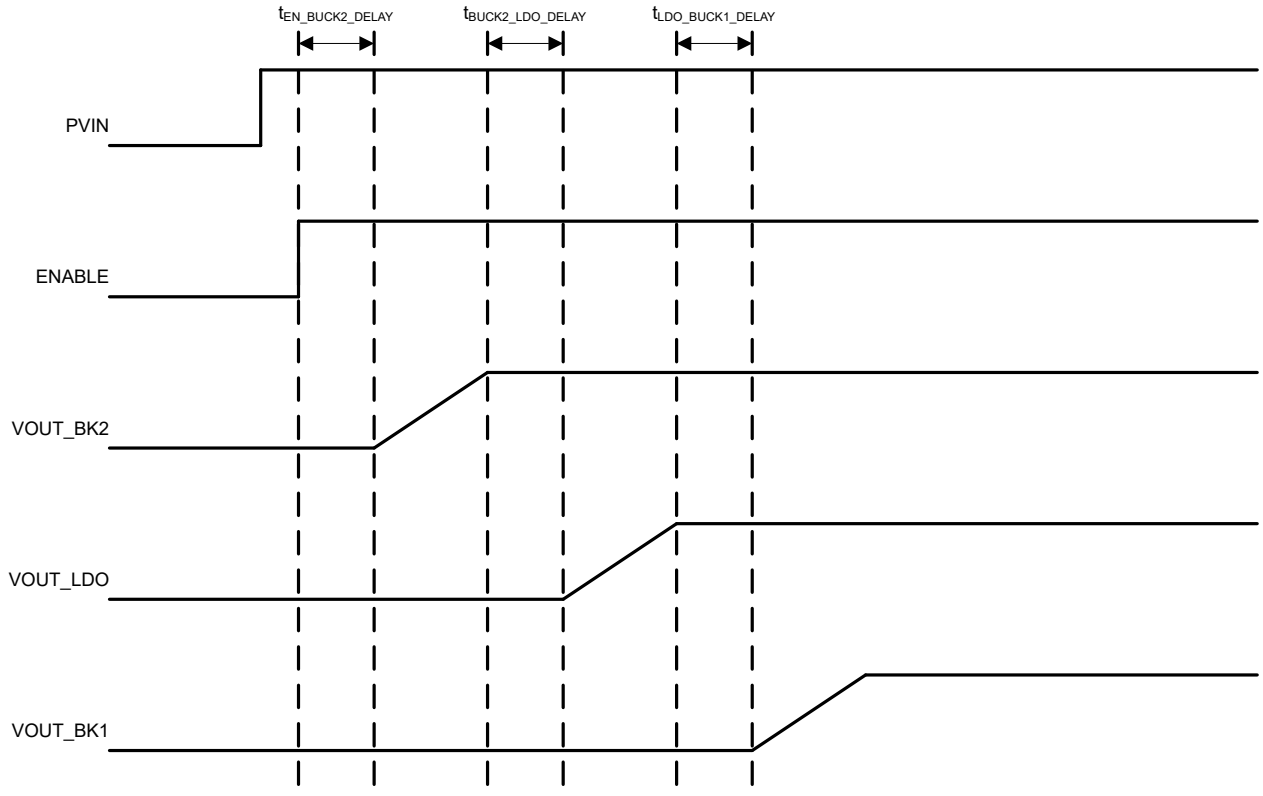

Figure 8. Power-up sequence timing diagram - WLCSP package option

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5.5 Power good

The PM823 contains a power good comparator which pulls low when the output voltage falls below 90% of its regulated value, or when the output voltage is above 95% of its regulated value when the output voltage is rising. The PGOOD output is an open-drain transistor which is off and becomes high impedance when the output voltage is in regulation. This high impedance state allows an external resistor to pull the PGOOD pin high when this transistor is off, or when the buck regulator is disabled via the enable pin.

5.6 Operating modes

The PM823 supports four operating modes selected by the Dynamic Voltage Scaling (DVS) pins and the internal register as shown in Table 8. Each operating mode provides different power saving features to meet different application needs. For example, even if the serial interface is not used, the DVS pins are still able to provide the power saving feature.

Table 8. Operating mode selections

Operating mode	DVS1	DVS0	Reg 0x05 bit [2]	Functional description
Active Mode 1	High	SDI	X (don't care)	Full power mode and the serial interface (pin DVS0) is enabled
Active Mode 2	Low	High	1	Full power mode, but the serial interface is disabled
Active Mode 3	Low	High	0	Automatic power saving mode and the serial interface is disabled
Sleep Mode	Low	Low	1	Lowest power mode and the serial inter-face is disabled

The PM823 supports two full power modes, Active Mode 1 and Active Mode 2. Both full power modes have the same power consumption. The major differences are first that the serial interface is not enabled in Active Mode 2, and second that the buck1 regulator can be programmed to different output voltages in Active Modes 1 and 2 to support different applications.

When the PM823 is set to Active Mode 3, the internal clock automatically turns off during a light load (PFM) condition to reduce the system power consumption, but the output voltage remains the same as in Active Mode 1. Active Mode 3 improves the system power consumption if the serial interface is not used.

The PM823 also supports the Sleep Mode function which minimizes the system power during a low power mode event. The PM823 quiescent current is reduced to 15 µA during Sleep Mode. However, during Sleep Mode, the maximum output current for each regulator is limited to 10 mA. If the load current is increased beyond the limit, the over current protection mechanism kicks in and shuts down the output voltage. The buck1 output voltage can be set through Register 0x02.

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5.7 DVS output voltage settings

The PM823 buck1 output voltage can be set to different output voltages in different operating modes through the internal registers. The buck2 and LDO output voltages can be changed as well during Active Mode 1 through programming. However, the buck2 and LDO remain the same across different operating modes.

Table 9. DVS output voltage settings

Operating mode	DVS1	DVS0	Reg 0x05 bit [2]	Buck1 output voltage settings
Active Mode 1	High	SDI	X (don't care)	See Section 10.3.1 "Buck1 active mode 1 and mode 3 output voltage control".
Active Mode 2	Low	High	1	See Section 10.3.2 "Buck1 active mode 2 output voltage control".
Active Mode 3	Low	High	0	See Section 10.3.1 "Buck1 active mode 1 and mode 3 output voltage control".
Sleep Mode	Low	Low	1	See Section 10.3.3 "Buck1 sleep mode output voltage control".

The time to change from one output voltage level to another can be calculated with the following equation:

$$t_{DV} = \frac{|V_{OUT_CURRENT} - V_{OUT_NEW}|}{DV_{RAMP_RATE}}$$

Example:

$V_{OUT_CURRENT}$ = 1.2000V

V_{OUT_NEW} = 1.2500V

DV_{RAMP_RATE} = 7 mV/µs

$$7.1429\mu s = \frac{|1.2000V - 1.2500V|}{(7mV)/(\mu s)}$$

5.8 Sleep mode

The PM823 supports the sleep mode function which saves power when the system is in low power mode. The maximum output current for each regulator is limited to 10 mA. If the load current is increased beyond the sleep mode current limit, the PM823 over-current protection kicks in and shuts down the corresponding output. The DVS0 and DVS1 pins are used to set the PM823 to different operating modes. Before entering sleep mode, the host needs to enable the DVS function by setting the REG5 bit[2] to 1. The sleep mode buck1 output voltage can be preprogrammed using REG0 bit[6:5] and REG2 bit[4:0]. The PM823 enters sleep mode when all the required registers are set and both DVS0 and DVS1 pins are asserted to low.

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5.9 Under voltage lock-out (UVLO)

This feature ensures that both internal MOSFETs for the step-down regulators and for the LDO regulator have adequate voltage levels to operate. When the input voltage is below UVLO low threshold, both MOSFETs for the step-down regulators and for the LDO regulator are off until the input rises above the UVLO high threshold. The switching nodes (SW) for both step-down regulators are in high Z state when the input voltage is less than UVLO high threshold.

5.10 Over voltage protection (OVP)

An over-voltage comparator guards against line transient overshoots, as well as other serious conditions that may damage the IC. When the input voltage is above OVP high threshold the output turns off and the switching node (SW) for both step-down regulators are high Z. The device will remain at this state until the input voltage comes back below OVP low threshold.

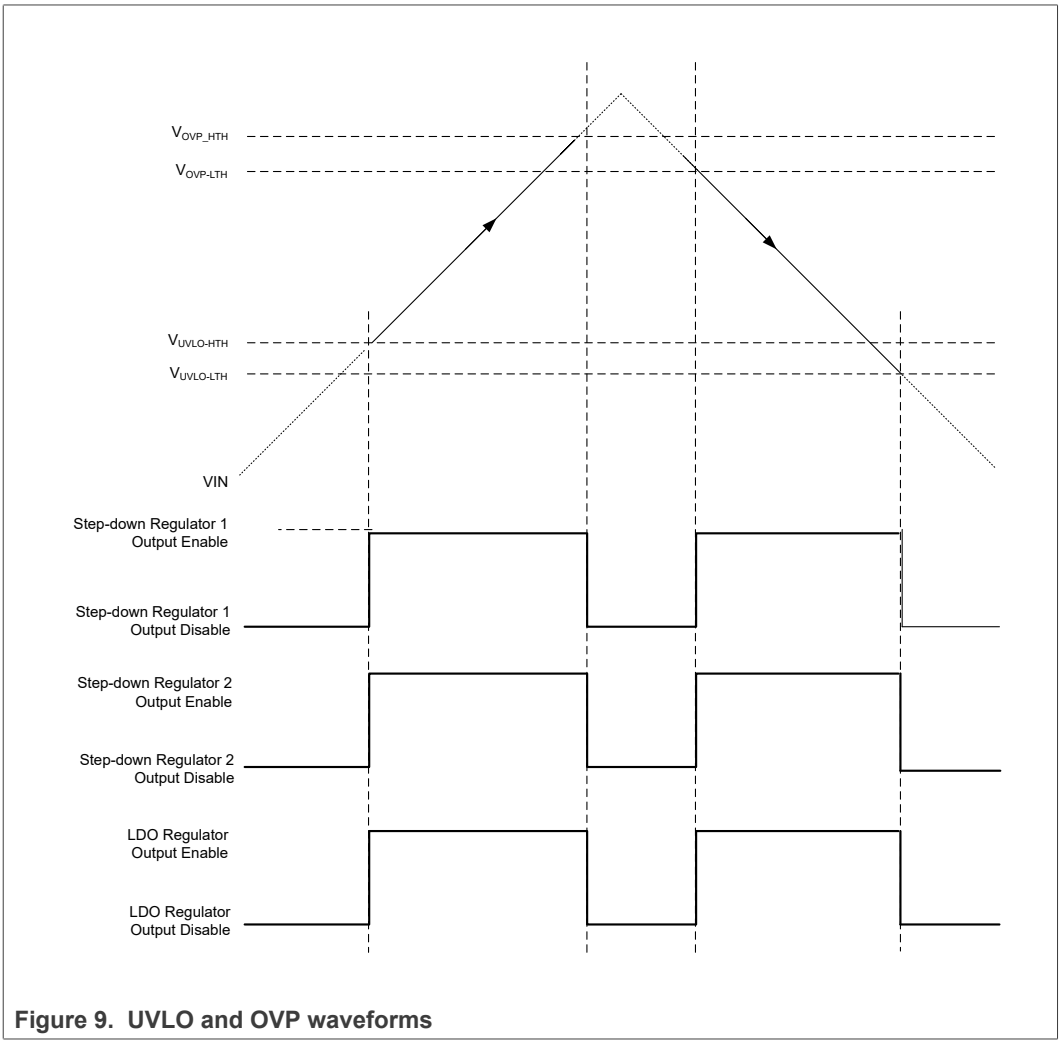

Figure 9. UVLO and OVP waveforms

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5.11 Over-temperature thermal shutdown (OTS)

When the junction temperature exceeds OTS high threshold, the thermal shutdown circuitry disables the PM823. The device is enabled again once the junction temperature is below OTS low threshold.

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6 Functional characteristics

See Section 8.2 "PCB schematics".The following applies unless otherwise noted: T_A = 25°C,

V_{IN} = 5V, V_{OUT_BK1} = 1.1V, V_{OUT_BK2} = 2.2V, and V_{OUT_LDO} = 1.8V.

6.1 Start-up waveforms

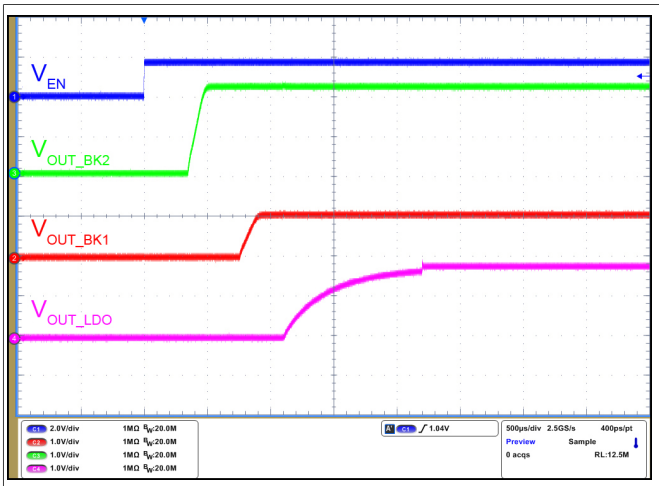

Figure 10. Startup

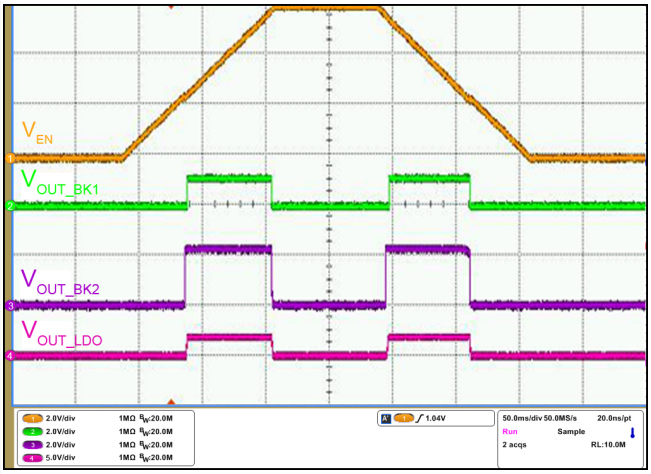

Figure 11. UVLO / OVP Thresholds

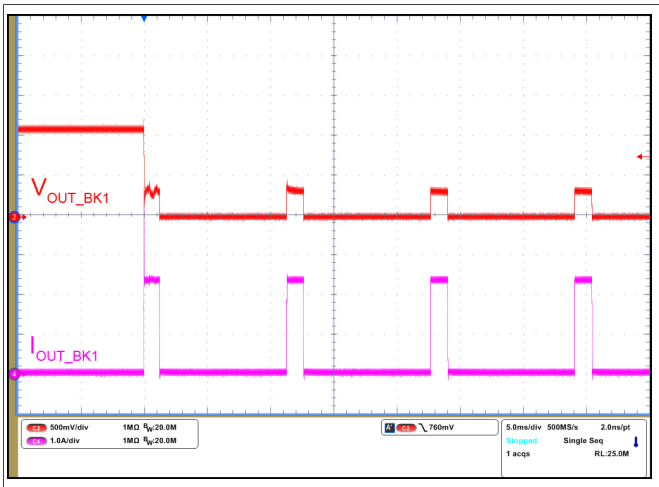

Figure 12. Buck1 short circuit

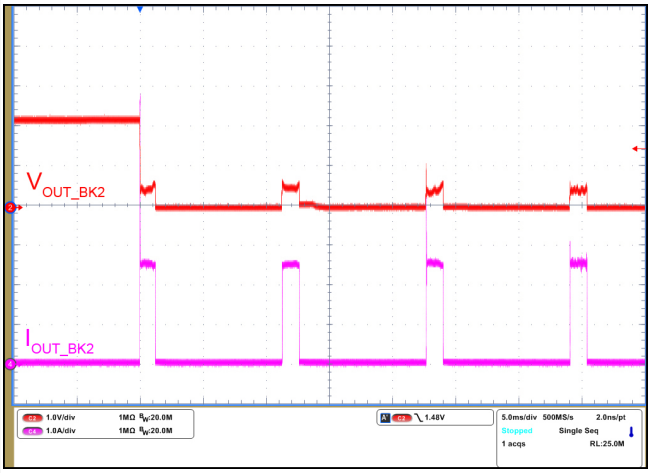

Figure 13. Buck2 short circuit

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6.2 Load transient waveforms

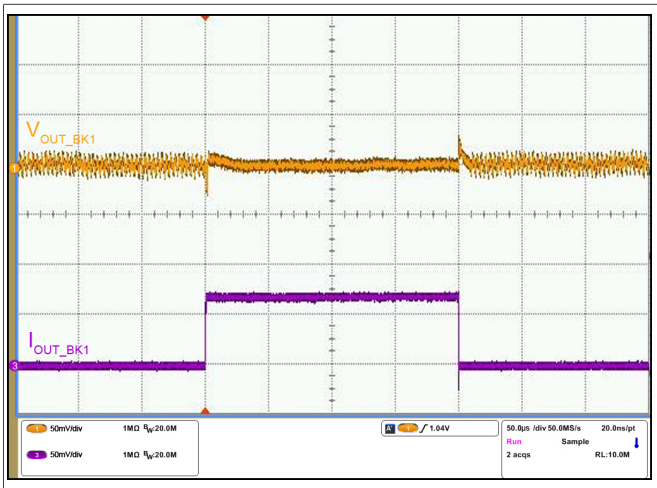

Figure 14. Buck1 (1.1V) load transient response 100 mA to 750 mA

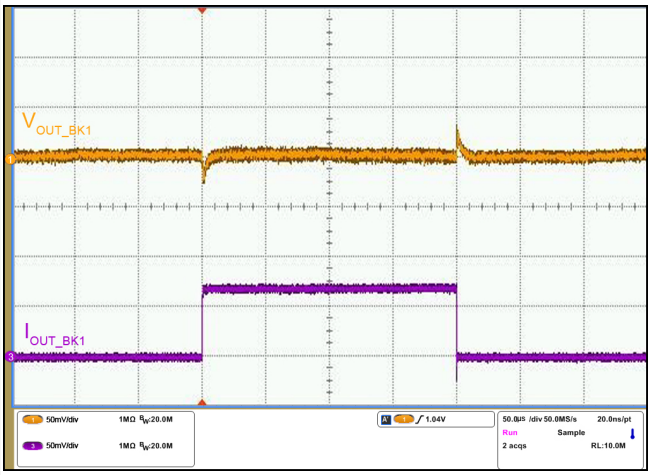

Figure 15. Buck1 (1.1V) load transient response 750 mA to 1.5A

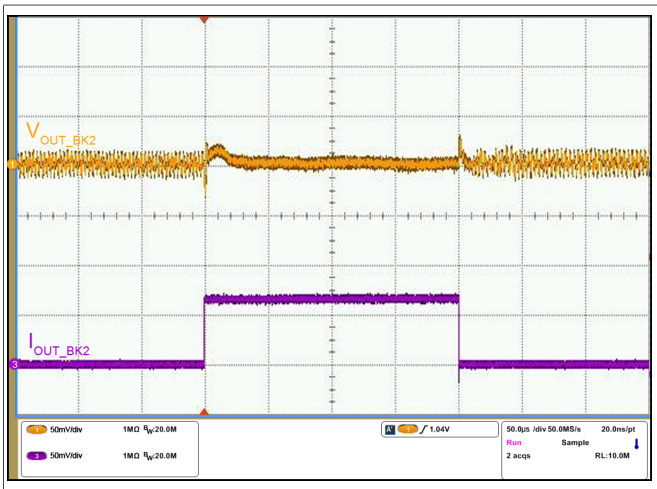

Figure 16. Buck2 (2.2V) load transient response 100 mA to 750 mA

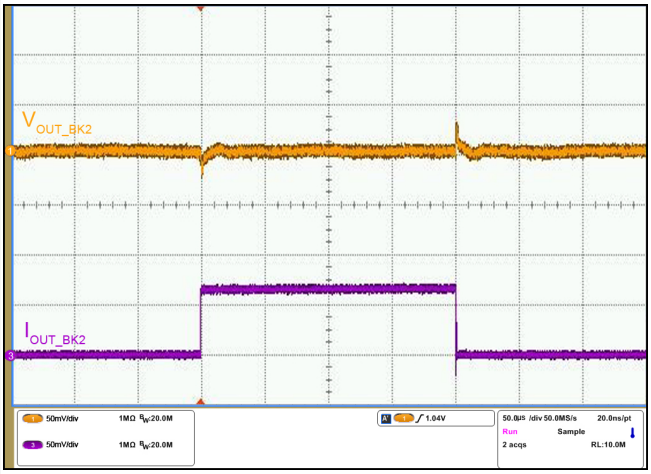

Figure 17. Buck2 (2.2V) load transient response 750 mA to 1.5A

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6.3 Switching waveforms

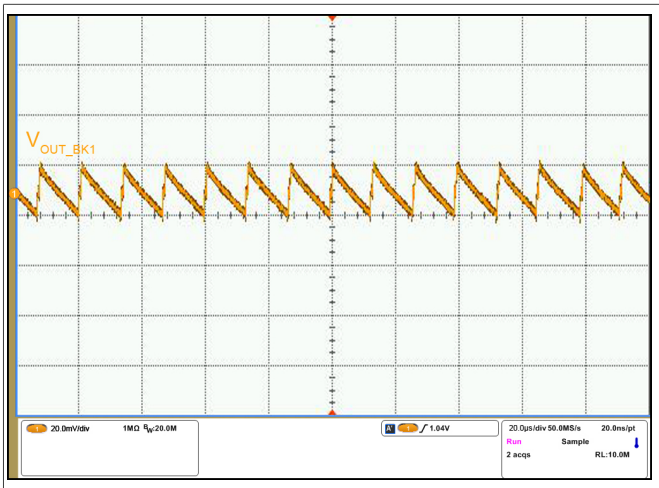

Figure 18. Buck1 (1.1V) PFM Output Ripples at 25 mA

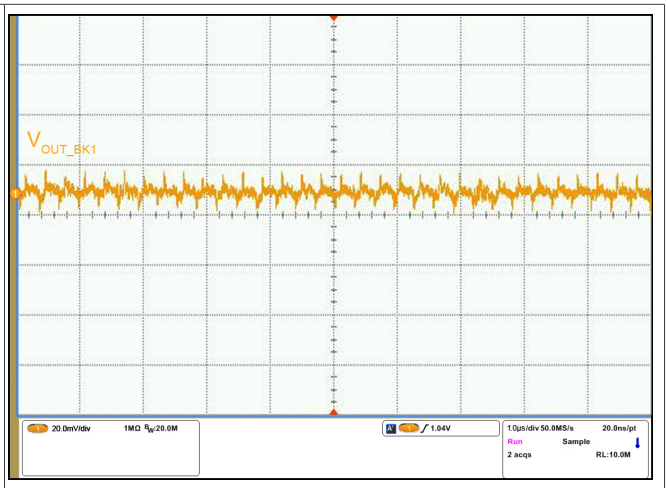

Figure 19. Buck1 (1.1V) PWM Output Ripples at 1.5A

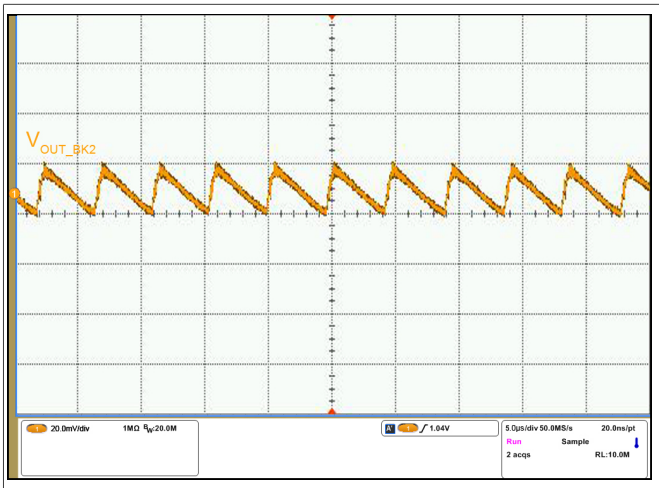

Figure 20. Buck2 (2.2V) PFM Output Ripples at 45 mA

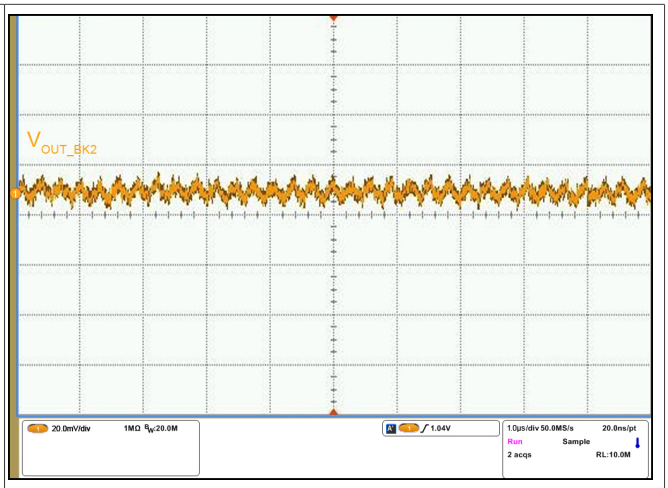

Figure 21. Buck2 (2.2V) PWM Output Ripples at 1.5A

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7 Typical characteristics

Unless otherwise noted, the following typical scope photographs were taken using the test circuits shown in Section 8.2 "PCB schematics" at T_A = 25°C.

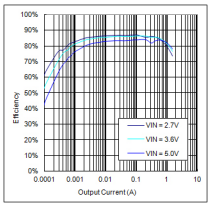

Figure 22. Buck1 (1.1V) efficiency vs output current WLCSP-12

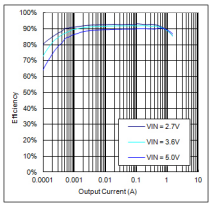

Figure 23. Buck2 (2.2V) efficiency vs output current WLCSP-12

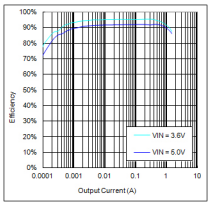

Figure 24. Buck1 (3.3V) efficiency vs output current QFN-24

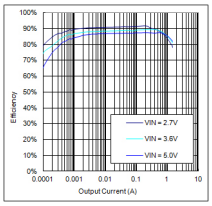

Figure 25. Buck2 (1.8V) efficiency vs output current QFN-24

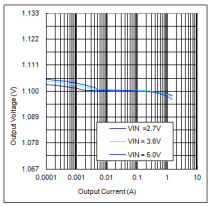

Figure 26. Buck1 (1.1V) output voltage vs output current WLCSP-12

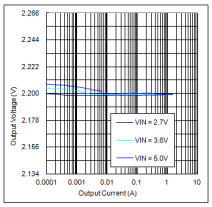

Figure 27. Buck2 (2.2V) output voltage vs output current WLCSP-12

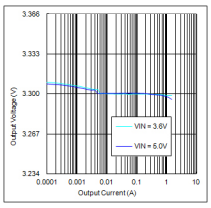

Figure 28. Buck1 (3.3V) output voltage vs output current QFN-24

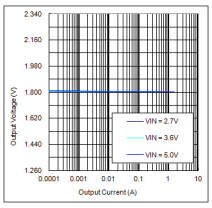

Figure 29. Buck2 (1.8V) output voltage vs output current QFN-24

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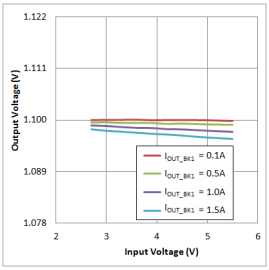


Figure 30. Buck1 output voltage vs input voltage WLCSP-12

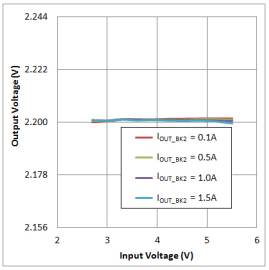
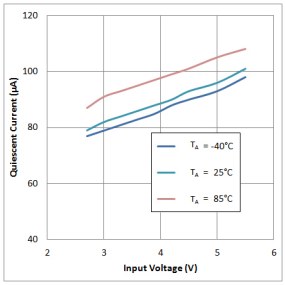


Figure 31. Buck2 Output Voltage vs Input Voltage WLCSP-12



(BK1=1.1V, BK2=2.2V, LDO=1.8V, V_{INLDO} connect to V_{INBUCK})

Figure 32. Quiescent Current vs Input Voltage For Active Mode 3

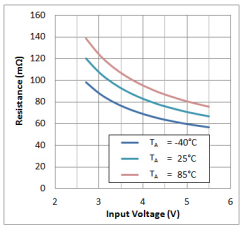


Figure 33. Buck1 high side $R_{DS(ON)}$ vs. input voltage WLCSP-12

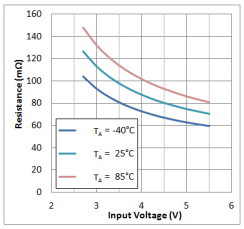


Figure 34. Buck2 high side $R_{DS(ON)}$ vs. input voltage WLCSP-12

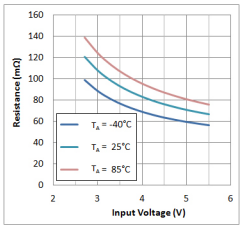


Figure 35. Buck1 low side $R_{DS(ON)}$ vs. input voltage WLCSP-12

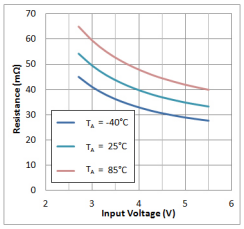


Figure 36. Buck2 low side $R_{DS(ON)}$ vs. input voltage WLCSP-12

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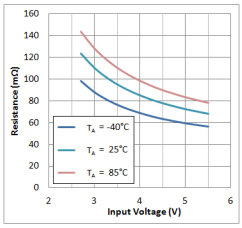


Figure 37. Buck1 high side $R_{DS(ON)}$ vs. input voltage QFN-24

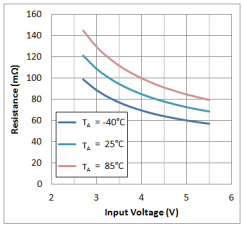


Figure 38. Buck2 high side $R_{DS(ON)}$ vs. input voltage QFN-24

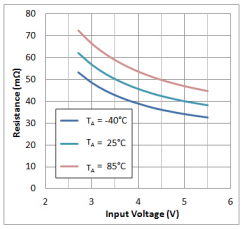


Figure 39. Buck1 low side $R_{DS(ON)}$ vs. input voltage QFN-24

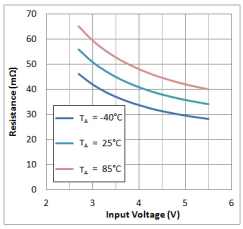


Figure 40. Buck2 low side $R_{DS(ON)}$ vs. input voltage QFN-24

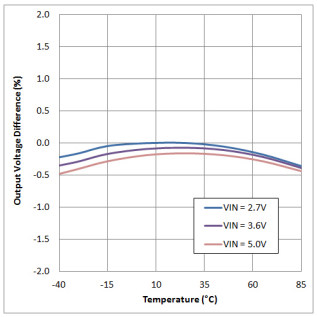


Figure 41. Buck1 Output Voltage Error vs Temperature

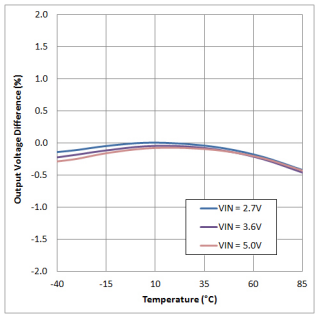
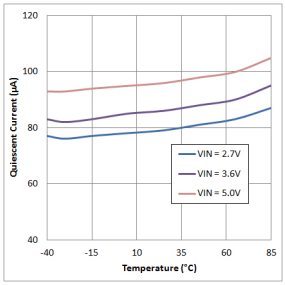


Figure 42. Buck2 Output Voltage Error vs Temperature



(BK1=1.1V, BK2=2.2V, LDO=1.8V, V_{INLDO} connect to V_{INBUCK})

Figure 43. Quiescent current vs temperature for active mode 3

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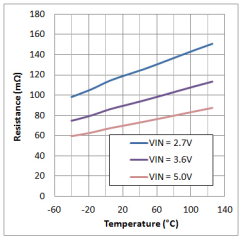

Figure 44. Buck1 high side $R_{DS(ON)}$ vs. temperature WLCSP-12

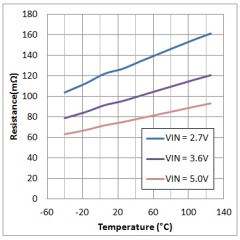

Figure 45. Buck2 high side $R_{DS(ON)}$ vs. temperature WLCSP-12

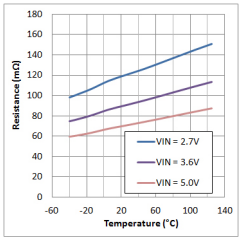

Figure 46. Buck1 low side $R_{DS(ON)}$ vs. temperature WLCSP-12

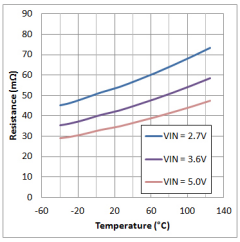

Figure 47. Buck2 low side $R_{DS(ON)}$ vs. temperature WLCSP-12

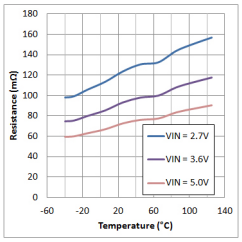

Figure 48. Buck1 high side $R_{DS(ON)}$ vs. temperature QFN-24

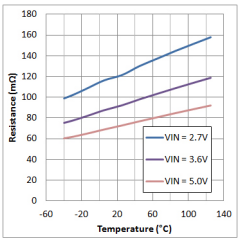

Figure 49. Buck2 high side $R_{DS(ON)}$ vs. temperature QFN-24

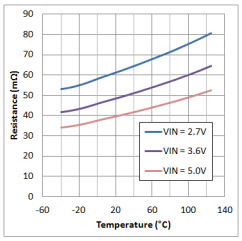

Figure 50. Buck1 low side $R_{DS(ON)}$ vs. temperature QFN-24

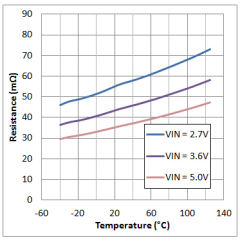

Figure 51. Buck2 low side $R_{DS(ON)}$ vs. temperature QFN-24

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8 Application information

8.1 PC board layout considerations and guidelines

Caution: To avoid abnormal noise and operating behavior follow these layout recommendations.

The PC board layout is very critical in any switching converter application. An improper layout can contribute to system instability, excessive EMI (electromagnetic interference), and high switching loss. Follow these basic guidelines to assure a good PCB layout:

1. Copy these layout guidelines within this section as much as possible including the use of the recommended BOM
2. Before importing the net list into the layout tool, it is highly recommended to go through the board floor planning phase (the process defining the general location of components on the blank PCB before drawing in any traces).
   a. It is highly recommended to allocate 40% or more of the layout schedule to dedicate for floor planning of the board.
   b. Here are some of the questions that are commonly derived from the floor planning phase.
   Where to place the SOC on the board?
   On the top or bottom layer?
   In the center?
   c. After deciding where to place the SOC, the next step is to place the power management IC for the core voltage of the SOC.
   d. The optimum position to place the power management IC is on the same layer as the SOC. The output voltage of the power management IC should be close to the input voltage of the SOC.
   e. Continue this floor planning phase for the rest of the voltage rails before starting to layout the board.
3. ATTENTION: Before starting to route any traces and after choosing where to place the power management IC on the board, the next step is to place the input capacitors.
   a. Place input capacitor for the SVIN and SGND pins on the same layer as the IC.
   b. Then, place input capacitor for the PVIN and PGND pins on the same layer as the IC.
   c. Next, place the negative terminal for the output capacitors next to the negative terminal of the input capacitors.
   d. See Section 4.4 "Electrical characteristics " for the recommended input and output capacitor values.
   e. See Section 4.4 "Electrical characteristics " for the recommended distance between the IC and the input and output capacitors.
   f. **Do not place the inductor before placing the capacitors.** The input capacitors placement is the most crucial for proper operation. The AC current circulating through the input capacitors, loop (LP1), is a square wave with rise and fall times as fast as 8ns (typical) with slew rates being as high as 300µA/µs (typical). At these fast slew rates, stray and parasitic PCB inductance can generate voltage spikes as high as 3V per inch of the PCB trace;
   V_{IND} = L * di/dt.

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   g. Keep loop 2 (LP2) as small as possible and connect the negative terminal of the output capacitor as close to the negative terminal of the input capacitor as possible.

4. The input capacitors for the SVIN and PVIN pins need to be Ceramic or equivalent low ESR capacitor.
   a. **Do not replace the Ceramic input or output capacitors with Tantalum capacitors.**
   b. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor is placed next to the IC. If Tantalum input capacitors are used, it must be rated for switching regulator applications and the operating voltage must be de-rated by 50%.
   c. Any type of capacitor can be placed in parallel with the output capacitor.
   d. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that Ceramic capacitors provide the lowest noise and smallest foot print solution.
5. Use planes for the ground, input and output power to maintain good voltage filtering and to keep power losses low. If there is not enough space to place a power plane for the input sup-ply, then the input supply trace must be at least 3/8 of an inch wide.
6. Keep the switching and all sensitive traces away from the fast dv/dt to minimize capacitive coupling effects.

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8.2 PCB schematics

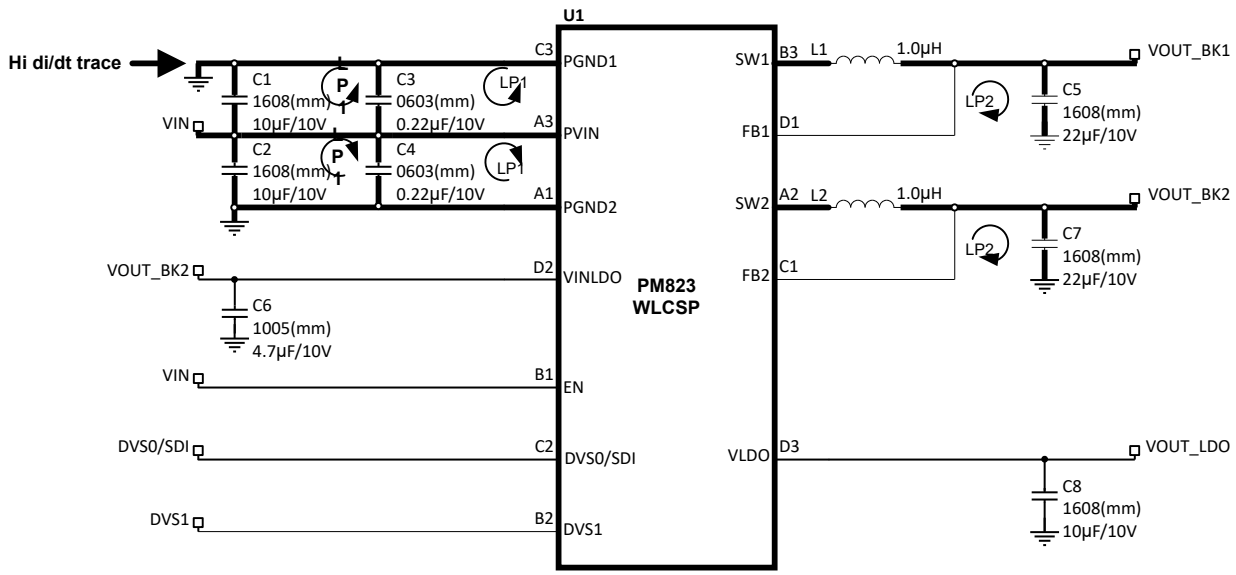

Figure 52. PCB schematic - WLCSP package

Notes:

- For C3 and C4, can use 0.1 µF but it is best to use maximum capacitance for the 0603(mm)/0201(in) case size. For example, 0.22 µF is available 0603(mm)/0201(in) size.
- For all capacitors, use the highest voltage rating available for the case size. For example, 22 µF is available in 1608(mm)/0603(in) case size with 6.3V and 10V rating. Use 22 µF/10V rating instead of 22 µF/6.3V rating
- See Section 5.4 "Power-up sequence" for the power sequence function
- See Section 5.7 "DVS output voltage settings" for DVS0 and DVS1 function and configuration. Do not float DVS/SDI and DVS1 pin.

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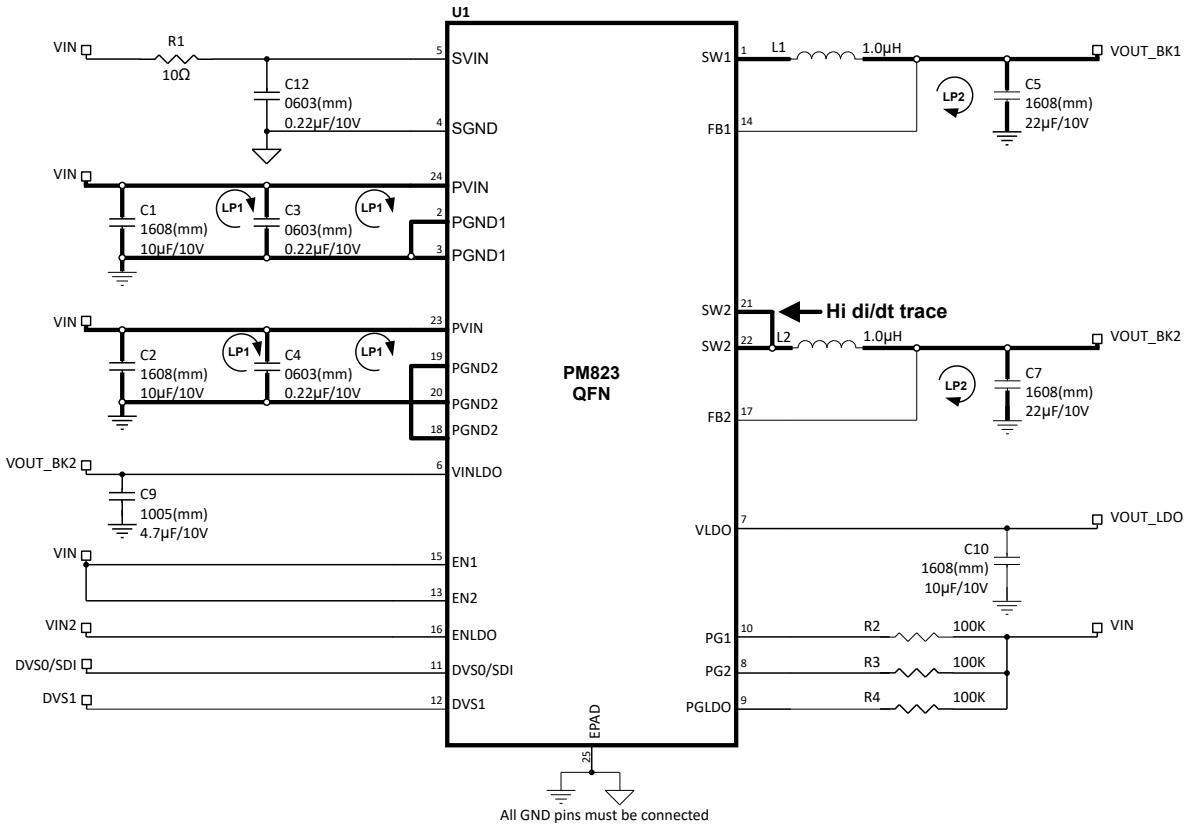

Figure 53. PCB schematic - QFN package

Notes:

- For C3 and C4, can use 0.1µF but it is best to use maximum capacitance for the 0603(mm)/0201(in) case size. For example, 0.22µF is available 0603(mm)/0201(in) size
- For all capacitors, use the highest voltage rating available for the case size. For example, 22µF is available in 1608 (mm) / 0603 (in) case size with 6.3V and 10V rating. Use 22µF/10V rating instead of 22µF/6.3V rating
- For EN1, EN2, and ENLDO pins, can connect directly to VIN or through a 100K pull-up resistor if all outputs are turned on at the same time
- If the LDO output voltage comes after the Buck2 output, then connect VIN_LDO to VOUT2_BK2. Either have the ENLDO pin connect to VOUT_BK2 or connect through a 100K pull-up resistor.
- See Section 5.2 "Serial interface (1-wire)" for the SDI function and configuration
- See Section 5.4 "Power-up sequence" for the power sequence function
- See Section 5.7 "DVS output voltage settings" for DVS0 and DVS1 function and configuration. Do not float DVS0/SDI and DVS1 pin.

8.3 PCB layout examples

- WLCSP actual board size = 286 mil x 258 mil
- QFN actual board size = 409 mil x 510 mil

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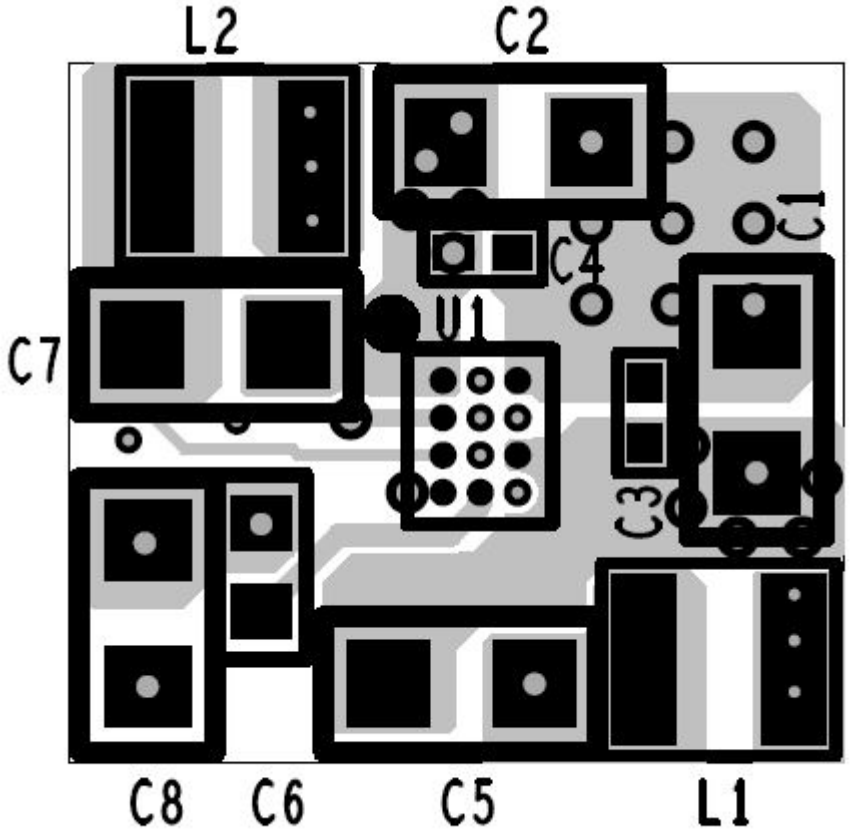
- WLCSP total copper layers = 4
- QFN total copper layers = 2

8.3.1 PCB layout for WLCSP package



The input capacitors must be placed closely to the corresponding power and ground pins (PVIN/PGND) on the same PCB layer as the IC.

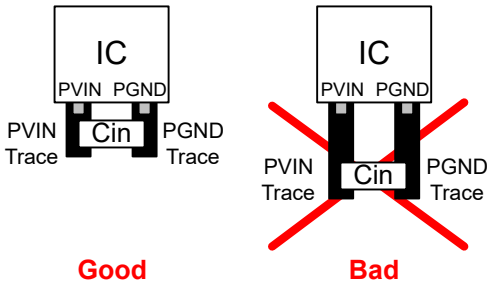


Figure 54. Top traces, vias, and copper (not to scale)

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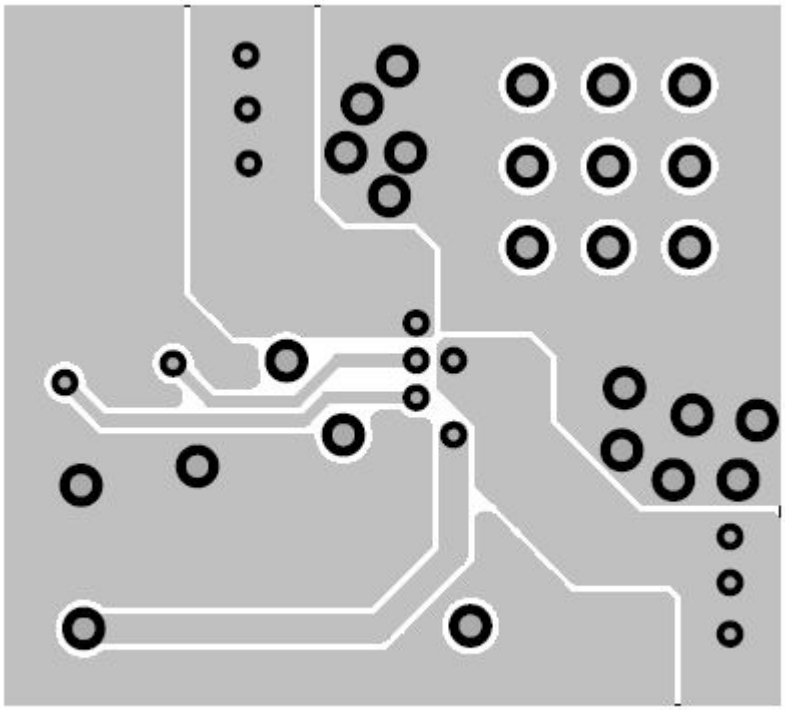

Figure 55. Layer 2 vias and copper (not to scale)

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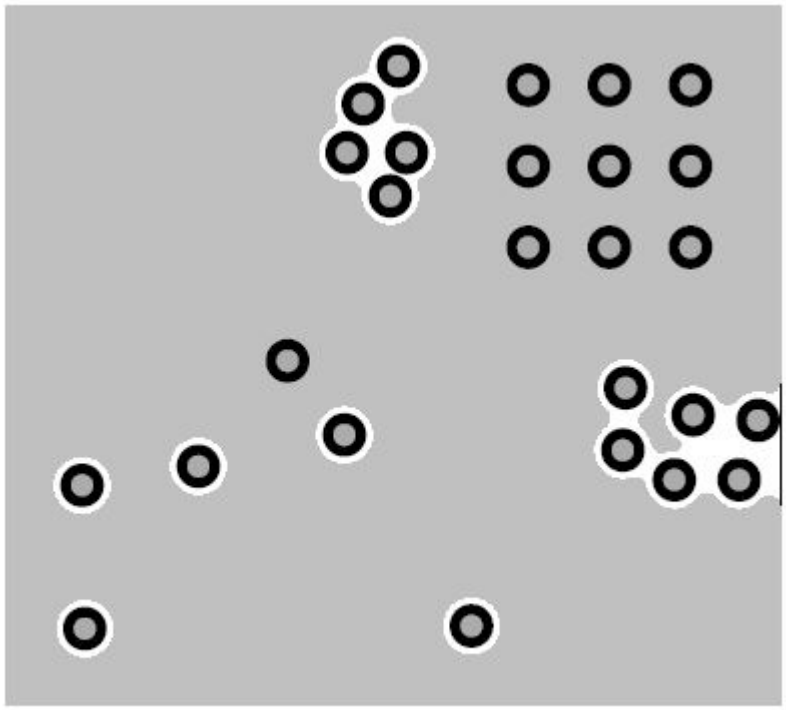

Figure 56. Layer 3 vias and copper (not to scale)

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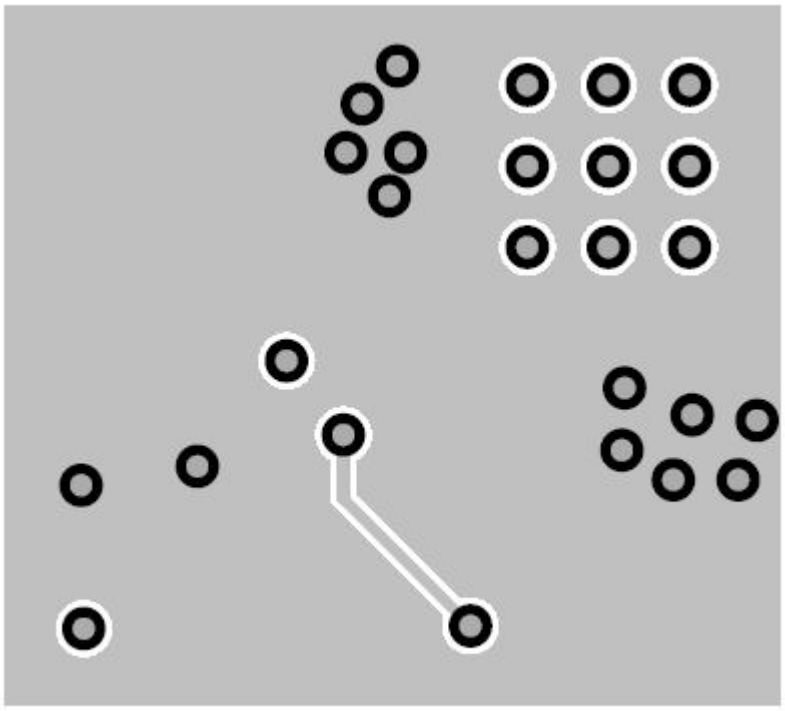

Figure 57. Bottom traces, vias, and copper (not to scale)

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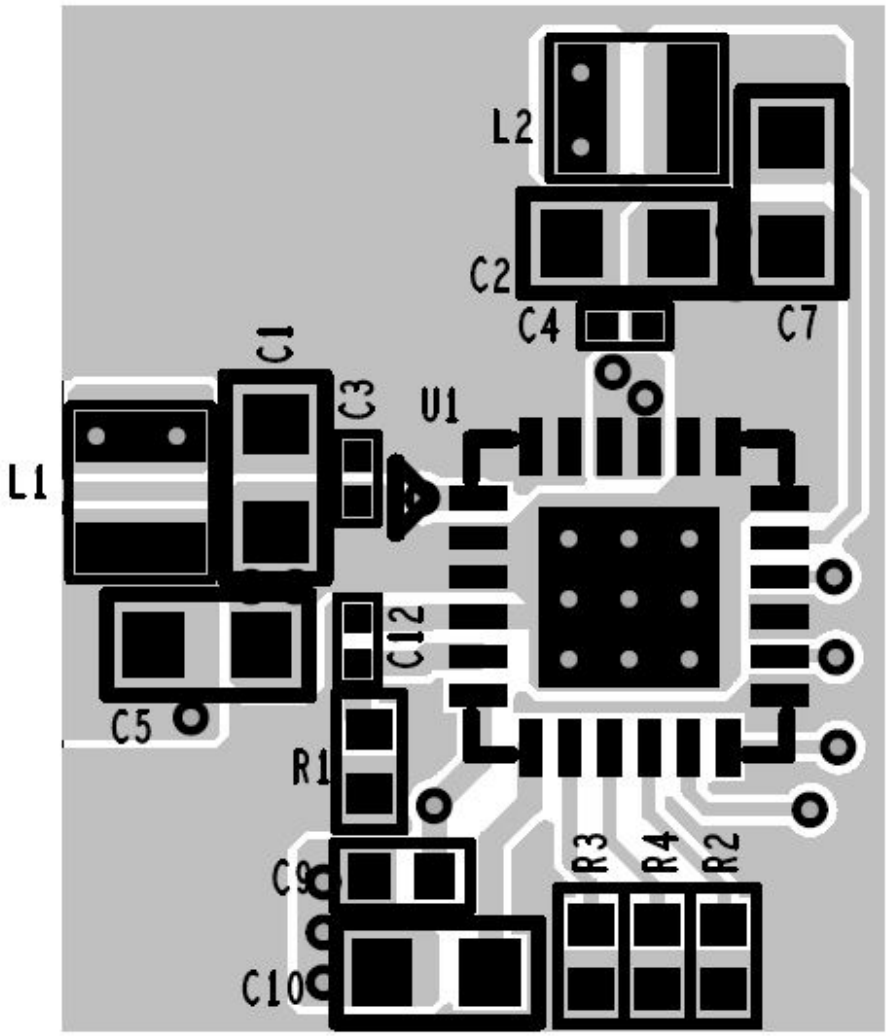
8.3.2 PCB layout for QFN package



The input capacitors must be placed closely to the corresponding power and ground pins (PVIN/PGND) on the same PCB layer as the IC.

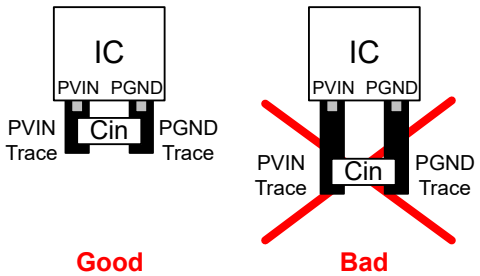


Figure 58. Top traces, vias, and copper (not to scale)

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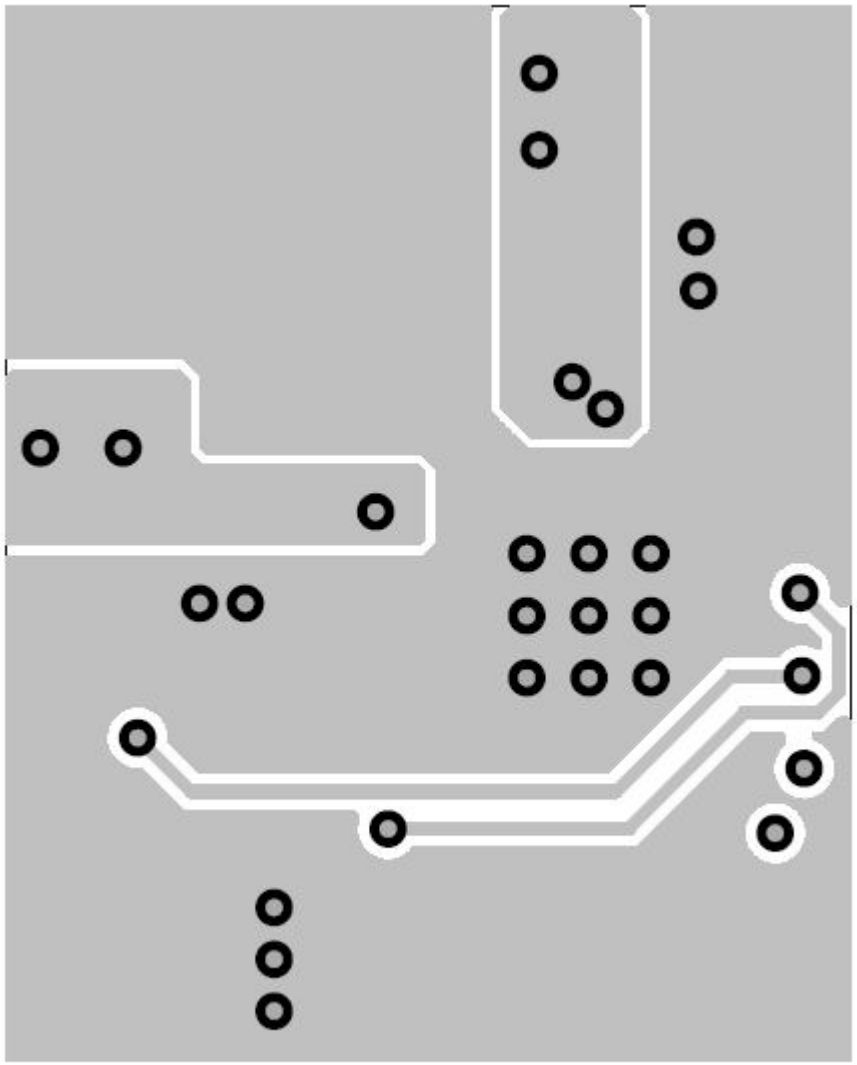

Figure 59. Bottom traces, vias, and copper (not to scale)

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8.4 Bill of materials (BOM)

Note:

Check component datasheets for the latest updates before designing these components in the schematic.

Check the maximum temperature of the applications and maximum heat source that these components will be placed next to. For example, these components might be placed near the SOC and the SOC might act as the heat source. This heat source can have a higher temperature than the ambient temperature. These recommended components are suitable for hand-held and portable applications. Components with high temperature ratings might be needed based on the maximum temperature of the application or the maximum heat source that these components will be subject to.

Table 10. BOM for WLCSP package

Item	Qty	Ref	Manufacturer part number	Manufacturer	Description
1	3	C1,C2, C8	GRM188R61A106KE69D	Murata	CAP CER 10µF 10V ±10% X5R 1608(mm) / 0603(in)
2	2	C3,C4	GRM033R61A224ME90D	Murata	CAP CER 0.22µF 10V ±20% X5R 0603(mm) / 0201(in)
3	2	C5,C7	GRM188R61A226ME15	Murata	CAP CER 22µF 10V ±20% X5R 1608(mm) / 0603(in)
4	1	C6	GRM155R61A475MEAA	Murata	CAP CER 4.7µF 10V ±20% X5R 1005(mm) / 0402(in)
5	2	L1,L2	HEI201612A-1R0M-Q8D2	Chilisin	HEI201612A Series 1.0µH, L = 2.0mm, W = 1.6mm, H = 1.2mm
			MHCD201612A-1R0M-A8SDZ	Chilisin	MHCD201612A Series 1.0µH, L = 2.0mm, W = 1.6mm, H = 1.2mm
6	**1**	**U1**	**PM823**	**NXP**	**PM823 in WLCSP-12 package with dual synchronous bucks and LDO**

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Table 11. BOM for QFN Package

Item	Qty	Ref	Manufacturer part number	Manufacturer	Description
1	3	C1,C2, C10	GRM188R61A106KE69	Murata	CAP CER 10µF 10V ±10% X5R 1608(mm) / 0603(in)
2	3	C3,C4, C12	GRM033R61A224ME90D	Murata	CAP CER 0.22µF 10V ±20% X5R 0603(mm) / 0201(in)
3	2	C5,C7	GRM188R61A226ME15	Murata	CAP CER 22µF 10V ±20% X5R 1608(mm) / 0603(in)
4	1	C9	GRM155R61A475MEAA	Murata	CAP CER 4.7µF 10V ±20% X5R 1005(mm) / 0402(in)
5	2	L1,L2	HEI201612A-1R0M-Q8D2	Chilisin	HEI201612A Series 1.0µH, L = 2.0mm, W = 1.6mm, H = 1.2mm
			MHCD201612A-1R0M-A8SDZ	Chilisin	MHCD201612A Series 1.0µH, L = 2.0mm, W = 1.6mm, H = 1.2mm
6	1	R1	RC0402FR-0710RL	Yageo	RES 10Ω 1/16W ±1% 0402 SMD
7	3	R2,R3, R4	RC0402JR-07100KL	Yageo	RES 100kΩ 1/16W ±5% 0402 SMD
8	**1**	**U1**	**PM823**	**NXP**	**PM823 in QFN-24 package with dual synchronous bucks and LDO**

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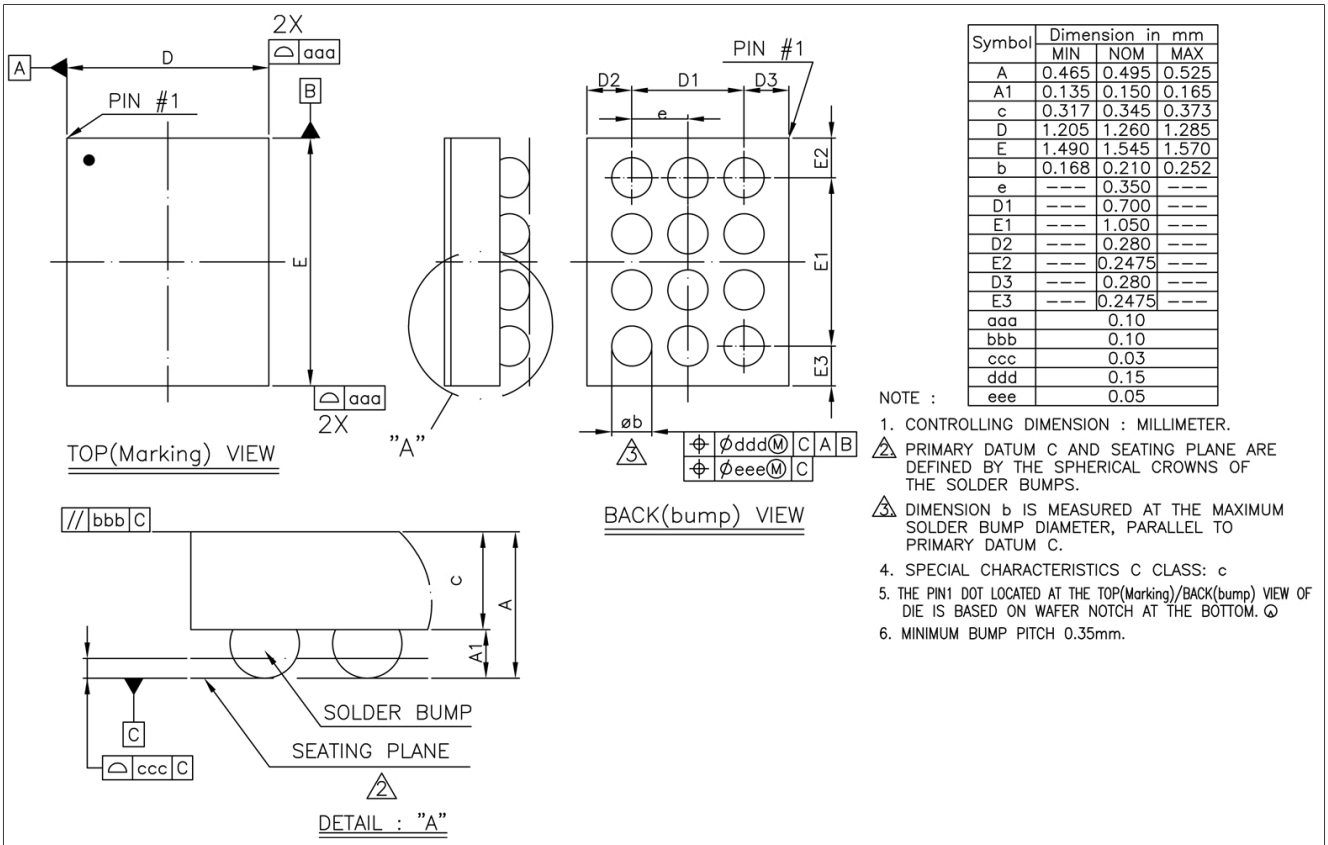
9 Package information

9.1 Package mechanical drawings



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.465	0.495	0.525
A1	0.135	0.150	0.165
c	0.317	0.345	0.373
D	1.205	1.260	1.285
E	1.490	1.545	1.570
b	0.168	0.210	0.252
e	---	0.350	---
D1	---	0.700	---
E1	---	1.050	---
D2	---	0.280	---
E2	---	0.2475	---
D3	---	0.280	---
E3	---	0.2475	---
aaa	0.10		
bbb	0.10		
ccc	0.03		
ddd	0.15		
eee	0.05		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: c
5. THE PIN1 DOT LOCATED AT THE TOP(Marking)/BACK(bump) VIEW OF DIE IS BASED ON WAFER NOTCH AT THE BOTTOM.
6. MINIMUM BUMP PITCH 0.35mm.

Figure 60. 1.260mm x 1.545mm WLCSP-12 mechanical drawing

Note: *All dimensions in mm. See Section 9.2 "Package markings" for package marking and pin 1 location.*

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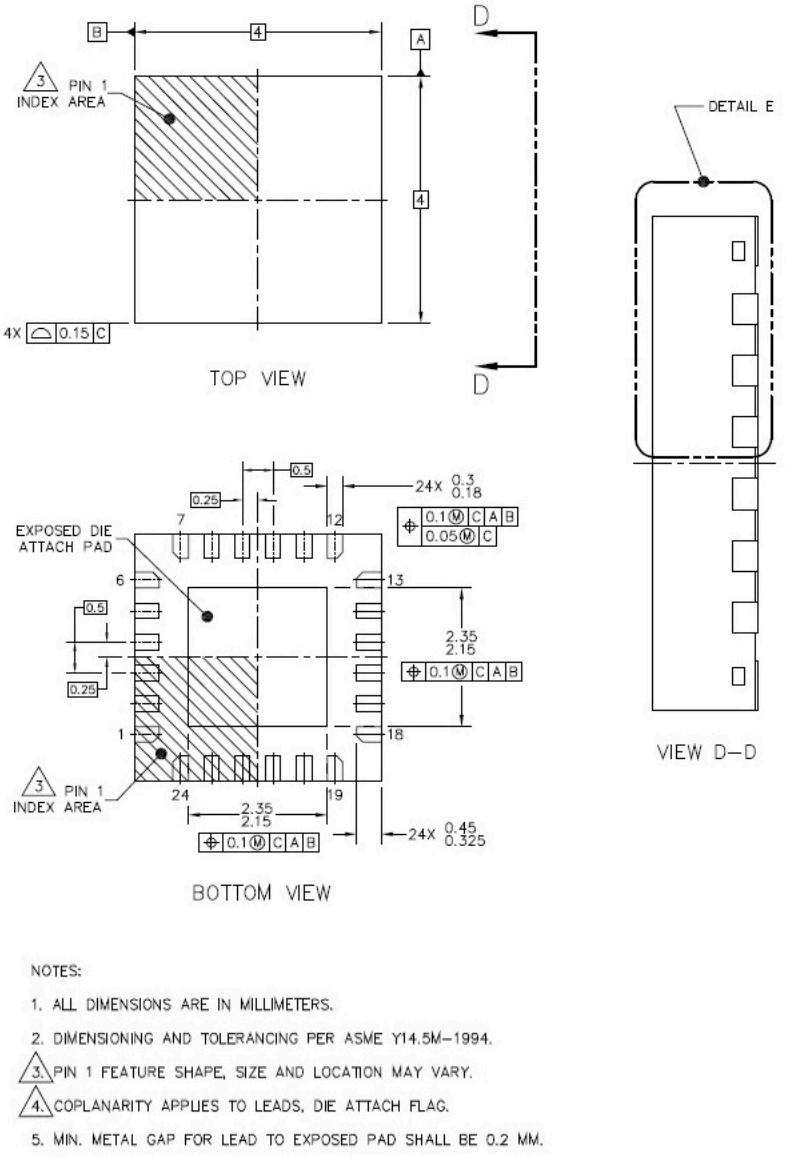

Figure 61. 4mm x 4mm QFN-24 mechanical drawing

Note: *All dimensions in mm. See Section 9.2 "Package markings" for package marking and pin 1 location.*

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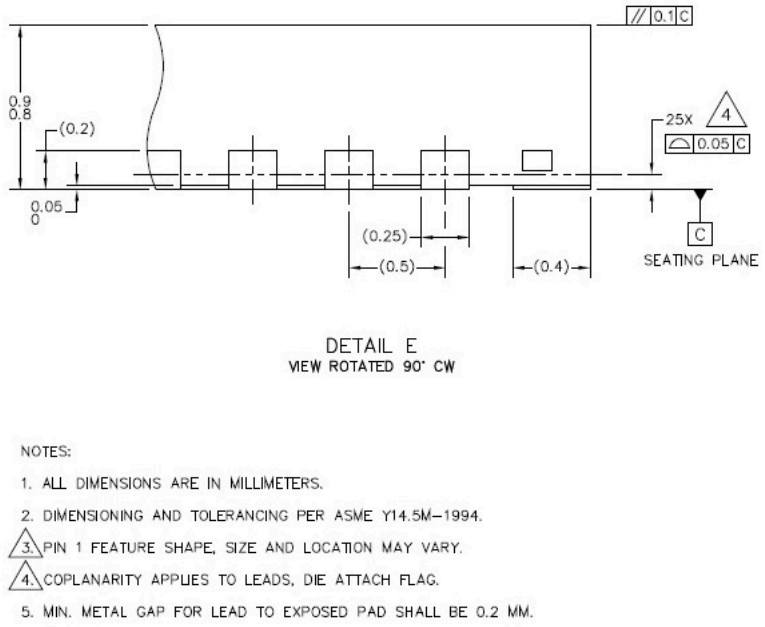

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

Figure 62. 4mm x 4mm QFN-24 mechanical drawing - Details E

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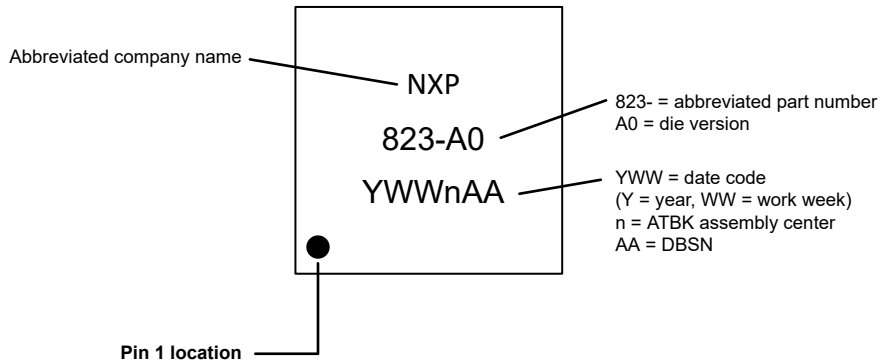
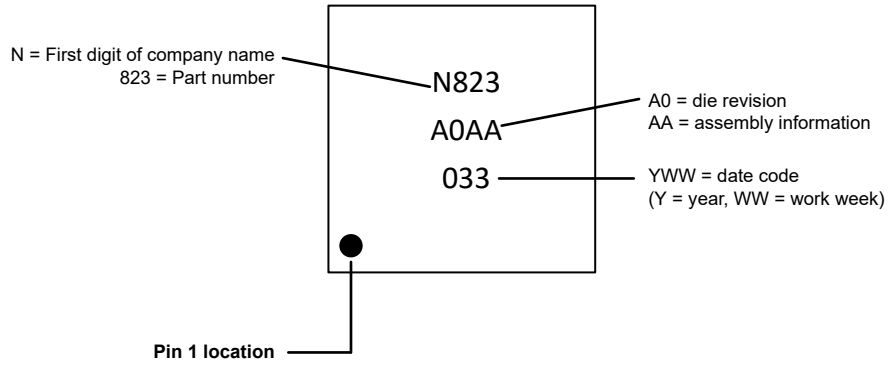
9.2 Package markings



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 63. Package marking and pin 1 location - QFN package



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 64. Package marking and pin 1 location - WLCSP package

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10 PM823 register sets

10.1 Register conventions

The register tables include the following information:

- **Register address**: included in the table caption
- **Bits**: Bits and/or bit fields
- **Type**: Read (R), write (W), read/write (RW)
- **Default**: Power-on hardware reset default value
- **Description**: Description of the bit or bit field and definition of the values

10.2 Register map

Table 12. Register map

Register name	Register address	Read / Write
Buck1 Active Mode 0 and Mode 3 Output Voltage Control	0x00	W
Buck1 Active Mode 1 Output Voltage Control	0x01	W
Buck1 Sleep Mode Output Voltage Control	0x02	W
Buck2 Output Voltage Control	0x03	W
LDO Output Voltage Control	0x04	W
MISC Control	0x05	W

10.3 Register descriptions

10.3.1 Buck1 active mode 1 and mode 3 output voltage control

Table 13. Register 0x00

Bit	Field	Type	Default	Description
D[7]	EN_BK1_ ENABLE	W	1	**Buck1 Software Enable** 1: Buck1 is enabled 0: Buck1 is disabled
D[6:5]	BK1_ VOUT_ RANGE	W	00	**Buck1 V_{OUT}** Range Used to set the Buck1 output voltage range 00: 0.6V ~ 1.375V 01: 1.4V ~ 2.85V 10: 2.9V ~ 3.3V 11: Reserved

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Table 13. Register 0x00*...continued*

Bit	Field	Type	Default	Description		
D[4:0]	BK1_M0_VOUT	W	1_0100	**Buck1 Active Mode 0 Output Voltage** When the DVS1 input pin is high, Buck1 is set to Active Mode 0 and these register bits with the BK1_VOUT_RANGE register are used to set the Buck1 output voltage		
				BK1_VOUT_RANGE = 00	**BK1_VOUT_RANGE = 01**	**BK1_VOUT_RANGE = 10**
				0_0000 = 0.6V 0_0001 = 0.625V 0_0010 = 0.65V 0_0011 = 0.675V 0_0100 = 0.7V 0_0101 = 0.725V 0_0110 = 0.75V 0_0111 = 0.775V 0_1000 = 0.8V 0_1001 = 0.825V 0_1010 = 0.85V 0_1011 = 0.875V 0_1100 = 0.9V 0_1101 = 0.925V 0_1110 = 0.95V 0_1111 = 0.975V 1_0000 = 1.0V 1_0001 = 1.025V 1_0010 = 1.05V 1_0011 = 1.075V 1_0100 = 1.1V 1_0101 = 1.125V 1_0110 = 1.15V 1_0111 = 1.175V 1_1000 = 1.2V 1_1001 = 1.225V 1_1010 = 1.25V 1_1011 = 1.275V 1_1100 = 1.3V 1_1101 = 1.325V 1_1110 = 1.35V 1_1111 = 1.375V	0_0000 = 1.4V 0_0001 = 1.425V 0_0010 = 1.45V 0_0011 = 1.475V 0_0100 = 1.5V 0_0101 = 1.55V 0_0110 = 1.6V 0_0111 = 1.65V 0_1000 = 1.7V 0_1001 = 1.75V 0_1010 = 1.8V 0_1011 = 1.85V 0_1100 = 1.9V 0_1101 = 1.95V 0_1110 = 2.0V 0_1111 = 2.05V 1_0000 = 2.1V 1_0001 = 2.15V 1_0010 = 2.2V 1_0011 = 2.25V 1_0100 = 2.3V 1_0101 = 2.35V 1_0110 = 2.4V 1_0111 = 2.45V 1_1000 = 2.5V 1_1001 = 2.55V 1_1010 = 2.6V 1_1011 = 2.65V 1_1100 = 2.7V 1_1101 = 2.75V 1_1110 = 2.8V 1_1111 = 2.85V	0_0000 = 2.9V 0_0001 = 2.95V 0_0010 = 3.0V 0_0011 = 3.05V 0_0100 = 3.1V 0_0101 = 3.15V 0_0110 = 3.2V 0_0111 = 3.25V 0_1000 = 3.3V Others Reserved

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10.3.2 Buck1 active mode 2 output voltage control

Table 14. Register 0x01

Bit	Field	Type	Default	Description		
D[7:5]	Reserved	W	000	**Reserved** Set bits to 0 when written		
D[4:0]	BK1_M1_VOUT	W	1_0100	**Buck1 Active Mode 1 Output Voltage** When the DVS1=0 and DVS0=1 register bit is set to 1, Buck1 is set to Active Mode 0 and these register bits with the BK1_VOUT_RANGE register are used to set the Buck1 output voltage		
				BK1_VOUT_RANGE = 00	**BK1_VOUT_RANGE = 01**	**BK1_VOUT_RANGE = 10**
				0_0000 = 0.6V 0_0001 = 0.625V 0_0010 = 0.65V 0_0011 = 0.675V 0_0100 = 0.7V 0_0101 = 0.725V 0_0110 = 0.75V 0_0111 = 0.775V 0_1000 = 0.8V 0_1001 = 0.825V 0_1010 = 0.85V 0_1011 = 0.875V 0_1100 = 0.9V 0_1101 = 0.925V 0_1110 = 0.95V 0_1111 = 0.975V 1_0000 = 1.0V 1_0001 = 1.025V 1_0010 = 1.05V 1_0011 = 1.075V 1_0100 = 1.1V 1_0101 = 1.125V 1_0110 = 1.15V 1_0111 = 1.175V 1_1000 = 1.2V 1_1001 = 1.225V 1_1010 = 1.25V 1_1011 = 1.275V 1_1100 = 1.3V 1_1101 = 1.325V 1_1110 = 1.35V 1_1111 = 1.375V	0_0000 = 1.4V 0_0001 = 1.425V 0_0010 = 1.45V 0_0011 = 1.475V 0_0100 = 1.5V 0_0101 = 1.55V 0_0110 = 1.6V 0_0111 = 1.65V 0_1000 = 1.7V 0_1001 = 1.75V 0_1010 = 1.8V 0_1011 = 1.85V 0_1100 = 1.9V 0_1101 = 1.95V 0_1110 = 2.0V 0_1111 = 2.05V 1_0000 = 2.1V 1_0001 = 2.15V 1_0010 = 2.2V 1_0011 = 2.25V 1_0100 = 2.3V 1_0101 = 2.35V 1_0110 = 2.4V 1_0111 = 2.45V 1_1000 = 2.5V 1_1001 = 2.55V 1_1010 = 2.6V 1_1011 = 2.65V 1_1100 = 2.7V 1_1101 = 2.75V 1_1110 = 2.8V 1_1111 = 2.85V	0_0000 = 2.9V 0_0001 = 2.95V 0_0010 = 3.0V 0_0011 = 3.05V 0_0100 = 3.1V 0_0101 = 3.15V 0_0110 = 3.2V 0_0111 = 3.25V 0_1000 = 3.3V Others Reserved

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10.3.3 Buck1 sleep mode output voltage control

Table 15. Register 0x02

Bit	Field	Type	Default	Description		
D[7:5]	Reserved	W	000	**Reserved** Set bits to 0 when written		
D[4:0]	BK1_SLP_VOUT	W	1_0100	**Buck1 Sleep Mode Output Voltage** When the DVS1=0 and DVS0=0 and DVS_EN register bit is set to 1, Buck1 is set to Active Mode 0 and these register bits with the BK1__VOUT_RANGE register are used to set the Buck1 output voltage		
				BK1_VOUT_RANGE = 00	**BK1_VOUT_RANGE = 01**	**BK1-VOUT_RANGE = 10**
				0_0000 = 0.6V 0_0001 = 0.625V 0_0010 = 0.65V 0_0011 = 0.675V 0_0100 = 0.7V 0_0101 = 0.725V 0_0110 = 0.75V 0_0111 = 0.775V 0_1000 = 0.8V 0_1001 = 0.825V 0_1010 = 0.85V 0_1011 = 0.875V 0_1100 = 0.9V 0_1101 = 0.925V 0_1110 = 0.95V 0_1111 = 0.975V 1_0000 = 1.0V 1_0001 = 1.025V 1_0010 = 1.05V 1_0011 = 1.075V 1_0100 = 1.1V 1_0101 = 1.125V 1_0110 = 1.15V 1_0111 = 1.175V 1_1000 = 1.2V 1_1001 = 1.225V 1_1010 = 1.25V 1_1011 = 1.275V 1_1100 = 1.3V 1_1101 = 1.325V 1_1110 = 1.35V 1_1111 = 1.375V	0_0000 = 1.4V 0_0001 = 1.425V 0_0010 = 1.45V 0_0011 = 1.475V 0_0100 = 1.5V 0_0101 = 1.55V 0_0110 = 1.6V 0_0111 = 1.65V 0_1000 = 1.7V 0_1001 = 1.75V 0_1010 = 1.8V 0_1011 = 1.85V 0_1100 = 1.9V 0_1101 = 1.95V 0_1110 = 2.0V 0_1111 = 2.05V 1_0000 = 2.1V 1_0001 = 2.15V 1_0010 = 2.2V 1_0011 = 2.25V 1_0100 = 2.3V 1_0101 = 2.35V 1_0110 = 2.4V 1_0111 = 2.45V 1_1000 = 2.5V 1_1001 = 2.55V 1_1010 = 2.6V 1_1011 = 2.65V 1_1100 = 2.7V 1_1101 = 2.75V 1_1110 = 2.8V 1_1111 = 2.85V	0_0000 = 2.9V 0_0001 = 2.95V 0_0010 = 3.0V 0_0011 = 3.05V 0_0100 = 3.1V 0_0101 = 3.15V 0_0110 = 3.2V 0_0111 = 3.25V 0_1000 = 3.3V Others Reserved

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10.3.4 Buck2 output voltage control

Table 16. Register 0x03

Bit	Field	Type	Default	Description		
D[7]	EN_BK2_ ENABLE	W	1	**Buck2 Software Enable** 1: Buck2 is enabled 0: Buck2 is disabled		
D[6:0]	BK2_ VOUT	W	1_0100	**Buck2 Output Voltage** Used to control the Buck2 output voltage		
				0_0000 = 0.6V 0_0001 = 0.625V 0_0010 = 0.65V 0_0011 = 0.675V 0_0100 = 0.7V 0_0101 = 0.725V 0_0110 = 0.75V 0_0111 = 0.775V 0_1000 = 0.8V 0_1001 = 0.825V 0_1010 = 0.85V 0_1011 = 0.875V 0_1100 = 0.9V 0_1101 = 0.925V 0_1110 = 0.95V 0_1111 = 0.975V 1_0000 = 1.0V 1_0001 = 1.025V 1_0010 = 1.05V 1_0011 = 1.075V 1_0100 = 1.1V 1_0101 = 1.125V 1_0110 = 1.15V 1_0111 = 1.175V 1_1000 = 1.2V 1_1001 = 1.225V 1_1010 = 1.25V 1_1011 = 1.275V 1_1100 = 1.3V 1_1101 = 1.325V 1_1110 = 1.35V 1_1111 = 1.375V	0_0000 = 1.4V 0_0001 = 1.425V 0_0010 = 1.45V 0_0011 = 1.475V 0_0100 = 1.5V 0_0101 = 1.55V 0_0110 = 1.6V 0_0111 = 1.65V 0_1000 = 1.7V 0_1001 = 1.75V 0_1010 = 1.8V 0_1011 = 1.85V 0_1100 = 1.9V 0_1101 = 1.95V 0_1110 = 2.0V 0_1111 = 2.05V 1_0000 = 2.1V 1_0001 = 2.15V 1_0010 = 2.2V 1_0011 = 2.25V 1_0100 = 2.3V 1_0101 = 2.35V 1_0110 = 2.4V 1_0111 = 2.45V 1_1000 = 2.5V 1_1001 = 2.55V 1_1010 = 2.6V 1_1011 = 2.65V 1_1100 = 2.7V 1_1101 = 2.75V 1_1110 = 2.8V 1_1111 = 2.85V	0_0000 = 2.9V 0_0001 = 2.95V 0_0010 = 3.0V 0_0011 = 3.05V 0_0100 = 3.1V 0_0101 = 3.15V 0_0110 = 3.2V 0_0111 = 3.25V 0_1000 = 3.3V Others Reserved

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10.3.5 LDO output voltage control

Table 17. Register 0x04

Bit	Field	Type	Default	Description
D[7:5]	Reserved	W	000	**Reserved** Set bits to 0 when written
D[4]	EN_LDO	W	1	**LDO Software Enable** 1: LDO is enabled 0: LDO is disabled
D[3:0]	LDO_VOUT	W	1000	**LDO Output Voltage Setting** Used to set the LDO output voltage as follows...
				0000 = 1.6V 0001 = 1.625V 0010 = 1.65V 0011 = 1.675V 0100 = 1.7V 0101 = 1.725V 0110 = 1.75V 0111 = 1.775V 1000 = 1.8V 1001 = 1.825V 1010 = 1.85V 1011 = 1.875V 1100 = 1.9V 1101 = 1.925V 1110 = 1.95V 1111 = 1.975V

10.3.6 Miscellaneous control

Table 18. Register 0x05

Bit	Field	Type	Default	Description
D[7:3]	Reserved	W	0000_0	**Reserved** Set bits to 0 when written
D[2]	DVS_EN	W	0	**DVS Enable** 1: DVS is enabled 0: DVS is disabled
D[1]	FPWM_BK1	W	0	**Buck1 FPWM** 1: When set, forces PWM mode 0: Auto switch between PWM and PFM modes
D[0]	FPWM_BK2	W	0	**Buck2 FPWM** 1: When set, forces PWM mode 0: Auto switch between PWM and PFM modes

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11 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PM823 v4.0	20220623	Product data sheet	-	PM823 v3.0
Modifications	Changed the document confidentiality level from "Company Confidential" to "Public". No changes in the content.			
PM823 v3.0	20210524	Product data sheet	-	PM823 v2.0
Modifications	**Signal description** • Figure 4 "1.26 mm x 1.545 mm WLCSP-12 lead, pop (see through) view": corrected **Application information** • Figure 53 "PCB schematic - QFN package": corrected **Package information** • Section 9.2 "Package markings": updated with the marking of QFN (Figure 63) and WLCSP (Figure 64) packages			
PM823 v2.0	20210512	Product data sheet	-	PM823 v1.0
Modifications	**Signal description** • Figure 5 "4 mm x 4 mm QFN-24 in 0.5 mm pitch pin configuration, top (see through) view": corrected			
PM823 v1.0	20201118	Objective data sheet	-	-

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12 Legal information

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".
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Tables

Tab. 1. Part order options 4
Tab. 2. Pin types 6
Tab. 3. Pin description 7
Tab. 4. Absolute maximum ratings 11
Tab. 5. Recommended operating conditions 11
Tab. 6. External passive components 12
Tab. 7. Electrical characteristics 13
Tab. 8. Operating mode selections 20
Tab. 9. DVS output voltage settings 21
Tab. 10. BOM for WLCSP package 41
Tab. 11. BOM for QFN Package 42
Tab. 12. Register map 47
Tab. 13. Register 0x00 47
Tab. 14. Register 0x01 49
Tab. 15. Register 0x02 50
Tab. 16. Register 0x03 51
Tab. 17. Register 0x04 52
Tab. 18. Register 0x05 52
Tab. 19. Revision history 53

Figures

Fig. 1. PM823 typical application-QFN package option 2
Fig. 2. PM823 typical application-WLCSP package option 3
Fig. 3. Part numbering scheme 4
Fig. 4. 1.26 mm x 1.545 mm WLCSP-12 lead, pop (see through) view 5
Fig. 5. 4 mm x 4 mm QFN-24 in 0.5 mm pitch pin configuration, top (see through) view 6
Fig. 6. Block diagram 17
Fig. 7. Serial programmability 18
Fig. 8. Power-up sequence timing diagram - WLCSP package option 19
Fig. 9. UVLO and OVP waveforms 22
Fig. 10. Startup 24
Fig. 11. UVLO / OVP Thresholds 24
Fig. 12. Buck1 short circuit 24
Fig. 13. Buck2 short circuit 24
Fig. 14. Buck1 (1.1V) load transient response 100 mA to 750 mA 25
Fig. 15. Buck1 (1.1V) load transient response 750 mA to 1.5A 25
Fig. 16. Buck2 (2.2V) load transient response 100 mA to 750 mA 25
Fig. 17. Buck2 (2.2V) load transient response 750 mA to 1.5A 25
Fig. 18. Buck1 (1.1V) PFM Output Ripples at 25 mA 26
Fig. 19. Buck1 (1.1V) PWM Output Ripples at 1.5A 26
Fig. 20. Buck2 (2.2V) PFM Output Ripples at 45 mA 26
Fig. 21. Buck2 (2.2V) PWM Output Ripples at 1.5A 26
Fig. 22. Buck1 (1.1V) efficiency vs output current WLCSP-12 27
Fig. 23. Buck2 (2.2V) efficiency vs output current WLCSP-12 27
Fig. 24. Buck1 (3.3V) efficiency vs output current QFN-24 27
Fig. 25. Buck2 (1.8V) efficiency vs output current QFN-24 27
Fig. 26. Buck1 (1.1V) output voltage vs output current WLCSP-12 27
Fig. 27. Buck2 (2.2V) output voltage vs output current WLCSP-12 27
Fig. 28. Buck1 (3.3V) output voltage vs output current QFN-24 27
Fig. 29. Buck2 (1.8V) output voltage vs output current QFN-24 27
Fig. 30. Buck1 output voltage vs input voltage WLCSP-12 28
Fig. 31. Buck2 Output Voltage vs Input Voltage WLCSP-12 28
Fig. 32. Quiescent Current vs Input Voltage For Active Mode 3 28
Fig. 33. Buck1 high side RDS(ON) vs. input voltage WLCSP-12 28
Fig. 34. Buck2 high side RDS(ON) vs. input voltage WLCSP-12 28
Fig. 35. Buck1 low side RDS(ON) vs. input voltage WLCSP-12 28
Fig. 36. Buck2 low side RDS(ON) vs. input voltage WLCSP-12 28
Fig. 37. Buck1 high side RDS(ON) vs. input voltage QFN-24 29
Fig. 38. Buck2 high side RDS(ON) vs. input voltage QFN-24 29
Fig. 39. Buck1 low side RDS(ON) vs. input voltage QFN-24 29
Fig. 40. Buck2 low side RDS(ON) vs. input voltage QFN-24 29
Fig. 41. Buck1 Output Voltage Error vs Temperature 29
Fig. 42. Buck2 Output Voltage Error vs Temperature 29
Fig. 43. Quiescent current vs temperature for active mode 3 29
Fig. 44. Buck1 high side RDS(ON) vs. temperature WLCSP-12 30
Fig. 45. Buck2 high side RDS(ON) vs. temperature WLCSP-12 30
Fig. 46. Buck1 low side RDS(ON) vs. temperature WLCSP-12 30
Fig. 47. Buck2 low side RDS(ON) vs. temperature WLCSP-12 30

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Fig. 48. Buck1 high side RDS(ON) vs. temperature QFN-24 30
Fig. 49. Buck2 high side RDS(ON) vs. temperature QFN-24 30
Fig. 50. Buck1 low side RDS(ON) vs. temperature QFN-24 30
Fig. 51. Buck2 low side RDS(ON) vs. temperature QFN-24 30
Fig. 52. PCB schematic - WLCSP package 33
Fig. 53. PCB schematic - QFN package 34
Fig. 54. Top traces, vias, and copper (not to scale) 35
Fig. 55. Layer 2 vias and copper (not to scale) 36
Fig. 56. Layer 3 vias and copper (not to scale) 37
Fig. 57. Bottom traces, vias, and copper (not to scale) 38
Fig. 58. Top traces, vias, and copper (not to scale) 39
Fig. 59. Bottom traces, vias, and copper (not to scale) 40
Fig. 60. 1.260mm x 1.545mm WLCSP-12 mechanical drawing 43
Fig. 61. 4mm x 4mm QFN-24 mechanical drawing 44
Fig. 62. 4mm x 4mm QFN-24 mechanical drawing - Details E 45
Fig. 63. Package marking and pin 1 location - QFN package 46
Fig. 64. Package marking and pin 1 location - WLCSP package 46

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Contents

1 Product overview 1
2 Ordering information 4
3 Signal description 5
3.1 Pin configuration 5
3.1.1 12-lead WLCSP configuration 5
3.1.2 24-pin QFN configuration 6
3.2 Pin descriptions 6
4 Electrical specifications 11
4.1 Absolute maximum ratings 11
4.2 Recommended operating conditions 11
4.3 External passive components 12
4.4 Electrical characteristics 13
5 Functional description 16
5.1 Overview 16
5.2 Serial interface (1-wire) 18
5.3 Soft start 19
5.4 Power-up sequence 19
5.5 Power good 20
5.6 Operating modes 20
5.7 DVS output voltage settings 21
5.8 Sleep mode 21
5.9 Under voltage lock-out (UVLO) 22
5.10 Over voltage protection (OVP) 22
5.11 Over-temperature thermal shutdown (OTS) 23
6 Functional characteristics 24
6.1 Start-up waveforms 24
6.2 Load transient waveforms 25
6.3 Switching waveforms 26
7 Typical characteristics 27
8 Application information 31
8.1 PC board layout considerations and guidelines 31
8.2 PCB schematics 33
8.3 PCB layout examples 34
8.3.1 PCB layout for WLCSP package 35
8.3.2 PCB layout for QFN package 39
8.4 Bill of materials (BOM) 41
9 Package information 43
9.1 Package mechanical drawings 43
9.2 Package markings 46
10 PM823 register sets 47
10.1 Register conventions 47
10.2 Register map 47
10.3 Register descriptions 47
10.3.1 Buck1 active mode 1 and mode 3 output voltage control 47
10.3.2 Buck1 active mode 2 output voltage control 49
10.3.3 Buck1 sleep mode output voltage control 50
10.3.4 Buck2 output voltage control 51
10.3.5 LDO output voltage control 52
10.3.6 Miscellaneous control 52
11 Revision history 53
12 Legal information 54

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