TEA19162HT/2

PFC controller

Rev. 1 — 25 September 2018 Product data sheet

1 General description

The TEA19162HT and TEA19161T are combined controller (combo) ICs for resonant topologies including PFC. They provide high efficiency at all power levels. Together with the TEA1995T dual LLC resonant SR controller, a cost-effective resonant power supply can be built. This power supply meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design Directive of the European Union, the European Code of Conduct, and other guidelines.

The TEA19162HT is a Power Factor Correction (PFC) controller. The IC communicates with the TEA19161T on start-up sequence and protections. It also enables a fast latch reset mechanism. To maximize the overall system efficiency, the TEA19161T allows setting the TEA19162HT PFC to burst mode at a low output power level.

Using the TEA19161T and TEA19162HT combo together with the TEA1995T secondary synchronous rectifier controller, a highly efficient and reliable power supply can be designed with a minimum of external components. The target output power is between 90 W and 500 W.

The system provides a very low no-load input power (< 75 mW; total system including the TEA19161T/TEA19162HT combo and the TEA1995T) and high efficiency from minimum to maximum load. So, no additional low-power supply is required.

2 Features and benefits

2.1 Distinctive features

- Complete functionality as TEA19161T/TEA19162HT combo
- Integrated X-capacitor discharge without additional external components
- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Integrated soft start and soft stop
- Accurate boost voltage regulation

2.2 Green features

- Valley/zero voltage switching for minimum switching losses
- Frequency limitation to reduce switching losses
- Reduced supply current (200 µA) when in burst mode

2.3 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection with demagnetization detection
- Accurate OverVoltage Protection (OVP)
- Open-Loop Protection (OLP)
- Short-Circuit Protection (SCP)
- Internal and external IC OverTemperature Protection (OTP)
- Low and adjustable OverCurrent Protection (OCP) trip level
- Adjustable brownin/brownout protection
- Supply UnderVoltage Protection (UVP)

3 Applications

- Desktop and all-in-one PCs
- LCD television
- Notebook adapter
- Printers
- Gaming console power supplies

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA19162HT/2	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 Marking

Table 2. Ordering information

Type number	Marking code
TEA19162HT/2	A19162H

6 Block diagram

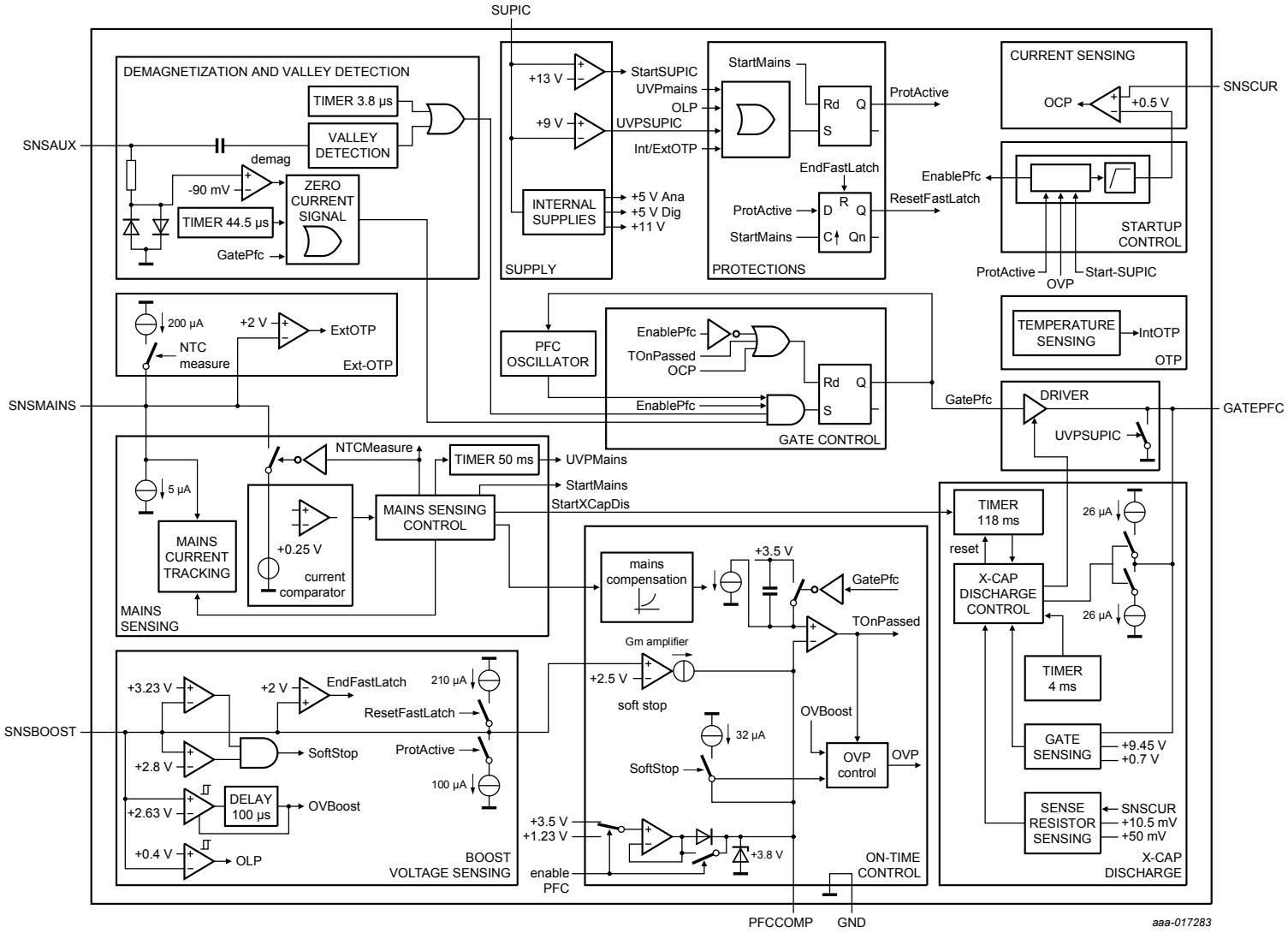


Figure 1. TEA19162HT block diagram

7 Pinning information

7.1 Pinning

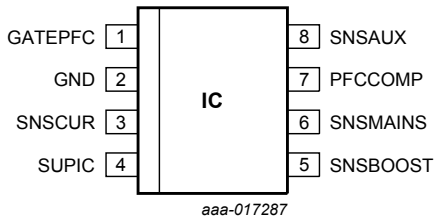


Figure 2. Pin configuration (SOT96-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GATEPFC	1	gate driver output for PFC
GND	2	ground
SNSCUR	3	programmable current sense input for PFC
SUPIC	4	supply voltage
SNSBOOST	5	sense input for PFC output voltage
SNSMAINS	6	sense input for mains voltage
PFCCOMP	7	frequency compensation pin for PFC
SNSAUX	8	input from auxiliary winding for demagnetization timing and valley detection for PFC

8 Functional description

8.1 General control

The TEA19162HT is a controller for a power factor correction circuit. Figure 3 shows a typical configuration.

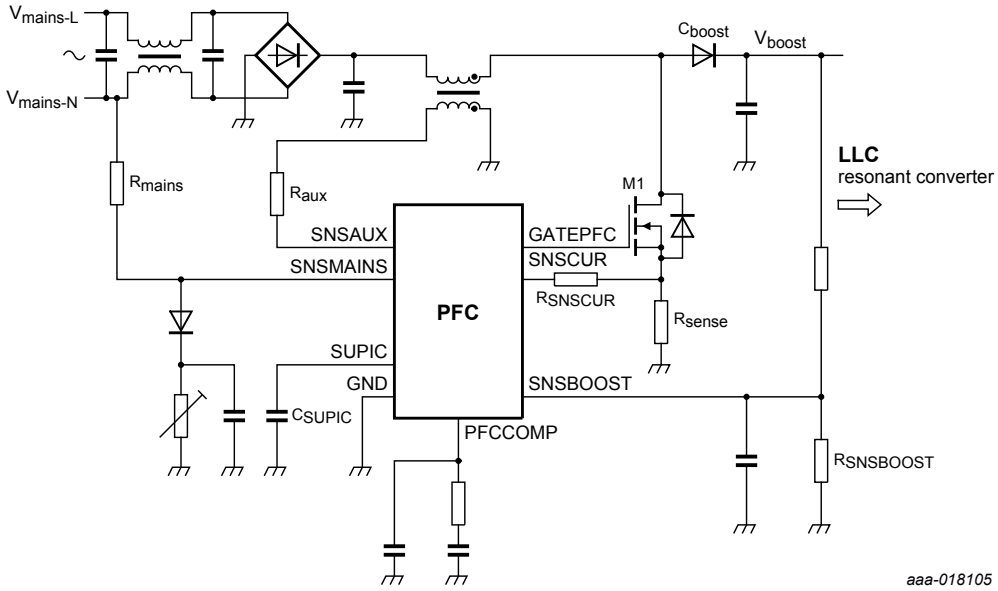


Figure 3. TEA19162HT typical configuration

8.2 Supply voltage and start-up

When using the TEA19162HT (PFC) together with the TEA19161T (LLC), connect the SUPIC pin of the TEA19162HT to the SUPIC pin of the TEA19161T. The LLC controller then supplies the PFC either via the high-voltage supply pin of the TEA19161T (SUPHV) or via the primary auxiliary winding.

To enable the PFC, the SUPIC voltage must exceed the $V_{start(SUPIC)}$ level (13 V typical). Although the $V_{start(SUPIC)}$ level of the LLC is higher than the $V_{start(SUPIC)}$ level of the PFC, the system ensures that both converters (PFC and LLC) start up at the same time. Therefore, the LLC initially pulls down the SNSBOOST pin, disabling the PFC until the SUPIC voltage reaches the $V_{start(SUPIC)}$ level of the LLC.

When both conditions are met and the SNSMAINS is above the brownin level, the PFC starts up via an internal soft start (see Figure 4).

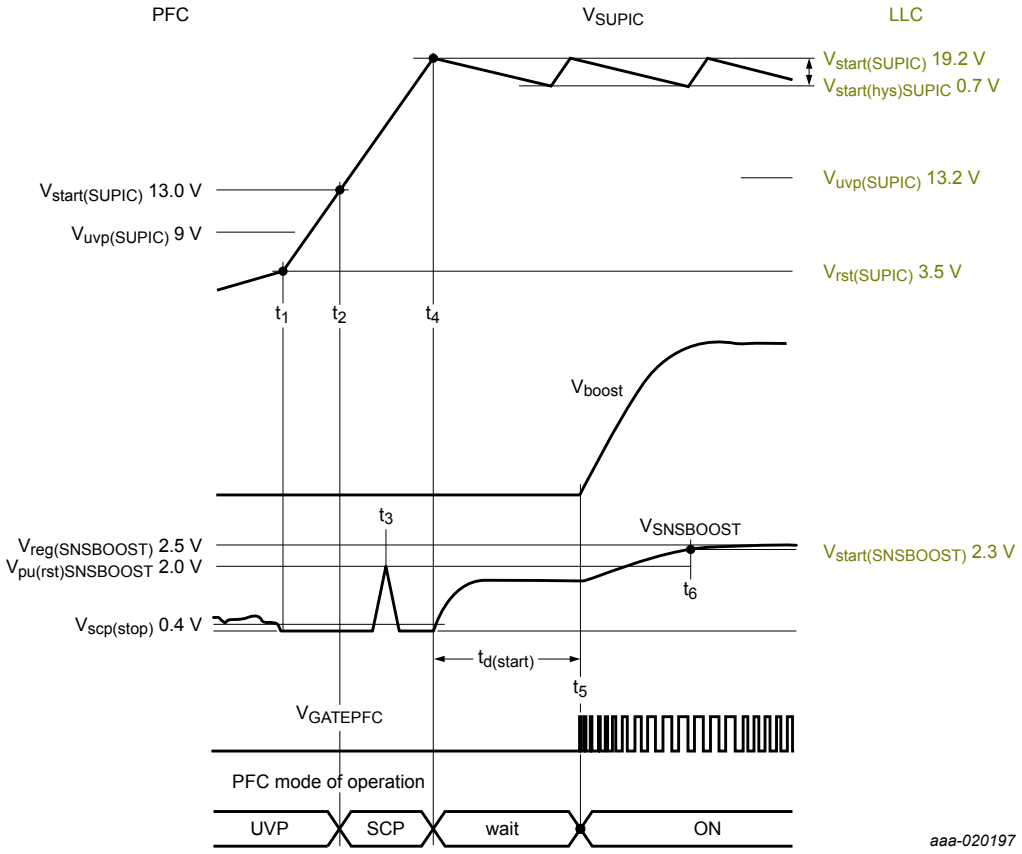


Figure 4. Start-up of the PFC and LLC

The exact start-up sequence of the PFC depends on the availability of start-up conditions (brownin level, $V_{start(SUPIC)}$ of the PFC, and $I_{en(PFC)}$).

Before t1, the SUPIC voltage is below the UVP level of the PFC and LLC. When the LLC reaches a minimum supply voltage level (t1), the LLC pulls down the SNSBOOST pin to disable the PFC.

At t2, the SUPIC voltage reaches the start level of the PFC converter. However, as the LLC pulls low the SNSBOOST to below the PFC short protection level, the PFC is still off. When the mains voltage exceeds the brownin level, the PFC resets its latched protection by pulling $V_{SNSBOOST}$ to the $V_{pu(rst)SNSBOOST}$ level (t3). However, the LLC returns it to the protection mode. When at t4 the SUPIC voltage reaches the start level of the LLC, the SNSBOOST is released. The SNSBOOST voltage increases because of the resistive divider which is connected to the PFC bus voltage. To ensure that this voltage is representative of the V_{boost} voltage before the system actually starts to switch, an additional delay ($t_{d(start)}$; 3.62 ms) is active before the PFC starts switching (t5).

Another important condition for the PFC start is a precharge of the compensation circuitry connected to the PFCCOMP pin. This condition is met when the current out of the PFCCOMP pin < $|I_{en(PFCCOMP)}|$.

When at t6 the SNSBOOST voltage reaches the start level of the LLC ($V_{start(SNSBOOST)}$), the LLC converter starts to switch.

When $V_{SUPIC} < V_{uvp(SUPIC)}$, the PFC controller stops switching immediately.

8.3 Protections

Table 4 gives an overview of the available protections.

Table 4. Protections overview

Protection	Description	Action	LLC [1]	
UVP-SUPIC	undervoltage protection SUPIC	PFC = off; restart when $V_{SUPIC} > V_{start(SUPIC)}$; SNSBOOST pulled low, disabling the LLC.	off	Section 8.2
OTP-internal	internal overtemperature protection	latched; SNSBOOST pulled low, disabling the LLC.	off	Section 8.3.1
OTP-external	external overtemperature protection	latched; SNSBOOST pulled low, disabling the LLC.	off	Section 8.3.2
brownout-mains	undervoltage protection mains	PFC = off; restart when $I_{SNSMAINS} > I_{bi}$ [2]	-	Section 8.3.2
SoftStop-OVP-SNSBOOST	overvoltage protection boost voltage followed by a soft stop	PFC = off via soft stop; restart when $V_{SNSBOOST} < V_{ovp(start)}$	-	Section 8.3.3
OVP-SNSBOOST	overvoltage protection boost voltage	PFC = off; restart when $V_{SNSBOOST} < V_{ovp(SNSBOOST)}$	-	Section 8.3.4
SCP-SNSBOOST	short-circuit protection	PFC = off; restart when $V_{SNSBOOST} > V_{scp(start)}$	-	Section 8.3.5
OLP-PFC	open-loop protection	PFC = off; restart when $V_{SNSBOOST} > V_{scp(start)}$	-	Section 8.3.5
OCP	overcurrent protection	PFC MOSFET switched off,continue operation	-	Section 8.3.6

[1] [2] Some protections also disable the LLC (see Section 8.5.1).
[2] At start-up, the PFC disables the LLC converter until the mains voltage exceeds the brownin level.

8.3.1 Internal OverTemperature Protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature ($T_{pl(IC)}$), the IC stops switching.

The internal overtemperature protection is a latched protection. It also disables the LLC converter by pulling down the SNSBOOST pin.

8.3.2 Brownin/brownout and external overtemperature protection

On the TEA19162HT, the mains measurement and external temperature are combined at the SNSMAINS pin (see Figure 5).

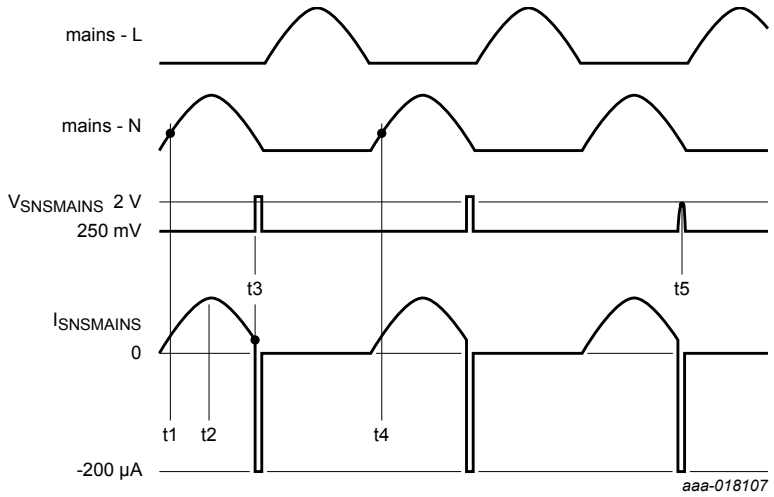


Figure 5. Mains and external OTP measurement

At t1, the voltage at the SNSMAINS pin is internally regulated to $V_{regd(SNSMAINS)}$ (250 mV). The current into the SNSMAINS pin is a measure of the system input mains voltage. The TEA19162HT continuously measures the SNSMAINS current and waits until it detects a peak in the measured current (t2). This peak current value is internally stored and used as an input for the brownout/brownin detection and the mains compensation.

When, at t3, the current into the SNSMAINS pin is well below the brownin level ($< I_{en(NTC)}$), the controller starts to measure the value of the external NTC. The external NTC is measured by sourcing a current ($I_{o(SNSMAINS)}$) out of the SNSMAINS pin. When, after a maximum measuring time of $t_{det(NTC)max}$ (1 ms), the voltage remains below $V_{det(SNSMAINS)}$ during four consecutive NTC measurements, the OTP protection is triggered (t5).

To prevent the PFC from operating at very low mains input voltages, the PFC stops switching when the measured peak current drops to below I_{bo}. When the measured current exceeds I_{bi}, the PFC restarts with a soft start.

8.3.3 Soft stop overvoltage protection (SNSBOOST pin)

When the SNSBOOST voltage is between the $V_{det(L)SNSBOOST}$ and $V_{det(H)SNSBOOST}$, the TEA19162HT stops switching via a soft stop. The TEA19161T uses this function to force the TEA19162HT to operate in burst mode with a specific duty cycle (see Section 8.5.2). Audible noise is avoided because at the end of a switching period, the PFC stops via a soft stop. After an OVP event, the system always starts via a soft start.

8.3.4 Overvoltage protection (SNSBOOST pin)

To prevent output overvoltage during load steps and mains transients, an overvoltage protection circuit is built in.

When the voltage on the SNSBOOST pin exceeds the $V_{ovp(stop)}$ level and is outside the $V_{det(L)SNSBOOST}$ and $V_{det(H)SNSBOOST}$ window for a minimum period of $t_{d(ovp)}$ (100 µs), switching of the power factor correction circuit is inhibited. When the SNSBOOST pin voltage drops to below the $V_{ovp(start)}$ ($V_{ovp(stop)} - V_{hys(ovp)}$) level again, the switching of the PFC recommences. The IC always restarts with a soft start (see Section 8.4.1).

8.3.5 PFC open-loop protection (SNSBOOST pin)

The PFC does not start switching until the voltage on the SNSBOOST pin exceeds $V_{scp(start)}$. This function acts as short circuit protection for the boost voltage (SCP-SNSBOOST; see Table 4).

8.3.6 Overcurrent protection (SNSCUR pin)

Sensing the voltage across an external sense resistor, R_{sense}, on the source of the external MOSFET, limits the maximum peak current cycle-by-cycle. The voltage is measured via the SNSCUR pin.

8.3.7 Fast latch reset

The restart of the system after a protection is triggered depends on the type of protection. In a safe restart protection (only applicable for the LLC), the system typically restarts after the restart delay time (1 s).

It is different for latched protections. Typically, in a latched protection, the SUPIC must reach the undervoltage protection level to release the protection mode and to restart the system. The release/restart can only be achieved by disconnecting the mains.

In the protection mode, the TEA19161T regulates the voltage of the SUPIC pin to its start level. The PFC output capacitor supplies the SUPIC pin via the SUPHV pin of the TEA19161T. So it takes a long time before the voltage of the SUPIC pin drops below its undervoltage level after the mains is disconnected. To prevent this delay, a special fast latch reset function is implemented in the TEA19162HT, which also releases the protection mode when the mains is reconnected.

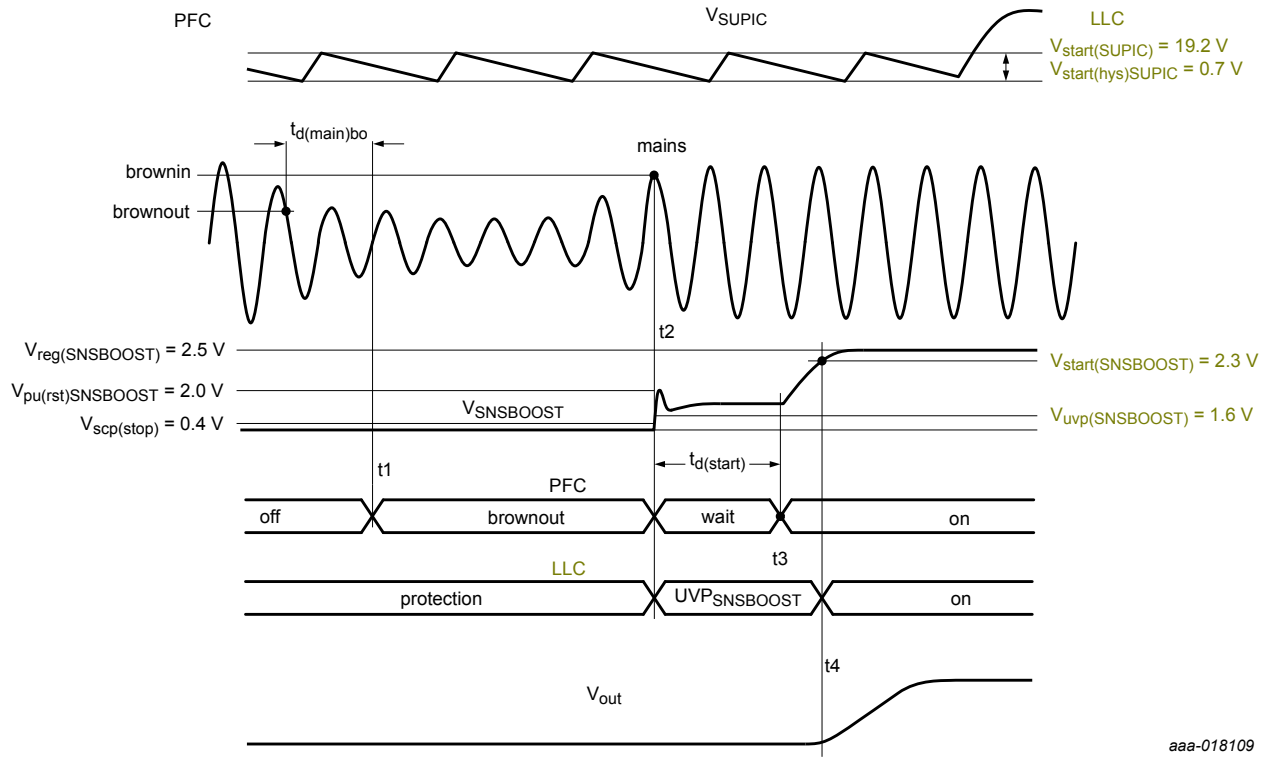


Figure 6. Fast latch reset

Before t1, the LLC (and/or PFC) is in a (latched) protection and pulls down the SNSBOOST pin, which also disables the PFC.

When the mains voltage drops to below the brownout level (I_{bo}) and the time $t_{d(det)bo}$ (50 ms) expires (t1), the PFC enters the brownout protection mode. When, in the brownout protection mode, the mains voltage increases again and exceeds the brownin level (I_{bi}; t2), the PFC pulls up the SNSBOOST voltage to the $V_{pu(rst)SNSBOOST}$ level (see Figure 6). Because the $V_{pu(rst)SNSBOOST}$ level of the PFC exceeds the $V_{uvp(SNSBOOST)}$ level of the LLC, the LLC converter resets the protection mode. However, switching is still inhibited as the SNSBOOST voltage remains below the start level ($V_{start(SNSBOOST)}$) of the LLC. The SUPIC voltage is still regulated to the $V_{start(SUPIC)}$ level of the LLC converter. To ensure that the voltage at the SNSBOOST pin accurately reflects the output voltage of the PFC, the PFC converter starts after a delay time ($t_{d(start)}$) (t3). The start of the PFC converter is followed by a start-up of the LLC converter (t4).

8.4 Power factor correction regulation

The power factor correction circuit operates in quasi-resonant or discontinuous conduction mode with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. To detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch, the voltage on the SNSAUX pin is used.

8.4.1 Soft start (SNSCUR pin)

To prevent audible transformer noise at start-up or during hiccup, the soft start function slowly increases the transformer peak current (see Figure 7).

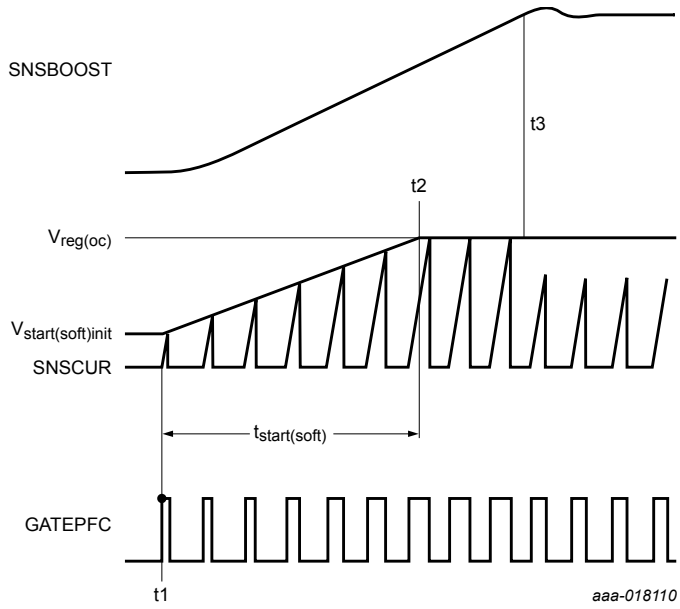


Figure 7. PFC start-up

At t1, all conditions to start up the PFC are fulfilled. The maximum voltage on the SNSCUR pin is limited to $V_{start(soft)init}$ (125 mV). When the PFC starts switching, the maximum SNSCUR voltage is increased to $V_{reg(oc)}$ within a time period of $t_{start(soft)}$ (3.62 ms) or until the t_{on} regulation limits the on-time of the PFC external MOSFET.

8.4.2 t_{on} control

The power factor correction circuit is operated in t_{on} control. The resulting mains harmonic reduction of a typical application is well within the class-D requirements.

The following circuits determine the on-time of the external PFC MOSFET:

- The error amplifier and the loop compensation which define the voltage on the PFCCOMP pin. At $V_{tonzero(PFCCOMP)}$ (3.5 V), the on-time is reduced to zero. At $V_{tonmax(PFCCOMP)}$ (1.23 V), the on-time is at a maximum.
- Mains compensation which uses the current through the SNSMAINS pin to represent the mains input voltage level.

8.4.3 PFC error amplifier (PFCCOMP and SNSBOOST pins)

The boost voltage is divided using a high-ohmic resistive divider and is supplied to the SNSBOOST pin. The transconductance error amplifier, which compares the SNSBOOST voltage with an accurate trimmed reference voltage ($V_{reg(SNSBOOST)}$) is connected to this pin. The external loop compensation network on the PFCCOMP pin filters the output current. In a typical application, a resistor and two capacitors set the regulation loop bandwidth.

The transconductance of the error amplifier is not constant. To avoid triggering the OVP during start-up and during a converter transient response, the transconductance is increased to a level of $g_{m(high)}$ starting at $V_{gm(high)start}$ (see Figure 8).

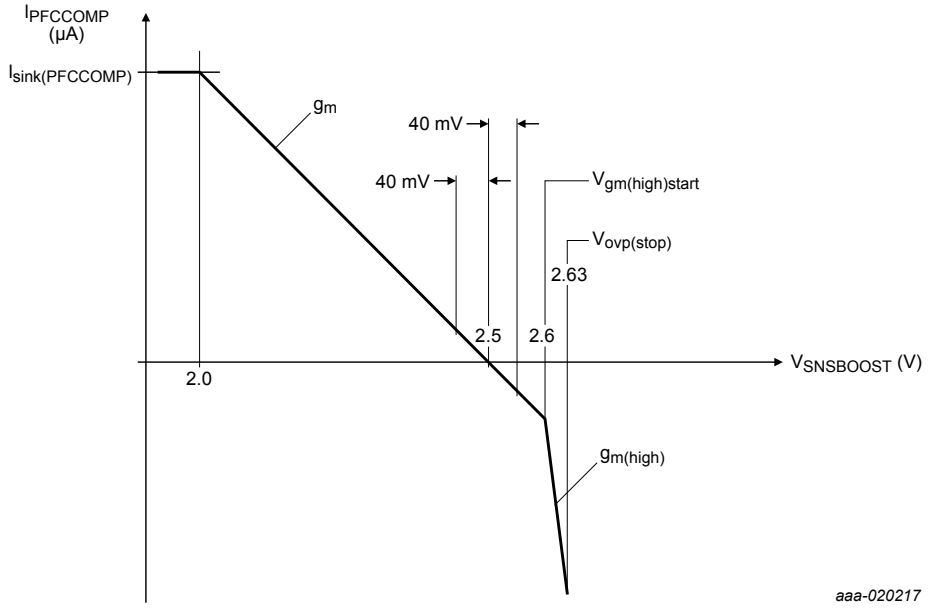


Figure 8. Transconductance of the PFC error amplifier

8.4.4 Valley switching and demagnetization (SNSAUX pin)

To ensure that the TEA19162HT operates in discontinuous or quasi-resonant mode, the PFC MOSFET is switched on after the transformer is demagnetized. To reduce switching losses and ElectroMagnetic Interference (EMI), the next stroke is started when the PFC MOSFET drain-source voltage is at its minimum (valley switching). The demagnetization and valley detection are measured via the SNSAUX pin.

If no demagnetization signal is detected on the SNSAUX pin, the controller generates a demagnetization signal ($t_{to(demag)}$; 44.5 µs typical) after the external MOSFET is switched off.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal ($t_{to(vrec)}$; 3.8 µs typical) after demagnetization is detected.

To protect the internal circuitry, for example during lightning events, connect a 5 kΩ series resistor (R_{aux}; see Figure 13) to the SNSAUX pin. Also connect a 1 kΩ (typical) external sense resistor (R_{SNSCUR}; see Figure 13) to the SNSCUR pin. To prevent incorrect switching due to external disturbance, place the resistors close to the IC.

8.4.5 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation exceeds the $f_{sw(PFC)max}$ limit, the system enters Discontinuous Conduction Mode (DCM). When the system is in DCM, the PFC MOSFET switches on at a minimum voltage across the switch (valley switching).

To ensure correct control of the PFC MOSFET under all circumstances, the minimum off-time is limited at $t_{off(PFC)min}$.

8.4.6 Active X-capacitor discharge

The TEA19162HT provides an active X-capacitor discharge after the mains voltage is disconnected. When the mains input voltage (and so also the measured current into the SNSMAINS pin) increases (see Figure 9, t2 − t1), the system assumes the presence of a mains voltage. When the mains voltage does not increase for a minimum period of $t_{d(dch)}$, the active X-capacitor discharge is activated (t3).

When the active X-capacitor discharge function is activated, the X-capacitor is discharged via the external PFC MOSFET (see Figure 10). To avoid any increase of the PFC output voltage, the external PFC MOSFET is slowly turned on until a small current is detected via the SNSCUR pin (see Figure 9, t4). A slow increase of the GATEPFC voltage is achieved via a current source ($I_{ch(GATEPFC)}$) that slowly charges the external gate-source capacitance of the external MOSFET.

When the voltage at the SNSCUR exceeds $V_{ch(stop)SNSCUR}$ level (10.5 mV), the voltage at the GATEPFC pin slowly decreases by activating a current sink ($I_{dch(GATEPFC)}$). As a result, the gate-source capacitance of the external MOSFET is discharged. When the voltage on the GATEPFC pin drops to below $V_{dch(stop)GATEPFC}$ level (0.7 V), the current sink is switched off. The charge/discharge cycle is repeated after the period $t_{off(dch)}$ (t5). As for a typical power MOSFET the duration of charge/discharge pulses on the GATEPFC pin is shorter than 2 ms, T_p (4 ms typical) defines the pulse repetition time.

When the voltage on the GATEPFC pin exceeds $V_{dch(GATEPFC)}$ while the voltage on the SNSCUR pin is still below $V_{ch(stop)SNSCUR}$, the system assumes a full discharge of the X-capacitor. It starts to ramp down the GATEPFC voltage. Unless the mains is reconnected, the next active X-capacitor discharge cycle is started after $t_{d(dch)}$. Reconnecting the mains is detected via a positive dI/dt at the SNSMAINS pin.

While the GATEPFC pin discharges the X-capacitor, the mains can be reconnected. In that case, the current through the external MOSFET increases rapidly. If the voltage on the SNSCUR pin exceeds $V_{dch(SNSCUR)}$, the internal driver stage rapidly turns off the GATEPFC pin. When the mains is disconnected again (measured via the SNSMAINS pin), the next active X-capacitor discharge cycle starts, followed by a delay of $t_{d(dch)}$.

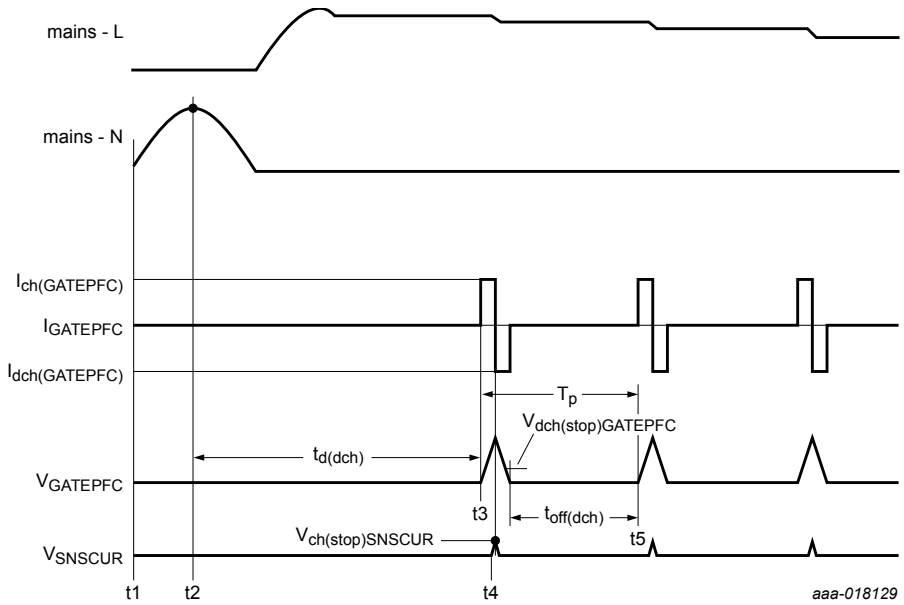


Figure 9. Active X-capacitor discharge

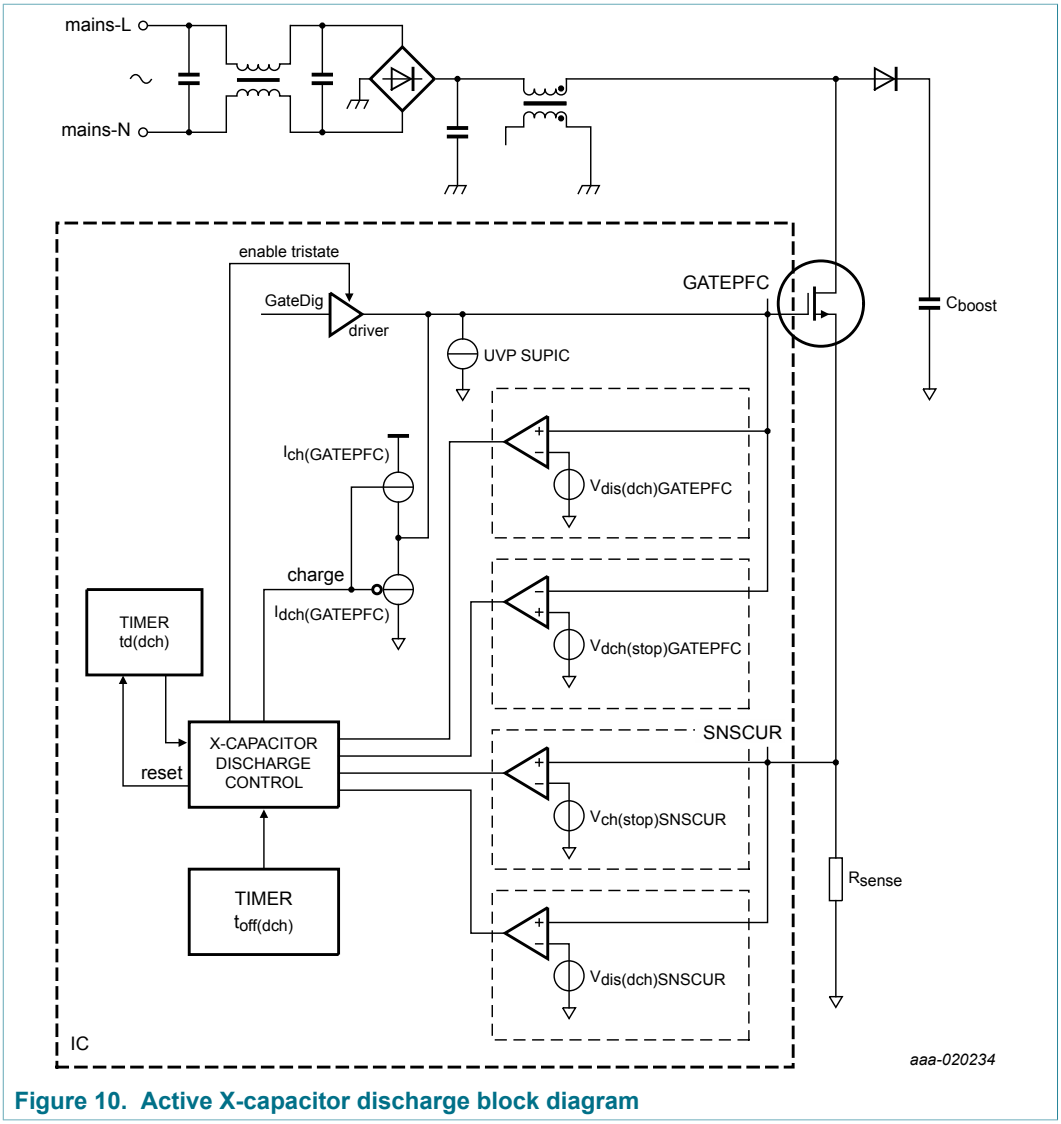


Figure 10. Active X-capacitor discharge block diagram

8.5 PFC-LLC communication protocol

The TEA19162HT (PFC controller) is designed to cooperate with the TEA19161T (LLC controller) in one system. Both controllers can be seen as a combo IC, split up into two packages. All required functionality between the TEA19162HT and TEA19161T is arranged via the combined SUPIC and SNSBOOST pins.

Both controllers are supplied via the SUPIC pin (see Section 8.2). The SNSBOOST pin is used to communicate about the protection states of both controllers. The TEA19161T forces the TEA19162HT to enter burst mode also using the SNSBOOST pin.

8.5.1 Protections

When a protection is triggered in the PFC or the LLC, it can also disable the other converter. For example, if an OVP is detected at the LLC, both converters are stopped. Also, at initial start-up, the PFC disables the LLC converter until the brownin level of the mains voltage is detected.

The SNSBOOST pin is used for the communication about such protection states. By pulling down the SNSBOOST pin below the $V_{uvp(SNSBOOST)}$ level of the LLC converter, the PFC can disable the LLC converter. Similarly, by pulling down the SNSBOOST pin below the short protection level $V_{scp(stop)}$ of the PFC converter, the LLC can disable the PFC.

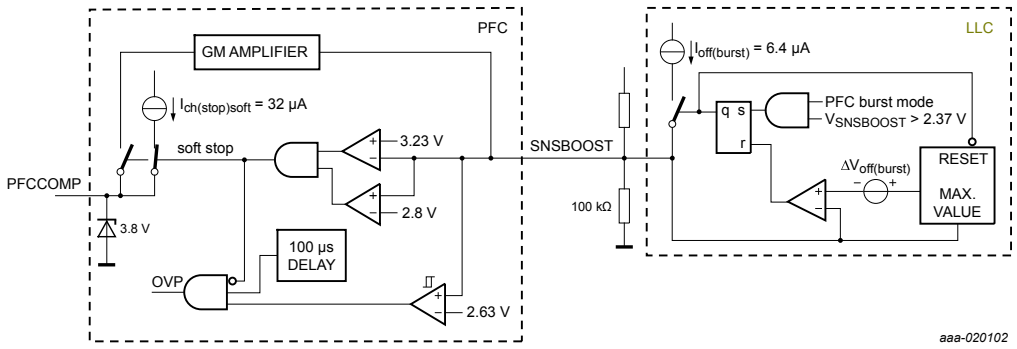
Table 4 in Section 8.3 gives an overview of all protections in the PFC converter. The PFC protections that also disable the LLC are listed in the LLC-column.

When the mains voltage initially drops to below the brownout level and then increases to above the brownin level, all protections of the PFC and the LLC are reset. A reset of all protections is also communicated via the SNSBOOST pin by pulling it up to the $V_{pu(rst)SNSBOOST}$ level (see Section 8.3.7).

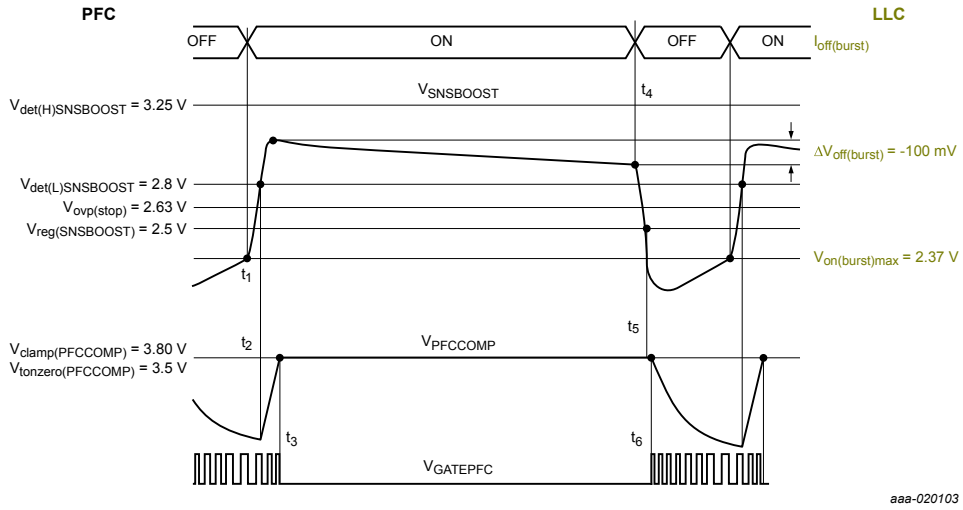
The IC starts and remains in the protection mode until the mains brownin level is reached. The IC current consumption is then at power-saving level.

8.5.2 PFC burst mode

Based on the output power level of the LLC converter, the LLC determines when the PFC enters burst mode. During the burst mode, the LLC converter disables the PFC by increasing the SNSBOOST voltage to between $V_{det(L)SNSBOOST}$ and $V_{det(H)SNSBOOST}$ (see Figure 11). It ensures a soft start and a soft stop at the start and the end of a switching period, respectively. This increase in the voltage on the SNSBOOST pin is achieved by an additional current out of the LLC converter towards the SNSBOOST pin. The additional current creates a positive voltage shift because of the external resistive network at the SNSBOOST pin.



a. Block diagram



b. Timing diagram

Figure 11. PFC burst mode

At t1, the current out of the LLC SNSBOOST pin ($I_{off(burst)}$) is activated and the voltage on the SNSBOOST pin increases. When a 100 kΩ external resistor $R_{SNSBOOST}$ between the SNSBOOST pin and GND pin is used (see Figure 11), the SNSBOOST voltage increase is about 640 mV (= $I_{off(burst)SNSBOOST}$ * $R_{SNSBOOST}$). As due to this increase the SNSBOOST voltage is between $V_{det(L)SNSBOOST}$ and $V_{det(H)SNSBOOST}$ levels (t2), the soft stop of the PFC converter is started. In the soft stop state, the current out of the PFCCOMP pin ($I_{ch(stop)soft}$) is activated. At the end of the soft stop, the PFC enters the energy safe state and stops switching (t3). The voltage at the PFCCOMP pin is clamped at $V_{tonzero(PFCCOMP)}$ (3.5 V). It remains at this level during the energy safe state. As the LLC converter operates continuously, even when the PFC is stopped, the PFC output capacitor discharges.

When the PFC boost capacitor is discharged so much that the voltage on the SNSBOOST pin drops by 75 mV ($\Delta V_{off(burst)}$; t4), the internal current source in the LLC converter is switched off. Because of the negative voltage drop at the SNSBOOST pin, the SNSBOOST voltage drops below the regulation level ($V_{reg(SNSBOOST)}$; t5). The PFC starts switching again (t6). When $V_{SNSBOOST}$ exceeds the LLC $V_{on(burst)max}$ level (2.37 V) again, the internal current is reactivated and the PFC stops switching again.

The TEA19162HT current consumption in the burst mode depends on whether the IC is switching or not. During burst mode on-time and burst mode off-time, the current consumption is at operating level and power-saving level, respectively.

8.5.3 Soft stop

A soft stop always precedes the PFC burst mode. It reduces audible noise of the converter.

The internal current source activated in the LLC converter (see Figure 11) pulls up the voltage at the PFC SNSBOOST pin. When the SNSBOOST pin voltage is between $V_{det(L)SNSBOOST}$ (2.8 V) and $V_{det(H)SNSBOOST}$ (3.23 V), the PFC soft stop begins. Then, a PFC internal current source $I_{ch(stop)soft}$ is activated and the transconductance error amplifier in the PFC control loop is switched off (see Figure 11).

The activated current source provides a current of 32 µA ($I_{ch(stop)soft}$) out of the PFCCOMP pin. This current slowly increases the voltage of the PFCCOMP pin, gradually reducing the converter switching on-time. When the zero on-time is reached, the soft stop ends. The zero on-time corresponds with the PFCCOMP pin voltage of $V_{tonzero(PFCCOMP)}$ (3.5 V).

The detection of the overvoltage on the SNSBOOST pin at the normal OVP level ($V_{ovp(stop)}$) is delayed for the time $t_{d(ovp)}$ (100 µs). This additional delay is required to verify if the system should stop immediately because of an OVP or via a soft stop when activating the burst mode.

8.5.4 Mains voltage compensation (SNSMAINS pin)

The equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, the result is a low bandwidth for low mains input voltages. At high mains input voltages, the Mains Harmonic Reduction (MHR) requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA19162HT contains a correction circuit. The input voltage is measured via the SNSMAINS pin (see Section 8.3.2) and the information is fed to an internal mains compensation circuit (see Figure 1). With this compensation, it is possible to keep the regulation loop bandwidth constant over the full mains input range. The result is that a mains voltage independent transient response on load steps is yielded, while still complying with class-D MHR requirements.

In a typical application, an external circuitry at the PFCCOMP pin (see Section 8.4.3) sets the bandwidth of the regulation loop.

8.6 Driver (pin GATEPFC)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of 600 mA and a current sink capability of 1.4 A typical. These capabilities allow a fast turn-on and turn-off of the power MOSFET, ensuring efficient operation.

When the SUPIC voltage is below its start level, the internal keep-off circuitry of the PFC driver pulls down the GATEPFC pin. The pulling down of the GATEPFC pin prevents that an external power MOSFET is activated when the IC power supply is absent or when the $V_{SUPIC} < V_{start(SUPIC)}$. The keep-off circuitry (see Figure 12) is supplied via the GATEPFC pin. So, if the actual IC supply is absent or too low ($V_{SUPIC} < V_{start(SUPIC)}$), the circuit works correctly.

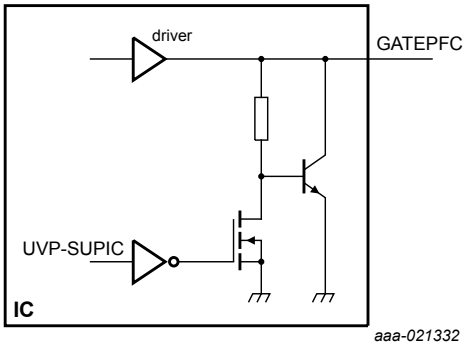


Figure 12. Keep-off circuitry at the GATEPFC pin

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{SUPIC}	voltage on pin SUPIC			−0.4	+38	V
$V_{SNSMAINS}$	voltage on pin SNSMAINS	current limited		−0.4	+12	V
$V_{PFCCOMP}$	voltage on pin PFCCOMP	current limited		−0.4	+12	V
V_{SNSAUX}	voltage on pin SNSAUX	current limited		−25	+25	V
V_{SNSCUR}	voltage on pin SNSCUR	current limited		−0.4	+12	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST	current limited		−0.4	+12	V
$V_{GATEPFC}$	voltage on pin GATEPFC	current limited		−0.4	+12	V
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.45	W
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			-40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	• human body model	[1]	−2000	+2000	V
		• charged device model	[2]	−500	+500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

10 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air;JEDEC test board	150	K/W

11 Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{SUPIC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (SUPIC pin)						
$V_{start(SUPIC)}$	start voltage on pin SUPIC		12.35	13	13.65	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		8.55	9	9.45	V
I_{CC}	supply current	operating mode; f_{sw} = 100 kHz; pin GATEPFC = floating; $V_{SNSBOOST}$ = 2.2 V	-	-	0.80	mA
		power-save mode; pin PFCCOMP = floating; $V_{SNSBOOST}$ = 2.7 V	-	-	0.20	mA
Gate driver output (GATEPFC pin)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V; V_{SUPIC} ≥ 13 V	-	−0.6	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V; V_{SUPIC} ≥ 13 V	-	0.6	-	A
		$V_{GATEPFC}$ = 10 V; V_{SUPIC} ≥ 13 V	-	1.4	-	A
$V_{o(max)GATEPFC}$	maximum output voltage on pin GATEPFC		10.0	11.0	12.0	V
Mains voltage sensing (SNSMAINS pin)						
I_{bi}	brownin current		5.35	5.75	6.15	µA
I_{bo}	brownout current		4.65	5.00	5.35	µA
$I_{bo(hys)}$	hysteresis of brownout current	$I_{bi} - I_{bo}$	640	750	820	nA
$t_{d(det)bo}$	brownout detection delay time		45.2	50	55.5	ms
$V_{regd(SNSMAINS)}$	regulated voltage on pin SNSMAINS	mains detection period; no current at SNSMAINS; $C_{max(SNSMAINS)}$ = 100 pF	230	250	270	mV
X-capacitor discharge (SNSCUR and GATEPFC pins)						
$t_{d(dch)}$	discharge delay time	x-capacitor discharge	109	118	128	ms
$I_{ch(GATEPFC)}$	charge current on pin GATEPFC	x-capacitor discharge	−29	−26	−23	µA
$I_{dch(GATEPFC)}$	discharge current on pin GATEPFC	x-capacitor discharge	23	26	29	µA
$V_{ch(stop)SNSCUR}$	stop charge voltage on pin SNSCUR	x-capacitor discharge; stop of external MOST gate charge; dV/dt = 0	8.00	10.50	12.50	mV
$V_{dch(stop)GATEPFC}$	stop discharge voltage on pin GATEPFC	x-capacitor discharge; stop of external MOST gate discharge	0.3	0.7	1.1	V
$t_{off(dch)}$	discharge off-time	x-capacitor; time between discharge/charge pulses; GATEPFC pin	1.88	-	6.40	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_p	pulse period	x-capacitor discharge; pulse duration < 2 ms (typical); GATEPFC pin	3.76	4.00	4.27	ms
$V_{dis(dch)GATEPFC}$	disable discharge voltage on pin GATEPFC	x-capacitor discharge	9.00	9.45	9.90	V
$V_{dis(dch)SNSCUR}$	disable discharge voltage on pin SNSCUR	x-capacitor discharge	44	50	56	mV
Output voltage sensing, regulation and compensation (SNSBOOST and PFCCOMP pins)						
$V_{reg(SNSBOOST)}$	regulation voltage on pin SNSBOOST	$I_{PFCCOMP}$ = 0 A	2.475	2.500	2.525	V
g_m	transconductance	error amplifier; $V_{SNSBOOST}$ to $I_{PFCCOMP}$; $\lvert V_{SNSBOOST} - V_{intregd(SNSBOOST)} \rvert$ < 40 mV	−90	−75	−60	µA/V
$I_{sink(PFCCOMP)}$	sink current on pin PFCCOMP	$V_{SNSBOOST}$ = 2 V; $V_{PFCCOMP}$ = 2.75 V	30.0	35.5	41.0	µA
$g_{m(high)}$	high transconductance	error amplifier; $V_{SNSBOOST}$ to $I_{PFCCOMP}$; $V_{start(gm)high} \leq V_{SNSBOOST} < V_{stop(ovp)}$	-	−1.26	-	mA/V
$V_{gm(high)start}$	start high transconductance voltage	pin SNSBOOST	2.56	2.60	2.63	V
$I_{clamp(max)}$	maximum clamp current	pin PFCCOMP; energy-save mode; PFC off; $V_{PFCCOMP}$ = 0 V	−260	−220	−190	µA
$I_{en(PFC)}$	PFC enable current	pin PFCCOMP	−15	−11.5	−8	µA
$V_{clamp(PFCCOMP)}$	clamp voltage on pin PFCCOMP	bidirectional clamp; energy-save mode; PFC off	3.40	3.50	3.60	V
		upper clamp voltage; unidirectional clamp; operating mode; PFC on; $I_{PFCCOMP}$ = 120 µA	3.70	3.80	3.90	V
		lower clamp voltage; unidirectional clamp; operating mode;PFC on; $V_{SNSBOOST}$ = 2.5 V; $I_{PFCCOMP}$ = 30 µA	$V_{tonmax(PFCCOMP)}$			V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mains compensation						
$t_{on(PFC)}$	PFC on-time	minimum mains voltage compensation current; $V_{PFCCOMP}$ = 1.25 V; $V_{SNSBOOST}$ = 2.5 V; $I_{mvc(SNSMAINS)}$ = 5.25 µA	30	37.5	45	µs
		maximum mains voltage compensation current; $V_{PFCCOMP}$ = 1.25 V; $V_{SNSBOOST}$ = 2.5 V; $I_{mvc(SNSMAINS)}$ = $I_{mvc(max)SNSMAINS}$	1.5	3	4.5	µs
$I_{mvc(max)SNSMAINS}$	maximum mains voltage compensation current on pin SNSMAINS		18	20	22	µA
PFC on-timer (PFCCOMP pin)						
$V_{tonzero(PFCCOMP)}$	zero on-time voltage on pin PFCCOMP		3.40	3.50	3.60	V
$V_{tonmax(PFCCOMP)}$	maximum on-time voltage on pin PFCCOMP		1.18	1.23	1.28	V
$f_{sw(PFC)max}$	maximum PFC switching frequency		328	365	402	kHz
$t_{off(PFC)min}$	minimum PFC off-time		1.25	1.55	1.85	µs
Demagnetization sensing (pin SNSAUX)						
$V_{det(demag)SNSAUX}$	demagnetization detection voltage on pin SNSAUX		−125	−90	−55	mV
$t_{to(demag)}$	demagnetization time-out time		37	44.5	52	µs
$I_{prot(SNSAUX)}$	protection current on pin SNSAUX	pin SNSAUX = open; V_{SNSAUX} = 50 mV	-	−40	-	nA
Valley sensing (SNSAUX pin)						
$(\Delta V/\Delta t)_{vrec(min)}$	minimum valley recognition voltage change with time		-	-	1.7	V/µs
$t_{to(vrec)}$	valley recognition time-out time		3.0	3.8	4.6	µs
Output current sensing (SNSCUR pin)						
$V_{reg(oc)}$	overcurrent regulation voltage	dV/dt = 0	0.48	0.50	0.52	V
$t_{d(swoff)driver}$	driver switch-off delay time	pin GATEPFC	-	80	-	ns
t_{leb}	leading edge blanking time	V_{SNSCUR} = 0.75 V	240	300	360	ns
$I_{prot(SNSCUR)}$	protection current on pin SNSCUR	pin SNSCUR = open	-	−50	-	nA
Output voltage protection sensing (pin SNSBOOST)						
$I_{pd(SNSBOOST)}$	pull-down current on pin SNSBOOST	protection active; $V_{SNSBOOST}$ = 1.0 V	85	100	115	µA
$V_{scp(stop)}$	stop short-circuit protection voltage		0.35	0.40	0.45	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{scp(start)}$	start short-circuit protection voltage		0.45	0.50	0.55	V
$t_{d(start)}$	start delay time	after short-circuit protection removed	3.30	3.62	4.00	ms
$I_{pu(rst)SNSBOOST}$	reset pull-up current on pin SNSBOOST	fast latch reset; $V_{SNSBOOST}$ = 1.5 V	−245	−210	−175	µA
$V_{pu(rst)SNSBOOST}$	reset pull-up voltage on pin SNSBOOST	fast latch reset	1.94	2.00	2.06	V
$I_{prot(SNSBOOST)}$	protection current on open pin SNSBOOST	pin SNSBOOST = open	-	35	-	nA
$V_{ovp(stop)}$	stop overvoltage protection voltage		2.59	2.63	2.67	V
$V_{ovp(start)}$	start overvoltage protection voltage		2.47	2.53	2.59	V
$V_{hys(ovp)}$	overvoltage protection hysteresis voltage on pin SNSBOOST	$V_{ovp(stop)} - V_{ovp(start)}$	0.07	0.10	0.13	V
Soft start (pin SNSCUR)						
$t_{start(soft)}$	soft start time		3.30	3.62	4.00	ms
$V_{start(soft)init}$	initial soft start voltage		100	125	155	mV
Soft stop (pins SNSBOOST and PFCCOMP)						
$V_{det(L)SNSBOOST}$	LOW-level detection voltage on pin SNSBOOST	soft stop	2.74	2.80	2.86	V
$V_{det(H)SNSBOOST}$	HIGH-level detection voltage on pin SNSBOOST	soft stop	3.17	3.23	3.29	V
$I_{ch(stop)soft}$	soft stop charge current	pin PFCCOMP	−36	−32	−28	µA
$t_{d(ovp)}$	overvoltage protection delay time	pin SNSBOOST	80	100	120	µs
External and internal overtemperature measurement						
$I_{en(NTC)}$	NTC enable current	pin SNSMAINS; NTC measurement;mains measurement period; falling slope	2.0	2.5	3.0	µA
$I_{o(SNSMAINS)}$	output current on pin SNSMAINS		−214	−200	−186	µA
$t_{det(NTC)max}$	maximum NTC detection time		0.92	1.00	1.08	ms
$V_{det(SNSMAINS)}$	detection voltage on pin SNSMAINS	NTC measurement; $I_{SNSMAINS}$ = −200 A	1.95	2.00	2.05	V
$T_{pl(IC)}$	IC protection level temperature		130	150	160	°C

12 Application information

Capacitor C_{SUPIC} filters the IC supply voltage, which must be supplied externally. Sense resistor R_{sense} converts the current through the MOSFET M1 to a voltage on the SNSCUR pin. The R_{sense} value determines the maximum primary peak current in MOSFET M1.

To limit the current into the SNSCUR pin due to negative voltage spikes across the sense resistor, resistor R_{SNSCUR} is added.

To protect the IC from damage during lightning events, resistor R_{aux} is added.

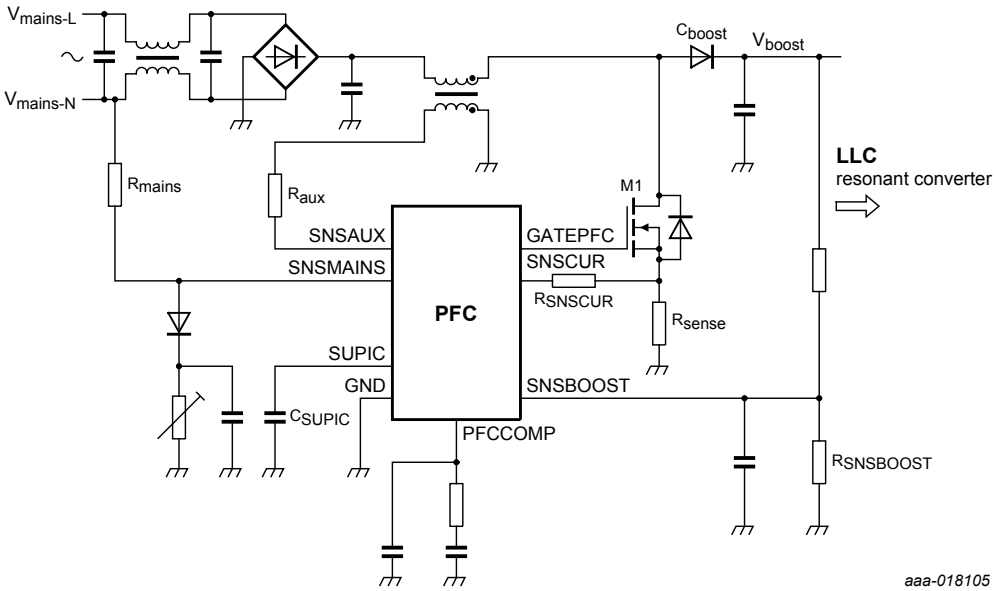
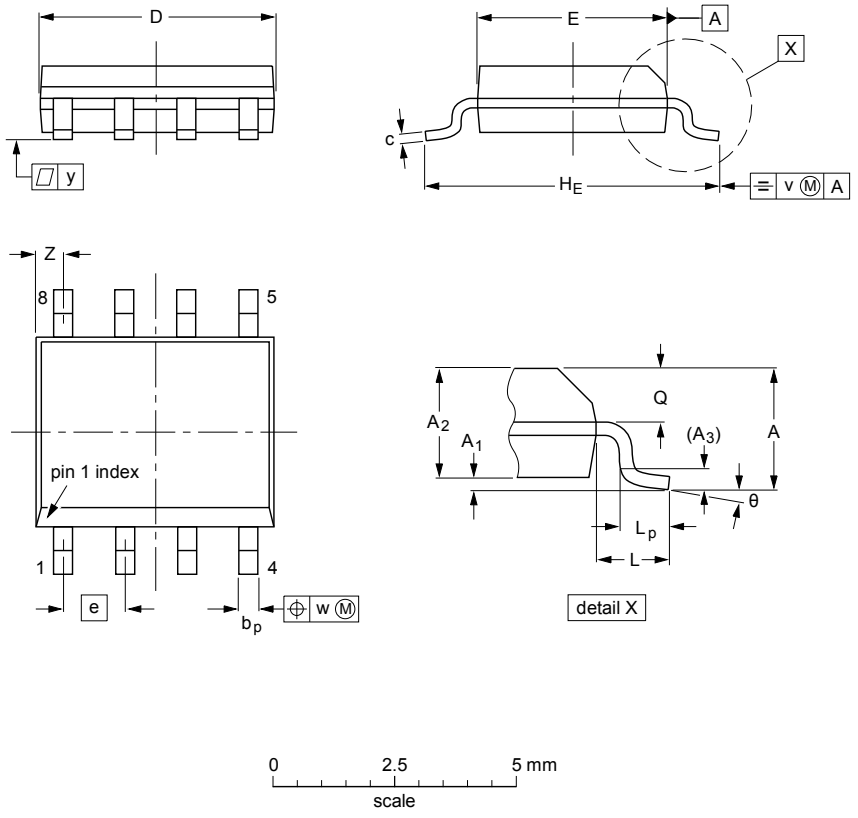


Figure 13. Application diagram

13 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 14. Package outline SOT96-1 (SO8)

14 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA19162HT v.1	20180925	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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