TEA1938T

GreenChip SMPS primary side control IC

Rev. 1 — 1 September 2017

Product data sheet
COMPANY PUBLIC

1 General description

The TEA1938T is a member of the GreenChip family of controller ICs for switched-mode power supplies. It is intended for flyback topologies to be used either standalone or together with USB PD or smart charging controllers (like the TEA190x series) at the secondary side. The built-in green functions provide high efficiency at all power levels.

The TEA1938T is compatible with multiple output voltage applications with a wide output range from 5 V to 20 V in Constant Voltage (CV) mode. When used with a secondary-side controller IC, like the TEA190x series, it supports Constant Current (CC) mode down to 3 V output voltage.

At high power levels, the flyback converter operates in Quasi-Resonant (QR) mode. At lower power levels, the controller switches to Frequency Reduction (FR) in Discontinuous Conduction Mode (DCM) operation. The peak current is limited to a minimum level. Valley switching is used in all operating modes.

At very low power levels, the controller uses a minimum-ripple burst mode to regulate the output power. A special optocoupler current reduction regulation has been integrated which reduces the average optocoupler current in all modes to a minimum level. This reduction ensures high efficiency at low power and excellent no-load power performance. As the number of pulses per burst is kept at a minimum in this mode, the output ripple is minimized. For further efficiency optimization, the internal IC supply current is minimized during the non-switching phase of the burst mode.

The TEA1938T includes a wide set of protections that are safe-restart protections. One of these protections is an accurate OverPower Protection (OPP). If the output is shorted, the system stops switching and restarts. The output power is then limited to a lower level.

The TEA1938T is manufactured in a high-voltage Silicon-On-Insulator (SOI) process. The SOI process combines the advantages of a low-voltage process (accuracy, high-speed protection, functions, and control). However, it also maintains the high-voltage capabilities (high-voltage start-up, low standby power, and brownin/brownout sensing at the input).

The TEA1938T enables low-cost, highly efficient, and reliable supplies for power requirements up to 75 W using a minimum number of external components.

2 Features and benefits

2.1 General features

- SMPS controller IC supporting smart-charging applications and multiple-output-voltage applications
- Wide output range (5 V to 20 V in CV mode, 3 V to 20 V in CC mode, and 3 V to 6.5 V in direct charging mode)
- Housed in a small SO10 package
- Adaptive dual supply for highest efficiency over the entire output voltage range
- Reduced optocurrent enabling low no-load power (20 mW at 5 V output)
- Fast transient response from 0 to full load
- Minimal audible noise and output voltage ripple in all operating modes
- Minimum ripple burst mode at very low power levels allowing the minimizing of the size of output capacitors
- Integrated soft start

2.2 Green features

Enables high-efficiency operation over a wide power range via:

- Low supply current during normal operation (0.6 mA without load)
- Low supply current during non-switching state in burst mode (0.2 mA)
- Valley switching for minimum switching losses
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels

2.3 Protection features

All protections are safe-restart protections.

- Mains voltage compensated OverPower Protection (OPP)
- OverTemperature Protection (OTP)
- Integrated overpower timeout
- Integrated restart timer for system fault conditions
- Continuous mode protection using demagnetization detection
- Accurate OverVoltage Protection (OVP)
- General-purpose input for safe restart protection; for use with system OverTemperature Protection (OTP)
- Driver maximum on-time protection
- Brownin and brownout protection

3 Applications

- Battery chargers for smart phones and media tablets
- Battery chargers for mobile devices with touchpad display

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1938T/1	SO10	plastic small outline package; 10 leads; body width 3.9 mm; body thickness 1.35 mm	SOT1437-1

5 Marking

Table 2. Marking code

Type number	Marking code
TEA1938T/1	TEA1938

6 Block diagram

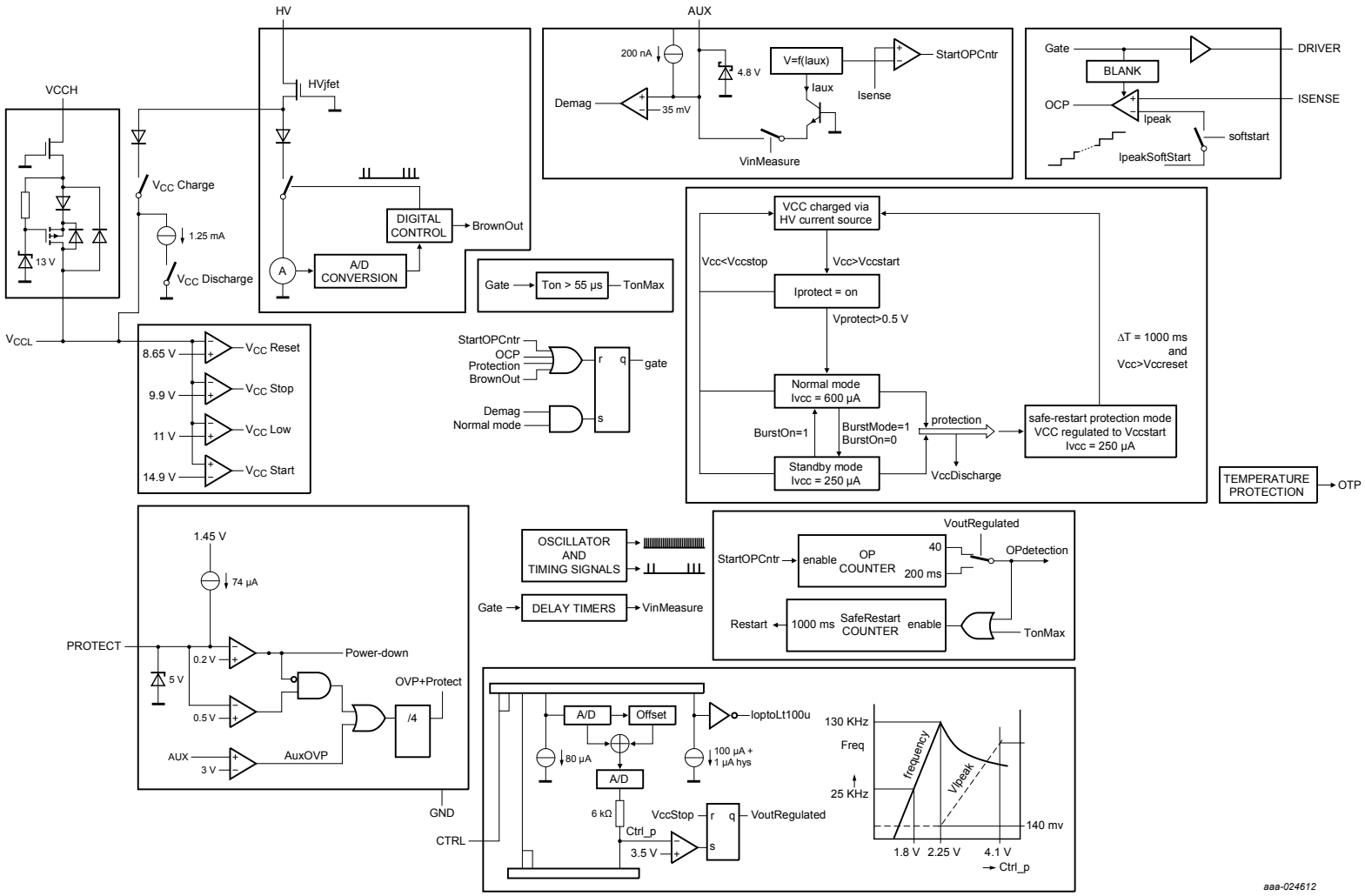


Figure 1. TEA1938T block diagram

7 Pinning information

7.1 Pinning

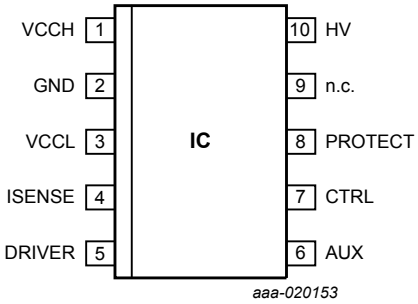


Figure 2. TEA1938T pin configuration (SO10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VCCH	1	higher supply voltage
GND	2	ground
VCCL	3	lower supply voltage
ISENSE	4	current sense input
DRIVER	5	gate driver output
AUX	6	auxiliary winding input for demagnetization timing, valley detection, overpower correction, and OVP
CTRL	7	control input
PROTECT	8	general-purpose protection input; pin for power-down mode
n.c.	9	not connected; high-voltage safety spacer
HV	10	high-voltage start-up; brownin/brownout sensing

8 Functional description

8.1 Supply management

During start-up and in protection mode, high-voltage mains via the HV pin supplies the chip. When the system starts switching, the auxiliary windings take over the supply.

The IC has two supply pins, the VCCH and VCCL pins. The lower pin (VCCL) supplies the IC directly. The higher supply pin (VCCH) is connected to the VCCL pin via an internal voltage regulator. When used in an application, which supports multiple output voltages, a pair of auxiliary transformer windings can be used to supply the IC efficiently at all output levels. To supply the IC at higher output voltages, the winding with fewer turns can be connected to the VCCL pin. At the lower output voltages, the winding with more turns can supply the IC via the VCCH pin. The voltage capability of these pins is chosen such that applications with an output voltage range from 3 V to 20 V are supported optimally. When the voltage on the VCCL pin drops to below $V_{intregd(VCCL)}$, the regulator between the VCCH and VCCL pins turns on.

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature-compensated current reference circuit.

8.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCCL pin is charged from the high-voltage mains using the HV pin. The voltage on the VCCH pin follows (via an internal diode) the voltage on VCCL pin. In this way, the capacitor on the VCCH pin is charged. As long as V_{CC} (the voltage on pin VCCL) is below $V_{startup}$, the IC current consumption is minimized. When V_{CC} reaches the $V_{startup}$ level, the control logic activates the internal circuitry. The IC waits for the PROTECT pin to reach $V_{det(PROTECT)} + V_{det(hys)PROTECT}$ and for the mains voltage to increase to above the brownin level. Meanwhile, the internal power-control signal (which depends on the current at the CTRL pin) also increases to its maximum value. When all these conditions are met, the system starts switching with a soft start. In a typical application, the auxiliary winding of the transformer takes over the supply.

During the start-up period, the VCC pin is continuously regulated to the $V_{startup}$ level using the HV charge current. The pin is regulated until the output voltage is at its regulation level, which is detected via the CTRL pin. In this way, the VCC capacitor value can be limited. Due to the limited current capability from the HV pin, the voltage on pin VCC can still drop slightly during the start-up period.

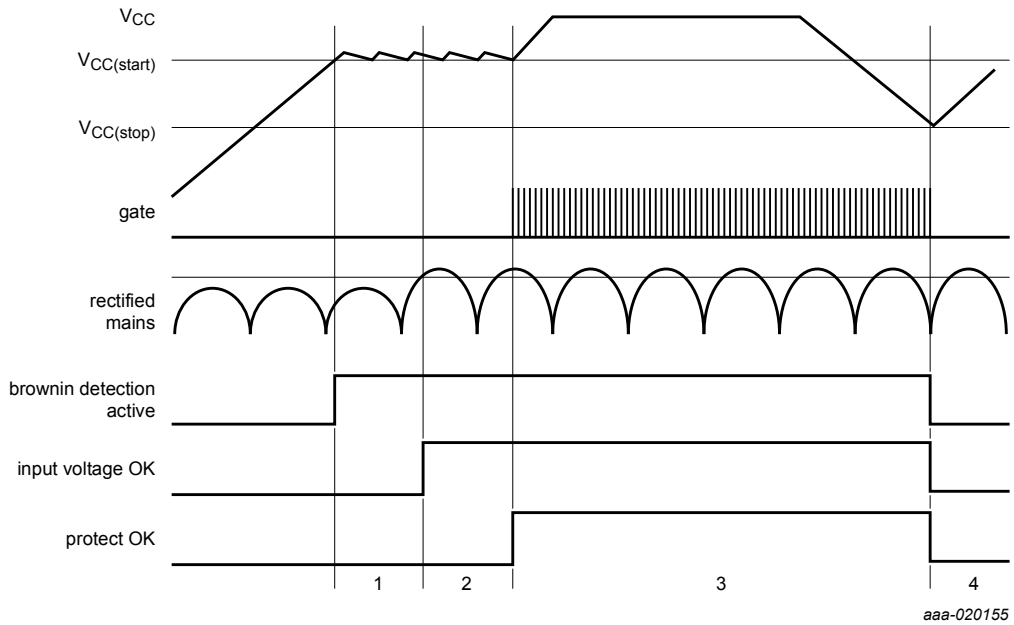


Figure 3. Start-up sequence

8.3 Modes of operation

The TEA1938T operates primarily in fixed-frequency DCM mode. At low powers, it enters burst mode. At high powers, it can operate in Quasi-Resonance (QR) mode (see Figure 4). The auxiliary winding of the flyback transformer provides demagnetization information.

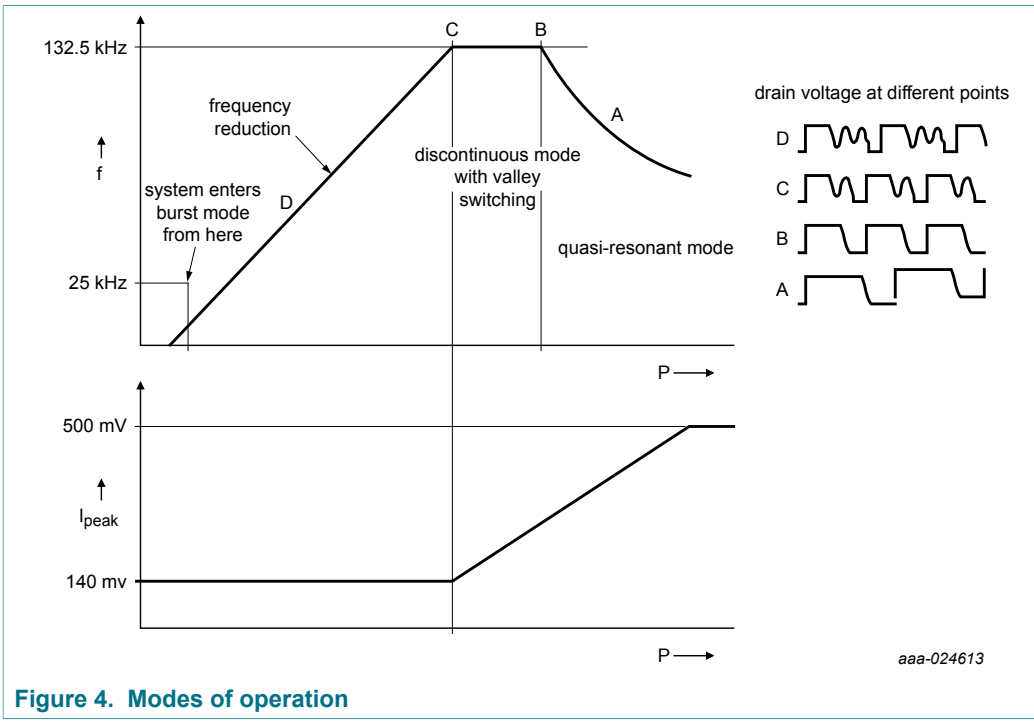


Figure 4. Modes of operation

At high output power, the converter operates in QR-mode. Each converter cycle starts after the demagnetization of the transformer and the detection of the valley at the end of the previous cycle. In QR-mode, switching losses are minimized because the external MOSFET is switched on while the drain-source voltage is minimal.

To limit the frequency of operation and enable good efficiency, the QR operation switches to DCM operation with valley skipping when the maximum frequency limit ($f_{sw(max)}$) is reached. This frequency limit reduces the MOSFET switch-on losses and conducted ElectroMagnetic Interference (EMI).

At medium power levels, the controller enters Frequency Reduction (FR) mode. A Voltage Controlled Oscillator (VCO) controls the frequency. The minimum frequency in this mode is ($f_{sw(min)}$). To maintain high efficiency, the primary peak current is kept at a minimum level during FR-mode. Valley switching is also active in this mode.

At low power, the converter enters the minimum-ripple burst mode.

8.4 Mains voltage measuring

In a typical application, the mains input voltage is measured using the HV pin.

The mains voltage is measured every 1 ms by pulling down the HV pin to ground and measuring its current. This current then reflects the input voltage.

The system determines if the mains voltage exceeds the brownin level.

When the mains exceeds the brownin level, the system is allowed to start switching.

If the mains voltage is continuously below the brownout level for at least 30 ms, a brownout is detected and the system immediately stops switching. This period is required to avoid that the system stops switching during a short mains interruption.

If the measured mains level exceeds the brownin/brownout threshold, subsequent measuring of the mains input voltage is stopped for 7 ms to improve efficiency. In burst mode, this waiting period is increased to 104 ms.

8.5 Auxiliary winding

To supply the control IC efficiently, the VCCH and VCCL pins are connected to auxiliary windings via a diode and a capacitor.

To detect demagnetization and input and output voltage, one of the auxiliary windings is connected to the AUX pin via a resistive divider (see Figure 16 and Figure 17). Each switching cycle is divided in sections. During each section, the system knows if the voltage or current out of the AUX pin reflects the demagnetization, valley, input voltage, or output voltage (see Figure 5).

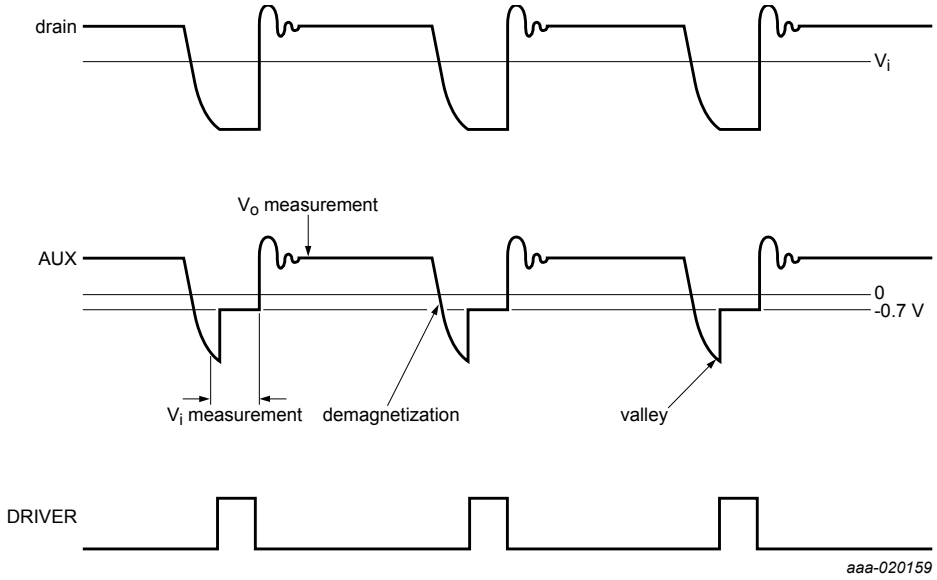


Figure 5. AUX pin used for demagnetization and input and output voltage measurement

When the external MOSFET is switched on, the voltage at the auxiliary windings reflects the input voltage. The AUX pin is clamped to −0.7 V. The output current is a measure of the input voltage. This current value is internally used to set the overpower limit on $V_{sense(ipk)}$. The demagnetization, valley, and output voltages are measured as a voltage on the AUX pin. In this way, the input voltage measurement and OVP can be adjusted independently.

8.6 Protections

If a protection is triggered, the controller stops switching. To avoid false triggering, some protections have a built-in delay.

Table 4. Protections

Protection	Delay	Action	V_{CC} regulated
AUX open	no	wait until AUX is connected	no
brownout	30 ms	wait until $V_{mains} > V_{bi}$	yes
maximum on-time	no	safe restart	yes
OTP internal	4.5 µs	safe restart	yes
OTP via the PROTECT pin	2 ms to 4 ms	safe restart	yes
OVP via the AUX pin	4 driver pulses[1]	safe restart	yes
OVP via VCCL pin	4 driver pulses[1]	safe restart	yes
overpower timeout	40 ms to 200 ms	safe restart	yes
overpower + UVLO	no	safe restart	yes
overcurrent protection	blanking time	safe restart	no
UVLO	no	Wait until $V_{VCCL} > V_{startup}$	yes

[1] When the voltage on the PROTECT pin is below $V_{det(PROTECT)}$, the clock of the delay counter is changed from the driver pulse to 1 ms internal pulse.

When the system stops switching, the VCCH and VCCL pins are not supplied via the auxiliary winding anymore. Depending on the protection triggered, V_{VCCL} is either regulated to the $V_{startup}$ level via the HV pin or decreases until the UVLO protection triggered (see Table 4).

8.6.1 OverPower Protection (OPP)

The overpower protection function is used to realize a maximum output power which is nearly constant over the full input mains.

For applications intended to operate fully in DCM mode, a constant overpower protection level can be set by using the flat portion of the OPP curve (see Figure 6). On the other hand, applications designed to operate in QR mode at maximum power require the OPP level to be compensated for mains. They can be set to use the variable part of the OPP curve.

The resistors connected to the AUX pin set the I_{AUX}. They determine which part of the OPP curve is used by the application.

The overpower compensation circuit measures the input voltage via the AUX pin. The circuit outputs an overpower reference voltage that depends on this input voltage. If the measured voltage at the ISENSE pin exceeds the overpower reference voltage ($V_{opp(ISENSE)}$), the DRIVER output is pulled low (the primary stroke is cut short). The overpower timer starts. In this way, the system limits the power to the maximum rated value on a cycle-by-cycle base. If the overpower situation persists continuously for 200 ms, an overpower timeout is triggered. Figure 6 shows the overpower protection curve.

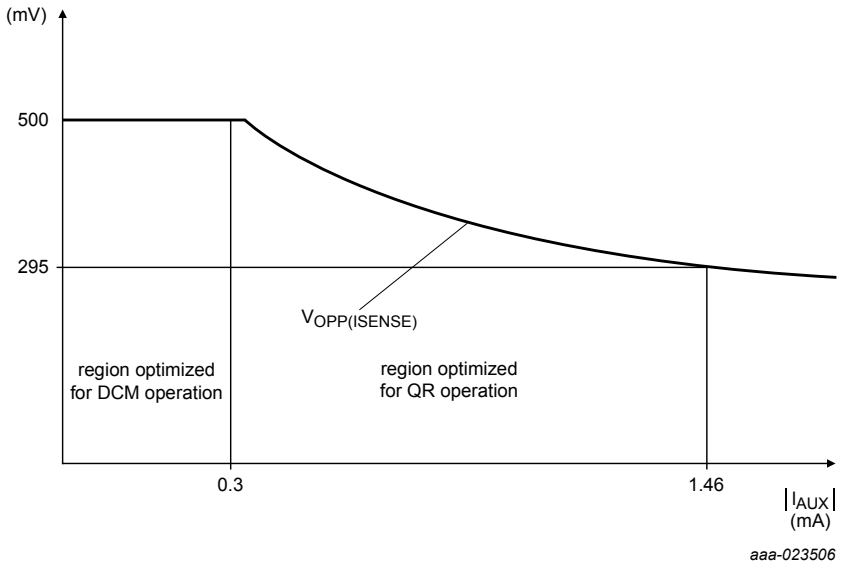


Figure 6. Overpower protection curve

During system start-up, the maximum timeout period is lowered to 40 ms. When the output voltage is within its regulation level, the maximum timeout period returns to 200 ms, limiting the output power to a minimum at a shorted output. Shortening the overpower timer ensures that the input power of the system is limited to < 5 W at a shorted output.

If the load requires more power than allowed by the OPP limit, the output voltage drops because of the limited output power. As a result, the V_{CC} voltage also drops and UVLO can be triggered. To retain the same response in an overpower situation (whether UVLO is triggered or not), the system enters the overpower protection mode when overpower and UVLO are detected. The system entering the protection mode does not depend on the value of the OP counter.

8.6.2 OverVoltage Protection (OVP; pins AUX and VCCL)

An accurate output OVP is implemented by measuring the voltage at the AUX pin during the secondary stroke. As the auxiliary winding voltage is a well-defined replica of the output voltage, the external resistor divider ratio R_{AUX2} / (R_{AUX1} + R_{AUX2}) can adjust the OVP level.

An accurate OVP circuit is also connected to the VCCL pin. It measures if the VCCL pin voltage exceeds the level $V_{ovp(VCCL)}$ at the end of primary stroke.

An internal counter of four gate pulses prevents false OVP detection which can occur during ESD or lightning events.

8.6.3 Protection input (PROTECT pin)

The PROTECT pin is a general-purpose input pin. It can be used to trigger one of the protection types shown in Table 4. When the voltage on the PROTECT pin is pulled below $V_{det(PROTECT)}$ (0.5 V), the converter is stopped.

The PROTECT pin can be used to create an OTP function. To create the OTP function, a Negative Temperature Coefficient (NTC) resistor must be connected to this pin. When the voltage on the PROTECT pin drops to below 0.5 V, overtemperature is detected. The PROTECT current (maximum 74 µA) flowing through the external NTC resistor creates the voltage. The PROTECT voltage is clamped to maximum 1.45 V. At room temperature, the resistance value of the NTC resistor is much higher than at high temperatures. Because of the clamp, the current out of the PROTECT pin is 1.45 V divided by the resistance, which is much lower than 74 µA.

A filter capacitor can be connected to the PROTECT pin.

To avoid false triggering, an internal filter of 2 ms to 4 ms is applied.

8.6.4 OverTemperature Protection (OTP)

If the junction temperature exceeds the thermal temperature shutdown limit, an integrated OTP feature ensures that the IC stops switching. OTP is a safe restart protection.

A built-in hysteresis ensures that the internal temperature must drop 10 °C before the IC restarts.

8.6.5 Maximum on-time

The controller limits the on-time of the external MOSFET to 55 µs. When the on-time is longer, the IC stops switching and enters safe restart mode.

8.6.6 Safe restart

If a protection is triggered and the system enters the safe restart mode (see Table 4), the system restarts after a delay time ($t_{d(restart)}$). An internal current source ($I_{CC(dch)}$) discharges the voltage on pin VCCL. The discharge allows the conditions at a restart to be similar to a normal start-up. Because the system is not switching, the VCCL and VCCH pins are supplied from the mains via the HV pin.

After the restart delay time ($t_{d(restart)}$), the control IC measures the mains voltage. If the mains voltage exceeds the brownin level, the control IC activates the PROTECT pin current source and the internal voltage sources connected to the CTRL pin. When the voltages on these pins reach a minimum level, the soft-start capacitor on the ISENSE pin is charged and the system starts switching again.

The V_{CC} is continuously regulated to the $V_{startup}$ level until the output voltage is within the regulation level again.

8.7 Optobias regulation (CTRL pin)

In a typical application, the output voltage (or current) is sensed on the secondary side (by a TL431 or a controller such as TEA190x). The feedback signal is passed to the primary side via an optocoupler. The optocoupler sends the current information to the CTRL pin of the TEA1938T (see Figure 16 and Figure 17).

The TEA1938T applies a relatively fixed voltage at the CTRL pin (the input impedance of the CTRL pin is $R_{int(CTRL)}$). It senses the current through the optocoupler. The TEA1938T compares the current with an internal regulation level $I_{IO(reg)CTRL}$ (80 µA). The difference is integrated with a slow time constant (in ms). It is added to the control signal that sets the output power. If the optocurrent (at CTRL pin) exceeds the regulation level ($I_{IO(reg)CTRL}$), the control signal reduces in this way, which leads to an output power decrease and vice versa. The optocurrent (at the CTRL pin) slowly regulates toward the regulation level ($I_{IO(reg)CTRL}$). The result is a constant optocurrent during stable operation at all output power levels.

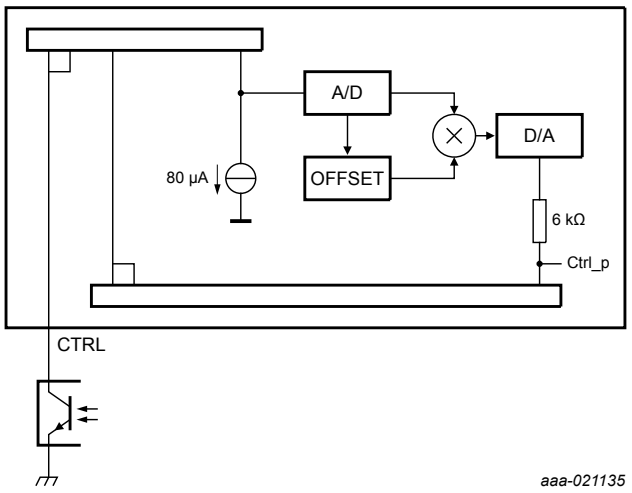


Figure 7. Optobias regulation

Figure 7 shows the slow optocurrent regulation loop.

In addition to the slow optocurrent regulation loop, the CTRL current directly contributes to the internal power control by creating a voltage drop across a 6 kΩ resistor (see Figure 7). It determines the transient behavior of the power regulation loop, which remains similar to ICs, like the TEA1836. The control loop responds to load or line variations through this direct optocurrent contribution, whereas the slow offset loop simply sets the steady state operation point.

The advantages of this type of regulation are:

- The optocoupler collector parasitics do not influence the loop. So, more freedom in tuning the loop characteristics is ensured.
- Unlike the traditional situation where the optocoupler current becomes much higher at lower output power, it retains the same low value in steady state at all powers.
- The optocurrent is only 80 µA even at low powers. So, a load step to a very high load can result in a maximum decrease of the optocurrent by this amount only. It limits the possible power increase. To counter this possibility, the offset loop enters a fast regulation mode when a significant optocurrent decrease is detected (to about 20 µA under the regulation level). The fast regulation mode ensures a quick output power increase.

8.8 Minimum-ripple burst mode operation

When the output power drops to below the minimum level the system can supply while operating at the minimum power setting (i.e. the switching frequency is at its minimum), it can no longer reduce the optocurrent level to the regulation level $I_{IO(reg)CTRL}$ (= 80 µA). In this situation, the optocurrent increases to exceed the level of the burst threshold ($I_{th(burst)CTRL}$) and the burst mode is entered. Switching is paused and a burst-off period commences. Consequently, the optocurrent decreases.

When the optocurrent drops to a level below the burst threshold (with a small hysteresis to ensure stable operation), a new burst of switching cycles is started. As a result, the optocurrent increases again. If it increases and remains above the burst threshold at the end of any switching pulse period, the switching pauses and that burst is ended.

For most of the burst mode, a single pulse is sufficient for the optocurrent to increase and remain above the burst threshold. It leads to operation with one pulse per burst period with an increasing repetition rate of bursts as the required output power increases. As power increases further, one pulse may not be sufficient to increase the optocurrent so it exceeds the burst threshold. In this case, more pulses are made in each burst period at a switching frequency of $f_{sw(min)}$. Increasing the load further, increases the number of pulses per burst, until the IC switches continuously at $f_{sw(min)}$. The optocurrent drops from the burst threshold ($I_{th(burst)CTRL}$) to the regulation level ($I_{reg(burst)CTRL}$) and burst mode is exited. This burst scheme provides the lowest possible output ripple for any load in burst mode, which minimizes the value of the output capacitance. In addition, the optocoupler current is maintained at a very low level during low-load and standby operation. The result is a very low standby power consumption.

At very low output power, the repetition rate of the single-pulse bursts decreases as well to a very low value. To improve the no-load input power and efficiency at low load further, the current consumption of the IC is lowered to 240 µA during the non-switching period in the burst mode.

To achieve a good transient response at an increased output load, the system starts switching immediately when I_{CTRL} drops to below $I_{start(burst)}$. It keeps switching until the optocurrent exceeds the level of $I_{start(burst)CTRL}$ (100 µA). To achieve a good transient response at a decreased output load, the system stops switching immediately when the optocurrent exceeds the level of $I_{stop(burst)CTRL}$ (200 µA) at a decreased output load.

8.9 Soft start-up (ISENSE pin)

To prevent audible noise during start-up or a restart condition, an integrated soft-start feature is implemented. When the converter starts switching, the primary peak current slowly increases to the regulated level in 15 steps.

The soft-start time constant is 4 ms, set by an internal time.

8.10 Driver (DRIVER pin)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of 300 mA and a current sink capability of 750 mA. These capabilities allow a fast turn-on and turn-off of the power MOSFET for efficient operation.

The maximum driver output is limited to 10.5 V. The DRIVER output pin can be connected to the gate of a MOSFET directly or via a resistor.

9 Limiting values

Table 5. Limiting values

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
$V_{IO(HV)}$	input/output voltage on pin HV			−0.4	+500	V
V_{VCCH}	voltage on pin VCCH	dual supply voltage		−0.4	+120	V
V_{VCCL}	voltage on pin VCCL	dual supply voltage		-	50	V
$V_{IO(CTRL)}$	input/output voltage on pin CTRL			−0.4	+12	V
$V_{I(ISENSE)}$	input voltage on pin ISENSE			−0.4	+12	V
$V_{IO(PROTECT)}$	input/output voltage on pin PROTECT	current limited		−0.4	+5	V
$V_{IO(AUX)}$	input/output voltage on pin AUX	current limited		−5	+5	V
Currents						
$I_{IO(AUX)}$	input/output current on pin AUX			−1.5	+1	mA
$I_{IO(HV)}$	input/output current on pin HV			−1	+5	mA
$I_{IO(CTRL)}$	input/output current on pin CTRL			−3	0	mA
$I_{IO(PROTECT)}$	input/output current on pin PROTECT			−1	+1	mA
$I_{O(DRIVER)}$	output current on pin DRIVER	$\delta < 10\ \%$		−0.4	+1	A
General						
P_{tot}	total power dissipation	$T_{amb} < 75\ °C$		-	1	W
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+150	°C
ElectroStatic Discharge (ESD)						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model	[1]		2000	V
		machine model		-	200	V
		charged device model	[2]	-	500	V

[1] According to JEDEC JS-001.
[2] According to JEDEC JESD22-C101 and ANSI S5.3.1.

10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
$V_{IO(HV)}$	input/output voltage on pin HV		0	380	V
V_{VCCH}	voltage on pin VCCH	dual supply voltage	0	120	V
V_{VCCL}	voltage on pin VCCL	dual supply voltage; continuous	-	45	V
$V_{IO(CTRL)}$	input/output voltage on pin CTRL		0	5	V
$V_{I(ISENSE)}$	input voltage on pin ISENSE		0	5	V
$V_{IO(PROTECT)}$	input/output voltage on pin PROTECT	current limited	0	2	V
$V_{IO(AUX)}$	input/output voltage on pin AUX	current limited	−5	+5	V
Currents					
$I_{IO(AUX)}$	input/output current on pin AUX		−1	+1	mA
$I_{IO(HV)}$	input/output current on pin HV		0	2	mA
$I_{IO(CTRL)}$	input/output current on pin CTRL		−1	0	mA
$I_{IO(PROTECT)}$	input/output current on pin PROTECT		−1	+1	mA
General					
T_j	junction temperature		−25	+125	°C

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	148	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	86	K/W

12 Characteristics

Table 8. Characteristics

Limits are production tested at 25 °C and are guaranteed by statistical characterization in the temperature operating range. V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (HV pin)						
$I_{startup(HV)}$	start-up current on pin HV	V_{HV} > 10 V	0.8	1.15	1.5	mA
		V_{CC} > $V_{startup}$; HV not sampling	-	-	1	µA
V_{clamp}	clamp voltage	I_{HV} < 2 mA	-	-	680	V
Supply voltage management (VCCL pin)						
$V_{startup}$	start-up voltage		16	17.5	19	V
$V_{intregd(VCCL)}$	internal regulated voltage on pin VCCL	via VCCH; I_{CC} = 0.5 mA	12.1	12.5	12.9	V
$V_{restart}$	restart voltage	burst mode	9.9	11	12.1	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		9.0	9.9	10.8	V
V_{rst}	reset voltage		7.75	8.65	9.55	V
$I_{CC(startup)}$	start-up supply current	V_{HV} = 0 V	-	40	-	µA
		V_{HV} > 10 V	−1.45	−1.1	−0.75	mA
$I_{CC(oper)}$	operating supply current	driver unloaded; excluding optocurrent	-	600	-	µA
$I_{CC(burst)}$	burst mode supply current	non-switching; excluding optocurrent	-	250	-	µA
$I_{CC(prot)}$	protection supply current		-	235	-	µA
$I_{CC(dch)}$	discharge supply current	safe restart protection; V_{CC} > $V_{startup}$	1.45	1.88	2.25	mA
Mains detect (HV pin)						
$t_{p(HV)}$	pulse duration on pin HV	measuring mains voltage	18.5	20.6	22.7	µs
$f_{meas(HV)}$	measurement frequency on pin HV	measuring mains voltage	0.89	1.0	1.11	kHz
$t_{d(norm)HV}$	normal mode delay time on pin HV	measuring mains voltage	6.2	7	7.8	ms
$t_{d(burst)HV}$	burst mode delay time on pin HV	measuring mains voltage	97	104	115	ms
$I_{bo(HV)}$	brownout current on pin HV		552	587	622	µA
$I_{bi(HV)}$	brownin current on pin HV		623	663	703	µA
$I_{bo(hys)HV}$	hysteresis of brownout current on pin HV		-	76	-	µA
$I_{clamp(HV)}$	clamp current on pin HV	during measurement time	-	-	1.75	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{meas(HV)}$	measurement voltage on pin HV		-	2.9	-	V
$t_{d(det)bo}$	brownout detection delay time		-	30	-	ms
Peak current control (pin CTRL)						
$V_{IO(CTRL)}$	input/output voltage on pin CTRL		-	2.7	-	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		-	1.7	-	kΩ
$I_{startup}$	start-up current	input/output current	−580	−500	−420	µA
Burst mode (pin CTRL)						
$I_{th(burst)CTRL}$	burst mode threshold current on pin CTRL		−125	−110	−95	µA
$I_{stop(burst)CTRL}$	burst mode stop current on pin CTRL		−230	−200	−170	µA
Oscillator						
$f_{sw(max)}$	maximum switching frequency		120	128	136	kHz
$f_{sw(min)}$	minimum switching frequency	burst mode ≥ 2 pulses	23	25.5	28	kHz
Current sense (pin ISENSE)						
$V_{sense(peak)}$	peak sense voltage	output overpower		$V_{opp(ISENSE)}$		mV
		burst mode	130	145	160	mV
$t_{PD(sense)}$	sense propagation delay	from the ISENSE pin reaching $V_{sense(max)}$ to driver off; V_{ISENSE} pulse-stepping 100 mV around $V_{sense(max)}$	-	120	-	ns
t_{leb}	leading edge blanking time		275	325	375	ns
Soft start (pin ISENSE)						
$t_{start(soft)}$	soft start time		3.3	3.7	4.1	ms
Demagnetization and valley control (pin AUX)						
$V_{det(demag)}$	demagnetization detection voltage		20	40	60	mV
$I_{prot(AUX)}$	protection current on pin AUX		-	−200	-	nA
$t_{blank(det)demag}$	demagnetization detection blanking time		1.9	2.3	2.7	µs
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time	positive ΔV/Δt	0.25	0.37	0.49	V/µs
		negative ΔV/Δt	−2.45	−1.95	−1.5	V/µs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time		-	120	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{clamp(AUX)}$	clamp voltage on pin AUX	I_{AUX} = 1 mA	4.4	4.8	5.2	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		2.0	2.4	2.8	µs
Maximum on-time (pin DRIVER)						
$t_{on(max)}$	maximum on-time		45	55	65	µs
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	−0.3	-	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	-	0.3	-	A
		V_{DRIVER} = 10 V	-	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Overpower protection (pin ISENSE and pin AUX)						
$V_{clamp(AUX)}$	clamp voltage on pin AUX	primary stroke; I_{AUX} = −0.3 mA	−0.8	−0.7	−0.6	V
$t_{d(clamp)AUX}$	clamp delay time on pin AUX	after rising edge of pin DRIVER	1.9	2.3	2.7	µs
$V_{opp(ISENSE)}$	overpower protection voltage on pin ISENSE	counter trigger level				
		I_{AUX} = −0.3 mA	460	510	560	mV
		I_{AUX} = −1.46 mA	268	298	328	mV
$t_{d(opp)}$	overpower protection delay time	start-up mode; I_{CTRL} < 100 µA	35.5	40	44.5	ms
		normal mode	178	200	222	ms
$t_{d(restart)}$	restart delay time		890	1000	1110	ms
External protection (pin PROTECT)						
$V_{det(PROTECT)}$	detection voltage on pin PROTECT		0.47	0.5	0.53	V
$V_{det(hys)PROTECT}$	detection voltage hysteresis on pin PROTECT		-	50	-	mV
$I_{O(PROTECT)}$	output current on pin PROTECT	normal mode	−79	−74	−69	µA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT		1.2	1.4	1.6	V
Overvoltage protection (pin AUX)						
$V_{ovp(AUX)}$	overvoltage protection voltage on pin AUX		2.88	3	3.12	V
$V_{ovp(VCCL)}$	overvoltage protection voltage on pin VCCL		46.5	48	49.5	V
$t_{det(ovp)}$	overvoltage protection detection time	in the secondary stroke	2	2.4	2.8	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C
$T_{pl(IC)hys}$	hysteresis of IC protection level temperature		-	10	-	°C

12.1 Typical temperature performance characteristics

12.1.1 Start-up voltage

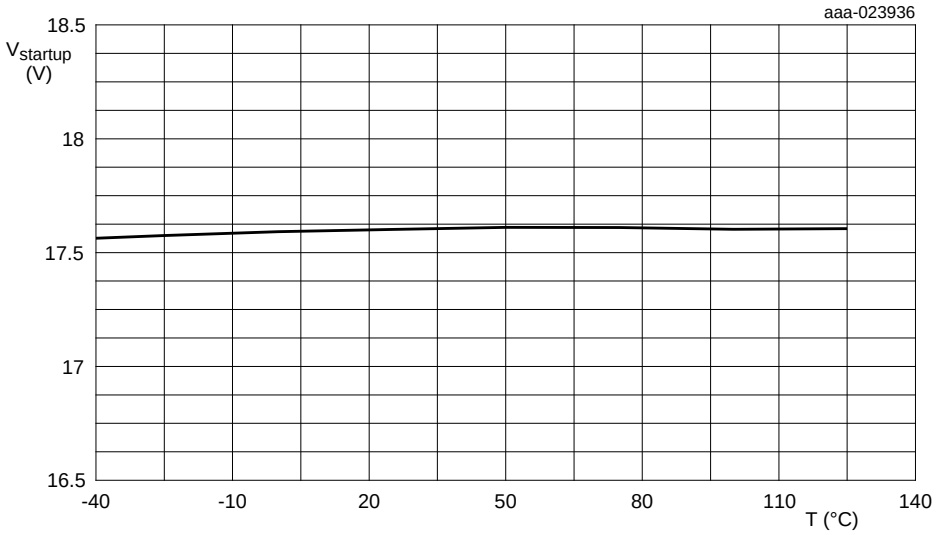


Figure 8. start-up voltage as a function of temperature

12.1.2 Undervoltage lockout threshold voltage

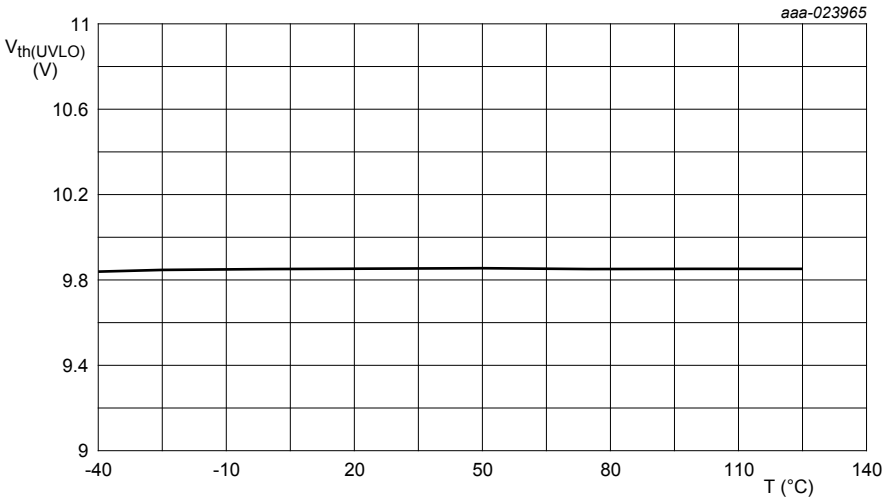


Figure 9. Undervoltage lockout threshold voltage as a function of temperature

12.1.3 Detection voltage (pin PROTECT)

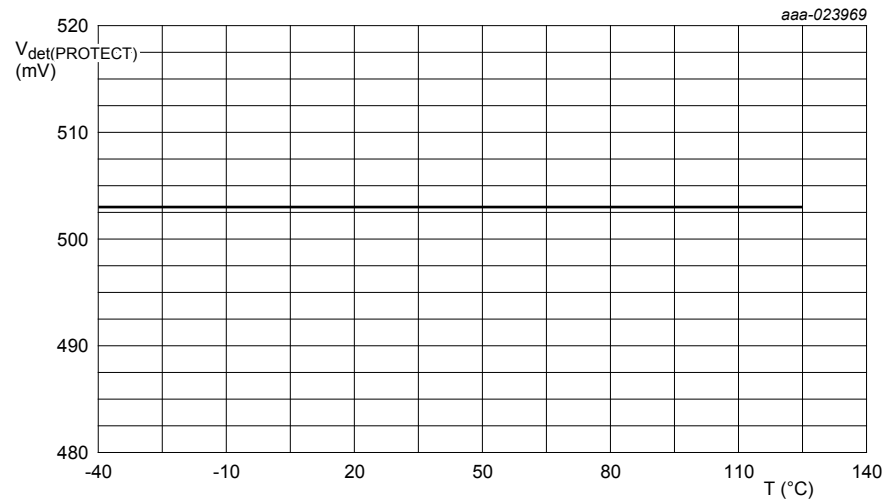


Figure 10. Detection voltage (pin PROTECT) as a function of temperature

12.1.4 Switching frequency

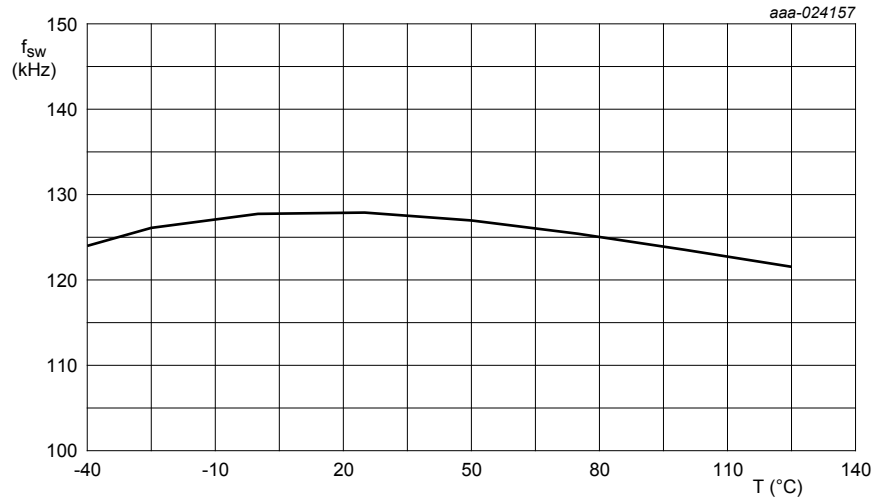


Figure 11. Switching frequency as a function of temperature

12.1.5 Overpower protection voltage (pin ISENSE)

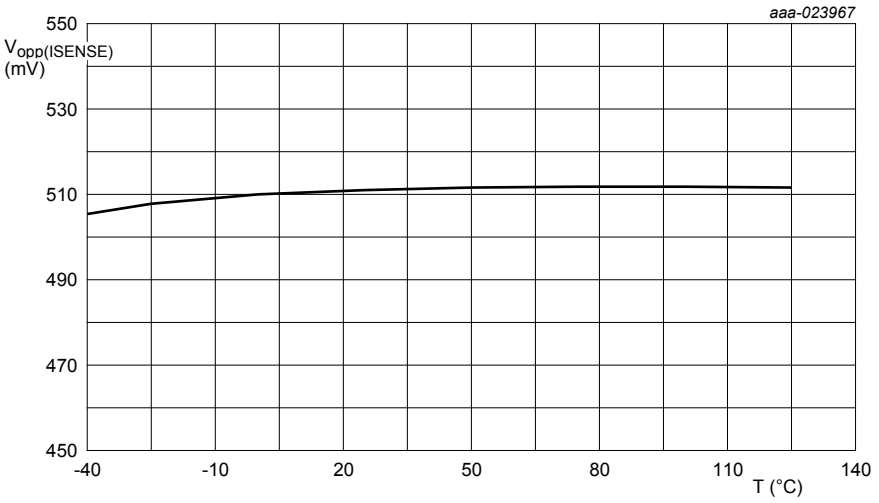


Figure 12. Overpower protection voltage (pin ISENSE) as a function of temperature

12.1.6 Overpower protection (at I_{AUX} = 1.46 mA)

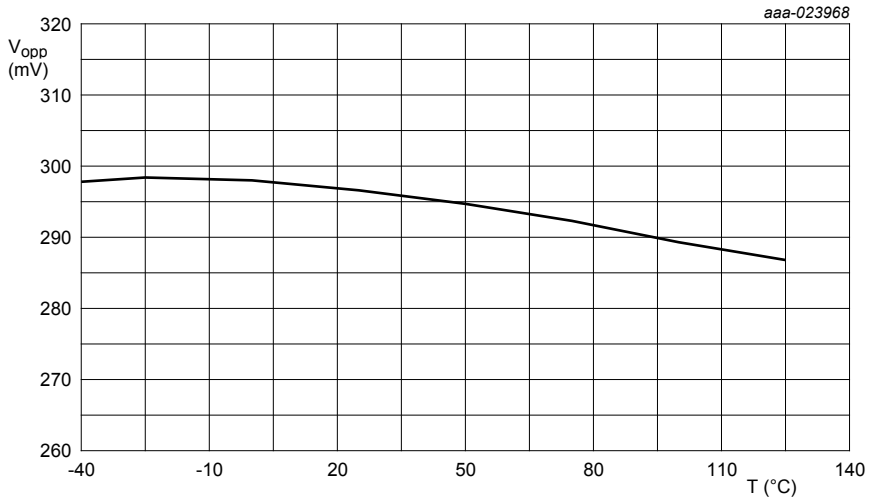


Figure 13. Overpower protection voltage (at I_{AUX} = 1.46 mA) as a function of temperature

12.1.7 Output current (pin PROTECT)

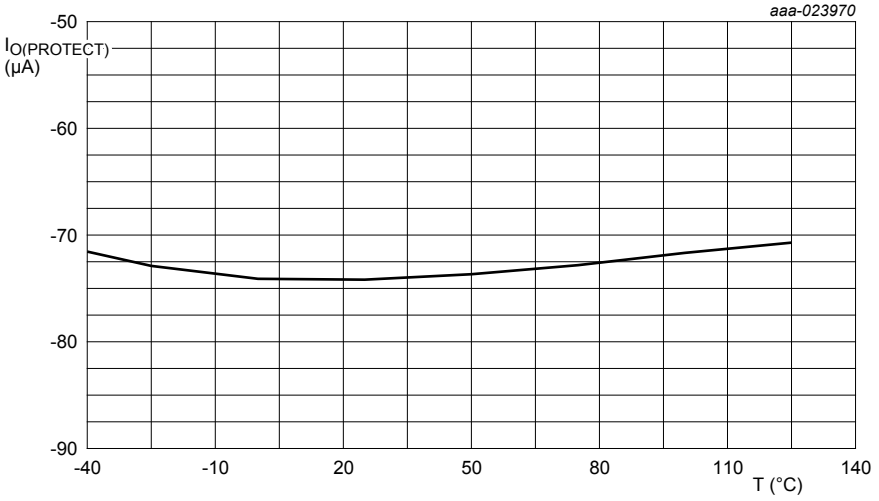


Figure 14. Output current (pin PROTECT) as a function of temperature

12.1.8 Overvoltage protection voltage (pin AUX)

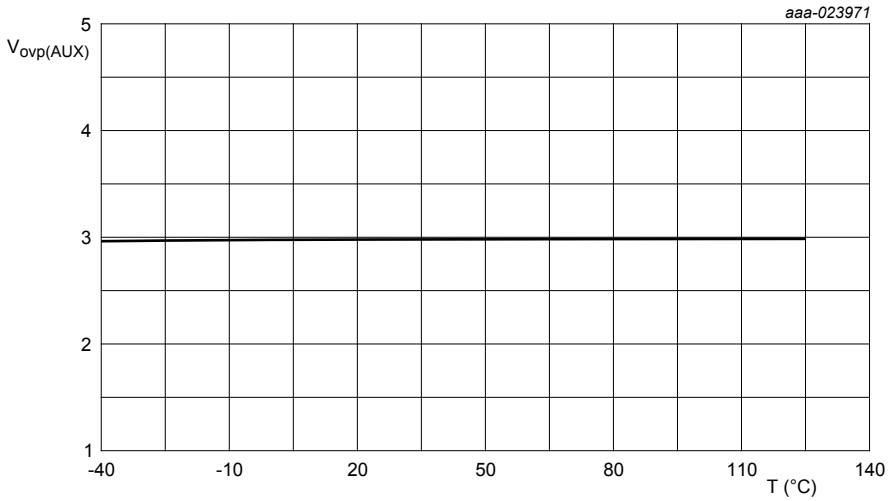


Figure 15. Overvoltage protection voltage (pin AUX) as a function of temperature

13 Application information

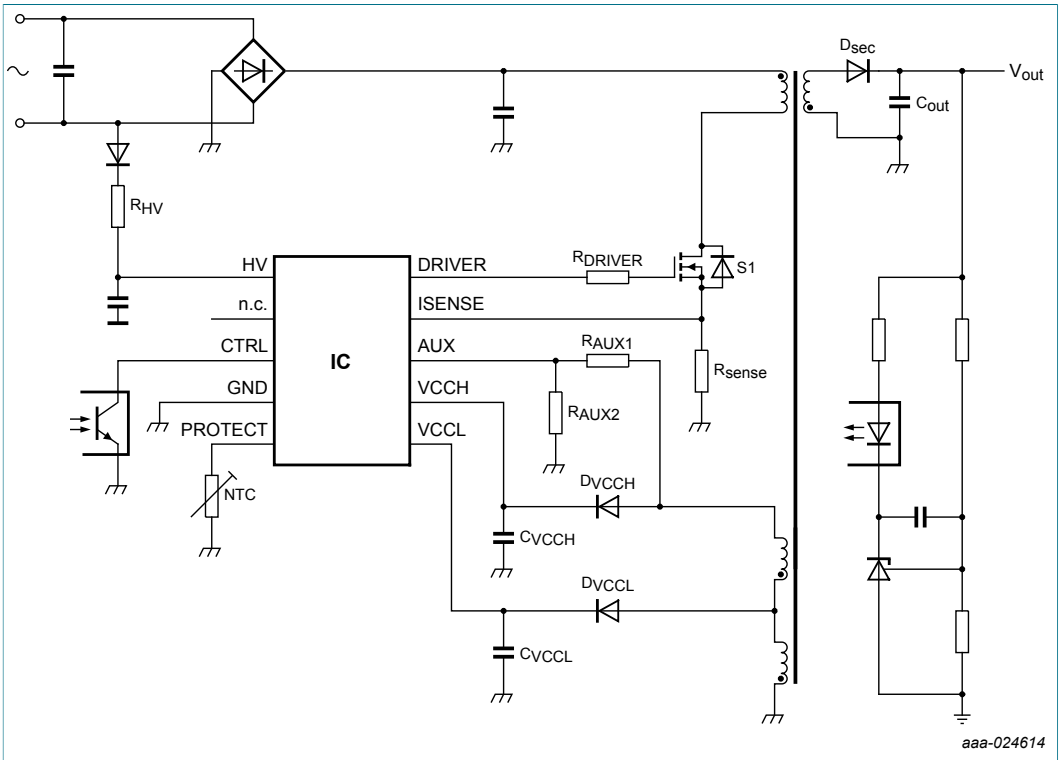


Figure 16. TEA1938T application diagram

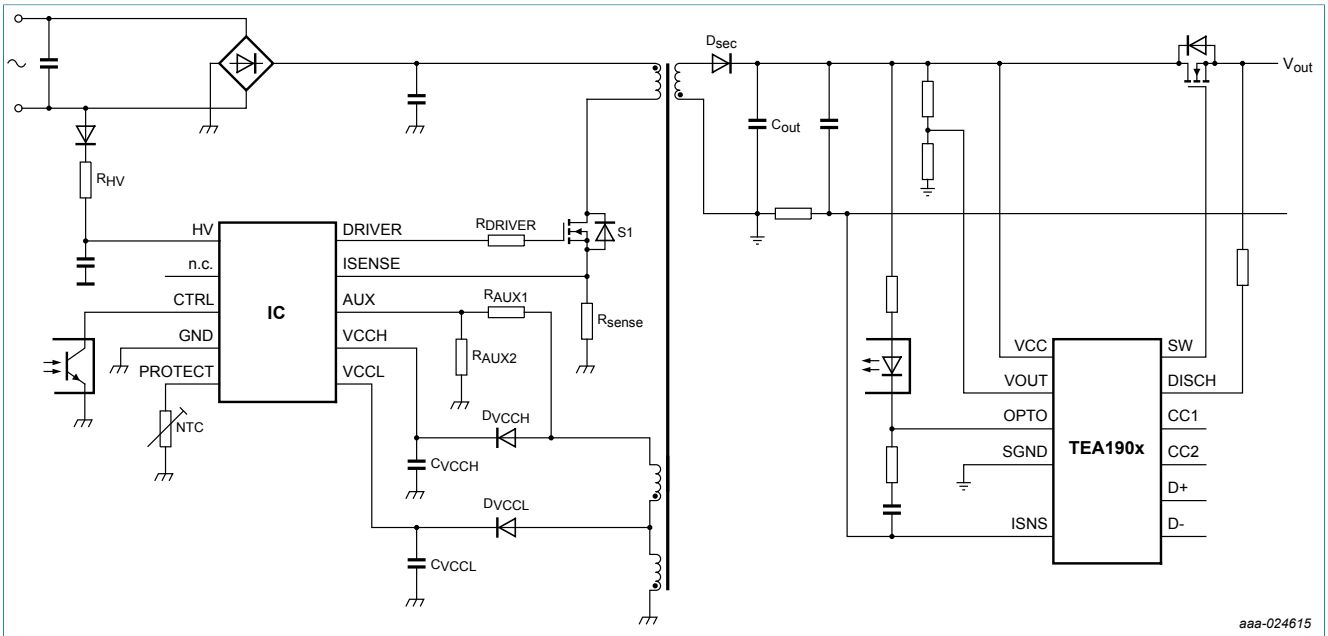
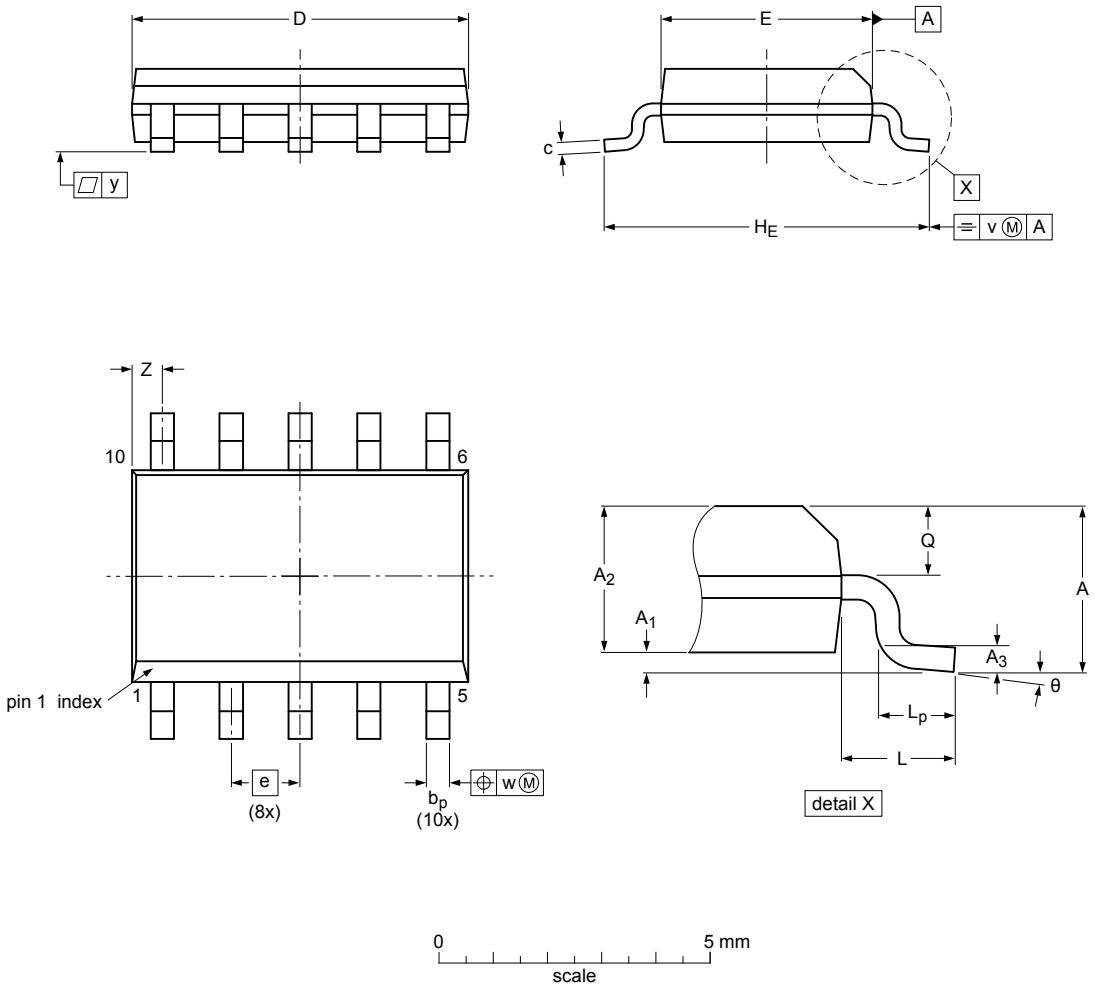


Figure 17. TEA1938T application diagram with TEA190xT

14 Package outline

SO10: plastic small outline package; 10 leads; body width 3.9 mm; body thickness 1.35 mm **SOT1437-1**



Dimensions

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.75	0.25	1.45		0.49	0.25	6.3	4.0		6.20		1.00	0.70				0.70	8°
	nom		0.18	1.35	0.25	0.43	0.22	6.2	3.9	1.27	6.00	1.05	0.70	0.65	0.25	0.25	0.1	0.56	4°
	min		0.10	1.25		0.36	0.19	6.1	3.8		5.80		0.40	0.60				0.30	0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1437-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1437-1						~~15-02-09~~ 15-03-06

Figure 18. Package outline SOT1437-1 (SO10)

15 Abbreviations

Table 9. Abbreviations

Acronym	Description
CC	Constant Current
CV	Constant Voltage
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR	Frequency Reduction
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCP	OverCurrent Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
QR	Quasi-Resonant
SMPS	Switch Mode Power Supply
SOI	Silicon-On-Insulator
UVLO	UnderVoltage LockOut
VCO	Voltage Controlled Oscillator

16 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1938T v.1	20170901	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 September 2017
Document identifier: TEA1938T