Application Report
SPRAC54A–April 2017–Revised November 2017

66AK2Gx Schematic Checklist

1 Introduction

This article applies to the 66AK2Gx.

TI hardware designs based on the 66AK2Gx: 66AK2Gx (K2G) General Purpose EVM

Check the 66AK2Gx errata when designing a board (see the product folder on ti.com). This has important information on silicon issues which may alter your board design. Also check these other useful links:

- 66AK2Gx BGA Escape Routing Guidelines
- TI Pinmux tool

2 Recommendations Specific to 66AK2Gx

2.1 EVM versus Data Sheet

In case of any discrepancy between the TI EVMs and the device data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors which, while functional, are not completely aligned with the data sheet specification. Thus, the EVM designs should not be considered as reference designs and should not be blindly reused.

2.2 Power

- Check that the correct voltages are applied to the correct power pins on the chip, and that the required current can be supplied.
- Zero ohm resistors in line with the core and other power sections of the board are recommended for initial PCB prototype builds, if the user wants to measure power. The user should then remove the resistor in the production builds, and connect the power planes with wide copper or multiple vias. Power measurement is the purpose of these resistors in the EVM designs. The implementation of these resistors adds inductance and resistance that can impair power supply and power distribution performance.
- Proper power supply sequencing in proper correlation with resets and clocks is required. Refer to the device-specific data sheet for the recommended power sequencing requirements.
- Each of the VDDAHV power input pins should be connected to DVDD18 through a filter circuit.
- The DDR3 interface requires a VTT termination at the end of the flyby chain for the DDR3 address, command, control, and clock signals. The VTT termination voltage is generated using a special push/pull termination regulator specifically designed to meet the VTT requirements for DDR3.
- The VTT regulator can also provide the voltage rail for the DDR reference voltage. If not, a voltage divider using tight tolerance (1% or better) resistors can be used. If a resistor divider is used, the VREFSSTL source voltage must be generated from the DVDD_DDR supply, allowing it to track that supply.
- C66AK2Gx devices contain multiple analog power pins that provide power to sensitive analog circuitry, such as PLLs, DLLs, and SERDES buffers and terminations. These must be attached to filtered power sources. These filter solutions must match the recommendations in the Hardware Design Guide.
- The internal LDO regulators on the 66AK2Gx require external capacitors connected to their output pins (LDO_PCIE_CAP, LDO_USB_CAP). Place a 1-µF capacitor from each of these LDO outputs to ground (VSS). See the 66AK2Gx Data Manual (SPRS932) for the list of LDO outputs. These capacitors must

be placed as close to the respective pin as possible (within 0.25" of the package boundary).

- If OTP eFuse programming is needed for secure devices, the voltage must be supplied to the VPP pins on the 66AK2Gx. This supply rail has specific ramping and sequencing requirements. Check that the power supply used meets the requirements found in the data manual.

Texas Instruments supports a PMIC device designed specifically for use with the 66AK2Gx. The use of the PMIC is not required. A discrete power supply solution may be implemented, but care should be taken to ensure that the power supply meets the requirements specified in the 66AK2Gx data manual and the Power Consumption Estimation Tool, including sequencing, voltage levels, regulation, and current capabilities.

2.2.1 PMIC

- Review the TPS659118 User's Guide for 66AK2Gx Processor (SWCU176). Also check the product data sheet for specific part numbers to be used for the 66AK2Gx operating at 600 MHz.. The following part numbers are recommended:

  TPS659118
- Review the TPS65911A User's Guide for 66AK2G12 Processor (SWCU187). Also check the product data sheet for specific part numbers to be used for the 66AK2Gx operating at 1 GHz. The following part number is recommended:

  TPS65911A (implemented on the 66AK2Gx GP EVM)
- Ensure that the current capabilities of the DC/DC switchers and LDOs meet the maximum demand of all attached devices. Find the maximum current draw of all 66AK2Gx I/O rails in the Power Consumption Model for 66AK2Gx. If the rails from the PMIC also power other devices, the maximum current draw of these devices should also be considered.
- Ensure I2C1 is used for communication to PMIC. All TI software distributions (Linux® SDK) assume the use of this interface with the PMIC.

2.2.2 Discrete Power Supplies

- Ensure that each supply selected meets the requirements for the rail it is supporting.
- If the voltage level selected for CVDD and CVDD1 are the same, these pins may be driven by a single power supply. Include the current requirements for both rails when specifying the power supply.
- Ensure that the power supply sequencing for each rail matches the sequence specified in the 66AK2Gx data manual. A subset of the supply rails should not be powered for a significant period of time. When the sequencing has begun, each rail should be powered within 80 ms of the previous rail in the sequence.
- If a power supply is used for both the 66AK2Gx and other components on the board, select a power supply rated for the current needed by all components.
- If separate IO supplies are used for the 66AK2Gx and for other components in the design, ensure that the IOs of the 66AK2Gx are not driven before the power supply for the IO cell is present. IO cells for the 66AK2Gx are not fail-safe. Driving an IO before the power supply for the IO cell is present can result in excessive current, and can damage the IO cell.

2.3 Reset

- TI recommends that the hard reset PORn be driven from power good circuitry to assure proper sequencing. Power should be stable, and input clock signals should be present before PORn is released. Check the data manual for details about the requirements of PORn.
- The RESETFULLn is provided as a second reset capable of placing the part in the power-on reset state. If not used, RESETFULLn should be pulled to DVDD33.
- Reset pins must be driven as defined in the device data manual. This sequencing in relation to clocks and power supply ramping must be followed in all operating conditions, including boundary scan testing.
- The PORn pin has special properties, which holds all output pins at high impedance when low. When controlled from logic derived from a power good indication, it can safely shut down the device and prevent output contention if a power supply fault occurs.

- All control pins must be held at the proper input level prior to the rising edge of PORn. The rising edge of PORn captures the bootmode and configuration signals which are latched.
- RESETSTATn is driven low whenever the device enters the reset state. RESETSTATn is undefined until the power supplies are stable, and then remains low until the 66AK2Gx exits the reset state. Ensure peripheral reset inputs can handle this. If there is sensitivity, add a 100-Ω resistor in series before sending RESETSTATn to peripheral circuits. Check the EVM schematic for an example.

2.4 Boot Modes

- BOOTMODE pins must be properly configured and at a stable voltage level to specify the proper boot mode before the rising edge of PORn. These can be set by resistor population or driven from logic such as an FPGA.

NOTE: If pulling resistors are used, all BOOTMODE and configuration pins should have a resistor present.

- If the BOOTMODE pins are redefined for another purpose during operation, they must be released and set back to the proper levels to select the boot mode whenever PORn goes low.

2.5 Unused Signals

Signals on unused interfaces can typically be left as no connect. Check the Pin Attributes table to determine if the unused pin has an internal pulling resistor during reset. If the pin does not have an internal pulling resistor active during reset, an external pulling resistor should always be included in the design. If present, the internal pulling resistor holds the unused pin in a known state, provided no external connection is made to the pin. If any trace or via is connected to the pad for an unused pin, an external pulling resistor must be included in the design. This includes test points, test headers, and dogbone connections for a fully populated CAD footprint.

2.6 Unused Power Rails

The 66AK2Gx requires that all power rails be present when the SoC is in use. Failure to power any of the rails could result in damage to the part.

2.7 System Issues

2.7.1 Pullup Resistors

Ensure all pullups connected to 66AK2Gx are pulled up to the correct I/O voltage, to avoid any leakage between the I/O rails of the device. Each terminal has an associated supply voltage used to power its I/O cell. This can be found in the 66AK2Gx data sheet, in the Ball Characteristics table.

Most signal pins on the 66AK2Gx have internal pulling resistors present by default when the device is in reset. If an external pulling resistor is used to pull the signal high or low in opposition to the internal pulling resistor, it must be of sufficient strength to avoid a mid-voltage condition. A mid-voltage condition results in high-leakage current, which could damage the IO cell.

2.7.2 Peripheral Clock Outputs

Put series resistors (close to processor) on the output clocks of the following modules: MMC, GPMC, McASP (both clock and frame sync), SPI, and QSPI. The value of the resistor should be determined using simulation of the PCB. Generally, a 22-Ω resistor is a good starting value.

2.7.3 General Debug

The output clock SYSCLKOUT is present on a dedicated pin. TI recommends having a test point for this signal output. SYSCLKOUT can be used to determine the output frequency of the main PLL before and after it is programmed. The SYSCLKOUT can be disabled using a control register to prevent EMI.

2.8 Low Power Considerations

If designing for low power, optimize the design for low power:

- On early prototype boards, TI recommended to include small shunt resistors in the voltage rail paths of each of the following power rails of 66AK2Gx: CVDD, CVDD1, DVDD33, DVDD_DDR, and DVDD18. (These are listed in order of priority; if they cannot all be isolated, the most important appear at the beginning of the list. The filter components for the AVDDA_xxxxx supplies may used as measurement points if needed.) This helps to measure the power consumption of each rail, and potentially pinpoint high-power consumption during development. The user can also add these shunt resistors for power supplies connected to other devices, to measure power on those key devices. The 66AK2Gx EVMs have examples of these shunt resistors.

NOTE: Measurements should never be substituted for the data provided by the Power Consumption Model when determining limits for the power supply design. There can be a wide variation in current consumption between 66AK2Gx devices at different process levels and at different temperatures.

For production, these shunt resistors must be removed from the design (that is, turned into a continuous plane), because these resistors restrict current flow and add inductance to the PDN.

2.9 Clocking

- When the using a crystal, connect VSS_OSC_SYS or VSS_OSC_AUDIO to board ground.
- If the internal oscillator is used, it is preferable to always have bias and dampening resistors that can help tune the crystal. See the OSC0 External Crystal section of the device data sheet for more details.

2.10 General DDR Guidelines

- Follow the DDR3 routing guidelines in the 66AK2Gx data sheet. These guidelines ensure a proper DDR3 operation.
- When using a resistor divider for DDR_VREF, ensure resistors are high-precision resistors (1% or better), as specified in the data sheet.
- Provide adequate decoupling capacitors on the DDR power rails, both at the 66AK2Gx as well as at the DDR SDRAM devices. Proper distribution of these capacitors is mandatory when referencing fly-by signals to DVDD_DDR.
- Designs with point-to-point connections between the 66AK2Gx and a single DDR3 SDRAM typically do not need VTT termination, although this may be needed depending on the specific PCB characteristics. For multiple device topologies or multi-die packages, VTT termination is required unless complete simulation of the interface is performed. A VTT termination regulator is required for properly terminating the address, command, and control fly-by signals. Check the data sheet or reference schematic for proper connection. TI recommends the TPS51200 for use as the VTT termination regulator.
- Do not connect DDR_RESET to VTT termination resistors. DDR_RESET should be connected directly between the 66AK2Gx and the SDRAMs. TI also recommends the addition of a pulldown resistor.
- Check the data sheet for proper termination voltages. Termination for the fly-by clock signals is to DVDD_DDR (through termination resistors to a balancing coupling capacitor), whereas all other fly-by signals must use terminations resistors connect to VTT for the termination voltage. Refer to the device data sheet for details.
- VREF can be obtained from the VTT termination regulator or from a resistor divider (2.2 kΩ 1% resistors) with capacitive decoupling to ground. It is used as references for both CA and DQ pins on the memory, as well as the VREF signal on the 66AK2Gx. Ensure resistors are a high precision (1% or better) resistors, as specified in the data sheet. Follow the VREF routing guidelines in the data sheet.
- If a particular DDR interface is not used, then the applicable DDRx_DQS and DDRx_DQSn should be tied to the appropriate GND or power through a 1-kΩ resistor to keep the signals inactive. See the 66AK2Gx data manual for complete directions for the termination of unused pins.

2.11 MMC0

- MMC0 signals use IO buffers powered by DVDD33, and can be connected directly to 3.3-V IOs of an SD-CARD or an eMMC memory.
- Include a series resistor on MMC0_CLK (as close to the processor as possible). The value of the resistor should be determined from simulation of the PCB. Generally, a 22-Ω resistor is a good starting value. This signal is used as an input on read transactions, and the resistor eliminates possible signal reflections on the signal which can cause false clock transitions.
- Pullup resistors are needed on all data signals and on the command signal. These pullups should be 10 kΩ for SD-CARD implementations, and 49.9 kΩ for embedded device connections, such as eMMC memory devices.
- Internal pull-down resistors should be disabled for MMC0 signals. Pulling resistors are disabled using the padconfig registers for each signal.

2.12 MMC1

- MMC1 signals use IO buffers powered by DVDD18, and cannot be connected directly to 3.3-V IOs of an SD-CARD or an eMMC memory. All IO signals must be connected through a voltage conversion IC. This includes the MMC1_CLK, MMC1_CMD, MMC1_DATA[7:0], MMC1_POW, MMC1_SDCD, and MMC1_SDWP signal. If the signal is pulled high, it must be pulled to DVDD18.
- Include a series resistor on MMC1_CLK (as close to the processor as possible). The value of the resistor should be determined from simulation of the PCB. Generally, a 22-Ω resistor is a good starting value. This signal is used as an input on read transactions, and the resistor eliminates possible signal reflections on the signal, which can cause false clock transitions.
- Pullup resistors are needed on all data signals and on the command signal. These pullups should be 10 kΩ for SD-CARD implementations, and 49.9 kΩ for embedded device connections, such as eMMC memory devices.
- Internal pull-down resistors should be disabled for MMC1 signals. Pulling resistors are disabled using the padconfig registers for each signal.

2.13 I2C

- Pullup resistors must be attached on all I2C signals (I2Cx_SDA and I2Cx_SCL) and should be 2.2K. Ensure the pullup resistors connect to the DVDD33 voltage rail. See Section 2.7.1.
- If planning to use TI's software (Linux SDK), connect I2C1 to the PMIC, as this is the port used for PMIC control.
- All I2C interfaces use true open-drain buffers fully compliant to the I2C specifications. These support 100-kHz and 400-kHz operation.

2.14 NAND

Typically the R/B# signal from the NAND is open-drain and connected to the 66AK2Gx GPMC_WAIT signal. Include a 4.7K pullup to the DVDD33.

2.15 USB

- Refer to the High-Speed Interface Layout Guidelines Application Report (SPRAAR7) for detailed recommendations for proper USB signal connection and routing.
- For USB device operation, USB VBUS decoupling capacitance should be < 10 µF.
- For USB host operation, USB VBUS decoupling capacitance should be > 120 µF.
- Ensure the VBUS decoupling capacitance is connected close to USB connector.
- USBx_DP and USB_DM should never have any series resistors or capacitance on these signals. These signals should be straight traces to the connector with no stubs or test points.
- Typical connections of the 66AK2Gx for a USB Device:
  - USBx_DP and USBx_DM are connected directly to the USB connector
  - Connector ID pin can be left unconnected
  - USBx_DRVVBUS is not used and can be left unconnected

- If there is a possibility that the USB interface will be connected to a host before the voltage for the 66AK2Gx is present, the USBx_VBUS pin for the 66AK2Gx has fail-safe protection, which allows the VBUS pin on the USB connector to be connected directly. This is not true of all TI parts.
- Typical connections of the 66AK2Gx for a USB host:
  - USBx_DP and USBx_DM are connected directly to the USB connector
  - Connector ID should be grounded
  - USBx_DRVVBUS should be connected to the enable of the 5-V VBUS power source
  - Connector VBUS should be connected to the output of the 5-V VBUS power from the power switch by USBx_DRVVBUS
- Typical connections for a USB host with USB hub:
  - USBx_DP and USBx_DM are connected directly to the USB hub upstream port (hub then distributes these signals to the downstream ports as needed)
  - Connector ID should be grounded to enable host mode
  - USBx_DRVVBUS should be unconnected
  - USBx_VBUS should be connected to the output of the 5-V VBUS power source. It is also connected to the VBUS detect on the hub, which then allows the hub to selectively enable or disable typically through a power switch to each downstream port.
- USB signals have special routing requirements. It is always a good practice to reference the routing requirements in the schematic.

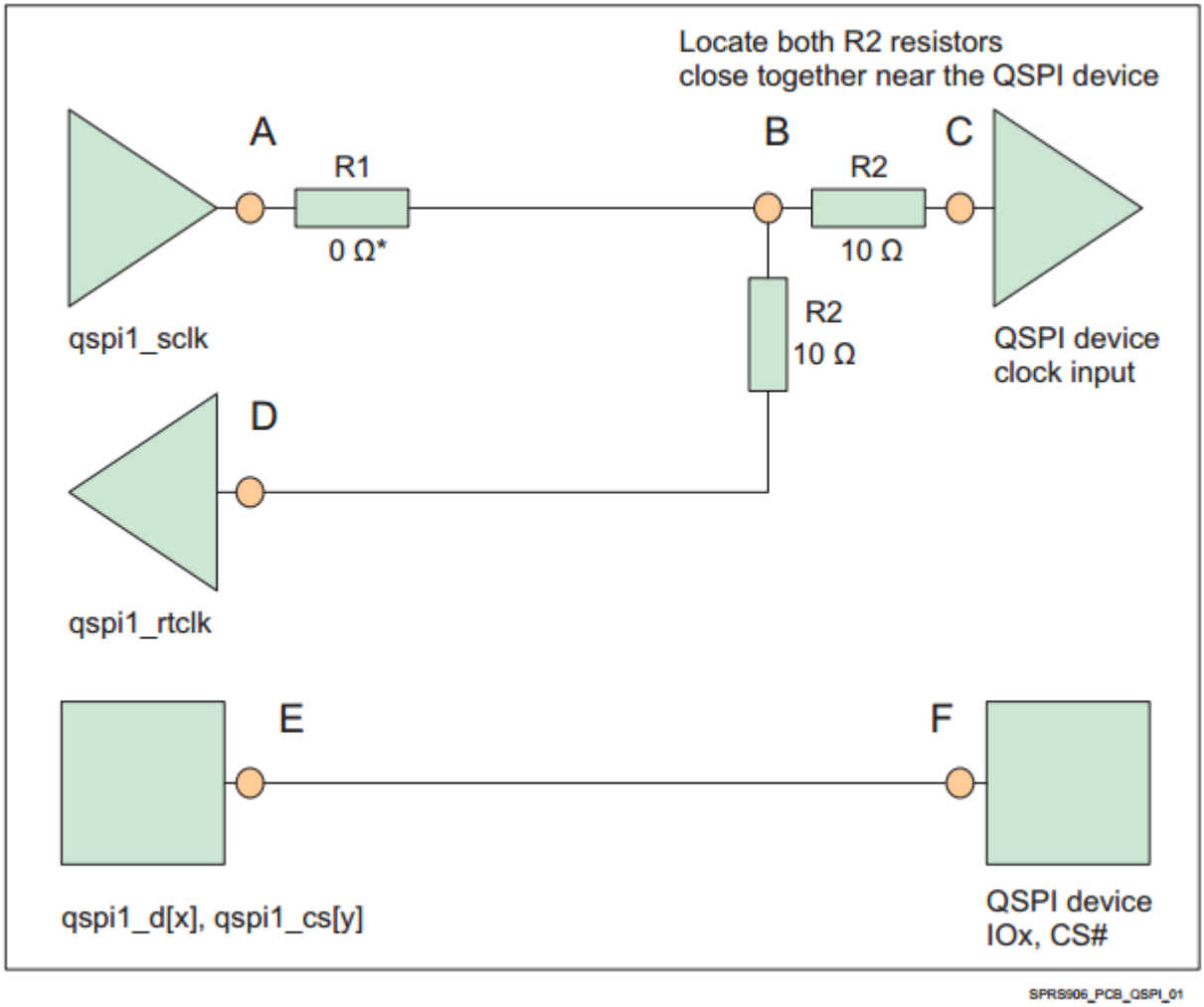
2.16 Ethernet

- No series resistors are required for MII signals. They may be implemented on the clock signals, if the routes are long or through a connector.
- For the RGMII interfaces, 22-Ω series termination resistors must be placed on all 12 interface signals, as close to the transmitting I/O a possible. Check voltage compatibility between the 66AK2Gx I/O and the Ethernet PHY I/O.
- RGMII signals have special routing requirements. It is always a good practice to reference the routing requirements in the schematic.

2.17 QSPI

- The QSPI interface includes both the QSPI_CLK signal and the QSPI_RCLK signal. For proper operation, the QSPI_CLK must be connected to both the CLK input on the QSPI device and the QSPI_RCLK input. The proper length matching must be achieved, and including some additional resistors between these connections can help.
  - Place a 0-Ω resistor close to the QSPI_CLK output. This allows the clock signal to be tuned by allowing a series termination.
  - Place a 10-Ω resistor close to the clock CLK input for the QSPI device. This resistor should be located close to that device.
  - Place a second 10-Ω resistor close to the QSPI device, connected to the QSPI_CLK on one end and the QSPI_RCLK on the other end.
- If the schematic tool allows, include the length matching requirements based on Figure 1.
  - Length A to B < 450 ps
  - Length B to C < 60 ps
  - Length A to C = Length C to D = Length E to F to within 60 ps

Figure 1. Length Matching Requirements



2.18 PRU

- The PRU module provides an extra layer of pin multiplexing, using the internal wrapper multiplexing. This is described in the PRU-ICSS I/O Interface section of the K2G TRM (SPRUHY8). The internal wrapper multiplexing is included in the use cases listed for the PRUSSx_PRU in the PINMUX tool. Use the table in the TRM to determine the proper GPI and GPO selections for the internal wrapper multiplexing selection.
- Both the GPIx/GPOx signal name selected by the PADCONFIG register and the signal name associated with the internal wrapper multiplexing should be associated on the schematic page. They could both be included in the pin name for the SoC, or a cross-reference table could be included on the schematic page. This can be cross-checked against the internal wrapper multiplexing table in the TRM to ensure the schematic is correct.
- For the MII interfaces, 22-Ω series termination resistors must be placed on all interface signals, as close to the transmitting I/O as possible. Check voltage compatibility between the 66AK2Gx I/O and the Ethernet PHY I/O. If a different voltage is needed by the PHY, voltage translation logic must be included in the design.
- Always consult the Ethernet PHY data manual for specific schematic requirements. Many PHYs use pulling resistors on MII signals to determine initial configuration. The internal pulls on the PRU signals using the PADCONFIG register may need to be modified to prevent conflict with the pulls needed by the PHY. Never rely on the internal pulling resistors to establish the initial configuration for the PHY. If the PHY requires a pullup or pulldown, an external resistor should be included in the design.

2.19 JTAG and EMU

- Clock and signal buffering are required whenever the JTAG interface connects to more than one device. Clock buffering is strongly recommended even for single device implementations. Verify series terminations are provided on each clock buffer output, and ideally, that the clock output tracks are skew matched.
- EMU pins must not be buffered. EMU[1:0] can be bussed to multiple devices. Other EMU pins connected for trace usage must be short and skew matched.
- For more recommendations on EMU routing, refer to Emulation and Trace Headers Technical Reference Manual (SPRU655).
- Similarly, a summary of this information is available at XDS Target Connection Guide.
- Adaptive clocking must be implemented correctly using the RTCK output.
- If the JTAG and EMU interface is not used, all pins except TRSTn and TMS can be left floating. TRSTn must be pulled low to ground through a 4.7-kΩ resistor, and TMS must be pulled to VDDSHV3 through a 4.7-kΩ resistor. However, TI strongly recommends that all board designs contain at least a minimal JTAG port connection, to test points or a header footprint to support early prototype debugging. The minimum connections are TCK, RTCK, TMS, TDI, TDO, and TRSTn. JTAG routes and component footprints (except the PD on TRSTn and the PU on TMS) can be deleted in the production version of the board, if desired.
- In the event that the JTAG interface is used and the EMU interface (or a subset of the emulation pins) is not used, the unused EMU pins can be left floating.

2.20 PCIe

- Refer to the High-Speed Interface Layout Guidelines Application Report (SPRAAR7) for detailed recommendations for proper USB signal connection and routing.
- DC blocking caps are needed on the reference clock input.
- DC blocking capacitors are required for data lanes, and should be implemented on the TX end.
- If the PCIE subsystem is connected as a root complex, the design must include a 100-MHz reference clock source for PCIE_CLK. If a reference clock is provided to a PCIE backplane connector, it should be generated from the same source, but connected to a different clock driver.
- If the PCIE subsystem is connected as an endpoint, it is always best to connect the reference clock provided by the root complex. If the root complex provides a spread-spectrum reference clock, the PCIE subsystem may not connect if a separate clock is connected to the PCIE_CLK.
- If the PCIE subsystem is not used in the design, the PCIE_CLK input is not needed, and can be terminated as defined in the 66AK2Gx Data Manual. Software should never attempt to access the PCIE subsystem if the PCIE_CLK is not present. This could result in a software hang.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision	Page
• Updated Power section.	2
• Updated PMIC section.	2

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265