Application Report
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# 66AK2G1x: EVMK2GX General Purpose EVM Power Distribution Network Analysis

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**ABSTRACT**

The purpose of a power distribution network (PDN) is primarily to provide clean and reliable power to the active devices on the system. The printed circuit board (PCB) is a critical component of the system-level PDN delivery network. As such, optimal design of the PCB power distribution network is of utmost importance for high performance microprocessors. This application report provides implementation guidelines and recommendations for designing printed circuit board (PCB) power delivery networks (PDN) for the Texas Instruments 66AK2G1x microprocessor.

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# 1 Introduction

This application report provides implementation guidelines and recommendations for designing printed circuit board (PCB) power delivery networks (PDN) for the Texas Instruments 66AK2G1x microprocessor. This application report will:

- Discuss PCB PDN design methodology
- Provide general PCB PDN design recommendations and requirements
- Discuss the rationale behind these design requirements
- Provide suggestions and methods that PCB designers can implement to ensure that the PDN requirements for a specific processor are met.

## *1.1 Acronyms Used in This Document*

**Table 1. Acronyms**

| Acronym | Description |
|---|---|
| AC | Alternating current |
| BGA | Ball grid array |
| DC | Direct current (static) |
| Df | Loss tangent |
| Dk | Dielectric constant |
| EDA | Electronic design automation |
| EM | Electromigration |
| ESL | Effective series inductance |
| ESR | Effective series resistance |
| FDTIM | Frequency domain target impedance method |
| HDI | High density interconnect (for example, buried/blind via) |
| IR | Product of current (I) x resistance (R) |
| PCB | Printed circuit board |
| PDN | Power distribution network |
| PM-IC/PMIC | Power management integrated circuit |
| PTH | Plated through hole |
| RLC | Resistance, inductance, and capacitance |
| SMPS | Switch mode power supply |
| SMT | Surface mount technology |
| SRF | Self resonant frequency |
| VIP | Via in pad |
| VRM | Voltage regulator module |

**NOTE:** Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this document are intended as guidelines only.

## 2 Guidelines for PCB Stack-Up

The PCB stack-up (or layer assignment) is an important factor in ensuring optimal performance of a power distribution scheme. An optimized PCB stack-up for improved power integrity performance can be achieved by following these recommendations:

- Power and ground plane pairs/"islands" should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply. Whenever possible the power and ground planes should be solid to provide a continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair so minimizing the separation distance (the dielectric thickness) will help to maximize the capacitance.
- Keep the power and ground plane pair as close to the PCB top and bottom surfaces as possible (see Figure 1). This will help to minimize the associated loop inductance of the decoupling capacitors, vias, and the power/ground plane pair spreading loop inductance.

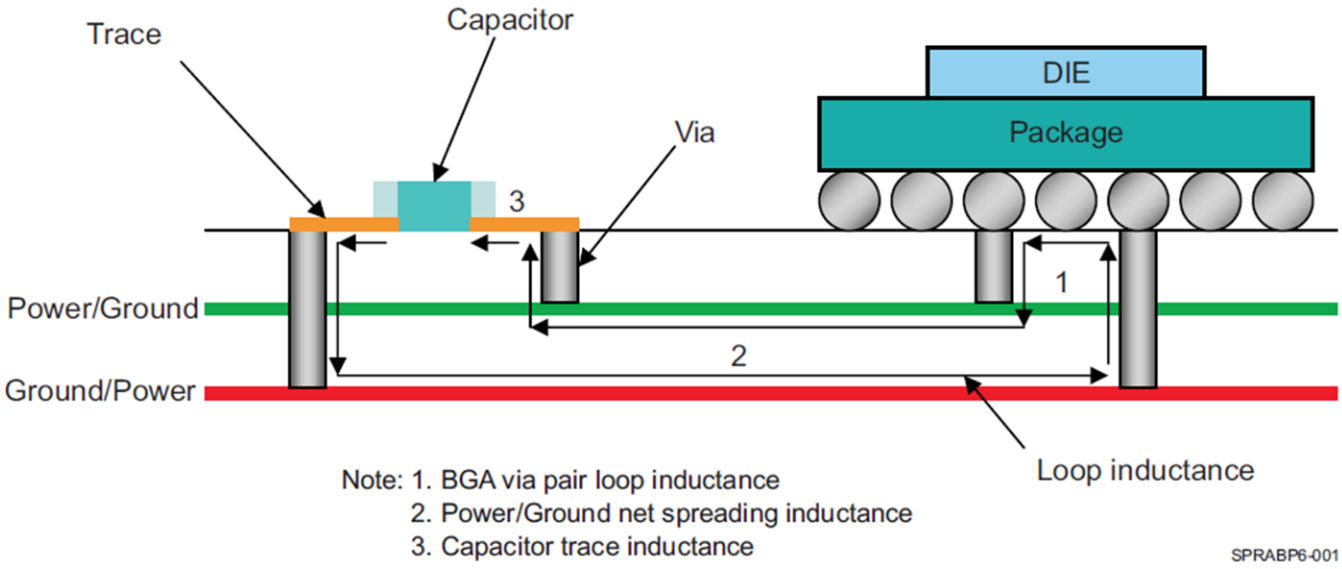


**Figure 1. Minimize Loop Inductance by Optimizing Layer Assignments in the PCB**

The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductance of the power current path as shown above. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stack-up and low-priority supplies in the bottom half of the stack-up as shown in the examples below. Figure 2 and Figure 3 show examples of typical PCB stack-ups designed with power distribution performance in mind. Device-specific stack-up examples can be found in Section 8.

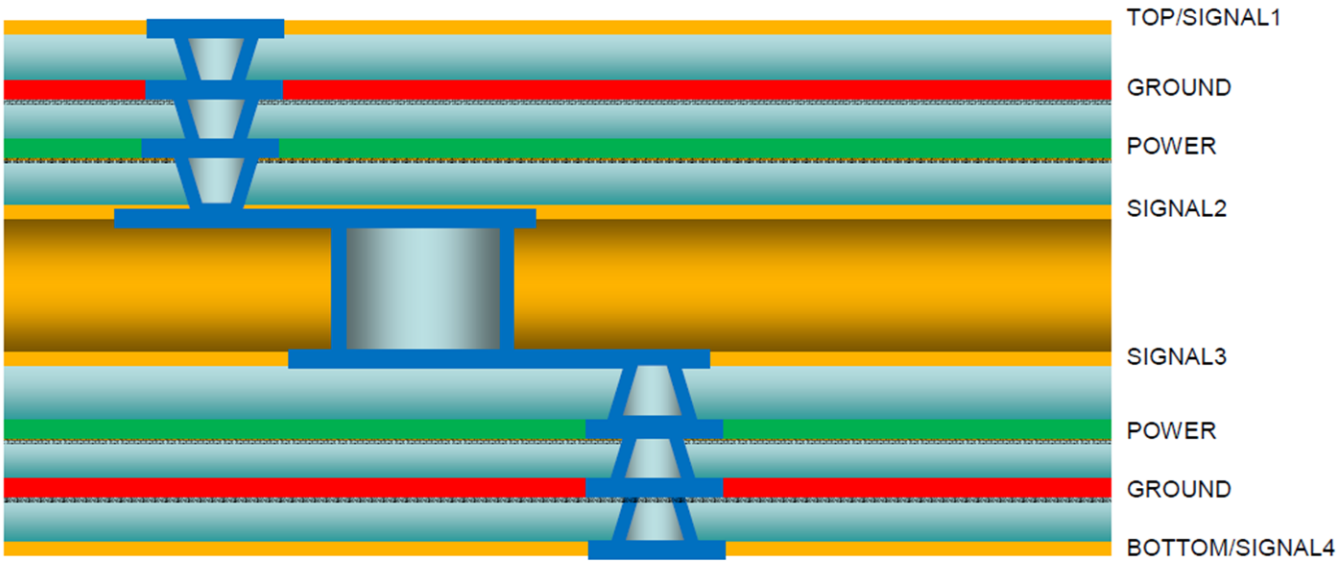


**Figure 2. Example Stack-Up Utilizing High-Density Interconnect Vias**

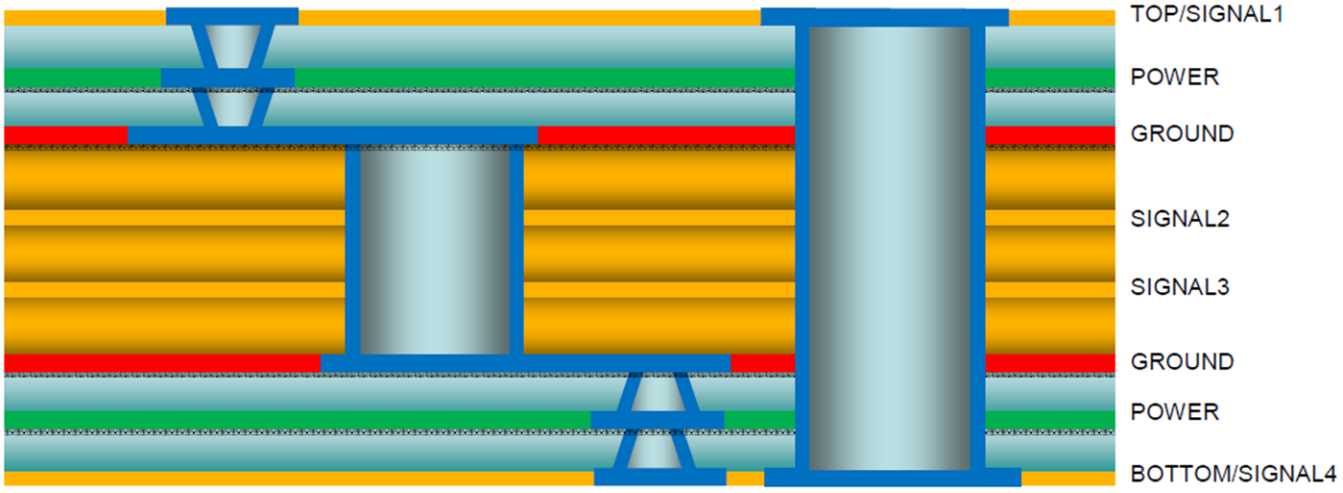


**Figure 3. Example Stack-Up Utilizing Plated-Through-Hole (PTH) Vias**

## 3 Physical Layout Optimization of the PDN

The following are important requirements that need to be implemented in the PCB PDN design:

- External power trace routing between components should be as wide as possible as wider traces result in reduced DC resistance and consequently a lower static IR drop. They also provide for lower loop inductance and higher capacitance.
- Whenever possible, attempt to achieve a ratio of 1:1 (or better) for component pins and associated vias. Do not share vias among multiple capacitors.
- Placement of decoupling capacitors and associated vias should be as close to the processor ball as possible.
- The maximum current-carrying capacity of each transitional via should be evaluated through simulation to determine the appropriate number of vias required to connect components. This ensures that the current-carrying ability of a via interconnect network is sufficient for the needs of each particular component. When a via interconnect, or a network of same, is unable to supply sufficient current, this is referred to as “via starvation”.
- TI highly recommends that both static and dynamic IR drop analysis (discussed in Section 4 and Section 5) be performed on any new PCB design prior to fabrication. These analyses should be used to assess the appropriate number of vias and geometrical trace width dimensions required to meet the IR drop requirements of system components.
- Whenever possible for the internal layers (both signal routing and power plane), wide traces and copper area fills are recommended for PDN layout. As discussed in previous sections of this document, routing power nets in planes provides for more inter-plane capacitance and improves high frequency performance of the PDN.
- Decoupling capacitors should be mounted with minimum impact to inductance. A capacitor has characteristics not only of capacitance but also inductance and resistance. Figure 4 shows the parasitic model of a real capacitor. A real capacitor should be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).


**Figure 4. Characteristics of a “Real” Capacitor With ESL and ESR**

The magnitude of the impedance of this series model is given in Equation 1.

$$|Z| = \sqrt{ESR^2 + \left(wESL - \frac{1}{wC}\right)^2} \quad (1)$$

where

$w = 2\pi f$

Figure 5 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown per Equation 1.

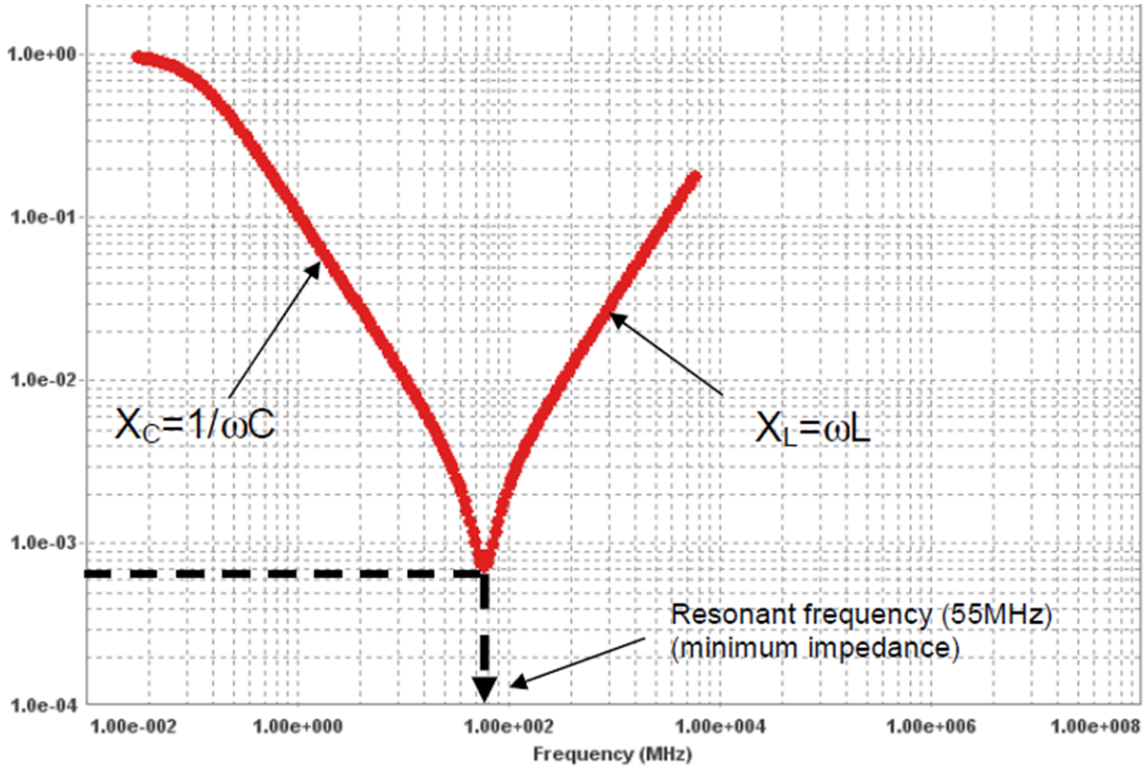


**Figure 5. Typical Impedance Profile of a Capacitor**

- Try to avoid different power nets coupling on the PCB by using “co-planar” shielding whenever appropriate. Figure 6 depicts an example of co-planar shielding for two different power nets (VDD_MPU_IVA and VDD_CORE).

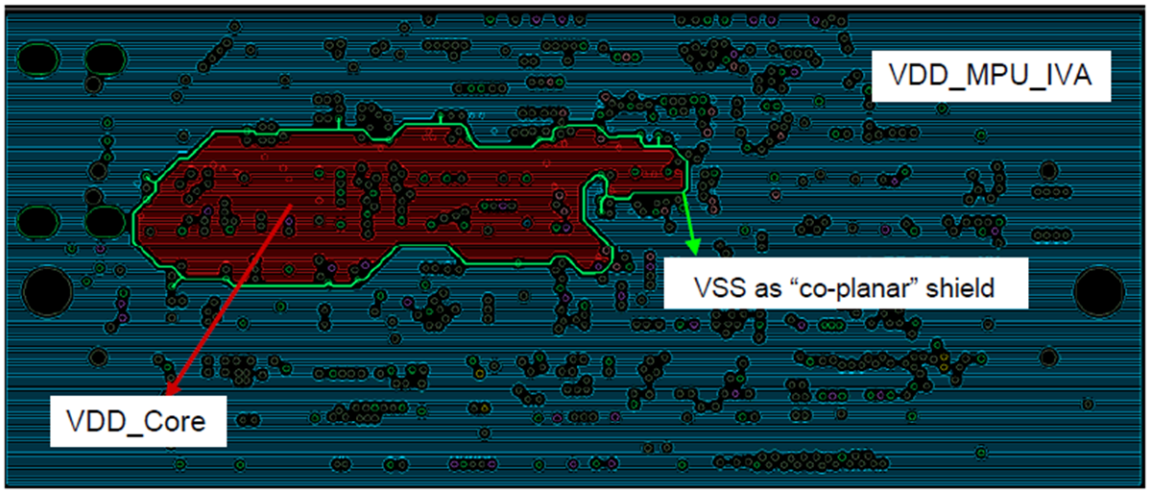


**Figure 6. Example of “Co-Planar’ Shielding of Power Net Using Ground Guard-Band**

As the capacitors have both series inductance and resistance that will impact their effectiveness, it is critical that the following recommendations are adopted in placing them on the power distribution network. Whenever possible make sure to mount the capacitor with the geometry that will minimize the mounting inductance and resistance. The capacitor mounting inductance and resistance includes the inductance and resistance of the pads, the trace, and the associated vias.

The length of a trace used to connect a capacitor has a significant impact on the parasitic inductance and resistance of the mounting. This trace should be as short and wide as possible. Wherever possible, minimize the trace by locating vias near the solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or by doubling the number of vias. If the PCB manufacturing process allows, and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

The most common via placement geometries are proved below, in order of preference for reducing parasitic impact:

1. Via-In-Pad (VIP)
2. Dual Offset Via
3. Single Offset Via
4. Pad to Via Trace (short)
5. Pad to Via Trace (long)

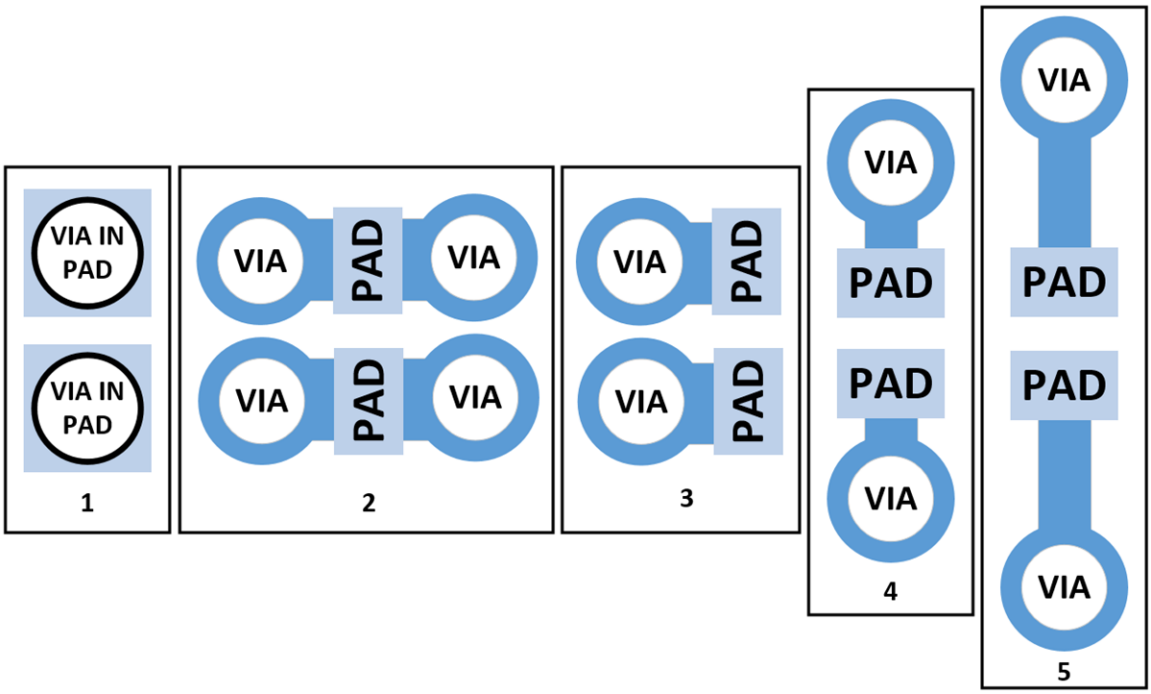


**Figure 7. Capacitor Mounting Geometries**

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (see Figure 1).

# 4 Static PDN Analysis (IR Drop Optimization)

Delivering reliable power to circuits is always of critical importance as IR drops can occur at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to IR drop, and designs that rely on battery power must further minimize voltage drop to avoid unacceptable power loss. Early DC assessments made through simulation help to determine power distribution basics such as the best available entry point for power, layer stack-up choices, and estimates for the amount of copper needed to carry the required current.

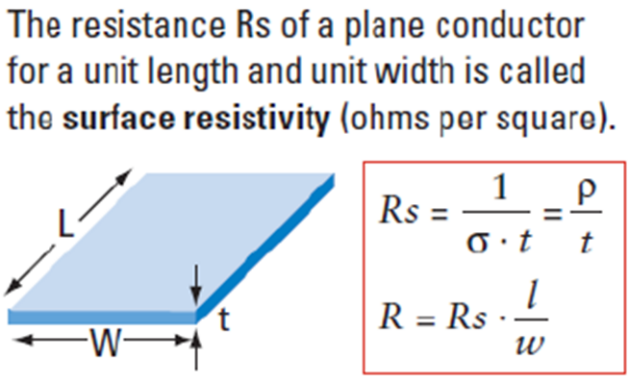


**Figure 8. Depiction of Sheet Resistivity and Resistance**

Ohm's Law (V=IR) relates conduction current to voltage drop, and at DC, the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor. Static IR or DC analysis/design methodology consists of designing the power distribution network such that the voltage drop (under DC operating conditions) across the power and ground pads of the application processor device is within a specified value of the nominal voltage to ensure proper functionality of the device. The PCB-level static IR drop budget is defined between the *pins/pads* of the power management device (PMIC/VRM/SMPS) and the *BGA balls* on the application processor device to which the power management device is supplying power (see Figure 9).

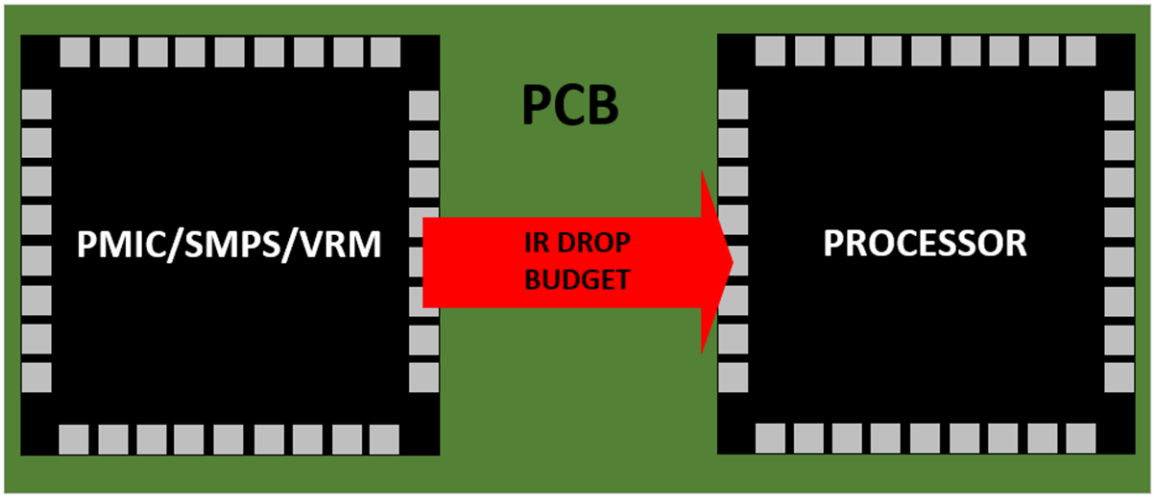


**Figure 9. PCB IR Drop Budget**

Given the total system-level margin allowed for proper device functionality, allowable voltage variation at the BGA of the device is typically specified at ±5% of the nominal voltage. [1] For devices implementing remote-sense functionality [2], it is a requirement that the power management device feedback/sense line(s) be placed as close to the relevant processor power balls as physically possible (see Figure 10) and that a supply input voltage difference of ≤5 mV under maximum current loading is maintained across all balls connected to a common power rail. This 5 mV maximum represents any voltage difference that may exist between a remote sense point and any associated power input (see Figure 11).

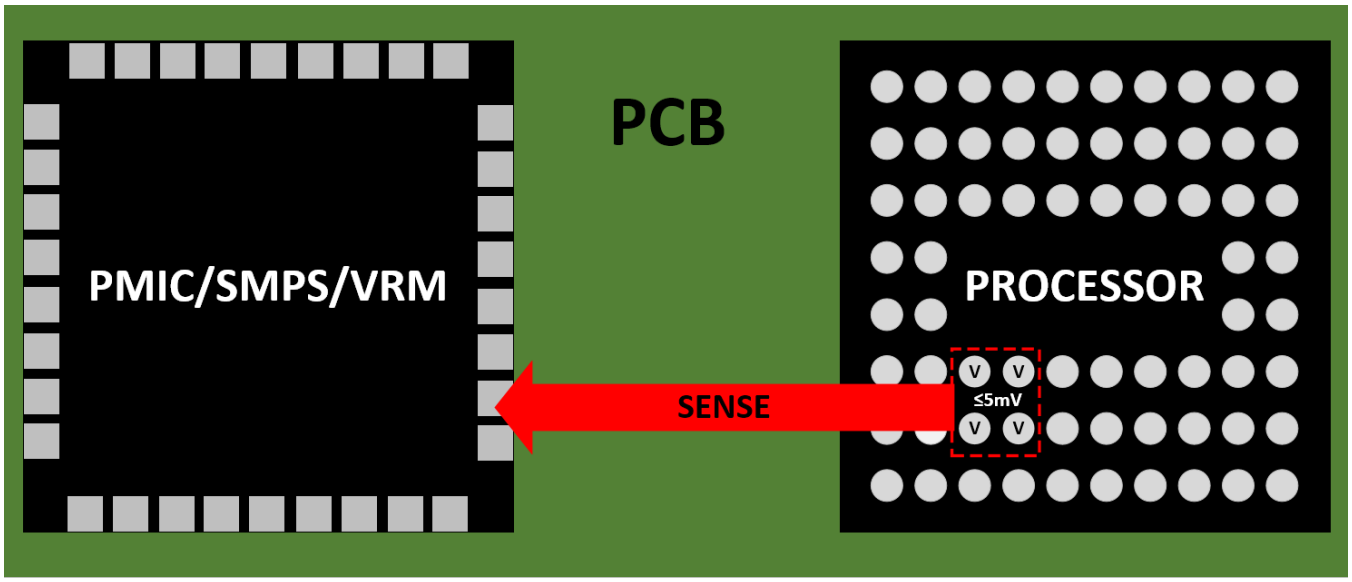


**Figure 10. Sense Line Placement**

[1] For processor power requirements, see the device-specific data manual.
[2] For remote-sense requirements, see the device-specific data manual.

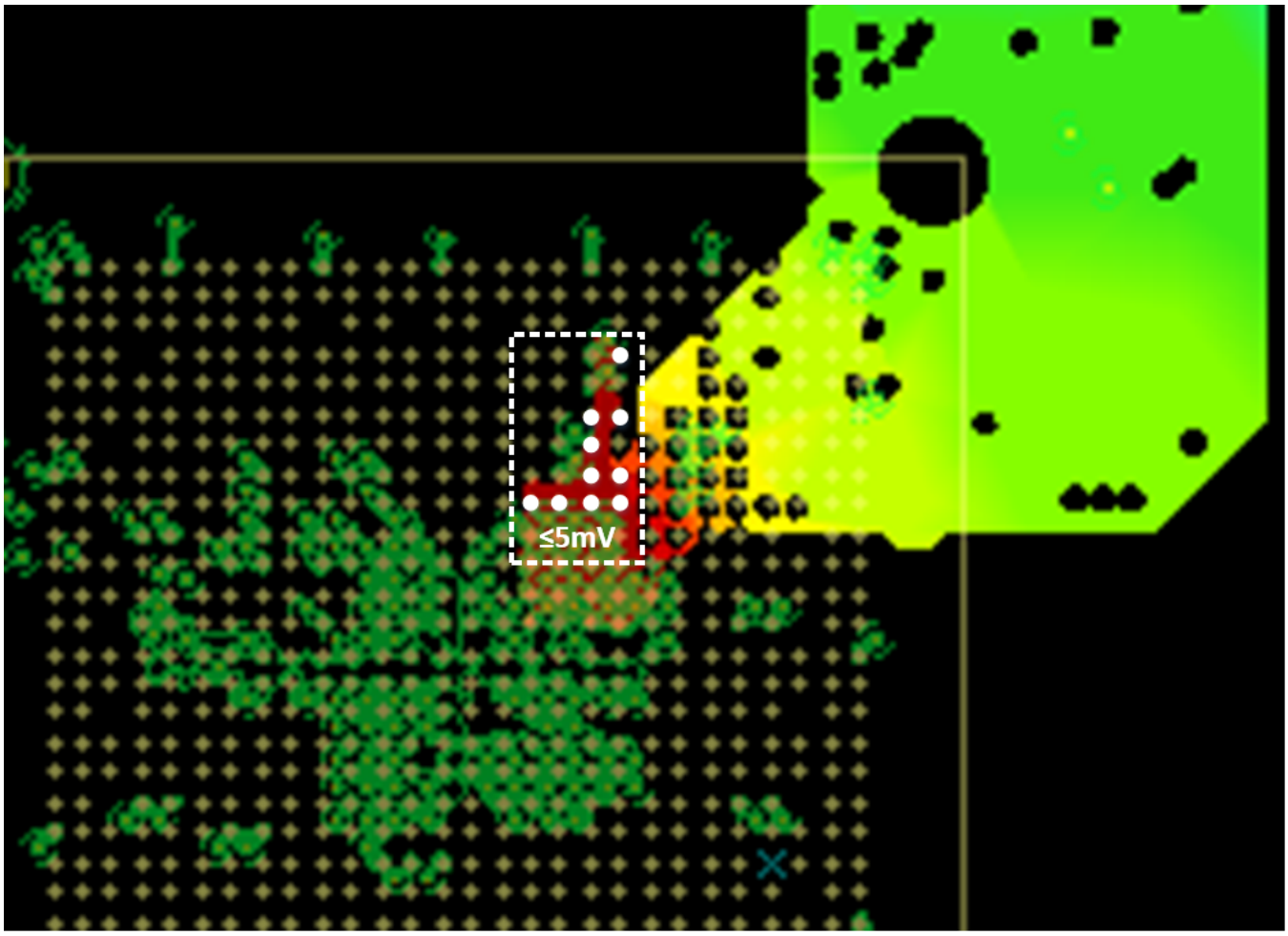


**Figure 11. Allowable Power Input Voltage Difference**

## 5 Dynamic Analysis of PCB PDN

The typical elements of the PDN are shown in Figure 12; which includes the chip-level power distribution with thin-oxide decoupling capacitors. The package-level power distribution with planes and mid-frequency decoupling capacitors; and the board-level (for example, PCB) power distribution with planes, low-frequency ceramic and bulk decoupling capacitors, and the voltage regulator module (VRM).

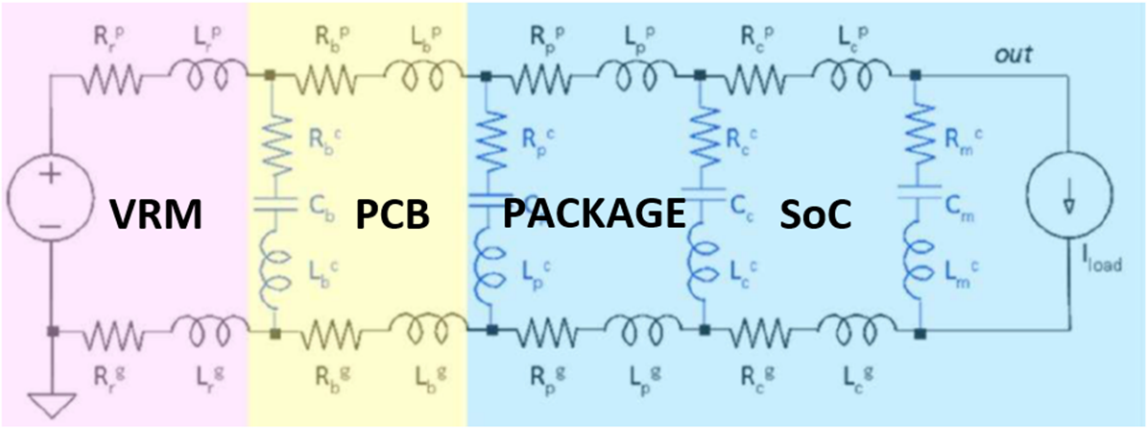


**Figure 12. Components of a Typical Power Distribution Network (PDN)**

The frequency ranges covered by these elements are shown in Figure 13. As the primary focus is on optimizing the PCB PDN for high performance, the methodology is developed around the areas over which the PCB designer has control over and can influence early in the design phase.

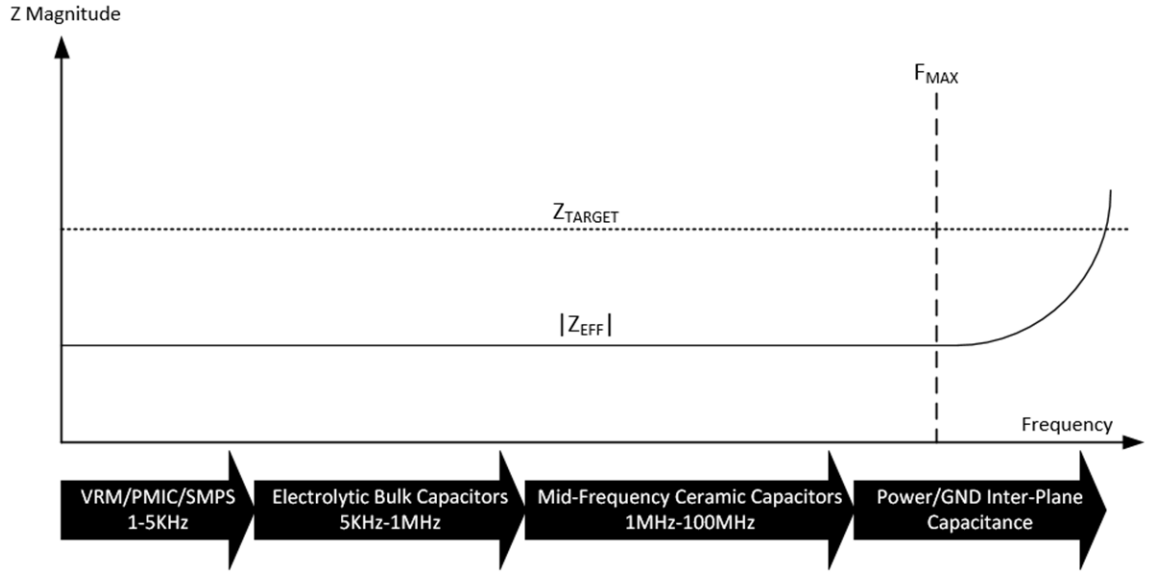


**Figure 13. Decoupling Frequency Range of PCB Components**

The VRM/PMIC/SMPS (or simply voltage regulator device) is the first major component of the PDN. It observes its output voltage and adjusts the amount of current being supplied to keep the voltage constant. Most common voltage regulators make this adjustment on the order of milliseconds to microseconds. They are effective at maintaining output voltage for events at all frequencies from DC to a few kilohertz (depending on the regulator dynamic response time). For all transient events that occur at frequencies above this range, there is a time delay before the voltage regulator can respond to the new level of demand. During this time delay the rail suffers from voltage droop. A power delivery network has an impedance ($Z_{PDN}$) associated with the path from the voltage regulator module to the processor. The magnitude of noise (voltage ripple) seen on a given power rail is proportional to the impedance ($Z_{PDN}$) and the transient current ($I_{TRANSIENT}$) draw associated with that rail.

Based on Ohm's Law,

$$V_{RIPPLE} = I_{TRANSIENT} \times Z_{PDN} \quad (2)$$

Typically the transient current is application-specific and is determined by a particular switching scenario. As a board designer, you have the ability to minimize the voltage ripple by reducing $Z_{PDN}$ either by reducing the inductance, or by maximizing the capacitance. To ensure that the voltage ripple noise is within the processor's specification, the $Z_{PDN}$ must be designed to meet a certain impedance, referred to as the target impedance ($Z_{TARGET}$). Using frequency domain target impedance method (FDTIM) to describe the behavior of a power delivery system has been widely accepted.

The key concept of the FDTIM is the determination of the target impedance $Z_{TARGET}$ (see Equation 3) for the power rail under consideration. For reliable operation of a power delivery system, its impedance spectrum needs to be maintained below the target value at the frequencies from DC to FMAX (see Figure 13). FMAX is the point in frequency after which adding a reasonable number of decoupling capacitors does not bring the power rail impedance |ZEFF| below the target impedance ($Z_{TARGET}$) due to the dominance of the parasitic planar spreading inductance and package inductances.

$$Z_{TARGET} = \frac{\text{Voltage Rail} \times \%\text{Ripple}}{0.5 \times \text{IMax}} \quad (3)$$

## 5.1 Selecting Decoupling Capacitors to Meet $Z_{TARGET}$

To maintain power integrity throughout the entire frequency range of interest, the power distribution network relies on the voltage regulator module (VRM/SMPS), the on-board discrete bulk electrolytic and ceramic decoupling capacitors, and the inter-plane capacitances (capacitance from the power-ground sandwich in the board stack-up). For a first-order analysis, the VRM of the power management integrated circuit (PMIC) can be modeled as a series-connected resistor and inductor. A PMIC, at low frequencies (up to 500 KHz-1 MHz), typically has low impedance and is capable of responding to the instantaneous requirements of the processor. The ESR and ESL values for the VRM are therefore very low. Beyond lower frequencies, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement of the device. The bulk and ceramic discrete decoupling capacitors must provide the required low impedance from the point at which the VRM becomes inductive. The effectiveness of the bulk and mid-frequency decoupling capacitors (1 MHz-70 MHz, depending on the capacitor's ESL and ESR) is limited by its placement (due to loop inductance), value, and type. Refer to Figure 14 for a capacitor placement example. Note that in order to minimize the loop inductance, the mid-frequency capacitors have been placed directly underneath the processor (on the bottom side of the PCB).

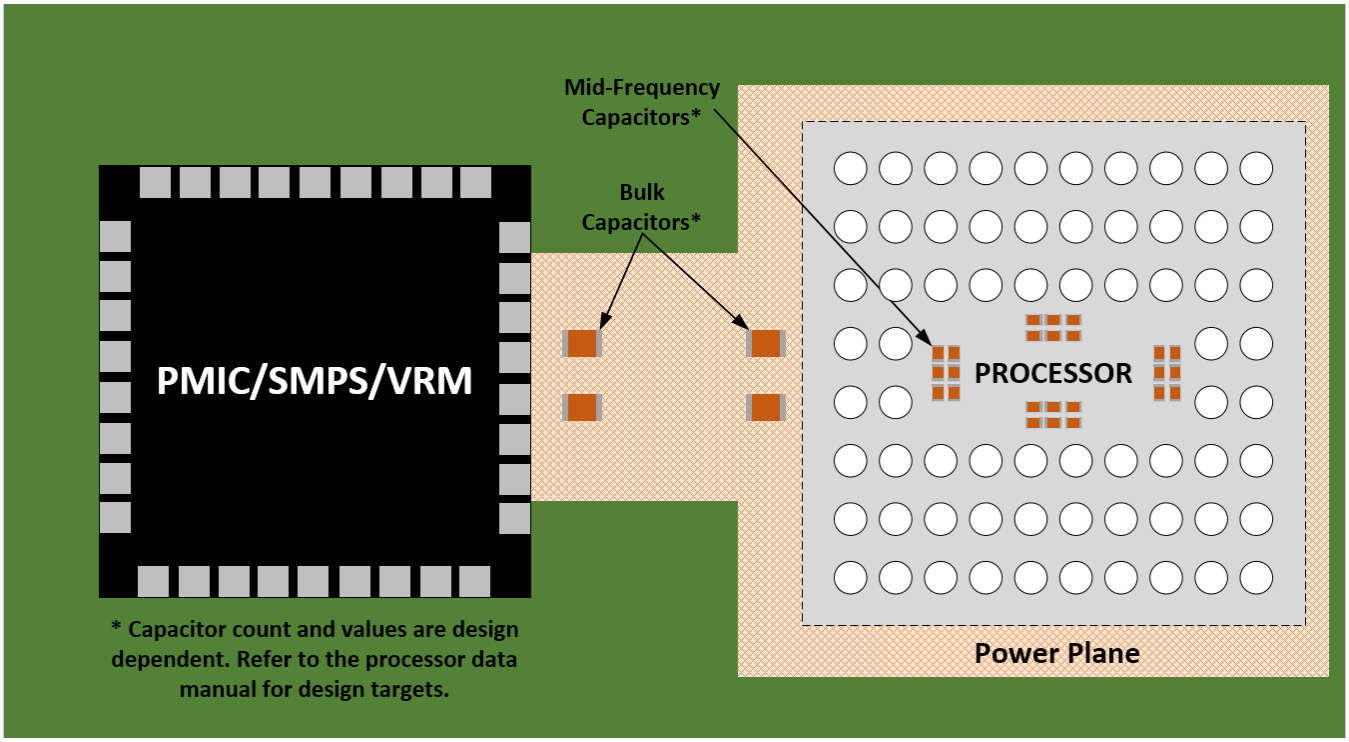


**Figure 14. Example Capacitor Placement**

The bulk capacitors should be located near the point of entry of the supply entrance to the board. The decoupling capacitors maintain the PDN impedance at the required value beyond the VRM frequency and until the frequency at which mid-frequency capacitors become useful. The mid-frequency SMT capacitors are useful in the 10 to 150 MHz range and higher. These capacitors are primarily ceramic capacitors that come in several dielectric types (NPO, X7R, X5R, and Y5V) and several sizes (1206, 0805, 0603, 0402, and so forth). The mid-frequency capacitors are much smaller than the bulk capacitors and can be placed closer to the transistor circuit. Since the ceramic capacitors are smaller, they have lower ESR and ESL and lower capacitance than bulk capacitors, leading to a higher resonance frequency with smaller impedance at resonance. Therefore, ceramic capacitors can be used at higher frequencies. Typical mid-frequency capacitors have capacitance in the range of 1 nF –100 nF, ESR in the range of 10-100 mΩ, and ESL in the range of 0.5 nH – 1 nH.

The concept of “loop inductance” is a useful metric for quantifying the effectiveness of the decoupling capacitors of a power distribution network. To calculate the loop inductance associated with decoupling capacitor placement, Equation 4 can be used:

$$L_{eff} = \frac{\text{Imaginary}\left(Z\left(\text{Power}, \text{GND pads of decap}\right)\right)}{2 \times \pi \times \text{Frequency}} \quad (4)$$

Where $L_{eff}$ is the effective loop inductance, Z ( power, GND pads of decap) represents the Z-parameters of the port defined across the power and ground pads of the corresponding decap. The frequency should be chosen in the “flat” region of the Z-parameter response, typically in the 50 MHz – 70 MHz range.

## 6 Checklist for PDN

Although this list is not inclusive of every parameter and variable that must be considered when designing a PCB, a PDN-optimized PCB design will implement these guidelines:

- ❑ Power and ground plane pairs (or “islands”) should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply at high frequencies.
- ❑ Whenever possible, the power and ground planes should be solid as this provides a continuous return path for return current.
- ❑ Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair so minimizing the separation distance (such as, the dielectric thickness) will maximize the resulting capacitance.
- ❑ The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductances of power current path. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, placing high priority supplies in the upper-half of the stack-up and low priority supplies in the lower half of the stack-up. This helps to minimize the loop inductance caused by decoupling capacitors and their associated vias.
- ❑ External power trace routing between components should be as wide as possible as wider traces result in reduced DC resistance and consequently a lower static IR drop.
- ❑ Whenever possible, attempt to achieve a ratio of 1:1 (or better) for component pins and associated vias. Do not share vias among multiple capacitors.
- ❑ Placement of decoupling capacitors and their associated vias should be as close to the processor ball as possible. Reserve the space directly underneath the processor for this purpose.
- ❑ Use of short and wide surface traces to connect capacitor pads to the vias connected to the planes below is preferred.
- ❑ Use of large diameter vias is preferred for reduced inductance/resistance.
- ❑ 1 oz – 2 oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, which helps to reduce processor junction temperatures. In addition, it is preferable to have the power / ground planes be located adjacent to the PCB surface on which the processor is mounted.
- ❑ Place the VRM as close as possible to the processor and on the same side of the PCB. In cases where a power management IC (PMIC) is implemented as the VRM, it should be aligned to minimize distance for the highest current rail.

# 7 66AK2G1x Example Stack-Up

| Lay # | Thick (in) | Picture | Type Dk Df | Description | Drill Picture |
|---|---|---|---|---|---|
| 0.0006/0.0013 | | | 4.5 | Soldermask | |
| 1 | 0.0020 | | F / S | 0.5oz w/plating | 1 |
| | 0.0035 | 2113 | 4.12 0.0152 | fill | |
| 2 | 0.0013 | | P | 1oz | 2 |
| | 0.0080 | 7628 | 4.25 0.0150 | core | |
| 3 | 0.0013 | | S | 1oz | 3 |
| | 0.0052 | 1080*2 | 3.92 0.0155 | fill | |
| 4 | 0.0013 | | P | 1oz | 4 |
| | 0.0040 | 2116 | 4.28 0.0149 | core | |
| 5 | 0.0013 | | M | 1oz | 5 |
| | 0.0211 | 7628*3 | 4.41 0.0147 | fill | |
| 6 | 0.0013 | | M | 1oz | 6 |
| | 0.0040 | 2116 | 4.28 0.0149 | core | |
| 7 | 0.0013 | | P | 1oz | 7 |
| | 0.0052 | 1080*2 | 3.93 0.0155 | fill | |
| 8 | 0.0013 | | S | 1oz | 8 |
| | 0.0080 | 7628 | 4.25 0.0150 | core | |
| 9 | 0.0013 | | P | 1oz | 9 |
| | 0.0035 | 2113 | 4.12 0.0152 | fill | |
| 10 | 0.0020 | | F / S | 0.5oz w/plating | 10 |
| 0.0006/0.0013 | | | 4.5 | Soldermask | |

| | |
|---|---|
| 0.0776 | Total thickness (in) Over mask on plated copper |
| 0.0737 | After lamination thickness (in) |
| 0.0751 | Over laminate thickness (in) (with soldermask) |
| 0.0790 | Customer Requirement (in) |
| +/-0.0079 | Customer Tolerance (in) |

**Impedance Constraint Information**

| Imp # | Impedance Type | | Affect Lyr (1) | Affect Lyr (2) | Cust L/W | Line Width (1) | Line Width (2) | CenterToCenter (1) | CenterToCenter (2) | Ref Plane Top | Ref Plane Bot | Targ ohms | Tol ohms | Predicted ohms@2GHz |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | EC MS | | 1 | None | 0.005 | 0.0052 | 0.0052 | 0.01085 | | None | 2 | 85 | 8.5 | 84.42 |
| 2 | EC MS | | 1 | None | 0.0041 | 0.0042 | 0.0042 | 0.0093 | | None | 2 | 90 | 9 | 89.67 |
| 3 | EC MS | | 1 | None | 0.004 | 0.0041 | 0.0041 | 0.013 | | None | 2 | 100 | 10 | 99.61 |
| 4 | Surf MS | | 1 | None | 0.005 | 0.005 | | | | None | 2 | 50 | 5 | 50.08 |
| 5 | Surf MS | | 1 | None | 0.004 | 0.004 | | | | None | 2 | 55 | 5.5 | 54.84 |
| 6 | EC SL | | 3 | None | 0.005 | 0.005 | 0.005 | 0.01085 | | 4 | 2 | 90 | 9 | 88.85 |
| 7 | EC SL | | 3 | None | 0.004 | 0.004 | 0.004 | 0.0105 | | 4 | 2 | 100 | 10 | 98.86 |
| 8 | Stripline | | 3 | None | 0.005 | 0.005 | | | | 4 | 2 | 50 | 5 | 50.58 |
| 9 | Stripline | | 3 | None | 0.004 | 0.004 | | | | 4 | 2 | 55 | 5.5 | 55.67 |
| 10 | EC SL | | 8 | None | 0.005 | 0.005 | 0.005 | 0.01085 | | 7 | 9 | 90 | 9 | 88.81 |
| 11 | EC SL | | 8 | None | 0.004 | 0.004 | 0.004 | 0.0105 | | 7 | 9 | 100 | 10 | 98.81 |
| 12 | Stripline | | 8 | None | 0.005 | 0.005 | | | | 7 | 9 | 50 | 5 | 50.54 |
| 13 | Stripline | | 8 | None | 0.004 | 0.004 | | | | 7 | 9 | 55 | 5.5 | 55.63 |
| 14 | EC MS | | 10 | None | 0.005 | 0.0052 | 0.0052 | 0.01085 | | None | 9 | 85 | 8.5 | 84.47 |
| 15 | EC MS | | 10 | None | 0.0041 | 0.0042 | 0.0042 | 0.0093 | | None | 9 | 90 | 9 | 89.71 |
| 16 | EC MS | | 10 | None | 0.004 | 0.0041 | 0.0041 | 0.013 | | None | 9 | 100 | 10 | 99.67 |
| 17 | Surf MS | | 10 | None | 0.005 | 0.005 | | | | None | 9 | 50 | 5 | 50.12 |
| 18 | Surf MS | | 10 | None | 0.004 | 0.004 | | | | None | 9 | 55 | 5.5 | 54.88 |

Trace widths measured at base of trace
All dimensions in inches (unless otherwise noted)
All values are calculated using a frequency of 2.00GHz

Products built using these specified nominal dimensions will have variation in physical and electrical results based on acceptable manufacturing materials and process tolerance.
This data is intended to provide one possible solution to meet a particular set of impedance and thickness requirements.
If any of these values are attached to fabrication prints, they should be marked as 'reference'.

**Table 2. 66AK2G1x PDN Requirements and Decoupling Example**

| Supply Name [1] | Frequency of Interest (MHz) | Number of Decoupling Capacitors Per Supply [2] [3] [4] | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 0.01 µF | 0.1 µF | 0.33 µF | 1 µF | 3.3 µF | 4.7 µF | 100 µF |
| CVDD | ≤40 | | 36 | 1 | 2 | 1 | 1 | 1 |
| CVDD1 | ≤40 | 1 | 5 | | | | | 1 |

(1) Ganged rails must meet all requirements of each member rail.

(2) The decoupling capacitor counts and values presented here are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PC designs be simulated prior to fabrication to ensure that all processor PDN requirements are met.

(3) For more information on peak-to-peak noise values, see the Recommended Operating Conditions table in the device-specific data manual.

(4) ESL must be as low as possible and not exceed 0.5 nH.

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

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