66AK2Gx Hardware

User's Guide

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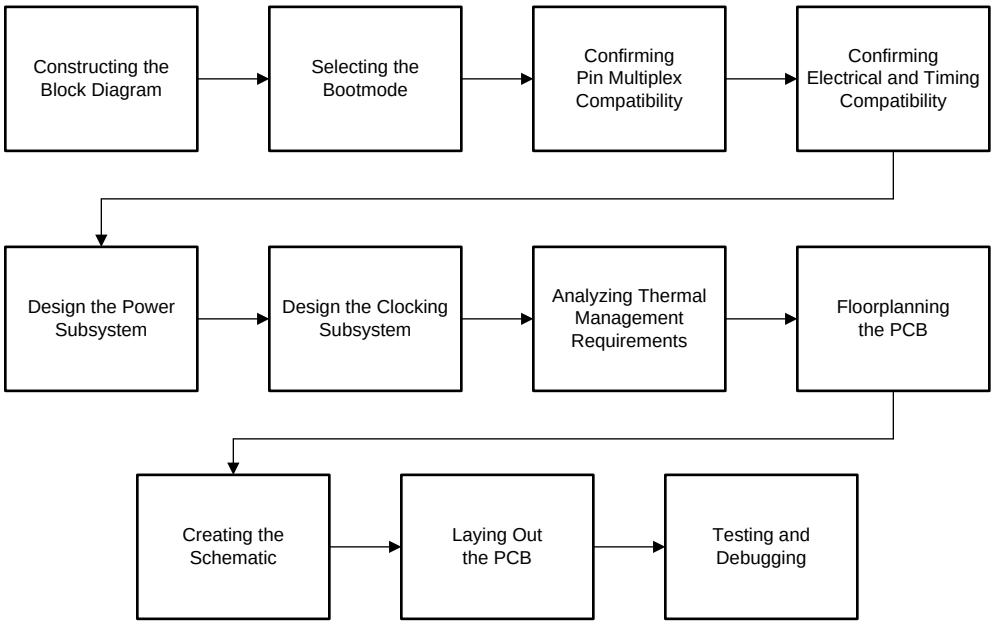
Introduction

Welcome to the hardware design guide. The purpose of this guide is to walk hardware designers through the various stages of designing a board on this platform. The guide follows the structure shown in Figure 1. Each of the design stages in the time line link to a collection of useful documentation, application notes, and design recommendations. Using this guide, hardware designers can efficiently locate the resources they need at every step in the board design flow.

Figure 1. Hardware Design Time Line



1 Constructing the Block Diagram

The first step in designing the hardware platform is to create a detailed block diagram. The block diagram must contain all major system ICs and illustrate which I/O ports are used for device interconnection. Review the 66AK2Gx SoC block diagram in the data manual and identify which external interfaces are needed. Match each of the system ICs with the interface to the SoC and include this connection in the block diagram. The following is a collection of resources to aid in the block diagram creation process.

- The 66AK2Gx General Purpose EVM is always a good source to start building a reference design for these devices. The 66AK2Gx EVM webpage includes all the technical documentation for the design.
- The links at the 66AK2G12 Product Folder provide block diagrams, application notes, tools, software, design considerations, and other related information for various products under the Related End Equipments category.
- Select from a list of complementary devices to attach to the 66AK2Gx device in your system. 66AK2Gx power management device: TPS65911

2 Selecting the Boot Mode

The block diagram must also indicate which interface is used for booting this device.

- These devices contain an on-chip ROM bootloader.
  - The boot config pins are sampled at power-on-reset.
  - Sets up system for boot depending on boot configuration selected
  - Depending on boot mode, the boot image is copied to internal RAM and then executed.
  - The maximum size of the boot image is 896 kB if internal memory is used for the boot image.
- The following boot modes are supported:
  - QSPI boot
  - SPI boot
  - GPMC boot using NAND or NOR flash
  - UART boot
  - I^2C master or slave boot using an EEPROM or an external host
  - Ethernet boot
  - PCIE boot
  - MMCSD boot using an embedded MMC (eMMC) or SD card
  - USB 2.0 device mode boot
- If the first boot source fails to boot, the ROM moves on to the next one in the sequence. Some boot sources take an extended period of time to time-out if that boot source is not available.
- Read the 66AK2Gx Technical Reference Manual initialization chapter to understand details on different boot modes.
- Key boot considerations:
  - TI recommends including population options for other boot modes to aid in development. At a minimum, an I^2C memory device allows the implementation of a two stage boot.
  - Boot pins have other functions after reset, ensure your board design takes this into account when choosing pullup and pulldown resistors for the boot pins.
  - All pins used for boot configuration must have external pulling resistors. Do not rely on internal pulling resistors for any of these pins.

3 Confirming Pin Multiplexing Compatibility

The 66AK2Gx device contains many peripheral interfaces. To reduce package costs while maintaining maximum functionality, many of the 66AK2Gx terminals can multiplex up to five signal functions. Some background about the 66AK2Gx pin multiplexing follows:

- Although many combinations of pin multiplexing are possible, only a certain number of sets, called I/O sets, are valid due to timing limitations. These valid I/O sets were carefully chosen to provide many possible application scenarios for the user.
- To guarantee the I/O timings published in the 66AK2Gx Data Manual over the lifetime of the device, the 66AK2Gx software must implement the proper pin configuration requirements. These requirements impact software configuration of the following registers and are fully documented in the Pad Configuration section of the 66AK2Gx TRM.
  - Pad configuration registers
    - muxmode
    - slew control
    - buffer class
    - and so on

  TI developed a Windows® and Linux® compatible application called TI PinMux Tool that helps system designers select the appropriate pin-multiplexing configuration for their 66AK2Gx-based product design. This tool lets users select valid I/O sets of specific peripheral interfaces, to ensure the pin-multiplexing configuration selected for a design only uses valid I/O sets supported by the 66AK2Gx.

4 Confirming Electrical and Timing Compatibility

A key step in the hardware design before beginning schematic capture is to confirm both DC and AC electrical compatibility between this device and the other ICs connected to it.

- The device data sheet has important information regarding timing and electrical characteristics.
- For high speed interfaces, users can run IBIS simulations using IBIS models provided for the 66AK2Gx ABY NFBGA-N625 package (ABY Package IBIS) to confirm signal integrity.
- Using IBIS Models for Timing Analysis

NOTE: TI provides PCB layout specifications for the following interfaces, eliminating the need to perform electrical analysis:

- DDR3L - see data sheet and the DDR3 Design Requirements for KeyStone Devices
- USB, HDMI, SATA, and PCIe - see the High-Speed Interface Layout Guidelines Application Report (SPRAAR7E)

5 Designing the Power Subsystem

Once the block diagram has been validated for pin multiplexing, as well as electrical and timing compatibility, the power subsystem can be designed.

TI provides a power management IC (PMIC) solution for 66AK2Gx designs: TPS659118

The PMIC is not required for 66AK2Gx designs. A discrete power supply design can be implemented but it must meet all of the voltage and current requirements specified by the 66AK2Gx data manual.

NOTE: The TPS659118 and TPS65911A PMICs require an external 32.768-KHz crystal. See the following resources on estimating power consumption and designing a 66AK2Gx power solution.

- 66AK2Gx Power Consumption Summary: the 66AK2Gx power numbers discuss the power consumption for common system application use scenarios for the 66AK2Gx KeyStone Processors. Power consumption is highly dependent on the individual user's application; however, this document focuses on providing several 66AK2Gx application-use case scenarios and the environment settings that were used to perform such power measurements.
- 66AK2Gx Power Estimation Tool: the power estimation tool (PET) provides users with the ability to gain insight into the power consumption of select KeyStone processors. The tool allows the user to choose multiple application scenarios and understand the power consumption for their specific application. The data manual does not provide upper limits for the current needed by each rail. The PET provides the limits needed for designing the power supply.
  - TPS65911 (66AK2Gx Power Solution) Data Sheet
  - TPS659118 User's Guide for 66AK2G0x Processor
  - TPS65911A User's Guide for 66AK2G1x Processor

6 Designing the Clocking Subsystem

In addition to the power subsystem, the clocking subsystem must be designed to provide appropriate clocks to all ICs in the system. These clocks can be created by pairing crystals with internal oscillators within the system ICs or they can be created by a separate clock generator. The 66AK2Gx was designed to simplify the clocking solution needed. All the clocks, with the exception of the PCIE reference clock, can be generated internally from a single external crystal. Conversely, separate clock input pins are available for customers that want an external clocking solution. See the following information on designing the clocking subsystem for your design.

- Key considerations:
  - The device operation requires the following clocks:
    - A system clock provided by either a crystal or an external clock source is required for proper operation.

    - A DDR reference clock which can be generated internally or from an external clock source.
- Optional clocks needed by the device include the following:
  - An audio clock can be generated internally or provided by either a crystal or an external clock source.
  - The USB reference clock can be generated internally or provided by an external clock source.
  - If the PCIE interface is used, an external 100 MHz reference clock must be provided.
- For more details, see the Clocking sections of the device data sheet and TRM.

7 Analyzing Thermal Management Requirements

The product design cycle must include thermal analysis and thermal management techniques to ensure the operating junction temperature of the device is within functional limits. The values calculated by the 66AK2Gx PET and an understanding of the operation environment are required to determine a proper thermal solution.

- Thermal Design Guide for KeyStone Devices
- 66AKG02 Thermal Model

8 Floor Planning the PCB

Before beginning schematic capture, TI recommends floor planning the system PCB to determine the interconnect distances between the various system ICs. It is always best to determine the placement of any high-speed interfaces. Devices using these interfaces must be positioned as close as possible to the pins on the K2G SoC. Floor planning highlights any conflicts between the ideal placement of components and the necessary position for the system.

9 Creating the Schematics

At this point in the design, it is time to start capturing the schematics. See the following collection of information to aid in creating the schematics.

- Key considerations:
  - Output clocks which are internally looped back
  - Remember to install a JTAG connection
  - JTAG: ensure to use the RTCK pin
- It is often helpful to refer to example schematics throughout the schematic capture process. The source for the 66AK2Gx General Purpose EVM can be used as a starting point for many schematic designs.
- Ensure to use one of the recommended topologies in the data sheet for the DDR3L interface.
- For detailed information on USB, HDMI, SATA, and PCIe board design, see the High-Speed Interface Layout Guidelines Application Report (SPRAAR7E)
- During and after schematic capture, check the design against the 66AK2Gx schematic checklist
- Plan to have an internal schematic review to go through the schematic checklist and inspect other key areas of the schematic to look for inaccuracies, missing net connections, and so on.

Symbols, footprints, and simulation models to aid in the design of the device placement and interconnects follow:

- Symbols and footprints generated by the Ultra Librarian Software
- Pin names and numbers available in the 66AK2Gx Data Manual
- BSDL Simulation Model
- IBIS Simulation Model
- General hardware design information: K2G BGA Escape Routing Design
- For selecting and placing decoupling capacitors in a BGA design: Decoupling (Bypass) Capacitor Selection and Placement for BGAs

10 Laying Out the PCB

After completing schematic capture, see the following information on laying out the PCB.

- It is often helpful to refer to an example layout when designing a custom PCB: K2G General Purpose EVM
- Ensure to follow the layout specifications for the following critical interfaces:
  - DDR3L – see data sheet
  - USB, PCIe – see the High-Speed Interface Layout Guidelines Application Report
- Plan to have an internal PCB layout review with your design team to verify that the net connection traces and power distribution network were created correctly.
- General information articles:
  - Understanding TI's PCB Routing Rule-Based DDR Timing Specification
  - 66AK2Gx BGA Escape Routing
  - 66AK2Gx General-Purpose EVM Power Distribution Network Analysis

11 Board Bring Up and Diagnostic

Once the custom PCB has been produced and assembled, refer to the following information on bringing up and debugging the system.

- Overview of Debug and Trace Tools
- Code Composer Studio™
- Using BSDL to validate the 66AK2Gx based board. Users can use 66AK2Gx BSDL files to validate the connectivity on board build.
- Processor SDK RTOS Diagnostics

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision	Page
• Updated Note.	5
• Added link to TPS65911A User's Guide for 66AK2G1x Processor.	5

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