

# ***From Sample Instant to Data Output: Understanding Latency in the GSPS ADC***

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## **ABSTRACT**

For many applications which use ultra high-speed ADCs, latency can be a critical performance specification. For example, if the ADC is used in any kind of feedback loop, then the absolute latency is an important factor. For a MIMO system such as a phased array radar, the relative difference and variability in latency becomes important. This application note covers latency in the GSPS ADC products, specifically for the ADC12D1800/1600/1000/800/500RF, the ADC12D1800/1600/1000, and the ADC10D1500/1000.

## **Contents**

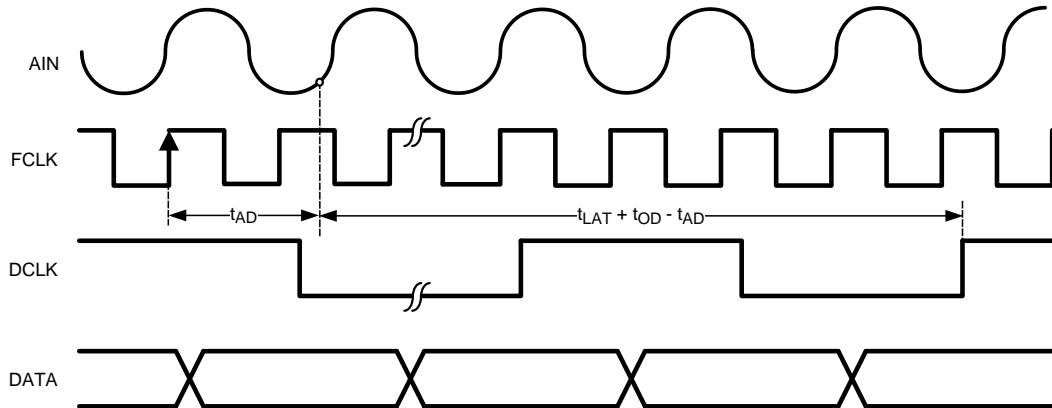
1	Introduction .....	2
2	$t_{AD}$ : Aperture Delay .....	2
3	$t_{LAT}$ : Conversion Latency .....	4
4	$t_{OD}$ : Sampling Clock to Data Output Delay .....	5
5	Calculating Total Latency .....	7
6	Calculating Sample Instant Variation and Variability .....	7
7	Acknowledgments .....	8

## **List of Figures**

1	GSPS ADC Latency Timing .....	2
2	Aperture Delay Concept.....	2
3	Constant Output Code for $F_{CLK} = F_{IN}$ .....	3
4	Measuring $t_{AD}$ for $n = 1$ .....	4
5	Measuring $t_{AD}$ for $n = 2$ .....	4
6	Measuring $t_{OD}$ by Varying FCLK.....	6
7	Measuring $t_{OD}$ by DCLK_RST Feature .....	7

## 1 Introduction

The total latency through the ADC,  $t_{LAT\_ADC}$ , is defined as the amount of time it takes for the digital equivalent of the sampled analog input value to arrive at the output, see [Figure 1](#). The analog input, AIN, is sampled by the sampling clock, FCLK, converted into a digital code and this DATA is clocked out on the data clock DCLK. The waveforms in this figure refer to the voltages at the pins of the chip.



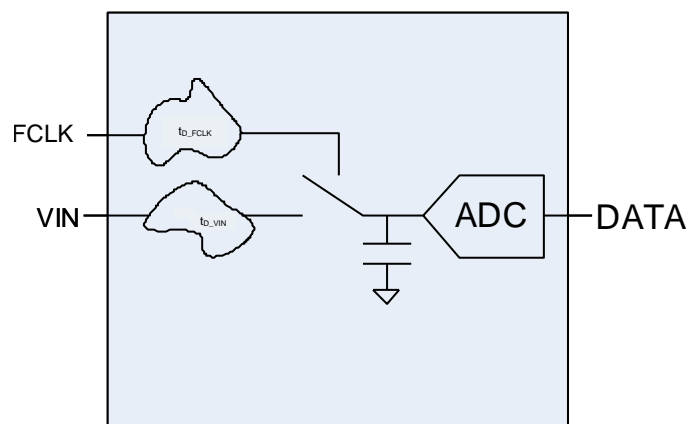
**Figure 1. GSPS ADC Latency Timing**

The Aperture Delay,  $t_{AD}$ , is the amount of delay, measured from the sampling edge of the clock input, after which the signal present at the input pin is sampled inside the device. The conversion latency,  $t_{LAT}$ , is the integer or half integer number of sampling clock cycles required for the analog sample to be converted into its digital equivalent. The sampling clock-to-data output delay,  $t_{OD}$ , is a fixed time delay in addition to the conversion latency. So the total latency for the ADC, also shown in [Figure 1](#), is:

$$t_{LAT\_ADC} = t_{LAT} + t_{OD} - t_{AD}$$

## 2 $t_{AD}$ : Aperture Delay

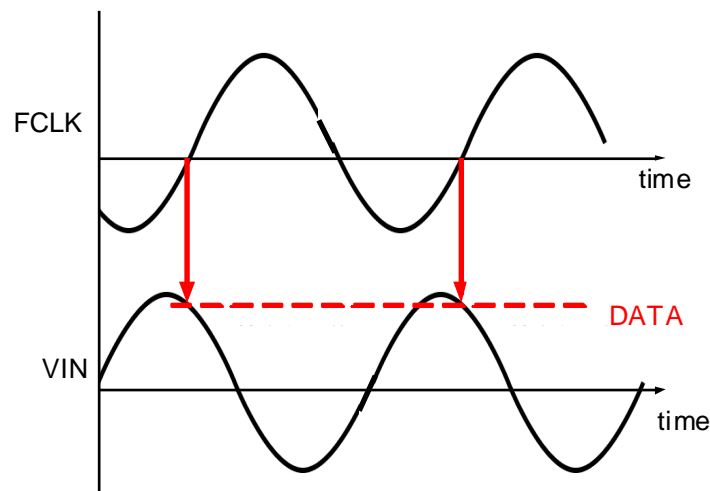
The actual analog input sampling event takes place inside the device at the track-and-hold. Due to routing and parasitic delays, the analog input signal, VIN, experiences some time delay,  $t_{D\_VIN}$ , from the input pin before reaching the track-and-hold. Similarly, the sampling clock, FCLK, experiences some delay,  $t_{D\_FCLK}$ , before reaching the track-and-hold. See [Figure 2](#). The aperture delay,  $t_{AD}$ , is effectively the difference between these two delays.



**Figure 2. Aperture Delay Concept**

Because of how it is defined,  $t_{AD}$  is reported in the datasheet as a positive value; also, it does not generally make sense to report a negative value for a time delay, as this only defines which event took place first. However, when  $t_{AD}$  is accounted for in the total latency,  $t_{LAT\_ADC}$ , it is subtracted from the total because the delay of the analog input is actually shorter than the delay of the sampling clock. This is because, internally to the device, the analog input arrives to the track-and-hold relatively faster, after some routing delays related to the mode configuration (dual-channel or interleaved). The sampling clock takes longer to arrive at the track-and-hold because it is conditioned and distributed via the clocking tree.

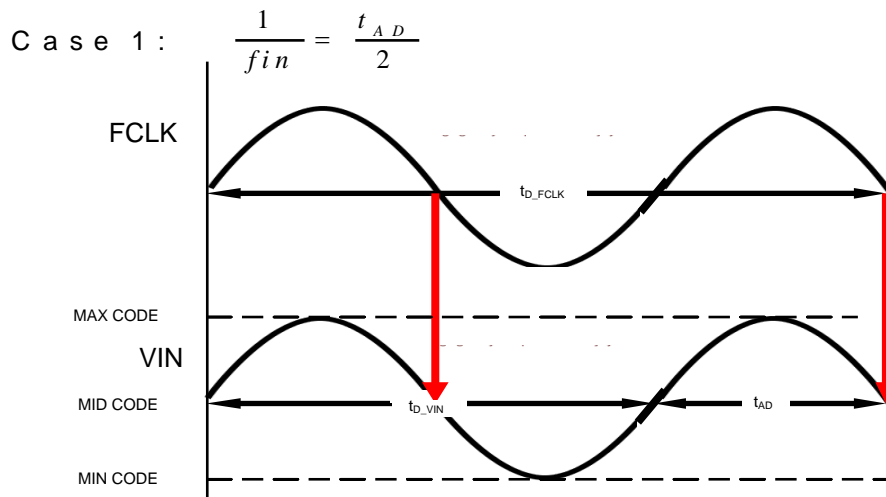
Measuring  $t_{AD}$  presents an interesting challenge since the endpoints of the delay path are located at a pin on the device and at a point internal to the device. Instead of measuring it directly from point-to-point, we can make use of some techniques related to the unique properties of a data converter. If the frequency of the sampling clock,  $F_{CLK}$ , is the same as the analog input,  $F_{IN}$ , then the resultant output code will be a constant value, see [Figure 3](#). This example shows  $F_{CLK}$  sampling on the rising edge of the clock.



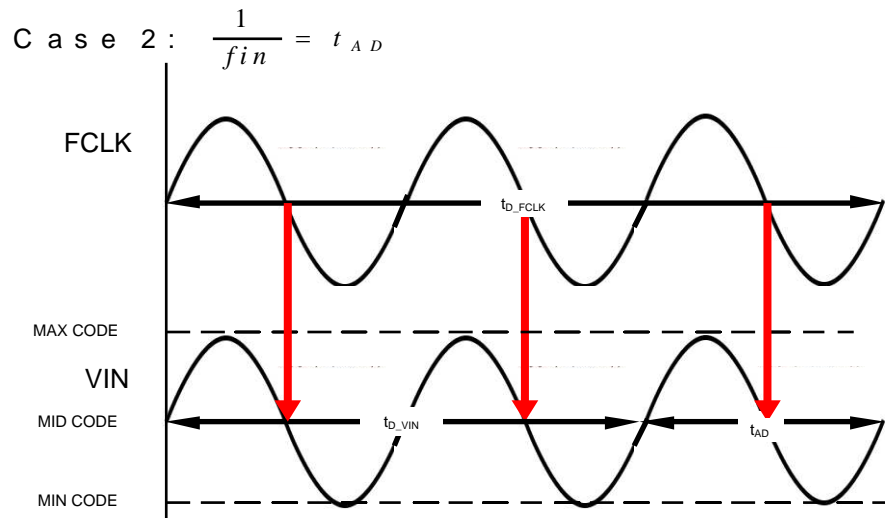
**Figure 3. Constant Output Code for  $F_{CLK} = F_{IN}$**

The examples in [Figure 4](#) and [Figure 5](#) show  $F_{CLK}$  sampling on the falling edge of the clock. For the purpose of measuring  $t_{AD}$ , the interesting frequency,  $f_{IN}$ , results in a mid-code value at the data converter output. For example, for a 12-bit converter, the mid-code output will be 2047 / 2048. This will occur for:  $f_{IN} = (n / 2) * f_{AD}$  where  $n$  is an integer, and  $f_{AD}$  is  $1 / t_{AD}$ .

See Case 1 where  $n = 1$  in [Figure 4](#). For this case, the aperture delay is equal to half a period of the input and sampling clock frequency. When testing in the lab, it is possible to apply the same frequency to analog input and sampling clock, and sweep through the frequencies while observing the digital output code to identify the mid-value cases. Note that there will be multiple frequencies for which a mid-code output occurs.


**Figure 4. Measuring  $t_{AD}$  for  $n = 1$** 

The case for  $n=2$  is shown in Figure 5 where  $f_{IN} = f_{AD}$ . So, it is possible to verify  $t_{AD}$  by observing it for  $n=1,2,3\dots$ . The lowest frequency for which it is possible to achieve a mid-value output code is for  $n=1$ ; using this fact, it is possible to know which case is being observed while sweeping frequencies.


**Figure 5. Measuring  $t_{AD}$  for  $n = 2$** 

### 3 $t_{LAT}$ : Conversion Latency

The conversion latency,  $t_{LAT}$ , is different from the total ADC latency,  $t_{LAT\_ADC}$ . The conversion latency only accounts for the number of sampling clock cycles to perform the actual conversion and encoding, but there are also analog delays at the input and output of the chip which contribute to the total latency and must be accounted for.  $t_{LAT}$  is measured in units of sampling clock cycles which differ by GSPS ADC product, output bank and mode (DES / Non-DES, Demux / Non-Demux); these values are guaranteed by design and are specified in the datasheet.

The fastest type of data converter architecture is a flash architecture, in which each analog input value may be converted in a few sampling clock cycles for conversion and encoding. Flash-based converters are generally susceptible to sparkle codes, which can occur when one bit in the digital output is reported incorrectly. Due to power and die size constraints, it is not practical to physically realize a 10- or 12-bit ADC using a flash architecture.

A pipeline ADC converts in sub-ranging stages from coarse to fine, and the resultant code is subtracted, so that the difference can be converted in the next stage. Pipeline ADCs are a good choice for high-speed, high-resolution ADCs, but for ultra-high speed ADCs, it is desirable to choose a flash-based architecture to achieve maximum speed.

The GSPS ADCs also use time-interleaving to achieve maximum speeds. In general, the conversion latency of the 10- and 12-bit GSPS ADCs is the same for all ADCs, with one notable exception, the ADC12D800/500RF. The ADC10D1500/1000, ADC12D1800/1600/1000, and ADC12D1800/1600/1000RF have a 2x interleave per channel. For example, this means that the Q-channel converter consists of two interleaved sub-converters, Q1 and Q2, each running at half the sample rate of the composite Q-channel. For the ADC12D800/500RF, the second sub-converter, Q2, is shut down. Because both sub-converters are running off the same sample clock, shutting one down results in a conversion latency which is roughly half the number of clock cycles, which is the case for the ADC12D800/500RF, see [Table 1](#). The Sample Clock Cycles per Conversion are for the DI bank in Non-DES Non-Demux Mode.

**Table 1. Sub-converters per channel by Product**

Product	Sub-converters per channel	Sample Clock Cycles per Conversion
ADC10D1500/1000	2	34
ADC12D1800/1600/1000	2	34
ADC12D1800/1600/1000RF	2	34
ADC12D800/500RF	1	17.5

To achieve ultra-high speeds and high resolution, the GSPS ADC products employ an innovative integration and implementation of classic ADC architectures. Considering the trade-offs of each technique, it is an interleaved, folded-interpolating architecture, which is a modified form of a flash, which addresses the power consumption and die size issues. A folding-interpolating architecture implies an increased conversion latency as compared to a flash architecture. The GSPS ADC architecture also incorporates pipelining, except that it operates 2x faster than the classic implementation. Part of the unique design of the TI GSPS ADC family is that it includes error correction as part of the conversion process, which results in the low code error rate (CER), at the price of increased latency. This unique architecture is what results in the fixed number of conversion cycles,  $t_{LAT}$ .

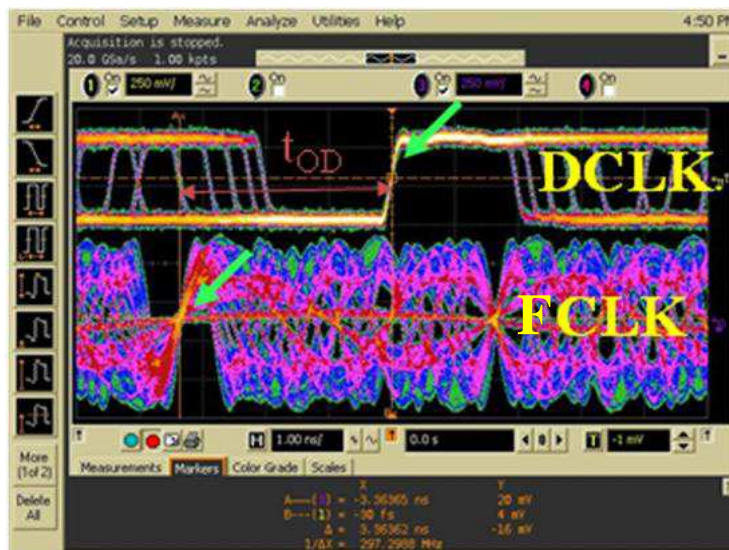
The conversion latency is approximately the same for the dual-channel (Non-DES) Mode and the interleaved (DES) Mode. For the DES Mode (which stands for Dual-Edge Sampling), each I- and Q-channel converter samples on the rising or falling edge of the sampling clock. So, for the DES Mode, the conversion latency per channel is unchanged, but both I- and Q-channels are converting the same analog input signal. Sampling on both edges of the clock gives rise to the number of sampling clock cycles being "N+0.5" where N is an integer for  $t_{LAT}$ . This is an interesting contrast to the conversion latency being roughly halved for the ADC12D800/500RF which operates with only one sub-converter, but it is because the sub-converters sample on the same sampling clock whereas the I- and Q-channel converters sample on the rising/falling edge of the sampling clock for the interleaved case.

For the Demux Mode, the outputs are produced on twice the number of buses at half the rate, to ease data capture requirements. For example, in Demux Mode, the ADC12D1800RF will produce data on two 12-bit buses at 900Mps as opposed to one 12-bit bus at 1800Mps for the Non-Demux Mode. This is accomplished by delaying the output at one bus. For example, the DQd bus where "d" stands for "delayed" is one full sample clock cycle delayed from the DQ bus. For example, this is why the DI<sub>d</sub> outputs are delayed by 1 sample clock cycle as compared to the DI outputs.

#### 4 $t_{OD}$ : Sampling Clock to Data Output Delay

From the edge of the sampling clock (FCLK) until the digital data is present at the outputs, there is an analog delay, in addition to the conversion latency, which is  $t_{OD}$ . This represents the total analog delay through the device because it is related to trace delays and parasitics and is a function of PVT, i.e. process, voltage and temperature, as opposed to the conversion latency which is a function of sample clock frequency. Note that  $t_{AD}$  is related to when the analog input is sampled, but  $t_{OD}$  is not affected by  $t_{AD}$ . For example, from [Figure 1](#), the delay from FCLK to data output is  $(t_{AD}) + (t_{LAT} + t_{OD} - t_{AD}) = t_{LAT} + t_{OD}$ .

The challenge in measuring  $t_{OD}$  is that it is not obvious which edge of the sample clock is associated with which data output. Once again, we can rely on the unique properties of a data converter as well as the feature set of the GSPS ADC family to measure this quality. There are two methods which are used to measure  $t_{OD}$ ; by varying the sample clock frequency, and by using the DCLK\_RST feature. Since the total latency is a function only of  $t_{OD}$  and  $t_{LAT}$ , it is possible to isolate  $t_{OD}$  by varying  $t_{LAT}$ , i.e. changing the sample clock frequency. The oscilloscope is set to infinite persistence while observing the output data clock (DCLK) and the sample clock (FCLK) as the sample clock is swept over frequency. It quickly becomes clear that, regardless of frequency, there is one particular edge of FCLK which is responsible for generating a particular edge of DCLK, see [Figure 6](#). This delay is  $t_{OD}$ .



**Figure 6. Measuring  $t_{OD}$  by Varying FCLK**

Another method of measuring  $t_{OD}$  is by using the DCLK\_RST feature. This feature is designed to synchronize the phase of the Data Clocks (DCLK) of multiple ADCs by releasing them at the same time, so that their phases are known and aligned. However, we can also use the feature to measure  $t_{OD}$ . This is accomplished by probing the FCLK, DCLK\_RST, and DCLK and observing the following sequence of events:

- (1) The DCLK\_RST signal is brought low to allow DCLK, after being held high, which prevented the DCLK from being generated.
- (2) The first rising edge of the FCLK, following DCLK\_RST transitioning low, is the edge from which the first DCLK will be generated.
- (3) An integer number of sample clock cycles pass, which are by design. This is specified in the datasheet as  $t_{SYNC\_DLY}$ .
- (4) The DCLK reappears at the output.  $t_{OD}$  is measured between (3) and (4) in [Figure 7](#).



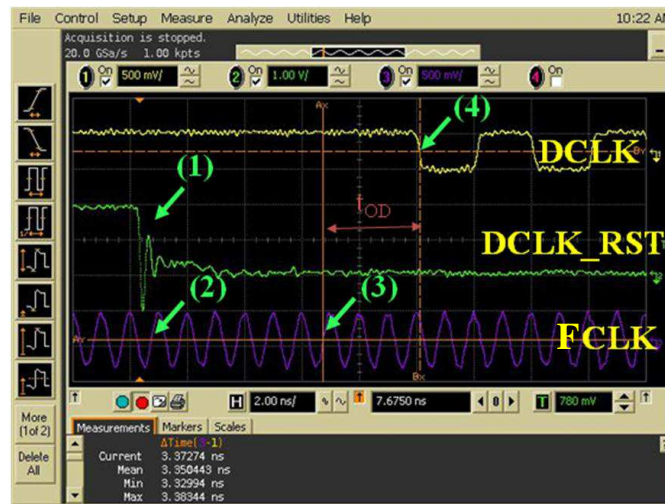


Figure 7. Measuring  $t_{OD}$  by DCLK\_RST Feature

Using both methods of measurement, as well as checking the simulated value, allows for corroboration of the correct value of  $t_{OD}$ .

## 5 Calculating Total Latency

To calculate the total latency, let us look at an example for the ADC12D1800RF. The typical values for  $t_{OD}$  and  $t_{AD}$  are simply found in the datasheet.  $t_{LAT}$  varies, depending upon mode and sample clock frequency. For this example, let us assume that  $F_{CLK} = 1.8$  GHz and that we are looking for the worst case, i.e. longest, conversion latency. From the datasheet, this occurs for the DQd outputs in 1:4 Demux DES Mode at 35.5 sampling clock cycles.

The total latency can be calculated by the equation:

$$\begin{aligned}
 t_{LAT\_ADC} &= t_{LAT} + t_{OD} - t_{AD} \\
 &= (35.5) * (1 / 1.8 \text{ GHz}) + 3.2 \text{ ns} - 1.29 \text{ ns} \\
 &= 21.63 \text{ ns}
 \end{aligned}$$

## 6 Calculating Sample Instant Variation and Variability

For applications with multiple ADCs, which are sensitive to variation in sample instant between ADCs, it is important to understand what the maximum variation may be. In most applications, it is desirable to maintain a variation between ADCs of less than one sample.

From simulation, the largest expected variation is as follows:

- $t_{OD}$  and  $t_{AD}$  vs. Temperature:  $\pm 8.3\%$
- $t_{OD}$  and  $t_{AD}$  vs. Supply:  $\pm 3.6\%$
- $t_{OD}$  and  $t_{AD}$  vs. Process:  $\pm 19.2\%$
- $t_{OD}$  and  $t_{AD}$  vs. Composite PVT:  $\pm 29.7\%$

For example, consider the ADC12D1600RF; here are some of the relevant numbers:

- $t_{OD} = 3.2$  ns
- $t_{AD} = 1.29$  ns
- $F_s = 1600$  MHz;  $T = 625$  ps
- Sample instant max PVT variation =  $\pm 29.7\%$

The time from sampling instant to data output is  $t_{LAT} + t_{OD} - t_{AD}$ . Since the latency for each ADC is the same, and the sampling clock to each is the same,  $t_{LAT}$  may be discounted. The maximum variation is:

$$\begin{aligned}
 &= ( t_{OD} - t_{AD} ) * dt(PVT) \\
 &= ( 3.2 \text{ ns} - 1.29 \text{ ns} ) * \pm 0.297 \\
 &= \pm 0.57 \text{ ns} = 1.13 \text{ ns}
 \end{aligned}$$

Since the max PVT variation > T (1.13 ns > 625 ps), it cannot be guaranteed that the same analog input, sampled at two different ADCs will be present at the same index output sample. However, this can be guaranteed for Fclk < 880 MHz ( T = 1.13 ns ). For a sample which is made at the same instant at two different ADCs, the maximum delta is shown in [Table 2](#). Note that the maximum number of sample instants variation is only N < 3. This is for the extreme corner case of (fast process, max voltage, cold temperature) vs. (slow process, min voltage, hot temperature). It is unlikely that this case will occur in a real world system, but it cannot be guaranteed by design, which is why the TimeStamp feature is necessary.

**Table 2. Maximum Delta Number Sample Instants**

	N < 1	N < 2	N < 3
ADC10D1500/1000	{150 MHz, 1295 MHz}	{1295 MHz, 1500 MHz}	N/A
ADC12D1800/1600/1000	{150 MHz, 821 MHz}	{821 MHz, 1642 MHz}	{1642 MHz, 1800 MHz}
ADC12D800/500RF	{150 MHz, 800 MHz}	N/A	N/A
ADC12D1800/1600/1000RF	{150 MHz, 881 MHz}	{881 MHz, 1762 MHz}	{1762 MHz, 1800 MHz}

The TimeStamp feature can be used to align the sample instant from multiple ADCs in a system. It is the subject of another, future Applications Note, but is described here in brief. When enabled, TimeStamp outputs the 1-bit converted value of the input to the DCLK\_RST+/- pins on the LSB of the 12-bit ADC family. Unfortunately, this means that the TimeStamp feature is not available on the 10-bit ADCs: ADC10D1500/1000. This is because the top 10 MSB of the 12 output bits are used for the 10-bit ADCs, and the 2 LSB are un-bonded. The key to the TimeStamp feature is that the total latency for the conversion of the input to the DCLK\_RST pins is identical to the total latency for the analog inputs. So, it is possible to do a system sample instant synchronization by using TimeStamp and monitoring the LSB; the TimeStamp input must be synchronized to the sampling clock. If the output of one ADC arrives earlier than the others, its data can be easily delayed by the appropriate number of samples in the FPGA.

Once the variation in sample instant variation between ADCs has been determined using the TimeStamp feature, this variation will not change over time or system power cycle, as long as the temperature also varies for both ICs by the same amount. The variation is a function of PVT only. Once the particular ADCs have been soldered down to a board, the process for each ADC will not change. Similarly, once the voltage regulators for each ADC have been soldered down, the voltage to each ADC will not change. Although a temperature differential can cause a change in total latency between ADCs, if all the ADCs in the system experience the same temperature shift, they will also vary their latency by a similar percentage and maintain the same sample instant variation.

## 7 Acknowledgments

The author would like to thank the GSPS ADC team for their support and review of this AN, as well as many customers for asking the questions.



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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
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## EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

**Certain Instructions.** It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

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