National Semiconductor

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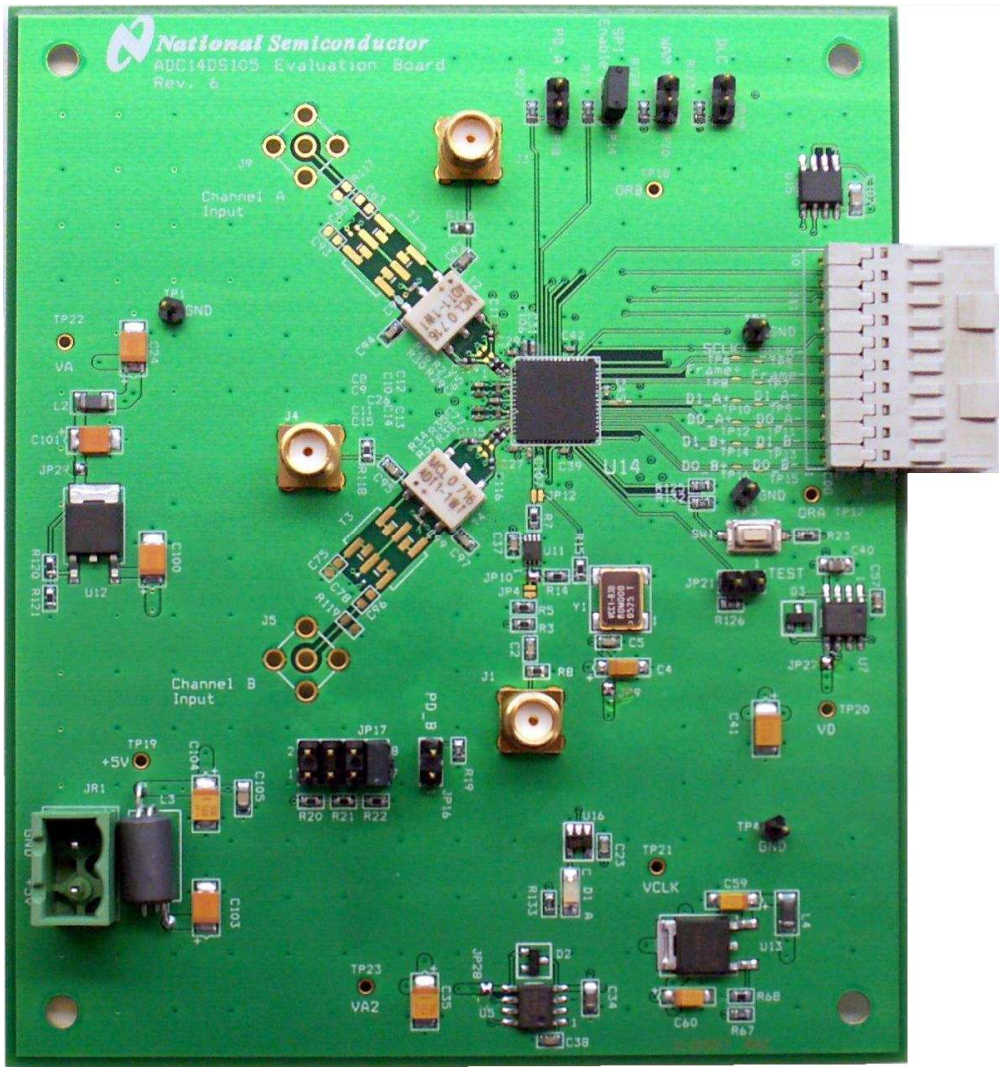
Evaluation Board User's Guide

ADC12DS080, 12-Bit, 80 Msps A/D Converter

ADC14DS080, 14-Bit, 80 Msps A/D Converter

ADC12DS105, 12-Bit, 105 Msps A/D Converter

ADC14DS105, 14-Bit, 105 Msps A/D Converter



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1.0 Introduction

This Evaluation Board may be used to evaluate one of the following A/D Converters : ADC12DS080, ADC14DS080, ADC12DS105, or ADC14DS105. The ADC is one of a family of 12 and 14 bit converters that provides data at rates of up to 105MHz. Further reference in this manual to the ADC14DS105 is meant to also include the other listed parts unless otherwise specifiedThe ADC14DS105LFEB Evaluation Board is for input frequencies less than 70 MHz.

The evaluation board is designed to be used with the WaveVision5™ Signal Path Data Interface Board (WAVEVSN5). The WAVEVSN5 captures and deserializes the LVDS serialized output data from the ADC. The WAVEVSN5 is connected to a personal computer through a USB port and running WaveVision5™ software, operating under Microsoft Windows. The software can perform an FFT on the captured data upon command and, in addition to a frequency domain plot, shows dynamic performance in the form of SNR, SINAD, THD SFDR and ENOB. The latest WaveVision hardware and software is available through the National Semiconductor website.

2.0 Board Assembly

The ADC14DS105 Evaluation Board comes pre-assembled. Refer to the Bill of Materials in *Section 8* for a description of components, to *Figure 1* for major component placement and to *Section 6* for the Evaluation Board schematic.

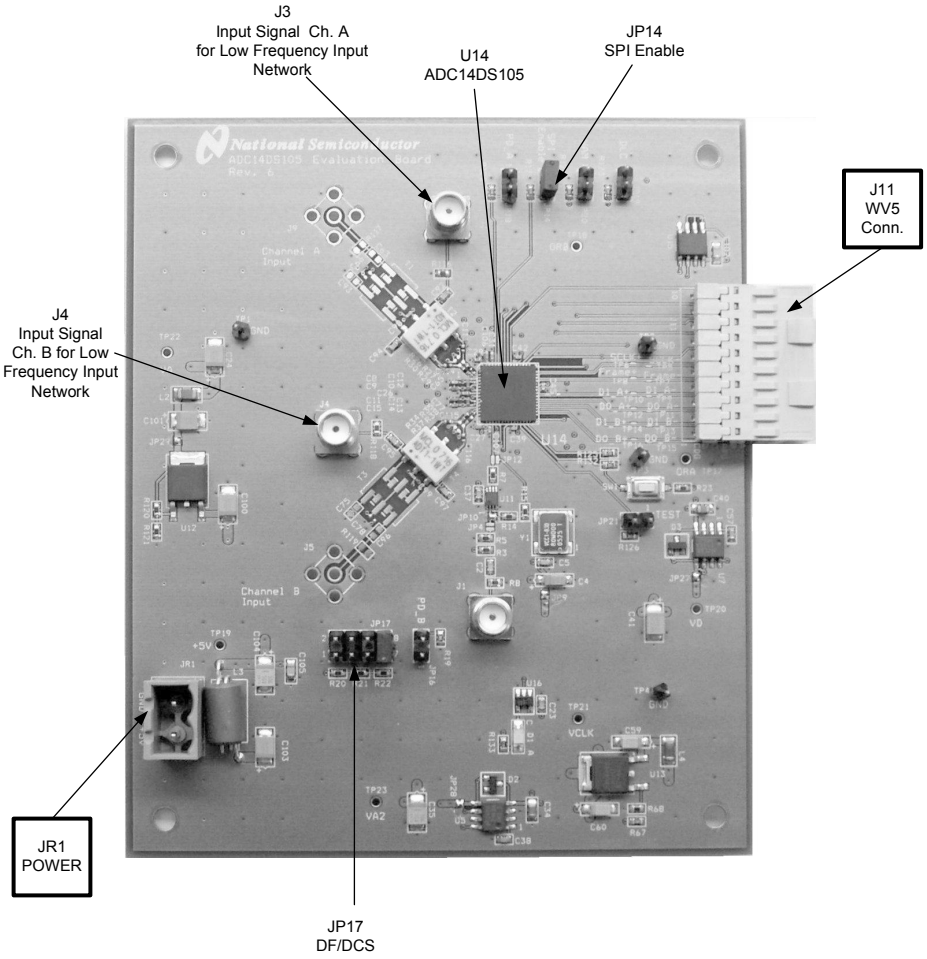


Figure 1. Major Component and Jumper Locations

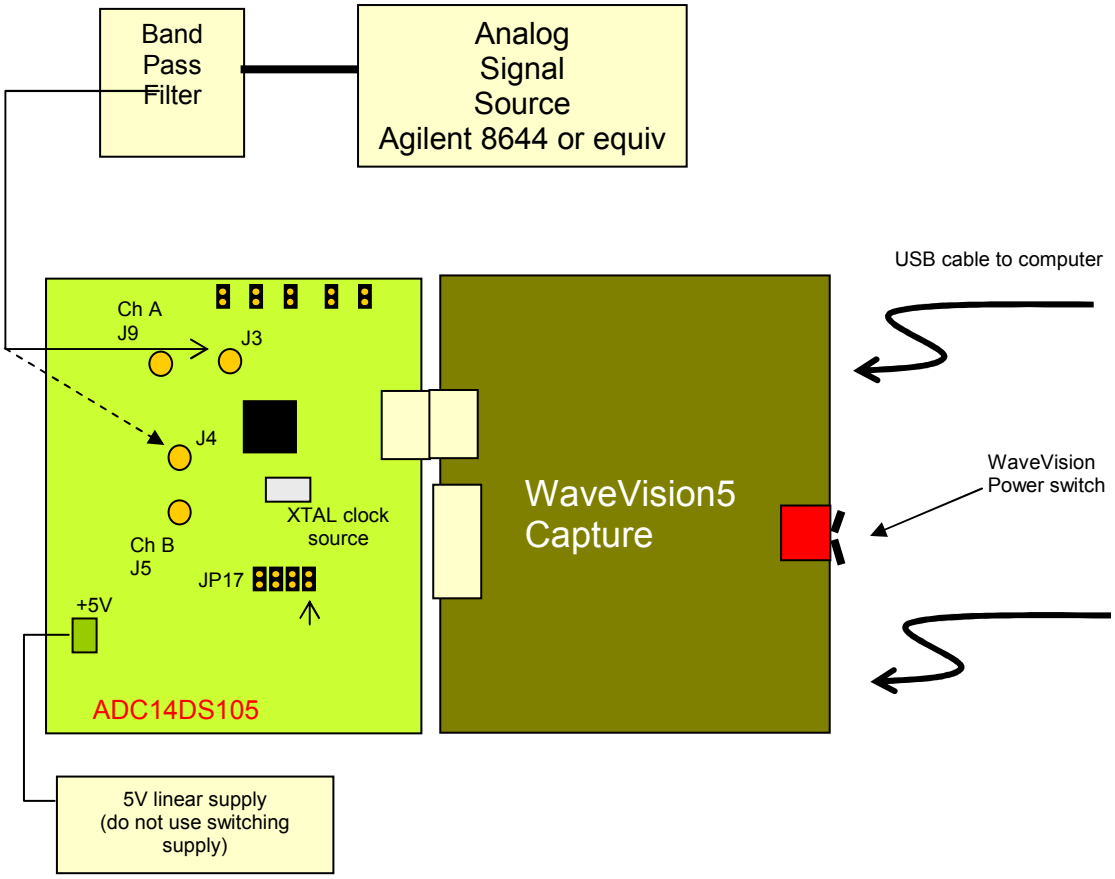


Figure 2. Test Set up

3.0 Quick Start

Refer to *Figure 1* for locations of jumpers, test points and major components. Refer to *Figure 2* for the test set up. The board is configured by default to use a crystal clock source and internal reference. Refer to Section 4.0 and the Appendix for more information on jumper settings.

You must have the WaveVision5™ data capture board and WaveVision5™ software to properly test this board. You can download the latest version from the National Semiconductor website.

1. Apply power to the WAVEVSN5 and connect it to the computer using a USB cable. See the WAVEVSN5 Manual for operation of that board. Connect the evaluation board to the WAVEVSN5. **NOTE: power to the WAVEVSN5 should be applied before power to the ADC14DS105 Evaluation Board to insure that the FPGA on the WAVEVSN5 is not damaged.**
2. Connect a clean +5V power supply to pin 2 of Power Connector JR1. Pin 1 is ground.
3. Connect a signal from a 50-Ohm source to connector J3. Be sure to use a bandpass filter before the Evaluation Board.
4. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examinining a histogram of the output data with the WaveVision™ software.

4.0 Functional Description

The ADC14DS105LFEB schematic is shown in *Section 6.* A list of test points and jumper settings can be found in the Appendix.

4.1 Analog Input

To obtain the best distortion results the analog input network must be optimized for the signal frequency being applied. *Figure 3* shows an example of a circuit that may be used for input frequencies greater than 70MHz. The ADC14DS105LFEB comes configured for input frequencies less than 70MHz. This circuit is shown in *Figure 4*.

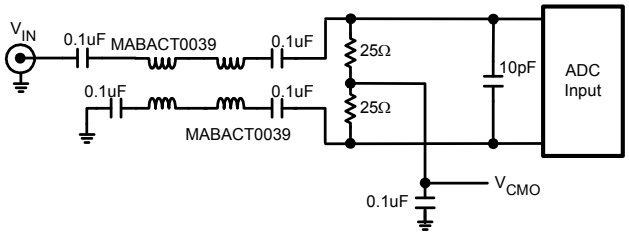


Figure 3. Analog Input Network for F_{IN} > 70MHz

The input network is intended to accept a low-noise sine wave signal of up to 1V peak-to-peak amplitude. To accurately evaluate the dynamic performance of this converter, the input test signal will have to be passed through a high-quality bandpass filter.

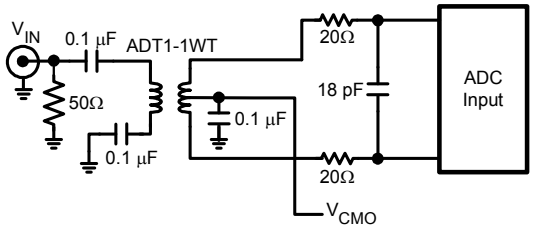


Figure 4. Analog Input Network for F_{IN} < 70MHz

The input signal for Channel A is applied to SMA connector J3. The input signal for Channel B is applied to SMA connector J4.

4.2 ADC reference circuitry

The ADC14DS105 can use an internal or external 1.2V reference. This Evaluation Board is configured to use the internal reference.

4.3 ADC clock circuit

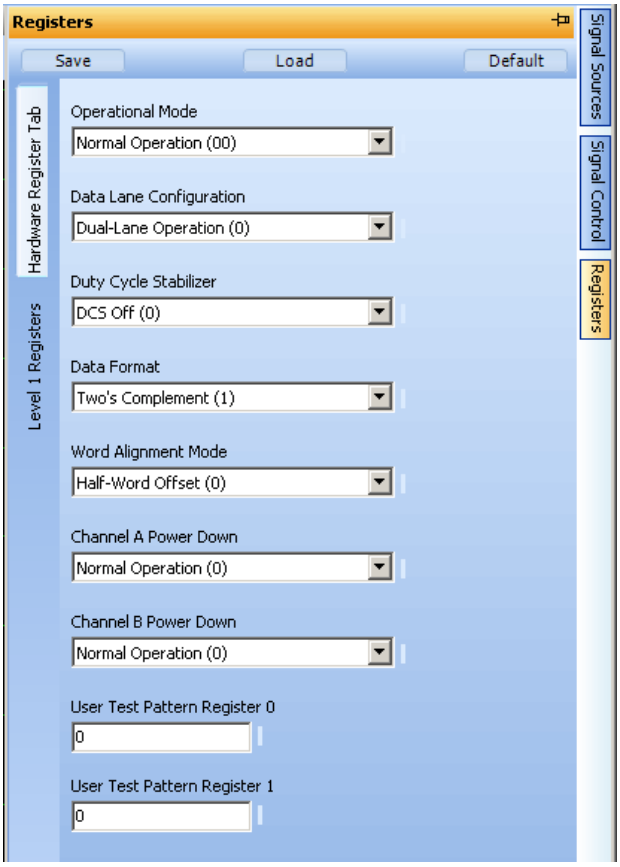
Solder jumpers are used to select the path of the clock to the ADC. While not as convenient as pin-type jumpers, these introduce less noise into the clock signal.

Care must be taken to provide a high quality low jitter clock source. The board has a Pletronics SM7745 or Vectron VCC1 type device crystal clock. The power supply to the crystal has been increased beyond its typical specificied 3.3V to about 3.9V. The crystal manufacturers have indicated that this will not damage the part. This increased voltage results in sharper edges and lower jitter. This is more important as the input frequency increases. The clock is then buffered by U11 (NS7WV125) and applied to the ADC's clock input pin.

The user can configure the board for an external clock at connector J1. For this option short the pins of solder jumper JP4 and open the pins of JP9 and JP10. Refer to the schematic for more detail.

4.4 Control Panel

The ADC14DS105LFEB is designed to be used with the WaveVision5™ Signal Path Data Interface Board (WAVEVSN5). This requires that the SPI is enabled by placing a shorting jumper across JP14. With the SPI enabled, the direct control pins (OF/DCS, WAM, TEST, PD_A, PD_B) have no effect. These functions can be set by changing the fields in the Registers Panel in the WaveVision 5 software. The Registers Panel is shown in *Figure 5*.



4.4.1 Operational Mode

Normal – The ADC is in normal operation

Fixed Test Mode – A fixed test pattern (10100110001110 msb->lsb) is sourced at the data outputs.

User Test Mode – The test pattern shown in the 'User Test Value' field is sourced at the data outputs.

4.4.2 Data Lane Mode

Dual Lane – The output data is for each channel is sourced on two LVDS pairs. This mode is required when the sample rate is greater than 65MHz when using the WAVEVSN5 to capture data.

Single Lane Mode - The output data is for each channel is sourced on one LVDS pairs.

4.4.3 Duty Cycle Stabilizer

On or Off – Select if Duty cycle stabilization is applied to the input clock.

4.4.4 Word Alignment

Half Word Offset or Word Aligned – Select if the output words should be aligned or offset when the part is used in Dual Lane Mode.

4.4.5 Channel A Mode

Select Normal Operation or Power Down

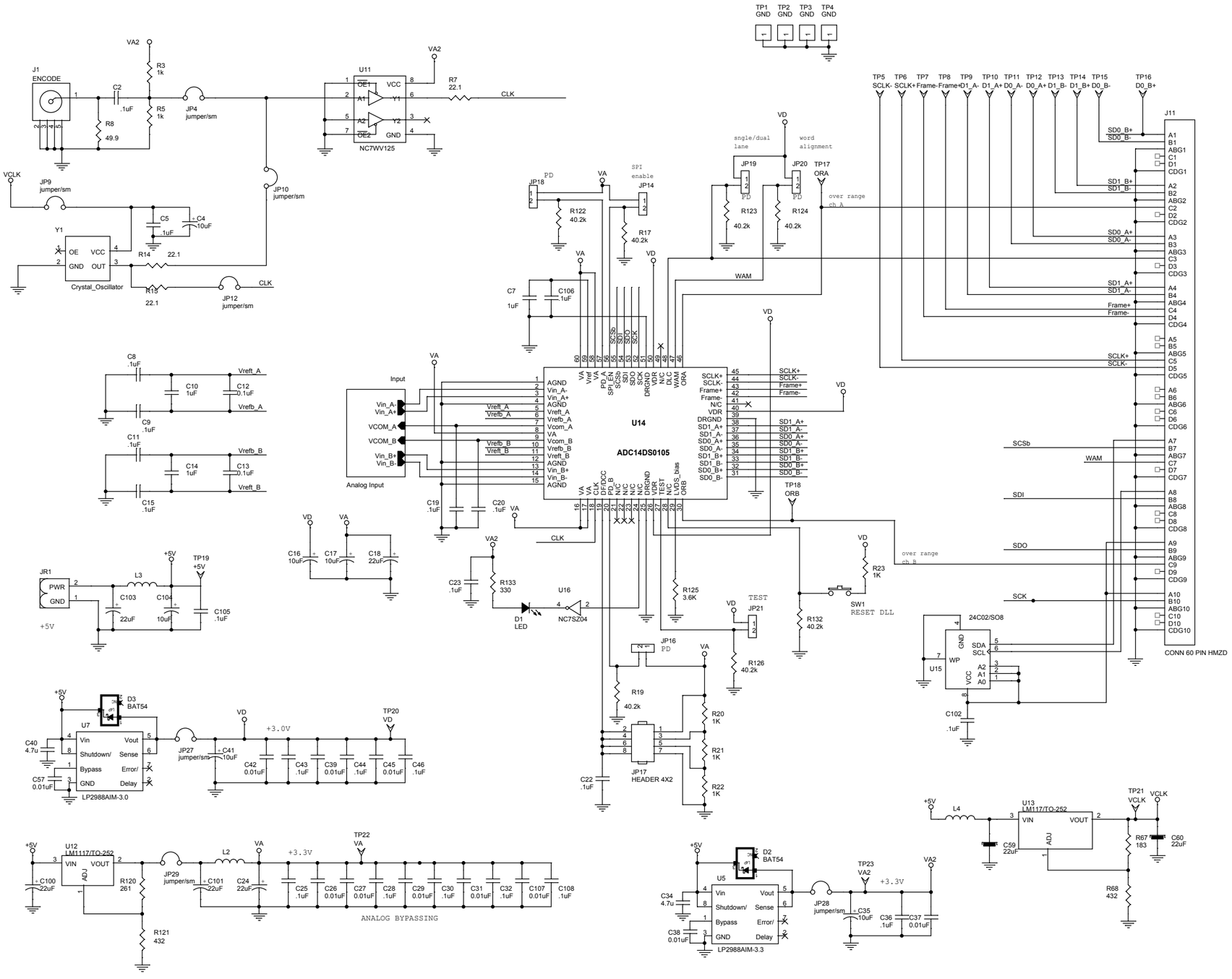
4.4.6 Channel B Mode

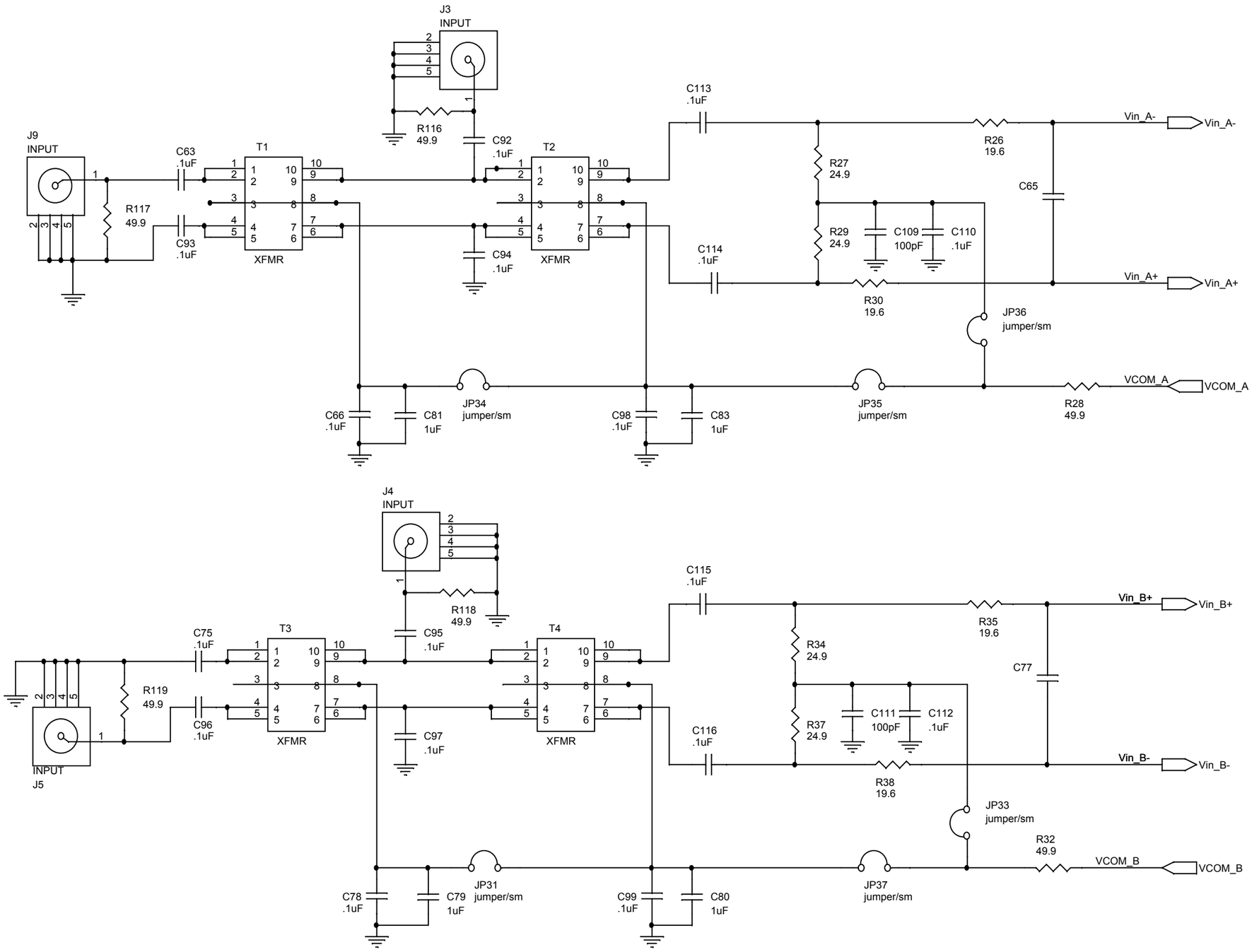
Select Normal Operation or Power Down

4.5 Power Requirements

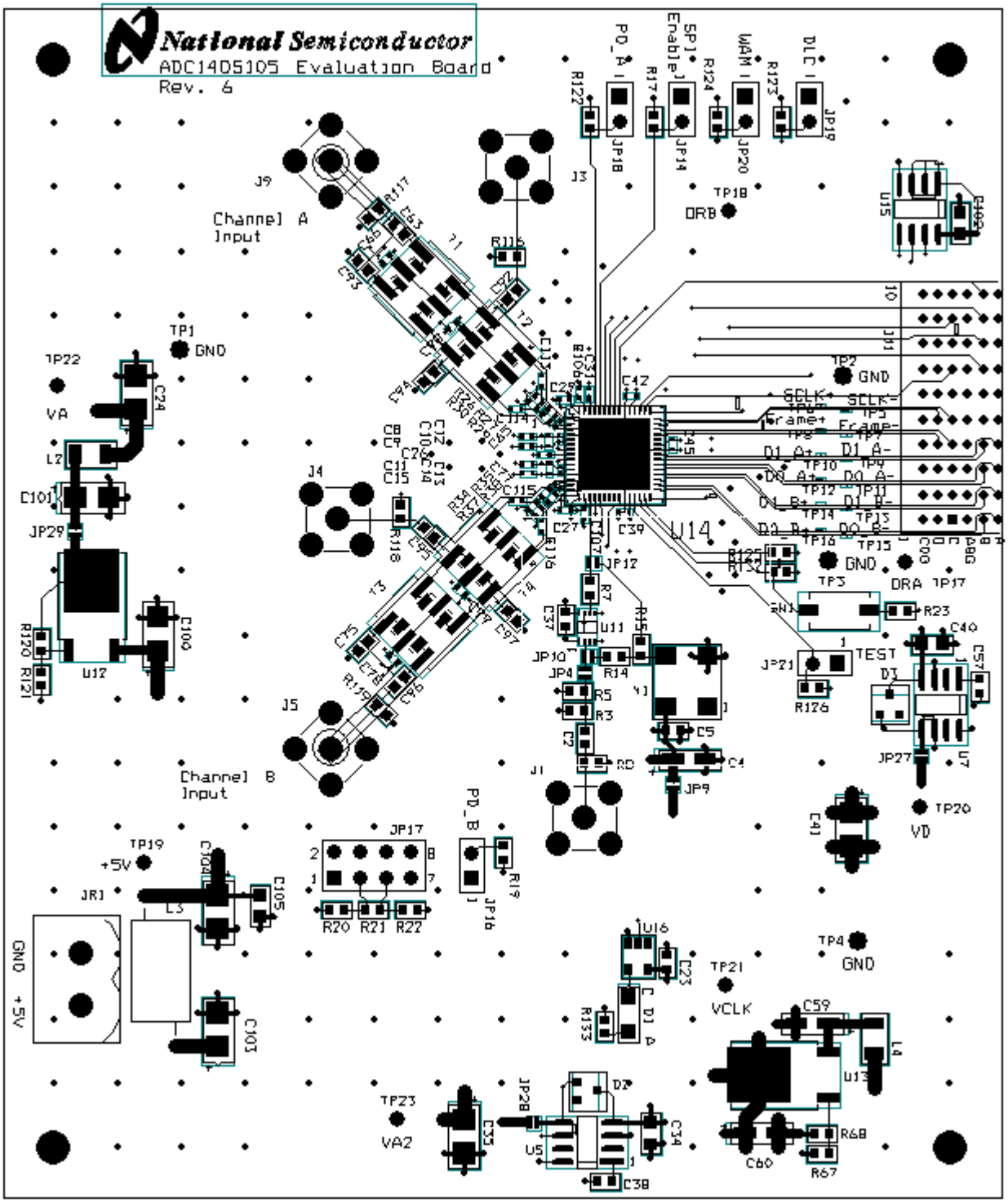
A 5V power supply capable of 0.5A should be connected to JR1. A linear supply is preferred since it will generate less noise than a switching power supply.

6.0 Hardware Schematic

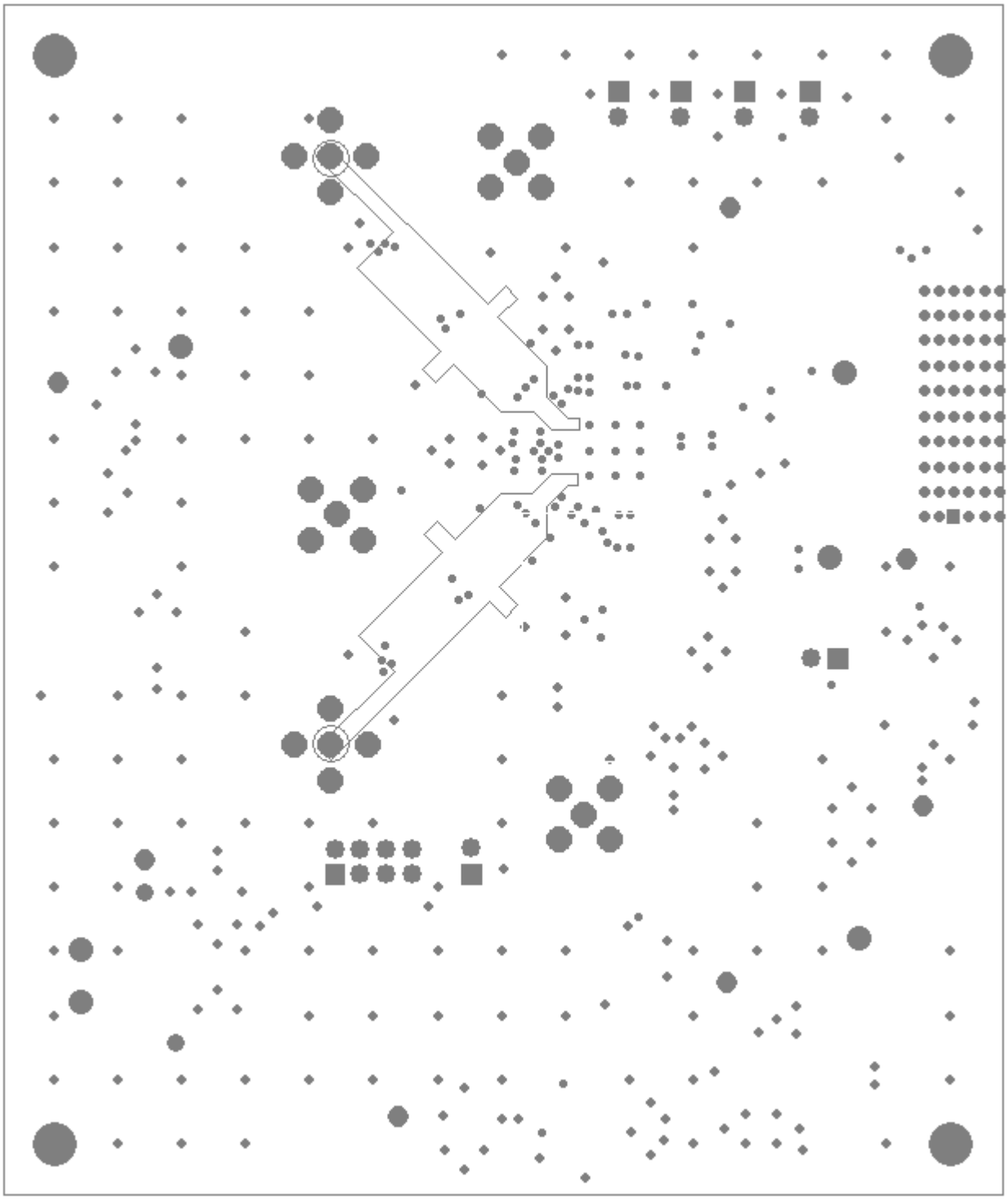



J3
INPUT
R116
49.9
C92
.1uF
J9
INPUT
C63
.1uF
T1
T2
R117
49.9
C93
.1uF
XFMR
XFMR
C94
.1uF
C113
.1uF
R26
19.6
Vin_A-
Vin_A-
R27
24.9
C65
R29
24.9
C109
100pF
C110
.1uF
C114
.1uF
Vin_A+
Vin_A+
R30
19.6
JP36
jumper/sm
C66
.1uF
C81
1uF
JP34
jumper/sm
C98
.1uF
C83
1uF
JP35
jumper/sm
VCOM_A
VCOM_A
R28
49.9
J4
INPUT
R118
49.9
C95
.1uF
C75
.1uF
T3
T4
R119
49.9
C96
.1uF
XFMR
XFMR
C97
.1uF
C115
.1uF
R35
19.6
Vin_B+
Vin_B+
R34
24.9
C77
C116
.1uF
R37
24.9
C111
100pF
C112
.1uF
Vin_B-
Vin_B-
R38
19.6
JP33
jumper/sm
INPUT
J5
C78
.1uF
C79
1uF
JP31
jumper/sm
C99
.1uF
C80
1uF
JP37
jumper/sm
R32
49.9
VCOM_B
VCOM_B

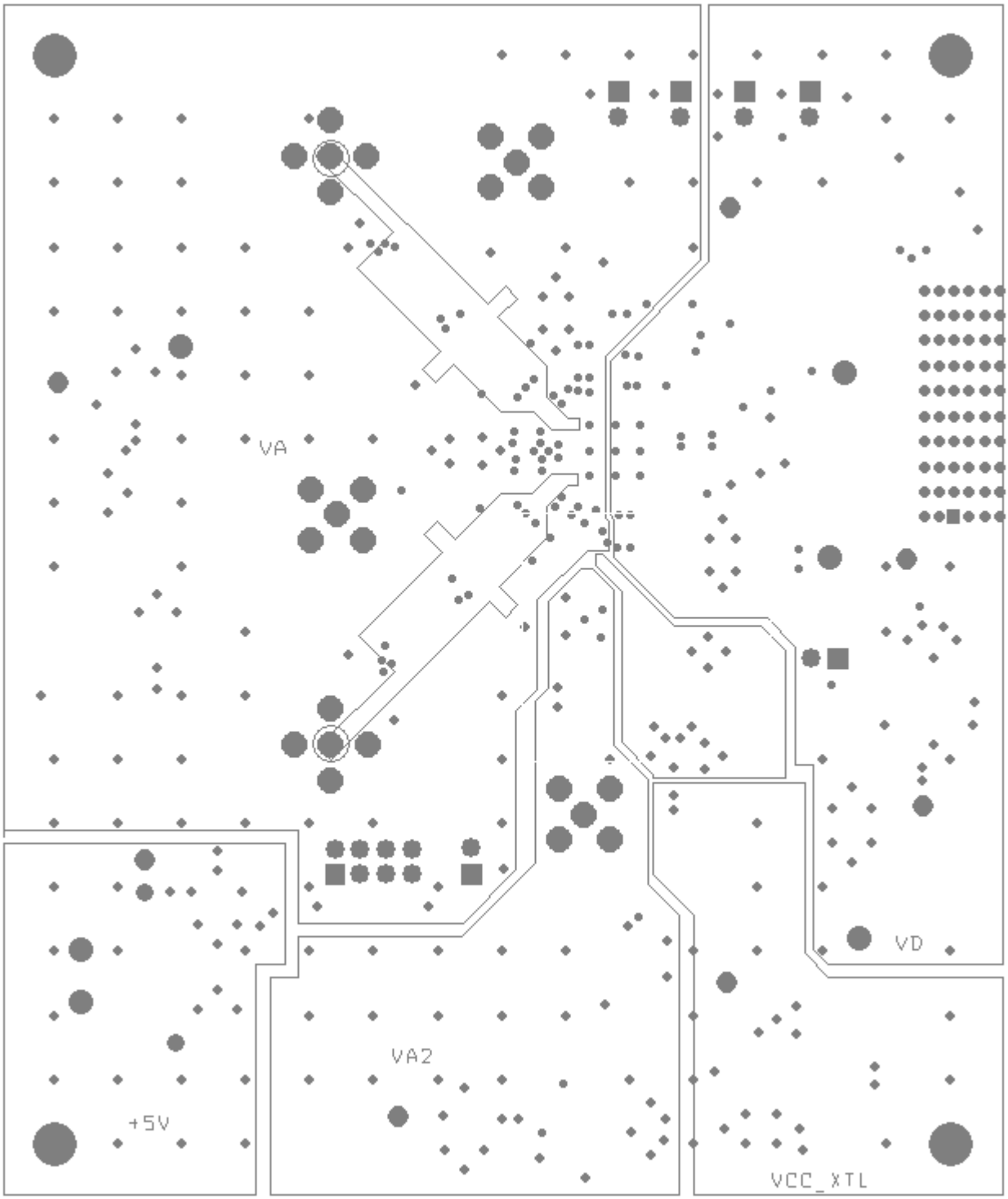
7.0 Evaluation Board Layout



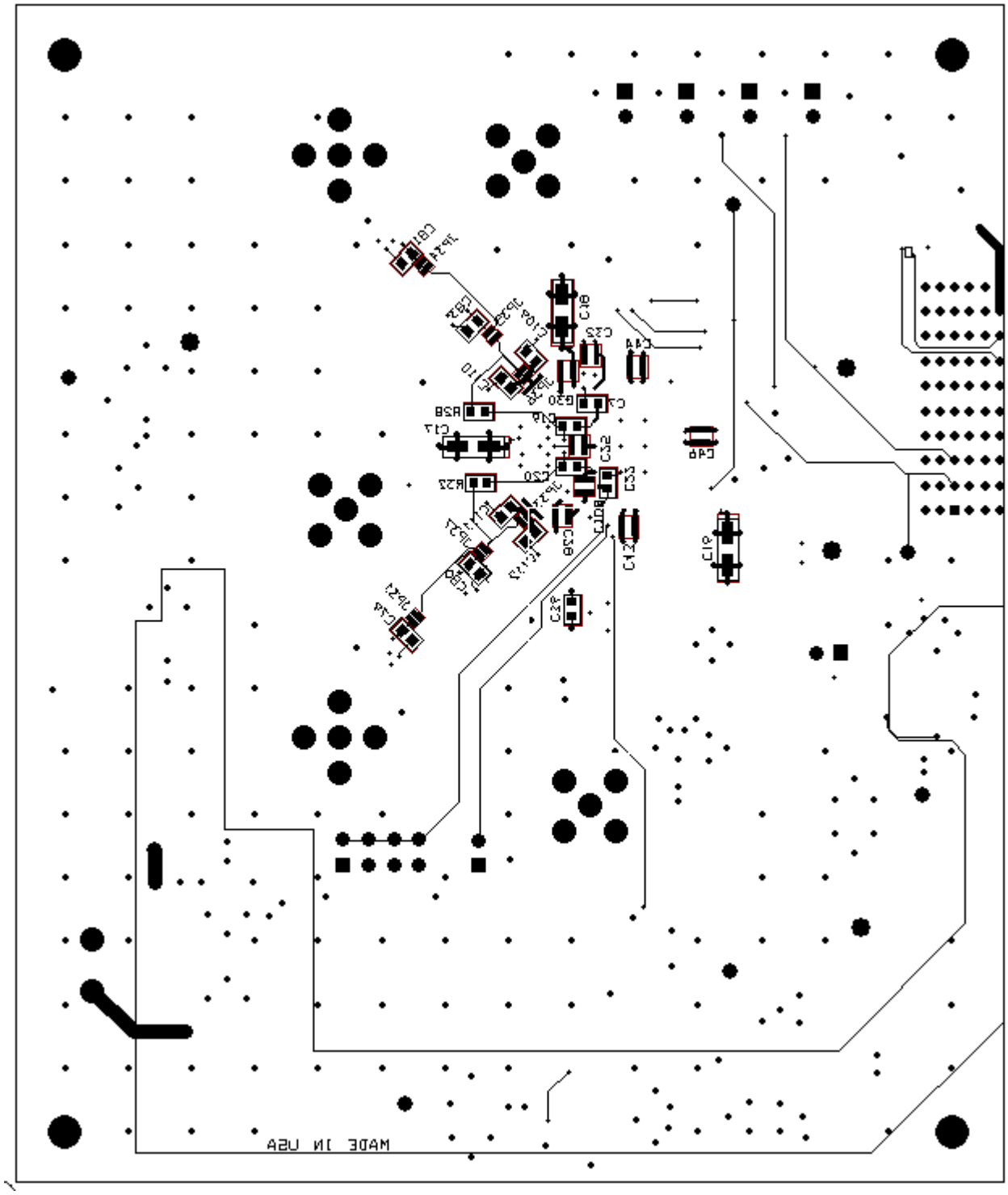
Layer 1 : Component Side



Layer 2 : Ground



Layer 3 : Power



Layer 4 : Circuit Side

8.0 Evaluation Board Bill of Materials

Qty	Reference	Part	PCB Footprint	Part Number	Vendor
13	C2,C5,C19,C20,C22,C23,C36,C92,C94,C95,C97,C110,C112	.1uF	sm/c_0603	PCC1762CT	Digi-Key
3	C4,C16,C17	10uF	sm/ct_3216_12	399-3683-1	Digi-Key
3	C7,C80,C83	1uF	sm/c_0603	PCC2224CT	Digi-Key
7	C8,C9,C11,C15,C98,C99,C106	.1uF	sm/c_0402_no_ss	PCC2146CT	Digi-Key
2	C10,C14	1uF	sm/c_0402_no_ss	PCC13493CT	Digi-Key
2	C12,C13	0.1uF	sm/c_0201_no_ss	PCC2336CT	
1	C18	22uF	sm/ct_3216_12	495-2207-1	Digi-Key
4	C24,C100,C101,C103	22uF	sm/ct_3528_12	478-3476-1	Digi-Key
8	C25,C28,C30,C32,C43,C44,C46,C108	.1uF	sm/c_0508_wide_no_ss	PCC2188CT	Digi-Key
8	C26,C27,C29,C31,C39,C42,C45,C107	0.01uF	sm/c_0402_no_ss	PCC2270CT	Digi-Key
2	C34,C40	4.7u	sm/c_0805	PCC1842CT	Digi-Key
3	C35,C41,C104	10uF	sm/ct_3528_12	495-2238-1	Digi-Key
3	C37,C38,C57	0.01uF	sm/c_0603	PCC1784CT	Digi-Key
2	C59,C60	22uF	SM/CT_3216_12	478-1754-1	Digi-Key
2	C65,C77	18pF	sm/c_0201_no_ss	PCC2116CT	Digi-Key
2	C102,C105	.1uF	sm/c_0805	PCC1828CT	Digi-Key
2	C109,C111	100pF	sm/c_0603	PCC101ACVCT	Digi-Key
1	D1	LED	sm/led_21	516-1440-1-ND	Digi-Key
2	D2,D3	BAT54	SM/SOT23	BAT54-FDICT-ND	Digi-Key
6	JP14,JP16,JP18,JP19,JP20, JP21	Header2	blkcon.100/vh/tm1sqs/w.100/2	929647-09-2	
1	JP17	HEADER 4X2	blkcon.100/vh/tm2oe/w.200/8	929665-09-4	
1	JR1	VA / VD Power	MSTBVA2.5/2-G-5.8	277-1150	Digi-key
1	J1	ENCODE	rf/sma/v_clr	ARFX1231	Digi-key
2	J3,J4	INPUT	rf/sma/v_clr	ARFX1231	Digi-key
1	J11	CONN 60 PIN HMZD	hmzd/2pr/ra/header	6469028-1	National
2	L2,L4	INDUCTOR	sm/l_1206	BLM31PG500SN1L	Digi-Key
1	L3	INDUCTOR	ferrite_choke	M8697	Digi-Key
4	C113,C114,C115,C116	0 ohms	0402 resistor in place of cap	311-0.0JRCT	Digi-Key
6	R3,R5,R20,R21,R22,R23	1K	sm/r_0603	P1.00KHCT	Digi-Key
3	R7,R14,R15	22.1	sm/r_0603	P22.1HCT	Digi-Key
5	R8,R28,R32,R116,R118	49.9	sm/r_0603	P49.9HCT	Digi-Key
7	R17,R19,R122,R123,R124, R126,R132	40.2k	sm/r_0603	311-40.2KHRCT	Digi-Key
4	R26,R30,R35,R38	19.6	sm/r_0402_no_ss	P19.6LCT	Digi-Key
1	R67	183	sm/r_0603	311-182DCT	Digi-Key
2	R68,R121	432	sm/r_0603	P432HCT	Digi-Key
1	R120	261	sm/r_0603	P261HCT	Digi-Key
1	R125	3.6K	sm/r_0603	311-3.60KHRCT	Digi-Key
1	R133	330	sm/r_0603	311-332DCT	Digi-Key

1	SW1	SW PUSHBUTTON	sm/sw	P8087SCT	Digi-Key
2	T2,T4	XFMR	soic10_special	ADT1-1WT+	Minicircuits
1	U5	LP2988AIM-3.3	sog.050/8/wg.244/l.200	LP2988AIM-3.3	Digi-Key
1	U7	LP2988AIM-3.0	sog.050/8/wg.244/l.200	LP2988AIM-3.0/NOPB	National
1	U11	NC7WV125	SOG.50M/8/WG3.10/L2.00	NC7WV125K8X	Mouser
1	U12	LM1117/TO-252	TO252	LM1117DT-ADJ/NOPB	National
1	U13	LM117/TO-252	TO252	LM1117DT-ADJ/NOPB	National
1	U14	ADC14DS080CISQ or ADC14DS105AISQ		ADC14DS080CISQ or ADC14DS105AISQ	National
1	U15	24C02/SO8	sog.050/8/wg.244/l.200	AT24C02AN-10SU-2.7	Mouser
1	U16	NC7SZ04	SM/SOT23-5	NC7SZ04M5X	Mouser
1	Y1	Crystal_Oscillator	SM/CRYSTAL/5X7	SM7745DV-80.0M or SM7745DV-105.0M	Pletronics

	DO NOT POPULATE			
	J5, J9			
	R27, R29, R34, R37, R117, R119			
	C63, C93, C75, C96, C66, C81, C78, C79			
	T1, T3			
	TP1,TP2,TP3,TP4	GND	tp/40	929647-09-1
	TP5	SCLK-	TP_SM/.00525	N/A
	TP6	SCLK+	TP_SM/.00525	N/A
	TP7	Frame-	TP_SM/.00525	N/A
	TP8	Frame+	TP_SM/.00525	N/A
	TP9	D1_A-	TP_SM/.00525	N/A
	TP10	D1_A+	TP_SM/.00525	N/A
	TP11	D0_A-	TP_SM/.00525	N/A
	TP12	D0_A+	TP_SM/.00525	N/A
	TP13	D1_B-	TP_SM/.00525	N/A
	TP14	D1_B+	TP_SM/.00525	N/A
	TP15	D0_B-	TP_SM/.00525	N/A
	TP16	D0_B+	TP_SM/.00525	N/A
	TP17	ORA	TP_500X/50	5002
	TP18	ORB	TP_500X/50	5002
	TP19	+5V	TP_500X/50	5002
	TP20	VD	TP_500X/50	5002
	TP21	VCLK	TP_500X/50	5002
	TP22	VA	TP_500X/50	5002
	TP23	VA2	TP_500X/50	5002

APPENDIX

A1.0 Operating in the Computer Mode

The ADC14DS105 Evaluation Board is compatible with the WaveVision5™ Data Capture Board and WaveVision5™ software.

When connected to the WaveVision5™ Board, data capture is easily controlled from a personal computer operating in the Windows environment. The data samples that are captured can be observed on the PC video monitor in the time and frequency domains. The FFT analysis of the captured data yields insight into system noise and distortion sources and estimates of ADC dynamic performance such as SINAD, SNR, THD, SFDR and ENOB.

A2.0 Summary Tables of Test Points, Connectors, and Jumper Settings

A2.1 Test Points

Test Points on the ADC14DS105 Evaluation Board

Voltage Signal Name	Measure at	Nominal Voltage (V)
+5V	TP19	5
VA	TP22	3.3
VA2	TP23	3.3
VD	TP20	3.0
VCLK	TP21	3.9

A2.2 Connectors

JR1 Connector - Power Supply Connections

1	GND	Power Supply Ground
2	+5V	+5V Power Supply

A2.3 Jumper settings

Note: Default settings are in **bold**

JP14 : SPI Enable

Connect 1-2	**The SPI mode is enabled. This is required when using the ADC14DS105LFEB with the WAVEVSN5. With the SPI enabled, the direct control pins (OF/DCS, WAM, TEST, PD_A, PD_B) have no effect.**
1-2 OPEN	The ADC is in normal operation

When the SPI is enabled, the setting of the following jumpers (JP16 – JP21) have no affect. These functions are controlled through the SPI interface.

JP18 : Power Down Channel A

Connect 1-2	Channel A of the ADC is in power down mode
1-2 OPEN	**The ADC is in normal operation**

JP16 : Power Down Channel B

Connect 1-2	Channel B of the ADC is in power down mode
1-2 OPEN	**The ADC is in normal operation**

JP17 : Output Data Format and Duty Cycle Stabilizer

Connect 1-2	Output format is 2's complement, DCS is Off
Connect 3-4	Output format is 2's complement, DCS is On
Connect 5-6	Output format is offset binary, DCS is On
Connect 7-8	**Output format is offset binary, DCS is Off**

JP19 : Single Lane/Dual Lane

Connect 1-2	Single Lane
1-2 OPEN	**Dual Lane**

JP20 : Word Alignment

Connect 1-2	The output words are aligned.
1-2 OPEN	**The output data words are offset by a half-word.**

JP21 : TEST

Connect 1-2	The ADC is in fixed test mode, a fixed test pattern (10100110001110 msb->lsb) is sourced at the data outputs.
1-2 OPEN	**The ADC is in normal operation**

A2.4 Clock Circuit Solder Jumper settings

Solder jumpers are used to select the path of the clock to the ADC. While not as convenient as pin-type jumpers, these introduce less noise into the clock signal.

By default the following jumpers are OPEN: JP9, JP10

By default the following jumpers are shorted: JP4, JP12

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