

Evaluation Board Instruction Manual

ADC14L020, 14-Bit, 20 Msps, 3.3V, 150 mW A/D Converter

ADC14L040, 14-Bit, 40 Msps, 3.3V, 235 mW A/D Converter

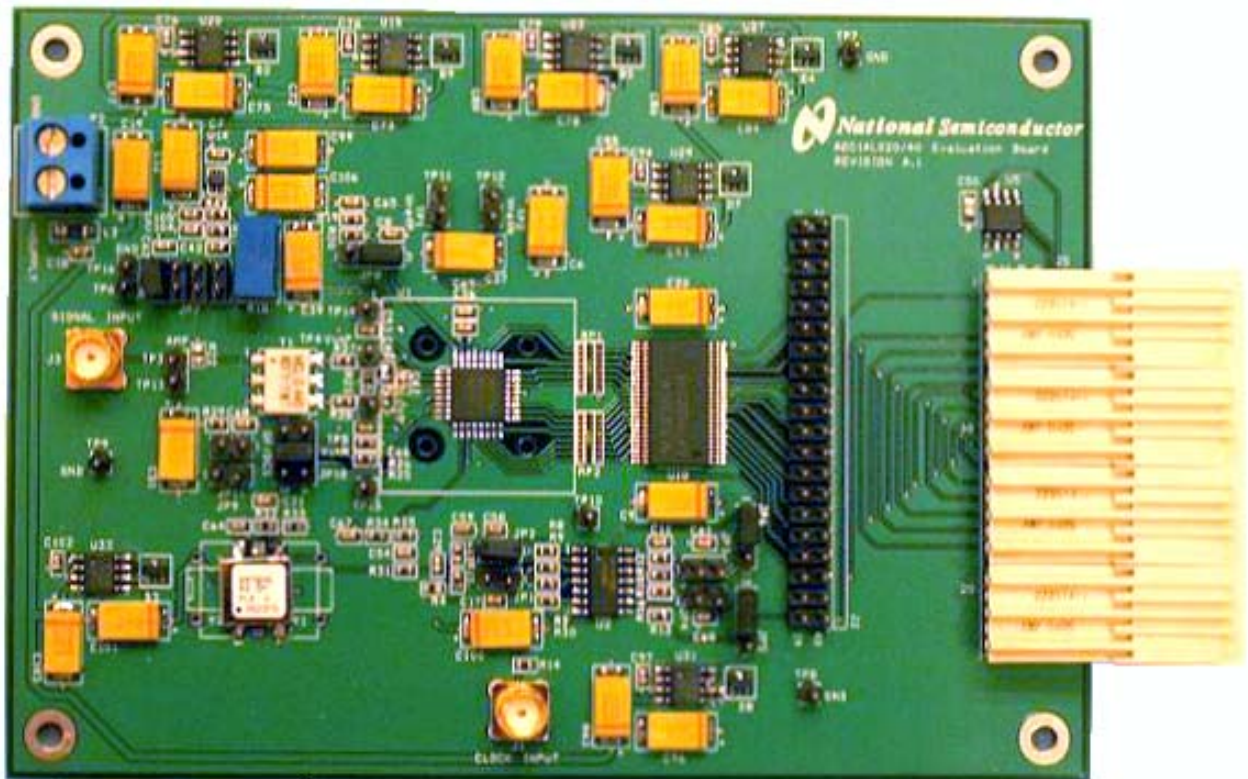


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1.0 Introduction

This Design Kit (consisting of an Evaluation Board and this manual) is designed to ease evaluation and design-in of National Semiconductor's ADC14L020 or ADC14L040 14-bit Analog-to-Digital Converters, which operate at speeds up to 20 Msps and 40 Msps respectively. Further reference in this manual to the ADC14L040 is meant to also include the ADC14L020 unless otherwise specified.

The evaluation board can be used in either of two modes. In the Manual mode suitable test equipment can be used with the board to evaluate the ADC14L040 performance. In the Computer mode evaluation is simplified by connecting the board to the WaveVision™ Digital Interface Board (order number WAVEVSN BRD 4.0), which is connected to a personal computer through a USB port and running WaveVision™ software, operating under Microsoft Windows. The software can perform an

FFT on the captured data upon command and, in addition to a frequency domain plot, shows dynamic performance in the form of SNR, SINAD, THD and SFDR.

The digital output data is available at pins B4 (MSB) through B17 of the WaveVision™ (WV4) connector J5 and odd-numbered pins 9 (MSB) through 35 of header J2. Header J2 is compatible with the National Semiconductor FC Capture Board, however, the WaveVision™ Digital Interface Board is recommended.

2.0 Board Assembly

The ADC14L040 Evaluation Board comes pre-assembled. Refer to the Bill of Materials in *Section 10* for a description of components, to *Figure 1* for major component placement and to *Section 8* for the Evaluation Board schematic.

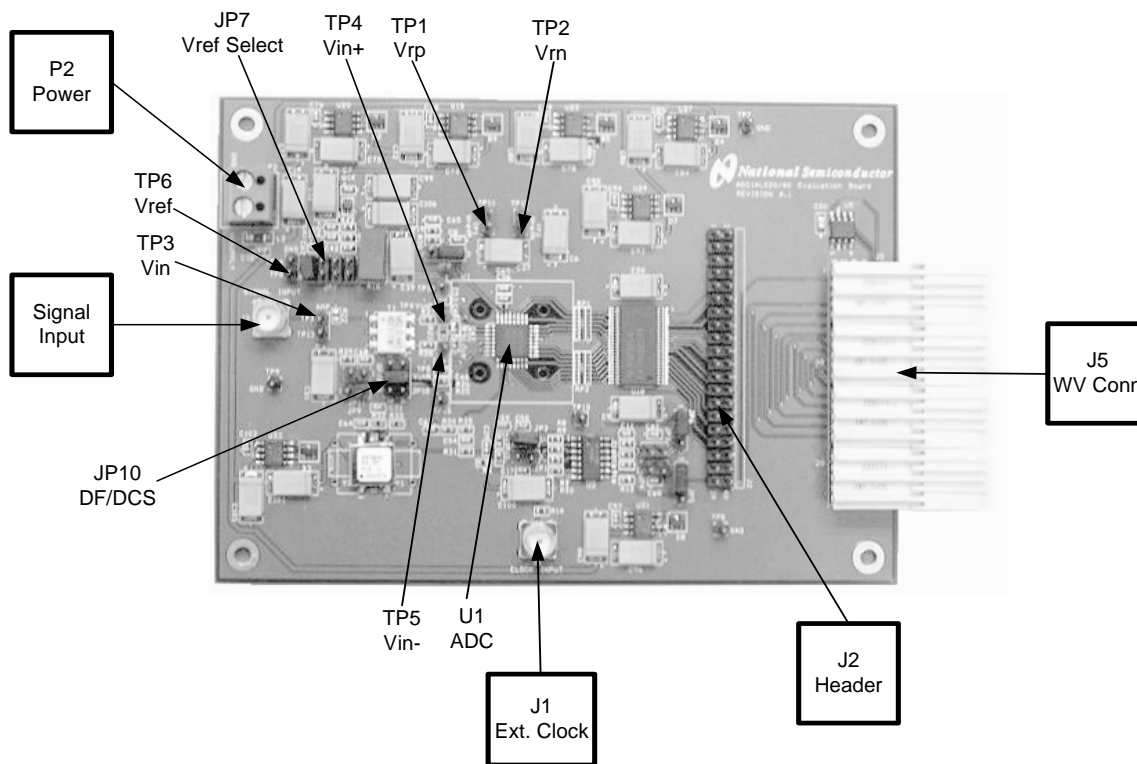


Figure 1. Major Component and Jumper Locations

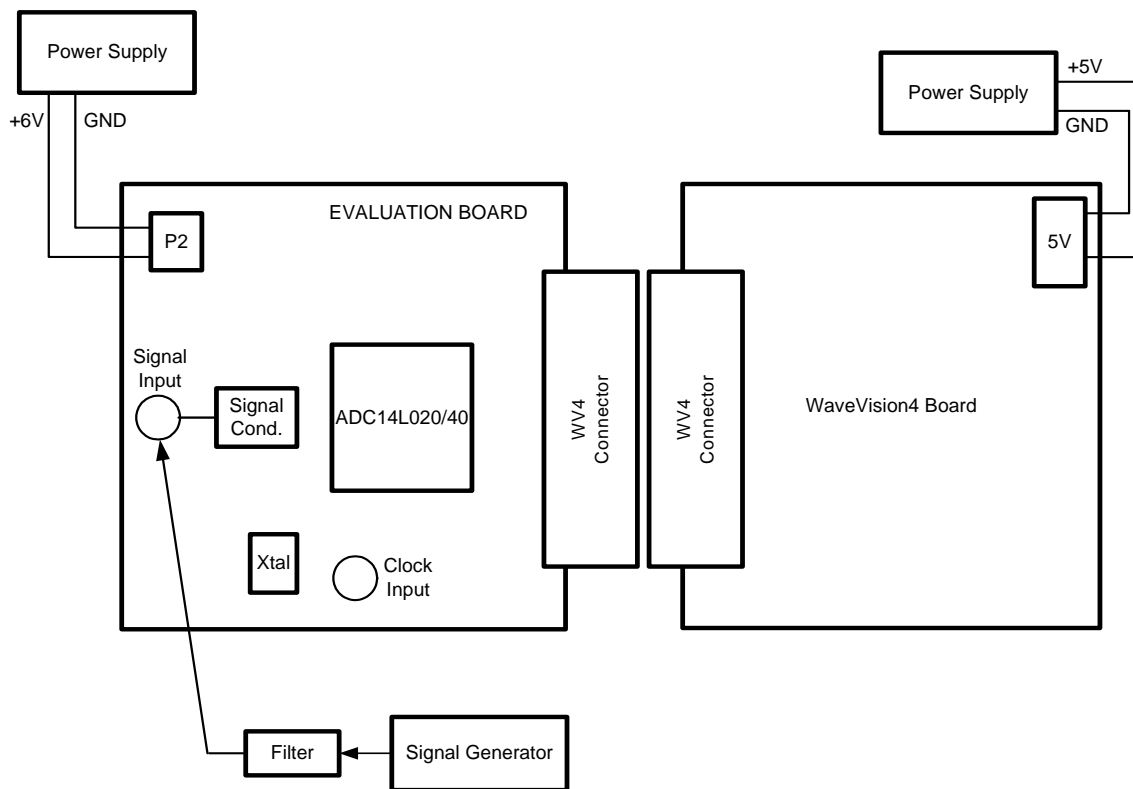


Figure 2. Test set up in Computer Mode

3.0 Quick Start

Refer to *Figure 1* for locations of jumpers, test points and major components. The board is configured by default to use a crystal clock source, internal 1.0V reference, offset binary output data format, and duty cycle stabilizer on. Refer to Section 4.0 and the Appendix for more information on jumper settings.

For Stand-Alone operation:

1. Connect a clean +6V power supply to pin 1 of Power Connector P2. Pin 2 is ground.
2. Connect a signal from a 50-Ohm source to connector J3. The ADC input signal can be observed at TP3. Be sure to use a bandpass filter before the Evaluation Board. Set the input signal amplitude to approximately 1.9Vpp as seen at TP3.
3. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data.
4. The digitized signal is available at odd-numbered pins 9 (MSB) through 35 of header J2. See board schematic in *Section 8*.

For Computer Mode operation:

You can download the latest version WaveVision™ software from:

<http://www.national.com/appinfo/adc/wv4.html>

1. The test set up is shown in *Figure 2*. Connect the evaluation board to the WaveVision™ Digital Interface Board. See the WaveVision™ Board Manual for operation of that board. Connect the WaveVision™ board to the computer using a USB cable. Connect a clean +5V power supply to the WaveVision™ board
2. Connect a clean +6V power supply to pin 1 of Power Connector P2. Pin 2 is ground.
3. Connect a signal from a 50-Ohm source to connector J3. The ADC input signal can be observed at TP3. Be sure to use a bandpass filter before the Evaluation Board. Set the input signal amplitude to approximately 1.9Vpp as seen at TP3.
4. Press the F1 key on the computer to acquire data. Adjust the input signal amplitude as needed to ensure that the signal does not over-range by examining a histogram of the output data with the WaveVision™ software.

4.0 Functional Description

The ADC14L040 Evaluation Board schematic is shown in *Section 8*. A list of test points and jumper settings can be found in the Appendix.

4.1 Input (signal conditioning) circuitry

The input signal to be digitized should be applied to SMA connector J3. This 50 Ohm input is intended to accept a low-noise sine wave signal of up to 2V peak-to-peak amplitude. To accurately evaluate the dynamic performance of this converter, the input test signal will have to be passed through a high-quality bandpass filter with at least 16-bit equivalent noise and distortion characteristics.

Signal transformer T1 provides single-ended to differential conversion. The voltage V_{RM} sets the common mode of the input signal by biasing the center tap of the secondary of T1.

4.2 ADC reference circuitry

The ADC14L040 can use an internal 1.0V reference, an internal 0.5V reference, or an external reference. The reference is selected using jumper JP7. The default is the internal 1.0V reference, shorting pins 7-8.

An adjustable reference circuit is provided on the board. The simple circuit here is not temperature stable and is not recommended for your final design solution. The reference circuit will generate a voltage in the range of 0.5 to 2.0V. The ADC14L040 is specified to operate with V_{REF} in the range of 0.8 to 1.2V, with a nominal value of 1.0V. The reference voltage is set with R18. Short pins 1-2 of JP7 to select this voltage as the reference.

Short pins 3-4 of JP7 to select the internal 0.5V reference.

To use an external reference voltage, remove the jumper from JP7 and apply the voltage to pin 4.

4.3 ADC clock circuit

The default clock source is the crystal, Y1. To use an external clock source, remove Y1 and R31, install a 0 ohm resistor at R4, and apply a clock source to connector J1.

4.4 Digital Data Output

The digital output data is available at pins B4 (MSB) through B17 of the WaveVision™ (WV4) connector J5 and odd-numbered pins 9 (MSB) through 35 of header J2.

4.5 Data Format/ Duty Cycle Stabilizer

Output data format and the duty cycle stabilizer (DCS) are controlled by jumper JP10.

Shorting pins 1-2 of JP10 sets the output format to 2's complement with DCS Off.

Shorting pins 3-4 of JP10 sets the output format to offset binary with DCS On. This is the default setting.

Shorting pins 5-6 of JP10 sets the output format to 2's complement with DCS On.

With no shorting jumper on JP10, the output format is offset binary and DCS is Off.

4.6 Power Supply Connections

Power to this board is supplied through power connector P2. The only supply needed is +6V at pin 1 plus ground at pin 2.

4.7 Power Requirements

Voltage and current requirements for the ADC14L040 Evaluation Board mode are:

- +6.0V at 500 mA

5.0 Installing the ADC14L040 Evaluation Board

The evaluation board requires power supplies as described in *Section 4.7*. An appropriate signal source should be connected to the Signal Input SMA connector J3. When evaluating dynamic performance, an appropriate signal generator (such as the HP8644B or the R&S SME-03) with 50 Ohm source impedance should be connected to the Analog Input connector J3 through an appropriate bandpass filter as even the best signal generator available can not produce a signal pure enough to evaluate the dynamic performance of an ADC.

If this board is used in conjunction with the the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software, a USB must be connected between the Digital Interface Board and the host. See the the WaveVision™ 4.0 Digital Interface Board manual for details.

6.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. The layout is taken care of with the design of this evaluation board. The FFT plots shown in this section are not from an ADC14L040, however, they illustrate the points made here.

6.1 Clock Jitter

When any circuitry is added after a signal source, some jitter is almost always added to that signal. Jitter in a clock signal, depending upon how bad it is, can degrade dynamic performance. We can see the effects of jitter in the frequency domain (FFT) as "leakage" or "spreading" around the input frequency, as seen in *Figure 3*. Compare this with the more desirable plot of *Figure 4*. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

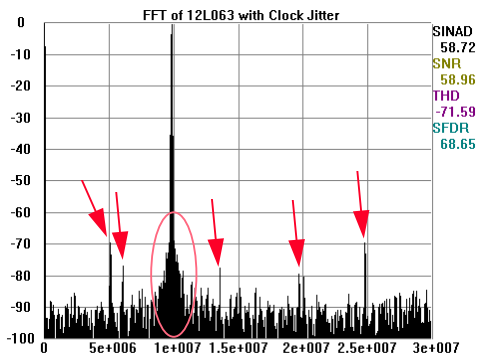


Figure 3. Jitter causes a spreading around the input signal, as well as undesirable signal spurs.

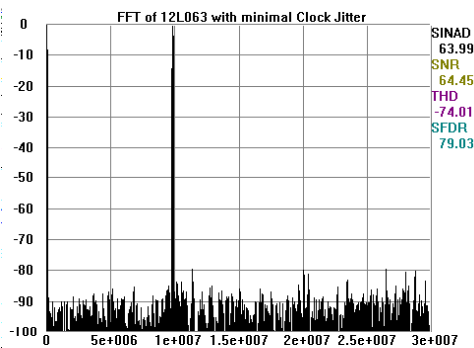


Figure 4. Eliminating or minimizing clock jitter results in a more desirable FFT that is more representative of how the ADC actually performs.

$$\frac{CY}{SS} = \frac{f_{in}}{f_s}$$

CY, the number of cycles in the data record, must be a prime integer number and SS, the number of samples in the data record, must be a factor of 2 integer.

Further, f_{in} (signal input frequency) and f_s (sampling rate) should be locked to each other so that the relationship between the two frequencies is exact. Locking the two signal sources to each other also causes whatever sample-to-sample clock edge timing variation (jitter) that is present in the two signals to cancel each other.

Windowing (an FFT Option under WaveVision™) should be turned off for coherent sampling.

7.0 Evaluation Board Specifications

Board Size:	3.5" x 5.253"
Power Requirements:	+6.0V, 0.5 A
Clock Frequency	20/40 MHz
Range:	
Analog Input	
Nominal Voltage:	2V _{P-P}
Impedance:	50 Ohms

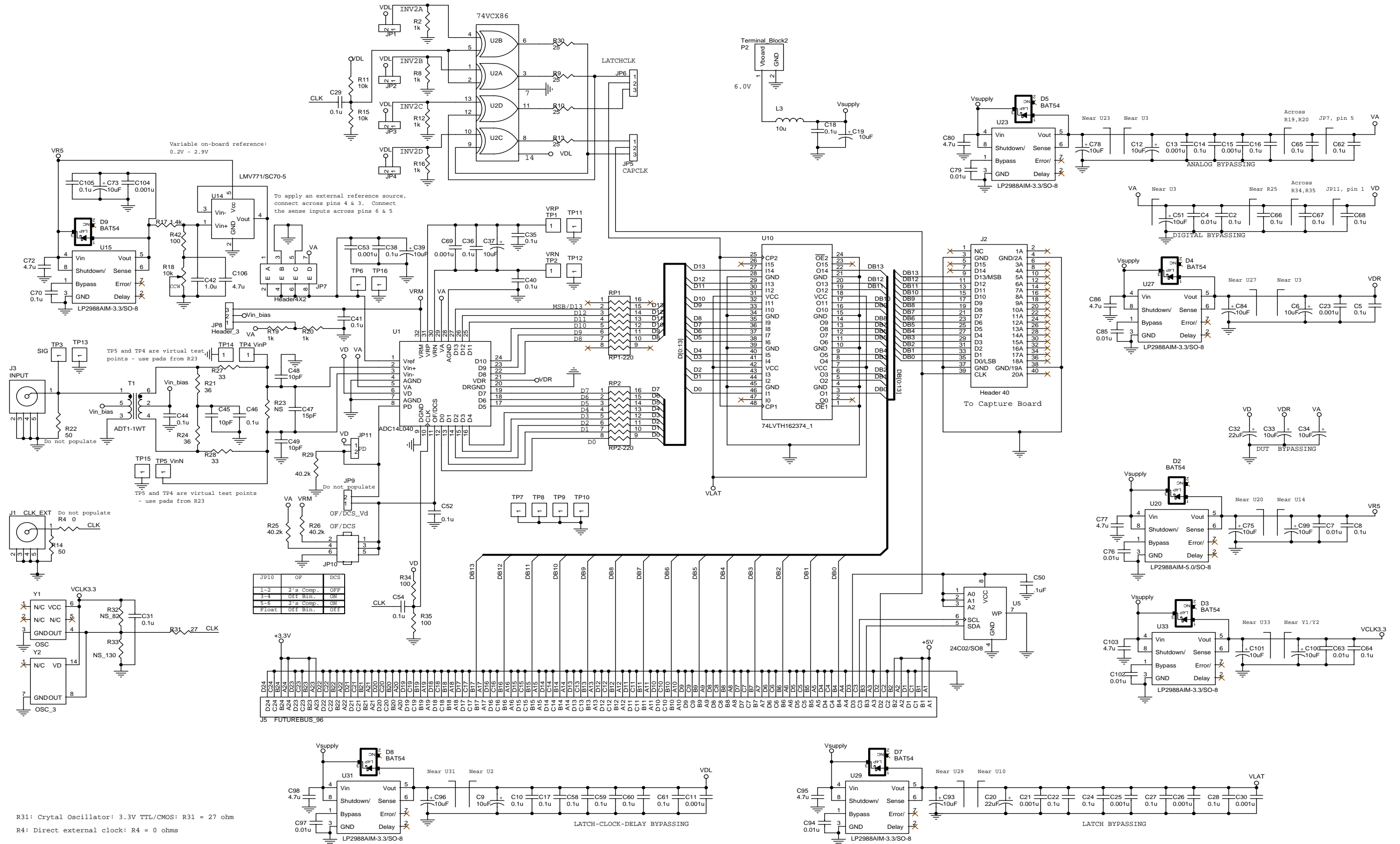
6.2 Coherent Sampling

Artifacts can result when we perform an FFT on a digitized waveform, producing inconsistent results when testing repeatedly. The presence of these artifacts means that the ADC under test may perform better than the measurements would indicate.

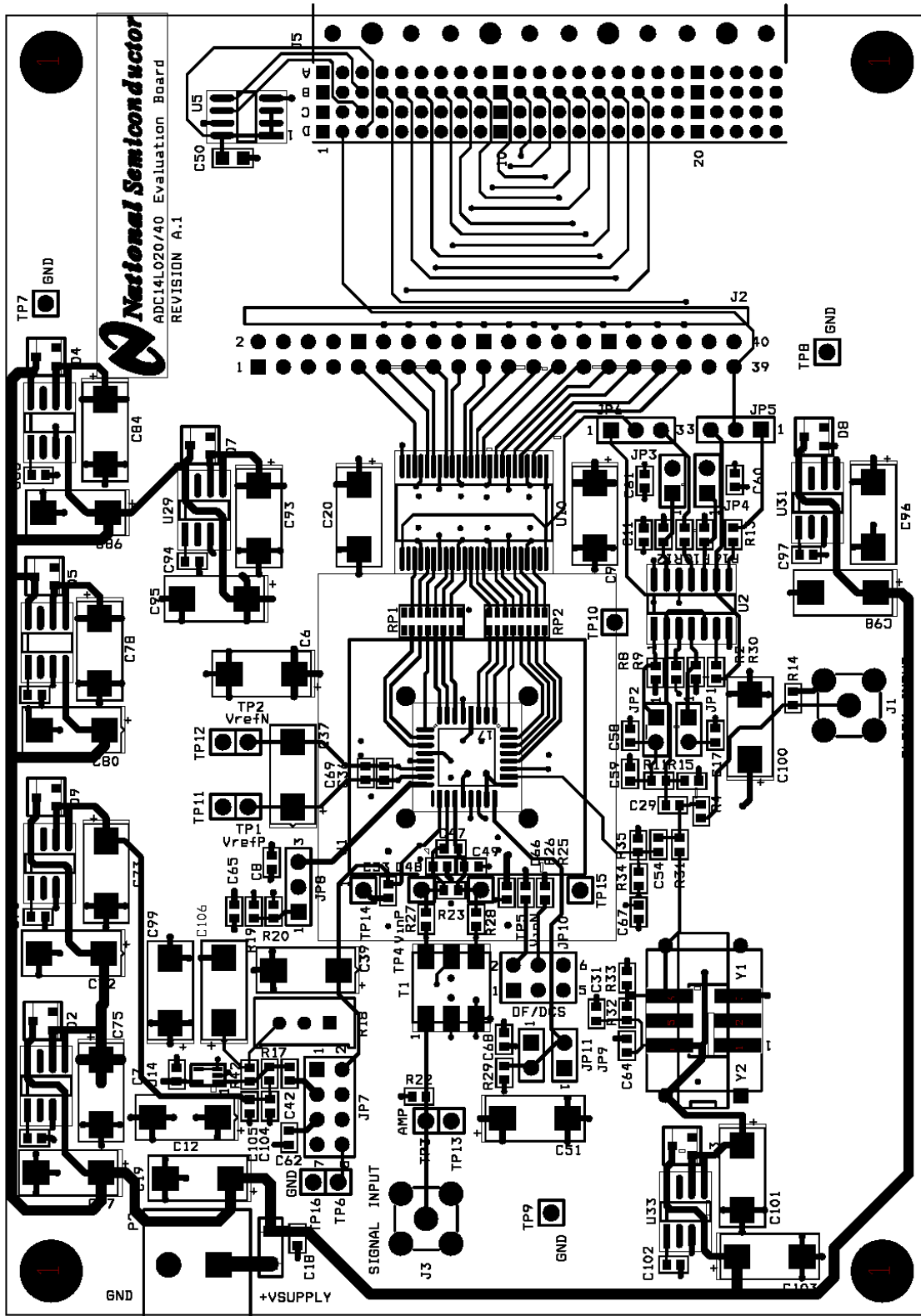
We can eliminate the need for windowing and get more consistent results if we observe the proper ratios between the input and sampling frequencies. We call this *coherent sampling*. Coherent sampling greatly increases the spectral resolution of the FFT, allowing us to more accurately evaluate the spectral response of the A/D converter. When we do this, however, we must be sure that the input signal has high spectral purity and stability and that the sampling clock signal is extremely stable with minimal jitter.

Coherent sampling of a periodic waveform occurs when a prime integer number of cycles exists in the sample window. The relationship between the number of cycles sampled (CY), the number of samples taken (SS), the signal input frequency (f_{in}) and the sample rate (f_s), for coherent sampling, is

8.0 Hardware Schematic



9.0 Assembly Drawing



10.0 Evaluation Board Bill of Materials

Qty	Reference	Part	Part Number
35	C2,C5,C8,C10,C14,C16,C17, C18,C22,C24,C27,C28,C29, C31,C35,C36,C38,C40,C41, C44,C46,C52,C54,C58,C59, C60,C61,C62,C64,C65,C66, C67,C68,C70,C105	0.1u	PCC1762CT
9	C4,C7,C63,C76,C79,C85, C94,C97,C102	0.01u	PCC1784CT
16	C6,C9,C12,C19,C37,C39, C51,C73,C75,C78,C84,C93, C96,C99,C100,C101	10uF	399-1635-1
11	C11,C13,C15,C21,C23,C25, C26,C30,C53,C69,C104	0.001u	PCC1772CT
1	C20	22uF	PCS3226CT
1	C32	22uF	P11304CT
2	C33,C34	10uF	399-1551-1
1	C42	1.0u	PCC2224CT
3	C45,C48,C49	10pF	PCC100CVCT
1	C47	Do not populate	
1	C50	.1uF	PCC1828CT
8	C72,C77,C80,C86,C95,C98, C103,C106	4.7u	399-1651-1
7	D2,D3,D4,D5,D7,D8,D9	BAT54	BAT54FSCT
5	JP1,JP2,JP3,JP4, JP11	Header2	S1011
3	JP5,JP6,JP8	Header_3	S1011
1	JP7	Header4X2	S2011
1	JP10	HEADER 3X2	S2011
1	J1	CLK_EXT	ARFX1231
1	J2	Header 40	S2011
1	J3	INPUT	ARFX1231
1	J5	FUTUREBUS_96	223514-1
1	L3	10u	490-1056-1
1	P2	Terminal_Block2	ED1609
1	RP1	RP1-220	742C163220JCT
1	RP2	RP2-220	742C163220JCT
6	R2,R8,R12,R16,R19,R20	1k	P1.00KHCT
4	R4, R22, R32, R33	Do not populate	
4	R9,R10,R13,R30	25	P24.9HCT
2	R11,R15	10k	P10.0KHCT
1	R14	50	P49.9HCT
1	R17	1.4k	P1.40KHCT
1	R18	10k	3386W-1-103
2	R21,R24	36	P36GCT
1	R23	Do not populate	

3	R25,R26,R29	40.2k	P40.2KHCT
2	R27,R28	33	P33.2HCT
1	R31	27	P27.4HCT
3	R34,R35,R42	100	P100HCT
1	TP1	VRP	S1011
1	TP2	VRN	S1011
1	TP3	SIG	S1011
1	TP4	VinP	S1011
1	TP5	VinN	S1011
11	TP6,TP7,TP8,TP9,TP10, TP11,TP12,TP13,TP14,TP15 , TP16	TestPoint	S1011
1	T1	ADT1-1WT	ATD1-1WT
1	U1	ADC14L040 or ADC14L020	
1	U2	74VCX86	74VCX86M
1	U5	24C02/SO8	AT24C02AN-10SI-2.7
1	U10	74LVTH162374_1	296-14929-1
1	U14	LMV771/SC70-5	LMV771MGCT
6	U15,U23,U27,U29,U31,U33	LP2988AIM-3.3/SO-8	LP2988AIM-3.3
1	U20	LP2988AIM-5.0/SO-8	LP2988AIM-5.0
1	Y1	OSC	Pletronics SM7745HV-40.0M-Y9 or SM7745HV-20.0M-Y9

APPENDIX

A1.0 Operating in the Computer Mode

The ADC14L040 Evaluation Board is compatible with the WaveVision™ 4.0 Digital Interface Board and WaveVision™ software. You can download the latest version from: <http://www.national.com/appinfo/adc/wv4.html>

When connected to the Digital Interface Board, data capture is easily controlled from a personal computer operating in the Windows environment. The data samples that are captured can be observed on the PC video monitor in the time and frequency domains. The FFT analysis of the captured data yields insight into system noise and distortion sources and estimates of ADC dynamic performance such as SINAD, SNR and THD. See the Digital Interface Board manual for more information.

A2.0 Summary Tables of Test Points, Connectors, and Jumper Settings

A2.1 Test Points

Test Points on the ADC14L040 Evaluation Board

TP 1	Vrp
TP 2	Vrn
TP3	Vin
TP4	Vin+
TP5	Vin-
TP6	Vref
TP7-15	Ground

A2.2 Connectors

P2 Connector - Power Supply Connections

P2-1	+6V	+6V Power Supply
P2-2	GND	Power Supply Ground

A2.3 Jumper settings

Note: Default settings are in **bold**

JP1 - JP4 : Gate Invert

Connect 1-2	Invert clock for latches
1-2 OPEN	Do not invert clock

JP5 : Capture Clock selection

Connect 1-2	Use output from U2 pin 8 as the clock for the capture device
Connect 2-3	Use output from U2 pin 6 as the clock for the capture device

JP6 : Latch Clock selection

Connect 1-2	Use output from U2 pin 3 as the clock for the latch
Connect 2-3	Use output from U2 pin 11 as the clock for the latch

JP7 : VREF selection jumper settings

Connect 1-2	Use external voltage from R18 as reference voltage
Connect 3-4	Use internal 0.5V reference
Connect 7-8	Use internal 1.0V reference

JP8 : Vcm selection

Connect 1-2	Use voltage from resistor divider R19-R20
Connect 2-3	Use common mode voltage from ADC

JP9 : not used**JP10 : Data Format / Duty Cycle Stabilizer**

Connect 1-2	Select Output format of 2's complement, Duty Cycle Stabilizer is OFF
Connect 3-4	Select Output format of Offset Binary, Duty Cycle Stabilizer is ON
Connect 5-6	Select Output format of 2's complement, Duty Cycle Stabilizer is ON
OPEN	Select Output format of Offset Binary, Duty Cycle Stabilizer is OFF

JP11 : Power Down

Connect 1-2	ADC is powered down
1-2 OPEN	ADC is operating

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