Application Report
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Spurs Analysis in the RF Sampling ADC

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ABSTRACT

The RF sampling architecture is the main communication architecture in the telecom industry due to its improved system flexibility, higher signal bandwidth, higher density, and lower cost. This document will briefly introduce the architecture of the RF sampling receiver and the block diagram of the RF analog-to-digital converter (ADC). The goal of this document is to identify spurs generated after the RF sampling, like the harmonic spur and interleaving spur. In addition, the effect of the spurs due to the numerically controlled oscillator (NCO) and decimation are discussed in this document.

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Trademarks

1 Introduction

The RF sampling receiver directly captures signals at RF frequencies and uses an NCO to shift the signal to the baseband or desired IF frequency. The RF sampling receiver eliminates the RF mixer, RF synthesizer, and IF channel filter, when compared with the traditional high-IF sampling receiver. Figure 1 shows the architecture of RF sampling receiver.

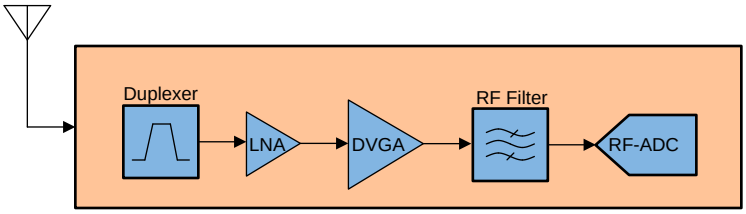

Figure 1. Architecture of RF Sampling Receiver

2 Structure of RF ADC

Figure 2 shows the internal block diagram of the ADC32RF45 RF ADC. The main blocks within the ADC follow[2]:

- Input Buffer: The buffered analog input with on-chip termination provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy.
- Interleaved ADCs: The ADC32RF45 is a dual, 14-bit, 3-GSPS ADC, and each ADC channel is internally interleaved four-times and equipped with analog and digital background, interleaving correction.
- NCOs: The device is equipped with three, independent, complex NCOs per ADC channel. The NCO is 16-bits and allows accurate frequency tuning within the Nyquist zone prior to the digital filtering.
- Decimation Filter: The decimation filter decreases the sample rate by removing samples from the data stream and keeps the data rates reasonable for data transmission.
- JESD Interface: The processed data is passed into the JESD204B interface, where the data is framed, encoded, serialized, and output on one to four lanes per channel, depending on the ADC sampling rate and decimation.

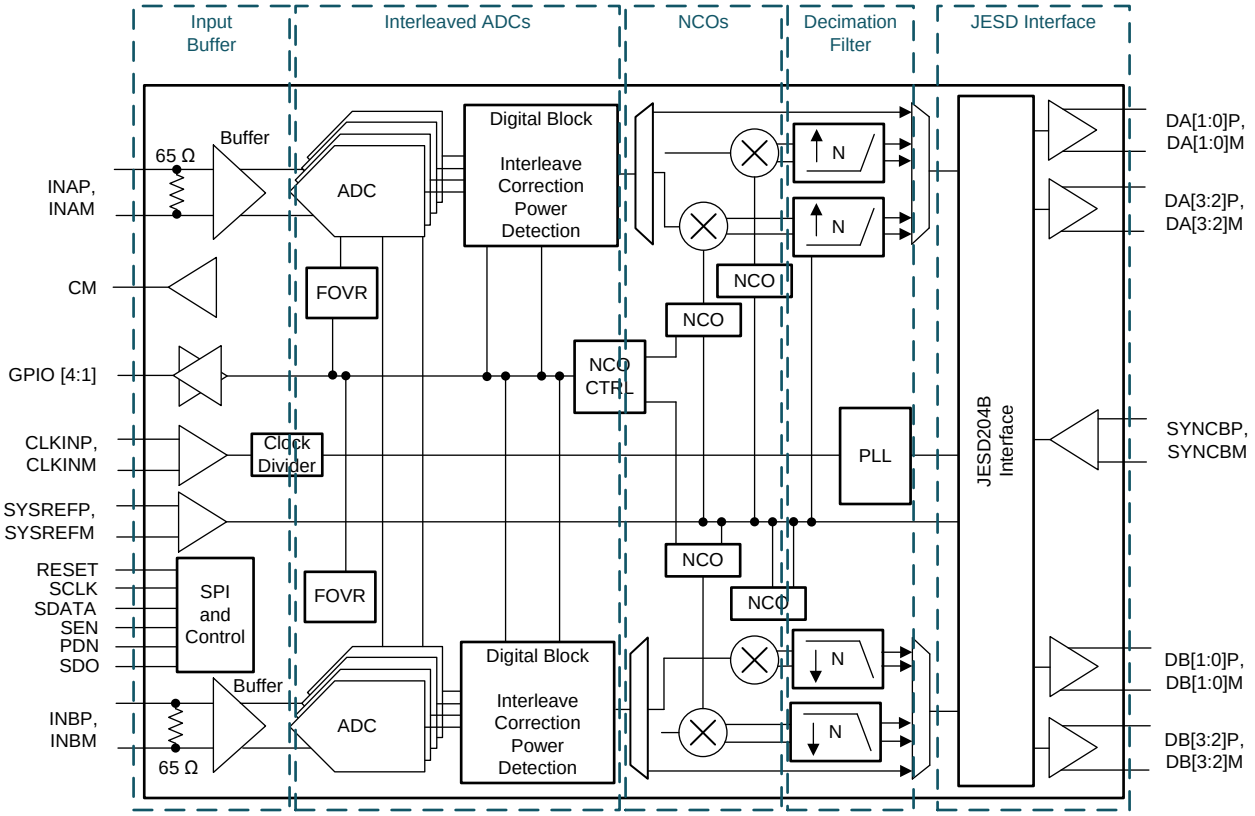

Figure 2. Functional Block Diagram of ADC32RF45

The interleaved ADCs first sample the RF signal; then the NCO shifts the frequency to the desired location. In the end, the sampling data will be transmitted by the JESD interface after passing through the decimation filter. In the sampling process, the non-linear circuits and mismatch of interleaved ADCs generates the harmonic spur and interleaving spurs. In addition, the NCOs and decimation filter change the location of the spurs.

3 Spurs Analysis

3.1 Spur Generation

The spurs are summarized as a harmonic spur or interleaving spur, depending on the cause. The cause of the harmonic spur is the non-linear behavior of the ADC, and the frequency of the spur is an integral multiple of the input signal. In addition, the harmonic distortion has an aliased signal in every Nyquist zone due to the sampling process. Equation 1 shows the nth order harmonic distortion.

$$\pm nFin \pm kFs \tag{1}$$

The variable *n* is the order of the harmonic distortion, and the variable *k* is an integer (k = 0, 1, 2, ...). Fin is the frequency of the input signal, and Fs is the sampling rate of the ADC. Changing the variable *k* locates the aliased harmonic spur in different Nyquist zones. The cause of interleaving spurs is the mismatch of DC offset, gain, and phase between interleaved ADCs. The offset error generates the spurs at the location indicated in Equation 2.

$$\frac{k}{M} \times Fs \tag{2}$$

The gain and phase error introduces the spurs at the location indicated in Equation 3[1].

$$\frac{k}{M} \times Fs \pm Fin \tag{3}$$

M is the number of interleaved ADCs, and k = 0, 1, 2, ... (an integer). Fin is the frequency of the input signal and Fs is the sampling rate of the ADC. In addition, the nonlinear and mismatch error of interleaved ADCs together introduces the spurs in the location indicated in Equation 4.

$$\frac{k}{M} \times Fs \pm HDn \tag{4}$$

HDn is the nth order harmonic spur. Table 1 lists the spurs.

Table 1. Spur Summary

Frequency of Spur	Cause	Feature
$\pm nFin \pm kFs$	Nonlinear parameters of the ADC	When the Fin moves 1 MHz, the spur moves n × MHz.
$\frac{k}{M} \times Fs$	Offset mismatch of interleaved ADCs	The frequency is a fractional multiple of the sampling clock.
$\frac{k}{M} \times Fs \pm Fin$	Gain and phase mismatch of interleaved ADCs	The spurs are symmetrical around the sampling clock.
$\frac{k}{M} \times Fs \pm HDn$	Nonlinear and mismatch of interleaved ADCs	

3.2 Shifting of the Spurs

The RF ADC integrates digital downconverters (DDC) to shift the spectrum in the RF frequency to baseband. The DDC also shifts the spurs. The main functional block of the DDC is the NCO and decimation filter. The NCO shifts the desired frequency and all of the spurs. Then, the data passes through the decimation filter which consists of a decimator and digital low-pass filter. The processing of the decimation filter is equivalent to changing the sampling rate to Fs/m, and passing the data through an analog anti-aliasing filter at fc = Fs/2m, where m = decimation count. As a result, the spurs alias to the first Nyquist zone which ranges from [-Fs/2m, Fs/2m] (complex output), by shifting the frequency of k × Fs/m (k = 0, 1, 2,…).

3.3 Example

To better understand the generation and shifting of the spurs, look at this example. Use the ADC32RF45 to sample an input frequency of 1960 MHz, with a sampling clock of 2949.12 MHz. Each channel of the ADC32RF45 has four interleaved ADCs. The DDC mode with a real input, a complex output, an NCO frequency of 1890 MHz, and 12× decimation filter is used. Table 2 lists the spurs introduced by each functional module. The spurs in Table 2 are calculated using the formulas in Table 1, per the following settings:

- Sampling rata: 2949.12 MHz
- Input frequency: 1960 MHz
- NCO frequency: 1890 MHz
- Decimation factor: 12×

Table 2. Calculation of the Spurs

Spectrum After the Process	Sampling		Shift by NCO		Decimation (12×)	
	Alias	Image	Alias	Image	Alias	Image
Alias of Input	989.12		–900.88		82.16	
Fs/4 + Fin(IL1)	1222.72	1726.4	–667.28	–163.6	70	82.16
Fs/4 – Fin(IL2)	251.84	2697.28	–1638.16	807.28	82.16	70
Fs/2 – Fin(IL3)	485.44	2463.68	–1404.56	573.68	70	82.16
FS/4(IL4)	737.28	2211.84	–1152.72	321.84	76.08	76.08
HD2	970.88	1978.24	–919.12	88.24	63.92	88.24
HD3	18.24	2930.88	–1871.76	1040.88	94.32	57.84
HD4	1007.36	1941.76	–882.64	51.76	100.4	51.76
HD5	952.64	1996.48	–937.36	106.48	45.68	106.48
FS/2 – HD2	503.68	2445.44	–1386.32	555.44	88.24	63.92
FS/4 – HD2	233.6	2715.52	–1656.4	825.52	63.92	88.24
FS/4 + HD2	1240.96	1708.16	–649.04	–181.84	88.24	63.92
FS/2 – HD3	1456.32	1492.8	–433.68	–397.2	57.84	94.32
FS/4 – HD3	755.52	2193.6	–1134.48	303.6	94.32	57.84
FS/4 + HD3	719.04	2230.08	–1170.96	340.08	57.84	94.32

The calculation steps are described as follows:

1. Because the NCO changes the location of the spur, the spurs in the second Nyquist zone fall into the first Nyquist zone after being shifted by the NCO. For every spur in the first Nyquist zone, calculate its image in the second Nyquist zone using Equation 5.

$$F' = Fs - F \quad (5)$$

F is the frequency of the spurs in the first Nyquist zone and F' is their image in the second Nyquist zone. The input signal is in the second Nyquist zone, so Equation 5 is used to calculate its alias. The alias for 1960 MHz, with a sampling rate of 2949.12 MHz, is 989.12 MHz.

2. Use Equation 1 to calculate the harmonic spurs. Take HD2 as an example, the calculation follows:

n = 2 and k = 1, HD2 = 1960 × 2 – 2949.12 = 970.88 MHz (6)

Then, its image is given in Equation 7.

$$2949.12 - 970.88 = 1978.24 \text{ MHz} \quad (7)$$

Then, the same method is used to calculate the harmonic spurs and their images.

3. Use Equation 2 and Equation 3 to calculate the interleaving spurs. Because the number of interleaved ADCs is four, and the spurs are considered in the first Nyquist zone, there are four interleaving spurs:

$$IL1 = \frac{Fs}{4} + Fin$$

$$IL2 = \frac{Fs}{4} - Fin$$

$$IL3 = \frac{Fs}{2} - Fin$$

$$IL4 = \frac{Fs}{4}$$

Because the input signal is in the second Nyquist zone, use the aliased signal in the first Nyquist zone to calculate the interleaving spurs, because the interleaving process is after the sampling process. The interleaving spur is calculated as follows:

$$IL1 = \frac{2949.12}{4} + 989.12 = 1726 \text{ MHz} \qquad \text{alias}: \ \frac{2949.12}{4} - 1726.4 = 1222.72 \text{ MHz}$$

$$IL2 = \frac{2949.12}{4} - 989.12 = -251.84 \text{ MHz}$$

$$IL3 = \frac{2949.12}{2} - 989.12 = 485.44 \text{ MHz}$$

$$IL4 = \frac{2949.12}{4} = 737.28 \text{ MHz}$$

Because the signal is real, if the spurs calculate to the negative frequency domain, it folds back into the first Nyquist zone. If the spurs calculate in the second Nyquist zone, they alias to the first Nyquist zone. The interleaving spurs follow:

- IL1 = 1222.72 MHz
- IL2 = 251.84 MHz
- IL3 = 485.44 MHz
- IL4 = 737.28 MHz

4. Use Equation 4 to calculate the spurs due to the nonlinear and interleaving of the ADC. Take HD2 as an example. There are three spurs, as follows:

$$\frac{Fs}{4} - HD2$$

$$\frac{Fs}{4} + HD2$$

$$\frac{Fs}{2} - HD2$$

The calculation follows (see Equation 8):

$$\frac{2949.12}{4} + 970.88 = 1708.16\ \text{MHz} \quad \text{alias}: 2949.12 - 1708.16 = 1240.96\ \text{MHz}$$

$$\frac{2949.12}{4} - 970.88 = -233.6\ \text{MHz}$$

$$\frac{2949.12}{2} - 970.88 = 503.68\ \text{MHz} \tag{8}$$

5. When the spurs and images are calculated, they are shifted by the NCO and decimation factor. Take the HD2 spur as an example. The HD2 spur is 970.88 MHz and the NCO is 1890 MHz. The result shifts to Equation 9.

$$970.88 - 1980 = -919.12\ \text{MHz} \tag{9}$$

The decimation factor is 12, so the HD2 spur will alias to the first Nyquist zone by shifting the frequency by 4 × 2949.12/12. The final location of the HD2 spur is given in Equation 10.

$$-919.12 + 4 \times \frac{2949.12}{12} = 63.92\ \text{MHz} \tag{10}$$

Figure 3 shows the FFT capture from the ADC32RF45 on the TSW40RF80 transceiver reference design. The spurs calculated from Table 2, close to the fundamental signal, are identified in the FFT plot.

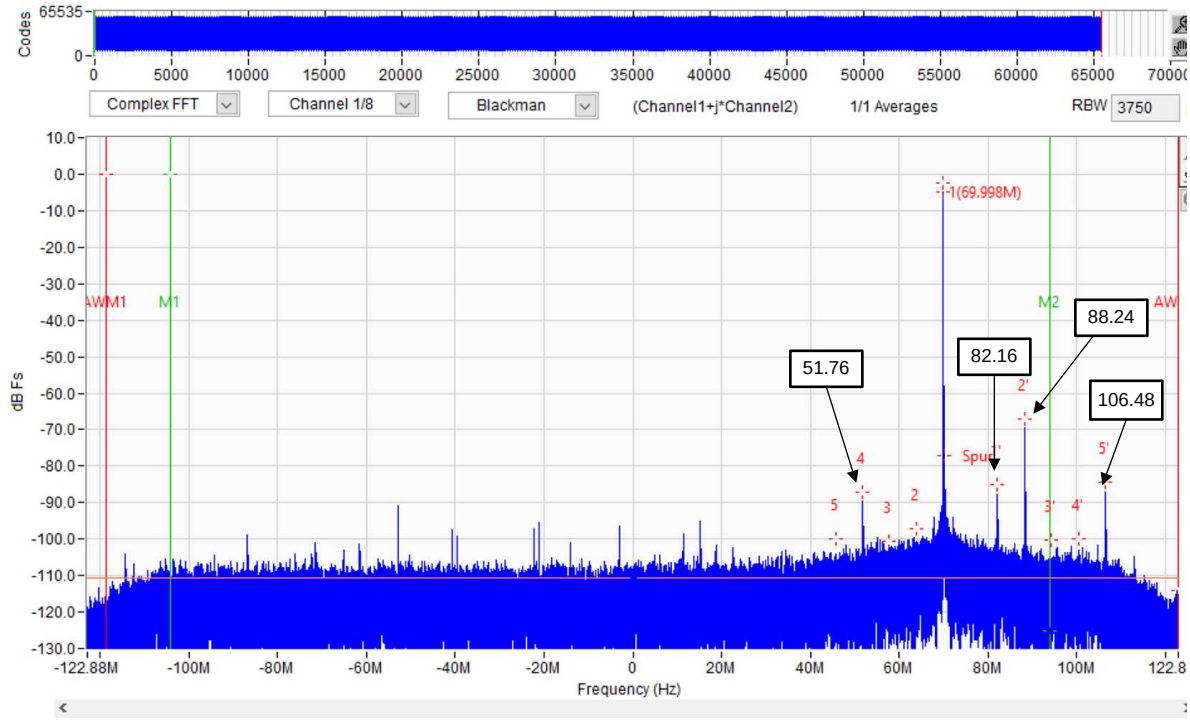

Figure 3. ADC32RF45 FFT Output

The HSDC GUI identifies some spurs according to the value of sampling rate, input signal frequency, NCO frequency, and decimation factor. The n (1, 2, 3, 4, 5) and n' (1', 2', 3', 4', 5') in Figure 3 define the spurs of n-order harmonic spurs and their images after the RF sampling.

4 Conclusion

The spurs degrade the performance of the RF ADC. When the spur locations are known, mitigation techniques like filtering, frequency planning, interleave correction, or differential balance can minimize or eliminate the spurs from degrading the system performance.

5 References

- Manganaro, Gabriele. Advanced Data Converters. Cambridge,UK: Cambridge University Press, 2011.
- Texas Instruments, ADC32RF45 Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter, data sheet
- Texas Instruments, TSW40RF8x Evaluation Module, user's guide

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