Minimum power specifications for high-performance ADC power-supply designs

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Implement an optimized power supply to minimize both cost and PCB area for your ADC.

High-performance analog-to-digital converters (ADCs) are defined as those with a high-frequency clock in conjunction with a high bit-count. There are three main ADC architectures: pipeline, successive approximation (SAR), and delta-sigma. Of these three, pipeline ADCs are the most sensitive to power supply noise because they have the lowest power supply rejection ratio (PSRR). They are followed by SAR ADC converters, with delta-sigma ADCs being the least sensitive to noise on the power supply.

In this paper, we assume that the maximum power supply ripple and thermal noise specifications were already created. The question that remains is, "How do I implement a suitable power supply without overdesigning it while minimizing both cost and occupied printed circuit board (PCB) area?"

Once we define what constitutes a high-performance ADC, we can determine the DC/DC converter parameters that may affect the signal chain performance. I will show how the DC/DC converter's performance/parameters impacts ADC performance, and provide examples of the impact of the loading DC/DC converter effect. With this background in place, we will look at a proposed high-performance power supply architecture solution that addresses system signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) optimizations.

High-performance ADC

To visualize what constitutes a high-performance ADC, let us take a look at **Figure 1**.

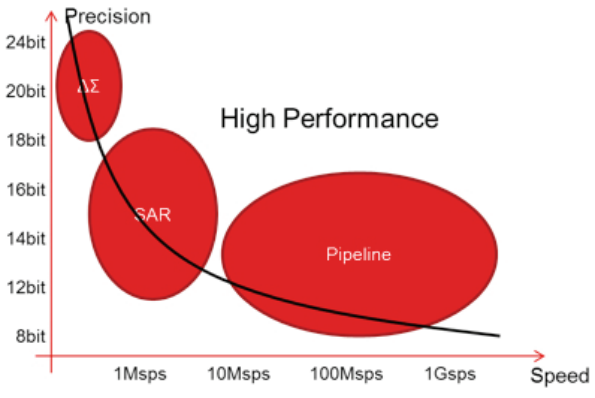


Figure 1 *High-performance ADC definition*

Broadly defined, a high-performance ADC is an ADC with high bit-count and/or high speed. For example, an 8-bit, 25 mega-samples-per-second (MSPS) pipeline ADC is not considered high-performance by most, although it may be sufficient for some applications. Similarly, a low bit-count (12-bit) SAR converter operating at 100 kilo-samples per second (kSPS) is not considered high-performance. On the other hand, a 16-bit or even 18-bit SAR data converter operating at 5 MSPS is considered a high-performance data converter. The line shown in **Figure 1** is arbitrary, but illustrates the combination of both speed and bit-count to be part of the high-performance category, which we will discuss shortly.

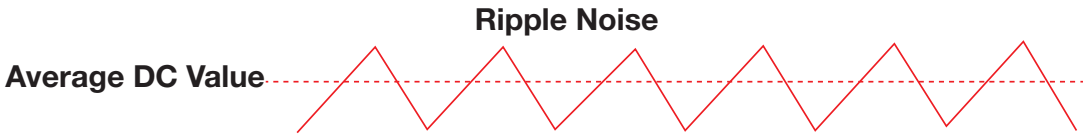


Figure 2. *Ripple noise overview (time domain)*

DC/DC converter noise

The main drawback of using DC/DC converters is their noise contribution. Due to its switching nature, the DC/DC converter has a ripple noise as well as a flicker and wideband thermal noise.

The ripple noise, represented in **Figure 2**, originates from the charging and discharging of the output capacitor around the regulated DC value.

For a high-current DC/DC converter, a ripple noise of 50 mV_{PP} is considered normal. It is possible to optimize the peak-to-peak ripple of a selected DC/DC converter to suit your requirement, but perhaps at the expense of decreased power efficiency or increased board complexity.

In the time domain representation shown in **Figure 2**, the thermal noise is completely ignored because oscilloscopes usually do not have the required resolution to capture it. Looking at the frequency domain in **Figure 3**, it is easy to represent both ripple and thermal noise.

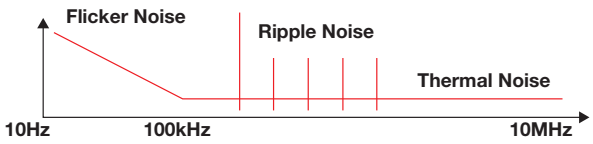


Figure 3. *Noise contributors represented in the frequency domain*

Herein, ripple noise is represented as the fundamental frequency of the ripple and its harmonics. The fundamental frequency of the ripple is located at the switching frequency of the DC/DC converter and, depending on the application, is typically located between a few hundred kilohertz to a few megahertz. The harmonics present are the odd harmonics: three, five, seven and nine.

Spectral noise density, excluding ripple noise, comprises two major components: flicker noise and thermal noise. Flicker noise, or 1/f noise, normally is dominant in the 10 Hz to 100 kHz band. For the convenience of this discussion, I selected this frequency band as it also appears in all TI low-noise low-dropout regulators (LDOs). To be technically correct, flicker noise depends on the process employed and has a corner frequency in the region of 100 Hz to tens of kHz. For a DC/DC converter, flicker noise generally is in the region of 1 to 2 mV_{RMS} for the 10 Hz to 100 kHz band.

Thermal noise corresponds to the LDO's wideband noise and typically is limited to 10 MHz, as the frequency response of the LDO rolls off and is defined here as starting from 100 kHz. A rule of thumb is that the thermal noise is 3.5 times that of the flicker noise. This is a rough approximation developed using low-noise, wideband LDOs. Total noise is calculated by taking the root mean square (RMS) of flicker and thermal noise.

Knowing the issues that the DC/DC converter can generate is only half the battle. To create a reliable power supply design, we need to know how the load, or ADC, will react to variation in its power supply. This information is normally found in the ADC's PSRR plots.

DC/DC ripple noise

In order to create a PSRR plot, we induce a known sine wave into the ADC's power supply and look at how the additional tone is impacting the fast Fourier transform (FFT). Using the ADC3444, which is a quad-channel, 14-bit, 125 MSPS ADC, the location of the power supply disturbance and how it interacts with the ADC's clock is shown in **Figure 4**. Essentially, for the analog voltage supply (AVDD), we find the 500 kHz disturbance at 500 kHz, as well as 500 kHz spurs on either side of the tone signal. On the digital voltage supply (DVDD), the disturbance is only at 500 kHz. This brings us to the following points for this ADC:

- The AVDD supply is more sensitive to signal originating in the power supply than the DVDD supply.
- A disturbance enters into the signal path through the AVDD supply by two modes of entry.
- A disturbance enters the signal path of the DVDD supply by only one mode of entry.

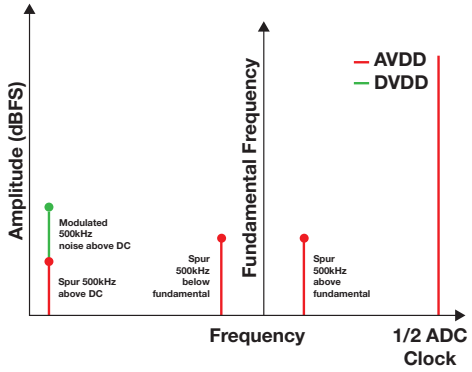


Figure 4. Power supply single-tone impact to the ADC signal path

For this discussion I specified the ADC3444 ADC since other ADCs may react differently. For example, the ADC34J45 has two modes of entry into the signal path for all three of its supplies (AVDD, DVDD and IOVDD). Knowing the PSRR for the specific ADC you are using is critical. The PSRR for the ADC3444 for both DVDD and AVDD is shown in **Figure 5**. From this point forward, this discussion assumes that by ADC we mean the ADC3444.

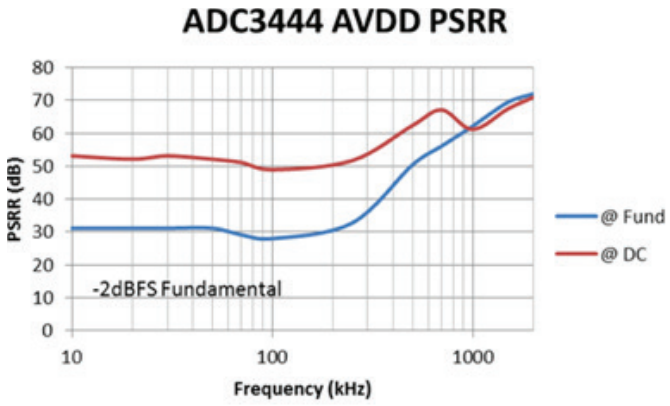


Figure 5. ADC PSRR for various power supply disturber frequency

To define the ADC PSRR completely, we need to take into consideration all parameters affecting the signal tone. We can envision PSRR versus ripple frequency, or versus signal-tone frequency, or even signal-tone amplitude. This is shown in **Figures 6-8**.

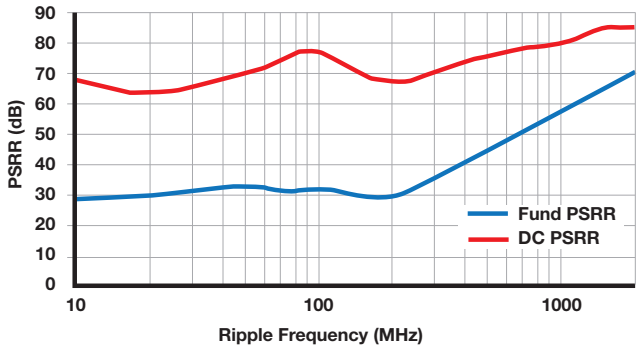


Figure 6. ADC PSRR vs. ripple frequency

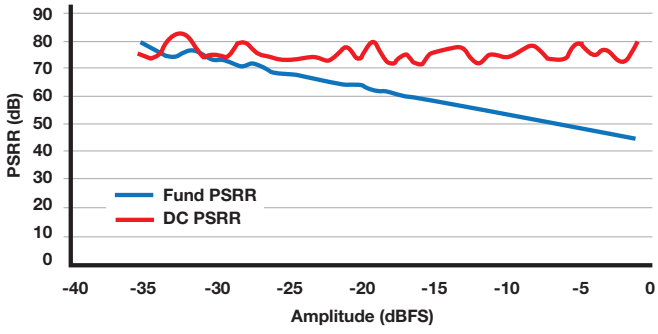


Figure 7. ADC PSRR vs. signal tone frequency

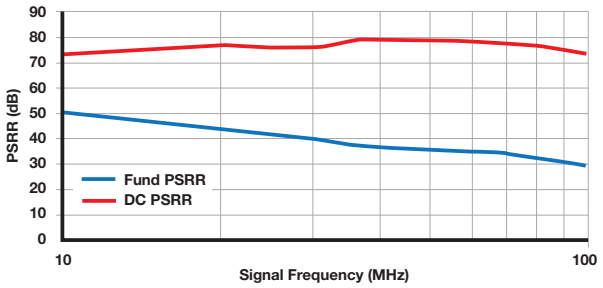


Figure 8. *ADC PSRR vs. signal tone amplitude*

All the PSRR plots versus frequency, signal tone amplitude, signal tone frequency, and so on, provide us with enough information to analyze ADC performance and predict the behavior of the power supply we will design later on.

Loading the DC/DC converter

Now that we understand which ADC parameters are affected, let us turn our attention to the effect of loading the DC/DC converter and how this impacts ADC performance. The goal here is to design a simple power supply that will not impact signal chain performance over process variations and temperature. For our purposes these errors will be considered as a whole in the PSRR margin term.

To compare the performance of any developed power supply solution, we generate a FFT from a "golden" power supply, which is created by combining a battery for the supply, followed by very low-noise LDOs to isolate AVDD from DVDD. In this reference FFT, all power supplies are linear, so there is no external disturbance. The reference power supply is constituted of a 6-V battery followed by two 4-µVRMS high-PSRR voltage regulators (TPS7A4700), each with a ferrite bead on its output forming a Pi-filter with the ADC's local bypass capacitors. We use one LDO for the AVDD and the other LDO for the DVDD supply. Using the lowest-noise configuration ensures there is no crosstalk between the AVDD and DVDD rails. Going forward, we will refer to the battery plus the TPS7A4700 solution as the reference power supply.

A comparison between this reference FFT and a switching solution using the TPS54320 DC/DC converter is shown in **Figure 9**, or the DC/DC. In this plot the reference power is linear to ensure that the only switching present takes place in the ADC.

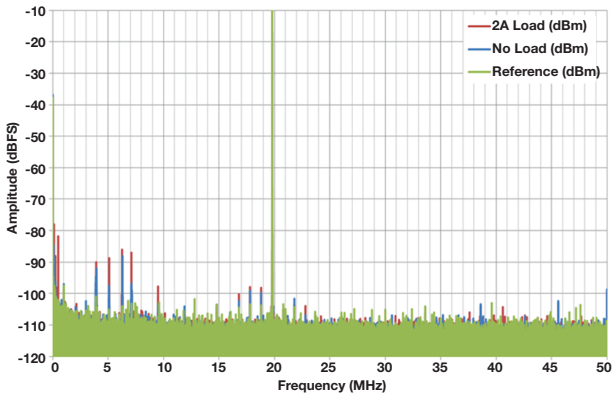


Figure 9. *Comparison between a reference plot and a DC/DC solution*

Similar to the reference power-supply solution, the DC/DC is followed by a ferrite bead on its output forming a Pi-filter with the local bypass capacitors. The Pi-filter has a resultant 36-kHz bandwidth minimizing the ripple noise of the DC/DC. The Pi-filter's 0 dB DC attenuation results in some of the DC/DC ripple and flicker noise feeding into the signal path (**Figure 10)**. The 500-kHz switching frequency is also present when 2 A additional current is drawn from the DC/DC.

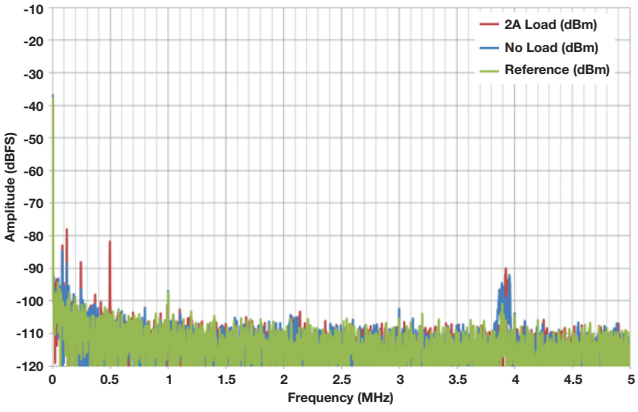
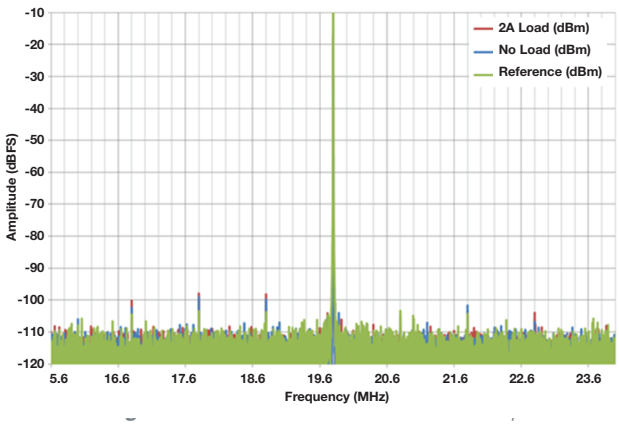


Figure 10. *DC to 5 MHz FFT close-up*



Looking closely at what is happening around the signal tone (**Figure 11**), the DC/DC converter's 500 kHz switching frequency is not showing up, but ADC spurs are amplified with each spur's energy spectrum spread over a wider band.

Although this solution may be sufficient for some applications, it also depends on the typical PSRR of the ADC and may not satisfy all requirements. Designing a solution that will work both over process and temperature variations requires that we introduce some margin into the design.

Figure 12 contains a block diagram used to generate the results shown in **Figure 9 – 11**.

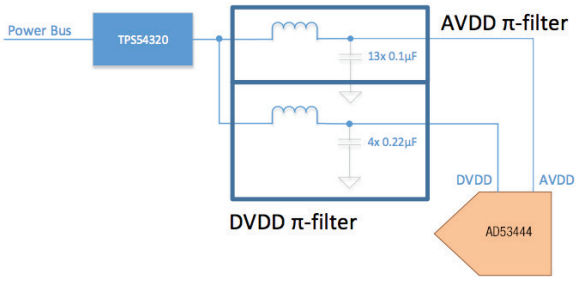


Figure 12. Tested solution

Improved power supply architecture

Description

To improve the system's overall performance, consider the following architecture where an LDO is added after the DC/DC converter. Ferrite beads are maintained on the LDO's output. The ferrite beads help to provide supply-to-supply isolation as both the ADC supply voltages are 1.8 V.

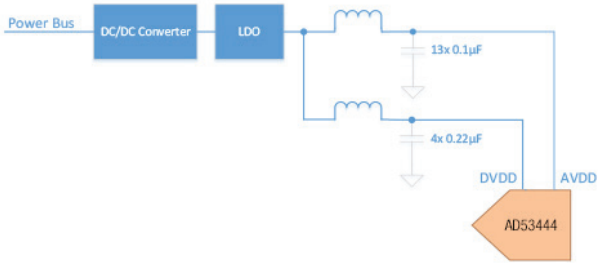


Figure 13. Improved power supply architecture

Implementation

The complete block diagram for the evaluation is shown in **Figure 14**.

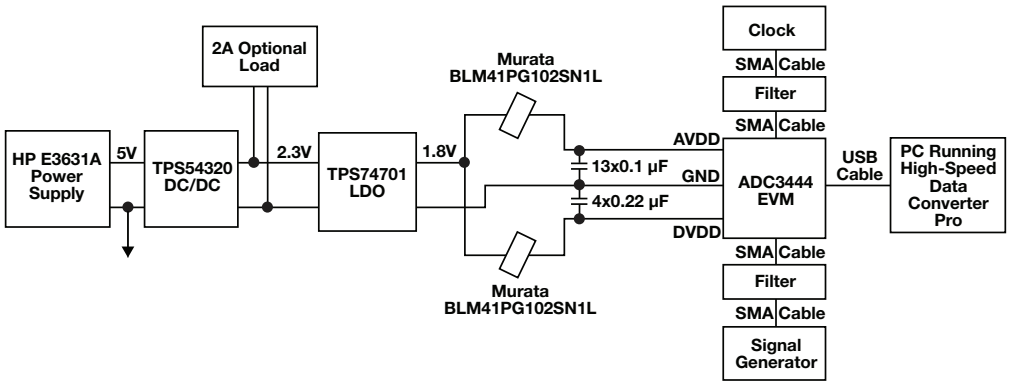


Figure 14. Evaluation system block diagram

In this block diagram, the power chain from the lab power supply to the ADC evaluation module (EVM). The DC/DC converter is powered from the lab supply and has an optional load connected to its output. The TPS74701, a programmable soft-start LDO, is selected for its output current and relatively low output noise. The LDO is operated from a 2.3-V supply and delivers the required 1.8-V supply. This configuration provides both a high PSRR to the load and a decent power efficiency of 78.2 percent. The ferrite beads are added to provide supply-to-supply isolation and form a Pi-filter with the distributed capacitors present on each of the ADC's supply pins.

The overall performance (**Figure 15**) is a remarkable improvement over the DC/DC alone and is now almost undistinguishable from the reference

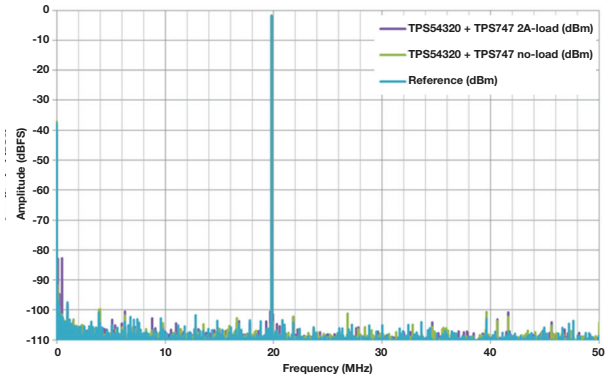


Figure 15. *Comparison between reference supply and proposed solution*

The only degradation at this level is the presence of a spur at 500 kHz when the DC/DC is loaded with the additional 2A load. The only thing left for us to do now is to analyze the performance to see where improvements can be made and then optimize the circuit for maximum efficiency.

Ripple performance analysis

We start by looking at the DC/DC ripple in the frequency domain (**Figure 13**). This approach has the advantage of being directly translatable into a table to easily compare the amplitude versus

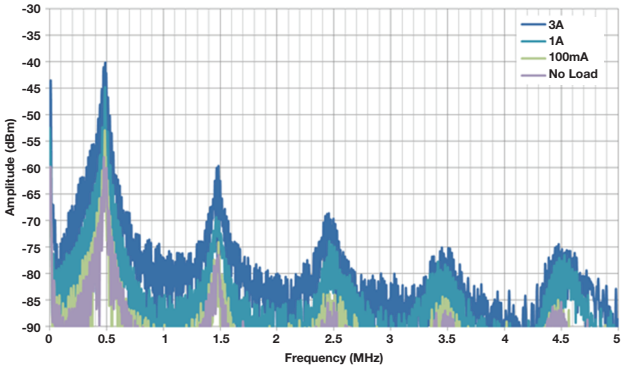


Figure 16. *Step-down buck converter ripple in frequency domain*

Table 1 shows the fundamental switching frequency for the step-down buck converter, as well as the third, fifth, seventh and ninth harmonic for both no-load and with an additional 2A-load.

Freq. (MHz)	No-load amplitude (dBm)	2-A load amplitude (dBm)
0.4	–58	–38
1.2	–77	–59
2.0	–85	–68
2.8	–87	–75
3.6	–85	–73

Table 1. *SStep-down buck converter no-load and 2-A load switching-frequency fundamental and harmonics amplitudes*

Table 1 shows the fundamental switching frequency of the step-down buck converter, as well as the third, fifth, seventh and ninth harmonic for both no-load condition, and with an additional 2-A load.

Figures 17, 18 and 19 show the LDO PSRR, Pi-

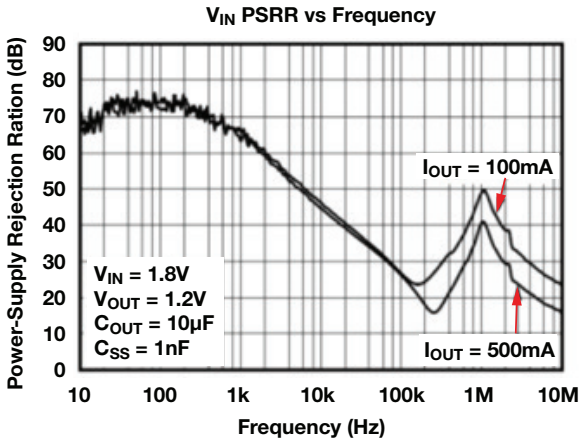


Figure 17. LDO PSRR

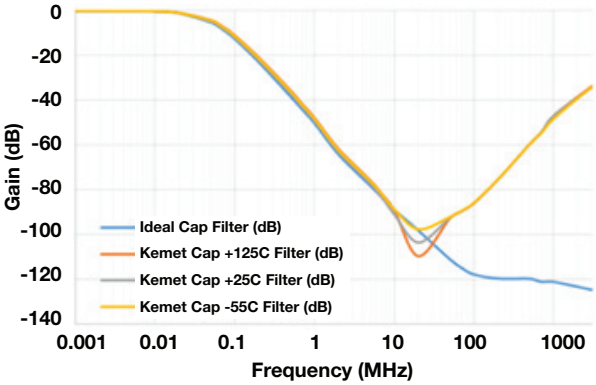


Figure 18. Pi-filter attenuation

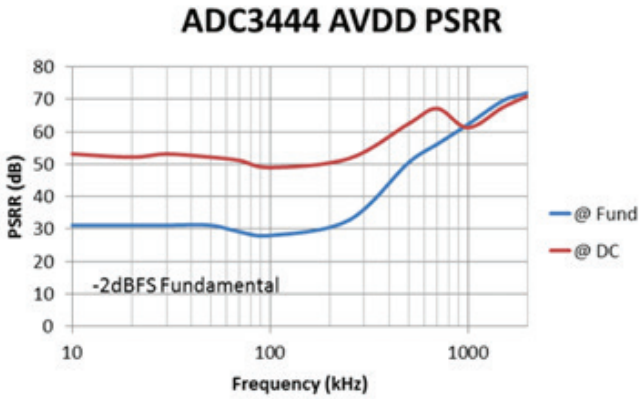


Figure 19. ADC PSRR

Freq. (MHz)	PSRR (dB)
0.5	38
1.5	45
2.5	38
3.5	30
4.5	27

Freq. (MHz)	2-A load Amp. (dB)
0.5	32
1.5	55
2.5	64
3.5	70
4.5	74

Freq. (MHz)	2-A load Amp. (dB)
0.5	45
1.5	60
2.5	
3.5	
4.5	

At DC/DC converter's output		At LDO output		At π-filter's output		Expected contributions to spurs in FFT	
Freq. (MHz)	2-A load Amp. (dBm	Freq. (MHz)	2-A load Amp. (dBm)	Freq. (MHz)	2-A load Amp. (dBm	Freq. (MHz)	2-A load Amp. (dBm)
0.4	–38	0.4	–76	0.4	–108	0.4	–153
1.2	–59	1.2	–104	1.2	–159	1.2	–219
2.0	–68	2.0	–106	2.0	–170	2.0	
2.8	–75	2.8	–105	2.8	–175	2.8	
3.6	–73	3.6	–100	3.6	–174	3.6	

Table 2. Ripple attenuation through the different stages

With this in place, we can look at the attenuation of the DC/DC converter ripple and see its impact on the ADC performance (**Table 2**).

The expected contribution to the FFT is negligible. In this case, the Pi-filter almost seems redundant for the system's overall performance. Remember that the Pi-filter used here is to isolate the AVDD from the DVDD, and not just for its attenuation characteristics.

Noise performance analysis

Looking at the noise contribution of each stage, we start with the step-down buck converter thermal noise, composed of both flicker and wideband noise (**Figure 20**). Flicker noise is found predominantly below 10 kHz and only the flat-band noise is present after that. Integrating the noise between 10 Hz and 100 kHz gives us a RMS noise for the DC/DC converter of 1 μV_{RMS}.

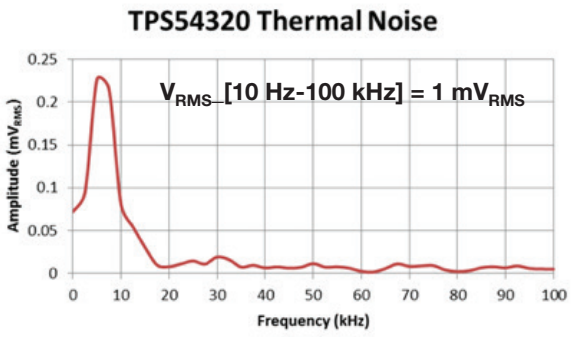


Figure 20. Step-down buck converter thermal noise

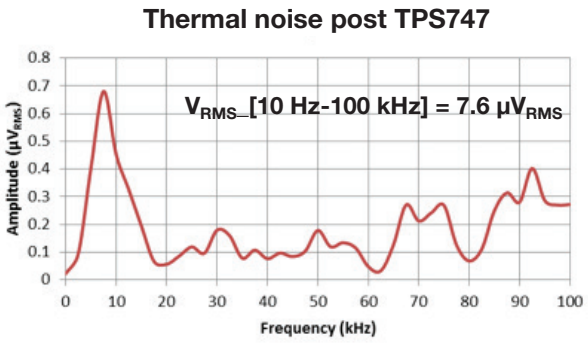


Figure 21. Step-down buck converter post-LDO noise

Calculating the same integration bandwidth, 10 Hz to 100 kHz, but accounting for the LDO PSRR gives us 7.6 μV_{RMS} as the DC/DC converter noise contribution. The 10 Hz-to-100 kHz noise has been attenuated from 1 mV_{RMS} (**Figure 20**) to 7.6 μV_{RMS} (**Figure 21**). Note that the Pi-filter with its –3-dB bandwidth of 36 kHz does not attenuate significantly the DC/DC flicker and thermal noise. After the LDO, only the ADC PSRR is left to reduce the thermal noise contribution to the system's SNR.

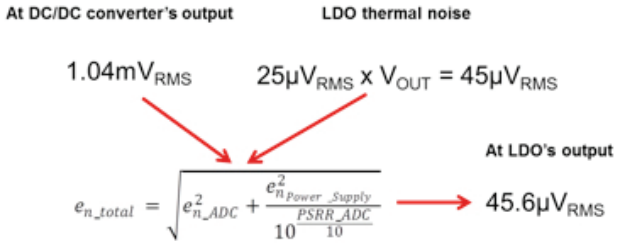


Figure 22. Combining DC/DC with LDO thermal noise

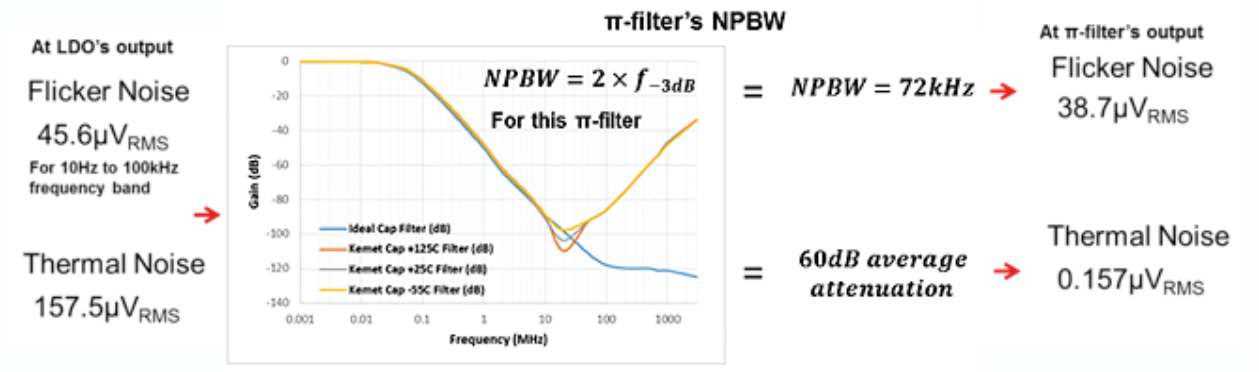


Figure 23. Noise contribution to ADC supply pins

Combining the step-down buck converter thermal noise with the LDO noise contribution of 45 μV_{RMS} (**Figure 22**), the overall noise is 45.6 μV_{RMS} – or a degradation of only 0.6 μV_{RMS}. The LDO has eliminated almost the DC/DC noise contribution from the system. The calculation for each respective component is shown in **Figure 22**.

Moving to LDO noise and separating flicker noise from wideband noise, we see that the Pi-filter plays an important role of further attenuating the noise. In particular it completely eliminates the LDO's wideband noise from the calculation (**Figure 23**).

This leaves a total noise contribution of 38.7 μVRMS to the ADC supply pin. **Table 3** contains the calculation of each power-supply contribution to the system SNR and applies the typical ADC PSRR.

Power supply noise	Noise (μV_{RMS})	PSRR (dB)	Noise (nV/vHz)	Combined SNR (dBFS)
ADC component			23.9	72.4
AVOD DC component	38.2	50	0.4	72.4
AVDD fund component	2x 38.2	28	9.6	71.8
DVDD DC component	38.2	75	0	72.4
Total			25.8	71.8

Table 3. SNR degradation due to each power supply contribution

Interestingly, the AVDD's second mode of entry appears to be the dominant term for the SNR degradation. If we use separate LDOs for the AVDD and DVDD supply to eliminate the ferrite bead, we would see a 66.5 dB total SNR. So the Pi-filter is critical as it further attenuates the noise coming from the power chain.

Since these PSRR numbers are typical, using a guard-band helps us to determine how much we can expect the system SNR to degrade over temperature and component variations.

Improving the power chain

Now that we have identified the additional margin on this power supply implementation, we can decrease V_{IN} and operate closer to V_{OUT}. This scenario degrades the LDO's PSRR, but not so much as to eliminate its main benefit of greatly reducing the DC/DC converter's flicker noise. Doing this achieves 90 percent efficiency on the LDO (V_{IN} = 2 V to V_{OUT} = 1.8 V).

The output signal of the LDO (TPS74701) is a very low dropout regulator that requires a maximum of 120 mV at 500 mA over temperature. If the overall noise performance of the LDO is not sufficient,

reducing the Pi-filter bandwidth on the AVDD pin can also reduce the main power supply noise source. This can easily be achieved by adding an additional capacitor. If this solution is not satisfactory from the perspective of PCB area, using a lower noise LDO may be required. TI has several LDO devices that may fit these needs. For example, the TPS73618 could reduce the output LDO noise to 15 μV_{RMS} or less. For even better performance (3.8 μV_{RMS}), increased power density and completely independent supplies, the dual 1A LDO TPS7A88 is available.

Conclusion

By taking into consideration both ADC and DC/DC converter performance, we have developed a minimum ADC power supply and provided the analytical means for optimizing it to your desired specificationsReferences.

References

- Download these datasheets: ADC3444, ADC34J45, TPS54320, TPS73618, TPS7A4700, TPS74701, TPS7A88.
- Overview for Linear Regulators (LDO).
- Support and training for Linear Regulators (LDO).
- A topical index of TI LDO application notes.

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