Application Note

Understanding the Differences Between the ADS114S06 and ADS114S08 Standard and Cost-Optimized Versions

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ABSTRACT

This document describes the differences between the standard and cost-optimized versions of the ADS114S06 and ADS114S08 (ADS114S0x) devices. Texas Instruments provides cost-optimized, *B-grade* versions of each device for systems that may not require the performance level and feature set offered by the standard devices. Table 1-1 lists the standard versus B-grade devices.

This application note also describes how the differences apply to the ADS114S08 evaluation module (EVM) because there is no dedicated EVM for the B-grade versions.

Table 1-1. Standard Versus B-Grade Devices

Standard Device	B-Grade Device
ADS114S06	ADS114S06B
ADS114S08	ADS114S08B

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Trademarks

1 Introduction

The 6-channel ADS114S06 and 12-channel ADS114S08 are 16-bit, 4000 sample-per-second (SPS), delta-sigma analog-to-digital converters (ADCs). These devices offer an integrated analog front-end that consists of:

- A fully-flexible input multiplexer
- Dual excitation current sources (IDACs)
- A low-noise programmable gain amplifier (PGA)
- A low-drift 2.5-V voltage reference with buffered reference output
- A temperature sensor
- A precision oscillator
- Multiple monitoring and diagnostic features

The ADC performance and feature set make these devices an excellent choice for all types of precision sensor measurements in end-equipment such as:

- Pressure transmitters
- Temperature controllers
- Temperature transmitters
- PLC analog input modules

Figure 1-1 illustrates the functional block diagram for these two ADCs.

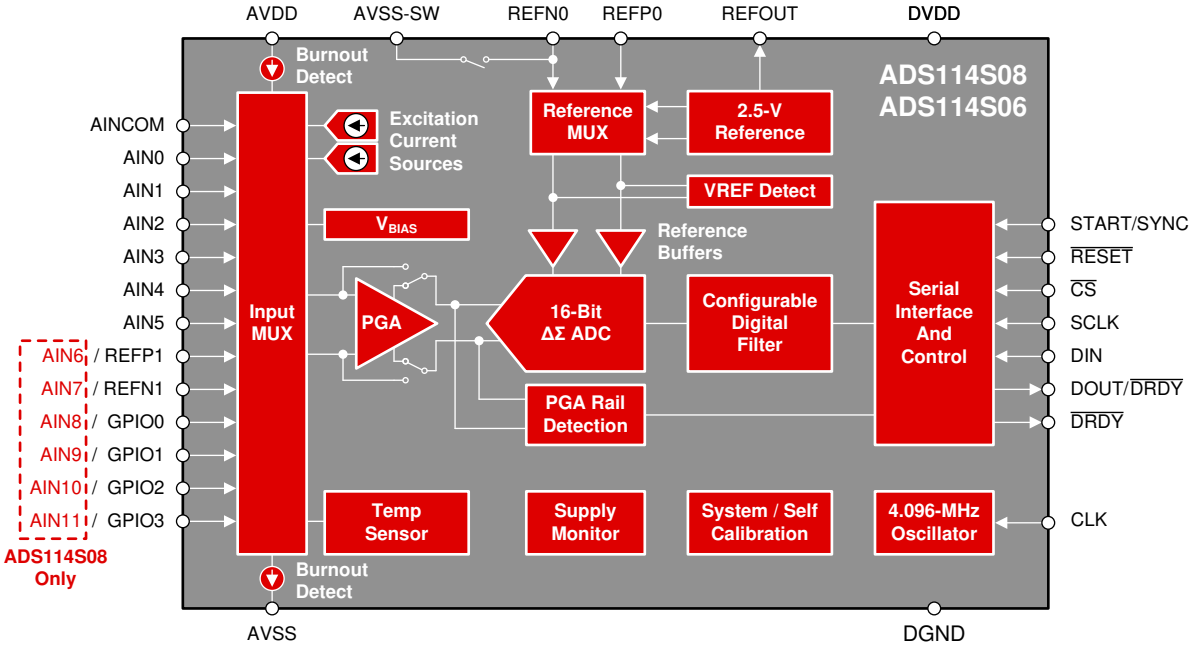

Figure 1-1. Functional Block Diagram

The differences between the standard and B-grade versions are separated into three different categories:

- Performance
- Features
- Specifications

These categories are discussed in detail in the following sections.

2 Performance

The ADS114S06B and ADS114S08B have some relaxed specifications to help optimize cost and enable use in end-equipment that does not require the performance of the standard-grade ADCs. Table 2-1 summarizes these relaxed specifications and compares their values to the standard-grade devices.

Table 2-1. Performance Differences Between the ADS114S0x and ADS114S0xB

PARAMETER	TEST CONDITIONS	ADS114S06 ADS114S08			ADS114S06B ADS114S08B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating ambient temperature		–50		125	–40		125	°C
Absolute input current	PGA enabled, all gains		0.1	±2		0.1	±10	nA
INL (best fit)	PGA bypassed, V_{CM} = AVDD / 2		1	10		1		ppm_{FSR}
	PGA enabled, gain = 1 to 8, V_{CM} = AVDD / 2		2	15		2	25	ppm_{FSR}
	PGA enabled, gain = 16 to 128, V_{CM} = AVDD / 2		3	15		2	25	ppm_{FSR}
Gain error	T_A = 25°C, PGA bypassed		0.004%	0.012%		0.01%	0.1%	
	T_A = 25°C, PGA enabled, gain = 1 to 32		0.004%	0.012%		0.025%	0.2%	
	T_A = 25°C, PGA enabled, gain = 64 and 128		0.004%	0.02%		0.025%	0.2%	
V_{REF} accuracy	T_A = 25°C, TQFP package	–0.05%	±0.01%	0.05%	–0.2%	±0.01%	0.2%	
	T_A = 25°C, QFN package	–0.1%	±0.01%	0.1%	–0.2%	±0.01%	0.2%	
V_{REF} temperature drift	T_A = –40°C to +85°C		2.5	8		8	40	ppm/°C
	T_A = –50°C to +125°C		3	10		N/A		ppm/°C
IDAC accuracy (each IDAC)	T_A = 25°C, 10 µA to 100 µA	–5%	±0.7%	5%	–6%	±1%	6%	
	T_A = 25°C, 250 µA to 2 mA	–3%	±0.5%	3%	–6%	±1%	6%	
IDAC current mismatch	T_A = 25°C, 10 µA to 100 µA		0.15%	0.8%		0.20%		
	T_A = 25°C, 250 µA to 750 µA		0.1%	0.6%		0.20%		
	T_A = 25°C, 1 mA to 2 mA		0.07%	0.4%		0.20%		
IDAC temperature drift	10 µA to 750 µA		20	120		100		ppm/°C
	1 mA to 2 mA		10	80		100		ppm/°C
IDAC temperature drift matching	10 µA to 100 µA		3	25		10		ppm/°C
	250 µA to 2 mA		2	15		10		ppm/°C
Oscillator accuracy		–1.5%		1.5%	–2%		2%	
Device cost		ADS114S06			ADS114S06B			USD ($)
		ADS114S08			ADS114S08B			USD ($)

3 Features

Several features that are available in the standard-grade devices are removed from the B-grade devices. Table 3-1 summarizes these features as well as their intended purpose in the standard-grade devices.

Table 3-1. Features Available Only in Standard-Grade Devices

Feature	Purpose
SINC3 Filter	Reduces ADC noise compared to low-latency filter, while increasing settling time
Low-Side Power Switch	Power-down path for resistive bridges to reduce power consumption between conversions
Global Chop	Averages two readings to reduce offset, offset drift, and noise
PGA Rail Detection	Detects if the PGA is operating outside the linear region of operation
Reference Detection(1)	Detects if the differential reference voltage drops below 1/3 × (AVDD – AVSS) V
Cyclic Redundancy Check (CRC)	Detects single-bit or multibit data-transmission errors
Programmable Conversion Delay	User-defined programmable delay time to compensate for external analog circuitry settling time when multiplexing through channels

(1) A 300-mV reference detection threshold is available on both the standard and B-grade versions of the ADS114S0x

4 Specifications

In addition to removing several features, the ADS114S06B and ADS114S08B datasheets remove several specifications that are included in the standard device datasheets. These specifications are generally unnecessary in more cost-sensitive applications that require a balance between performance and value. Table 4-1 summarizes the specifications removed from the B-grade devices.

Table 4-1. Specifications Removed From B-Grade Devices

Change	Specification
Minimum and maximum values removed	Differential input current
	Input offset voltage
	Offset drift
	VREF absolute input current
Minimum values removed	CMRR
	PSRR
Maximum values removed	Gain drift
	Analog supply current
	Digital supply current
Values not specified	Absolute input current drift
	Differential input current drift

5 EVM Differences

While there is no B-grade-specific EVM for the ADS114S06B or ADS114S08B, the behavior of these devices can be mimicked using the standard-grade ADS114S08EVM. Table 5-1 identifies the bit values within each field and register that must be set so that the ADS114S08EVM behaves as if a B-grade device is installed. However, please note that the EVM performance is not relaxed as per Table 2-1 and Table 4-1.

Table 5-1. Register Settings to Mimic ADS114S0xB Behavior on the ADS114S08EVM

Address	Register	Field	Bit No.	Bit Value
03h	PGA	DELAY[2:0]	7	0
			6	0
			5	0
04h	DATARATE	G_CHOP	7	0
		FILTER	4	1
05h	REF	FL_REF_EN[1:0]	7	0
			6	0 or 1
06h	IDACMAG	FL_RAIL_EN	7	0
		PSW	6	0
08h	VBIAS	VB_LEVEL	7	0
09h	SYS	CRC	1	0
		SENDSTAT	0	0

6 Alternative Device Recommendations

In addition to the 16-bit ADS114S06 and ADS114S08, Texas Instruments also offers the pin-to-pin compatible, 24-bit devices shown in Table 6-1. These ADCs include the same feature set and performance as their 16-bit counterparts, but with 24-bit resolution.

Table 6-1. Pin-Compatible, 24-Bit Versions of the ADS114S06 and ADS114S08

Device	Description
ADS124S06	24-bit, pin-to-pin compatible with the ADS114S06
ADS124S08	24-bit, pin-to-pin compatible with the ADS114S08

7 Conclusion

Many types of sensor measurement end-equipment often require the high-performance and extensive feature set of the 16-bit, 6-channel ADS114S06 and 12-channel ADS114S08. However, for more cost-sensitive applications, Texas Instruments offers pin-compatible, B-grade versions of these devices (the ADS114S06B and ADS114S08B) that offer an excellent combination of performance and cost.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2018) to Revision A (June 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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