Application Report
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ADS1258, ADS1258-EP, and ADS1158 SPI™ Timeout Function

Mark Berarducci *High-Performance Analog*

ABSTRACT

This application report describes the SPI timeout function of the ADS1258, ADS1258-EP, and ADS1158. The goal of this application report is to describe the SPI timeout function and operation.

1 SPI Timeout Function

The ADS1258, ADS1258-EP and ADS1158 are 24-bit (ADS1258 and ADS1258-EP) and 16-bit (ADS1158) precision analog-to-digital converters (ADCs) with sample rates up to 128 kSPS. The ADCs incorporate an SPI port that is used to both configure the ADC and to read conversion data. The SPI port consists of four signals: $\overline{CS}$, DIN, DOUT, and SCLK. $\overline{CS}$ selects the ADC for communication, DIN sends data to the ADC, DOUT reads data from the ADC, and SCLK shifts data in to and out of the ADC.

When $\overline{CS}$ is low, the ADC SPI port is active for communication. Data are transferred to and from the ADC by shifting data in on DIN and shifting data out on DOUT, which is controlled by clocking SCLK shift pulses. The SCLK shift pulses must be precisely controlled for proper SPI port operation.

In the event an unintended SCLK pulse should occur, SPI synchronization between an external controller and the ADC could be lost, in which case the ADC may exhibit no or erratic response. In this event, SPI synchronization can be restored by the following means:

- Toggle the ADC $\overline{CS}$ pin high and then back low to start a new communication
- Toggle the ADC RESET pin low then back high to reset the ADC
- Cycle power to the ADC
- Automatic reset of the SPI timeout function

The SPI timeout function automatically recovers the SPI interface. This recovery is accomplished by holding SCLK inactive (high or low) for 4096 or 256 f_{CLK} cycles (programmable). After 4096 or 256 f_{CLK} cycles of SCLK inactivity occur, the SPI port resets and is ready for new communication.

To ensure the timeout function does not affect normal SPI communications, care must be taken to avoid starting a new communication or continue on with the communication when the SPI timeout resets.

2 SPI Timeout Operation

When $\overline{CS}$ is taken low, or after detecting an SCLK transition (low-to-high or high-to-low), the SPI timer resets to the timeout value and then begins to time down. If no SCLK transition is detected during the time-down period, the timer expires and results in an SPI port reset. After an SPI reset, the SPI timer does not arm again until $\overline{CS}$ is taken high and then low or until the next SCLK transition is detected. During the time-down period, an SCLK transition causes the timer to reset again and the time-down period restarts. Figure 1 illustrates the timeout operation. The time-down tolerance is ±2 f_{CLK} cycles for the reset process to complete before the port is available for the next transaction.

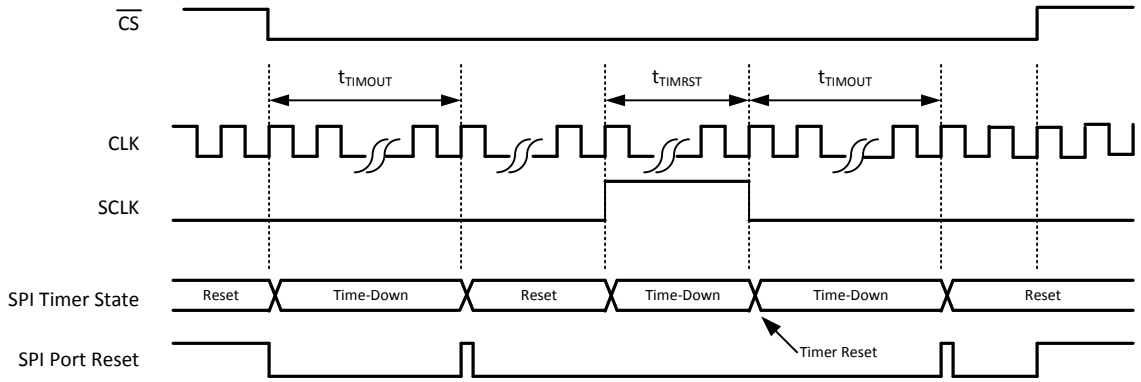

Figure 1. SPI Timeout Diagram

Table 1. SPI Timing Characteristics for Figure 1

PARAMETER		MIN	MAX	UNIT
t_{TIMOUT}	Time to SPI timeout	4096 (256) – 2	4096 (256) + 2	$1/f_{CLK}$
t_{TIMRST}	Time for no SPI timeout		4096 (256) – 2	$1/f_{CLK}$

It is important to avoid the SPI timer timeout during on-going or newly-started SPI transactions. Otherwise, unpredictable operation could result. SPI transaction interference with an SPI timeout can be avoided by keeping the SPI timer continuously reset by ensuring the time between the $\overline{CS}$ falling edge and the first SCLK transition and the time between subsequent SCLK transitions is less than the SPI timer value. Alternatively, the time between SPI transactions can be controlled in such a way to intentionally allow the SPI timeout to occur only during SPI inactivity. Once the SPI timeout occurs, the next SPI transaction can be started any time afterwards.

Toggling $\overline{CS}$ between each SPI transaction resets the SPI timer to a known and predictable starting value. Using $\overline{CS}$ for each SPI transaction reduces the external requirement to keeping the maximum time between $\overline{CS}$ low to the first SCLK transition, and for subsequent SCLK transitions, less than 4096 (256) – 2 f_{CLK} cycles to avoid an SPI timeout.

3 Conclusion

It is important to avoid starting ADC SPI transactions at the same time that an ADC SPI timeout occurs. This conflict can be avoided by controlling the timing of SPI transactions that can be made easier by toggling $\overline{CS}$ for each SPI transaction.

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