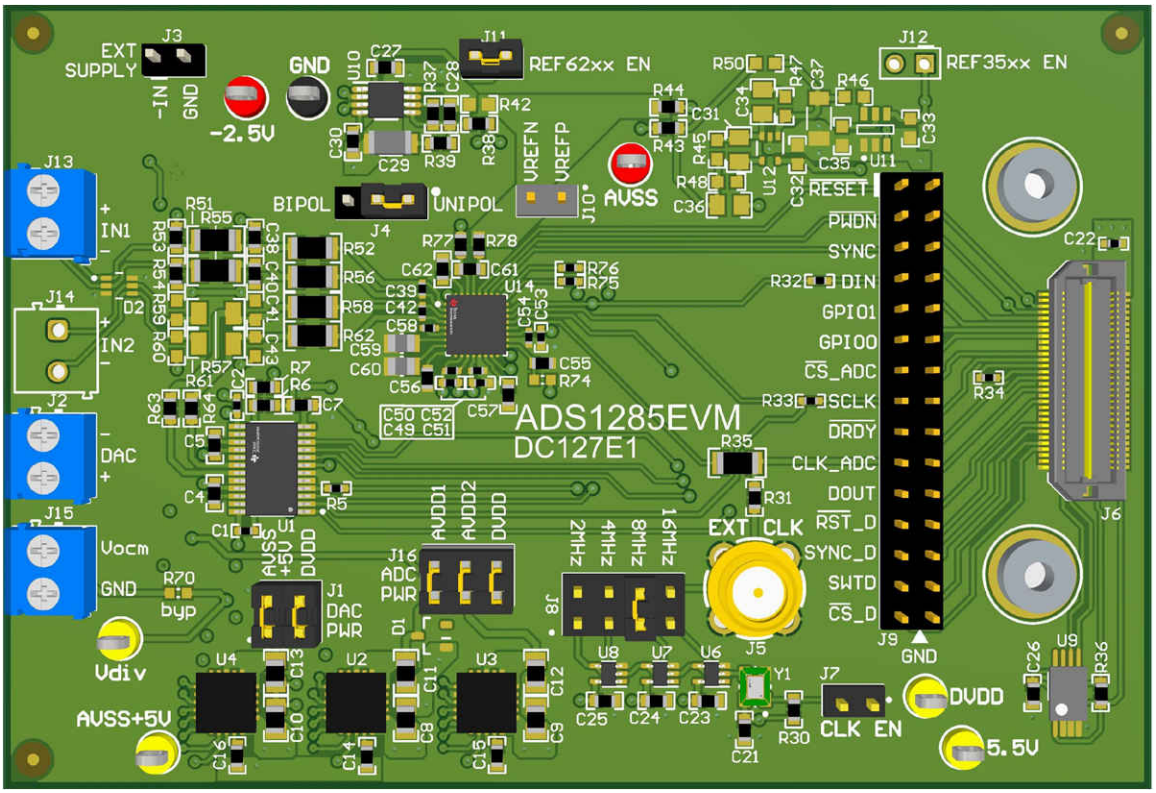
User's Guide

ADS1285EVM-PDK Evaluation Module

ABSTRACT



This user's guide describes the characteristics, operation, and use of the ADS1285EVM-PDK. This evaluation module (EVM) is an evaluation board for the ADS1285, a high-performance, 32-bit, multichannel, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The EVM allows evaluation of all aspects of the ADS1285. This manual covers the operation of the ADS1285EVM-PDK. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS1285EVM-PDK. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

Table of Contents

List of Figures

List of Tables

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1 EVM Overview

The evaluation kit includes the ADS1285EVM-PDK board and the precision host interface (PHI) controller board. The PHI board enables the accompanying computer software to communicate with the ADC over the universal serial bus (USB) for data capture and analysis because the ADS1285EVM-PDK does not contains a microprocessor on the board.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS1285EVM-PDK
- Supplies power to all active circuitry on the ADS1285EVM-PDK board

The following related documents are available for download through the Texas Instruments web site at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
ADS1285	SBASAK6

1.1 ADS1285EVM-PDK Kit

The ADS1285 evaluation module kit includes the following features:

- Contains all support circuitry needed for the ADS1285
- USB powered: No external power supply is required
- Voltage reference options: External or onboard
- Clock options: External clock source or 16.3840-MHz onboard crystal oscillator with dividers for 8.192-MHz, 4.096-MHz, and 2.048-MHz frequencies
- Voltage supply options: Unipolar or bipolar support with adjustable AVDD1 low-dropout regulator (LDO) and externally sourced –2.5-V LDO
- Signals contained within signal bank for ease of probing
- Built-in analysis tools including scope, FFT, and histogram display using the graphical user interface (GUI)

2 ADS1285EVM-PDK Quick-Start Guide

The following instructions are a step-by-step guide to connecting the ADS1285EVM-PDK to the computer and evaluating the performance of the ADS1285:

1. Review the default jumper settings in Section 7 and GUI software installation in Section 7.2.
2. Connect the ADS1285EVM-PDK to the PHI. Install the two screws as indicated in Figure 2-1.
3. Attach the micro USB to the PHI board and your PC. Three LEDs illuminate on the PHI board to indicate connectivity to the PC.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 2-1 shows the resulting LED indicators.

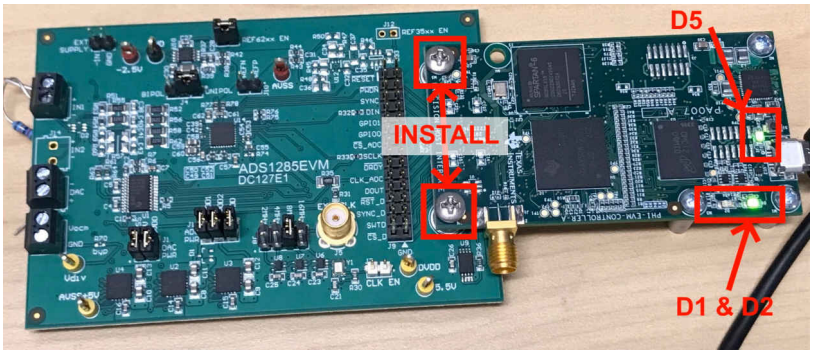


Figure 2-1. ADS1285EVM-PDK Hardware Setup and LED Indicators

4. Launch the ADS1285EVM-PDK GUI software and power will be supplied to the EVM.
   a. The default installation path is *C:\Program Files (x86)\Texas Instruments\ADS1285 EVM*.
5. As shown in Figure 2-2, use the *Configuration* section of the GUI for a specific clock input, desired data rate, and number of samples. Then, use the **Capture** button to collect data. Section 8.1 details the EVM GUI global input parameters and the various pages within the GUI.

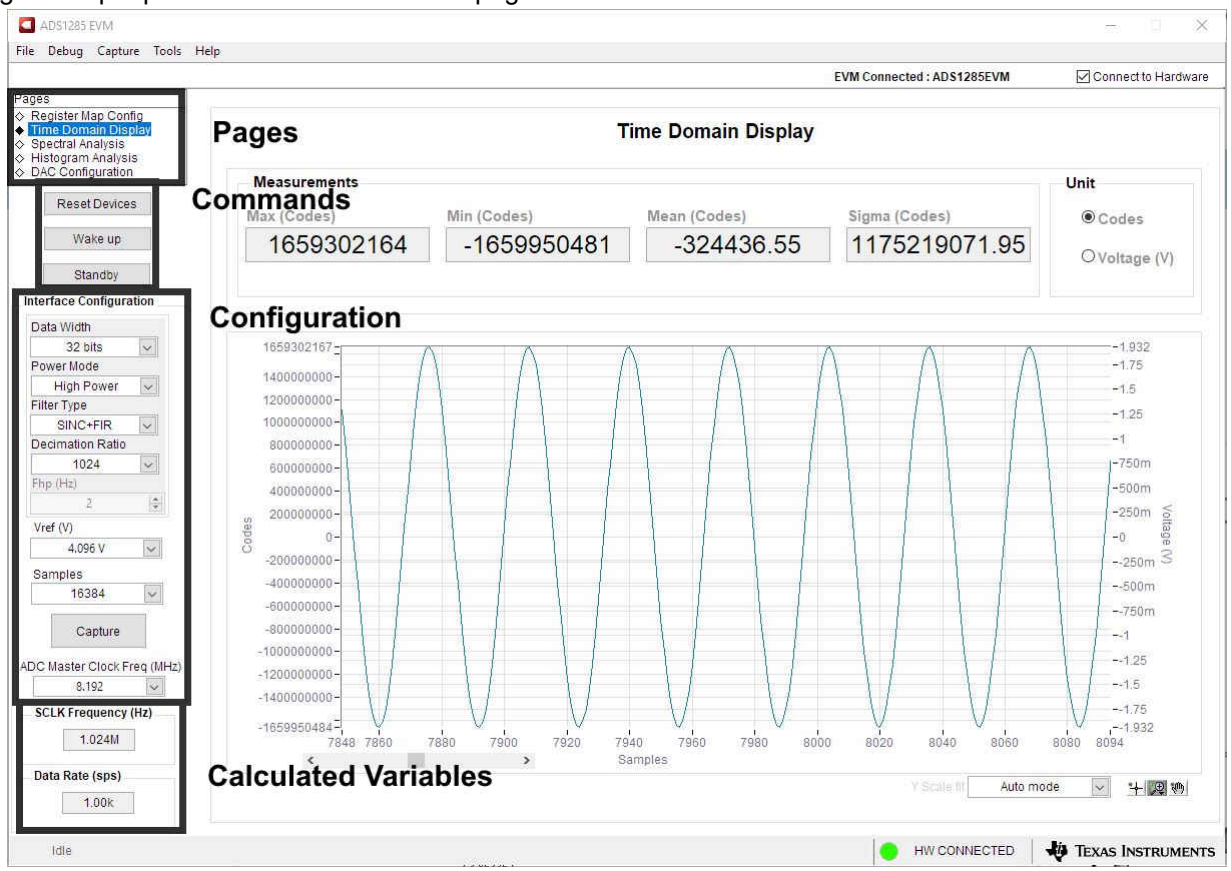


Figure 2-2. EVM GUI Global Input Parameters

3 EVM Analog Interface

The ADS1285EVM-PDK is designed for easy interfacing with analog sources. This section details the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

3.1 ADC Analog Input Signal Path

Analog inputs to the EVM can be connected to either terminal block associated with each ADC channel. The screw terminal blocks (J13, and J14) can interface directly with the leads of an external sensor input. Figure 3-1 depicts the signal chain used for the two input channels on the EVM and Table 3-1 lists the supported input options.

An input must not be applied such that the voltage on the input pins of the ADS1285 exceeds the absolute maximum ratings. For more details, see the *ADS1285 data sheet*.

R53 and R54 provide common-mode voltage paths for the channel 1 inputs. See Section 5 for more information. In addition, R51 and C38 (in combination with R55 and C40) provide the common-mode, low-pass filters for the positive and negative inputs, respectively. This configuration places the –3-dB cutoff frequency at approximately 720.0 kHz. Furthermore, R52 and R56 in combination with C39 provides the differential low-pass filter used in antialiasing, and –3-dB cutoff frequency is approximately 72.0 kHz. The series impedance is kept relatively low to maintain adequate total harmonic distortion (THD) performance. Similar differential and common-mode, low-pass filters are present on all inputs.

Specifically for channel 2, the default configuration is set up to use the DAC1282 on the input. The common mode filters for this configuration are not populated, instead R63 and R64 are populated so that they connect directly with the inputs for channel 2. Maintain this configuration if the DAC page of the GUI is used; see Section 6.

Note

A TPD4E1B06DCKR footprint is connected to all four inputs that function as a TVS diode. Even though the diode is not populated in the default version of the EVM, the diode can be populated for external protection.

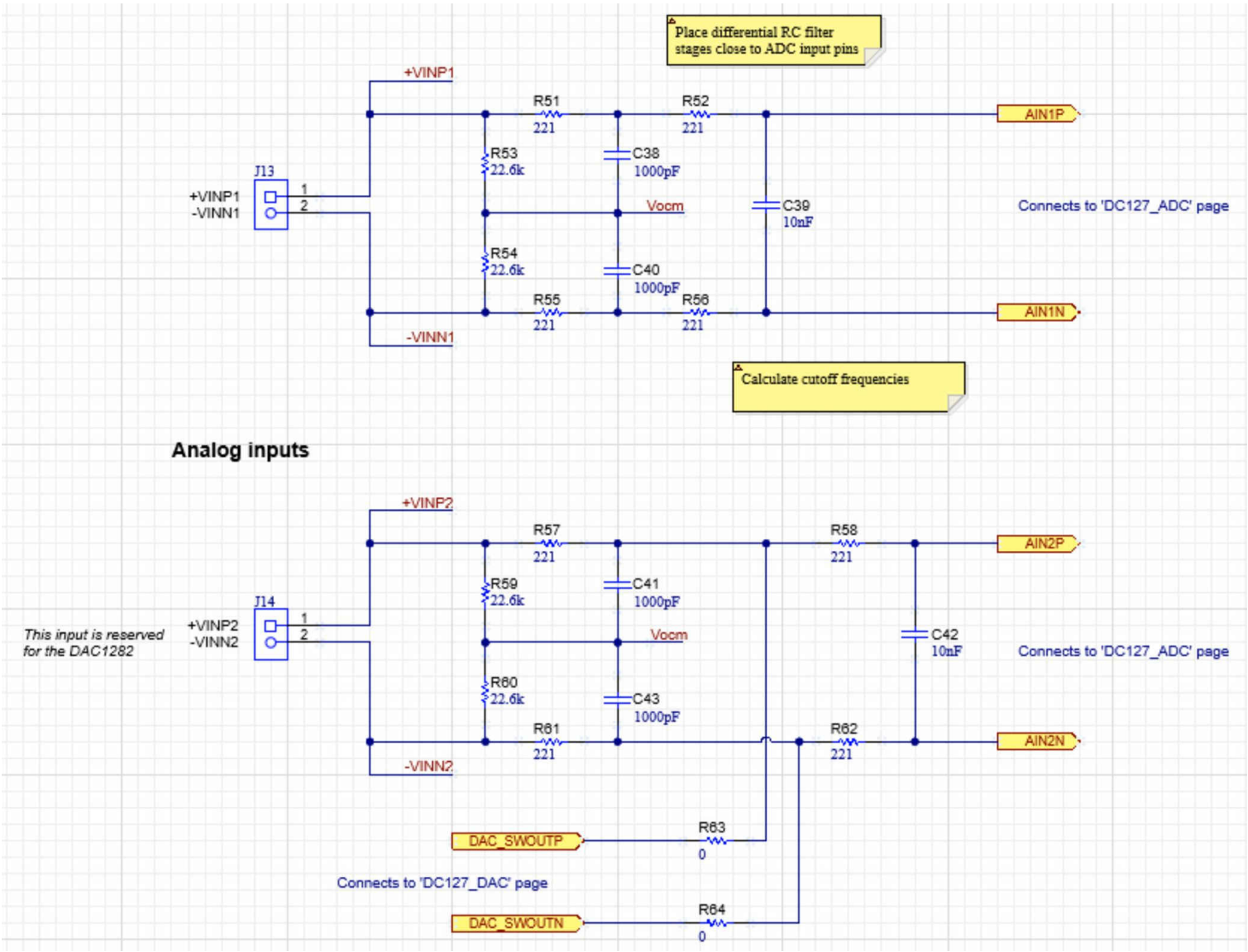


Figure 3-1. Input Terminal Blocks and Headers (Schematic)

Table 3-1. Analog Input Terminal Blocks (J13, J14)

Terminal Block	Pin	Function	ADS1285 Input Pin(s)
J13	1	Channel 1 positive input	+VINP1 (Eventually leading to AIN1P)
	2	Channel 1 negative input	–VINN1 (Eventually leading to AIN1N)
J14	1	Channel 2 positive input	+VINP2 (Eventually leading to AIN2P)
	2	Channel 2 negative input	–VINN2 (Eventually leading to AIN2N)

3.2 ADC Input Clock (CLK) Options

Using the onboard oscillator, clock dividers, and external connectors, the ADS1285EVM-PDK has device configuration flexibility. The ADC operates from CLK, which generates the modulator clock (f_{MOD}), provided in one of two ways:

- A crystal oscillator and the accompanying clock dividers can provide a selectable frequency for the entire range of the ADC.
  - The onboard crystal oscillator (Y1) provides the nominal 16.384-MHz clock frequency
  - The dividers (U6, U7, and U8) step down the frequency to 8.192 MHz (the default configuration), 4.096 MHz, and 2.048 MHz
  - J8 allows the user to select between these frequencies and connect them directly to CLK by using a shunt
- An external main clock can be provided to a subminiature version A (SMA) connector (J5) or to pins 8, 6, 4, or 2 of J7 when a shunt does not select the frequency from the crystal oscillator.
  - In this case, a shunt must not cover J7 so that CLK is connected to any of the crystal oscillator signals
  - Be sure to review the valid CLKIN input frequency in the data sheet

Note

All clock sources are sourced back to the PHI connector (J6) so that the GUI SCLK communication is synchronous with CLK.

Figure 3-2 shows a schematic for the clock source.

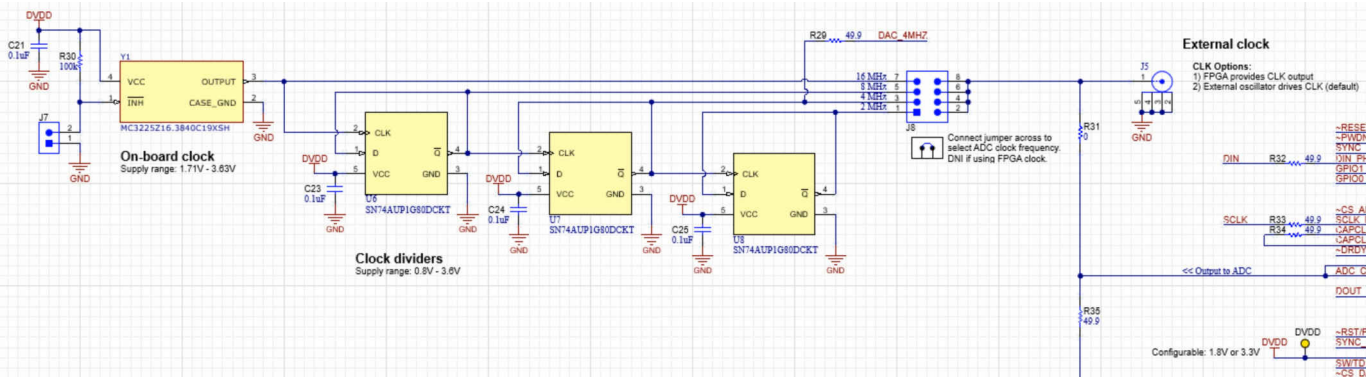


Figure 3-2. CLK Source (Schematic)

4 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS1285 ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS1285EVM-PDK GUI. When the hardware is initialized, the EEPROM is no longer used.

4.1 Connection to the PHI

The ADS1285EVM-PDK board communicates with the PHI through a shrouded, 60-pin connector, J6. There are two round standoffs next to J6 with Phillips-head screws. To connect the PHI to the EVM, remove the screws, attach the PHI to the EVM, and replace the screws into the standoffs. The screws secure the EVM to the PHI and ensures the connection between the boards.

Table 4-1 lists the different PHI connection and their functions.

Table 4-1. PHI Connector Pin Functions

PHI Connector Pin Name	PHI Connector Pin	Function
5.5V	J6[1]	Power-supply source for the analog section of the EVM
GND	J6[3]	Ground
~RESET	J6[6]	ADC reset pin, active low
~PWDN	J6[8]	ADC power-down pin, active low
SYNC	J6[12]	ADC synchronization, active high
DIN_PHI	J6[12]	SPI: DIN from the ADC, POCI, or serial interface data in
GPIO1	J6[14]	General-purpose I/O 1 pin from the ADC
GPIO0	J6[16]	General-purpose I/O 0 pin from the ADC
~CS_ADC	J6[22]	SPI: $\overline{CS}$, chip-select, or serial interface select, active low for the ADC
SCLK_PHI	J6[24]	SPI: Serial interface clock, or SCLK
CAPCLK_OUT	J6[26]	Output path for the PHI signal to synchronize captures with any delay from the EVM
CAPCLK_IN	J6[28]	Input path for the PHI signal to synchronize captures with any delay from the EVM
~DRDY	J6[30]	SPI: Data-ready signal for the ADS1285; active-low $\overline{DRDY}$
ADC_CLK (input)	J6[32]	Input for the PHI to sense CLK
ADC_CLK (output)	J6[34]	Possible output for the PHI to provide CLK (not supported on the ADS1285EVM-PDK)
DOUT	J6[38]	SPI: Serial data output for the ADS1285, or PICO
~RST/PWDN_DAC	J6[46]	Reset or power-down input pin for the DAC1282
SYNC_DAC	J6[48]	Synchronize input pin for the DAC1282
WP	J6[49]	Write protection for the EEPROM
DVDD	J6[50]	Power-supply source for the digital section of the EVM
SW/TD_DAC	J6[52]	Switch control input or bitstream input pin for the DAC1282
~CS_DAC	J6[54]	SPI: Serial port chip select, or $\overline{CS}$, for the DAC1282
SDA	J6[56]	I^2C serial data for the EEPROM used to identify the EVM
SCL	J6[58]	I^2C serial clock for the EEPROM used to identify the EVM
ID_PWR	J6[59]	Power-supply source for the EEPROM used to identify the EVM
GND	J6[60]	Ground

4.2 Digital Header

In addition to the PHI, the EVM has a header connected to the digital lines that can be used to connect a logic analyzer or oscilloscope. This placement allows for easy access to the digital communications. Header J7 is connected to the digital lines between the ADS1285 and the PHI connector. Table 4-2 describes the digital header pins.

Table 4-2. Digital Header Pins

Signal Name	Digital Header Pin
~RESET	J9[1]
~PWDN	J9[3]
SYNC	J9[5]
DIN_PHI	J9[7]
GPIO1	J9[9]
GPIO0	J9[11]
~CS_ADC	J9[13]
SCLK_PHI	J9[15]
~DRDY	J9[17]
ADC_CLK	J9[19]
DOUT	J9[21]
~RST/PWDN_DAC	J9[23]
SYNC_DAC	J9[25]
SW/TD_DAC	J9[27]
~CS_DAC	J7[29]

5 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer that is routed to the 5.5-V net on the ADS1285EVM-PDK on the board.

The EEPROM on the ADS1285EVM-PDK uses a 3.3-V power supply, ID_PWR, generated directly by the PHI. The 3.3-V supply to the digital section of the ADC, 3V3_IOVDD, is provided directly by a separate LDO on the PHI.

The PGA positive analog supply of the ADC, AVDD1, is powered by the TPS7A4701 (U2) onboard the EVM, which is a low-noise linear regulator that uses the 5.5-V supply on the PHI to generate a cleaner 5-V output. The TPS47A4701 is a configurable LDO so R8 to R13 can be used to change the voltage.

AVDD2 is the modulator analog supply that is also used by the ADC. As with AVDD1, AVDD2 is generated by the TPS7A4701 (U3) onboard the EVM, which is a low-noise linear regulator that uses the 5.5-V supply on the PHI to generate a cleaner 3-V output. The TPS7A4701-Q1 is a configurable LDO so R14 to R19 can be used to change the voltage.

AVSS+5V is used for the analog supply of the DAC1282. This pin also uses a TPS7A4701-Q1 (U4) onboard the EVM, which is a low-noise linear regulator that uses the 5.5-V supply on the PHI to generate a cleaner 5-V output. The DAC1282 requires a 5-V supply so R20 to R25 must not be modified.

The user has the option to configure the EVM for unipolar supplies (AVSS = 0 V) by placing a jumper to cover pins 1 and 2 of J4 (UNIPOL), or to configure the EVM for bidirectional supplies (AVSS = –2.5 V) by placing the jumper to cover pins 2 and 3 of JP4 (BIPOL). The TPS7A3001 (U5) is an LDO with a V_{IN} range from –3 V to –36 V that provides a clean –2.5-V output for the AVSS voltage. However, an external voltage is needed to supply the AVSS voltage, which can be supplied using J3. Because AVDD1 is referenced to AVSS, the output AVDD1 must be modified using R8 to R13 so that the AVDD1 to AVSS voltage does not go above the recommended operating conditions. The supply selection and –2.5-V generation circuit is illustrated in Figure 5-1.

AVDD1 is used as the supply for the REF6241, which is a high-precision voltage reference with an integrated high-bandwidth buffer in reference to AVSS. The voltage reference can be used to supply the positive reference,

VREFP, for the ADC using R38 as a pass transistor. Alternatively, R38 and R42 can be depopulated so the positive and negative reference externally using pins 1 and 2 of J10, respectively.

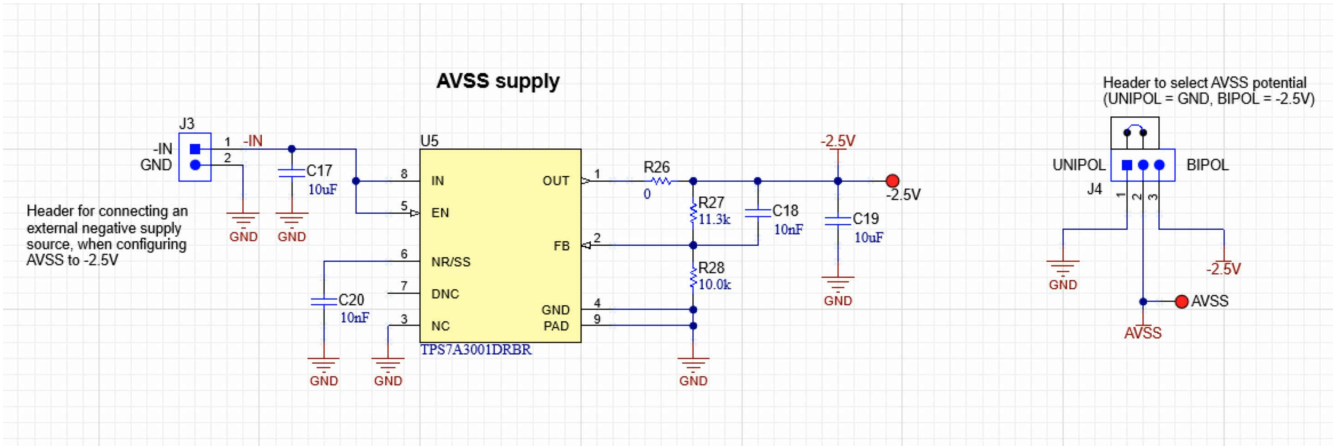


Figure 5-1. ADS1285EVM-PDK Unipolar and Bidirectional Supplies Selection

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and their loads to minimize inductance along the load current path.

As mentioned previously in Section 1, power to the EVM is supplied by the PHI through connector J5. For information about PHI pins and the power connections, see Table 4-1.

With modifications, the user may use external supplies for any voltage supplies. Using the ADC PWR header (J26), DAC PWR header (J1), and the unipolar or bipolar select (J4); the shunts can be depopulated for direct access to the AVDD1, AVDD2, AVSS+5V, DVDD, and AVSS pins.

6 DAC

The ADS1282EVM-PDK contains a DAC1282, which is a fully integrated digital-to-analog converter (DAC) that provides a low distortion, digital synthesized voltage output suitable for testing seismic equipment and the ADS128x family of devices; see the DAC1282 data sheet for more information. The DAC1282 can be used in combination with the GUI to directly supply an input voltage for testing and performance purposes. For more information on configuring the inputs to use the DAC1282, see Section 3.1.

The output frequency is programmable from 0.5 Hz to 250 Hz and the magnitude is scaled by both analog and digital control. The analog gain is adjustable in 6-dB steps and the digital gain in 0.5-dB steps. The analog gain settings match those of the ADS1282 for testing at all gains with high resolution. Controlling the settings of the DAC1282 can be done on the *DAC Configuration* page of the GUI.

The DAC1282 uses AVSS+5V and DVDD for its power supplies and shares the same reference as the ADS1285. This configuration minimizes potential errors from using separate references between the devices.

7 ADS1285EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS1285EVM-PDK.

7.1 Default Jumper Settings

After unpacking, the EVM is already configured with the default jumper settings. Figure 7-1 shows the locations for the default jumpers and Table 7-1 shows the functions of the default shunts.

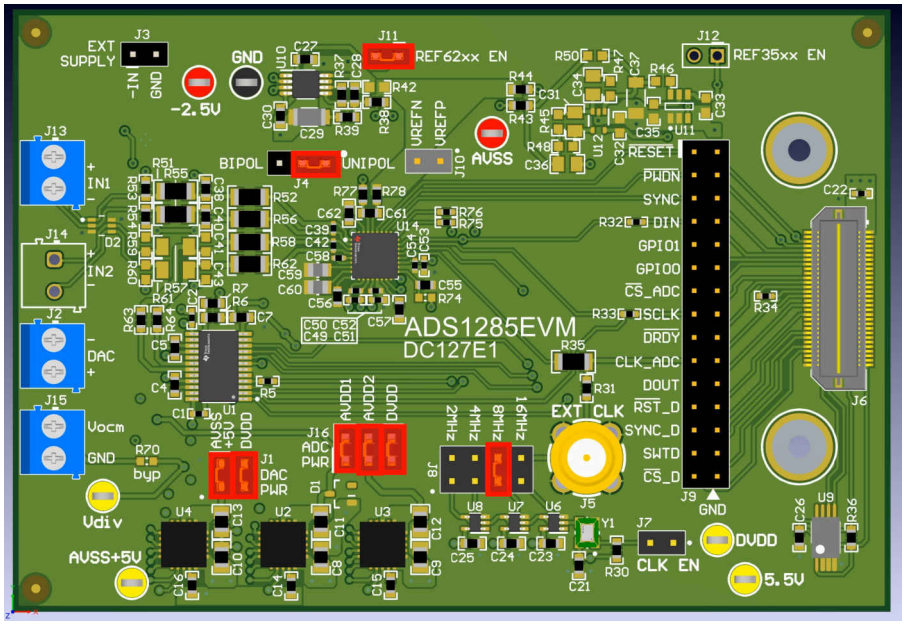


Figure 7-1. ADS1285EVM-PDK Jumper Default Settings

Table 7-1. Default Shunt Settings

Header Designator	Position	Function
J11	[1-2]	Enables the REF62x supply to VREFP
J4	[1-2]	Connects AVSS to GND for unipolar ADC supply mode
J8	[5-6]	Connects CLK to an 8.192-MHz source from the crystal oscillator and clock divider
J10	Not installed	Header to supply the external reference voltage to VREFN and VREFP
J1	[1-2]	DAC PWR: Connects the output of the U4 LDO (AVSS+5V) to the DAC analog supply pin (AVDD)
J1	[3-4]	DAC PWR: Connects the PHI digital supply (DVDD) to the DAC digital supply pin (DVDD)
J16	[1-2]	ADC PWR: Connects the output of the U2 LDO (AVDD1) to the ADC analog supply 1 (AVDD1)
J16	[3-4]	ADC PWR: Connects the output of the U3 LDO (AVDD2) to the ADC analog supply 2 (AVDD2)
J16	[5-6]	ADC PWR: Connects the PHI digital supply (DVDD) to the ADC digital supply (IOVDD)
J3	Not installed	Header to supply the external input to U5 for the –2.5-V supply

Table 7-2 lists the nominal voltages that result from the default configuration.

Table 7-2. Nominal Voltages Resulting From a Default Configuration

Supply Name	Voltage (Referenced to GND)
AVSS	GND (0 V)
AVSS+5V	5 V
DVDD (IOVDD)	3.3 V
AVDD1	5 V
AVDD2	3 V
5.5V	5.5 V
REFP	4.096 V
–2.5V	NA, external supply needed

7.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS1285EVM-PDK and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The .exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 7-2 to complete the installation.

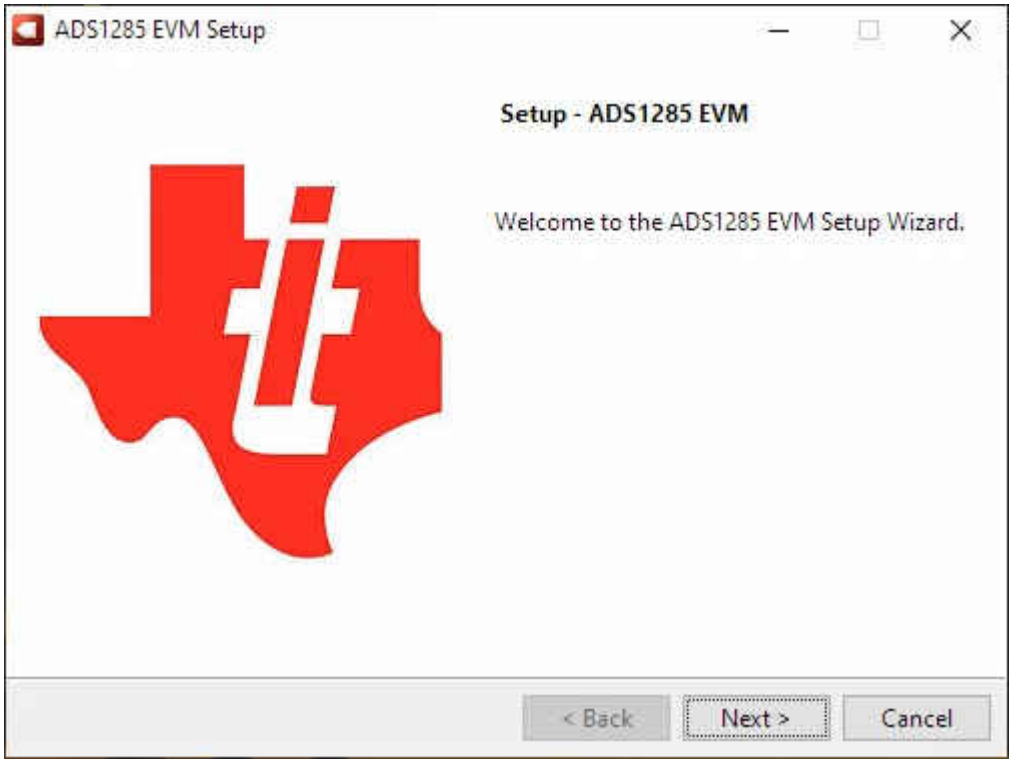


Figure 7-2. ADS1285 Software Installation Prompt

As part of the ADS1285EVM-PDK GUI installation, a prompt with a device driver installation (as shown in Figure 7-3) appears on the screen. Click *Next* to proceed.

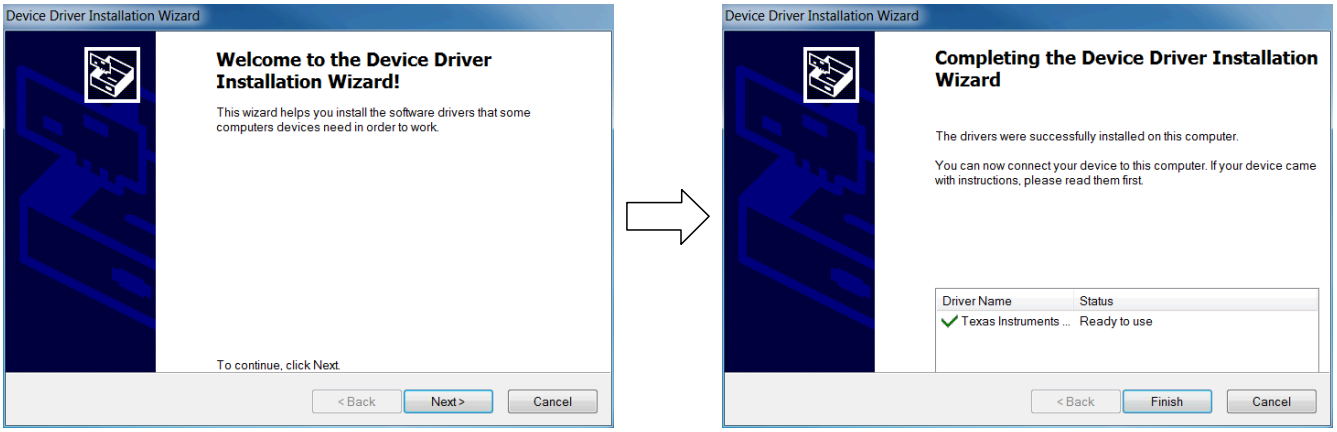


Figure 7-3. Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS1285EVM-PDK requires the LabVIEW® run-time engine and may prompt for the installation of this software, as shown in Figure 7-4, if not already installed.

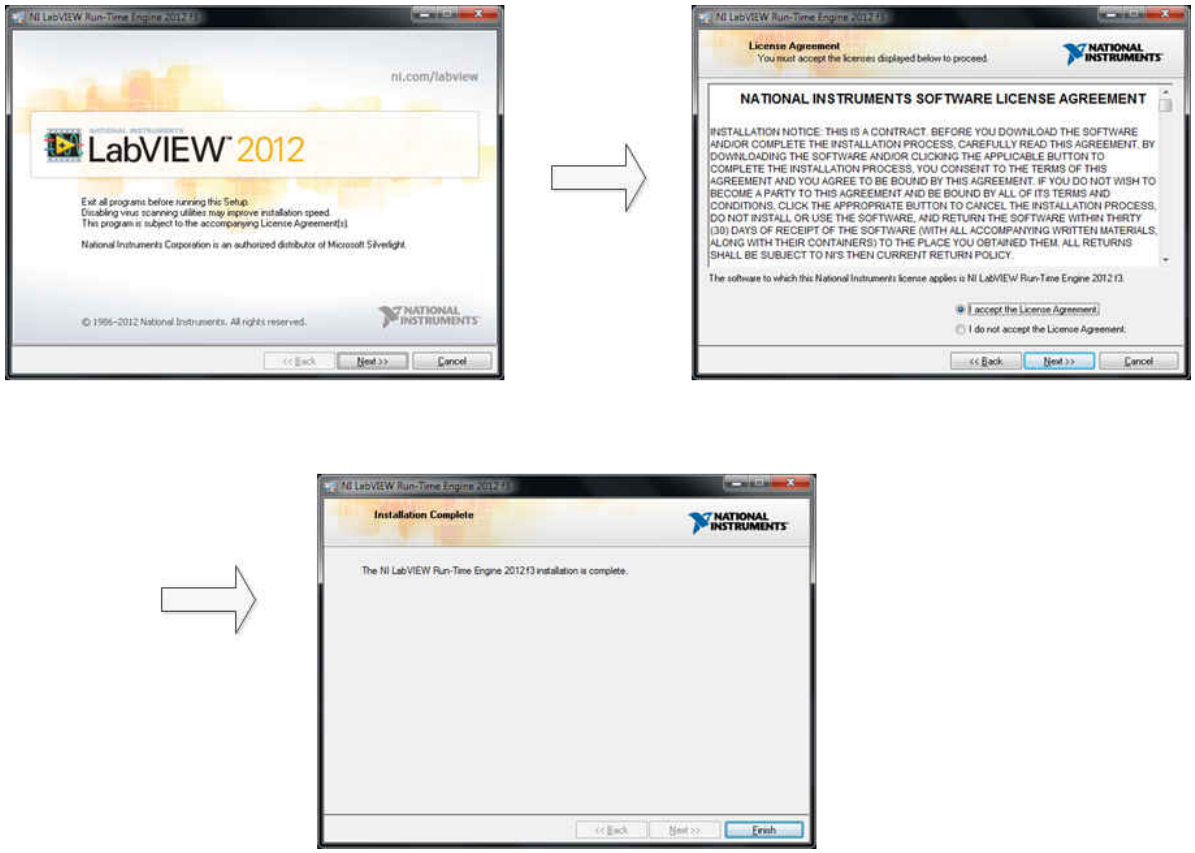


Figure 7-4. LabVIEW Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\ADS1285EVM-PDK* is available after these installations.

8 ADS1285EVM-PDK Software Reference

8.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over many other functions of the ADS1285, including: internal clock dividers, oversampling ratio (OSR), and number of samples to be captured. Figure 8-1 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS1285 can be exercised.

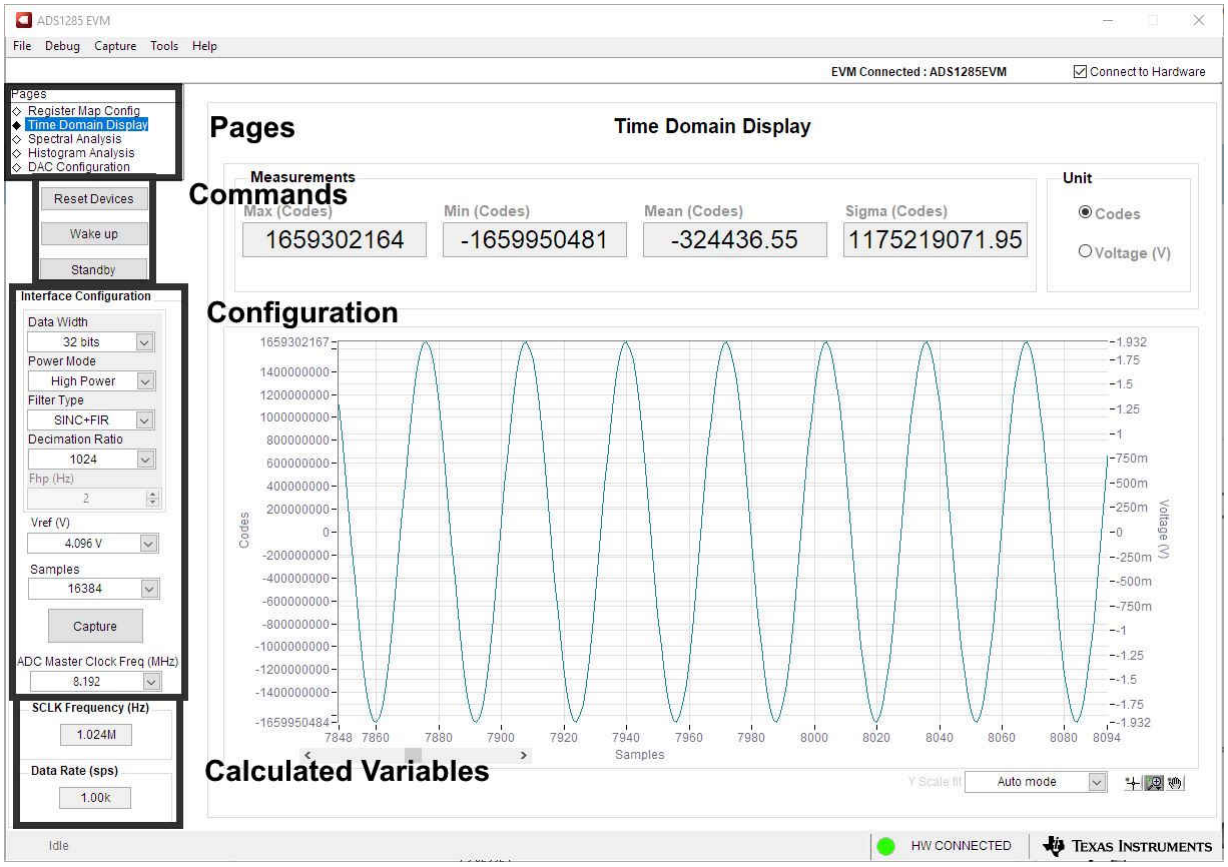


Figure 8-1. EVM GUI Global Input Parameters

There are four pages available in the ADS1285EVM-PDK GUI. The information area displays the results of each of the pages. Each of these pages display a different control or measurement of the device. The *Register Map Config* page reads and writes the registers of the device. The *Time Domain Display* page collects a set of data from the device and displays the result. The *Spectral Analysis* page can compute the FFT of the collected data, and the *Histogram Analysis* page shows a histogram of the collected data and displays basic statistics of the result.

The *Single Commands* section allows for direct control of the device for three basic functions. First, the **Reset** button sends a signal to the RESET pin to reset the device. The **Standby** button puts the device into a low-power state where all channels are disabled, and the reference and other non-essential circuitry are powered down. The **Wakeup** button exits standby mode.

The *Interface Configuration* section also sets the data rate by setting the internal clock dividers and OSR in the ADC. Finally, this section can set the power modes in the registers. The ADS1285 has three power modes (low-power, mid-power, and high-power) that are configured in the CONFIG0 register (bits 7-6). This configuration is used in conjunction with the jumper settings of JP8 for the CLK pin, as outlined in Section 3.2.

The *Clock and Sampling Rate* section allows the user to specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings, but the achievable

frequency may differ from the target value entered. This section also displays the sampling rate of the ADC as controlled by the internal clock dividers and the OSR.

The GUI is switched between hardware mode and simulation mode by checking and unchecking the *Connected to Hardware* box in the top right area of the screen at any time.

8.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS1285. This tool can be selected, as indicated in Figure 8-2, by clicking on the **Register Map Config** radio button at the *Pages* section of the left pane. On power-up, the values on this page correspond to the *Host Configuration Settings* that enable ADC sampling at the maximum sampling rate specified for the ADC. The register values can be edited by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately.

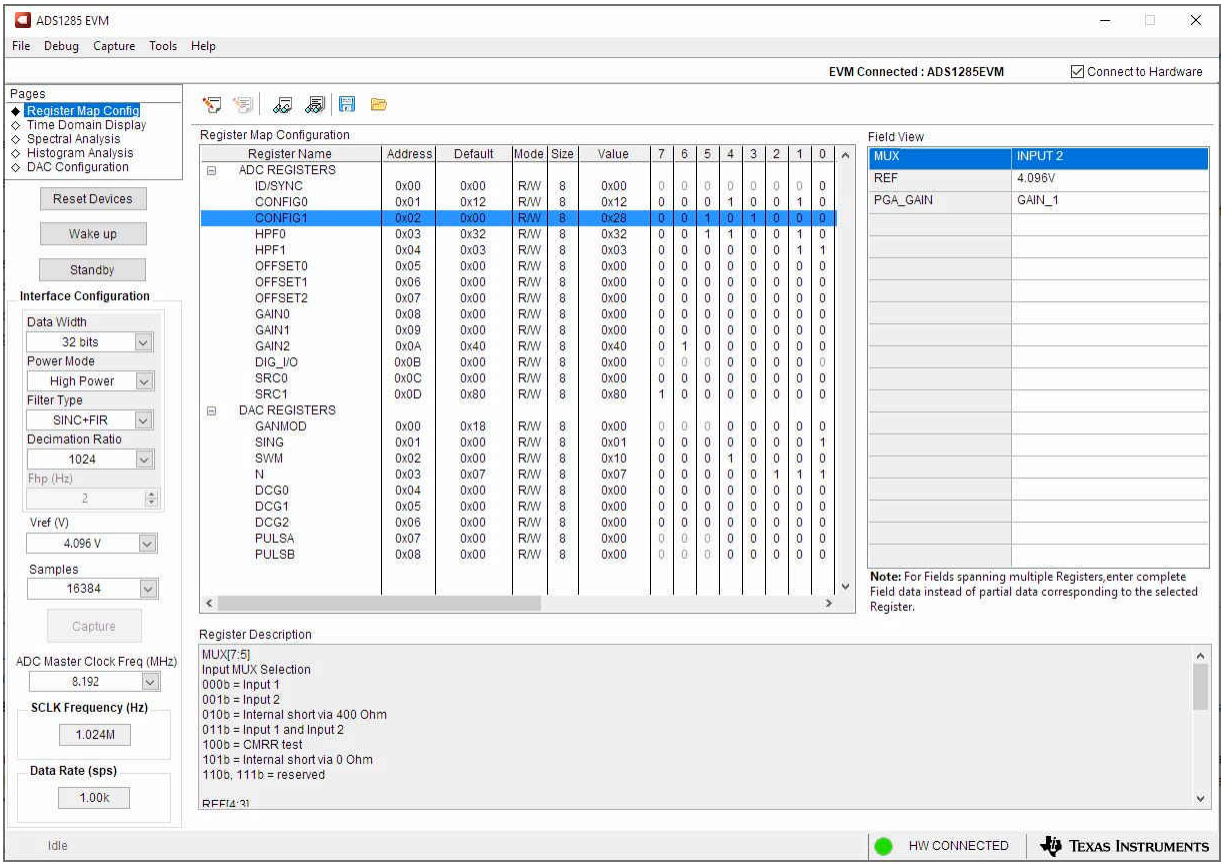


Figure 8-2. Register Map Configuration

Section 8.3 through Section 8.5 describe the data collection and analysis features of the ADS1285EVM-PDK GUI.

8.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS1285EVM-PDK, as per the current interface mode settings indicated in Figure 8-3 by using the **Capture** button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

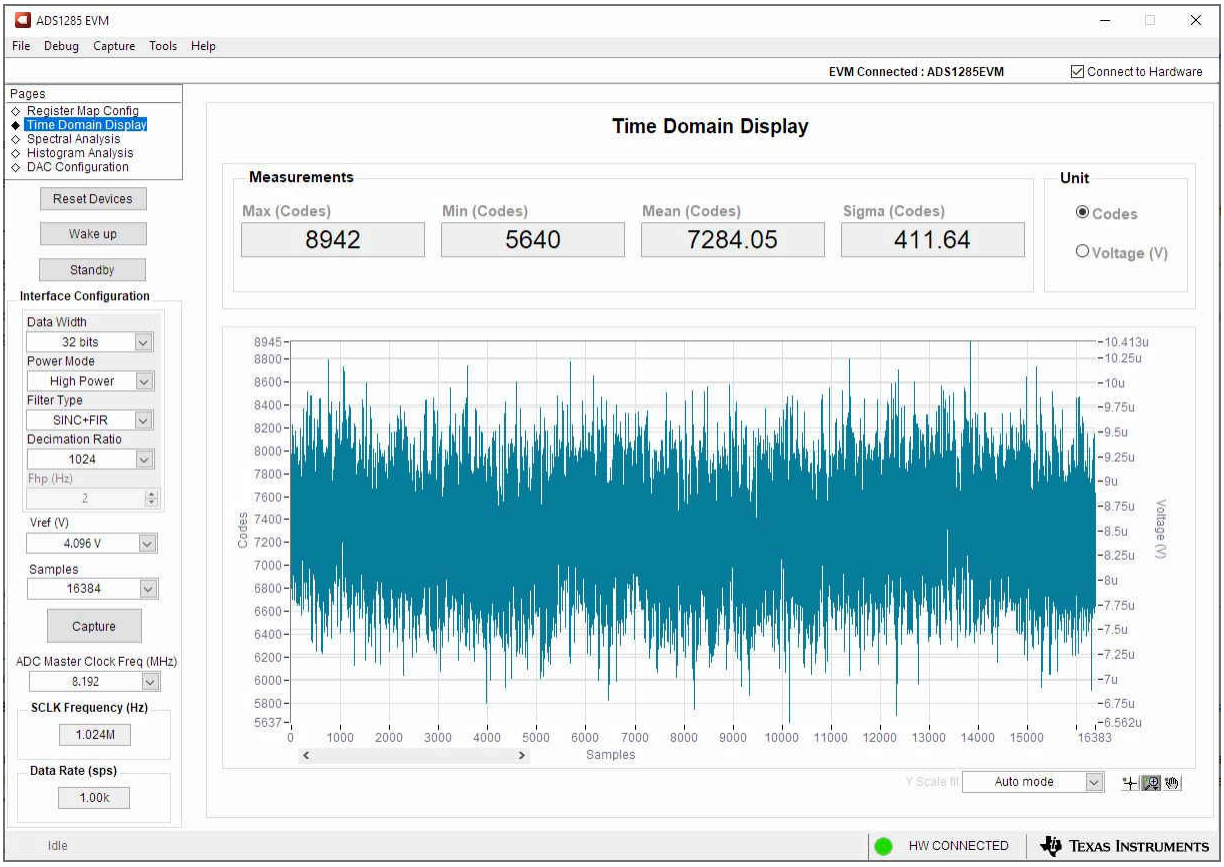


Figure 8-3. Time Domain Display Tool Options

8.4 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 8-4, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1285 ADC through single-tone sinusoidal signal FFT analysis using the *7-term Blackman-Harris* window setting.

Figure 8-4. Spectral Analysis Tool

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman-Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

8.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel.

As shown in Figure 8-5, the histogram corresponding to a DC input is displayed on clicking the **Capture** button.

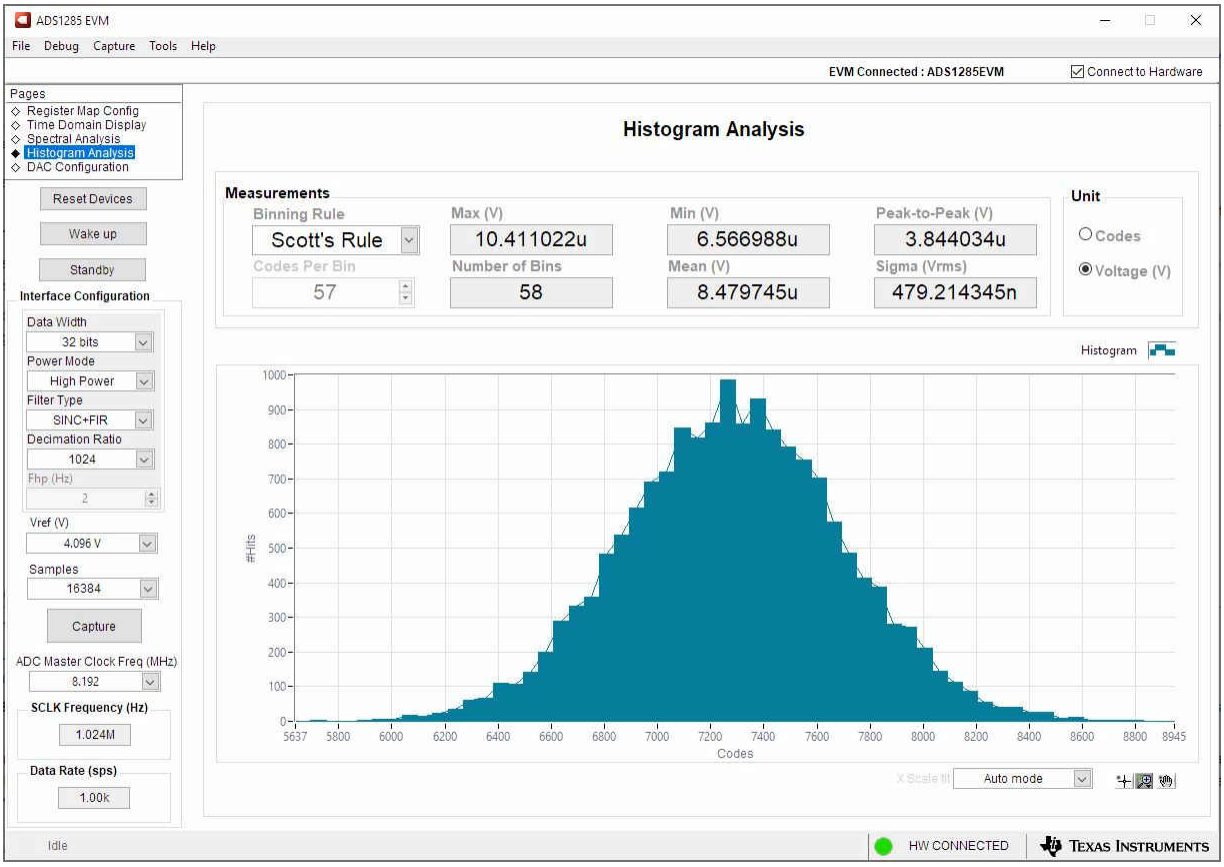


Figure 8-5. Histogram Analysis Tool

9 ADS1285EVM-PDK Bill of Materials, PCB Layout, and Schematics

9.1 Bill of Materials

Table 9-1 lists the ADS1285EVM-PDK bill of materials.

Table 9-1. ADS1285EVM-PDK Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC127	Any		
C1, C2, C3, C6, C22, C49, C51, C53, C63	9	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X5R, 0402	402	C1005X5R1V105K050BC	TDK		
C4, C5	2	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, C0G/NP0, 0603	603	06035A102KAT2A	AVX		
C7, C57, C61, C62	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X5R, 0603	603	C1608X5R1H104K080AA	TDK		
C8, C9, C10, C11, C12, C13, C17, C19	8	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	805	CL21A106KAFN3NE	Samsung Electro-Mechanics		
C14, C15, C16, C27, C30, C48	6	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	603	C0603C105K3RACTU	Kemet		
C18, C20	2	0.01uF	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X7R, 0603	603	8.85012E+11	Wurth Elektronik		
C21, C23, C24, C25, C26, C45	6	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X8R, AEC-Q200 Grade 0, 0603	603	CGA3E3X8R1H104K080AB	TDK		
C28	1	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 5%, C0G/NP0, 0603	603	C0603H103J3GACTU	Kemet		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C29	1	22uF	CAP, CERM, 22 µF, 16 V,+/- 20%, X5R, AEC-Q200 Grade 3, 1206	1206	CL31A226MOHNNNE	Samsung Electro-Mechanics		
C38, C40	2	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C102J5GACTU	Kemet		
C39, C42, C58	3	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, C0G/NP0, 0402	402	GCM155R71H103KA55D	MuRata		
C44, C46	2	0.033uF	CAP, CERM, 0.033 µF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	805	CGA4J2C0G1H333J125AA	TDK		
C47	1	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	CGA5L3X7R1H105K160AB	TDK		
C50, C52, C54	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	402	GCM155R71H104KE02D	MuRata		
C55	1	0.22uF	CAP, CERM, 0.22 uF, 25 V, +/- 10%, X7R, 0603	603	GRM188R71E224KA88D	MuRata		
C56	1	4700pF	CAP, CERM, 4700 pF, 50 V, +/- 10%, X7R, 0603	603	C0603X472K5RACTU	Kemet		
C59, C60	2	0.047uF	CAP, CERM, 0.047 µF, 25 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	805	C0805C473J3GACTU	Kemet		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL		
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik		
J1	1		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec		
J2, J13, J15	3		Terminal Block, 3.5mm, 2x1, Tin, TH	Terminal Block, 3.5mm, 2x1, TH	1776275-2	TE Connectivity		
J3, J11	2		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
J4	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
J5	1		Connector, SMA, TH	SMA	142-0701-231	Cinch Connectivity		
J6	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A-K-TR	Samtec		
J7	1		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J8	1		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec		
J9	1		Header, 100mil, 15x2, Gold, TH	15 x 2 Header	MTSW-115-22-G-D-315	Samtec		
J10	1		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J16	1		Header, 100mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions		
R1, R2, R30, R71, R72, R73	6	100k	RES, 100 k, 1%, 0.1 W, 0603	603	RC0603FR-07100KL	Yageo		
R3, R4, R5, R29, R32, R33, R34, R75, R76	9	49.9	RES, 49.9, 1%, 0.063 W, 0402	402	RC0402FR-0749R9L	Yageo America		
R6, R7, R26, R31, R38, R43, R44, R63, R64, R77, R78	11	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo		
R8, R11, R15, R20, R23	5	0	RES, 0, 5%, 0.063 W, 0402	402	RC0402JR-070RL	Yageo America		
R27	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	603	RC0603FR-0711K3L	Yageo		
R28, R36, R40, R67	4	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo		
R35	1	49.9	RES, 49.9, 1%, 0.25 W, 1206	1206	RC1206FR-0749R9L	Yageo America		
R37, R39	2	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3RQFR22V	Panasonic		
R51, R52, R55, R56, R58, R62	6	221	RES, 221, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8ENF2210V	Panasonic		
R53, R54	2	22.6k	RES, 22.6 k, 1%, 0.1 W, 0603	603	RC0603FR-0722K6L	Yageo		
R65	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031K00FKEA	Vishay-Dale		
R66	1	634k	RES, 634 k, 0.1%, 0.1 W, 0603	603	RT0603BRD07634KL	Yageo America		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R68	1	37.4	RES, 37.4, 1%, 0.1 W, 0603	603	RC0603FR-0737R4L	Yageo		
R69	1	1.00Meg	RES, 1.00 M, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031M00FKEA	Vishay-Dale		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP5, TP6, TP7	4		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone		
TP2, TP3	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone		
TP4	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone		
U1	1		Low Distortion Digital-to-Analog Converter for Seismic Applications 24-TSSOP -40 to 85	TSSOP24	DAC1282AIPW	Texas Instruments		
U2, U3, U4	3		Automotive 35V, 1A, 4.2µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701QRGWRQ1	Texas Instruments	TPS7A4701QRGWTQ1	Texas Instruments

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U5	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments	TPS7A3001DRBT	Texas Instruments
U6, U7, U8	3		Low-Power Single Postitive-Edge-Triggered D-Type Flip-Flop, DCK0005A, SMALL T&R	DCK0005A	SN74AUP1G80DCKT	Texas Instruments		
U9	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm		
U10	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6241IDGKR	Texas Instruments	REF6241IDGKT	Texas Instruments
U13	1		700 nA, Zero-Crossover Rail-to-Rail I/O Operational Amplifier, 1.8 to 5.5 V, -40 to 85 degC, 5-pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	DCK0005A	OPA369AIDCKT	Texas Instruments		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U14	1		ADS1285 High Resolution, Delta-Sigma ADC for Seismic 4000sps 1 to 64 as Gain 3-5.25V	VQFN32	ADS1285IRHBT	Texas Instruments		
Y1	1		16.384MHz XO (Standard) CMOS Oscillator 1.71V ~ 3.63V Standby (Power Down) 4-SMD, No Lead	SMT_XTAL_3MM2_2MM5	MC3225Z16.3840C19XSH	Kyocera	MC3225Z16.3840C19XSH	
C31, C34	0	0.033uF	CAP, CERM, 0.033 µF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	805	CGA4J2C0G1H333J125AA	TDK		
C32	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X8R, AEC-Q200 Grade 0, 0603	603	CGA3E3X8R1H104K080AB	TDK		
C33, C35	0	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	603	C0603C105K3RACTU	Kemet		
C36	0	10uF	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	805	GRM21BR71A106KA73L	MuRata		
C37	0	10uF	CAP, CERM, 10 µF, 25 V,+/- 20%, X5R, 1206	1206	GRM31CR61E106MA12L	MuRata		
C41, C43	0	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C102J5GACTU	Kemet		
D1	0	5V	Diode, Zener, 5 V, 250 mW, SOT-23	SOT-23	PLVA650A,215	Nexperia		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
D2	0		14.5V (Typ) Clamp 3A (8/20µs) Ipp Tvs Diode Surface Mount SC-70-6	SC70-6	TPD4E1B06DCKR	Texas Instruments		
J12	0		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
J14	0		Terminal Block, 3.5mm, 2x1, Tin, TH	Terminal Block, 3.5mm, 2x1, TH	1776275-2	TE Connectivity		
R9, R10, R12, R13, R14, R16, R17, R18, R19, R21, R22, R24, R25	0	0	RES, 0, 5%, 0.063 W, 0402	402	RC0402JR-070RL	Yageo America		
R41	0	120k	RES, 120 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603120KJNEA	Vishay-Dale		
R42, R74	0	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo		
R45, R50	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031K00FKEA	Vishay-Dale		
R46, R47, R49	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo		
R48	0	37.4	RES, 37.4, 1%, 0.1 W, 0603	603	RC0603FR-0737R4L	Yageo		
R57, R61	0	221	RES, 221, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8ENF2210V	Panasonic		
R59, R60	0	22.6k	RES, 22.6 k, 1%, 0.1 W, 0603	603	RC0603FR-0722K6L	Yageo		
R70	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic		

Table 9-1. ADS1285EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U11	0		Ultra Low-Power, High-Precision Voltage Reference, SOT23-6	SOT23-6	REF3516QDBVR	Texas Instruments		
U12	0		700 nA, Zero-Crossover Rail-to-Rail I/O Operational Amplifier, 1.8 to 5.5 V, -40 to 85 degC, 5-pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	DCK0005A	OPA369AIDCKT	Texas Instruments		

9.2 PCB Layout

Figure 9-1 through Figure 9-6 illustrate the ADS1285EVM-PDK PCB layout.

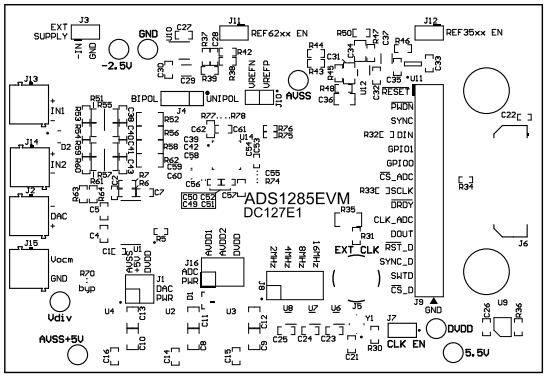


Figure 9-1. Top Silkscreen

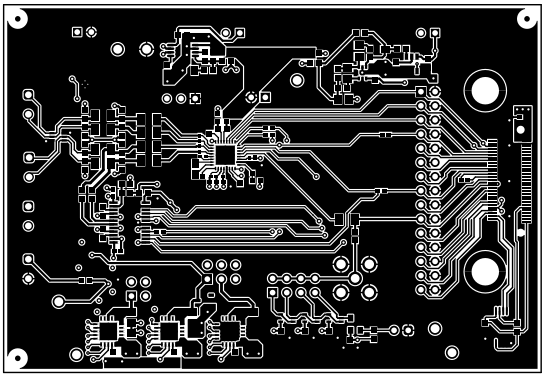


Figure 9-2. Top Layer

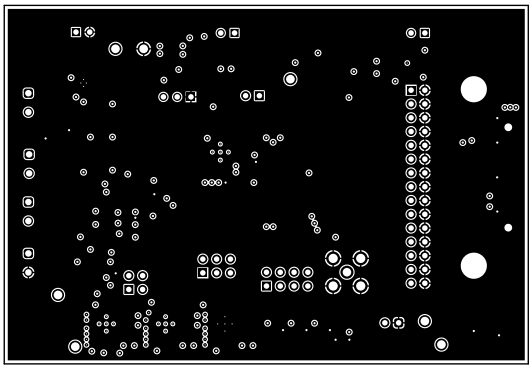


Figure 9-3. Ground Layer 1

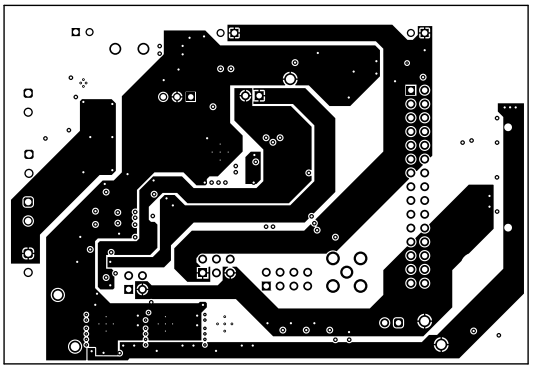


Figure 9-4. Power Layer

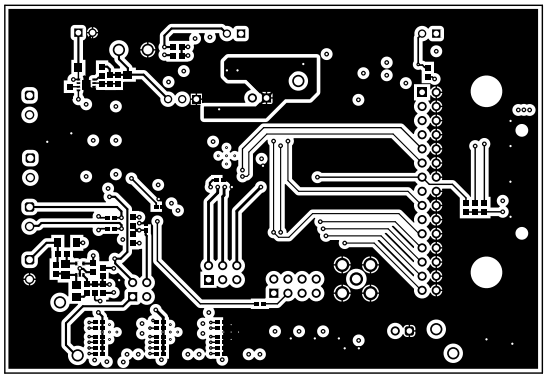


Figure 9-5. Bottom Layer

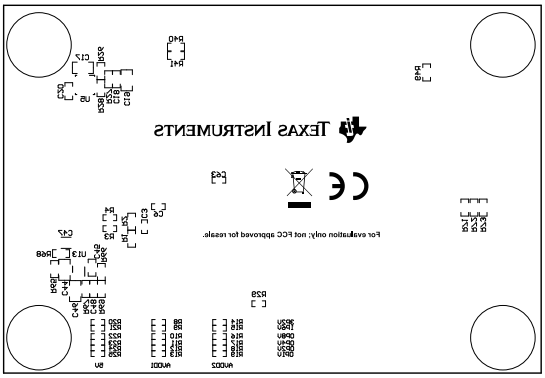


Figure 9-6. Bottom Silkscreen

9.3 Schematics

Figure 9-7 shows a block diagram of the ADS1285EVM-PDK.

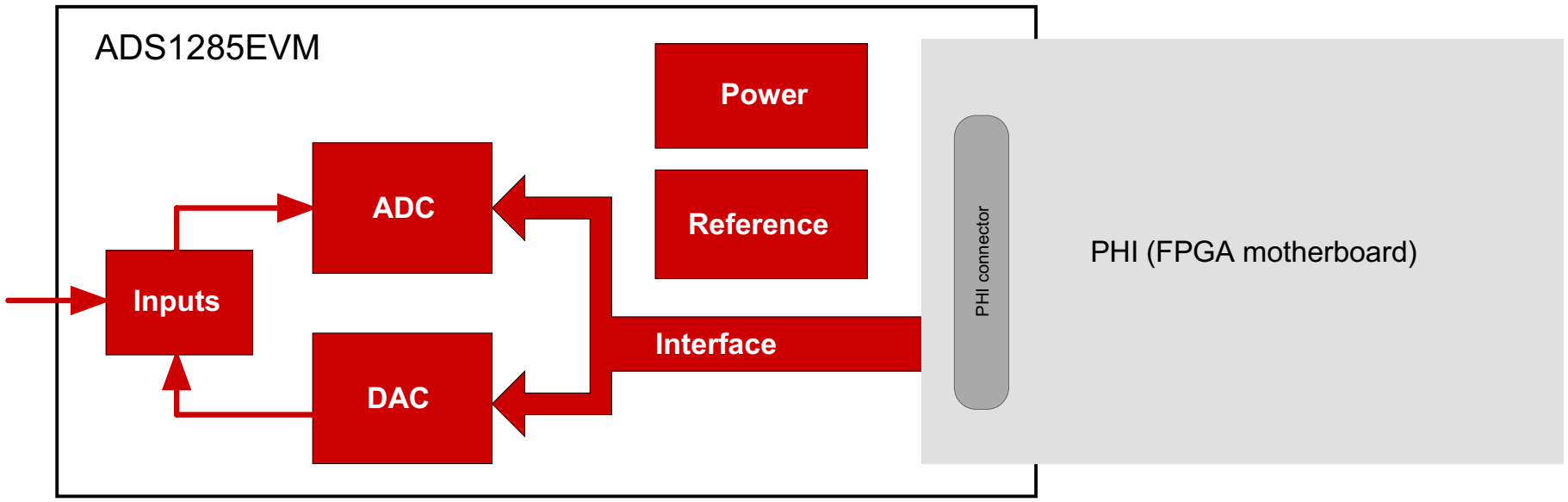
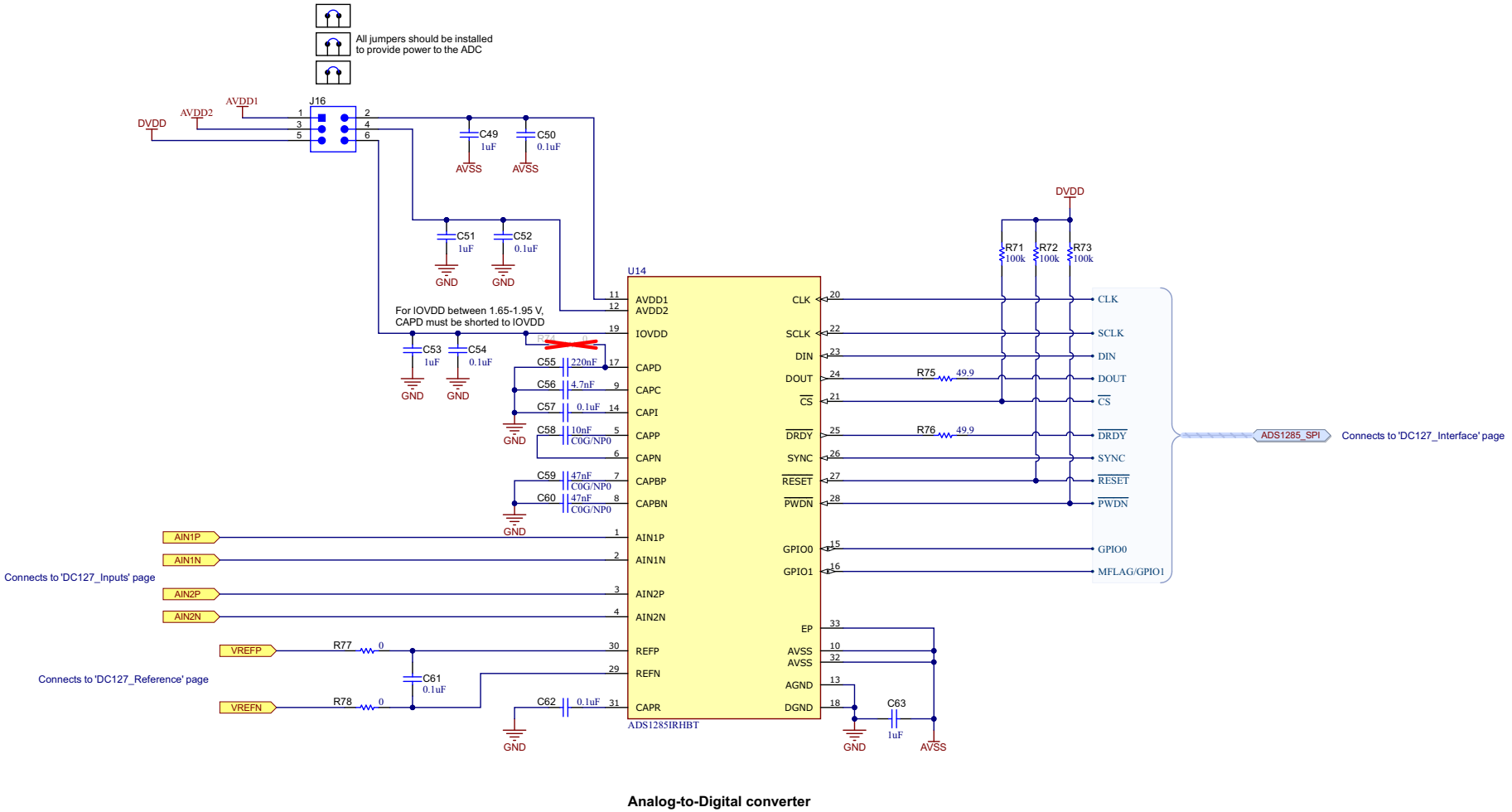


Figure 9-7. ADS1285EVM-PDK Block Diagram

Figure 9-8 through Figure 9-13 illustrate various schematics for the ADS1285EVM-PDK ADC.



Analog-to-Digital converter

Figure 9-8. ADS1285EVM-PDK ADC Schematic

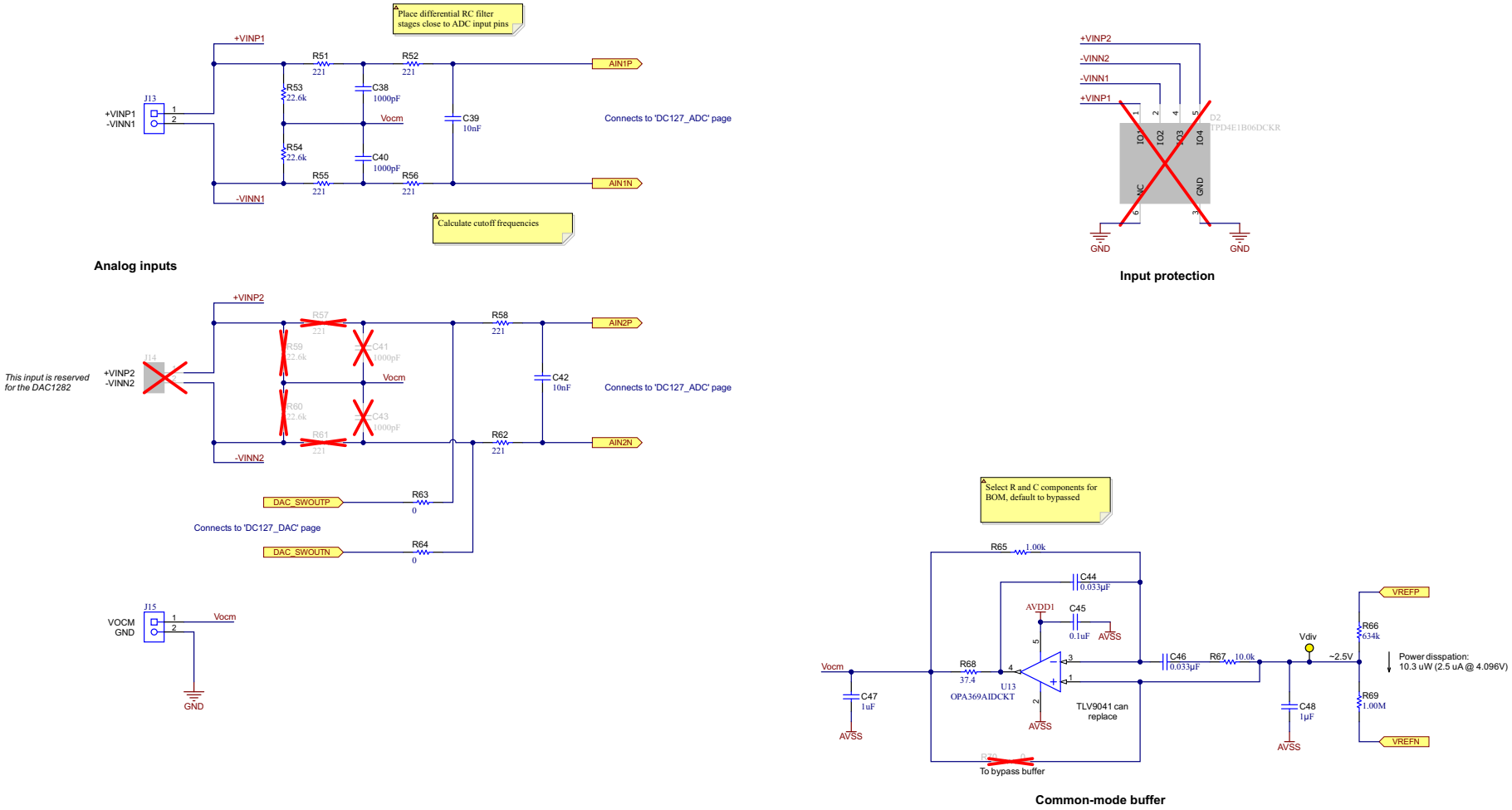


Figure 9-9. ADS1285EVM-PDK Analog Inputs and Common-Mode Buffer Schematic

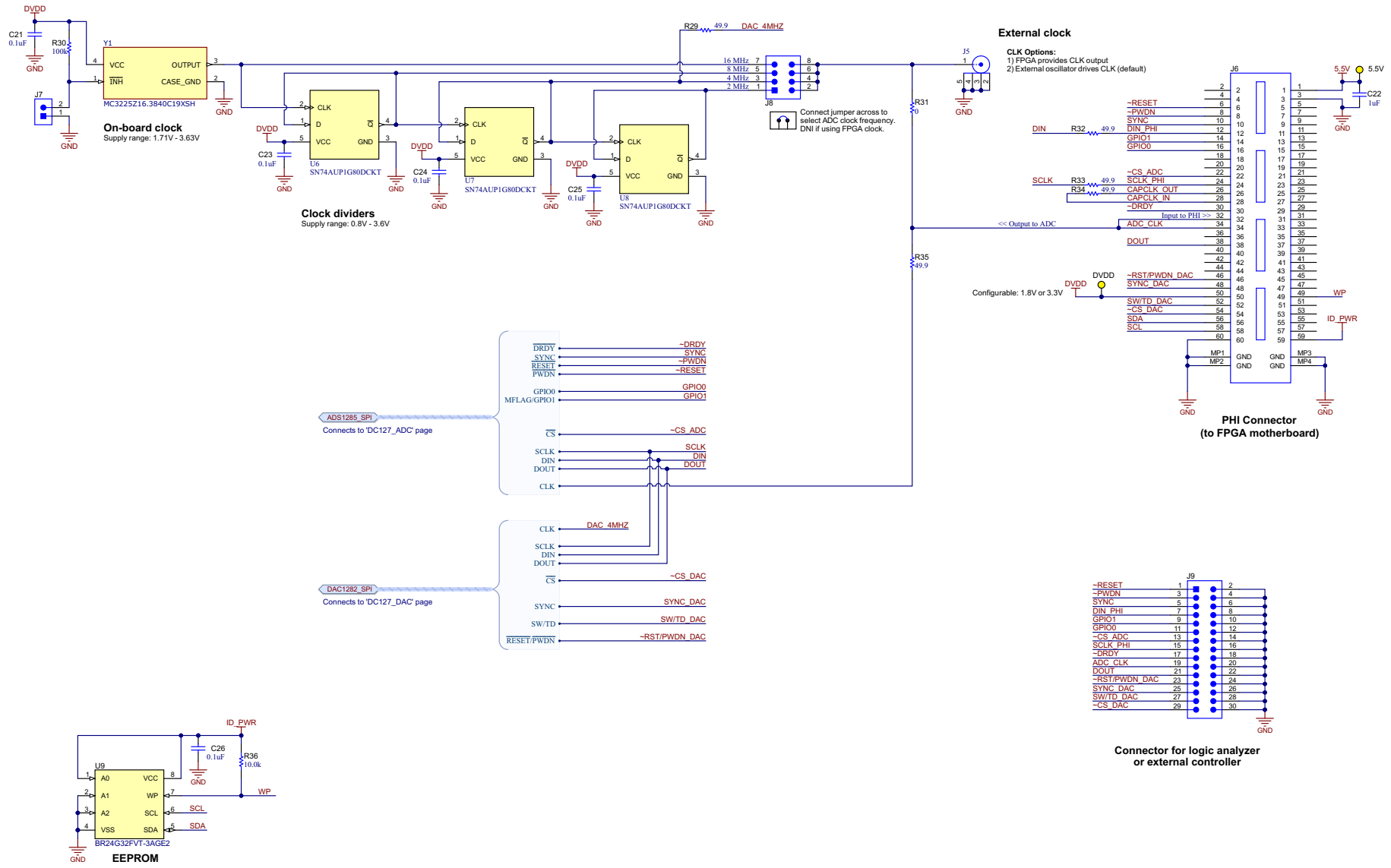
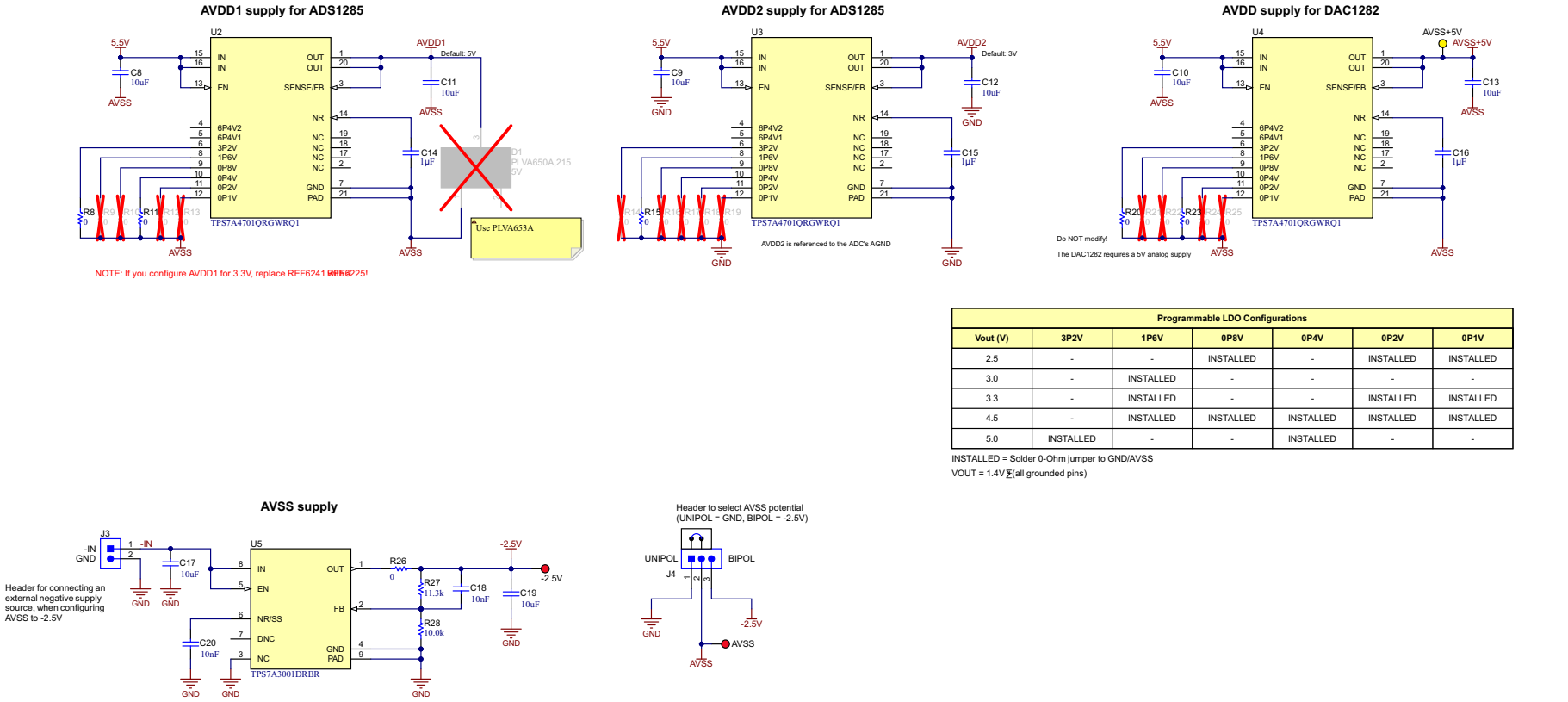


Figure 9-10. ADS1285EVM-PDK Clock and Interface Schematic



Programmable LDO Configurations						
Vout (V)	**3P2V**	**1P6V**	**0P8V**	**0P4V**	**0P2V**	**0P1V**
2.5	-	-	INSTALLED	-	INSTALLED	INSTALLED
3.0	-	INSTALLED	-	-	-	-
3.3	-	INSTALLED	-	-	INSTALLED	INSTALLED
4.5	-	INSTALLED	INSTALLED	INSTALLED	INSTALLED	INSTALLED
5.0	INSTALLED	-	-	INSTALLED	-	-

INSTALLED = Solder 0-Ohm jumper to GND/AVSS
VOUT = 1.4V ∑(all grounded pins)

Figure 9-11. ADS1285EVM-PDK Power-Supply Schematic

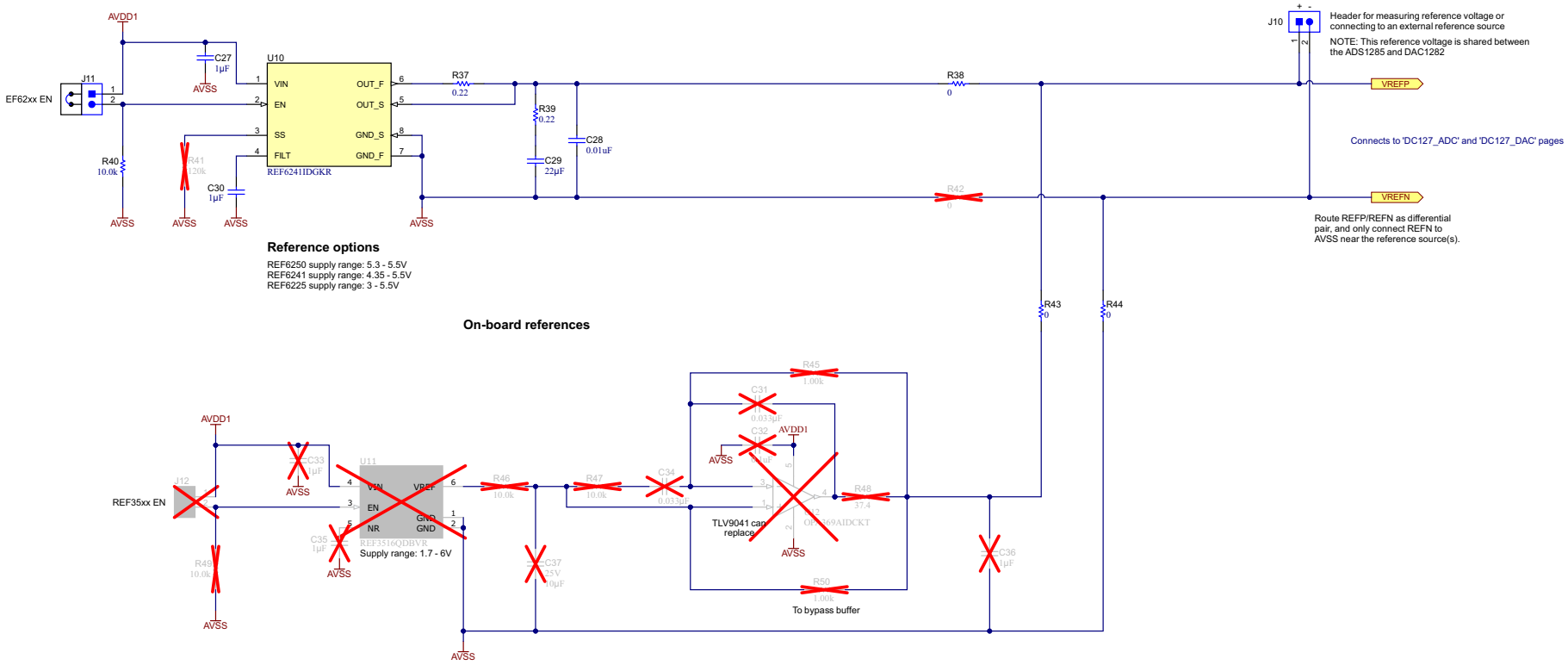


Figure 9-12. ADS1285EVM-PDK Reference Voltage Schematic

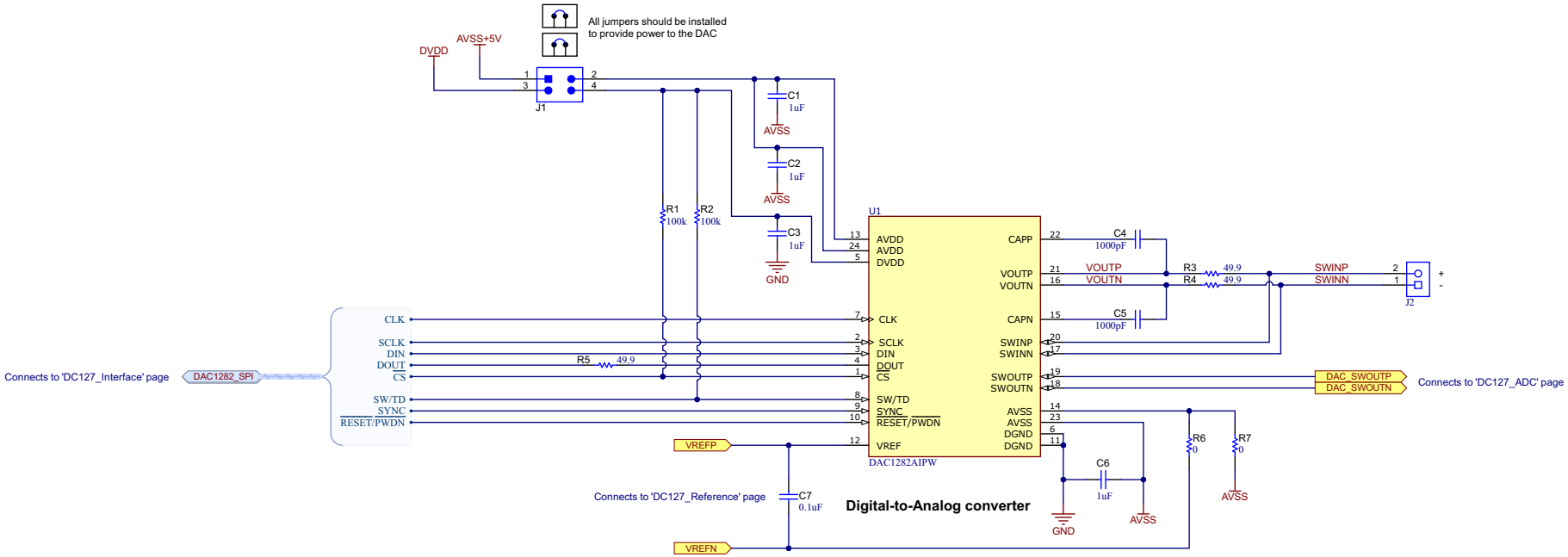


Figure 9-13. ADS1285EVM DAC Schematic

10 References

- Texas Instruments, *DAC1282 Low Distortion Digital-to-Analog Converter for Seismic* data sheet
- Texas Instruments, *REF62xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* data sheet

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265