SBAS178B – DECEMBER 2000 – REVISED MAY 2002

Dual, 12-Bit, 32MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **SPURIOUS-FREE DYNAMIC RANGE: 73dB at 10MHz f_{IN}**
- **HIGH SNR: 67dB (2Vp-p), 69dB (3Vp-p)**
- **INTERNAL OR EXTERNAL REFERENCE**
- **LOW DLE: ±0.4LSB**
- **FLEXIBLE INPUT RANGE: 2Vp-p to 3Vp-p**
- **TQFP-64 POWER PACKAGE**

APPLICATIONS

- **COMMUNICATIONS IF PROCESSING**
- **COMMUNICATIONS BASESTATIONS**
- **TEST EQUIPMENT**
- **MEDICAL IMAGING**
- **VIDEO DIGITIZING**
- **CCD DIGITIZING**

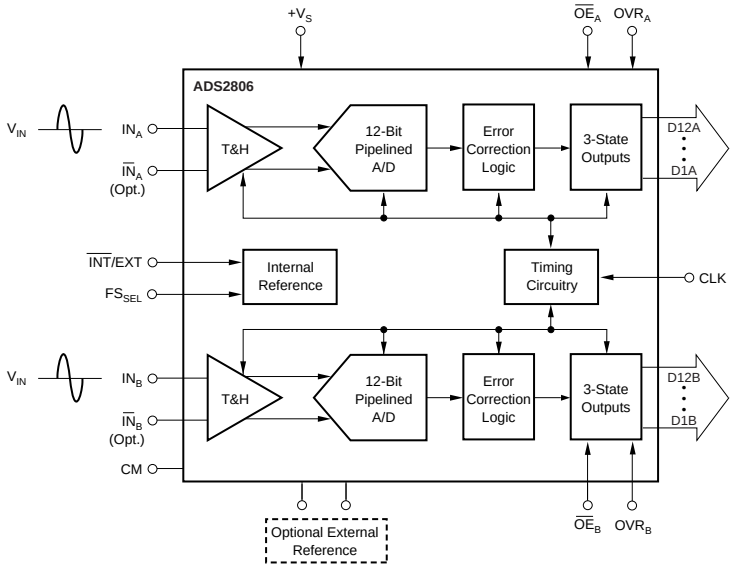
DESCRIPTION

The ADS2806 is a dual, high-speed, high dynamic range, 12-bit pipelined Analog-to-Digital Converter (ADC). This converter includes a high-bandwidth track-and-hold that gives excellent spurious performance up to and beyond the Nyquist rate. The differential nature of this track-and-hold and ADC circuitry minimizes even-order harmonics and gives excellent common-mode noise immunity. The track-and-hold can also be operated single-ended.

The ADS2806 provides for setting the full-scale range of the converter without any external reference circuitry. The internal reference can be disabled allowing low drive, external references to be used for improved tracking in multichannel systems.

The ADS2806 provides an over-range indicator flag to indicate an input signal that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of front end gain control circuitry. There is also an output enable pin to allow for multiplexing and testability on a PC board.

The ADS2806 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. The ADS2806 is available in a TQFP-64 power package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	(–0.3V) to ($+V_S$ + 0.3V)
Logic Input	(–0.3V) to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS2806Y	TQFP-64	PAP	–40°C to +85°C	ADS2806Y	ADS2806Y/1K5	Tape and Reel, 1500
"	"	"	"	"	ADS2806Y/250	Tape and Reel, 250

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 32MSPS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS2806Y MIN	ADS2806Y TYP	ADS2806Y MAX	UNITS
RESOLUTION			12 Tested		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air	–40		+85	°C
ANALOG INPUT					
2V Full-Scale Input Range (Differential)	2Vp-p, INT or EXT Ref	2		3	V
2V Full-Scale Input Range (Single-Ended)	2Vp-p, INT or EXT Ref	1.5		3.5	V
3V Full-Scale Input Range (Differential)	3Vp-p, INT or EXT Ref	1.75		3.25	V
3V Full-Scale Input Range (Single-Ended)	3Vp-p, INT or EXT Ref	1		4	V
Analog Input Bias Current			1		µA
Analog Input Bandwidth			270		MHz
Input Impedance			1.25 || 3		MΩ || pF
CONVERSION CHARACTERISTICS					
Sample Rate		10k		32	Samples/s
Data Latency			6		Clock Cycles
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.35	±1.0	LSB
f = 10MHz			±0.4		LSB
No Missing Codes			Tested		
Integral Linearity Error, f = 1MHz			±2.5	±4.0	LSBs
Spurious-Free Dynamic Range[1]					
f = 1MHz (–1dB input)			73		dBFS[2]
f = 10MHz (–1dB input)		67	73		dBFS
2-Tone Intermodulation Distortion[3]					
f = 9MHz and 10MHz (–7dB each tone)			–74.6		dBc
Signal-to-Noise Ratio (SNR)					
f = 1MHz (–1dB input)			67		dBFS
f = 10MHz (–1dB input)		63	66		dBFS
f = 1MHz (–1dB input)	3Vp-p		69		dBFS
f = 10MHz (–1dB input)	3Vp-p		68		dBFS
Signal-to-(Noise + Distortion) (SINAD)[4]					
f = 1MHz (–1dBFS input)			66		dBFS
f = 10MHz (–1dBFS input)		61	65		dBFS
f = 1MHz (–1dBFS input)	3Vp-p		69		dBFS
f = 10MHz (–1dBFS Input)	3Vp-p		69		dBFS

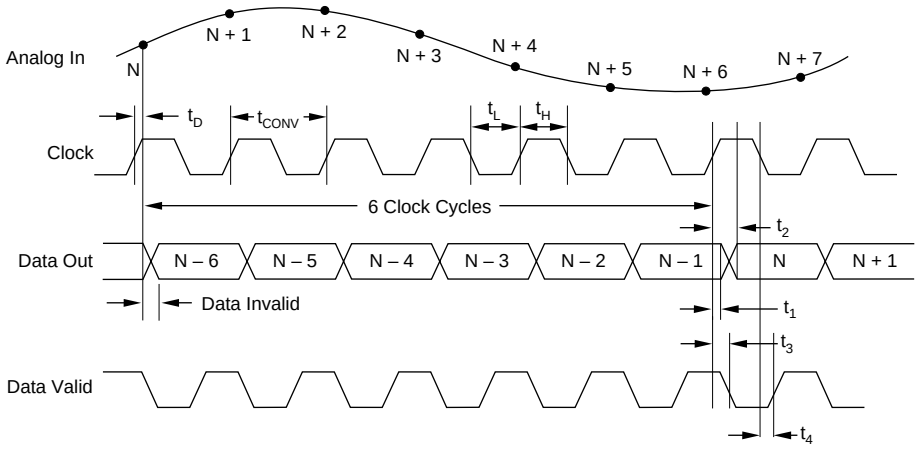
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 32MSPS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS2806Y MIN	ADS2806Y TYP	ADS2806Y MAX	UNITS
DYNAMIC CHARACTERISTICS (Cont.)					
Channel-to-Channel Crosstalk	2Vp-p		80		dBc
Output Noise	Input Grounded		0.2		LSBs rms
Aperture Delay Time			2		ns
Aperture Jitter			1.2		ps rms
Overvoltage Recovery Time			2		ns
DIGITAL INPUTS					
Logic Family			+3V/+5V CMOS Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = 5V)				+50	µA
Low Level Input Current (V_{IN} = 0V)				+10	µA
High Level Input Voltage		+2.4			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA)	VDRV = 5V			+0.1	V
Low Output Voltage, (I_{OL} = 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage, (I_{OH} = 50µA)	VDRV = 5V	+4.9			V
High Output Voltage, (I_{OH} = 0.5mA)	VDRV = 5V	+4.8			V
Low Output Voltage, (I_{OL} = 50µA)	VDRV = 3V			+0.4	V
High Output Voltage, (I_{OH} = 50µA)	VDRV = 3V	+2.4			V
3-State Enable Time	$\overline{OE}$ = L[5]		20	40	ns
3-State Disable Time	$\overline{OE}$ = H[5]		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)					
Zero Error (Midscale)	at 25°C		±0.5		%FS
Zero Error Drift (Midscale)			16		ppm/°C
Gain Error[6]	at 25°C		±1.5		%FS
Gain Error Drift[6]			66		ppm/°C
Gain Error[7]	at 25°C		±1.0		%FS
Gain Error Drift[7]			23		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		70		dB
REFT Tolerance					
2V Full Scale	Deviation From Ideal 3.0V		±10	±65	mV
3V Full Scale	Deviation From Ideal 3.25V		±20		mV
REFB Tolerance					
2V Full Scale	Deviation From Ideal 2.0V		±10	±65	mV
3V Full Scale	Deviation From Ideal 1.75V		±20		mV
External REFT Voltage Range		REFB + 0.4	3	V_S – 1.70	V
External REFB Voltage Range		1.70	2	REFT – 0.4	V
Reference Input Resistance			375		Ω
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		78		mA
Power Dissipation: VDRV = 5V	External Reference		430		mW
VDRV = 3V	External Reference		400		mW
VDRV = 5V	Internal Reference		450		mW
VDRV = 3V	Internal Reference		420	475	mW
Thermal Resistance, θ_{JA}					
TQFP-64			21.5		°C/W

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full-Scale. (3) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by as (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pins. (6) Includes internal reference. (7) Excludes internal reference.

TIMING DIAGRAM

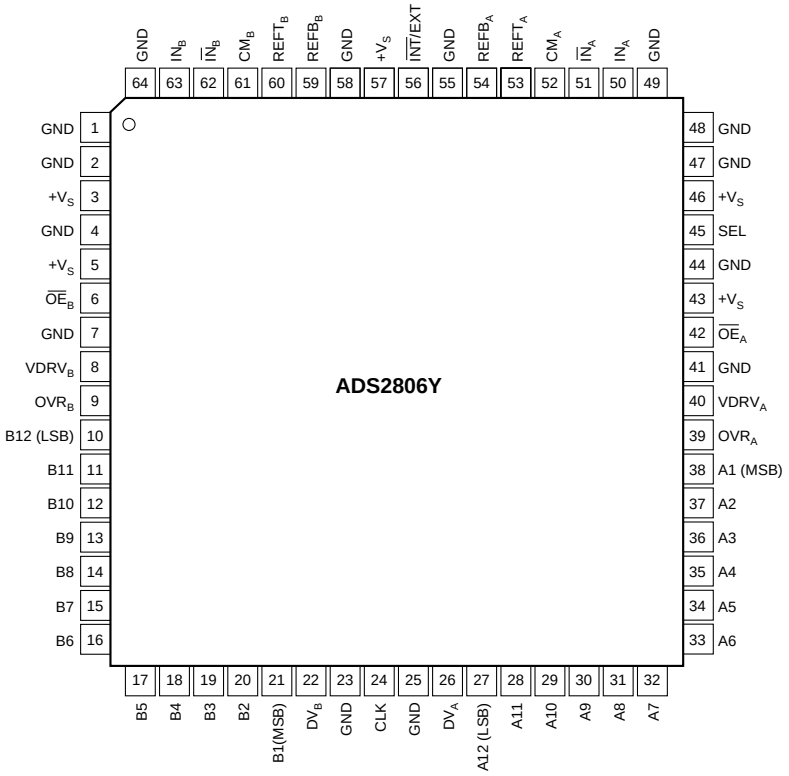


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	31.25		100µs	ns
t_L	Clock Pulse Low	14.6	$t_{CONV}/2$		ns
t_H	Clock Pulse High	14.6	$t_{CONV}/2$		ns
t_D	Aperture Delay		2		ns
t_1(1)	Data Hold Time, C_L = 0pF	2.7			ns
t_2(1)	New Data Delay Time, C_L = 15pF max		8.2	12	ns
t_3	Data Valid Falling Edge Delay, C_L = 15pF max		7.5		ns
t_4	Data Valid Rising Edge Delay, C_L = 15pF max		5.6		ns

NOTE: (1) t_1 and t_2 times are valid for VDRV voltages of +2.7V to +5V.

PIN CONFIGURATION

Top View **TQFP**



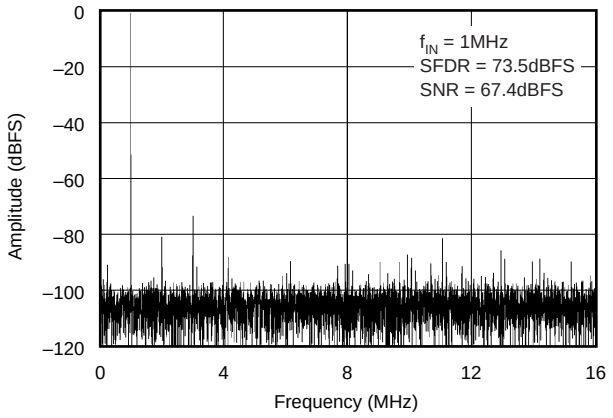
PIN DESCRIPTIONS

PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		GND	Ground	34	O	A5	Data Bit 5 (D7), Channel A
2		GND	Ground	35	O	A4	Data Bit 4 (D8), Channel A
3		$+V_S$	+5V Supply	36	O	A3	Data Bit 3 (D9), Channel A
4		GND	Ground	37	O	A2	Data Bit 2 (D10), Channel A
5		$+V_S$	+5V Supply	38	O	A1 (MSB)	Data Bit 1 (D11), Channel A
6	I	$\overline{OE}_B$	Output Enable, Channel B	39	O	OVR_A	Over-Range Indicator, Channel A
7		GND	GND	40		$VDRV_A$	Logic Driver Supply Voltage, Channel A
8		$VDRV_B$	Logic Driver Supply Voltage, Channel B	41		GND	Ground
9	O	OVR_B	Over-Range Indicator, Channel B	42	I	$\overline{OE}_A$	Output Enable, Channel A
10	O	B12 (LSB)	Data Bit 12 (D0), Channel B	43		$+V_S$	+5V Supply
11	O	B11	Data Bit 11 (D1), Channel B	44		GND	Ground
12	O	B10	Data Bit 10 (D2), Channel B	45	I	SEL	Input Range Select: HIGH = 3V, LOW = 2V
13	O	B9	Data Bit 9 (D3), Channel B	46		$+V_S$	+5V Supply
14	O	B8	Data Bit 8 (D4), Channel B	47		GND	Ground
15	O	B7	Data Bit 7 (D5), Channel B	48		GND	Ground
16	O	B6	Data Bit 6 (D6), Channel B	49		GND	Ground
17	O	B5	Data Bit 5 (D7), Channel B	50	I	IN_A	Analog Input, Channel A
18	O	B4	Data Bit 4 (D8), Channel B	51	I	$\overline{IN}_A$	Complementary Analog Input, Channel A
19	O	B3	Data Bit 3 (D9), Channel B	52	O	CM_A	Common-Mode, Channel A
20	O	B2	Data Bit 2 (D10), Channel B	53	I/O	$REFT_A$	Top Reference/Bypass, Channel A
21	O	B1 (MSB)	Data Bit 1 (D11), Channel B	54	I/O	$REFB_A$	Bottom Reference/Bypass, Channel A
22	O	DV_B	Data Valid, Channel B	55		GND	Ground
23		GND	Ground	56	I	$\overline{INT}$/EXT	Reference Select: HIGH = External, LOW = Internal 50kΩ Pull-Up Resistor
24	I	CLK	Clock	57		$+V_S$	+5V Supply
25		GND	Ground	58		GND	Ground
26	O	DV_A	Data Valid, Channel A	59	I/O	$REFB_B$	Bottom Reference/Bypass, Channel B
27	O	A12 (LSB)	Data Bit 12 (D0), Channel A	60	I/O	$REFT_B$	Top Reference/Bypass, Channel B
28	O	A11	Data Bit 11 (D1), Channel A	61	O	CM_B	Common-Mode, Channel B
29	O	A10	Data Bit 10 (D2), Channel A	62	I	$\overline{IN}_B$	Complementary Analog Input, Channel B
30	O	A9	Data Bit 9 (D3), Channel A	63	I	IN_B	Analog Input, Channel B
31	O	A8	Data Bit 8 (D4), Channel A	64		GND	Ground
32	O	A7	Data Bit 7 (D5), Channel A				
33	O	A6	Data Bit 6 (D6), Channel A				

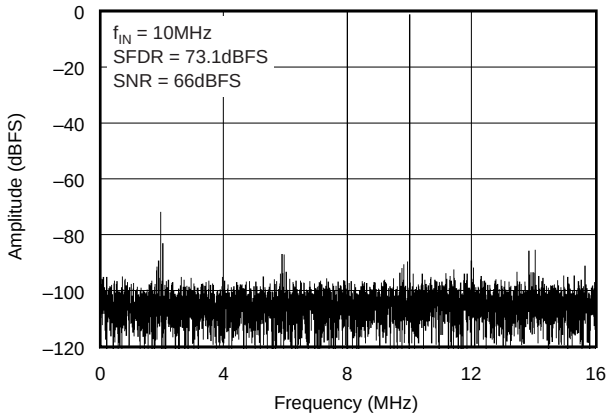
TYPICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 32MSPS, unless otherwise noted.

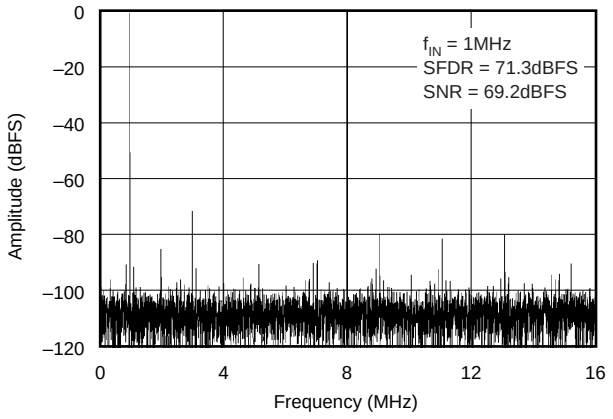
SPECTRAL PERFORMANCE
(Differential, 2Vp-p)



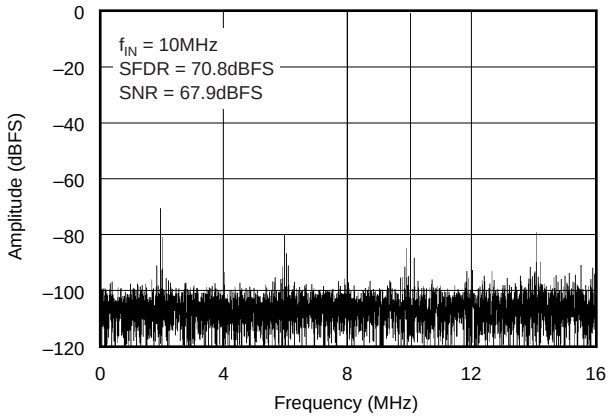
SPECTRAL PERFORMANCE
(Differential, 2Vp-p)



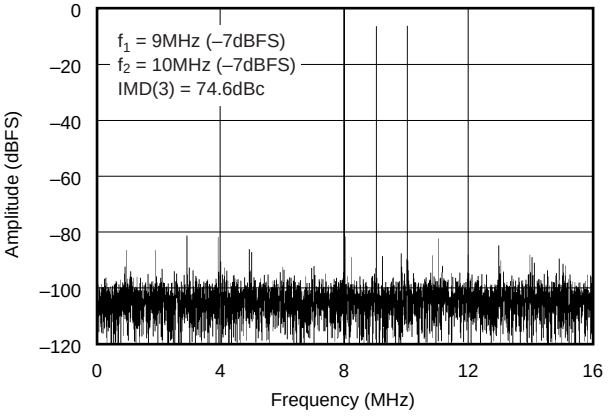
SPECTRAL PERFORMANCE
(Differential, 3Vp-p)



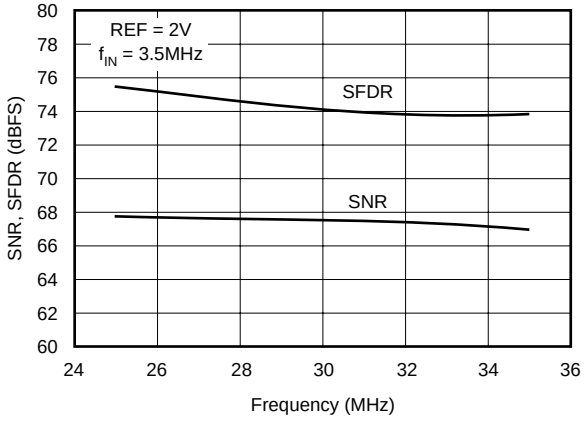
SPECTRAL PERFORMANCE
(Differential, 3Vp-p)



2-TONE INTERMODULATION DISTORTION



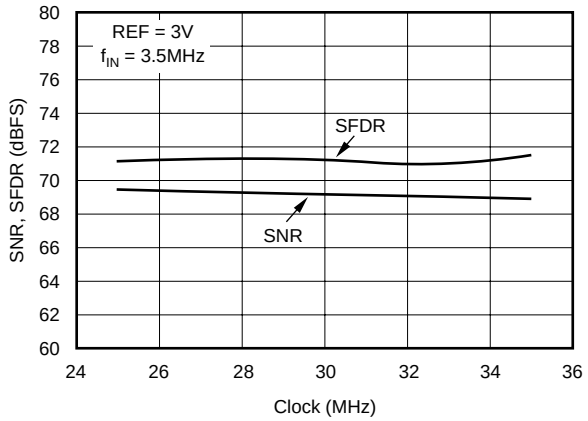
DYNAMIC PERFORMANCE vs CLOCK



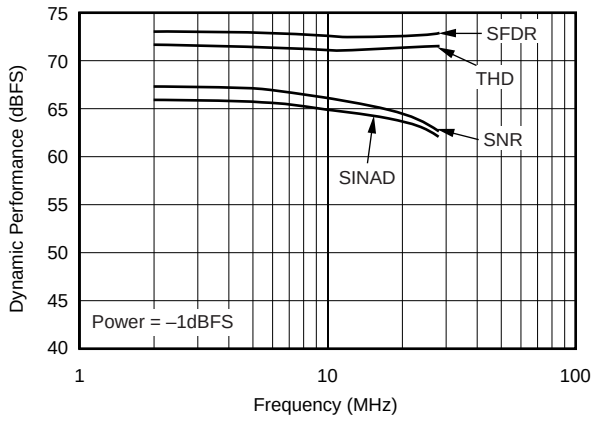
TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 32MSPS, unless otherwise noted.

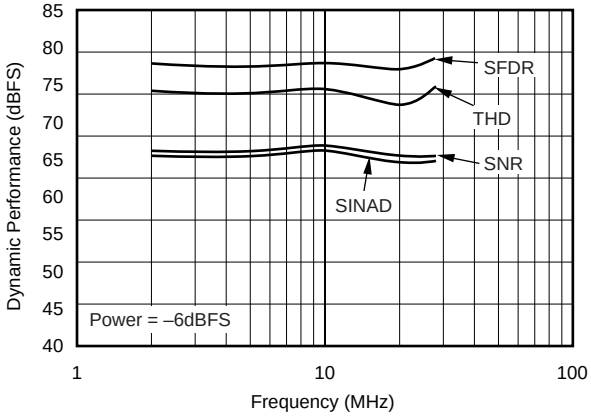
DYNAMIC PERFORMANCE vs CLOCK



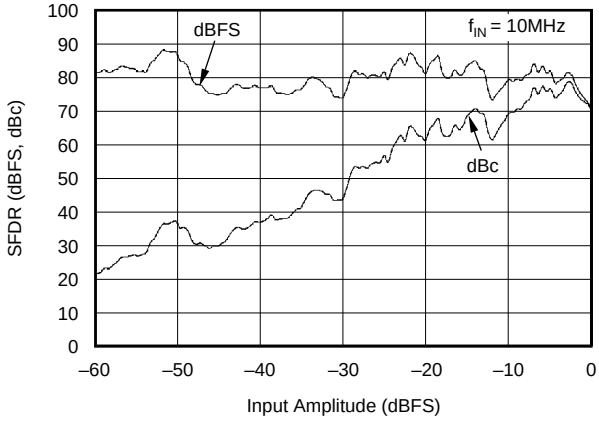
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



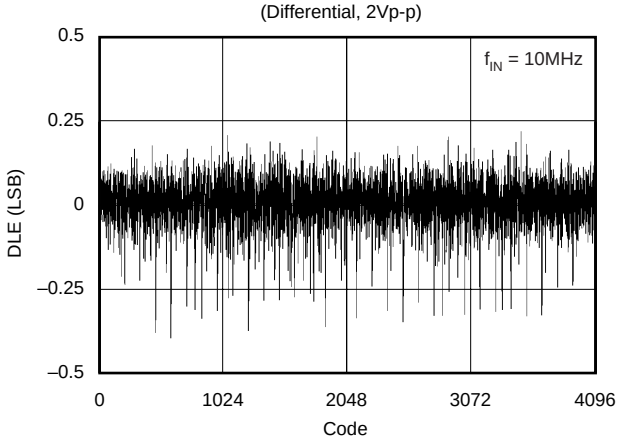
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



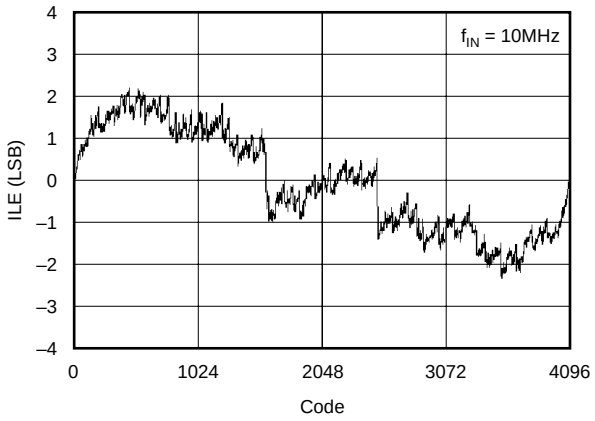
SWEPT POWER (SFDR)



DIFFERENTIAL LINEARITY ERROR
(Differential, 2Vp-p)



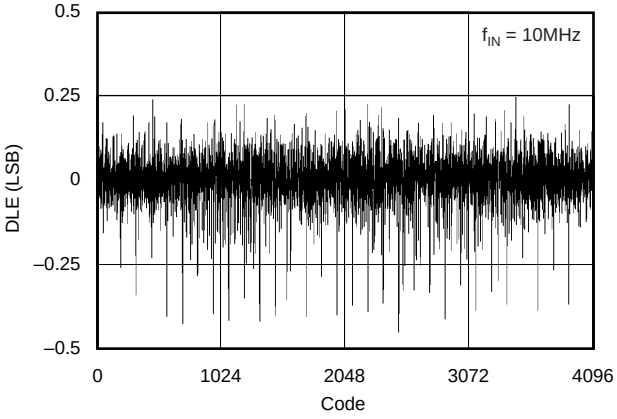
INTEGRAL LINEARITY ERROR
(Differential, 2Vp-p)



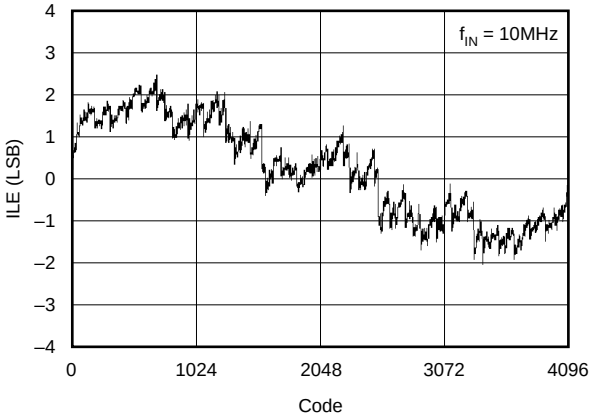
TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 32MSPS, unless otherwise noted.

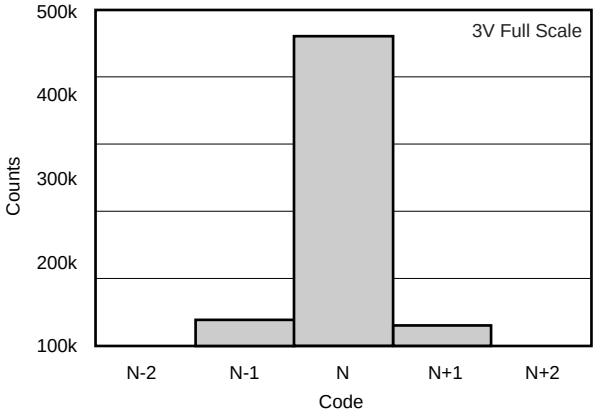
DIFFERENTIAL LINEARITY ERROR
(Differential, 3Vp-p)



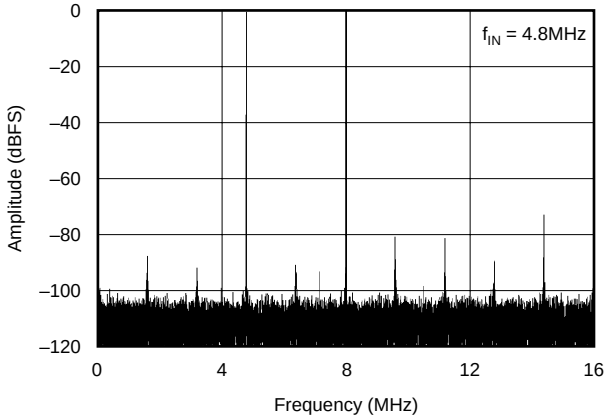
INTEGRAL LINEARITY ERROR
(Differential, 3Vp-p)



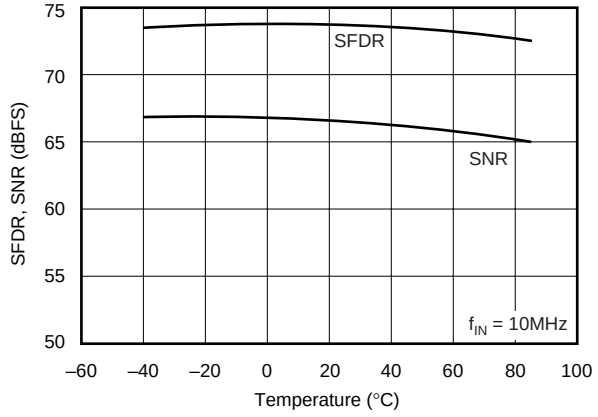
OUTPUT NOISE HISTOGRAM (DC Input)



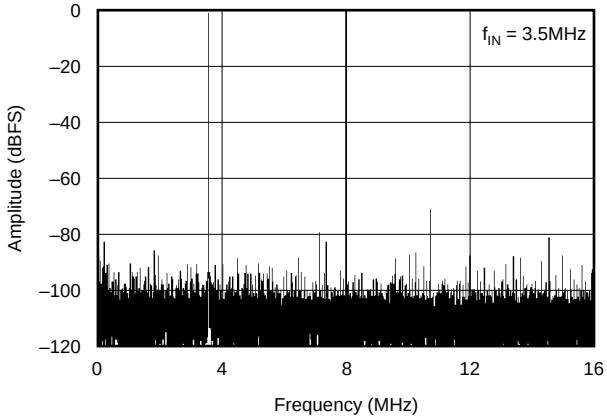
CROSSTALK (Channel A)



DYNAMIC PERFORMANCE vs TEMPERATURE



CROSSTALK (Channel B)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS2806 integrates two high-speed CMOS ADCs and an internal reference. The ADCs utilize a pipelined converter architecture consisting of 11 internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level. The output data becomes valid after the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 6 clock cycles.

The analog input of the ADS2806 consists of a differential track-and-hold circuit. The differential topology along with tightly matched poly-poly capacitors produce a high level of AC performance at high sampling rates and in some under-sampling applications.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

DRIVING THE ANALOG INPUTS

The analog inputs of the ADS2806 are very high impedance and should be driven through an R-C network designed to pass the highest frequency of interest. This prevents high-frequency noise in the input from affecting SFDR and SNR. The ADS2806 can be used in a wide variety of applications and deciding on the best performing analog interface circuit depends on the type of application. The circuit definition should include considerations of input frequency spectrum and amplitude, single-ended or differential drive, and available power supplies. For example, communication (frequency domain) applications process frequency bands not including DC. In imaging (time domain) applications, the input DC component must be maintained into the ADC. Features of the ADS2806 include full-scale select (SEL), external reference, and CM output, providing flexibility to accommodate a wide range of applications. The ADS2806 should be configured to meet application objectives, while observing the headroom requirements of the driving amplifiers, to yield the best overall performance.

The ADS2806 input structure allows it to be driven either single-ended or differentially. Differential operation of the ADS2806 requires an in-phase input signal and a 180° out-of-phase part simultaneously applied to the inputs (IN, $\overline{IN}$). The differential operation offers a number of advantages that, in most applications, will be instrumental in achieving the best dynamic performance of the ADS2806:

- The signal swing is half of that required for the single-ended operation and, therefore, is less demanding to achieve while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom in the interface circuitry and, therefore, a wider selection of the best suitable driver op amp.
- Even-order harmonics are minimized.
- Improves the noise immunity based on the converter's common-mode input rejection.

Using the single-ended mode, the signal is applied to one of the inputs, while the other input is biased with a DC voltage to the required common-mode level. Both inputs are equal in terms of their impedance and performance, except that applying the signal to the complementary input ($\overline{IN}$) instead of the IN input will invert the input signal relative to the output code. For example, in the case when the input driver operates in inverting mode, using $\overline{IN}$ as the signal input will restore the phase of the signal to its original orientation. Time-domain applications may benefit from a single-ended interface configuration and its reduced circuit complexity. Driving the ADS2806 with a single-ended signal will result in a reduction of the distortion performance, while maintaining good Signal-to-Noise Ratio (SNR). Employing dual-supply amplifiers and AC-coupling will usually yield the best results, while DC-coupling and/or single-supply amplifiers impose additional design constraints due to their headroom requirements, especially when selecting the 3Vp-p input range. However, single-supply amplifiers have the advantage of inherently limiting their output swing to within the supply rails. Alternatively, a voltage limiting amplifier, like the OPA688, may be considered to set fixed-signal limits and avoid any severe over-range condition for the ADC.

The full-scale input range of the ADS2806 is defined by the reference voltages. For example, setting the range select pin to SEL = LOW, and using the internal references (REFT = +3.0V and REFTB = +2.0V), the full-scale range is defined as: FSR = 2 • (REFT – REFB) = 2Vp-p.

The trade-off of the differential input configuration versus the single-ended is its higher complexity. In either case, the selection of the driver amplifier should be such that the amplifier's performance will not degrade the ADC's performance. The ADS2806 operates on a single power supply that requires a level shift for ground-based bipolar input signals to comply with its input voltage range requirements.

The input of the ADS2806 is of a capacitive nature and the driving source needs to provide the current to charge or discharge the input sampling capacitor while the track-and-hold is in track mode. This effectively results in a dynamic input impedance that depends on the sampling frequency. In most applications, it is recommended to add a series resistor, typically 20Ω to 50Ω, between the drive source and the converter inputs. This will isolate the capacitive input from the source, which can be crucial to avoid gain peaking when using wideband operational amplifiers. Secondly, it

will create a 1st-order, low-pass filter in conjunction with the specified input capacitance of the ADS2806. Its cutoff frequency can be adjusted even further by adding an external shunt capacitor from each signal input to ground. The optimum values of this R-C network depend on a variety of factors that include the ADS2806 sampling rate, the selected op amp, the interface configuration, and the particular application (time domain versus frequency domain). Generally, increasing the size of the series resistor and/or capacitor will improve the SNR performance, but depending on the signal source, large resistor values may be detrimental to achieving good harmonic distortion. In any case, optimizing the R-C values for the specific application is encouraged.

Transformer Coupled, Single-Ended to Differential Configuration

If the application requires a signal conversion from a single-ended source to drive the ADS2806 differentially, an RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to improved distortion performance.

The differential input configuration provides the noticeable advantage of achieving high SFDR over a wide range of input frequencies. In this mode, both inputs of the ADS2806 see matched impedances. Figure 1 shows the schematic for the suggested transformer coupled interface circuit. The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \bullet R_G$ to match the source impedance (R_G) for good power transfer and VSWR.

The circuit example of Figure 1 shows the voltage feedback amplifier OPA680 driving the RF transformer, which converts the single-ended signal into a differential. The OPA680 can be employed for either single- or dual-supply operation. For details on how to optimize its frequency response, refer to the OPA680 data sheet (SBOS083) on our web site at www.ti.com. With the 49.9Ω series output resistor, the amplifier emulates a 50Ω source (R_G). Any DC content of the signal can be easily blocked by a capacitor (0.1µF) to avoid DC loading of the op amp's output stage.

AC-Coupled, Single-Ended to Differential Interface with Dual-Supply Op Amps

Some applications demand a very high dynamic range and low levels of intermodulation distortion, but usually allow the input signal to be AC-coupled into the ADC. Appropriate driver amplifiers need to be selected to maintain the excellent distortion performance of the ADS2806. Often, these op amps deliver the lowest distortion with a small, ground-centered signal swing that requires dual power supplies. Because of the AC-coupling, this requirement can be easily accomplished, and the needed level shifting of the input signal can be implemented without affecting the driver circuit.

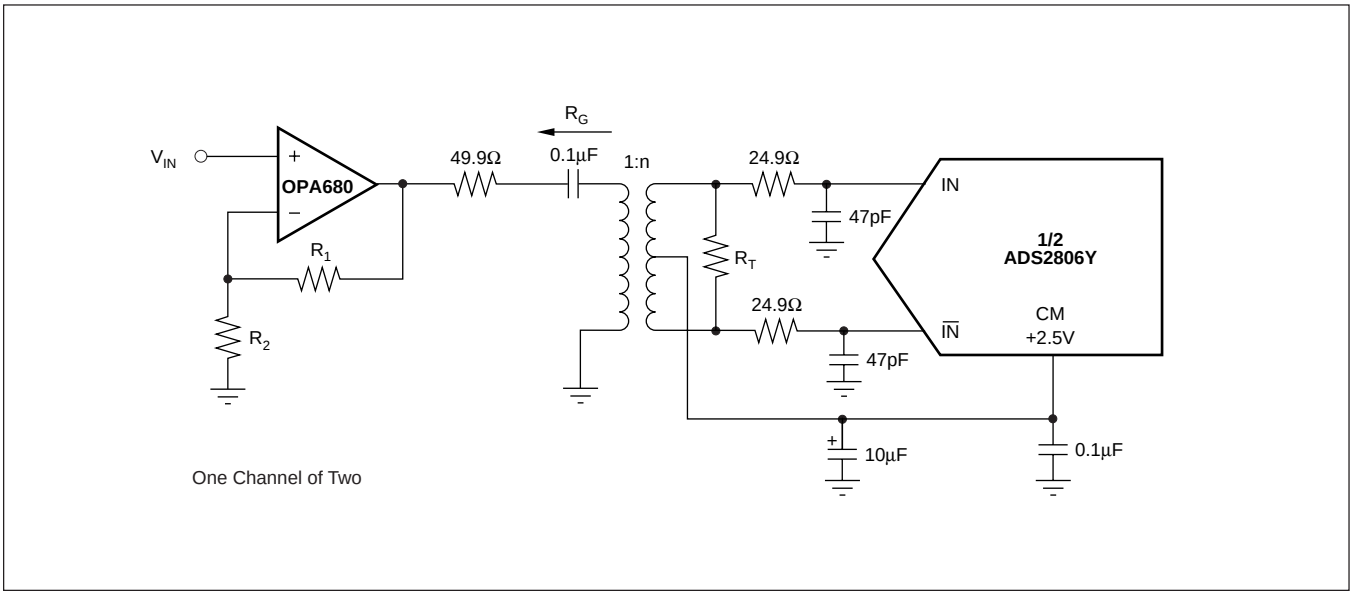


FIGURE 1, Converting a Single-Ended Input Signal into a Differential Signal Using an RF-Transformer.

Figure 2 shows an example of such an interface circuit specifically designed to maximize the dynamic performance. The voltage feedback amplifier, OPA642, maintains an excellent distortion performance for input frequencies of up to 15MHz. The two amplifiers (A1, A2) are configured as an inverting and noninverting gain stage to convert the input signal from single-ended to differential. The nominal gain for this stage is set to +2V/V. The outputs of the OPA642s are AC-coupled to the converter's differential inputs. This will keep the distortion performance at its best since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. Four resistors located between the top (REFT) and bottom (REFB) reference shift the input signal to a common-mode voltage of approximately +2.5V.

The interface circuit of Figure 2 can be modified to extend the bandwidth to approximately 25MHz, by replacing the OPA642 with its decompensated version, the OPA643. The OPA643 provides the necessary slew rate for a low distortion front end to the ADS2806. With a minimum gain stability of +3, the gain resistors have to be modified, as well as optimizing the series resistor and shunt capacitance at each of the converter inputs.

AC-Coupled, Single-Ended-to-Differential Interface for Single-Supply Operation

The previously discussed interface circuit can be modified if the system only allows for a single-supply operation, e.g., V_S = +5V. Single-supply operation requires the driver amplifier to be biased as well in order to process a bipolar input signal. Typically, single-supply amplifiers do not achieve distortion performance as well as dual-supply op amps. The driver amplifier's output swing must exceed the full-scale input range of the converter. In addition, dual op amps, such as the current-feedback OPA2681, should be considered since they provide the closest open-loop gain and phase matching between the two channels. Shown in Figure 3 is a single-supply interface circuit for an AC-coupled input signal. With the ADS2806 set to the 2Vp-p input range, the

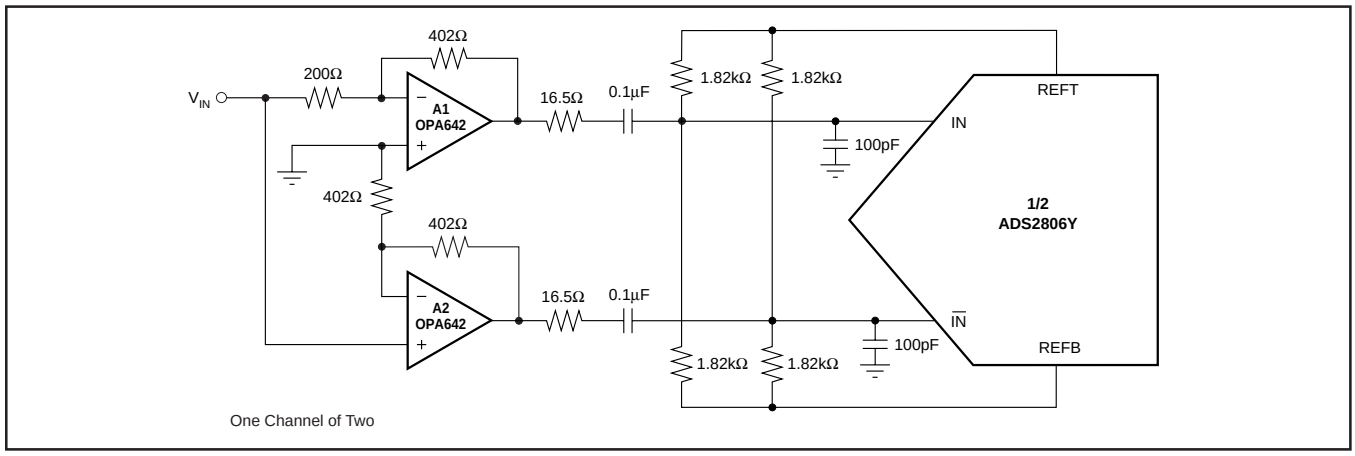


FIGURE 2. AC-Coupled Differential Driver Interface with OPA642.

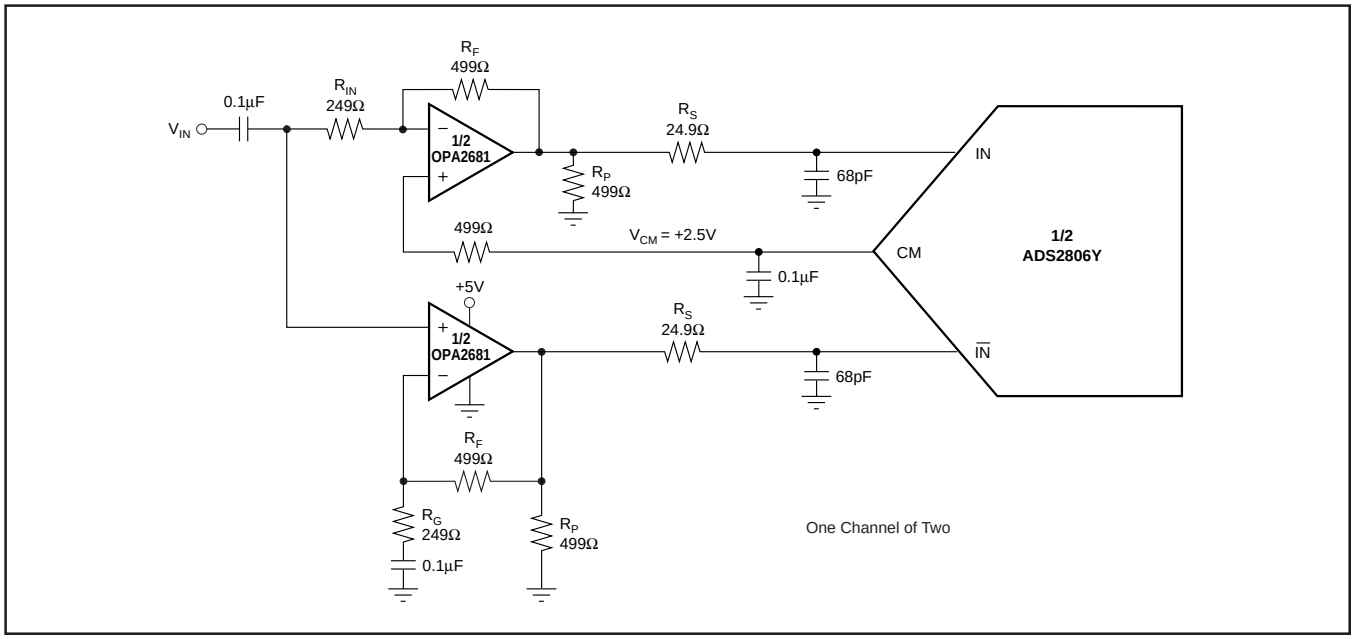


FIGURE 3. AC-Coupled, Differential Interface for Single-Supply Operation.

top and bottom references (REFT, REFB) provide an output voltage of +3.0V and +2.0V, respectively. The CM output of the ADS2806 is used to bias the inputs of the driving amplifiers. Using the OPA2681 on a single +5V supply, its ideal common-mode point is +2.5V, which coincides with the recommended common-mode input level for the ADS2806, thus eliminating the need for coupling capacitors between the amplifiers and the converter.

The addition of a small series resistor (R_S) between the output of the op amps and the input of the ADS2806 will be beneficial in almost all interface configurations. It will decouple the op amp's output from the capacitive load and avoid gain peaking that can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor, in combination with the shunt capacitor, establishes a passive low-pass filter limiting the bandwidth for the wideband noise, thus improving the SNR. The spurious-free dynamic range of this single-supply front end is limited by the 2nd-harmonic distortion. An improvement of several dB may be realized by adding a pull-down resistor (R_P) at the output of each amplifier. This pulls a DC bias current out of the output stage of the amplifier. It is set to approximately 5mA, see Figure 3, but will vary depending on the amplifier used.

Single-Ended, AC-Coupled, Dual-Supply Interface

The circuit provided in Figure 4 shows typical connections for using the ADS2806 in a single-ended input configuration. The bias requirements for AC-coupling are provided by a single resistor to the CM output lead. The single-ended mode of operation should be considered for ease of interface complexity and applications where the dynamic performance can be compromised. The series resistor R_S, along with the shunt capacitance, provide the means to adjust the bandwidth and optimize the performance towards good signal-to-noise ratio. In addition, the amplifier configuration can be easily modified for an anti-aliasing filter based on a 2nd-order Sallen-Key or Multiple-Feedback topology.

The interface example, shown in Figure 4, operates with the full-scale range of the ADS2806 set to 2Vp-p, leaving sufficient headroom for the output of the OPA642 to drive the converter and maintain low signal distortion.

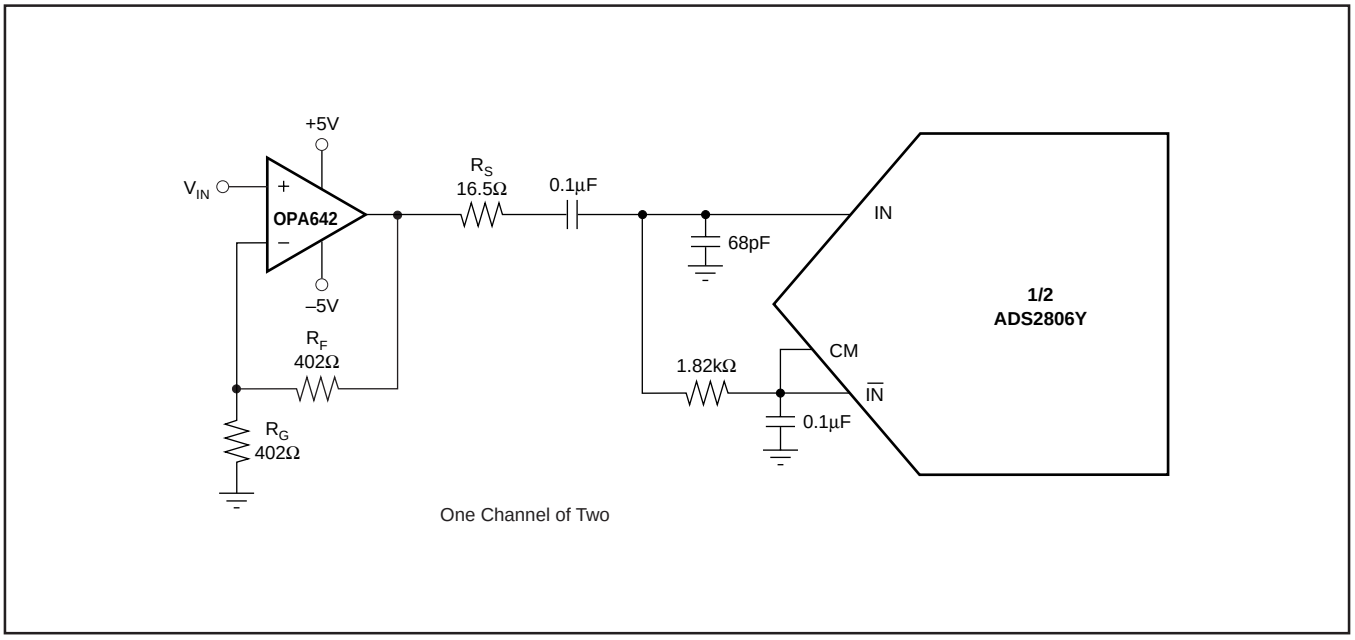


FIGURE 4. AC-Coupling the Dual-Supply Amplifier OPA642 to the ADS2806 for a 2Vp-p Full-Scale Input Range.

DC-Coupled, Differential Driver with Level Shift

Several applications will require that the bandwidth of the signal path include DC, in which case, the signal has to be DC-coupled to the ADC. An op amp based interface circuit can be configured to scale and level shift the input signal to be compatible with the selected input range of the ADC. The circuit shown in Figure 5 employs a dual op amp, OPA2681, to drive the input of the ADS2806 differentially. The single-supply, general-purpose op amp OPA234 is added to buffer the common-mode voltage of +2.5V, available at the CM pin, and apply it to the input of the driver amplifier. This sets the correct DC voltage to bias the inputs of the ADS2806. It should be noted that any DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS2806 will result in an offset error.

Using the OPA2681, this circuit can be operated either with a single or a dual ±5V supply.

REFERENCE OPERATION

The internal reference consists of a bandgap voltage reference, the drivers for the top and bottom reference, and the resistive reference ladder. References are internally connected, e.g.: $REFT_A$ is connected to $REFT_B$, and $REFB_A$ is connected to $REFB_B$. The bandgap reference circuit includes logic functions that allow setting the analog input swing of the ADS2806 to a differential full-scale range of either 2Vp-p or 3Vp-p by simply tying the SEL pin to a LOW or HIGH potential, respectively. While operating the ADS2806 in the external reference mode, the buffer amplifiers for REFT and REFB are disabled. The ADS2806 has an internal 50kΩ pull-down resistor at the range select pin (SEL). Therefore, this pin can be either hardwired to ground or left unconnected, which will default the converter to a 2Vp-p full-scale input range (FSR). While set for the 2Vp-p range, the top and bottom reference voltages will be REFT = +3.0V and REFB = +2.0V. Switching to the 3Vp-p range changes those voltages to REFT = +3.25V and REFB = +1.75V. The reference buffers can be utilized to supply up to 1mA/channel (2mA total, sink and source) to external circuitry. To ensure proper operation with any reference configuration, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum, as shown in Figure 6. Good performance requires using 0.1µF low inductance capacitors. All bypassing capacitors should be located as close to their respective pins as possible.

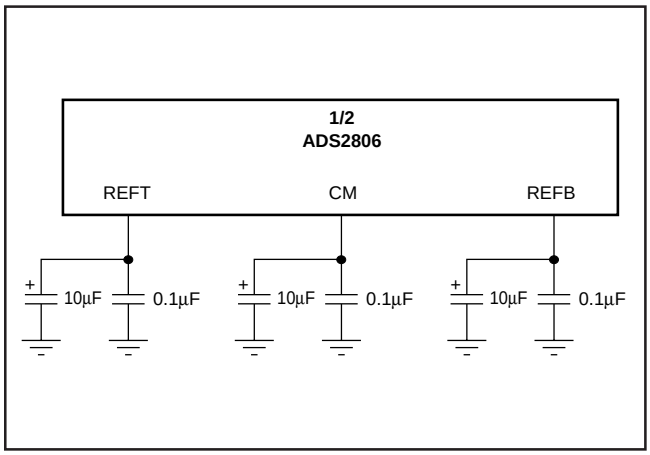


FIGURE 6. Recommended Bypassing for the Reference Pins.

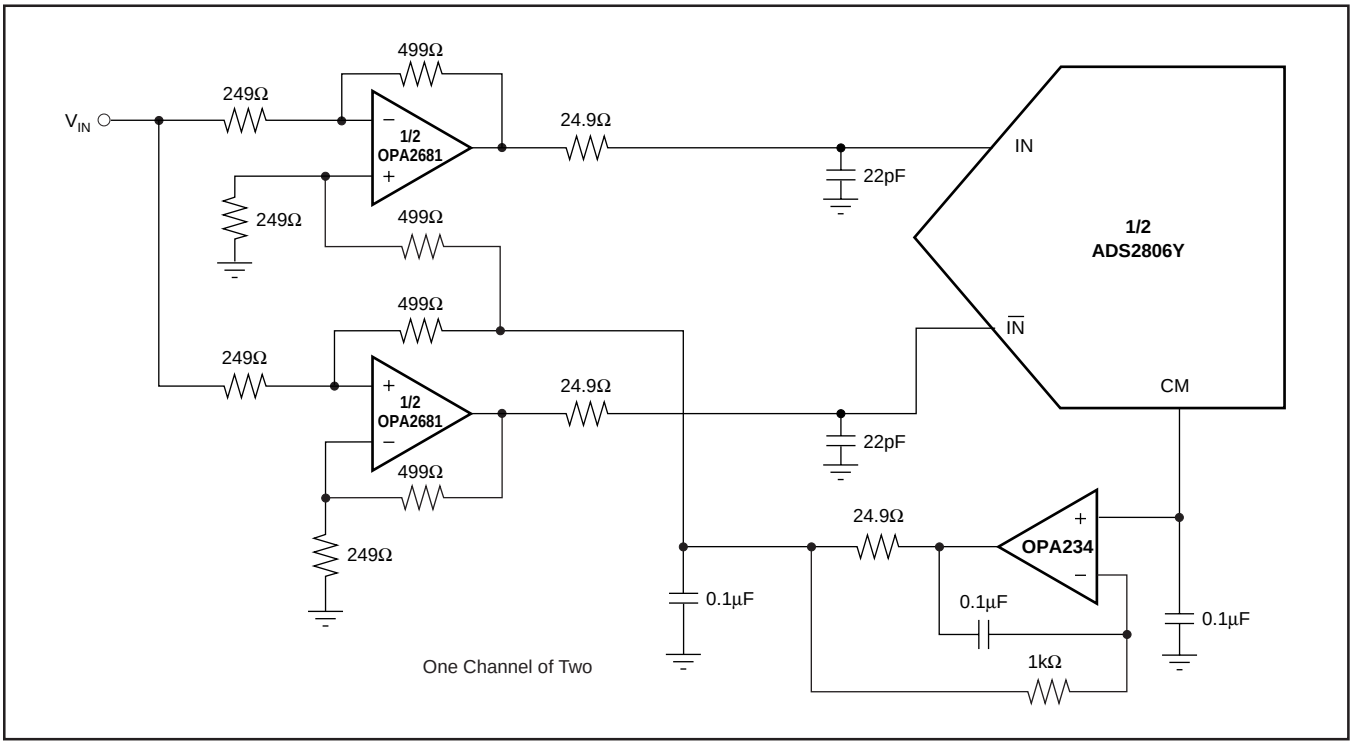


FIGURE 5. DC-Coupled Input Driver with Level Shifting.

USING EXTERNAL REFERENCES

For even more design flexibility, the internal reference can be disabled and an external reference voltage used. Driving both channels with an external reference offers the best performance, as it allows the channels to maintain balance. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. In multichannel applications, the use of a common external reference has the benefit of obtaining better matching and drift of the full-scale range between converters. Figure 7 gives an example of an external reference circuit using a single-supply, low-power, dual op amp (OPA2234).

The external references can vary as long as the value of the external top reference (REFT) stays within the range of V_S – 1.70V and REFB + 0.4V, and the external bottom reference (REFB) stays within 1.70V and REFT – 0.4V. Note that the function of the range selector pin (SEL) is disabled while the converter operates in external reference mode. Setting the ADS2806 for external reference mode requires the $\overline{INT}$/EXT pin (pin 18) to be HIGH.

The logic level applied to the $\overline{INT}$/EXT pin of the ADS2806 determines if the converter operates with either the built-in reference or external reference voltages. Due to this function pin having an internal 50kΩ pull-up resistor, the default configuration is external reference mode. Grounding this pin will activate the internal reference option.

The input track-and-hold amplifier is differential. A positive 1Vp-p on the IN and its compliment, a negative 1Vp-p, on the $\overline{IN}$ (see Figure 3) results in 2Vp-p on the output of the track-and-hold. Likewise, 2Vp-p on the IN and 0Vp-p on the $\overline{IN}$ (see Figure 4) results in 2Vp-p on the output of the track-and-hold. Therefore, the reference voltages, REFT and REFB, are the same for both differential and single-ended inputs, as shown in Table I.

INPUT	REFERENCE	IN (Pin-50, 63)	$\overline{IN}$ (Pin-51, 62)	REFT	REFB
2Vp-p Differential 1Vp-p Times 2 Inputs	Internal or External	2V to 3V	3V to 2V	+3V	+2V
2Vp-p Single-Ended 2Vp-p Times 1 Input	Internal or External	1.5V to 3.5V	$2.5V_{DC}$	+3V	+2V
3Vp-p Differential 1.5Vp-p Times 2 Inputs	Internal or External	1.75V to 3.35V	3.25V to 1.75V	+3.25V	+1.75V
3Vp-p Single-Ended 3Vp-p Times 1 Input	Internal or External	1V to 4V	$2.5V_{DC}$	+3.25V	+1.75V

TABLE I. Reference Voltages for Input Signal Ranges.

The external references may be changed for different tasks. The ADS2806 will follow the external references with a latency of 8 to 10 clock cycles. If it is desired to use $\overline{INT}$/EXT and SEL to change the configuration of a circuit for different tasks, a large amount of time must be allowed. This time could be hundreds of microseconds. Refer to the Diagram on the front page. Note that there is no disconnect for external references. If it is desired to switch between internal and external references, disconnect switches must be added between the external references and the ADS2806.

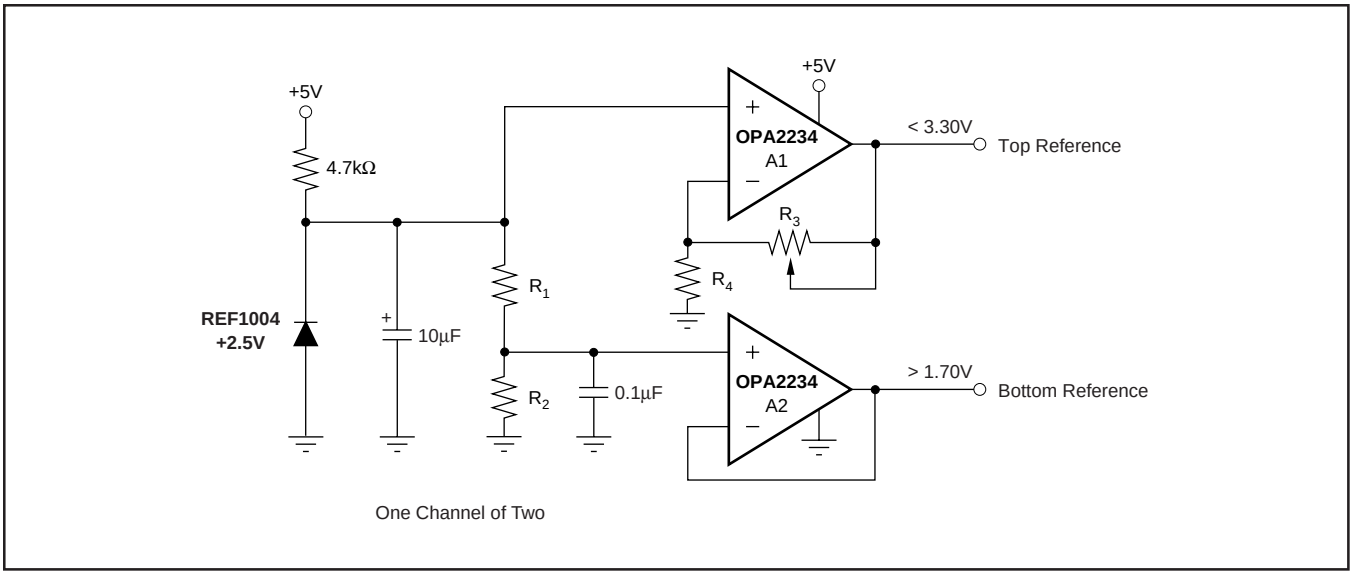


FIGURE 7. Example for an External Reference Driver Using the Dual, Single-Supply Op Amp, OPA2234.

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Both channels of the ADS2806 are controlled by the same clock on the rising edge. Utilizing a single clock reduces timing uncertainty in the sampling of the two channels. Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. Clock jitter leads to aperture jitter (t_A), which adds noise to the signal being converted. The ADS2806 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20\log\frac{1}{2\pi f_{IN}\, t_A}\text{rms signal to rms noise}$$

where: f_{IN} is input signal frequency

t_A is rms clock jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less. The clock input of the ADS2806 can be driven with either 3V or 5V logic levels. Using low-voltage logic (3V) may lead to improved AC performance of the converter.

Over Range Indicator (OVR)

If the analog input voltage exceeds the set full-scale range, an over range condition exists. The "OVR" pin of the ADS2806 can be used to monitor any such out-of-range condition. This "OVR" output is updated along with the data output corresponding to the particular sampled analog input voltage. Therefore, the OVR data is subject to the same pipeline delay as the digital data. The OVR output is LOW when the input voltage is within the defined input range. It will go HIGH if the applied signal exceeds the full-scale range.

Data Outputs

The digital outputs of the ADS2806 can be set to a high-impedance state by driving $\overline{OE}$ (pins 6 and 42) with a logic HIGH. Normal operation is achieved with pins 6 and 42 LOW due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly, or be dynamically changed during the conversion process. The output data format of the ADS2806 is in positive Straight Offset Binary code, as shown in Tables II and III. This format can easily be converted into the Binary Two's Complement code by inverting the MSB.

SINGLE-ENDED INPUT ($\overline{IN}$ = CM, Pins 52, 61)	STRAIGHT OFFSET BINARY (SOB)
+FS–1LSB (IN = CMV + FSR/2)	1111 1111 1111
+1/2 FS	1100 0000 0000
Bipolar Zero (IN = V_{CM})	1000 0000 0000
–1/2 FS	0100 0000 0000
–FS (IN = CMV – FSR/2)	0000 0000 0000

TABLE II. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ Tied to the Common-Mode Voltage.

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)
+FS–1LSB (IN = +3V, $\overline{IN}$ = +2V)	1111 1111 1111
+1/2 FS	1100 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = V_{CM})	1000 0000 0000
–1/2 FS	0100 0000 0000
–FS (IN = +2V, $\overline{IN}$ = +3V)	0000 0000 0000

TABLE III. Coding Table for Differential Input Configuration.

Data output is in the form of two parallel words. It is recommended that the capacitive loading on the data lines be as low as possible (< 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS2806 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS2806 from high-frequency digital noise on the bus coupling back into the converter.

Digital Output Driver Supply (VDRV)

Each channel of the ADS2806 has a separate dedicated supply pin (8, 40) for the output logic drivers, VDRV, which are not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS2806 produces corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS2806 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line that may affect the AC performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

OUTPUT ENABLE ($\overline{OE}$)

The digital outputs of the ADS2806 can be set to high impedance (tri-state) by driving $\overline{OE}_A$ and $\overline{OE}_B$ (pins 6, 42) with a logic HIGH. Normal operation is achieved with the same pins pulled LOW.

GROUNDING AND DECOUPLING

Proper grounding, bypassing, short trace lengths, and the use of power and ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages, such as minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS2806 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise that otherwise would be coupled into the converter and degrade the achievable performance. The ground pins should directly connect to an analog ground plane that covers the PC board area under the converter. While designing the layout it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Due to its high sampling rate, the ADS2806 generates high-frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 8 shows the recommended decoupling scheme for the ADS2806. In most cases, 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. If system supplies are not a low enough impedance, adding a small tantalum capacitor will yield the best results.

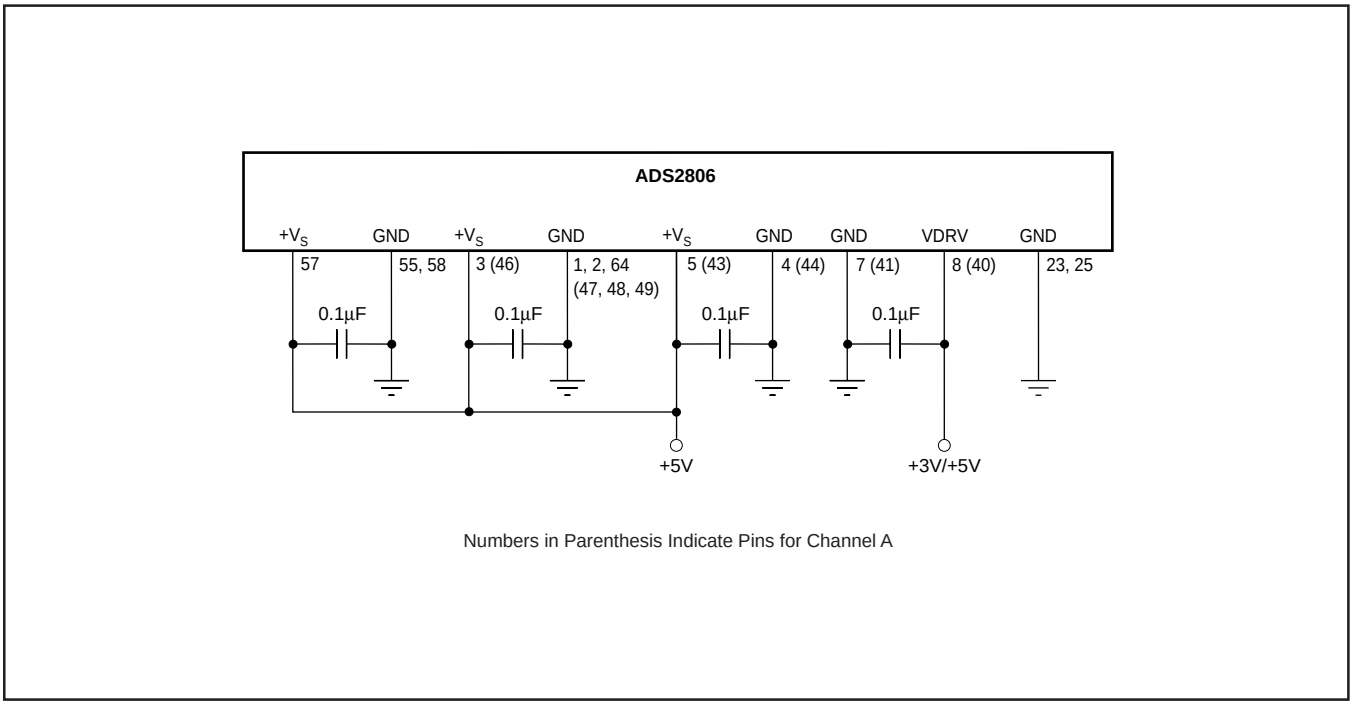


FIGURE 8. Recommended Bypassing for the Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS2806Y/250	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS2806Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

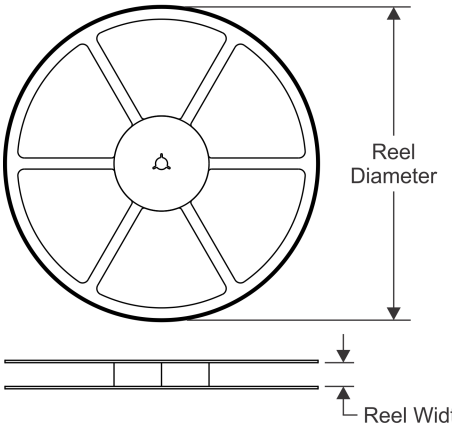
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

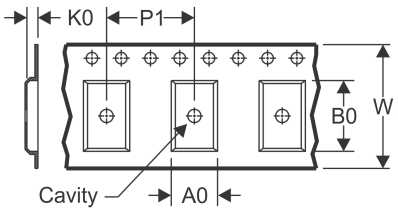
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

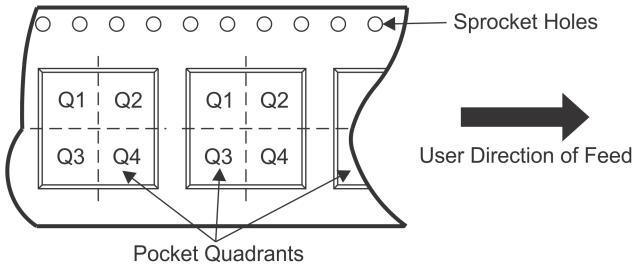


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

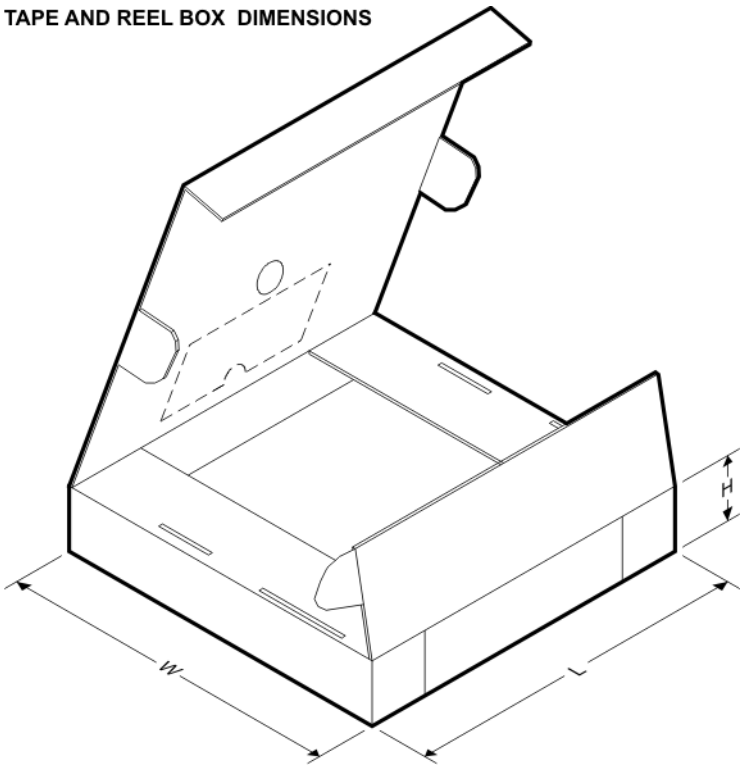
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS2806Y/250	HTQFP	PAP	64	250	180.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS2806Y/250	HTQFP	PAP	64	250	213.0	191.0	55.0

GENERIC PACKAGE VIEW

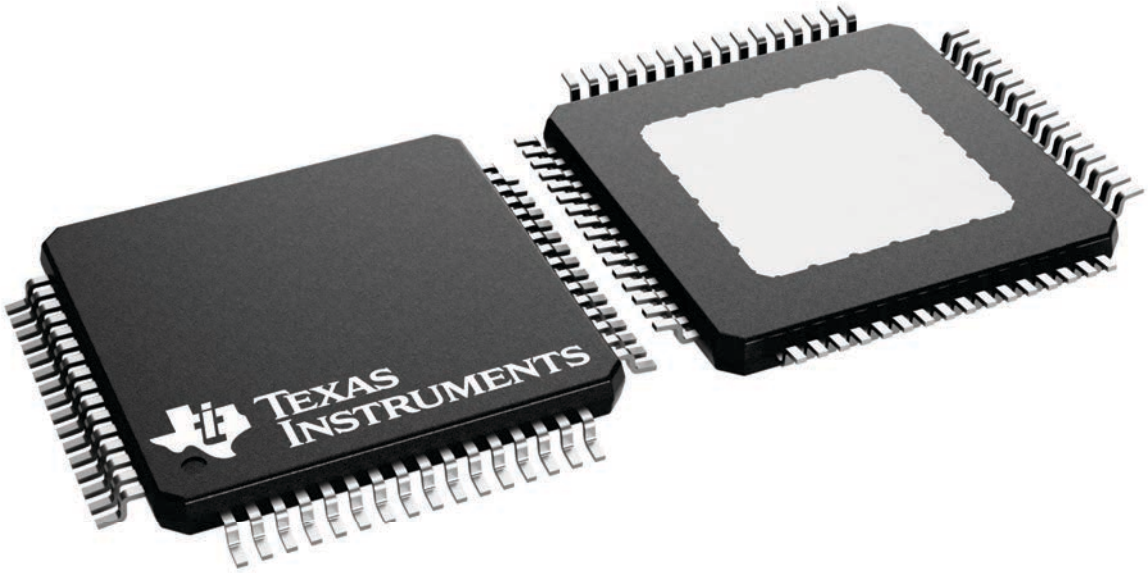
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



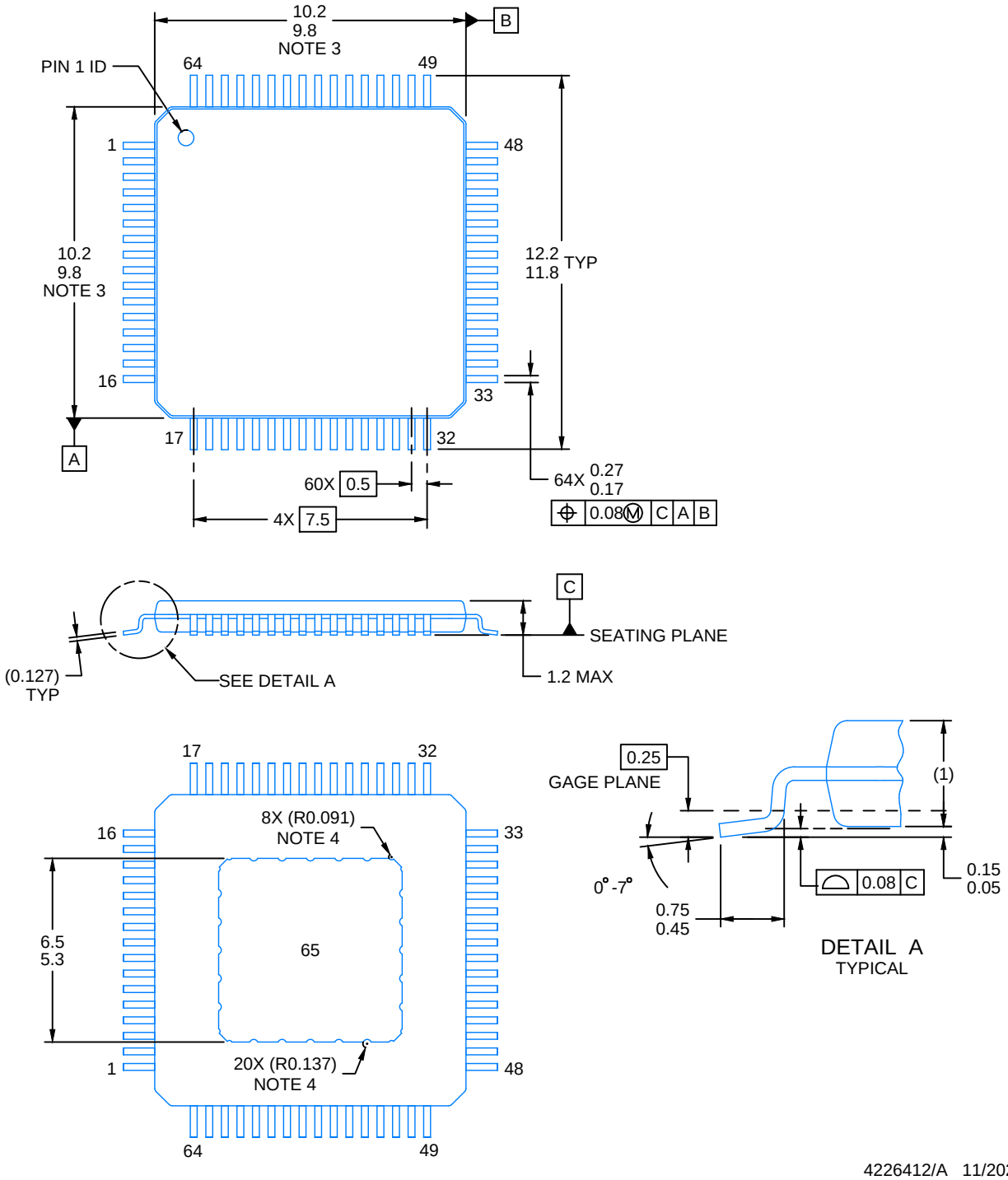
4226442/A

PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

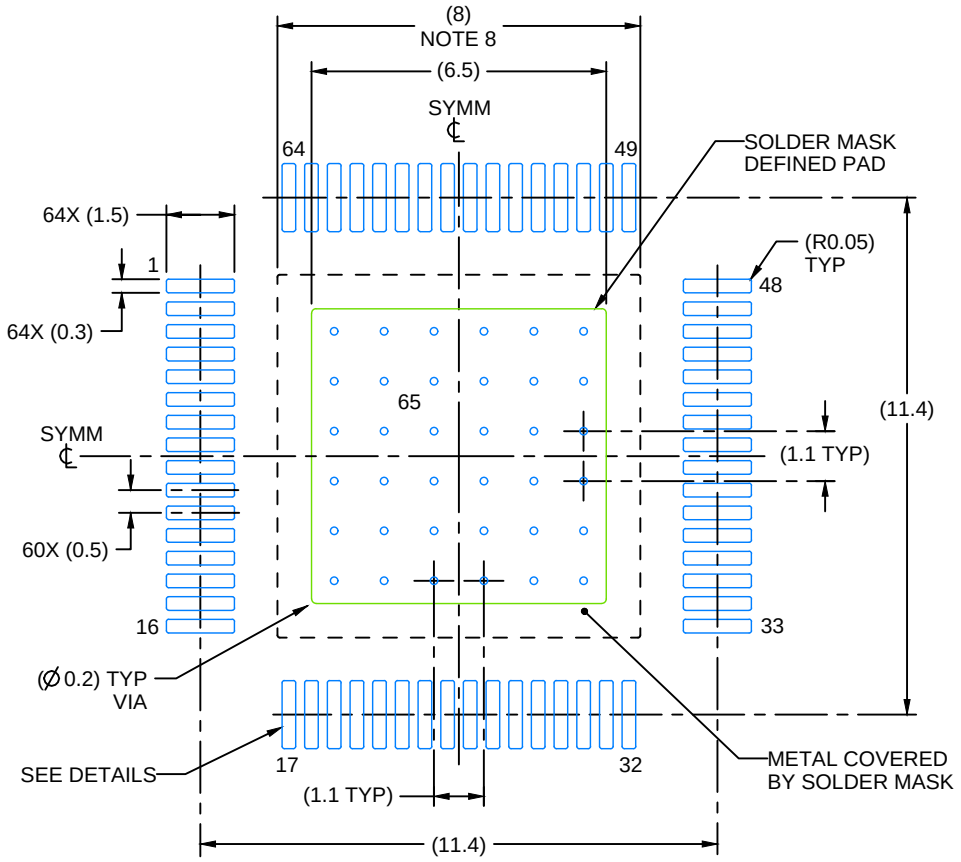
PLASTIC QUAD FLATPACK



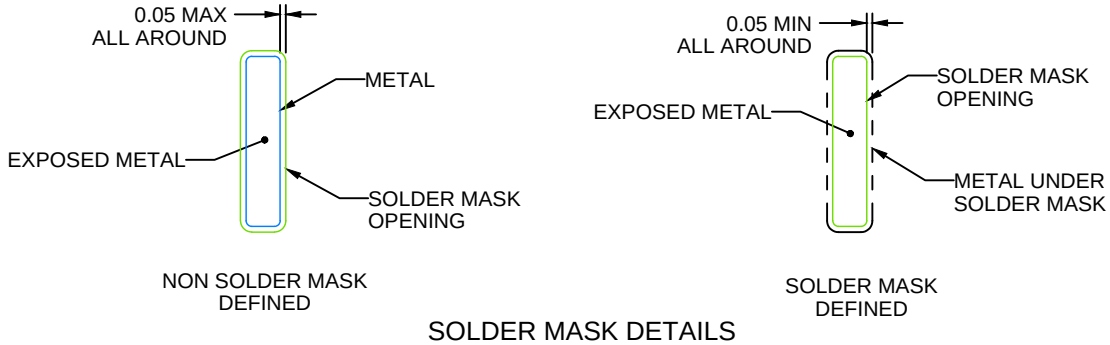
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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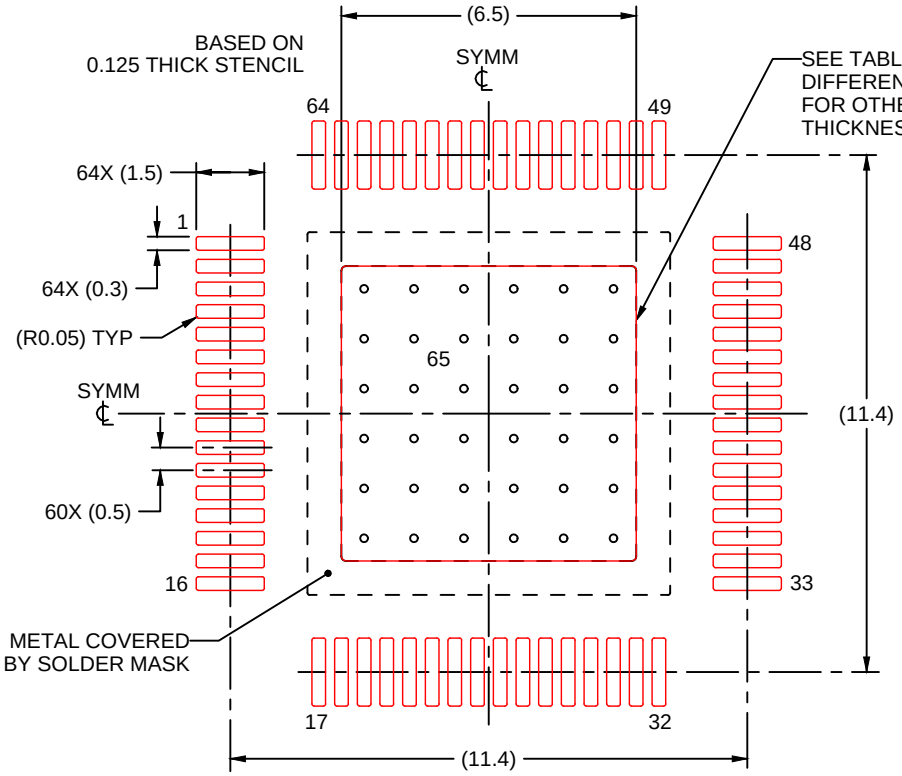
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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