Application Report
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LMK04828 as a Clock Source for the ADS42JB69

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ABSTRACT

The ADS42JB69 EVM includes the LMK04828 jitter cleaner clocking solution. This application note provides an overview of the different clocking configurations of the EVM and demonstrates how to achieve the best possible signal-to-noise ratio (SNR) when clocking the ADS42JB69 with the LMK04828. The LMK04828 is a dual-loop PLL and frequency synthesizer and supports the JESD204B interface.

In order to achieve very low phase noise and clock jitter, the LMK04828 is operated with an external 100-MHz VCXO to generate the 250-MHz sampling clock for the ADC. Alternatively, the ADS42JB69 provides an option to use an external low jitter signal source. However, even with an external clock source, in order to operate the JESD204B interface, the LMK04828 still must provide the SYSREF signal to the ADS42JB69, as well as the capture card solution.

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1 ADS42JB69 EVM Overview

In default operating condition, the LMK04828 provides the sampling clock for the ADS42JB69 using an external VCXO. The EVM provides a 10-MHz reference output to synchronize other signal generators for a coherent measurement setup. The loop filter can be customized for different VCXO frequencies.

Shared pads on the ADS42JB69 clock input traces provide an option to use an external clock signal. This connection can also be used to filter the clock output of the LMK04828 (available on the CLKOUT10 SMA connectors) and then loop it back to the external clock input.

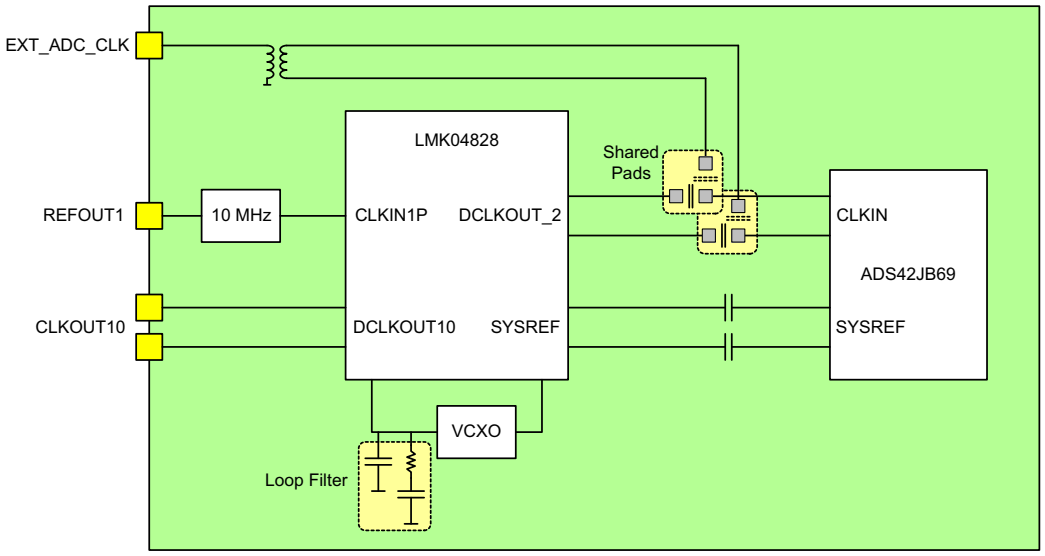
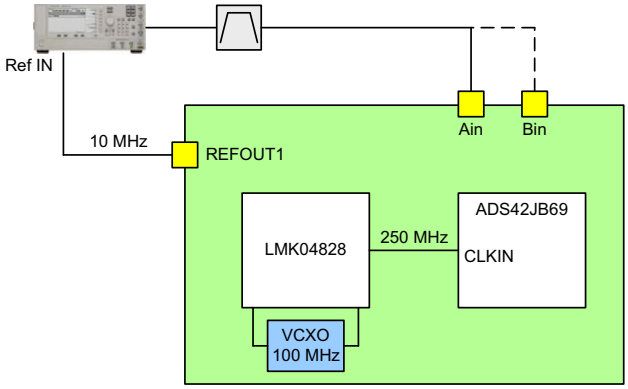


Figure 1. ADS42JB69 EVM Functional Block Diagram

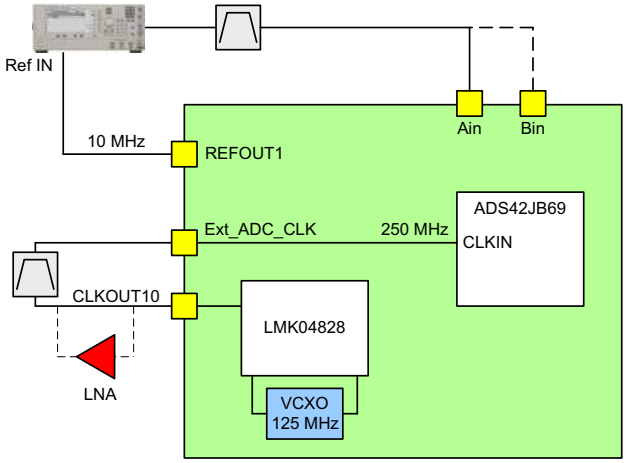
2 Test Configuration Options

In this application note, two different clocking configurations using the LMK04828 are examined and compared against the *ideal* scenario using an ultra-low-noise signal generator. Independent of configuration, a 100-MHz VCXO is used to generate the 250-MHz output clock.

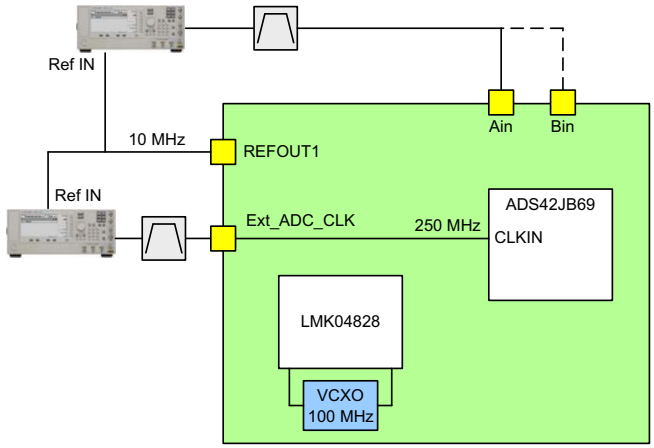
Option 1: Internal Clock The LMK04828 is configured to differential output signaling connected directly to the ADS42JB69 clock inputs, without any filtering. Two different output formats (LVPECL and HSDS) are examined.



Option 2: Internal Clock with External Filtering An external bandpass filter is used to limit the jitter contribution of the LMK04828 clock output which is available on the CLKOUT10 SMA connectors. The filtered clock signal is then applied to the EXT_ADC_CLK SMA connector and used as the sampling clock. Additionally, using an external low-power, low-noise amplifier was investigated to boost the clock amplitude in order to improve slew rate, and thus the ADC aperture jitter. Place the LNA prior to the bandpass filter in the signal chain so that its jitter degradation is minimized.



Option 3: External Clock with Filtering An external low jitter signal generator with bandpass filter is used to provide the sampling clock for the ADS42JB69.



3 Phase Noise Comparison

The phase noise or clock jitter contribution of the three different configuration options is best compared using a phase-noise analyzer.

Figure 2 illustrates that the external bandpass filter limits the far end noise floor and thus the clock jitter to about 4-MHz offset from the fundamental frequency. Furthermore, the filter impact diminishes if the clock amplitude itself gets too low (see LVPECL + BPF – Option 2").

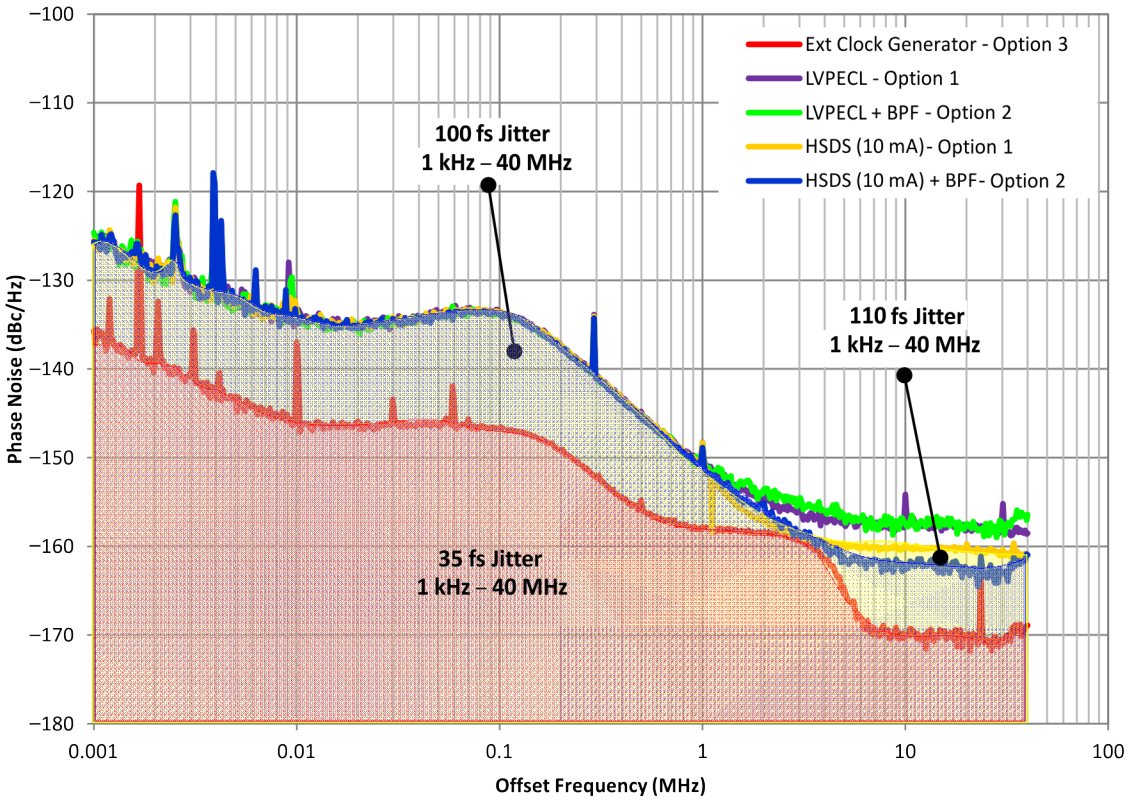


Figure 2. Phase Noise Comparison of Different Clocking Options

The jitter is calculated by integrating the phase noise between upper and lower integration bandwidths. If a bandpass filter is used, it sets the upper integration limit. For unfiltered clock inputs, the far end noise should be estimated flat and integrated to ~2x the sampling clock frequency, which equals an offset frequency of 1x the sampling rate (see SLYT389).

In reality, the far end noise floor is slightly lower than indicated in the measurement because the phase noise analyzer doesn't have a brick wall 40-MHz input filter but aliasing from higher input frequencies occurs. This should be taken into consideration when estimating jitter from unfiltered clock sources.

The lower integration limit is application dependent. If, for example, the closest adjacent carrier is 200 kHz, the jitter contribution within ~100 kHz offset can be ignored. When taking FFT measurements, the number of points determines the bin size. For example, a 65 k FFT with 250 MSPS results in a bin size of 3.81 kHz. Since the primary bin is centered around the fundamental, phase noise within ~1.9 kHz offset is lumped into the bin of the fundamental frequency and doesn't degrade SNR.

Integration Bandwidth	1 kHz – 40 MHz	10 kHz – 40 MHz	100 kHz – 40 MHz
External signal generator	35 fs	34 fs	32 fs
LVPECL – no BPF	117 fs	113 fs	101 fs
LVPECL – with BPF	120 fs	117 fs	104 fs
HSDS – no BPF	110 fs	107 fs	100 fs
HSDS – with BPF	101 fs	99 fs	84 fs

4 Measurement Results

The different clocking options were examined by sweeping the input frequency from 10 MHz to 230 MHz with a full-scale input amplitude of 2 Vpp and 2.5 Vpp.

As expected, the SNR showed a big dependence on the clock jitter and clock slew rate, while SFDR degraded a little bit with a slower slew rate. It can be observed that the bandpass filter improves the SNR performance quite a bit – at an input frequency of 170 MHz, the SNR improves approximately 0.8 dB from 71.7 dBFS to 72.5 dBFS.

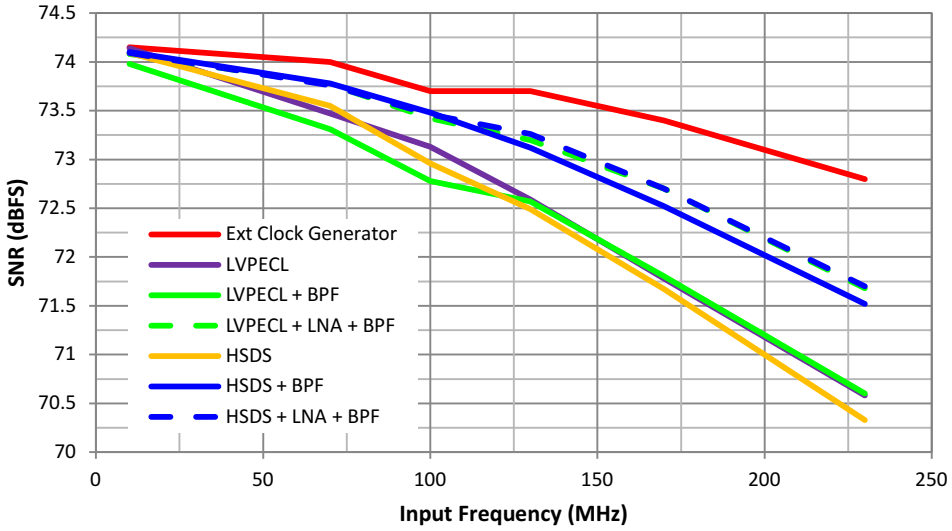


Figure 3. SNR versus Input Frequency (2 Vpp)

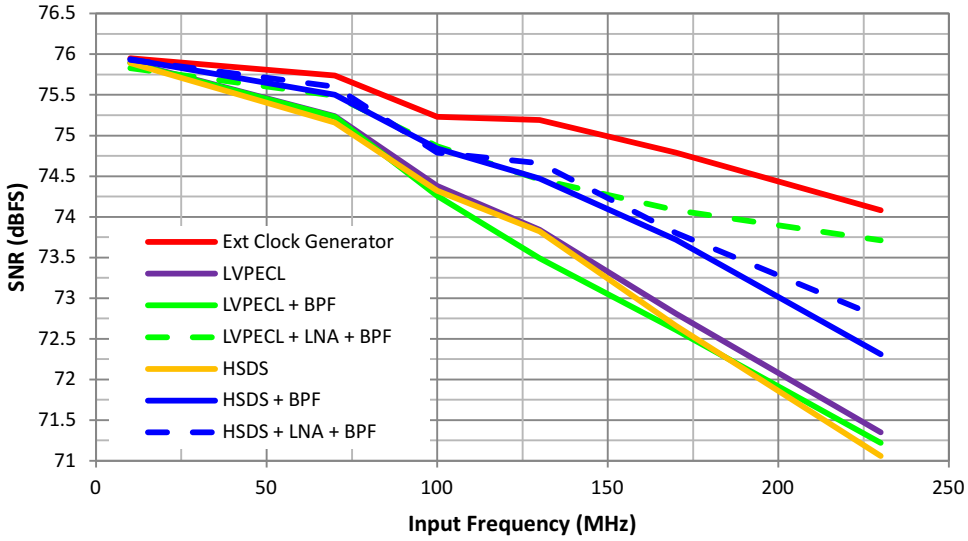


Figure 4. SNR versus Input Frequency (2.5 Vpp)

5 Unfiltered Clock

Next, the default clocking option on the ADS42JB69 EVM was closely examined. The LMK04828 is connected directly to the ADS42JB69 clock input without any bandpass filtering. As can be seen from the phase noise plot (Figure 2), the far end noise floor beyond 40-MHz offset frequency is about –160 dBc/Hz. Setting the upper integration bandwidth to 250 MHz (from 250 MHz to 500 MHz = 0- to 250-MHz offset frequency), the jitter calculates to ~150 fs (1 kHz to 250 MHz).

The SNR of the ADC is limited by the quantization noise (96 dB for a 16-bit ADC), the thermal noise (74.1 dBFS at 2 Vpp for ADS42JB69) the clock jitter which sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \times \log\left(2\pi \times f_{in} \times T_{Jitter}\right) \quad (2)$$

The total clock jitter (T_{Jitter}) has three components – the internal aperture jitter which is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. It can be calculated using Equation 3.

$$T_{Jitter} = \sqrt{\left(T_{Jitter,Ext.Clock\_Input}\right)^2 + \left(T_{Aperture\_ADC}\right)^2 + \left(T_{Jitter,Analog\_input}\right)^2} \quad (3)$$

Assuming the ADS42JB69 has a thermal noise of 74.1 dBFS (2 Vpp) and 85 fs of aperture jitter, the ADC SNR depending on input frequency can be calculated for the different clocking options:

- 35 fs for external signal generator
- 100 fs for filtered clock output
- 150 fs for unfiltered clock output

	Input Frequency (MHz)					
SNR (dBFS)	**10**	**70**	**100**	**130**	**170**	**230**
35 fs (calculated)	74.1	74.0	73.8	73.6	73.3	72.8
Ext. Clock Generator (measured)	74.1	74.0	73.7	73.7	73.4	72.8
100 fs	74.1	73.8	73.5	73.2	72.6	71.7
HSDS with BPF	74.1	73.8	73.5	73.1	72.5	71.5
150 fs	74.1	73.6	73.2	72.6	71.8	70.5
LVPECL unfiltered	74.1	74.0	73.1	72.6	71.8	70.6

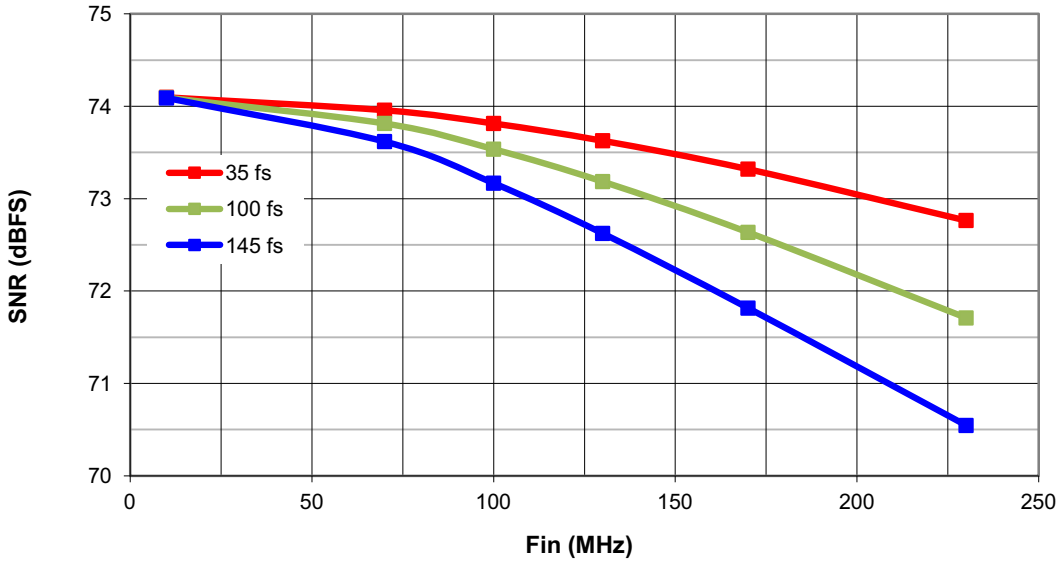


Figure 5. SNR (2 Vpp) versus Input Frequency and External Clock Jitter

It can be seen that the calculated values match the measured SNR extremely well for a given amount of clock jitter. By adding the clock filter, the total external jitter improves from ~150 fs to ~100 fs and improves the SNR to within ~0.8 dB of data sheet values at an input frequency of 170 MHz.

Adding the low-noise amplifier to boost the clock slew rate further improves the SNR by ~0.2 dB.

The following screen shots were made using the ADS42JB69SEK, along with the TSW1400 capture card at Fs = 250 MSPS and f_{in} = 170 MHz with a full-scale of 2 Vpp.

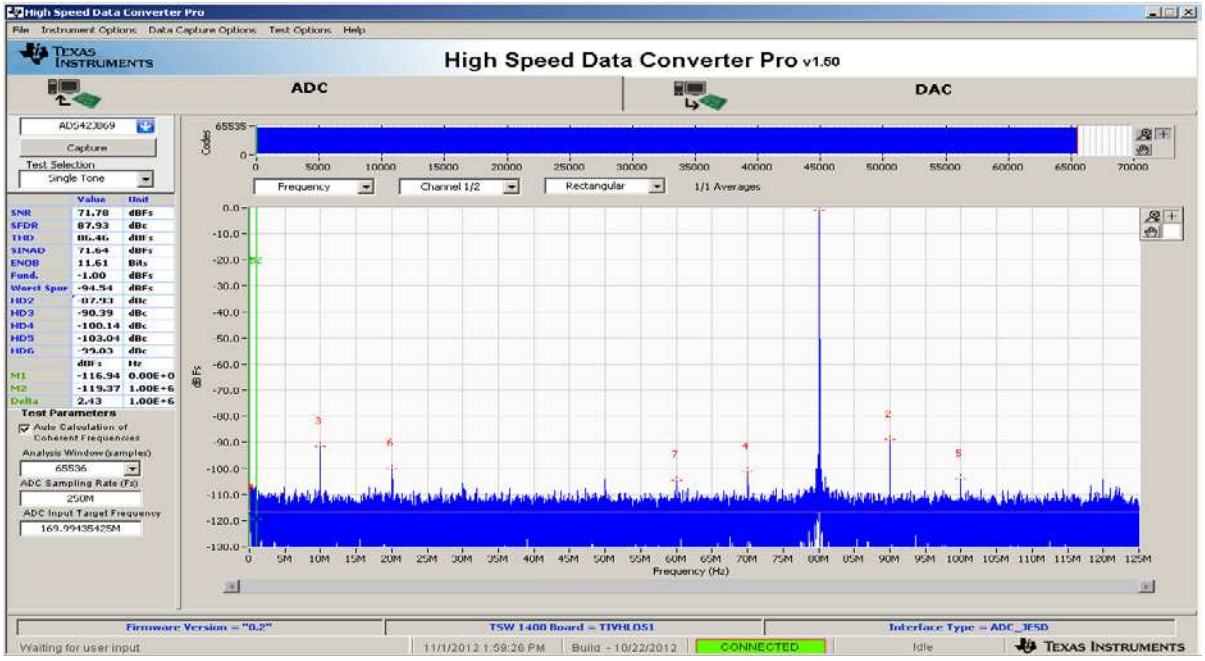


Figure 6. Default Clocking Option LVPECL Clock (Unfiltered)

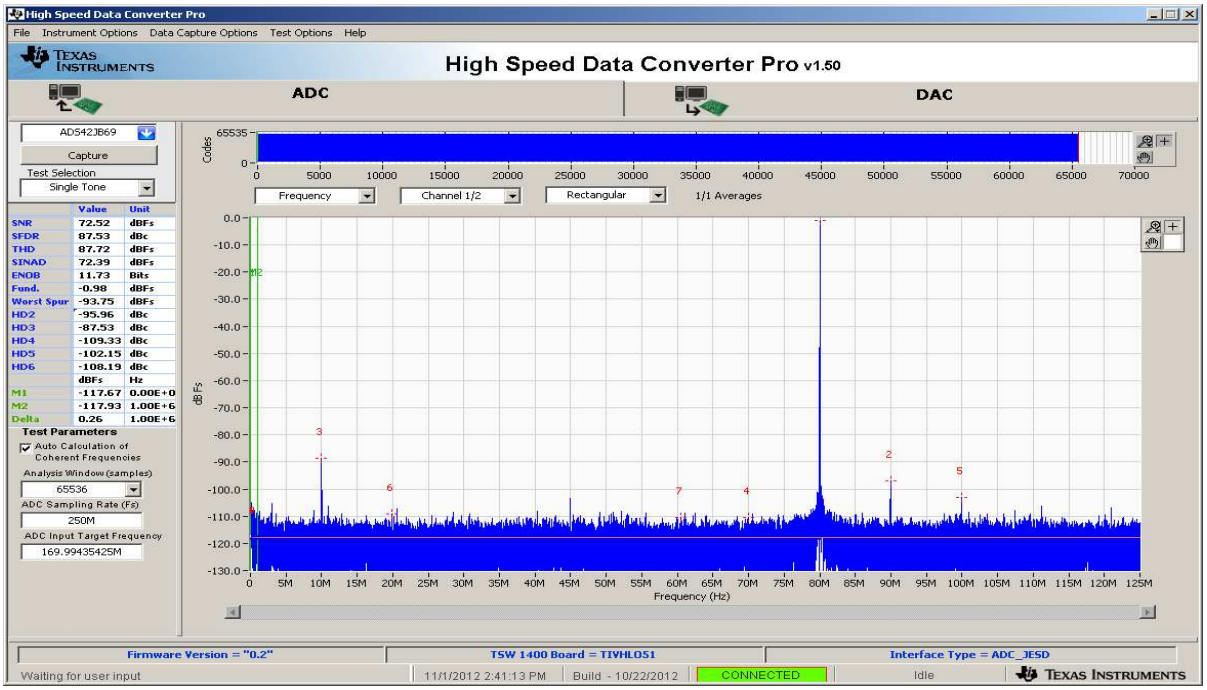


Figure 7. HSDS Clocking Option With External Bandpass Filtering

6 LMK04828 Setup

The LMK04828 was set up using the clock design tool. The PLL1 loop bandwidth was set to 1 MHz with an external 10-MHz reference and the PLL2 loop bandwidth was set to 100 MHz for the external 100-MHz VCXO. This calculates the values for loop filter components to:

- C1 = 27 pF
- R2 = 0.68 kΩ
- C2 = 2.7 nF

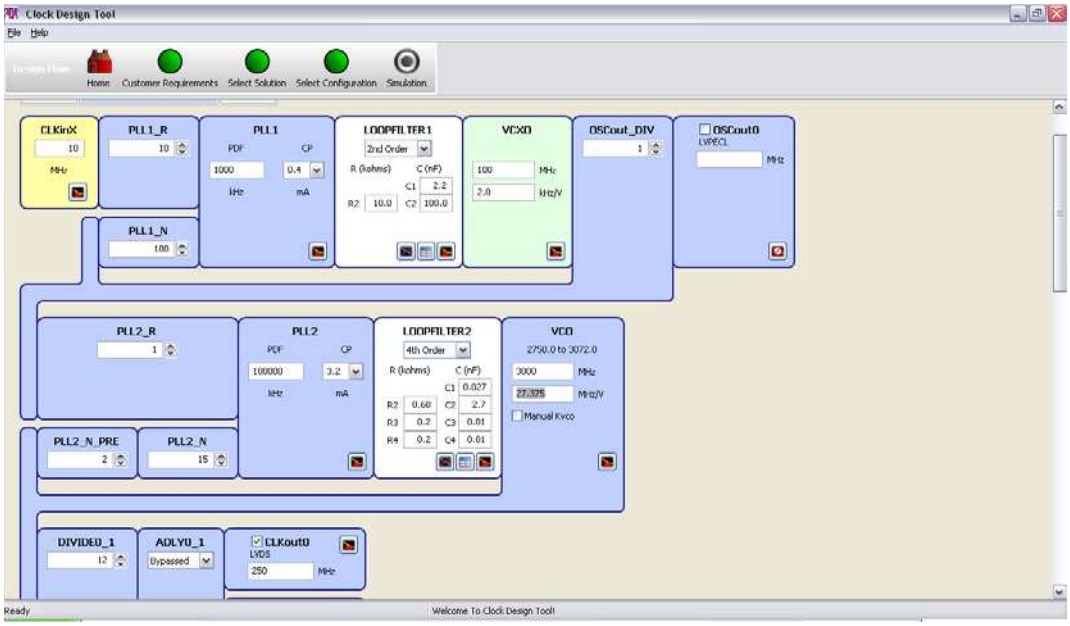


Figure 8. Clock Design Tool

The clock design tool is useful for checking the expected phase noise performance. If the loop filter is designed incorrectly, it can create peaking in the phase-noise response which is visible in the ADC output spectrum, degrading the SNR.

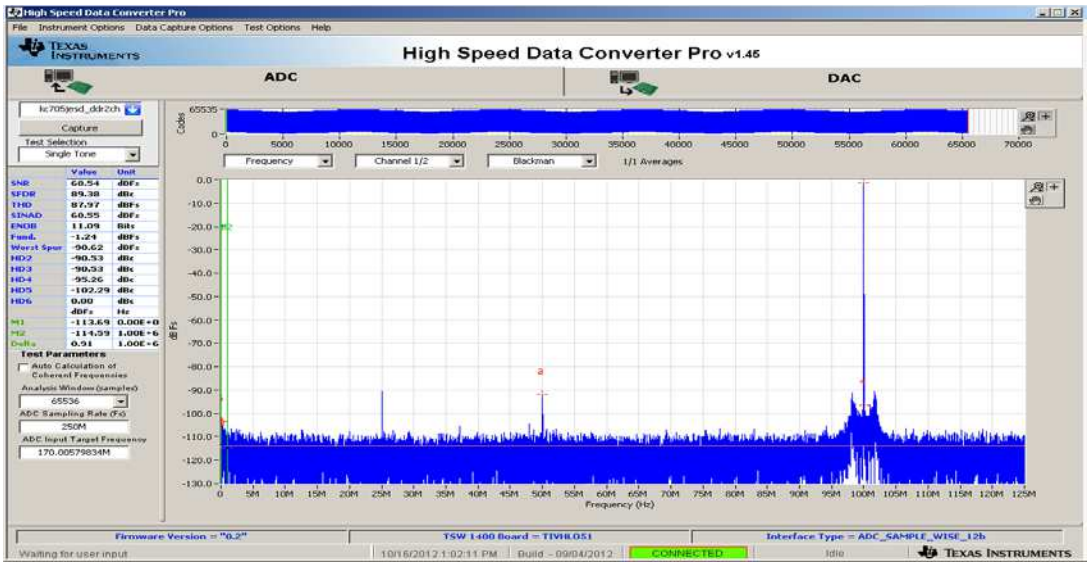


Figure 9. Phase-Noise Response Peaking

7 Tips and Tricks

In order to maximize the SNR performance of the ADS42JB69, the clock amplitude should be larger than ~1 Vpp. A bandpass filter on the clock input limits the jitter contribution but also removes the higher-order harmonics of the clock signal which help achieve a high slew rate. In addition, the insertion loss of the bandpass filter also reduces the clock amplitude which, in turn, further reduces the slew rate. A 1:4 step up transformer or a low noise amplifier can be used to improve clock amplitude and slew rate again.

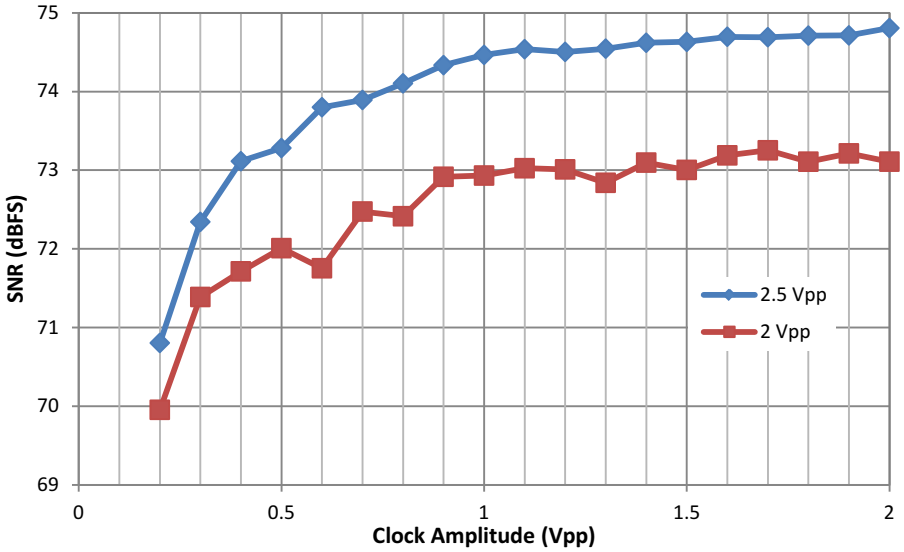


Figure 10. SNR (dBFS) versus Clock Amplitude (f_{in} = 170 MHz)

The LMK04828 has two internal high-frequency VCOs. For the measurements in this application note, internal VCO1 was used which showed slightly better phase-noise performance.

Special care should be given to the power supply filter design for the external VCXO (100 MHz). With insufficient power supply filtering, it is observed that a 100-MHz and 50-MHz spur couple into the LMK04828 clock output, which causes spurs in the ADC output spectrum at f_{in} ±100 MHz and f_{in} ±50 MHz. Unused outputs of the LMK04828 should be powered down, whenever possible. This can reduce the amplitude of low-level spurs in the ADC output spectrum.

The SYSREF output of the LMK04828 should be operated in pulse mode instead of continuous mode, if possible. Providing a constant SYSREF signal to the ADS42JB69 appears like an additional clock input signal which may cross couple internally and cause additional low-level spurs in the output spectrum.

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