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CDCE72010 as a Clocking Solution for High-Speed Analog-to-Digital Converters

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ABSTRACT

Texas Instruments has recently introduced a family of devices suitable to meet the demands of high-speed, high-IF sampling analog-to-digital converters (ADCs) such as the ADS5483, which is capable of sampling up to 135 MSPS. To realize the full potential of these high-performance devices, the system must provide an extremely low phase noise clock source. The CDCE72010 clock synthesizer chip offers a real-world clocking solution to meet these stringent requirements for high-speed ADCs. This report highlights the limiting agents associated with the clock source that adversely affect the ADC signal-to-noise performance. The performance of the ADS5483 ADC clocked with the CDCE72010 is presented and compared to ideal baseline performance. Further improvement topologies are offered, along with measured results that show the CDCE72010 can meet or exceed the required specifications at high sampling rates, even at demanding high-input frequencies.

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1 Introduction

New transceiver architectures and power amplifier (PA) linearization techniques are currently being investigated with the introduction of high sampling rate and high-IF capability ADCs. For example, digital predistortion requires high sampling rate ADCs to convert the PA output spectrum, including the desired signal and the third- and fifth-order intermodulation products, for linearization processing. Additionally, the bandwidth requirements for a multi-carrier WCDMA PA can be as high as 100 MHz. This level of performance requires high sampling rate ADCs to properly capture the signal.

For new receiver designs with multi-carrier signals that incorporate cost-saving topologies, there is a need for high-IF sampling ADCs. This design requirement effectively eliminates the need for a second analog miner or analog demodulator that simplifies the receiver architecture. A high-IF ADC is required to sample the signal at these frequencies with sufficient purity to meet advanced telecommunication standards.

Texas Instruments offers a series of high-IF, high sampling rate ADCs that are suitable for the wireless infrastructure market. The ADS5483, for example, is an industry-leading, 16-bit, 135-MSPS ADC that is capable of achieving good signal-to-noise ratio (SNR) performance with high input frequency signals. In order to realize the full potential of this device, however, it is important to use a low phase noise clock source. This requirement is often overlooked when evaluating and designing with high-end ADCs. Furthermore, although a suitable source may be used for evaluation purposes, finding a board-level solution often proves difficult.

Texas Instruments has developed a board-level, low phase noise clocking solution for the ADS5483 and other high-speed ADC devices using the CDCE72010 clock synthesizer chip. With proper configuration, the CDCE72010 can be used with high-speed ADCs to achieve ideal performance; this device is also suitable for direct implementation into printed circuit board (PCB) designs. In addition, the CDCE72010 has the capability to drive 10 independent outputs that can be independently divided down. This capability allows one clock circuit to provide a clock source for both the high-performance ADCs as well as the other devices on the board that require an independent clock, such as digital-to-analog converters (DACs), digital down-converters (DDCs), or digital up-converters (DUCs). Figure 1 illustrates how the CDCE72010 is used with the ADC and other devices in a typical transceiver block diagram.

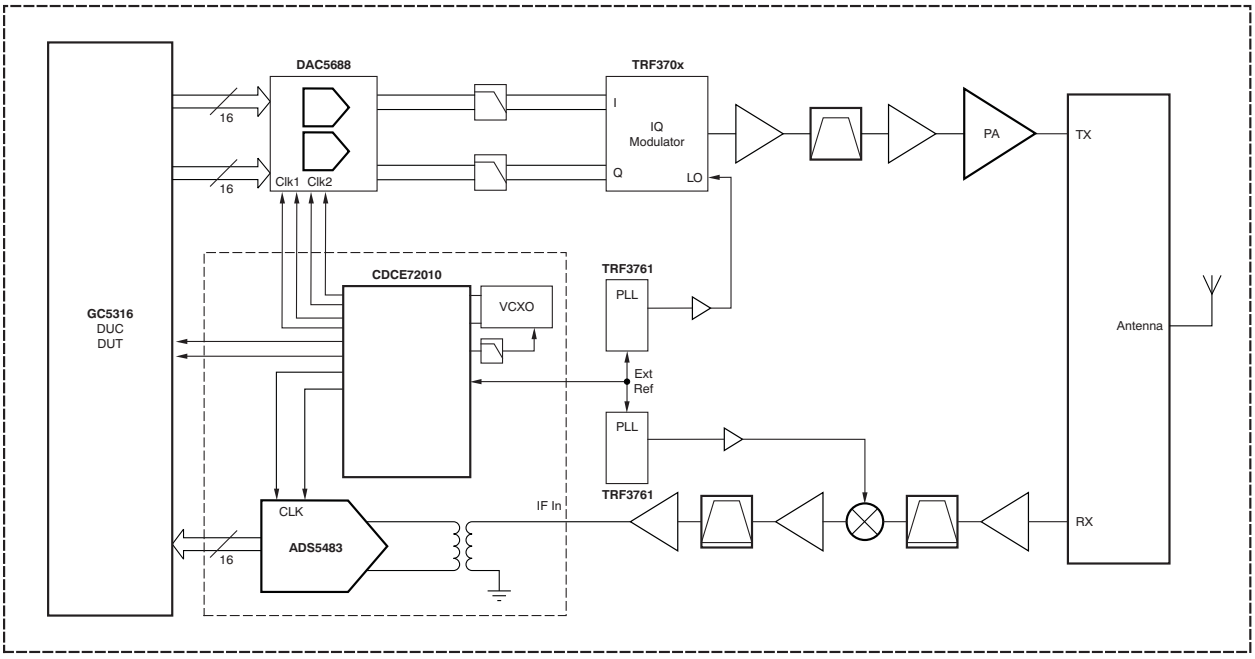

Figure 1. ADS5483 ADC with the CDCE72010 Clocking Solution Within a Typical Base Station Architecture

2 High-IF Sampling Challenges

Clock jitter is defined as the random variation of the clock position compared to its ideal position with respect to time. When the position of the clock varies slightly, it alters the position of the sampling point, which in turn samples the input waveform at an imprecise location. This error manifests itself as SNR degradation.

SNR degradation attributed to clock jitter and jitter inherent to the ADC is defined as:

$$SNR_T = -20\log\left(\frac{\frac{V_{fs}}{2} \times (2 \times \pi \times f_{in}) \times 10^{\frac{V_{IN}}{2}} \times t_j}{\sqrt{2}}\right) \quad (1)$$

Where:

- V_{fs} = Full-scale voltage of the ADC
- V_{in} = Relative input amplitude of the signal compared to V_{fs}, expressed in dBFS
- f_{in} = Input frequency
- t_j = Total system jitter (in seconds)

Total system jitter is defined as:

$$t_j = \sqrt{t^2_{ADC} + t^2_{CLK}} \quad (2)$$

Where:

- t_{ADC} = Aperture jitter of the ADC (in seconds)
- t_{CLK} = Clock jitter (in seconds)

Note that the SNR degradation as a result of clock jitter is independent of the sampling rate; however, it does depend on the input frequency. For much smaller input frequencies (relative to the sampling frequency), the SNR degradation comes from the quantization noise limitation of the ADC, and not from the clock jitter. For a given amount of clock jitter, it can also be seen from the above equations that a higher IF input signal will be more susceptible to SNR degradation. This phenomenon is illustrated in Figure 2.

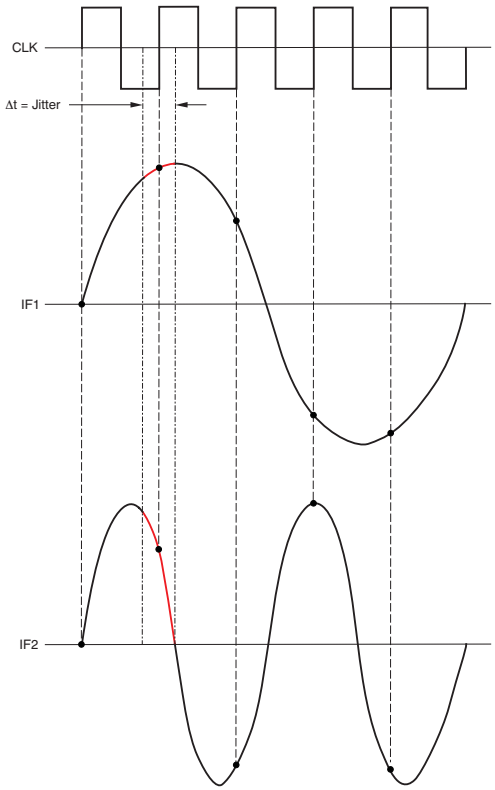

Figure 2. SNR Degradation as a Result of Jitter for Different IF Input Signals

Figure 2 depicts two IF input signals at different frequencies. An ideal clock source, with a given amount of jitter, samples each signal. The ideal sampling point is shown at the dots, but the jitter will alter the exact point where the signal is sampled. The potential points that could be sampled are depicted by the bold red line between the dashes. The error line on the lower frequency signal is smaller than that on the higher frequency signal. As a result, the higher IF signal will have higher SNR degradation due to clock jitter. The integration limits, important for the ADC SNR performance, for the jitter of the clock source from its the phase noise profile that can be obtained from the standards to which the system adheres.

Figure 3 shows the measured performance versus predicted performance of the ADS5483 at a sampling frequency of 122.88 MSPS.

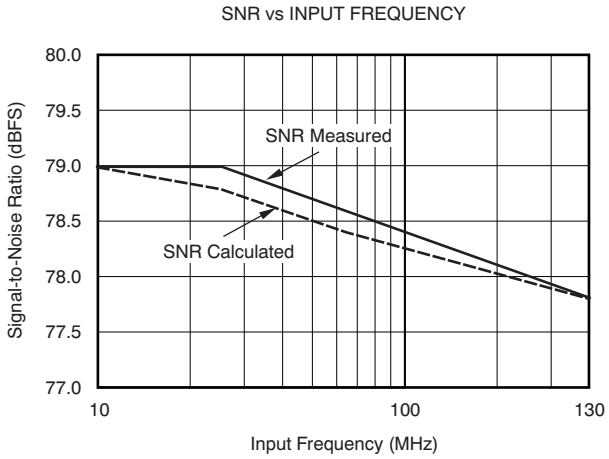

Figure 3. Measured vs. Predicted SNR Performance Over Input Frequency

The predicted values closely match the measured data for the device. Therefore, these equations can be used to predict performance at any desired input frequency.

3 Effect of Clock Amplitude

With an ideal square-wave clock, sampling is completed at the zero crossings of the waveform. Furthermore, in some ADC devices such the ADS6145, data are sampled and latched using the up-and-down cycles of the clock; thus, it is important for the clock to maintain a 50% duty cycle. Previously, it was shown that jitter affects the sampling position of the input waveform and degrades SNR performance. Thermal noise from a non-ideal clock also contributes to SNR degradation.

Thermal noise contributes a random amplitude vector to the clock source. With an ideal square-wave clock, the signal would slam instantly from one state to the other. In this scenario, slight amplitude variations because of noise would have no effect on the transition sampling point. Practically, however, even with a good square-wave clock, the transition from one state to the other is not instantaneous. There is a finite time in which the transition occurs. Noise on the waveform alters the signal such that the crossover points occur at positions that are slightly off the ideal. This offset causes a small error in the sampling point, which in turn degrades the SNR. Figure 4 illustrates an enlarged and zoomed image of the transition slope of the clock around the crossover point with added random noise. The noise component, Δn, raises the signal to the crossover point, and yields a small error, Δt.

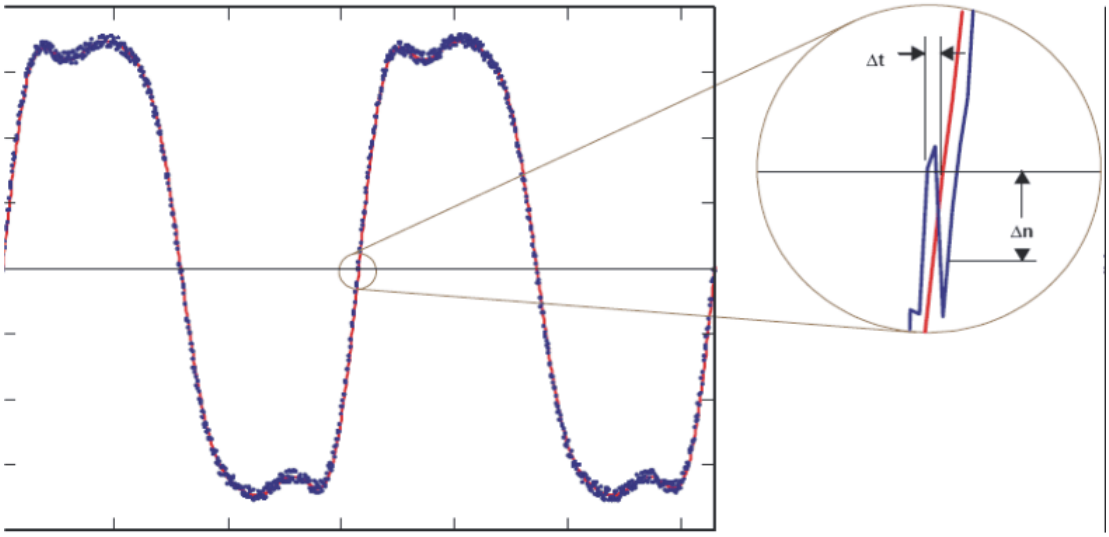

Figure 4. Sampling Error Caused by Thermal Noise Component

One way to minimize the impact of thermal noise degradation is to make the transition slope steeper. In other words, by increasing the transition slope of the clock signal, the signal more closely approximates the ideal square wave clock. Conversely, a less steep transition slope is more susceptible to SNR degradation because of thermal noise. Figure 5 illustrates two clock signal transition slopes, each subjected to the same thermal noise profile. The noise component is equal for both transition slopes, but the resulting timing error (Δt) is greater for the shallower slope. For this reason, it is desirable to keep the transition slopes as steep as possible in order to minimize the effect of thermal noise.

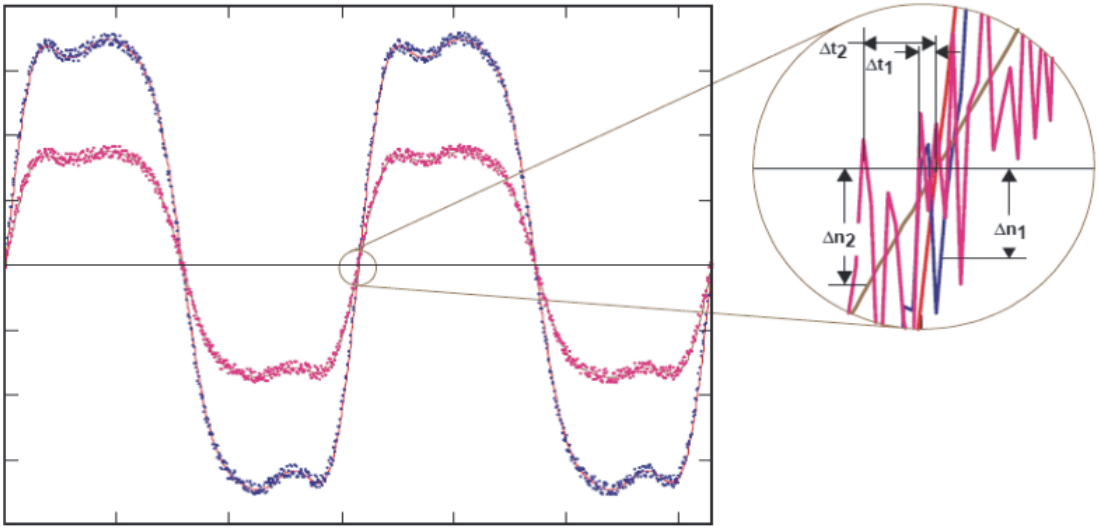

Figure 5. Thermal Noise Effect for Different Slope Clock Signals

For very high-IF input frequencies, the thermal noise component of the clock can be further minimized by including a band-pass filter at the clock input, centered at the clock frequency of choice. Any suitable band-pass filter topology will work well, such as an L-C filter, a surface acoustic wave (SAW) filter, or a crystal filter. Because the clock frequency is only a single tone, the most narrow bandwidth filter produces the best results.

The inclusion of a band-pass filter around the clock minimizes noise outside the filter bandwidth, but it also affects the transition slope of the clock signal. A square-wave clock signal is comprised of a fundamental tone and a series of higher-order harmonics. By inserting the narrow band-pass filter, the higher harmonic components of the clock signal are eliminated. The result is a pure fundamental tone in the frequency domain or a pure sine wave in the time domain. Though the filter has effectively minimized the noise components, it has also inadvertently reduced the transition slope of the clock signal because the transition of a sine-wave is shallower than that of a square wave. As shown previously, this shallower transition becomes more susceptible to noise contributions. The band-pass filter not only removes the harmonics of the clock signal, resulting in a sine-wave output signal; it also introduces an insertion loss of 2 dB to 6 dB. This insertion loss further reduces the amplitude of the clock signal and reduces the transition slope of the signal. In order to keep the transitions sharp, the amplitude of the sine-wave signal must be increased.

Figure 6 illustrates how error from thermal noise is minimized with a higher amplitude sine-wave signal, because it effectively increases the transition slope of the signal. A transformer can be inserted after the band-pass filter to amplify the signal in order to keep the transition slope as sharp as possible.

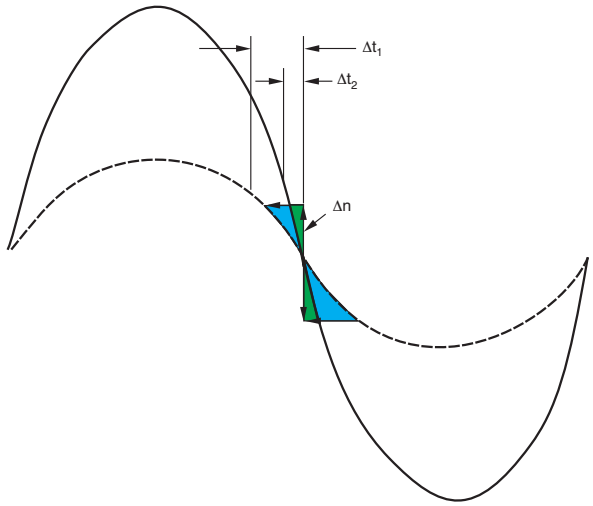

Figure 6. Thermal Noise Effect for Different Amplitude Sinusoids

4 CDCE72010 Clocking Solution

The CDCE72010 is a high-performance, low-jitter, differential/single-ended clock driver and clock distribution chip. It has 10 independently-controlled outputs that can be set to any combination of up to 10 differential (LVPECL or LVDS) outputs or 20 single-ended (LVMCOS) outputs that are suitable for clocking high-performance ADCs such as the ADS5483, as well as satisfy other clocking requirements on the board. The CDCE72010 offers a real-word clocking solution for these applications that can synchronize the clock output to a supplied board reference frequency.

5 CDCE72010-to-ADC Interface

For low- and medium-IF input frequencies to the ADC, the CDCE72010 output can be configured as a high-swing LVPECL signal (that provides a 10% increase in the amplitude over the regular LVPECL signal) and interfaced to the ADC, as Figure 7 shows. The high-swing LVPECL outputs must be properly terminated; for the best clock signal, it is important to properly terminate the clock lines close to the ADC device to minimize reflections. Using the differential output is ideal in this case, because it minimizes the susceptibility of outside noise coupling on the line. Loop filter components for the CDCE72010 are contingent on the frequency of the VCXO and the internal PLL structure.

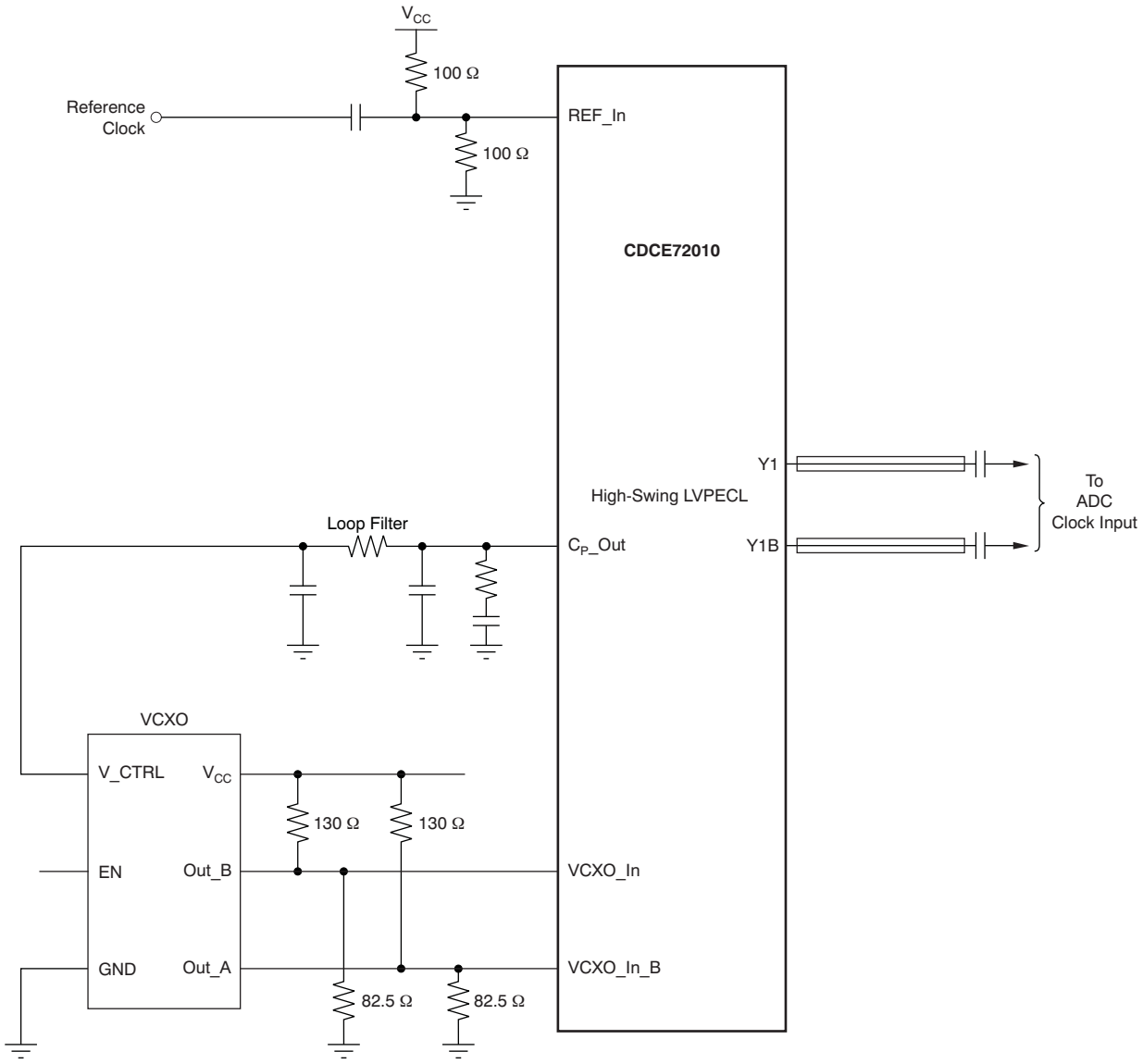

Figure 7. CDCE72010 Interface to ADCs for Low-/Mid-IF Input Frequencies

For high-IF input frequencies to the ADC, the CDCE72010 output can be configured as an LVCMOS signal and interfaced to the ADC as shown in Figure 8. The crystal filter removes excessive noise from the clock signal; because of its high insertion loss, an LVCMOS clock is recommended for larger filtered clock amplitude. The 4:1 transformer after the crystal filter then converts the single-ended signal to a differential signal and also boosts the amplitude. The crystal filter works best for matched 50-Ω loads, and thus care should be taken to match the lines to 50 Ω.

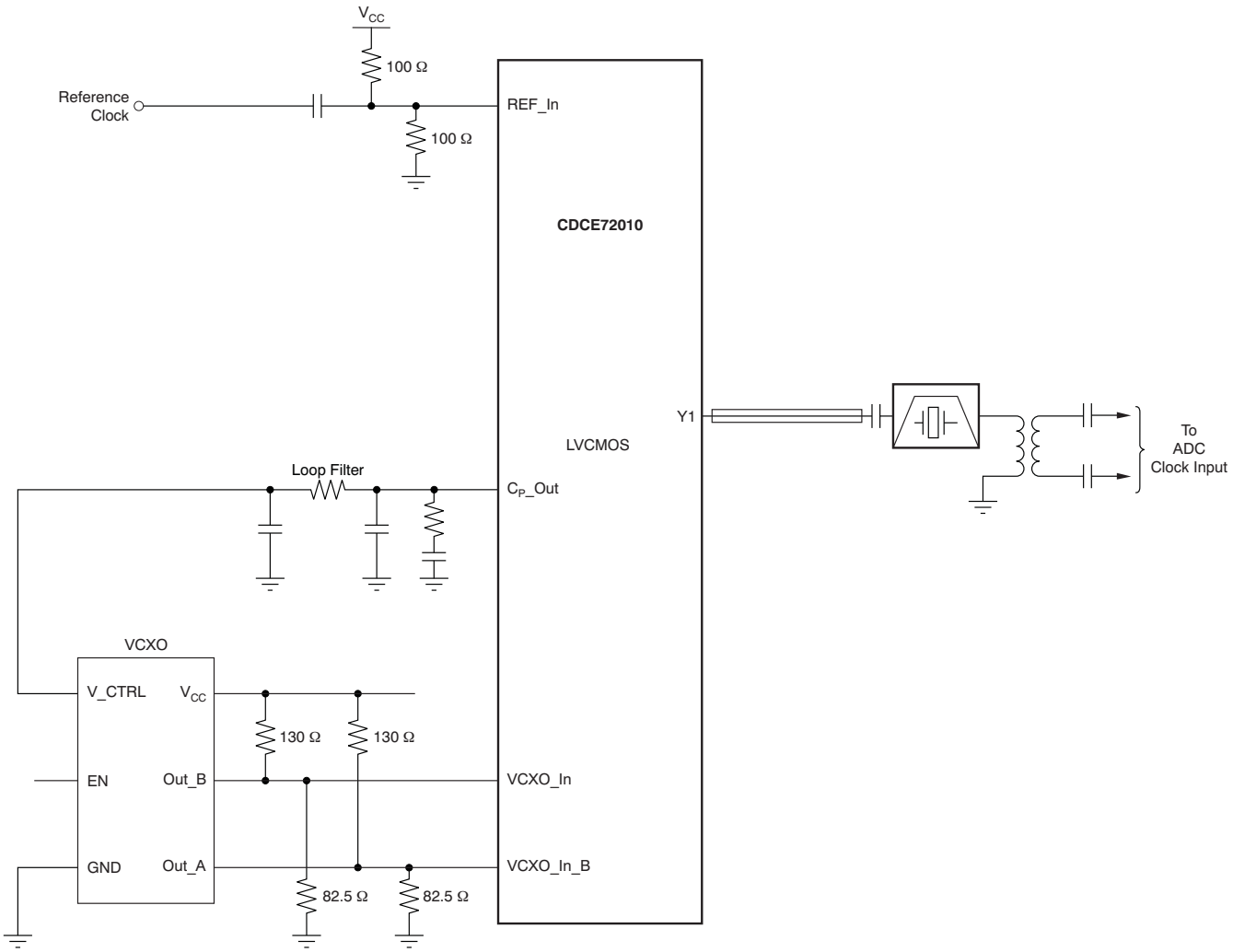

Figure 8. CDCE72010 Interface to ADCs for High-IF Input Frequencies

6 CDCE72010 Clock Source for the ADS5483

To illustrate the performance of the CDCE72010 clocking solution, the device is coupled with the Epson-Toyocom 122.88-MHz VCXO and supplies the clock signal to the ADS5483. The data are then compared to the baseline performance using an extremely good phase-noise generator with a crystal band-pass filter. The test setup is shown in Figure 9.

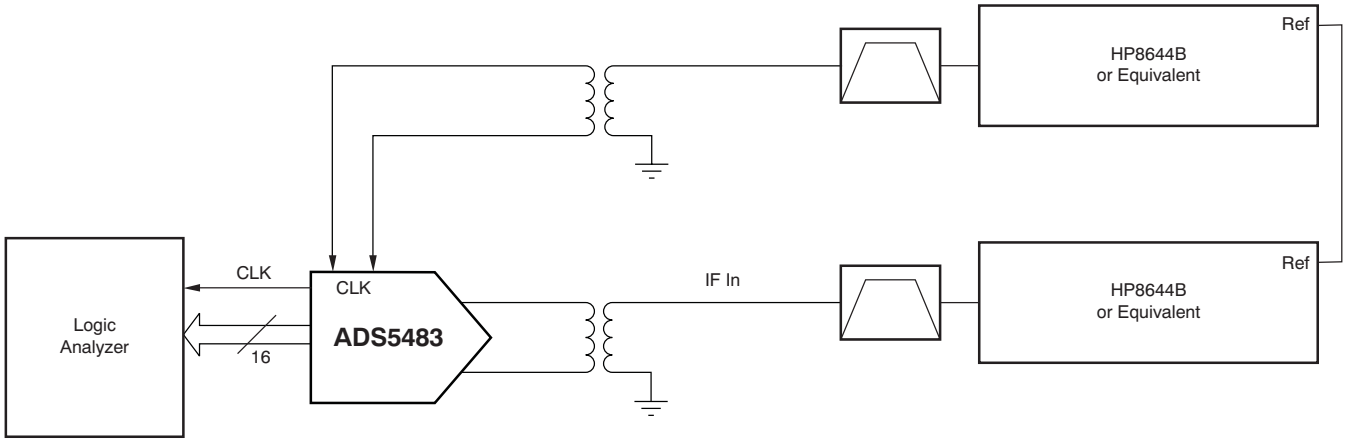

Figure 9. ADC Evaluation Test Setup (Baseline)

The measured performance of the device over frequency with a near-ideal clock source is compared to the performance using the CDCE72010 as a clock source. The block diagram of the ADC test setup that incorporates the CDCE72010 is shown in Figure 10.

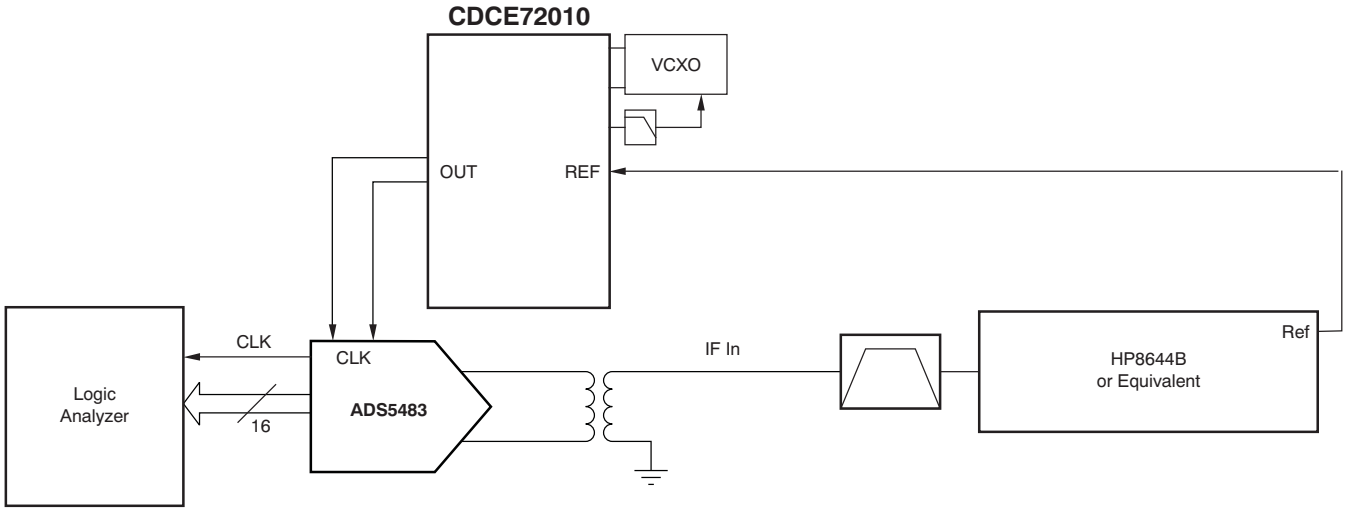

Figure 10. ADC Evaluation Test Setup with the CDCE72010 as Clock Source

The measured results for the ADC SNR and spurious free dynamic range (SFDR) are shown in Table 1.

Table 1. SNR and SFDR Measurements on ADS5483

Frequency (MHz)	SNR (dBFS)		SFDR (dBc)	
	Baseline	CDCE72010	Baseline	CDCE72010
30	78.5	78	95	93
70	78	75.8	93	91
100	77.6	74.2	87	84
130	77	72.7	84	80

Figure 11 compares the SNR results to frequency; Figure 12 displays the spectral plot of the performance at 30 MHz.

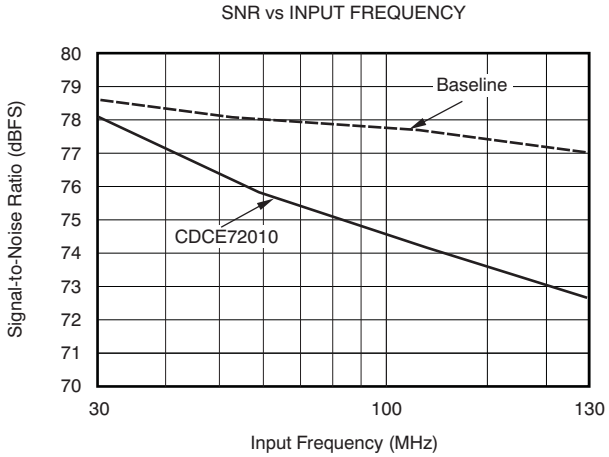

Figure 11. SNR Performance vs IF Input Frequency

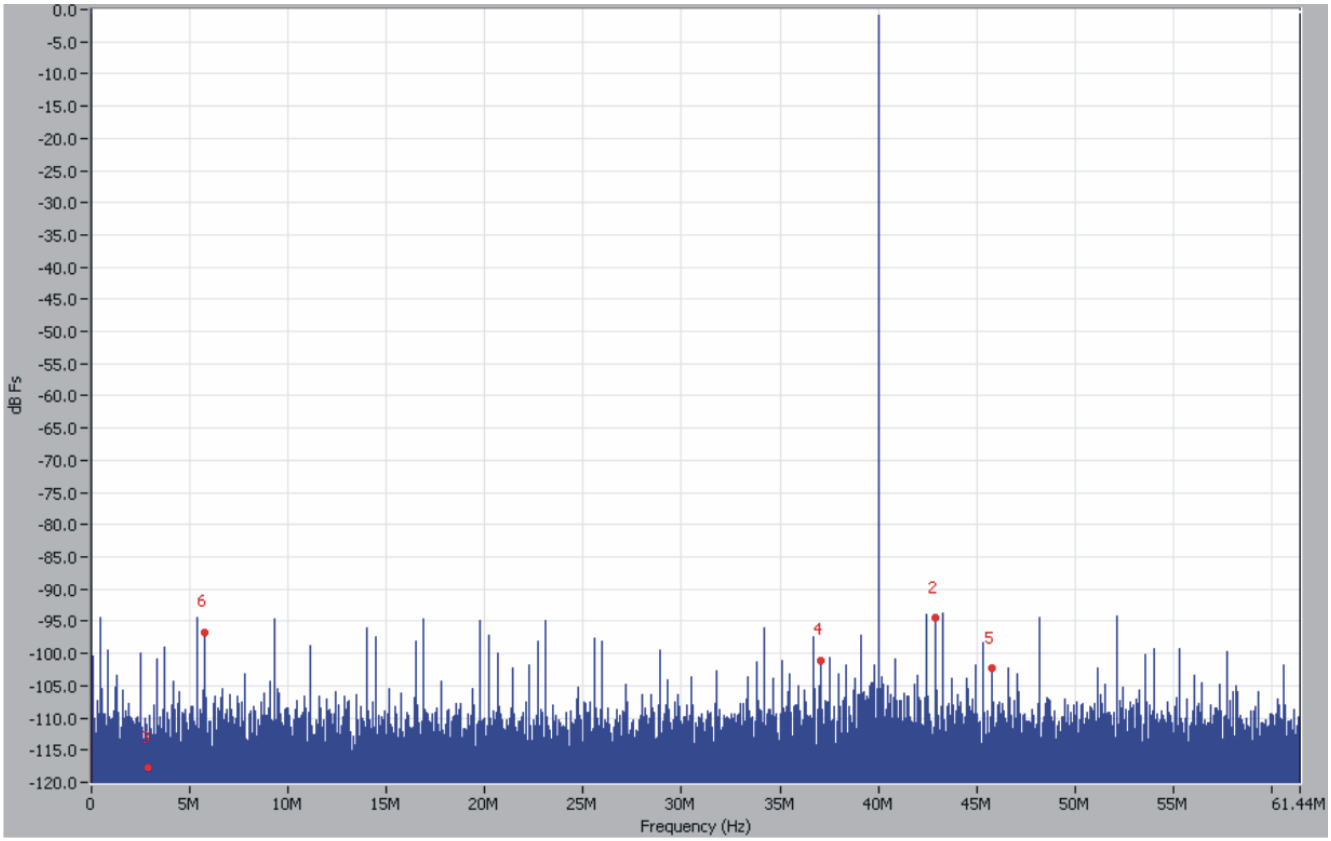

Figure 12. Spectral Performance with the CDCE72010 Clock Source at 30-MHz IF Input

If the IF input frequency is less than the first Nyquist zone (or 60 MHz for this sampling rate), the CDCE72010 provides a suitable clock source to achieve SNR values that are close to the baseline performance. As expected from the analysis in Section 2, the desired performance degrades at higher IF frequencies. Because the jitter associated with the CDCE73020 is not quite as good, SNR degradation is more severe when operating at higher IF frequencies. The SFDR performance is similar to that shown in the baseline case and does not degrade over higher IF frequencies.

7 Performance Improvements

7.1 Improved Jitter

One method to achieve performance improvements is to use a lower phase noise (or lower jitter) oscillator source. This option can be achieved by using a lower jitter VCXO or VCSO (voltage-controlled SAW oscillator) device. Note that the CDCE72010 is capable of dividing down any output, so that the oscillator frequency could be a much higher multiple of the desired clock, and thus lower the phase noise floor of the divided down clock. This method is useful for SAW oscillators that generally operate at 500 MHz and above. For lower sampling frequencies,tje use of LVCMOS VCXOs improves output clock jitter/phase noise, because LVCMOS VCXOs typically have lower phase noise floors than either LVPECL or LVDS VCXOs.

7.2 Lower Thermal Noise

As seen in Section 3, minimizing thermal noise on the clock improves the phase noise and the SNR performance. This technique is achieved by placing a narrowband crystal filter after the CDCE72010 LVCMOS output. The filter used for this investigation is an Epson-Toyocom TF2-C2EC1 122.88-MHz crystal filter with approximately 20 kHz of total pass bandwidth. The crystal filer introduces about 6dB of insertion loss. As previously discussed, the combination of the filter insertion loss and conversion from a square-wave output to a sine-wave output reduces the transition slope of the clock waveform. The benefit of the added filter is negated by the insertion loss and the loss of the signal slope. Adding a 4:1 transformer just after the filter compensates for the loss of the filter, and provides steep clock transitions. It also converts the single-ended filtered clock output to a differential signal.

The phase noise of the CDCE72010 LVPECL output (with an LVPECL VCXO) is shown in Figure 13; the CDCE72010 LVCMOS output (with an LVPECL VCXO), coupled with the filter, is shown in Figure 14. Comparing both figures, it can be seen that below the corner frequency of the band-pass filter, the performance between the two cases is nearly identical. Once the corner frequency is reached, phase noise of filtered clock output improves and rivals that of a near-identical source.

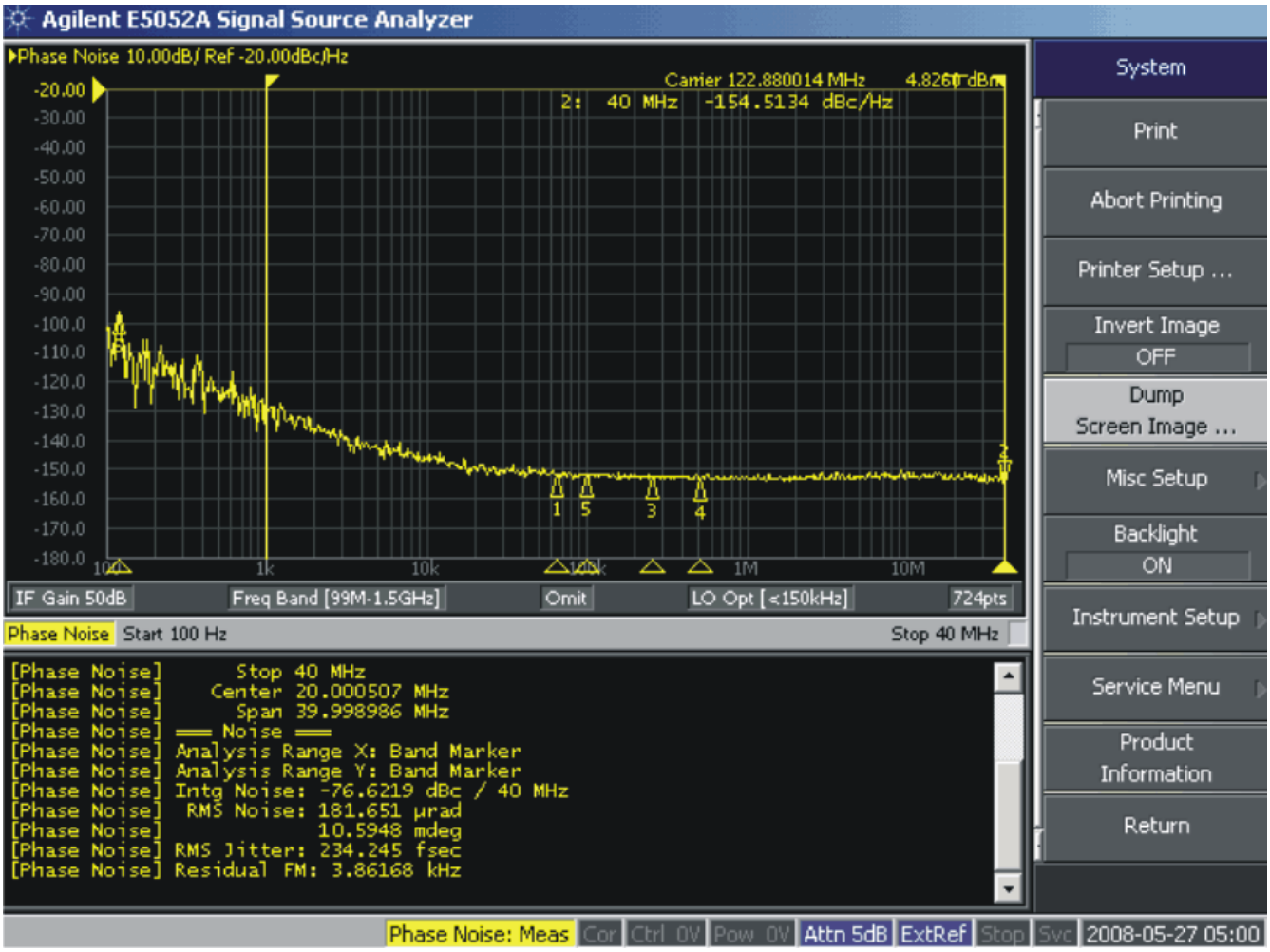

Figure 13. CDCE72010 122.88-MHz HS-LVPECL Output Phase Noise

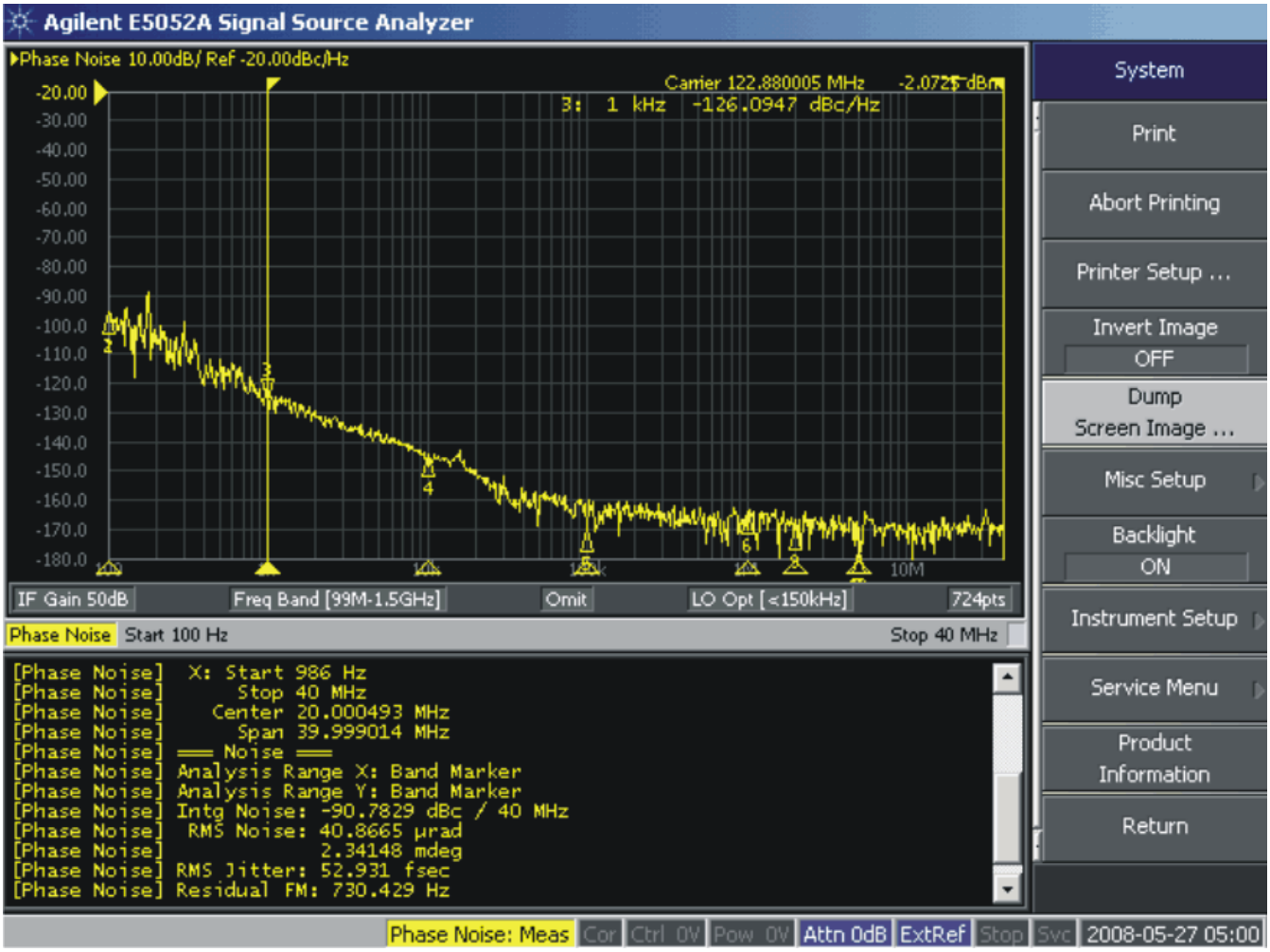

Figure 14. CDCE72010 122.88-MHz Filtered LVCMOS Output Phase Noise

The ADS5483 device was measured using the CDCE72010 with an LVPECL VCXO and the crystal filter-transformer network. The performance was measured over higher IF input frequencies; Table 2 shows the results.

Table 2. SNR and SFDR Measurements on ADS5483 with Modified Clock Source

Frequency (MHz)	SNR (dBFS)		SFDR (dBc)	
	Baseline	CDCE72010-BPF-Transformer	Baseline	CDCE72010-BPF-Transformer
70	78	77.8	93	93
100	77.6	77.2	87	87
130	77	76.5	84	84

Figure 15 compares the result of the device measured with the near-ideal clock and the CDCE72010 with a crystal filter and transformer.

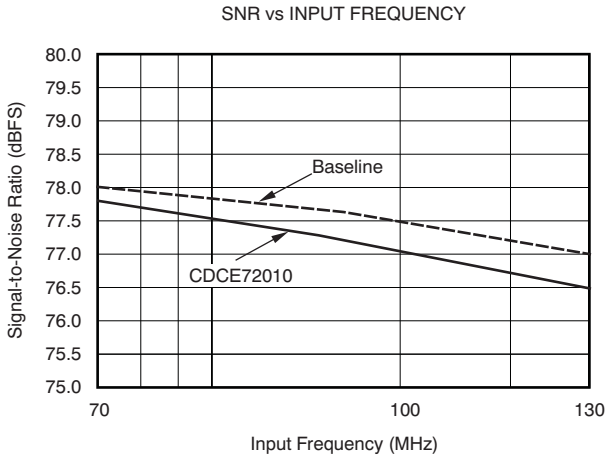

Figure 15. SNR Performance vs IF Input Frequency

Usng the crystal filter-transformer combination improves the SNR performance up to 5 dB at high-IF frequencies and closely matches the baseline performance. SNR performance of 75 dBFS or greater is achieved up to 130-MHz IF. The spectral plot of the performance at 130-MHz IF is shown in Figure 16.

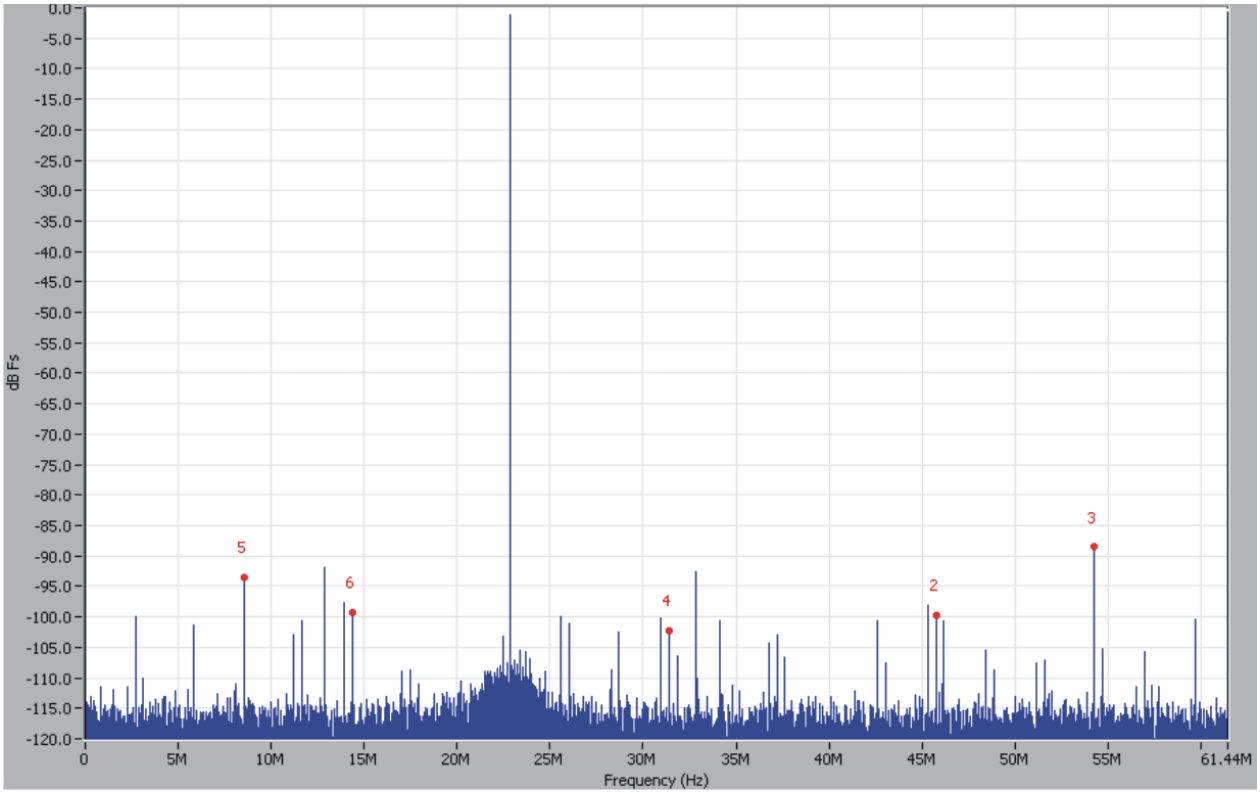

Figure 16. Spectral Performance with the CDCE72010-BPF-Transformer at 100-MHz IF Input

8 Conclusion

The CDCE72010 device is a clock synthesizer and distribution chip that satisfies the most stringent clocking requirements for high-end ADCs such as the ADS5483. For applications with the input frequency within the first Nyquist zone, the CDCE72010 is a suitable clock for the ADC device to achieve excellent performance. For applications that require a high-IF input frequency, the performance degrades in a linear fashion with respect to frequency. This degradation can be eliminated by including a narrowband filter, such as a crystal band-pass filter, at the output of the CDCE72010 along with a transformer to ensure sufficient clock amplitude. With this technique, near-ideal ADC performance is achievable with any desired IF frequency. Further, this technique provides an inexpensive real-world solution to clock high-speed ADCs at high-IF frequencies. Additionally, the CDCE72010 can supply the clock signal not only to the ADCs, but also the other sampled systems within the design.

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