Application Report
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Why Oversample when Undersampling can do the Job?

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ABSTRACT

System designers most often tend to use ADC sampling frequency as twice the input signal frequency. As an example, for a signal with 70-MHz input signal frequency with 20-MHz signal bandwidth, system designers often use more than 140 MSPS sampling rate for ADC even though anything above 40 MSPS is sufficient as the sampling rate. Oversampling unnecessarily increases the ADC output data rate and creates setup and hold-time issues, increases power consumption, increases ADC cost and also FPGA cost, as it has to capture high speed data.

This application note describes oversampling and undersampling techniques, analyzes the disadvantages of oversampling and provides the key design considerations for achieving the required ADC dynamic performance working with undersampling.

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1 Introduction

1.1 What is Oversampling?

As per Nyquist sampling theorem, a signal must be sampled at a rate greater than twice its maximum frequency component in order to ensure unambiguous data. If the Nyquist criterion is not met, aliasing will occur. Say, for example, if the maximum frequency of a sine wave is 70 MHz, then the minimum sampling frequency required is 140 MSPS, as per Nyquist criteria. If we use this Nyquist criterion, that is, the sampling frequency is sufficiently high which will not have any overlapped frequency components in the frequency domain; it is called normal sampling or oversampling. 2 × Fmax is called the Nyquist sampling rate where Fmax is the maximum frequency component in the signal. Also, the Fmax is called the Nyquist frequency. Nyquist rate is the minimum sampling rate to avoid aliasing.

The aliasing concept is explained in detail in *High-Speed, Analog-to-Digital Converter Basics* (SLAA510) with diagrams both in time and frequency domain. Please refer to pages 5–7 in that application note for a clear understanding of the aliasing concept. Understanding the aliasing concept will help while going through the rest of this document.

1.2 What is Undersampling?

If we use the sampling frequency less than twice the maximum frequency component in the signal, then it is called undersampling. Undersampling is also known as band pass sampling, harmonic sampling or super-Nyquist sampling. Nyquist-Shannon Sampling theorem, which is the modified version of the Nyquist sampling theorem, says that the sampling frequency needs to be twice the signal **bandwidth** and not twice the maximum frequency component, in order to be able to reconstruct the original signal perfectly from the sampled version. If B is the signal bandwidth, then Fs > 2B is required where Fs is sampling frequency. The signal bandwidth can be from DC to B or from f1 to f2 where B = f2 – f1.

The aliasing effect due to the undersampling technique can be used for our advantage. When a signal is sampled at a rate less than twice its maximum frequency, the aliased signal appears at Fs – Fin, where Fs is the sampling frequency and Fin in the input signal frequency. In the above case, if we sample the 70-MHz signal with 100 MSPS sampling rate, the aliased component will appear at 30 MHz (100 – 70). As we know in advance that the signal is aliased, we can recover the actual frequency by using the Fs – Fin relationship. The undersampling technique allows the ADC to behave like a mixer or a down converter in the receive chain. For a band-limited signal of 70 MHz with a 20-MHz signal bandwidth, if the sampling rate (Fs) is 100 MSPS, the aliased component will appear between 20 MHz to 40 MHz (30 ±10 MHz).

2 Oversampling Disadvantages

We will use the example of a 70-MHz signal with 20-MHz bandwidth (60 MHz to 80 MHz) for the discussion throughout this paper. For a radar application and for communication systems, generally 70 MHz is used as IF (intermediate frequency) with a specific bandwidth ranging from a few KHz to a few MHz. The maximum frequency component is 80 MHz in this signal. For an oversampling case, the minimum sampling rate is more than 160 MSPS. To keep this band of 60 MHz to 80 MHz in the middle of the first Nyquist Zone, the sampling frequency is 280 MSPS. This signal in frequency domain is shown in Figure 1.

Every Fs/2 zone starting from DC to Fs/2 is called the Nyquist Zone. The first Nyquist Zone is from DC to Fs/2, the second Nyquist Zone is from Fs/2 to Fs, and the third Nyquist Zone is from Fs to 3Fs/2, and so on.

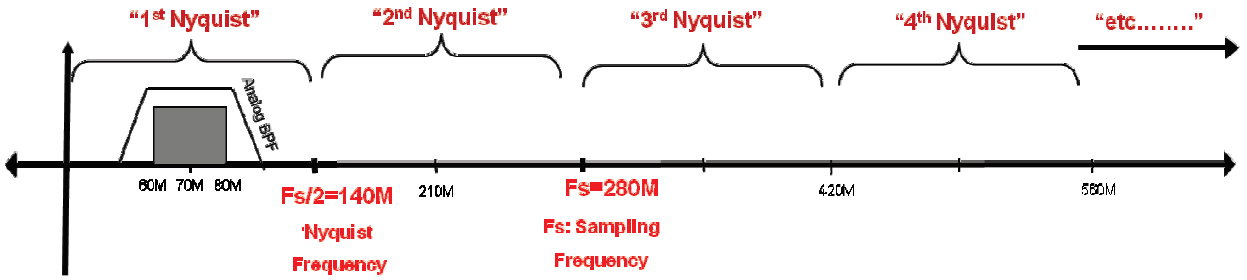


Figure 1. Normal Sampling (Oversampling) Case: IF Frequency in the Center of Nyquist Zone

To decrease the sampling rate in the oversampling case, even if the signal bandwidth need not to be in the middle of first Nyquist Zone, the minimum sampling frequency is around 200 MSPS (not 160 MSPS) for a practical application for taking care of band-pass filter design. This is shown in Figure 2.

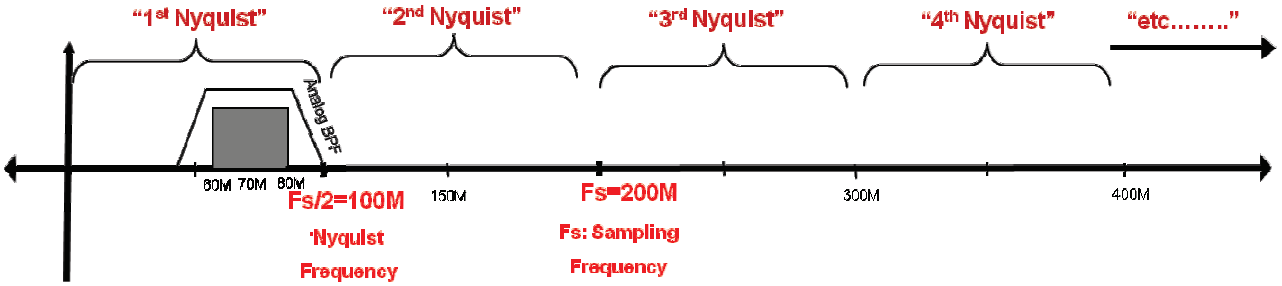
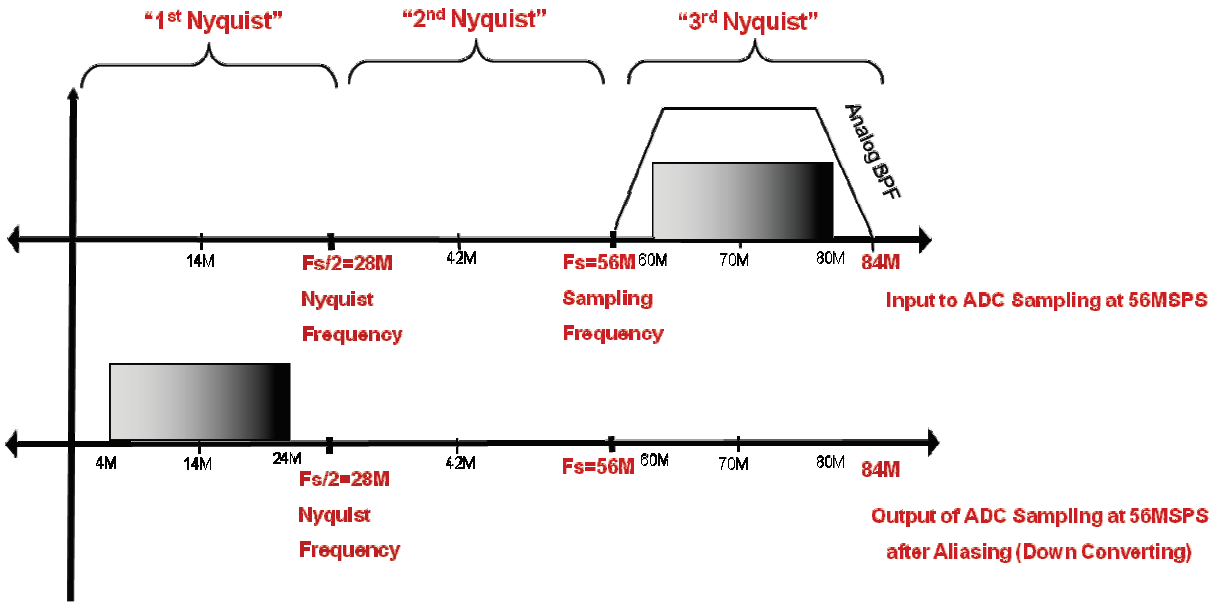


Figure 2. Practical Case of Normal Sampling (Oversampling) for Taking Care of the Band-Pass Filter

The same signal can be sampled at more than 40 MSPS, for example, 56 MSPS for keeping the signal in the center of third Nyquist Zone using the Undersampling technique. This is shown in Figure 3.



NOTE: The ADC is sampled at 56 MSPS. The aliased signal in the first Nyquist Zone is centered at 14 MHz with 20-MHz bandwidth.

Figure 3. Undersampling Case of 70-MHz IF Signal with 20-MHz Bandwidth

As shown in Figure 3, 70-MHz IF in the third Nyquist Zone is aliased back in the first Nyquist Zone centered at 14 MHz with a 56-MSPS undersampling rate. A digital down-converter (DDC) can recover this signal for digital frequency mixing for converting down to baseband and further digital filtering. TI's GC6016 or an FPGA can implement this DDC function. Many radio designers take full advantage of this undersampling technique for eliminating an entire analog frequency down-conversion stage, thus saving board space, power, and money. The signal is not spectrally inverted in this case as can be seen from Figure 3. The signal will not invert when it is in odd Nyquist zones like 3rd, 5th and so on. The spectral inversion happens when the signal band is in even Nyquist Zones like 2nd, 4th and so on. This spectral inversion is not a bad thing or disadvantage as this can be inverted back again in the digital domain inside the GC6016 receive block or inside the FPGA after receiving the data from the ADC. In some applications this spectral inversion impacts on the demodulating process and eventually causes serious problems when analyzing the signal quality such as EVM (Error Vector Magnitude). Spectral-wise, this inversion is not a problem as long as the spectrum has a good spectral flatness within in-band but a serious issue when demodulated for measuring EVM.

Make sure that the entire signal band is within the single Nyquist Zone and not spread across two Nyquist Zones. If the entire signal bandwidth is not within the single Nyquist Zone, it is an example of bad aliasing and the aliased component in the first Nyquist Zone cannot be retrieved by any DDC.

Details of oversampling disadvantages compared to undersampling are provided in the following subsections.

2.1 Higher Sampling Rate Increases the Data Rates to FPGAs

Generally, FPGAs are used to capture the data output from the ADCs. As the sampling rate of the ADC increases, the data rates to FPGA will also increase. This will impact the selection of the FPGA and in turn, the cost of the FPGA for the system designers. For the 60- to 80-MHz signal, the sampling rate of 200 MSPS due to the oversampling will increase the data rates to FPGA compared to the undersampling sampling rate of 56 MSPS. As the data rates increase, the layout of the boards, the signal routing and the placement of ADC and FPGA in the design needs to have the utmost care.

2.2 Setup and Hold Time Issues

As the speeds of the data rates are higher due to oversampling, the setup and hold times are critical for the ADC data capture inside the FPGA. The datasheets of the ADC and FPGA have the setup and hold time numbers for a specific sampling rate. The minimum setup and hold time provided by ADC needs to be accepted by the FPGA to properly capture the data. Some system designers use the typical numbers in the datasheet which is not the correct practice. They should always look at the minimum values for the setup and hold times in the datasheet for a reliable design of data capture inside the FPGA.

For the lower power consumption ADS4149 ADC, which samples at 250 MSPS, the setup and hold times are given in Table 1 for 200 MSPS and other sampling frequencies:

Table 1. LVDS Timing Across Sampling Frequencies

Sampling Frequency (MSPS)	Setup Time (ns)			Hold Time (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
230	0.85	1.25		0.35	0.6	
200	1.05	1.55		0.35	0.6	
185	1.1	1.7		0.35	0.6	
160	1.6	2.1		0.35	0.6	
125	2.3	3		0.35	0.6	
80	4.5	5.2		0.35	0.6	

FPGA needs to accept the setup time of 1.05 ns minimum and hold time of 0.35 ns minimum to capture the data properly for the oversampling case of 200 MSPS which is a critical requirement, whereas for the undersampling case of 56 MSPS, from Table 1, the setup time is more than 4.5 ns which is a more relaxed specification compared to the oversampling case of 200 MSPS.

2.3 Marginal Capturing Issue

When the data is captured without the sufficient setup and hold time of LVDS data then it is called marginal capturing. Due to higher data rates, long trace lengths, and mismatch between the trace lengths between the LVDS lines of data and clock, the setup and hold times will vary at the FPGA input and marginal capturing of the data can happen. During marginal capturing, some of the data bits may change its value, which is equivalent to providing improper ADC data to FPGA. The marginal capturing problem can be resolved by two methods. One method is to use the ADC LVDS features for changing the delays of LVDS data lines with respect to LVDS output clock. The other method is to use the delay elements inside the FPGA.

2.4 Higher Power Consumption

Increase in the data rates will increase the power consumption of the ADC. Power consumption always needs to be kept lower for most of the applications in defense and wireless infrastructure. Pipeline ADCs are used in these applications and these ADCs comparatively consume more power to get the required performance. Selection of oversampling will further increase the power consumption in the system. For hand-held software defined radio operating on a battery, the lowest power consumption of the ADC is most desirable as the receiver path is always enabled unlike the transmitter path. Similarly, for the battery operated test instruments, the lowest power consumption ADC is required. As shown in Figure 4, as the sampling rate increases, the power consumption of the ADS4149 is increasing. In the 56 MSPS case of undersampling and 200-MSPS oversampling example, the power consumption of the device is more than double, as can be seen in Figure 4.

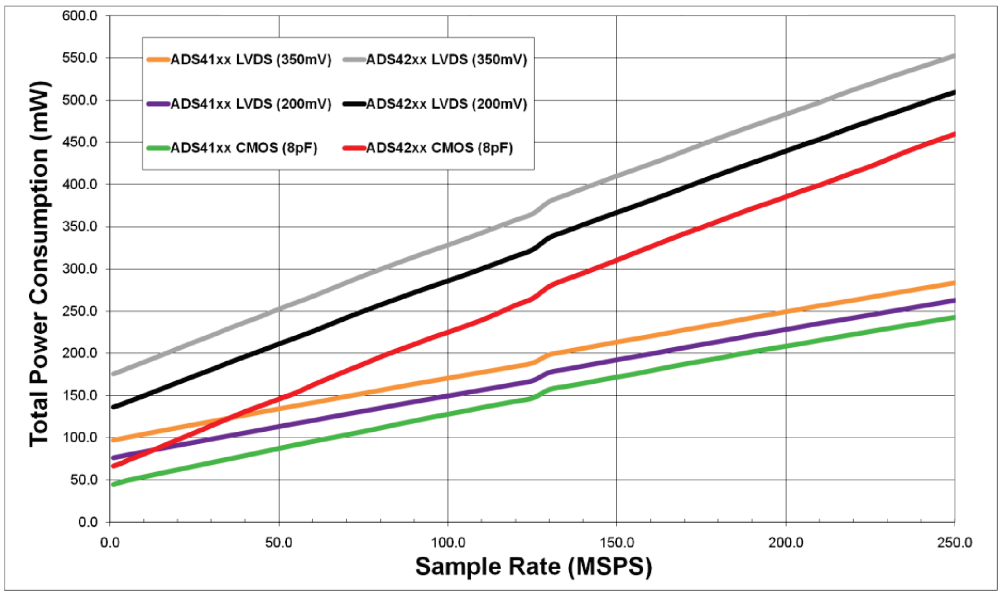
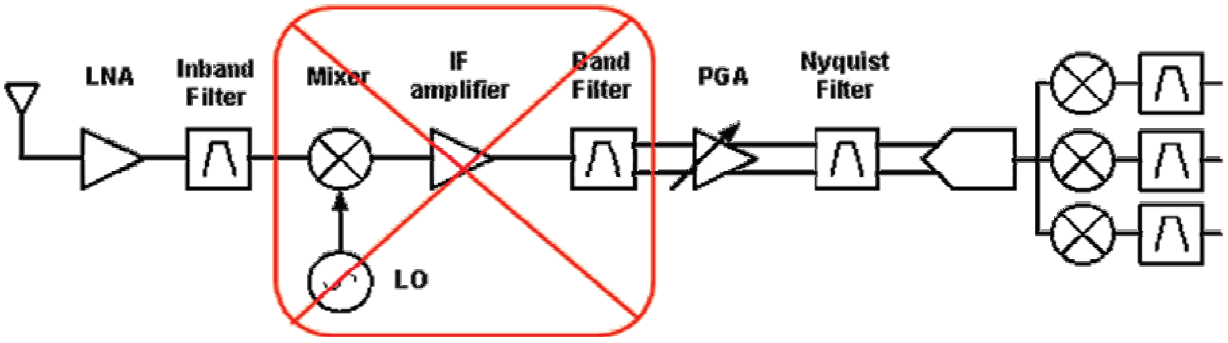


Figure 4. ADC Sampling Rate versus Power Consumption for ADS4xxx Family of ADCs

2.5 Additional Down Converter Stage Requirement

Some of the radio designs use the one down converter stage for converting the 70-MHz IF signal to a lower IF frequency, say 14 MHz. This is illustrated in Figure 5. By using the undersampling technique, this stage can be eliminated. As shown in Figure 3, by sampling the 70-MHz IF with a 56-MSPS sampling rate, the aliased component is at 14 MHz, which can be recovered. In this way, the ADC itself works as a down converter without using any additional down converter stage in front of the ADC. This is the advantage of a “good aliasing” result of undersampling technique.



NOTE: The mixer is used to convert the 70-MHz IF1 down to 14 MHz IF2. The undersampling technique removes this stage of down conversion and 70 MHz is directly given to ADC.

Figure 5. Radio Input Frequency 70-MHz IF with 20-MHz Bandwidth

2.6 Cost of the ADC

Oversampling increases the cost of the ADC. By using the above example of 70-MHz IF with 20-MHz , the sampling rate for the undersampling case is 56 MSPS whereas for the oversampling case it is 200 MSPS. The cost of 200 MSPS ADC is at least twice the cost of the 56 MSPS ADC which is an additional cost for the system designers. By effectively using the undersampling technique and designing the proper filter, the cost of the ADC can be reduced.

3 Are there any Advantages of Oversampling?

Yes. There are some specific advantages of oversampling which are described below.

3.1 Processing Gain

When the signal is oversampled a greater number of times than its signal bandwidth, then the processing gain is achieved in addition to the SNR shown in the ADC datasheets. For example, for the ADS4149, at 70 MHz, the SNR will be around 72 dB at the sampling rate of 200 MSPS. For our example of 70 MHz with 20-MHz bandwidth, the signal is oversampled by 10 times with respect to signal bandwidth. Note that with respect to the signal frequency of 70 MHz, it is oversampled only around 3 times.

Due to oversampling of 10 times to the bandwidth, system designers get the extra advantage of processing gain in addition to the actual SNR mentioned in the datasheet. For Fs of 200 MSPS, the SNR of 72 dB is for a Nyquist bandwidth of Fs/2, that is, 100 MHz. For the measurement of SNR of the ADC, the noise in the entire band of 100 MHz is considered in this case.

The processing gain is achieved by using the following formula:

Process Gain = 10 log ((Fs/2)/BW)

Where

Fs is the sampling Rate;
BW is the signal bandwidth;

For the oversampling example, BW is 20 MHz, Fs is 200 MHz. If we use the above formula, the processing gain is around 7dB. The total SNR can be calculated using the following formula:

SNR_{total} = SNR_{ds} + Process Gain

Where SNR_{total} is the total SNR after adding the processing gain and SNR_{ds} is the SNR value provided in the datasheet (without the processing gain).

SNR_{total} is 79 dBFS (72 + 7) using the above formula.

3.2 Frequency Plan Flexibility

With oversampling, the advantage is the frequency plan. System designers can select the IF frequency location wherever required in the first Nyquist Zone based on the availability of passive filter modules at that frequency and for optimizing selection of ADC front end circuit design in that frequency band. The IF frequencies can always be moved anywhere from DC to Fs/2 frequency, with an eye on keeping the flexibility on the filter design. The second and third harmonics of the 70-MHz IF falls out of the first Nyquist Zone and can be easily filtered in the oversampling case of 200 MSPS sampling rate. Whereas, in the undersampling case, the system designers must plan the filter design in such a way that the HD2 and HD3 impacts are minimal. The ADC input filter design has to take care of this distortion issue in the undersampling case.

3.3 Handling Higher Signal Bandwidths

The another inherent advantage of oversampling is the capability of handling higher-signal bandwidths. For the oversampling case of 200 MSPS, the ADC can handle around 100-MHz signal BW. This BW is called Nyquist BW. But as per our example case, the signal BW is only 20 MHz and hence the sampling rate of 56 MSPS will be good enough. For the TI ADC12D1600 ADC, the Nyquist BW is 1600 MHz with a sampling rate of 3200 MSPS. This type ADC is generally used for handling very high signal BWs for radio applications. Designers must make the right sampling rate choice for their specific design. The key thing to remember is keeping the entire signal BW inside a single Nyquist Zone for avoiding the bad aliasing effects and keeping the signal BW in the middle of any particular Nyquist Zone for flexibility in the filter design.

4 Undersampling Advantages

All six oversampling disadvantages mentioned in Section 2 become the advantages of the undersampling technique. The key advantages of undersampling include; the power consumption for the ADC is lower, the ADC cost is lower, easy capturing of ADC data due to relaxed setup and hold times, and easy interface to FPGAs due to lower speeds.

5 Key Design Considerations for System Designs Using Undersampling

As seen, the undersampling has advantages compared to oversampling. But there are certain challenges/disadvantages with undersampling. The analog anti-aliasing low pass filter design is easier with oversampling versus the tight narrow band BPF requirements of the undersampled system. Depending on the IF frequency and the BW, this can be a big challenge in the undersampling case, to get good narrow band filters with good differential response which could affect HD performance a lot. We will discuss this in Section 5.1, after checking the SNR and SFDR performances of oversampling and undersampling cases.

The SNR and SFDR performance measurements of ADS4149 are shown in Figure 6 and Figure 7.

Figure 6 clearly indicates that undersampling can be used without much degradation in the SNR performance for ADS414x.

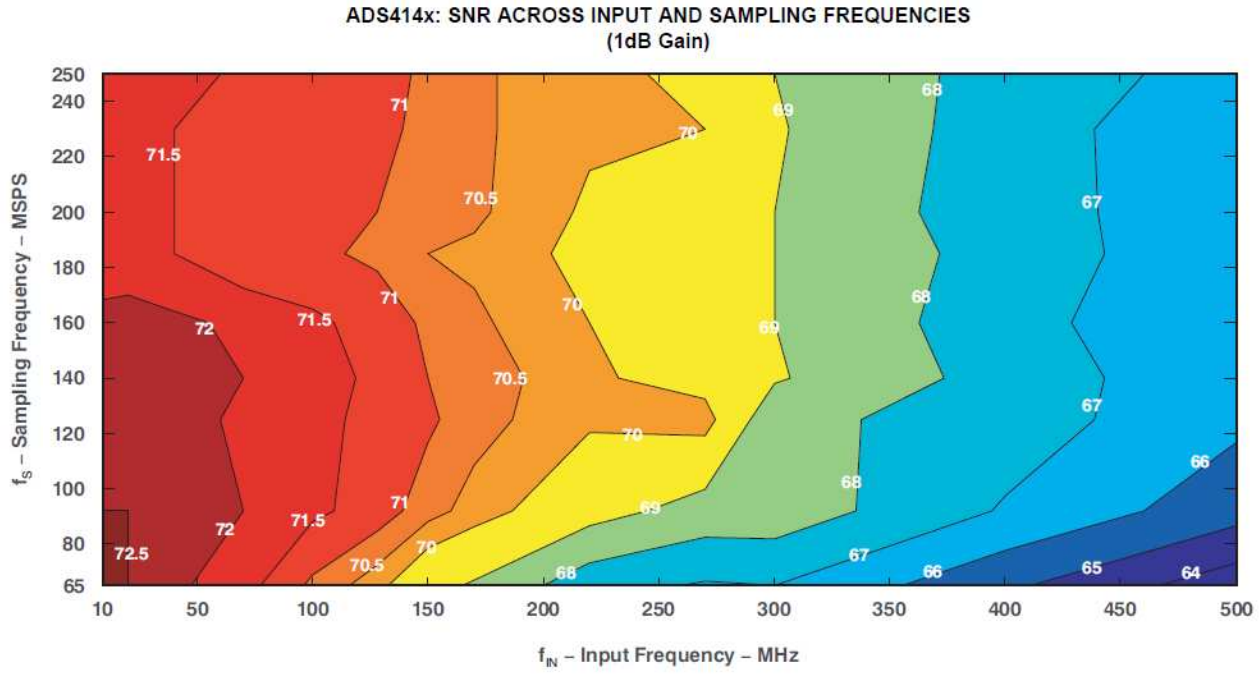


Figure 6. ADS414x SNR for 70-MHz IF Input and Across Sampling Frequencies

Figure 7 clearly indicates that the undersampling can be used without much degradation in the performance for ADS414x SFDR at 70-MHz IF input and across sampling frequencies.

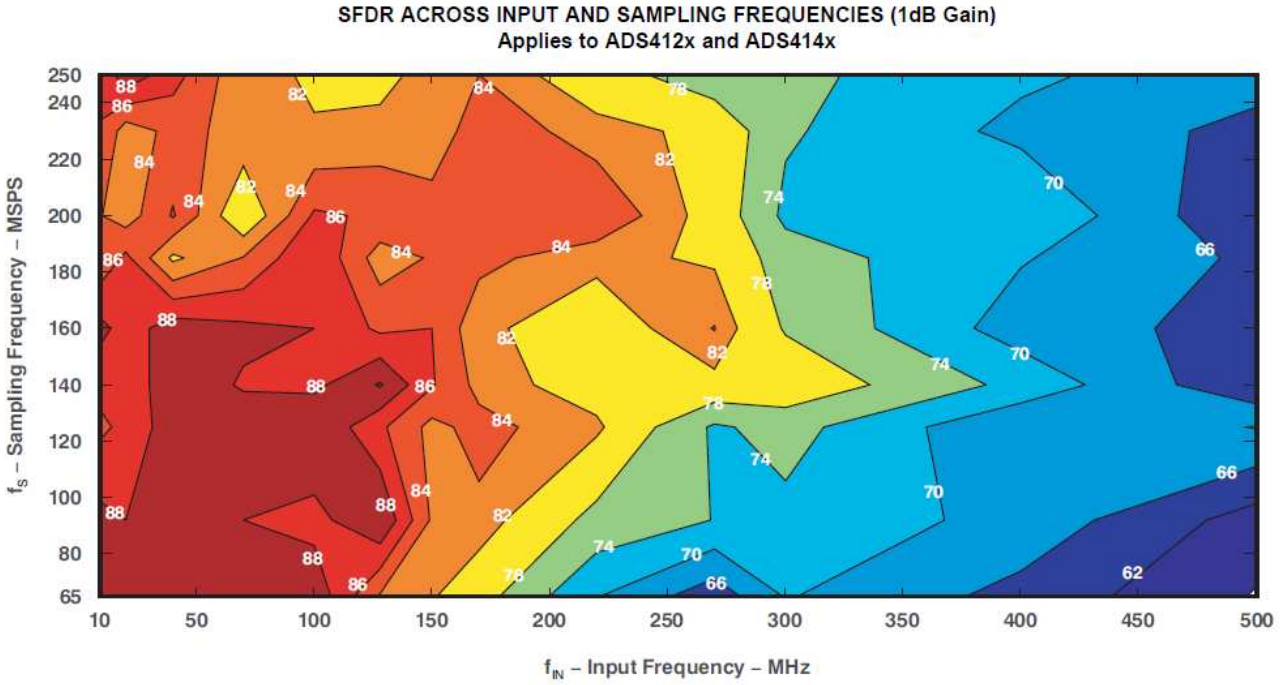


Figure 7. ADS414x SFDR for 70-MHz IF Input and Across Sampling Frequencies

For a wideband signal, the filter design needs to be taken care for HD2 and HD3 degradations to get the same performance similar to oversampling. The band-pass filter design in front of the ADC needs to make sure that the signal second and third harmonics and other frequency content are filtered out before feeding the signal to the ADC.

5.1 Analog Filter Design Considerations

We will consider our example case of 70-MHz IF and 20-MHz bandwidth for checking on the filter design requirements.

With the oversampling case of 200 MSPS, the 70 MHz is in the first Nyquist Zone and the filter can be easily designed in the first Nyquist zone. The second and third harmonics of 70 MHz falls well outside the first Nyquist Zone. A simple low-pass filter for the entire first Nyquist Zone (also called anti-aliasing filter) will remove the second and third harmonic components.

Whereas, in the undersampling case, the analog filter in front of the ADC should provide adequate attenuation for the harmonics. The analog filter for the 70-MHz IF with 3 dB lower and upper cutoff above the 20 MHz of signal BW (close to 30-MHz bandwidth for the filter) should reject the second and third harmonics of 70 MHz (that is, 140 MHz and 210 MHz) at the input of the ADC for getting good distortion performance.

Table 2 shows the HD2 and HD3 performance of ADC for 70-MHz IF input. The ADC HD2 is 85 dBc for HD2 and 82 dBc for HD3 at 70-MHz IF input. The 70-MHz-centered analog filter should reject the 140 MHz by well below 85 dBc and the filter should reject the 210 MHz by more than 82 dBc to not limit the HD2 and HD3 overall performance below what ADC can do. Basically, the filter should be designed in such a way that the input stage should not degrade the ADC HD2 and HD3 performance.

Table 2. ADS4149 Datasheet: HD2 and HD3 Performance

Second-harmonic distortion	HD2	f_{IN} = 10 MHz		91			89		dBc
		f_{IN} = 70 MHz		90			85		dBc
		f_{IN} = 100 MHz		88			84		dBc
		f_{IN} = 170 MHz	74.5	88		72	84		dBc
		f_{IN} = 300 MHz		79			75		dBc
Third-harmonic distortion	HD3	f_{IN} = 10 MHz		88			87		dBc
		f_{IN} = 70 MHz		87			82		dBc
		f_{IN} = 100 MHz		86			81		dBc
		f_{IN} = 170 MHz	74.5	82		72	82		dBc
		f_{IN} = 300 MHz		77			75		dBc

5.2 Positioning of ADC HD2 and HD3 Using Frequency Plan

With the proper input filter design, the SFDR is now entirely dependent on the ADC HD2 and HD3 performance and position of these HD components in the ADC output spectrum.

System designers need to plan the ADC sampling rate such that the aliased components of HD2 and HD3 from the ADC fall outside the signal bandwidth for better SFDR performance.

From the ADS4149 datasheet (SBAS483):

- ADS4149 SFDR at 70 MHz with HD2 and HD3: 82 dBc at 70 MHz
- ADS4149 SFDR at 70 MHz without HD2 and HD3: 88 dBc at 70 MHz

It shows there is an advantage of 6 dB SFDR without HD2 and HD3. This will help in wireless infrastructure designs where the system performance is limited by the ADC SFDR to potentially receive signals at very low power.

The TI frequency planning tool is available for download at:

http://focus.ti.com/docs/toolsw/folders/print/adc-harmonic-calc.html

5.3 Full-Power BW and Performance BW of the ADC

When using the undersampling technique, the system designer needs to check whether the ADC has adequate input bandwidth to use in the undersampling application. This input BW of the ADC is called full-power bandwidth where the input signal will have 3-dB loss at this frequency. Do not confuse full-power bandwidth with the input IF signal bandwidth. The full-power bandwidth or 3-dB bandwidth only provides the information that the ADC can handle up to this input signal frequency. This full-power bandwidth doesn't talk about the ADC performance at this frequency. The ADC performance needs to be verified in the ADC datasheet.

Performance bandwidth is the intended operating bandwidth or the maximum frequency where the ADC is already characterized and the results are provided in the datasheet. Figure 8 shows that the maximum analog input frequency is 800 MHz which is the full-power bandwidth of the ADS4149. Figure 8 also shows the maximum analog input frequency (full-power bandwidth) along with maximum analog input frequencies characterized for the ADS4149 as shown in the datasheet.

ANALOG INPUTS					
Differential input voltage range(1)		2		V_{PP}	
Input common-mode voltage		V_{CM} ± 0.05		V	
Maximum analog input frequency with $2V_{PP}$ input amplitude(2)		400		MHz	
Maximum analog input frequency with $1V_{PP}$ input amplitude(2)		800		MHz	

PARAMETER	TEST CONDITIONS	ADS4126 (160MSPS)			ADS4129 (250MSPS)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				12			12	Bits
SNR (signal-to-noise ratio), LVDS	f_{IN} = 10MHz		70.2			69.8		dBFS
	f_{IN} = 70MHz		70			69.7		dBFS
	f_{IN} = 100MHz		69.7			69.6		dBFS
	f_{IN} = 170MHz	66.5	69		65.8	69		dBFS
	f_{IN} = 300MHz		68			68		dBFS

Figure 8. ADS4149 Maximum Analog Input Frequency Datasheet Values

The ADC datasheet has SNR and SFDR graphs up to 500-MHz input frequency but once can easily notice that these values are reduced as the input frequency is increasing. One can consider this as the performance bandwidth of the ADS4149 where the performance is specified up to this frequency as specified in the datasheet. Generally, the full-power bandwidth exceeds the performance bandwidth for Pipeline ADCs like the ADS4149. The performance of any ADC above the performance bandwidth needs to be tested for a specific application and input signal conditions before finalizing the ADC. The ADC parameters; like its SFDR performance, SNR, and SINAD, are more important than the sampling rate itself for undersampling applications.

ADS4149 has 250 MSPS sampling rate and has input full-power bandwidth up to 800 MHz indicating system designers can select this ADC for the undersampling applications. For example, the input frequency of 300 MHz is the third Nyquist Zone for this ADC with the maximum sampling rate of 250 MSPS. The ADC datasheet performance shows that this ADC can be used in applications beyond fourth Nyquist Zone with the sampling rate of 250 MSPS.

The input bandwidth is the important criteria to check while selecting the ADCs for undersampling applications. All ADCs cannot work for undersampling. Some ADCs cannot be used for undersampling which are called Nyquist converters. These ADCs are usually high precision and have much slower sample rates. The other key thing to remember is that as the input frequency goes higher, the jitter requirements for the ADC clock are more stringent. Also, the aperture jitter of the ADC needs to be smaller for higher input frequency applications.

6 Conclusion

Undersampling provides many advantages for system designers compared to oversampling. With the proper understanding of the ADC full-power bandwidth, and with the proper design of the input filter for the ADC, and with proper positioning of the HD2 and HD3 components, undersampling can be effectively used in many defense and wireless applications.

System designers are encouraged to use undersampling as an alternate option to oversampling. Most of the recent ADCs are covering the SNR, SFDR specifications beyond its sampling rate, which clearly indicates that these ADCs can be used in undersampling applications. But system designers need to clearly understand the advantages and disadvantages of the undersampling before taking the decision on the specific sampling rate for the ADCs.

7 References

1. ADS4149 Datasheet (SBAS483)
2. HDx planning http://focus.ti.com/docs/toolsw/folders/print/adc-harmonic-calc.html

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