Designing a Small-Size and Cost-Optimized Multi-Channel Data Acquisition System

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In applications like patient monitoring, optical line cards, and test and measurement, there are several signals that need to be measured. This application note presents a cost optimized, low-power, and small-size solution for a multichannel data acquisition system. The *ADS8168* features a high-precision, 16 bit, 1 MSPS, SAR ADC with an eight channel multiplexer, low thermal drift voltage reference, precision reference buffer, and refby2 buffer for signal biasing.

Challenges in Signal Chain Design with Multichannel ADC

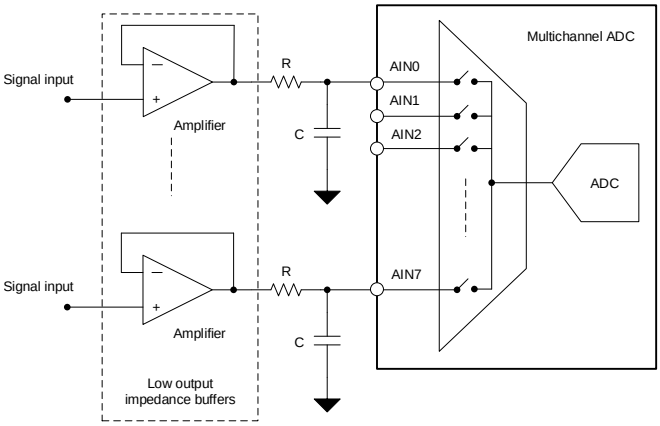


Figure 1. DAQ System Using Conventional Multichannel ADC

Figure 1 shows a typical multichannel data acquisition. Figure 2 shows the equivalent model for the MUX input channel AIN0 and ADC.

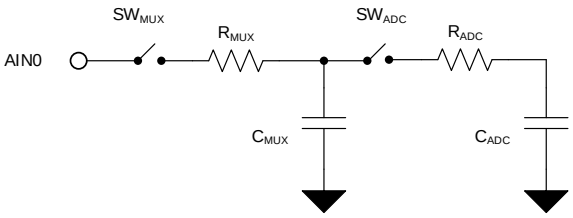


Figure 2. Equivalent Model of Channel AIN0 Connected to ADC

R_{ADC} is the resistance of sample-and-hold switch, SW_{ADC}, and C_{ADC} is the ADC sampling capacitor. R_{MUX} is the ON resistance of the MUX switch, SW_{MUX}, and C_{MUX} is the equivalent parasitic capacitance of the MUX.

When the sample-and-hold circuit connects to AIN0, a charge-kickback is created by the ADC sampling capacitor, C_{ADC}, and the MUX parasitic capacitor, C_{MUX}. The sampling capacitor of the ADC (typically 60 pF) is much larger than the MUX parasitic capacitance (typically 10 pF), hence ADC dominates the charge-kickback created at the MUX inputs.

To achieve a full sampling rate, the charge-kickback created by the ADC must be settled to be within 0.5 LSB of the ADC resolution. An ADC driver amplifier with more than 20-MHz bandwidth and low-output impedance is required to settle the charge-kickback. Every MUX input must be driven by an ADC driver amplifier to settle the charge-kickback.

The conventional circuit, shown in Figure 1, needs eight ADC driver amplifiers which increase system size, power, and cost. There is increased channel-to-channel performance mismatch as the amplifiers exhibit independent thermal drifts and offset errors. Refer to the *TI Precision Labs – ADCs* for more details on driving SAR ADC inputs.

Simplified Design with ADS8168

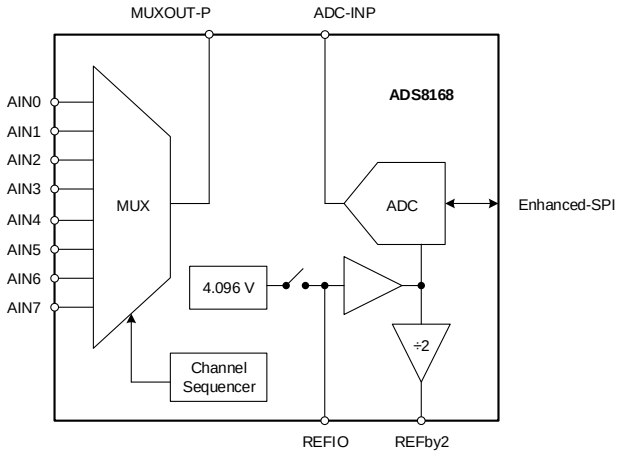


Figure 3. ADS8168 Block Diagram

The ADS8168 is a 16 bit, eight channel, SAR ADC with integrated reference and refby2 buffer and an *Enhanced-SPI* digital interface. For a complete list of devices in the ADS8168 device family, see Table 1. In ADS8168, the output of the multiplexer and ADC inputs are available to be used externally as shown in Figure 3. An ADC driver amplifier, common to all multiplexer channels, can be used as shown in Figure 4.

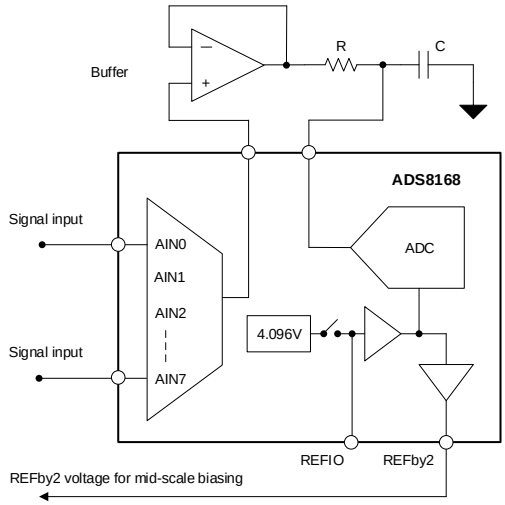


Figure 4. Low-Cost, Small-Size, Precision DAQ System Using ADS8168

Figure 5 shows an equivalent model of AIN0 and ADC. Charge-kickback from the ADC is settled by the ADC driver between the multiplexer output and the ADC input. Hence, there is no charge-kickback at the multiplexer inputs due to the ADC sampling capacitor.

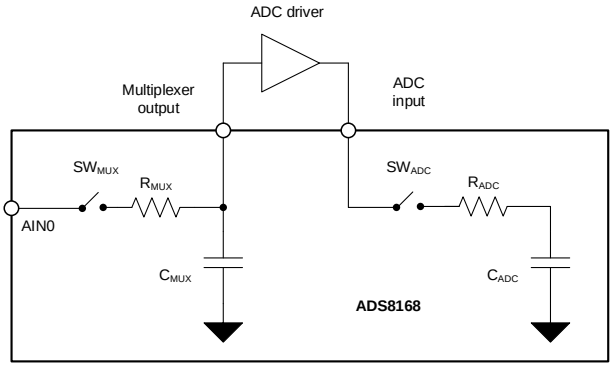
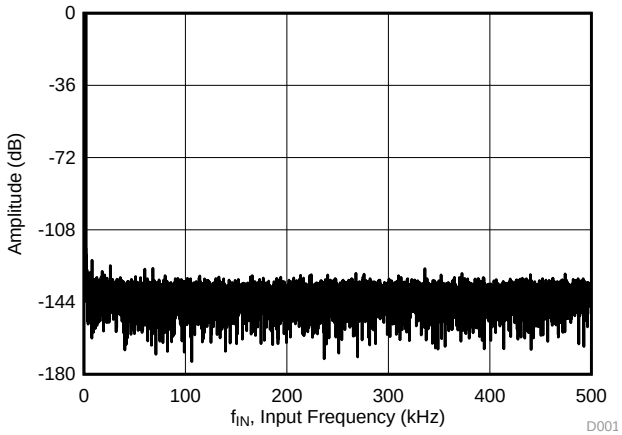


Figure 5. Equivalent Model of ADS8168 Analog Input

The ADS8168 supports extended settling time for analog signal inputs, which allows t_{CYCLE} – 100 ns settling time at the multiplexer inputs. See the section on *Early Switching for Direct Sensor Interface* in the ADS8168 datasheet for more details. The extended settling time and small charge-kickback at the multiplexer input enables connecting high-impedance sources without amplifiers.

The *ADS8168EVM-PDK* is designed with the common buffer amplifier topology shown in Figure 4. Figure 6 shows the FET plot for a 2-kHz sine way input signal.



f_{IN} = 2 kHz, SNR = 92 dB, THD = –109 dB

Figure 6. FFT Plot: AC Performance on ADS8168EVM-PDK

Conclusion

The ADS8168 enables design of a small-size and cost-optimized multichannel data acquisition system because:

- MUX breakout allows single ADC driver
- Extended settling time for high-impedance sources
- Integration of reference and refby2 buffer enables smaller system size

Table 1. ADS8168 Device Family

Device	Sampling Rate	Description
ADS8168	1000 kSPS	16-bit, 8-channel, high-precision, SAR ADC with integrated reference and refby2 buffer
ADS8167	500 kSPS	
ADS8166	250 kSPS	

Table 2. Related Documentation

Type	Title
Application Note	*Optimizing Data Transfer on High-Resolution, High-Throughput Data Converters* (SBAA249)
Application Note	*Optimizing Data Transfer on High-Resolution, High-Throughput Data Converters* (SBAA249)
Application Note	*Improving Input Settling for Precision Data Converters* (SBAA250)
Product List	List of ADCs with Enhanced-SPI Interface

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