

# Using ADS8410/13 in Daisy-Chain Mode

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## ABSTRACT

Many applications require multiple analog-to-digital converters (ADC) in a system. Daisy chaining multiple ADCs enables the use of a single data receiver or a small FPGA. It offers easy and minimal digital routing. This application report describes how multiple ADCs (ADS8410/13) work in a daisy-chain mode. The device offers a high-speed (200 Mbps) LVDS serial interface. This application report also suggests a way to de-serialize high-speed serial data. It discusses the board design aspects and test guidelines. It also presents reference schematics and layouts for the boards. Finally, the reference board results are presented.

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## 1 Introduction

In many applications, multiple ADCs are used to convert several analog channels. For stand-alone ADCs (i.e., ADCs without an option for daisy chain or cascade) multiple digital outputs are sometimes multiplexed with a digital multiplexer. In other cases, a high pin-count FPGA or DSP is used to receive multiple digital outputs. To avoid this complexity, the ADS8410/13 offers a daisy-chain mode (explained in detail later) in which data from multiple devices are transmitted through the chain and is received from only the last device. Layout is simpler because of point-to-point connection. The serial LVDS (low voltage differential signaling) interface offers high-speed (200 Mbps) data transmission to enable the use of more devices for a given throughput. The low differential swing in LVDS mode causes lower ground bounce in the system and less crosstalk among the digital signals. This helps to achieve a better signal-to-noise ratio in a system.

## 2 Description of the Device

The ADS8410 and ADS8413 are 16-bit 2-MSPS A/D converters with 4-V internal reference. The devices include a capacitor-based SAR A/D converter with inherent sample and hold.

These devices offer a 200-Mbps serial LVDS interface. The interface is designed to support cascading and daisy chaining of multiple devices. There is a mode to select 16/8-bit data frame to interface with shift registers for converting the data to parallel format.

ADS8410 has pseudo-differential input stage. The  $-IN$  swing of  $\pm 200$  mV is useful for compensating the ground voltage mismatch between the ADC and the sensor and also for canceling the common-mode noise.

The ADS8413 has unipolar differential input range, which supports differential input swing of  $-V_{REF}$  to  $+V_{REF}$  with a common mode of  $+V_{REF}/2$ .

The devices operate at a lower power when used at lower conversion rates, because of the nap feature. Nap mode shuts down the device partially when the device is not converting.

These devices are available in a 48-pin QFN package.

## 3 Digital Interface

The ADS8410/13 offers 200 Mbps LVDS interface. LVDS is current output which terminates at the receiver with a 100- $\Omega$  resistor which converts it to voltage. The high speed offers more device integration in a system at a given ADC sampling rate. LVDS has a typical differential swing of  $\pm 680$  mV ( $+680$  mV for logic 1 and  $-680$  mV for logic 0) which is better in a low-noise system. The differential nature of this signaling filters any common-mode noise.

#### 4 Definition of Daisy Chain

In daisy-chain mode, multiple devices are connected such that each device receives the previous devices' data and transfers it along with its own data. Consider a situation where N devices are in the chain. The second device receives the first device's data and passes this data along with its own data to the third device. The third device sends its own data along with first and second devices' data. The Nth device sends its own data with all N - 1 devices' data. Finally, one receiver is connected to the Nth device, which collects all the data from the Nth device. Figure 1 shows how three (N = 3) devices work in a daisy chain.

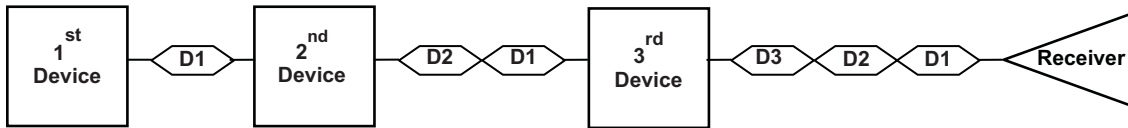
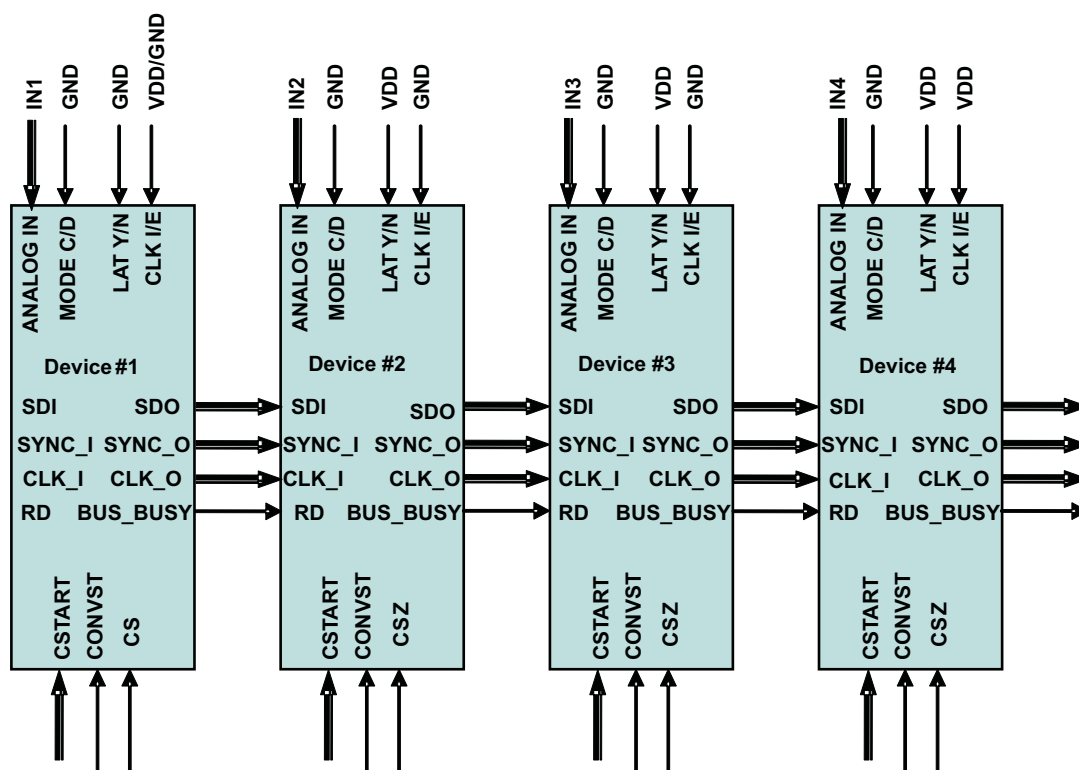


Figure 1. Three Devices in Daisy Chain

#### 5 Block Diagram

Figure 2 shows how four devices are connected in a daisy chain using the ADS8410/13. MODE C/ $\overline{D}$  (cascade or daisy-chain mode) has to be logic zero to operate in daisy-chain mode. The first device in the chain is identified by  $LAT\ Y/\overline{N} = 0$ . For all other devices,  $LAT\ Y/\overline{N} = 1$ .  $LAT\ Y/\overline{N}$  signifies that the first device sends out data without latency and the other devices send out data with latency. Either  $\overline{CSTART}$  (LVDS) or  $\overline{CONVST}$  (CMOS) is used as a conversion start signal. Depending on the  $CLK\ I/\overline{E}$  signal, the first device either takes in an external clock or generates an internal clock. This clock is used as the master clock for all the devices in the daisy chain, and the interface is synchronized with this clock. Other devices can only accept  $CLK\_O$  from the previous device as an external clock.  $SDI$  (Serial Data Input) and  $SYNC\_I$  (Frame Sync Input) of the first device should be logic 0 (+ve terminal to GND and -ve terminal to +VBD).  $BUS\_BUSY = 1$  signifies that the device is busy sending out data in the bus.  $\overline{RD}$  is Data Read Request to the Device and also acts as a handshake signal for daisy-chain and cascade operation.  $\overline{RD} = 1$  brings about a 3-state device output.  $BUS\_BUSY$  of the last device can be connected to  $\overline{RD}$  of the first device. Otherwise,  $BUS\_BUSY$  of the last device should be kept floating.  $\overline{RD}$  of the first device should be connected to GND in this case.



Separate  $\overline{CS}$ ,  $\overline{CONVST}$ ,  $\overline{CSTART}$  for each IC

Figure 2. Four Devices in Daisy-Chain Mode

## 6 Timing

### 6.1 Timing Requirements

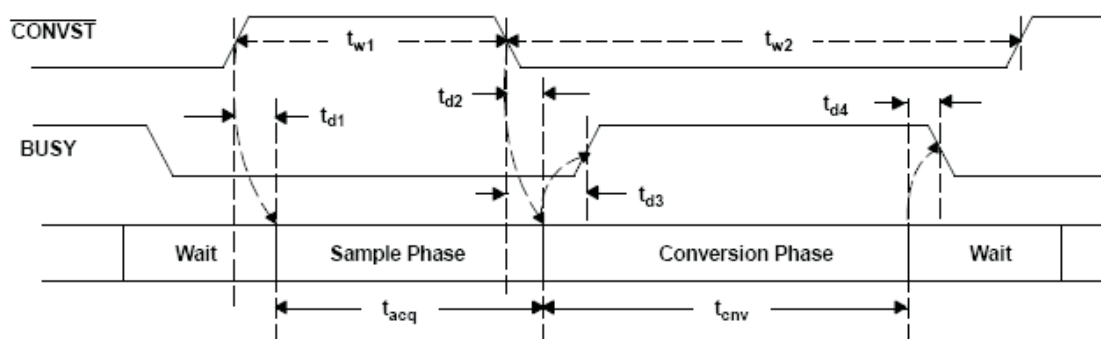
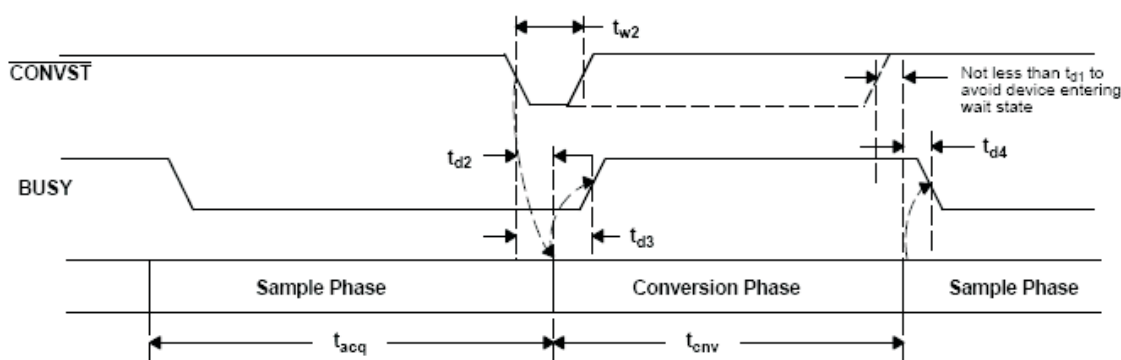
in the following timing table, all specifications are typical at  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $+V_A = +5\text{ V}$ ,  $+V_{BD} = +5\text{ V}$  and  $3.3\text{ V}$  (unless otherwise noted).

PARAMETER		MIN	TYP	MAX	UNIT	REF
<b>SAMPLING AND CONVERSION RELATED</b>						
$t_{acq}$	Acquisition time	100			ns	Figure 3, Figure 4
$t_{conv}$	Conversion time			391	ns	Figure 3, Figure 4
$t_{w1}$	Pulse duration, $\overline{CONVST}$ high	100			ns	Figure 3
$t_{w2}$	Pulse duration, $\overline{CONVST}$ low	40			ns	Figure 3, Figure 4
$t_{d1}$	Delay time, $\overline{CONVST}$ rising edge to sample start			5	ns	Figure 3
$t_{d2}$	Delay time, $\overline{CONVST}$ falling edge to conversion start			5	ns	Figure 3, Figure 4
$t_{d3}$	Delay time, $\overline{CONVST}$ falling edge to busy high	+VBD = 5 V		13	ns	Figure 3, Figure 4
		+VBD = 3.3 V		14		
$t_{d4}$	Delay time, conversion end to busy low	+VBD = 5 V		7	ns	Figure 3, Figure 4
		+VBD = 3.3 V		8		
$t_{w3}$	Pulse duration, $\overline{CSTART}$ high	100			ns	Figure 3, Table 1

PARAMETER		MIN	TYP	MAX	UNIT	REF
$t_{w4}$	Pulse duration, $\overline{CSTART}$ low	45			ns	Figure 3, Figure 4, Table 1
$t_{d5}$	Delay time, $\overline{CSTART}$ rising edge to sample start			7.5	ns	Figure 3, Figure 4 Table 1
$t_{d6}$	Delay time, $\overline{CSTART}$ falling edge to conversion start			7.5	ns	Figure 3, Figure 4 Table 1
$t_{d7}$	Delay time, $\overline{CSTART}$ falling edge to busy high	+VBD = 5 V		15.5	ns	Figure 3, Figure 4 Table 1
		+VBD = 3.3 V		16.5		
<b>I/O RELATED</b>						
$t_{d8}$	Delay time, $\overline{RD}$ falling edge while $\overline{CS}$ low to BUS_BUSY high			16	ns	Figure 6
$t_{d9}$	Delay time, $\overline{RD}$ falling edge while $\overline{CS}$ low to SYNC_O and SDO out of 3-state condition (for device with LAT_Y/N pulled low)	+VBD = 5 V		28	ns	Figure 6
		+VBD = 3.3 V		29		
$t_{d10}$	Delay time, pre_conversion end (point A) to SYNC_O and SDO out of 3-state condition			22	ns	Figure 7
$t_{d11}$	Delay time, pre_conversion end (point A) to BUS_BUSY high	+VBD = 5 V		7	ns	Figure 7
		+VBD = 3.3 V		8		
$t_{d12}$	Delay time, conversion phase end to SYNC_O high	6		$9 + t_{CLK}$	ns	Figure 7
$t_{d13}$	Delay time, $\overline{RD}$ falling edge while $\overline{CS}$ low to SYNC_O high	+VBD = 5 V	$5 + 4 \cdot t_{CLK}$	$8 + 5 \cdot t_{CLK}$	ns	Figure 6
		+VBD = 3.3 V	$5.5 + 4 \cdot t_{CLK}$	$8.5 + 5 \cdot t_{CLK}$		
$t_{w5}$	Pulse duration, $\overline{RD}$ low for device in no latency mode	5			ns	Figure 9
$t_{d14}$	Delay time, CLK_O rising edge to data valid	+VBD = 5 V		1.3	ns	Figure 6, Figure 7
		+VBD = 3.3 V		1.4		
$t_{d15}$	Delay time, BUS_BUSY low to SYNC_O high in daisy-chain mode indicating receiving device to output data	+VBD = 5 V	$4 \cdot t_{CLK} - 6$	$4 \cdot t_{CLK} - 2.5$	ns	Figure 8, Figure 10
		+VBD = 3.3 V	$4 \cdot t_{CLK} - 6.5$	$4 \cdot t_{CLK} - 3$		
$t_{d16}$	Delay time, CLK_O to SDO and SYNC_O 3-state			4	ns	Figure 8, Figure 10
$t_{pd1}$	Propagation delay time, SYNC_I to SYNC_O in daisy-chain mode			$11 + 0.5 \cdot t_{CLK}$	ns	Figure 10
$t_{d18}$	Delay time, $\overline{RD}$ rising edge to BUS_BUSY high for device with LAT_Y/N = 1	+VBD = 5 V		7	ns	Figure 9
		+VBD = 3.3 V		8		
$t_{d19}$	Delay time, point A indicating clear for bus 3-state release to BUSY falling edge	+VBD = 5 V		40	ns	Figure 7
		+VBD = 3.3 V		40.5		
$t_{clk}$	CLK frequency (serial data rate)	190	200	210	MHz	

## 6.2 Sample and Convert

The sampling and conversion process is controlled by the  $\overline{CSTART}$  (LVDS) or  $\overline{CONVST}$  (CMOS) signal. Both signals are functionally identical. The following diagrams show control with  $\overline{CONVST}$ . The rising edge of  $\overline{CONVST}$  (or  $\overline{CSTART}$ ) starts the sample phase, if the conversion has completed and the device is in the wait state. Figure 4 shows the case when the device is in the conversion phase at the rising edge of  $\overline{CONVST}$ . In this case, the sample phase starts immediately at the end of the conversion phase, and there is no wait state.


**Figure 3. Sample and Convert With Wait (Less Than 2-MSPS Throughput)**

**Figure 4. Sample and Convert With No Wait or Back to Back (2-MSPS Throughput)**

The device ends the sample phase and enters the conversion phase on the falling edge of  $\overline{\text{CONVST}}$  ( $\overline{\text{CSTART}}$ ). A high level on the  $\overline{\text{BUSY}}$  output indicates an ongoing conversion. The device conversion time is fixed. The falling edge of  $\overline{\text{CONVST}}$  ( $\overline{\text{CSTART}}$ ) during the conversion phase aborts the ongoing conversion. A data read after a conversion abort fetches invalid data. Valid data is only available after a sample phase and a conversion phase has completed. The timing diagram for control with  $\overline{\text{CSTART}}$  is similar to [Figure 3](#) and [Figure 4](#). [Table 1](#) shows the equivalent timing for control with  $\overline{\text{CONVST}}$  and  $\overline{\text{CSTART}}$ .

**Table 1.  $\overline{\text{CONVST}}$  and  $\overline{\text{CSTART}}$  Timing Control**

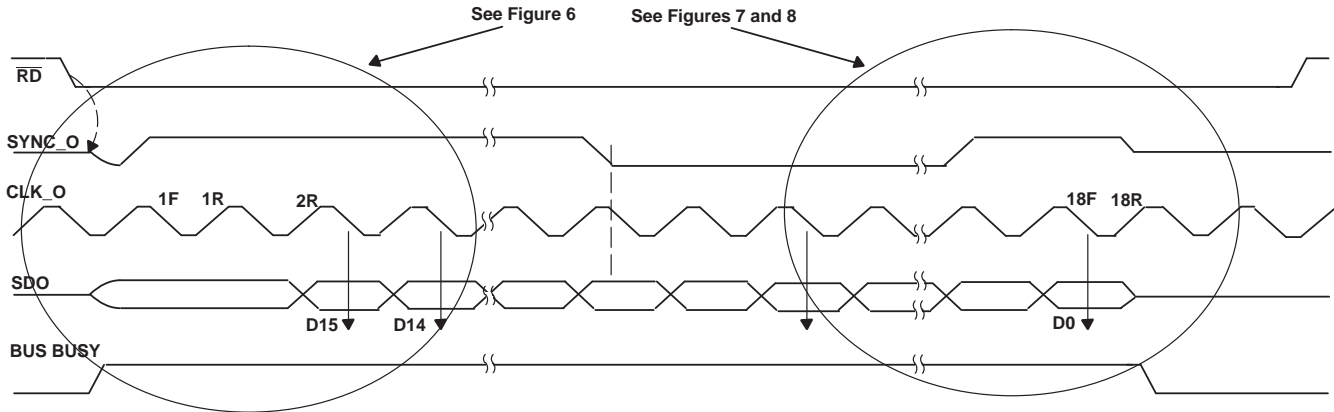
TIMING FOR CONTROL WITH $\overline{\text{CONVST}}$	TIMING FOR CONTROL WITH $\overline{\text{CSTART}}$
tw1	tw3
tw2	tw4
t1	t5
t2	t6
t3	t7

### 6.3 Data Read Operation

The ADS8413 supports a 200-MHz serial LVDS interface for data read operation. The three signal LVDS interface (SDO, CLK\_O, and SYNC\_O) is well suited for high-speed data transfers. An application with a single device or multiple devices can be implemented with a daisy-chain or cascade configuration. The following sections discuss data read timing when a single device is used.

### 6.3.1 Data Read for a Single Device (See Table 1 for Device Configuration)

For a single device, the two possible read cycle starts are: a data read cycle start during a wait or sample phase or a data read cycle start at the end of a conversion phase. Read cycle end conditions can change depending on MODE C/D selection. Figure 5 explains the data read cycle. The details of a read frame start with the two previous listed conditions and a read cycle end with MODE C/D selection are explained in Figure 6, Figure 7, and Figure 8, respectively.



**Figure 5. Data Read With  $\overline{CS}$  Low and BYTE = 0**

As shown in Figure 5, a new data read cycle is initiated with the falling edge of  $\overline{RD}$ , if  $\overline{CS}$  is low and the device is in a wait or sample phase. The device releases the LVDS o/p (SYNC\_O, SDO) from 3-state and sets BUS\_BUSY high at the start of the read cycle. The SYNC\_O cycle is 16 clocks wide (rising edge to rising edge) if the BYTE input is held low and can be used to synchronize a data frame. The clock count begins with the first CLK\_O falling edge after a SYNC\_O rising edge. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of the clock. The next rising edge of SYNC\_O coincides with the 16th rising edge of the clock. D0 is latched out on the 17th rising edge of the clock. The receiver can latch the de-serialized 16-bit word on the 18th rising edge (18R, or the second rising edge after a SYNC\_O rising edge).

$\overline{CS}$  high during a data read results in a 3-state SYNC\_O and SDO condition. These signals remain in the 3-state condition until the start of the next data read cycle.

### 6.3.2 Data Read Cycle Start During Wait or Sample Phase

As shown in Figure 6, the falling edge of  $\overline{RD}$ , with  $\overline{CS}$  low and when the device is in a wait or sample phase, triggers the start of a read cycle. The cycle starts when BUS\_BUSY goes high and SYNC\_O, SDO are released from the 3-state condition. SYNC\_O is low at the start and rises to a high level  $t_{d13}$  ns after the falling edge of  $\overline{RD}$ . As shown in Figure 6, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 5).

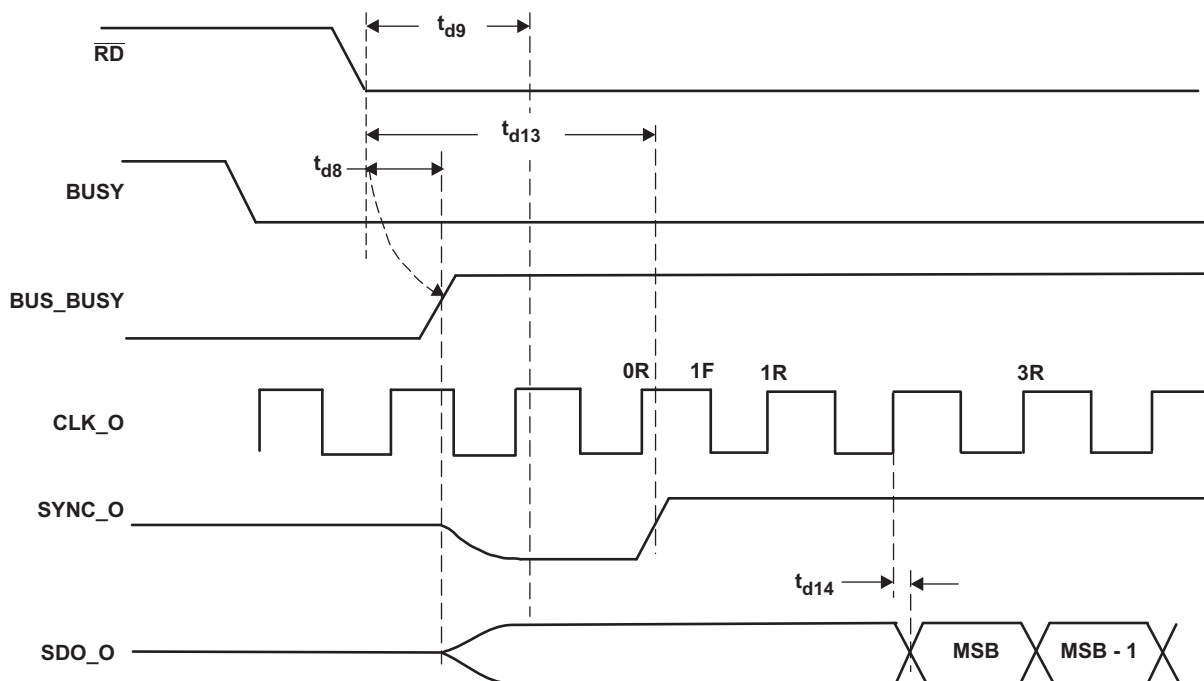


Figure 6. Start of Data Read Cycle With  $\overline{RD}$  and  $\overline{CS}$  Low and Device in Wait or Sample Phase

### 6.3.3 Data Read Cycle Start at End of Conversion Phase (Read Without Latency, Back-to-Back)

This mode is optimized for a data read immediately after the end of a conversion phase and ensures that the data read is complete before the sample end while running at 2 MSPS. Point A in Figure 7 indicates *pre\_conversion\_end*; it occurs  $t_{d19}$  ns before the falling edge of  $BUSY$  or  $[(t_{d2} + t_{cnv} + t_{d4}) - t_{d19}]$  ns after the falling edge of  $CONVST$ . A read cycle is initiated at point A if  $\overline{RD}$  is issued before point A while  $\overline{CS}$  is low. Alternately,  $\overline{RD}$  and  $\overline{CS}$  can be held low. At the start of the read cycle,  $BUS\_BUSY$  rises to a high level and the LVDS outputs are released from the 3-state condition. The rising edge of  $SYNC\_O$ , occurs  $t_{d12}$  ns after the conversion end. As shown in Figure 7, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 5).



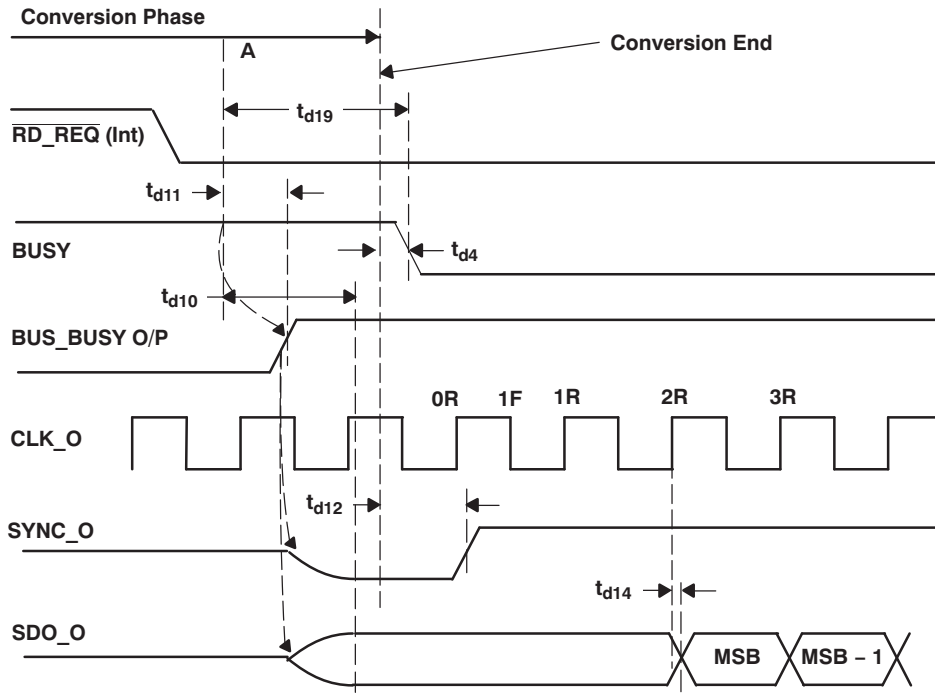


Figure 7. Start of Data Read Cycle With End of Conversion

### 6.3.4 Data Read Cycle End (With MODE C/D = 0)

A data read cycle ends after all 16 bits have been serially latched out. Figure 8 shows the timing of the falling edge of BUS\_BUSY and the rising edge of SYNC\_O with respect to SDO. SYNC\_O rises on the 16th rising edge of CLK\_O. As shown in Figure 6 and Figure 7, the MSB is shifted out on the 2nd rising edge of CLK\_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK\_O.

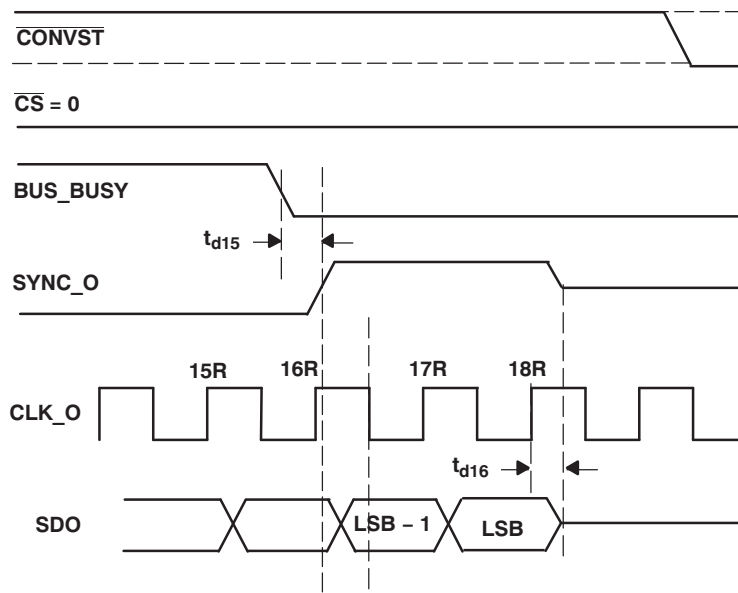


Figure 8. Data Read Cycle End With MODE C/D = 0

The next two rising edges of CLK\_O are shown as 17R and 18R in Figure 8. On 17R, the LSB is latched out, and on 18R, SDO and SYNC-O go to a 3-state condition. Note that BUS\_BUSY falls  $t_{d15}$  ns before the rising edge of SYNC\_O when MODE C/D = 0. Care must be taken not to allow LVDS bus usage by any other device until the end of the read cycle or  $(t_{d15} + 2/f_{CLK} + t_{d16})$  ns after the falling edge of BUS\_BUSY.

#### 6.4 Timing Diagrams for Daisy-Chain Operation

The conversion speed for  $n$  devices in the chain must be selected such that:

- $1/\text{conversion speed} > \text{read startup delay} + n \times (\text{data frame duration}) + t_{d16}$
- Read startup delay =  $10 \text{ ns} + (t_{d19} - t_{d4}) + t_{d12} + 2/f_{CLK}$
- Data frame duration =  $16/f_{CLK}$

Note that it is unnecessary for all devices in the chain to sample the data simultaneously. But, all of the devices must operate with the same exact conversion speed.

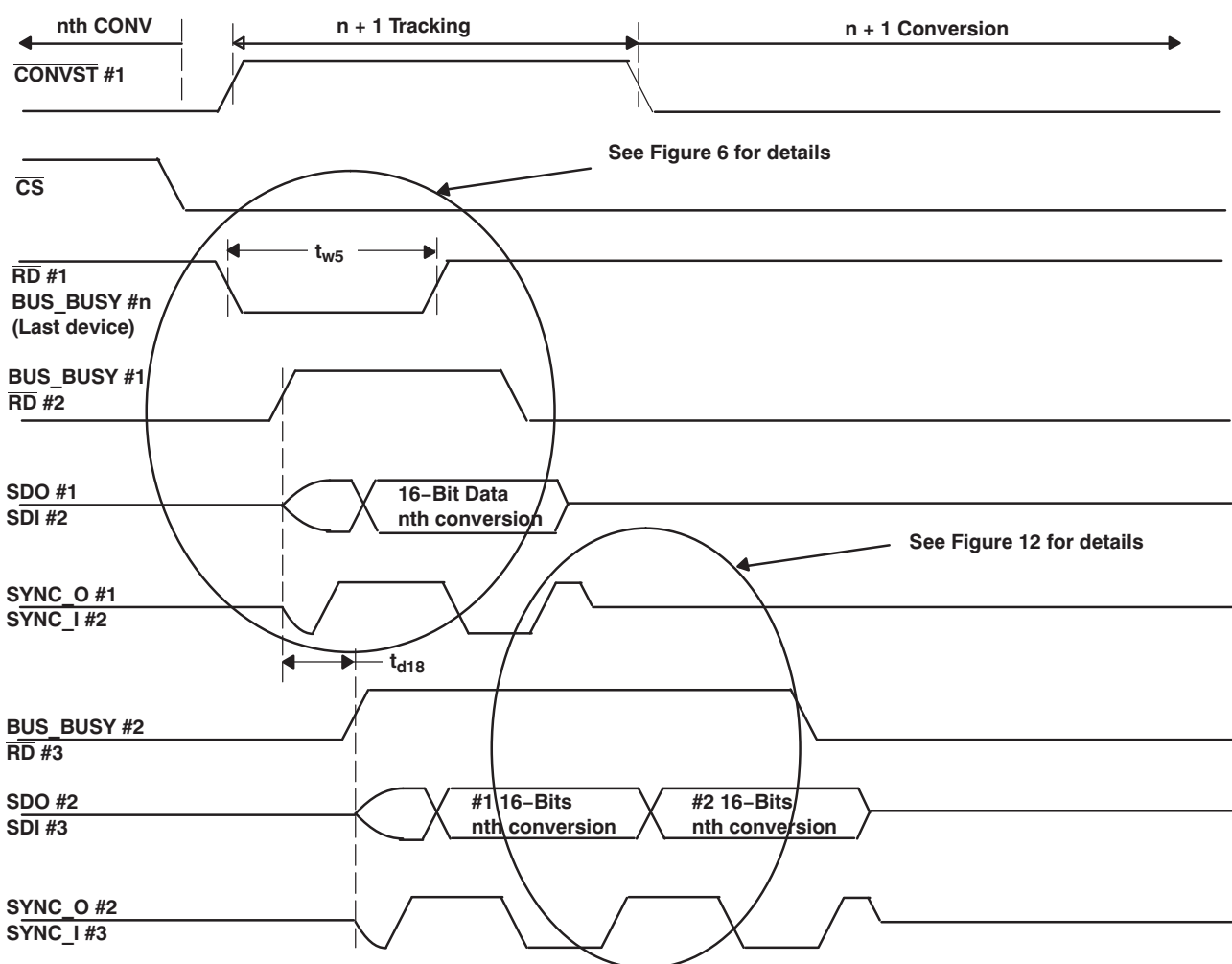
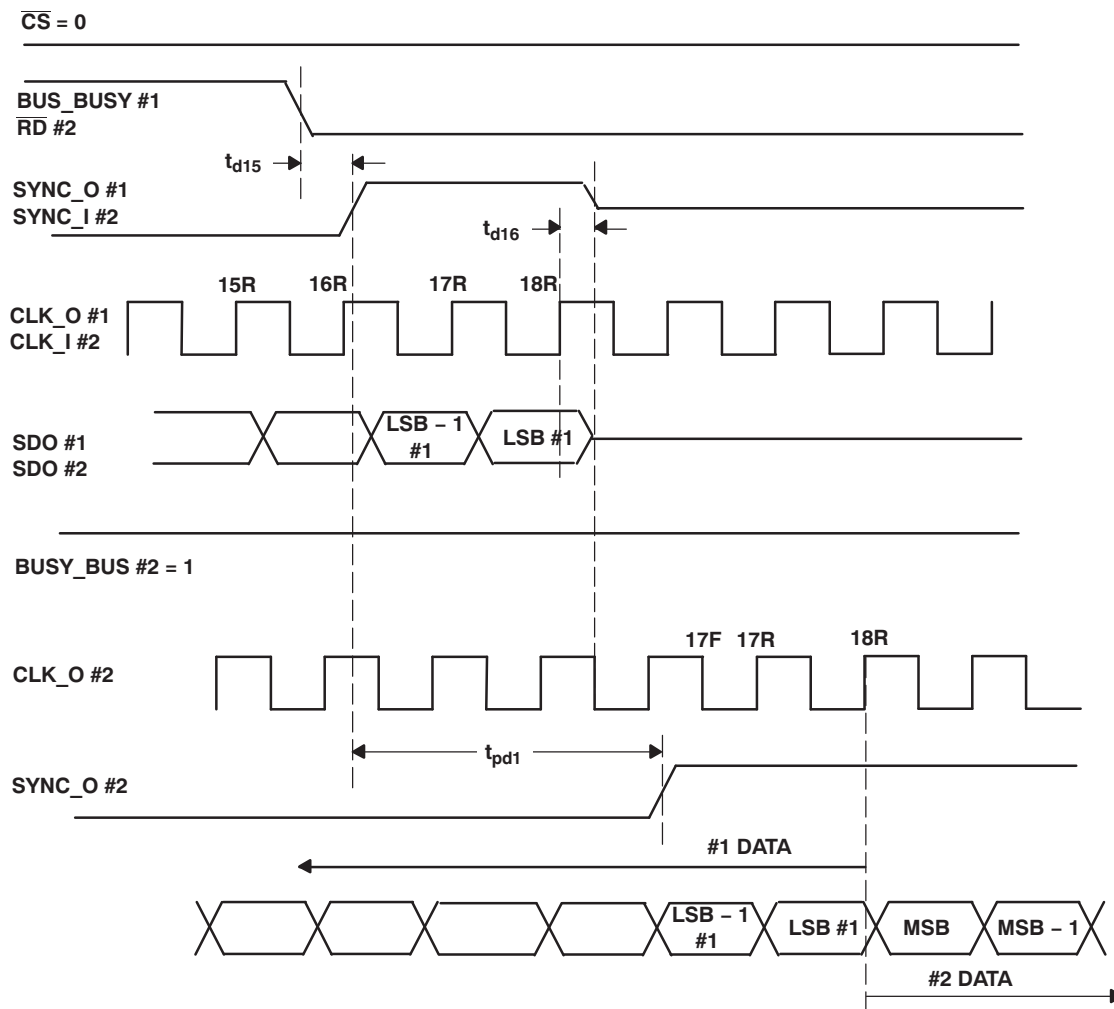


Figure 9. Data Read Operation for Devices in Daisy-Chain Mode

#### 6.5 Data Read Operation

On power up, BUS\_BUSY of all of the devices is low. The devices receive  $\overline{\text{CONVST}}$  or  $\overline{\text{CSTART}}$  to sample and start the conversion. The first device in the chain starts the data read cycle at the end of its conversion. BUS\_BUSY of device 1 (connected to RD of device 2) goes high on the read cycle start. Device 2 BUS\_BUSY goes high on the rising edge of RD #1. This propagates until the last device in the

chain. Device 2 receives CLK\_I, SDI, and SYNC\_I from device 1, and it passes all of these signals to the next device. Device 2 (and every subsequent device in the chain) passes the received signals to its output until it sees the falling edge of  $\overline{RD}$  #1 (same as BUS\_BUSY of the previous device). In daisy-chain mode, BUS\_BUSY for any device falls when it has passed all of the previous device data followed by its own data. The falling edge of BUS\_BUSY occurs before the rising edge of SYNC\_O. This indicates to the receiving device that the previous data chain is over, and it is now the receiving device's turn to output the data. The device outputs the data from the last completed conversion. BUS\_BUSY of the last device in the chain is fed back to  $\overline{RD}$  of the first device (or device 1  $\overline{RD}$  tied to 0). This makes sure that  $\overline{RD}$  of device 1 is low before its conversion is over. The chain continues with only one external signal ( $\overline{CONVST}$  or  $\overline{CSTART}$ ) when  $\overline{CS}$  is held low. Every device LVDS output goes to a 3-state condition once all data transfer through the device has been completed.  $\overline{CS}$  going high during the data read cycle of any device places its SYNC\_O and SDO in a 3-state condition. This halts the propagation of data through the chain. To reset this condition, it is necessary to assert  $\overline{CS}$  high for all devices. The new read sequence starts only after  $\overline{CS}$  for all devices is low before point A as shown in Figure 7. The high pulse on  $\overline{CS}$  must be at least 20 ns wide. It is better to connect  $\overline{CS}$  of all of the devices together to avoid undesired halting of the daisy chain.



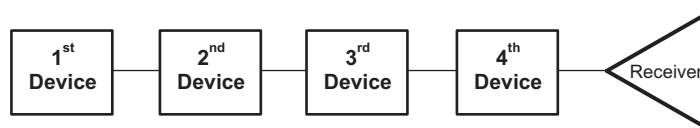
**Figure 10. Data Propagation From Device n to Device n+1 in Daisy-Chain Mode**

As shown in Figure 10, a propagation delay of  $t_{pd1}$  occurs from SYNC\_I to SYNC\_O or SDI to SDO. Note that the data frames of all devices in the chain appear seamless at the last device output. The rising edge of SYNC\_O occurs at an interval of 16 clocks (or 8 clocks in BYTE mode); this can be used as data frame sync. The deserializer at the output of the last device can shift the data on every falling edge of the clock and it can latch the parallel 16-bit word on the second rising edge of CLK\_O (shown as 18R) after every rising edge of SYNC\_O.

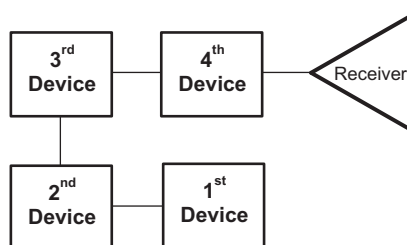
## 7 Board Design Aspects

### 7.1 Placement

Consider an application where four devices are operated in daisy-chain mode. There are two ways to do this layout. The chain can be in a straight line fashion (as in [Figure 11](#)) or in a circular fashion (as in [Figure 12](#)).



**Figure 11. Four Devices Placed in Straight Line Fashion**



**Figure 12. Four Devices Placed in Circular Fashion**

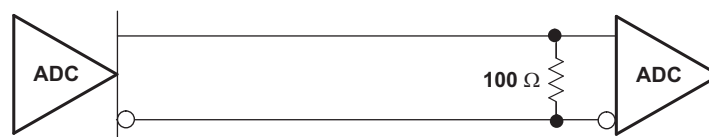
Any one of the layouts can be chosen depending on the area and shape of the printed-circuit board.

### 7.2 Signal Integrity

The device offers high speed LVDS CLK\_O (Clock Output), SDO (Serial Data Output) and SYNC\_O (Frame Sync Output) signals which have a typical rise time of only 700 ps. According to LVDS standards, the receiver termination needs to be 100  $\Omega$  (shunt resistance between +ve and -ve terminal of each LVDS signals) to have proper voltage swing. To avoid reflection, the differential characteristic impedance needs to match with the 100- $\Omega$  termination. So, CLK\_O, SDO, and SYNC\_O differential traces need to have 100- $\Omega$  differential characteristic impedance.

### 7.3 Termination Strategy

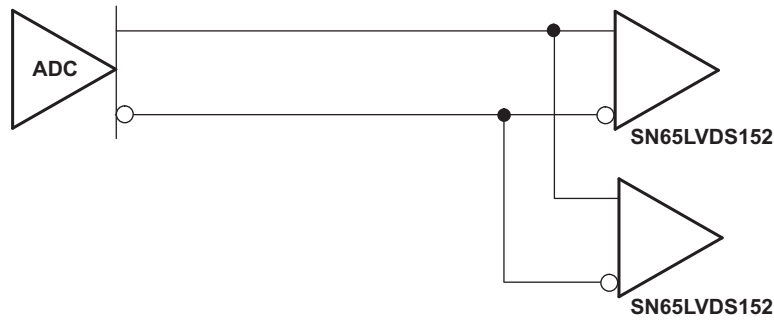
For point-to-point connection, LVDS signals are terminated with a 100- $\Omega$  resistor at the receiver end as shown in [Figure 13](#).



**Figure 13. LVDS Driver/ Receiver in Point-to-Point Connection**

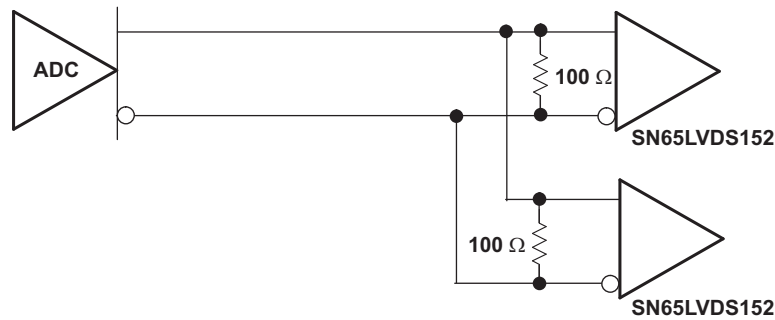
The differential characteristic impedance of the line should be maintained close to 100  $\Omega$ . This strategy is followed for signals which connect one ADC to another ADC. As an example, this is followed for the traces between CLK\_O of the first device and CLK\_I (Clock Input) of the second device.

This method is not valid for the signals which connect the last device in the chain to two deserializers which are in cascade (as shown in [Figure 14](#)).



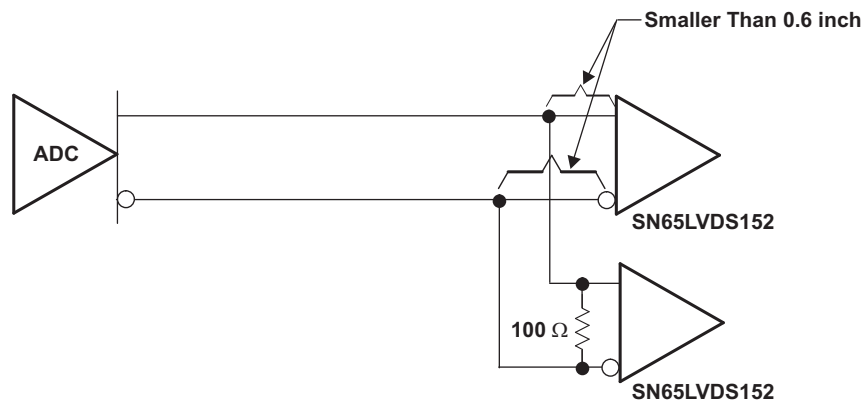
**Figure 14. CLK\_O and SYNC\_O Connection Between Last Device and the Deserializers**

One way to terminate this structure is to have two 100- $\Omega$  resistor termination at both receiver ends (see [Figure 15](#)). But because LVDS is a current source, two parallel resistors drive the voltage swing to half. If your receiver has lower threshold than one half of LVDS differential swing and you have enough noise margin for your system, you can use this termination strategy.



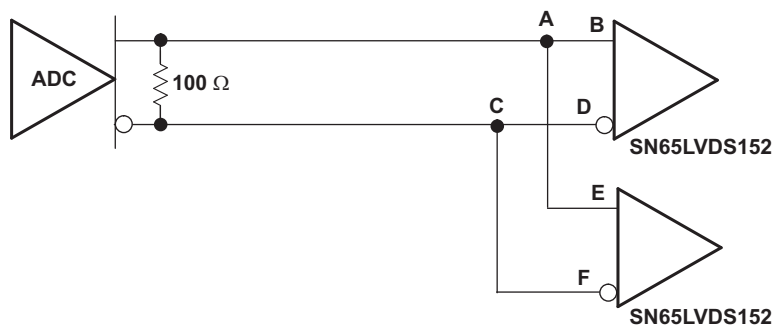
**Figure 15. Terminating at Both Receivers**

Another way to terminate is to put the termination at any one of the receiver ends. In this case, the signal is reflected from the receiver which is not terminated. Make sure that the trace length of the unterminated end from the common point is smaller than 0.6 inch (see [Figure 16](#)). This is valid for an FR4 printed-circuit board.



**Figure 16. Terminating at One Receiver**

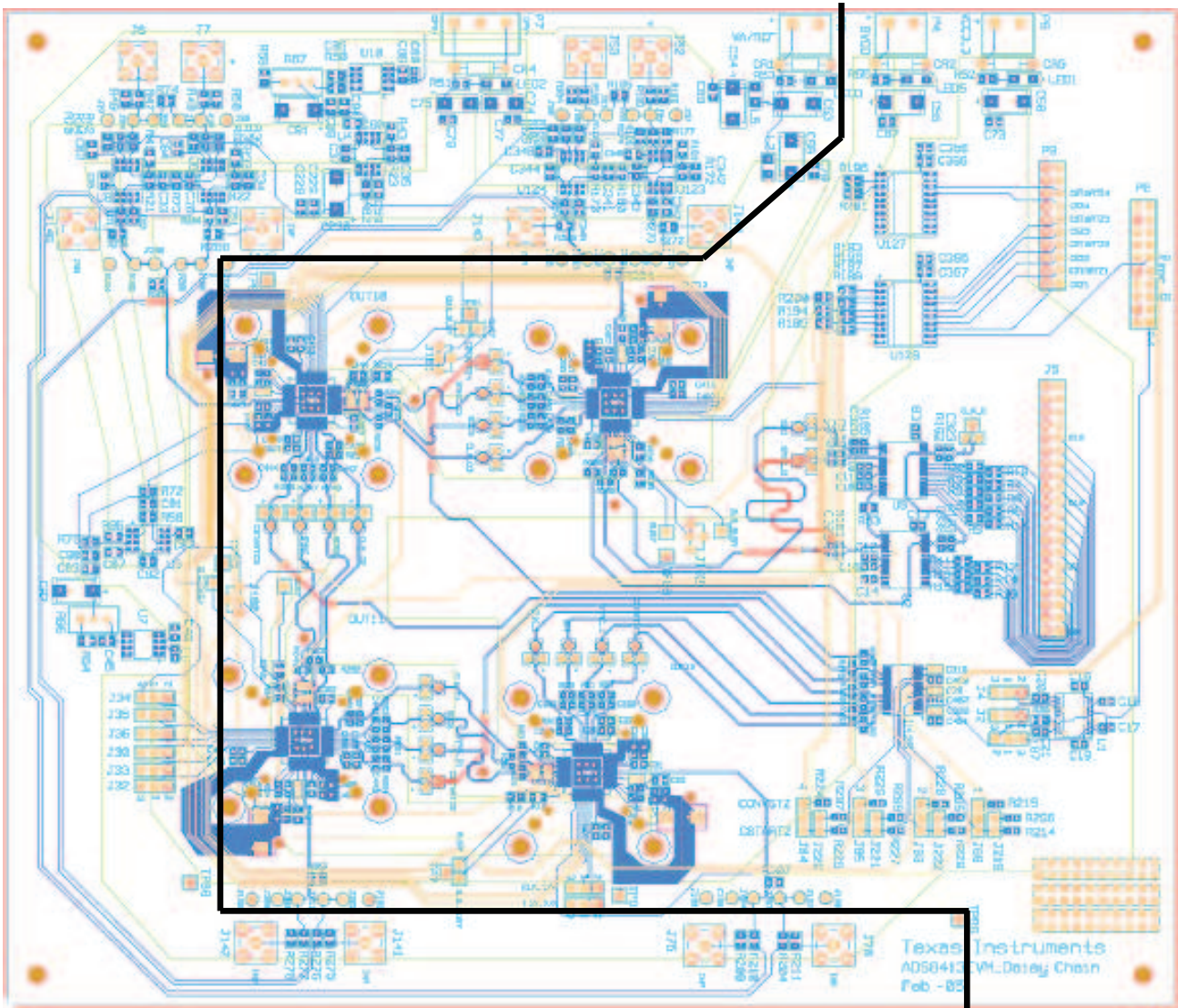
One more way to terminate in this case is to terminate at the driver end. The signal gets reflected from the receiver ends once and gets absorbed at the driver end fully. Ensure that the trace length of the unterminated trace from the common point (see [Figure 17](#), in this case point A to B, C to D, A to E, or C to F) is less than 0.6 inch.



**Figure 17. Terminating at Source End**

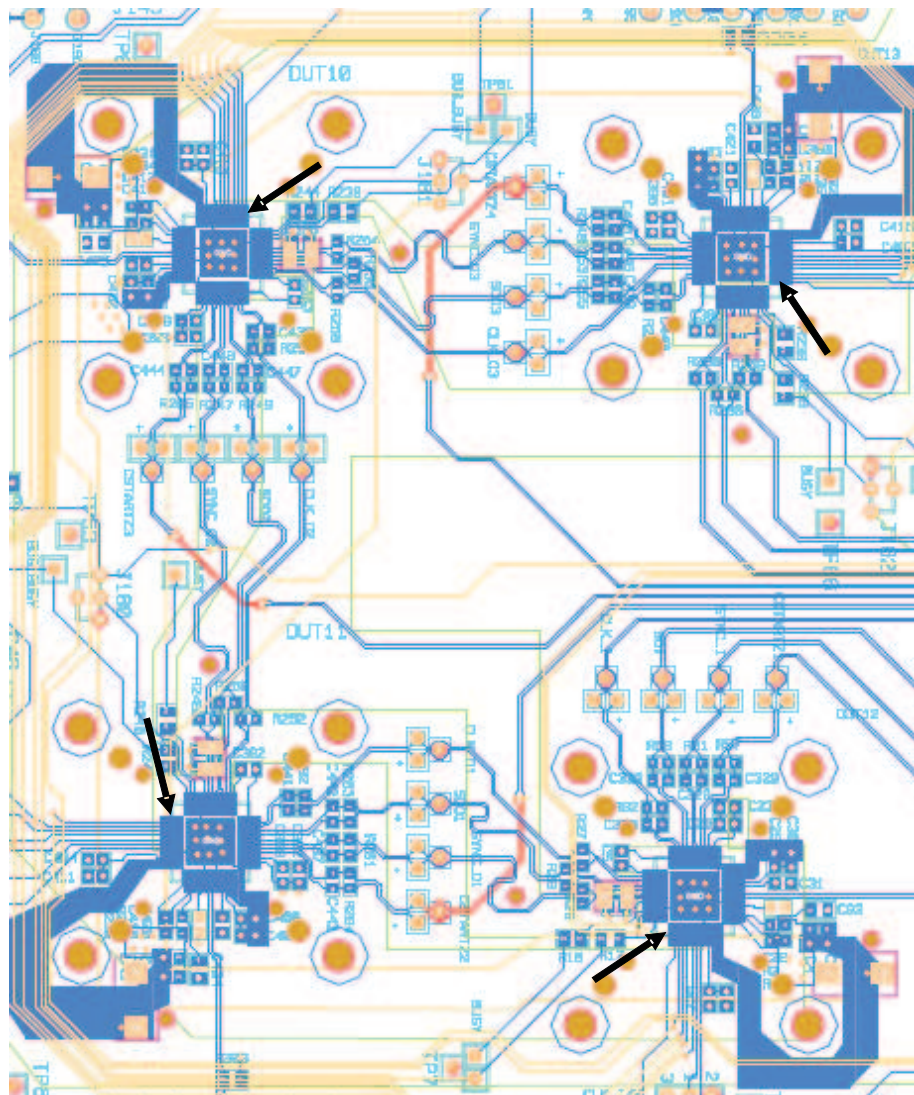
#### 7.4 Layout Guidelines

ADS8410/13 offers high-speed digital interface. Analog and digital layout should not be mixed up. Analog placement and routing should be separated from the digital placement and routing as far as possible. The black line in [Figure 18](#) is a virtual boundary for the analog and digital placement. Analog circuitry (operational amplifiers and reference input) is on the left side of the boundary. The digital circuitry (deserializer, clock multiplier, and digital buffers) is on the right side of the boundary.



**Figure 18. Analog and Digital Circuitry Are Separated in the Layout With a Virtual Boundary**

Each device (ADS8410/13) is rotated appropriately and placed such that LVDS outputs from the previous device and LVDS inputs of the device connects in the shortest path. In Figure 19, the arrows indicate pin number 1 for each device. Note that a device is rotated by 90 degrees with respect to the previous device to make the LVDS lines short.



**Figure 19. Devices Are Rotated and Placed to Reduce LVDS Trace Length**

ADS8410/13 offers high-speed (200 Mbps) LVDS interface. Therefore, it is important to meet setup and hold time requirements for LVDS signals. To achieve this, the length of CLK\_O to CLK\_I, SDO to SDI, and SYNC\_O to SYNC\_I (Figure 20) should be equal. This is valid for LVDS signals between two devices and also the LVDS signals between last device and the deserializers. Any length mismatch should be less than 100 mils (1 mil = 1/1000 inch). Sometimes, traces are made serpentine in nature to match the length. Figure 20 shows routing of LVDS signals between device 1 and 2. Also note that LVDS pairs are routed differentially to make the differential characteristic impedance constant.



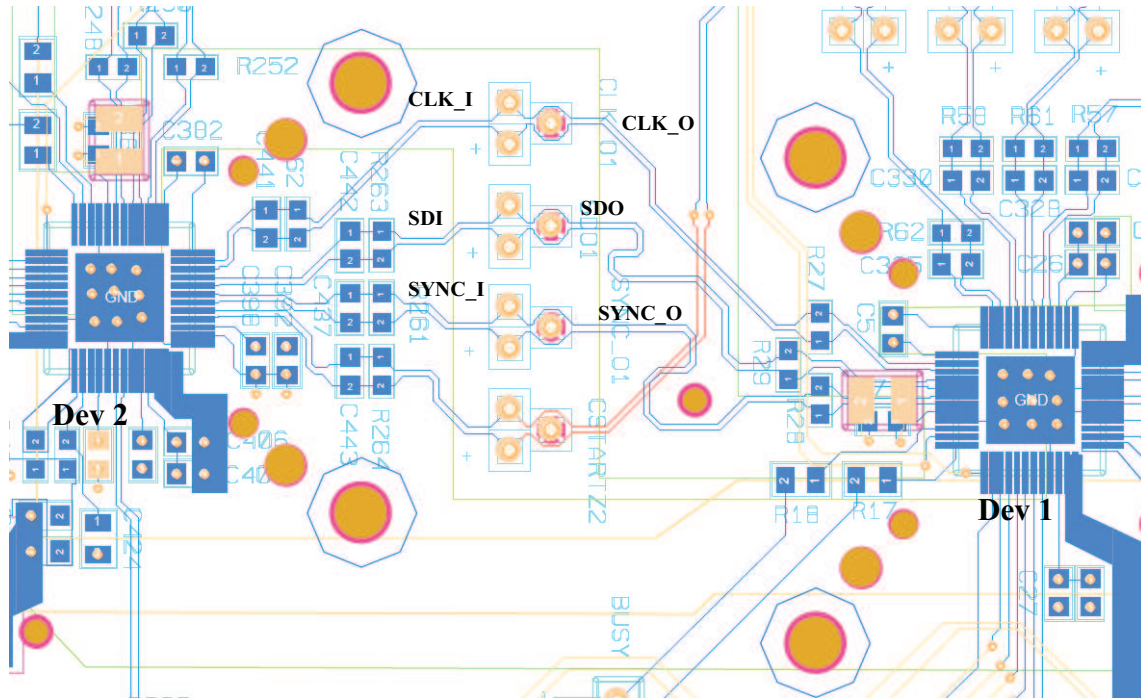


Figure 20. LVDS Routing

## 8 System Block Diagram

Figure 21 and Figure 22 show how four devices in a daisy chain are tested. Figure 21 shows how first and second devices are connected. A pattern generator is used to generate necessary control signals and clock. A 25-MHz clock is generated from the pattern generator and is multiplied by a clock multiplier (CDCF5801) to get a 200-MHz LVDS clock. CMOS to LVDS drivers (SN75LVDS389) are used to convert from CMOS/ TTL to LVDS.

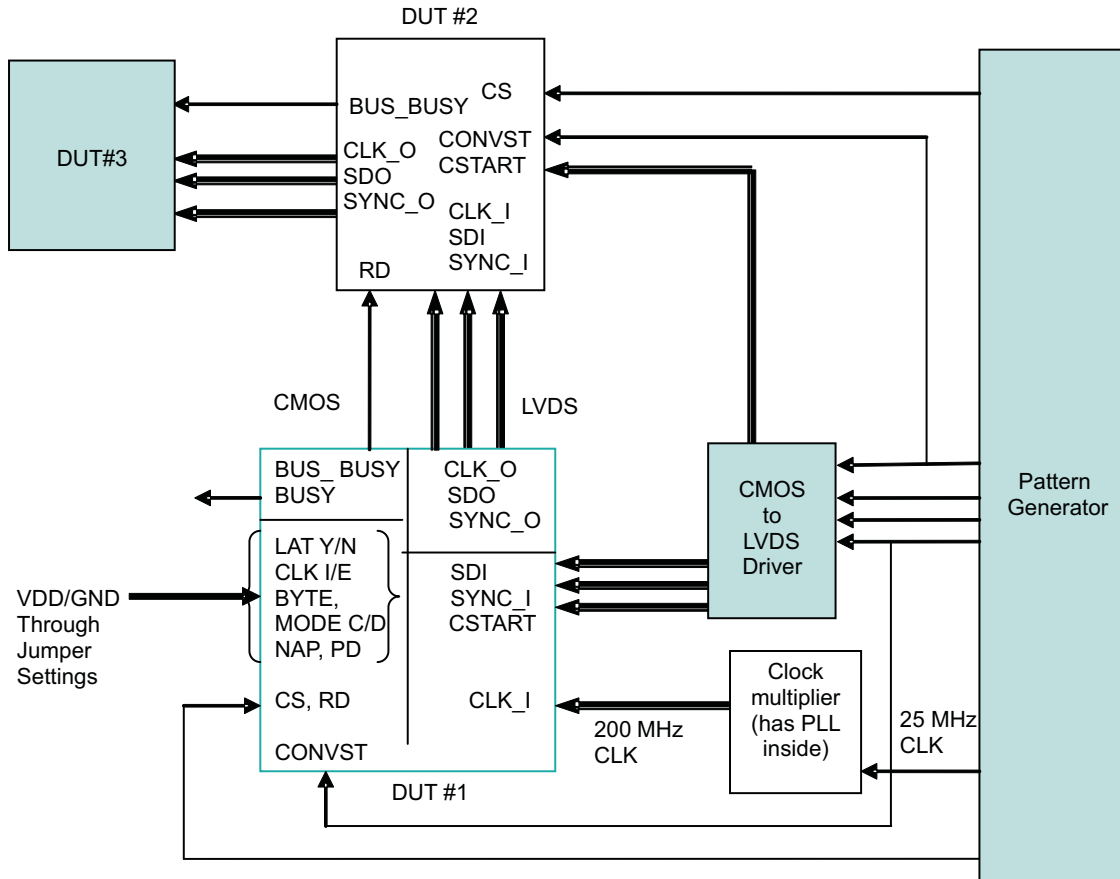


Figure 21. First and Second Device in the Chain

Figure 22 shows how third and fourth devices are connected. Serial data from the fourth device is converted to parallel by two cascaded SN65LVDS152

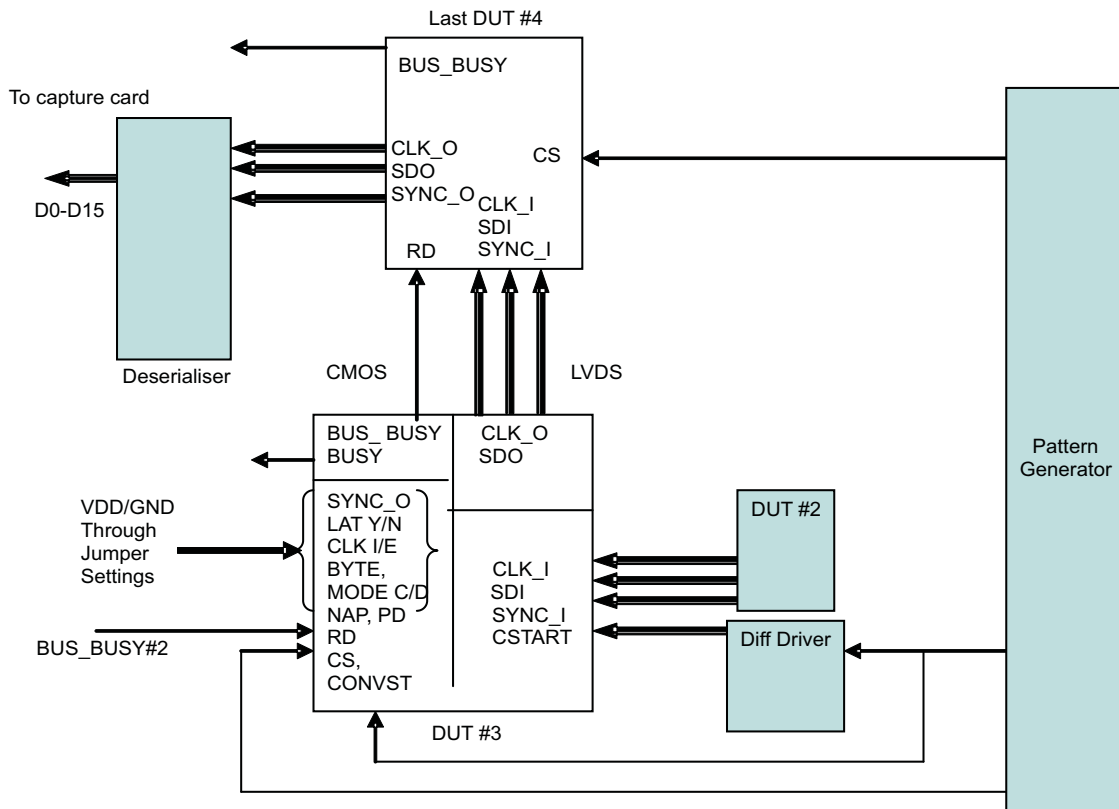
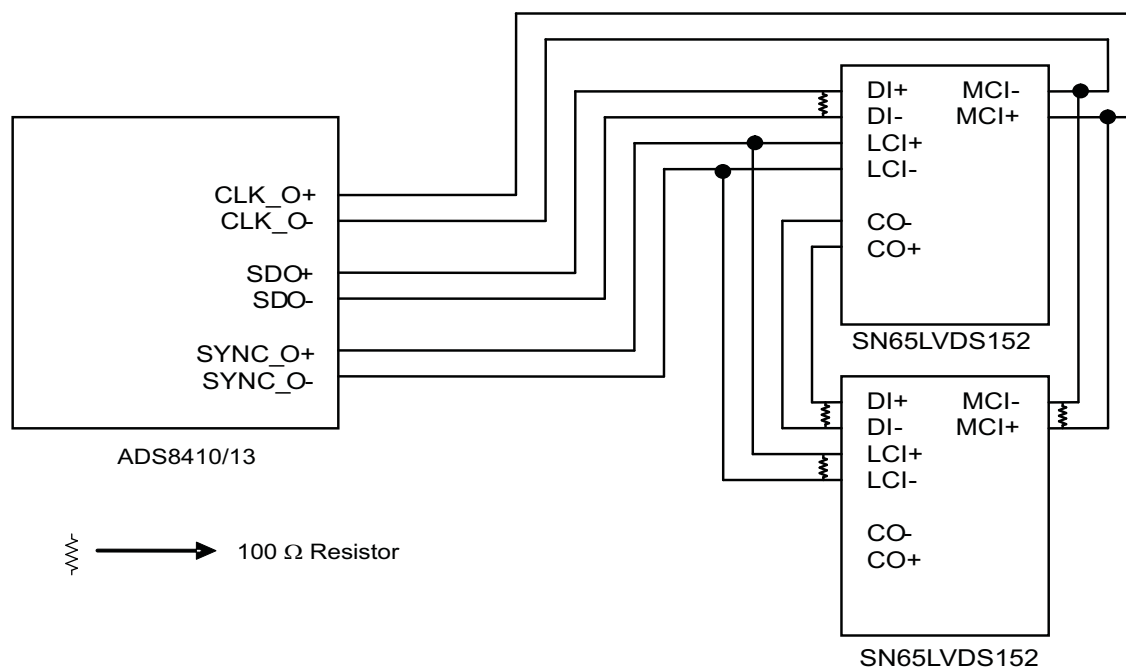


Figure 22. Third and Forth Device in the Chain

## 9 De-Serialization

The interface is compatible with the TI deserializer SN65LVDS152. SN65LVDS152 is a 10-bit deserializer. Two such devices are cascaded to get 16-bit parallel data output. The following diagram shows the connection of the deserializer with the ADC (this is the last ADC in the chain). [Figure 23](#) shows this connection with the necessary terminations.



**Figure 23. Last ADC in the Chain and the Deserializers**

## 10 Limitation on Number of Devices in the Chain

Theoretically, the number of devices that can be in daisy chained are unlimited. If more than four devices are used, the sampling rate needs to be reduced. See the *Timing Diagrams for Daisy Chain Operation* section of the ADS8410/13 data sheet for the relation between sampling rate and the number of devices in a daisy chain. However, the duty cycle of the clock output (CLK\_O) can be degraded to 40%–60% with the internal clock mode operation or with the external clock mode operation (provided external input clock (CLK\_I) duty cycle is 50%) at 200 MHz. CLK\_O of device 1 is CLK\_I of device 2. So, device 2 sees a clock with 40%–60% duty cycle as the external input clock. CLK\_O of device 2 is further degraded. Therefore, as the number of devices increases in a chain, the clock duty cycle of the last device can degrade further which may cause setup and hold-time violation. But typically, four devices can be operated in a daisy chain with a 200-MHz external or internal clock. If the clock frequency is reduced, more devices can be integrated in the chain.

## 11 Results

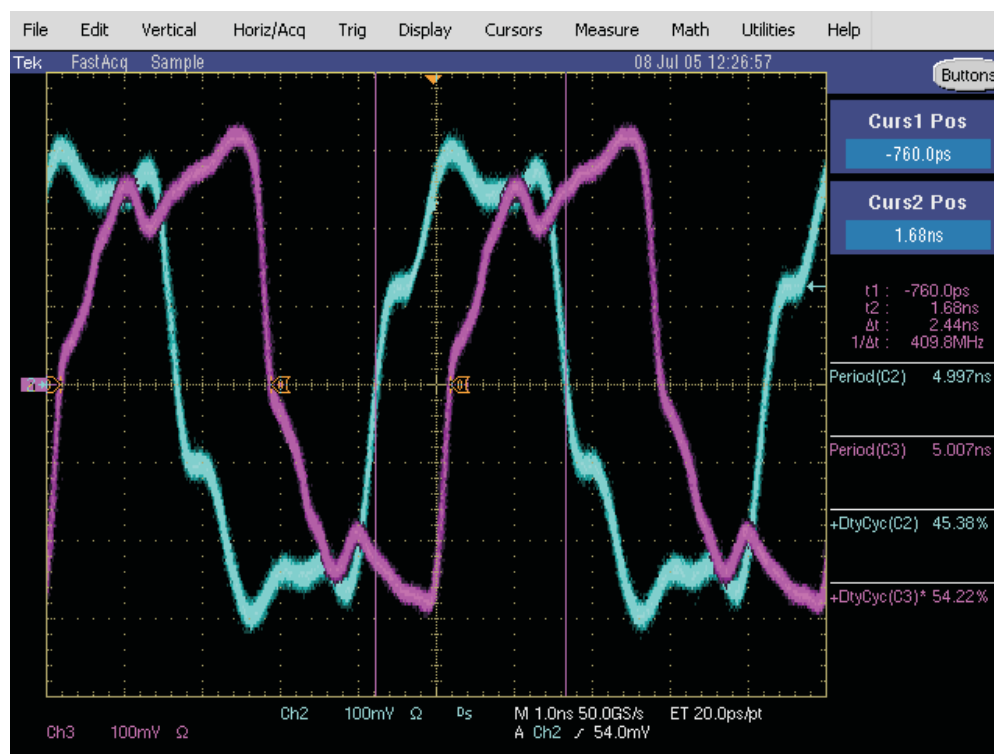
### 11.1 Clock Duty Cycle

One important parameter when multiple devices are daisy chained is the clock duty cycle. An external clock is used as an input to the first device, or the internal clock from the first device is used for the master clock. This clock then travels through four devices and finally comes out from the fourth device as CLK\_O. SDO and SYNC\_O are generated from the positive edge of CLK\_O, but they are latched at the deserializer at the negative edge of CLK\_O. Any degradation in the duty cycle shifts the negative edge of CLK\_O with respect to the positive edge of CLK\_O. This may violate setup and hold time. Careful design of transmitters and receivers of ADS8410/13 ensures that the duty cycle degradation is within the limit. [Table 2](#) lists the measured duty cycle with both external and internal clock.

**Table 2. Clock Duty Cycle**

	DUTY CYCLE				
	INPUT CLOCK	CLK_O #1	CLK_O #2	CLK_O #3	CLK_O #4
External clock	49%	56%	47%	58%	43%
Internal clock	–	52%	54%	51%	54%

The following [Figure 24](#) through [Figure 27](#) show CLK\_I and CLK\_O for four devices in a daisy chain. Blue color denotes CLK\_I, and pink color denotes CLK\_O. An external clock of 49% duty cycle is used in these examples.



**Figure 24. CLK\_I and CLK\_O of Device 1**

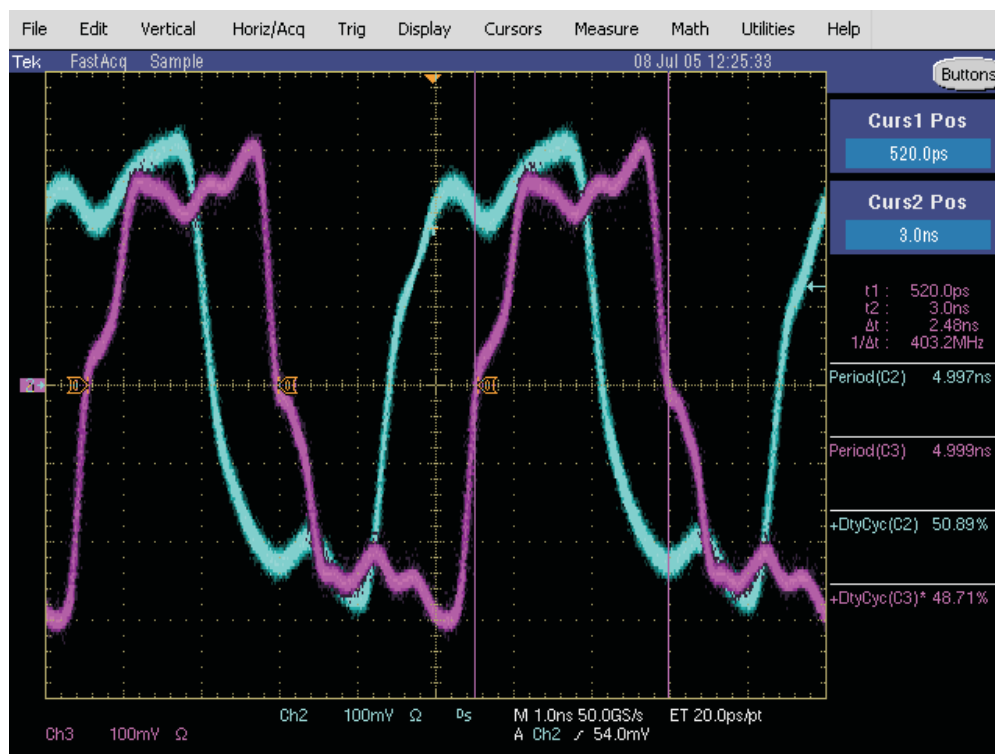


Figure 25. CLK\_I and CLK\_O of Device 2

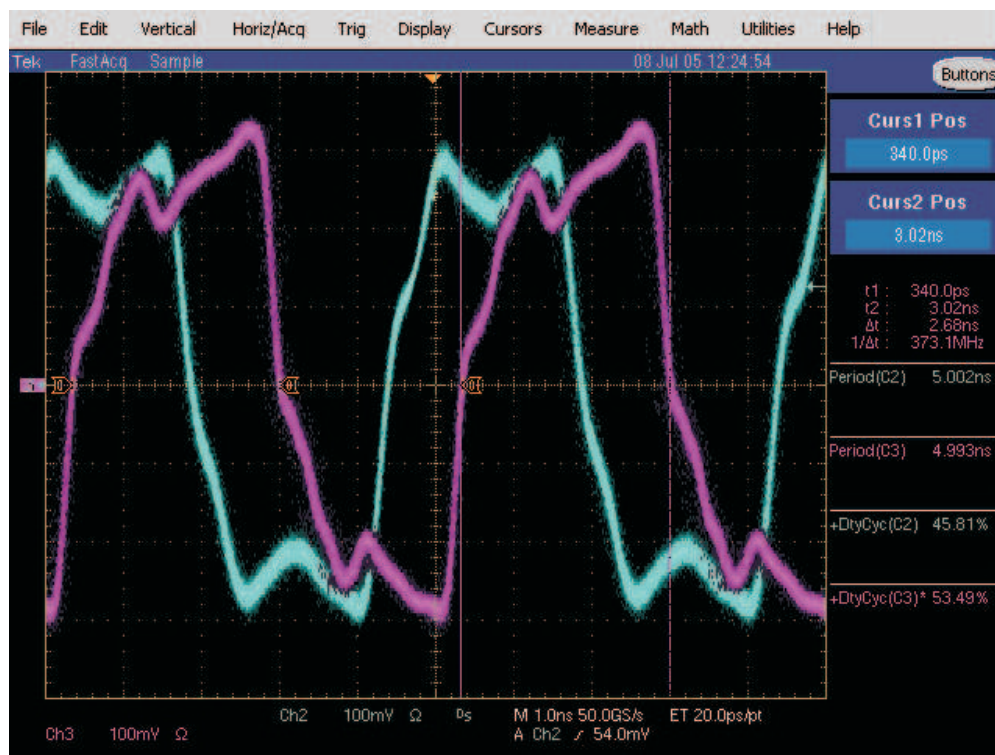


Figure 26. CLK\_I and CLK\_O of Device 3

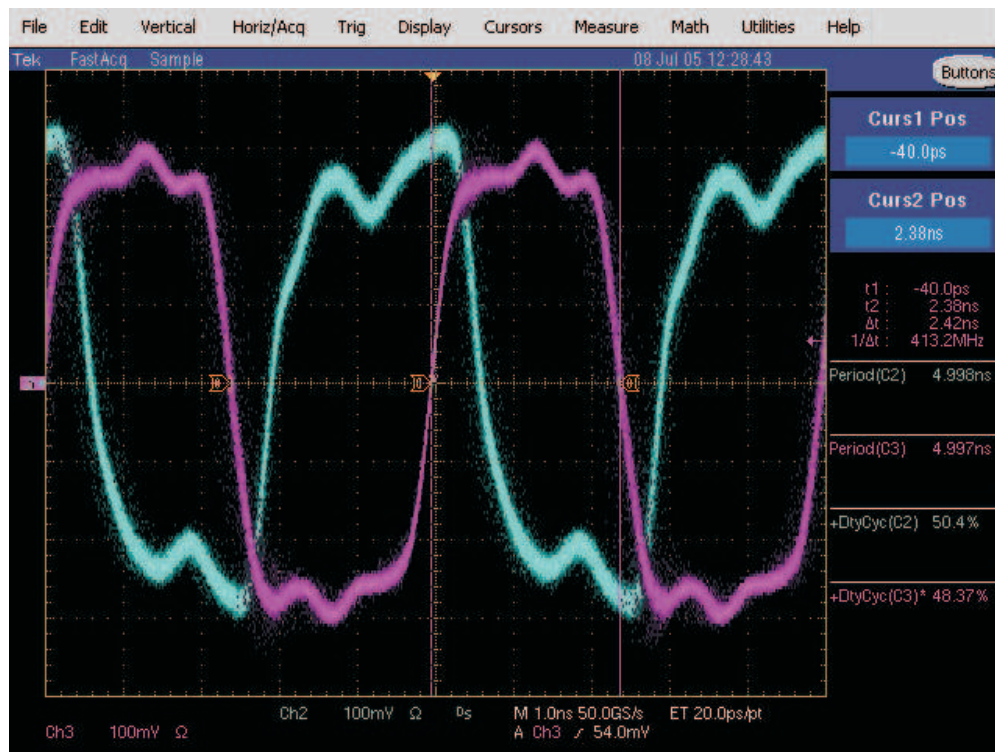


Figure 27. CLK\_I and CLK\_O of Device 4

## 11.2 Linearity Across Devices

Table 3 shows DNL and INL of ADS8413 versus the device number in the daisy chain. The data has been captured for four devices in the chain at 200-MHz external clock, and 2-MSPS throughput.

Table 3. Linearity of Four Devices in the Chain

DEVICE	DNL		INL	
	MAX	MIN	MAX	MIN
1	0.88	-0.68	1.13	-1.62
2	0.87	-0.77	1.59	-1.15
3	0.88	-0.70	1.14	-1.30
4	0.79	-0.73	1.36	-1.21

## 11.3 SNR and THD Across Devices

Table 4 shows the ac performance of ADS8413 in the daisy chain. The data has been collected for four devices with the input-signal frequency of 20 kHz at a sampling rate of 2 MSPS and an external clock of 200 MHz.

Table 4. SNR and THD of Four Devices in the Chain

DEVICE	SNR	THD
1	91.07	-103.66
2	90.54	-105.74
3	91.38	-101.08

**Table 4. SNR and THD of Four Devices in the Chain (continued)**

DEVICE	SNR	THD
4	91.39	-101.12

### 11.4 Overdrive Test

The ADS8410/13 works in daisy-chain mode excellently even if one or more devices are overdriven with input voltage more than device power supply. This was tested with a power supply of 5 V. The inputs (IN+, and IN-) were overdriven by 5.3 V (+0.3 V for IN- in case of ADS8410) and -0.3V (absolute maximum rating). The overdriven device outputs SDO, SYNC\_O, and CLK\_O normally. The data from the overdriven device may not be correct because absolute input voltage range is lower than this (-0.2 to Vref + 0.2). All other devices (without overdrive) function normally in the chain.

## 12 Conclusion

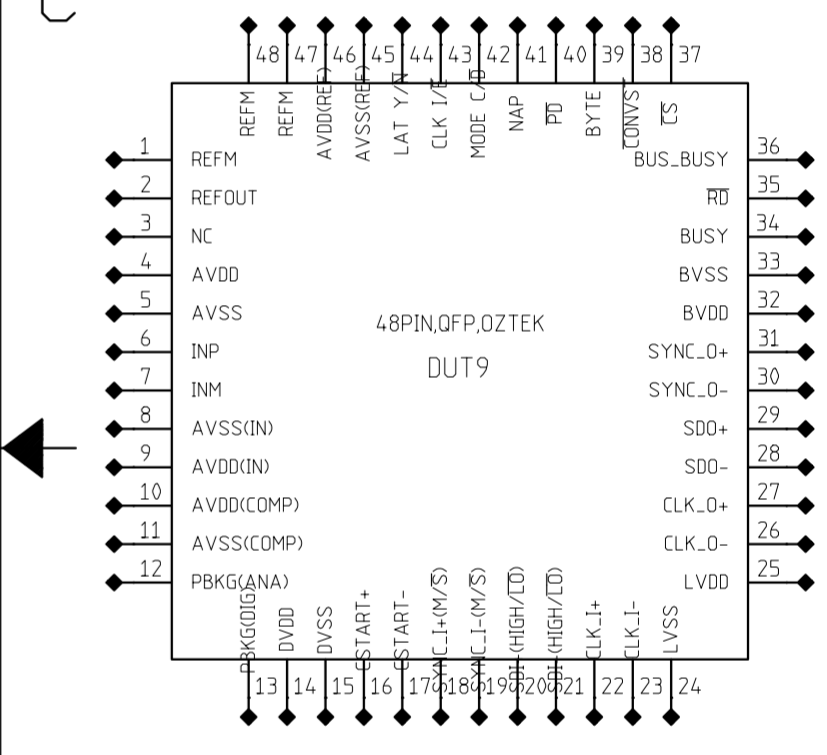
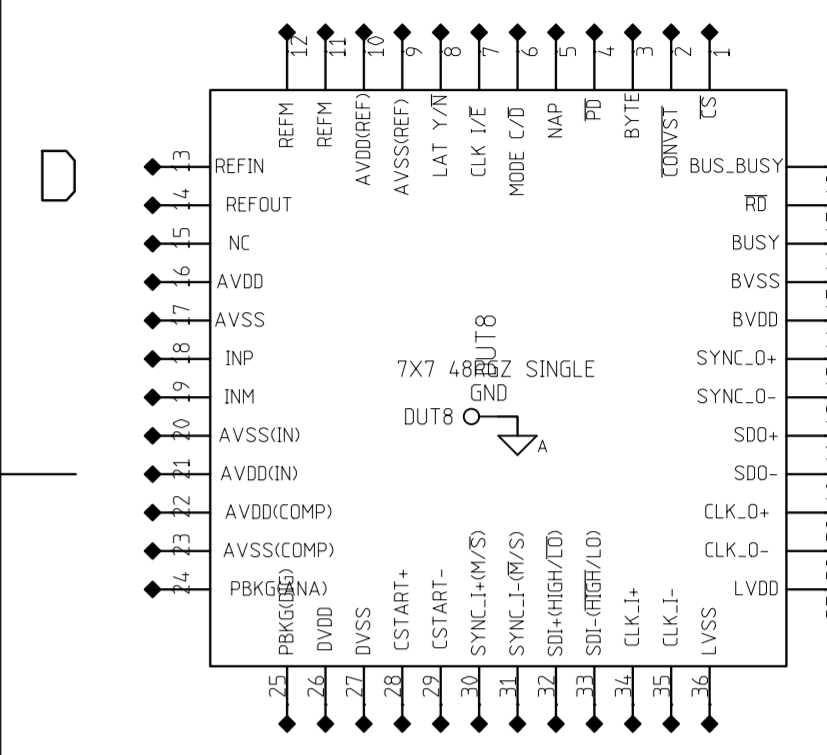
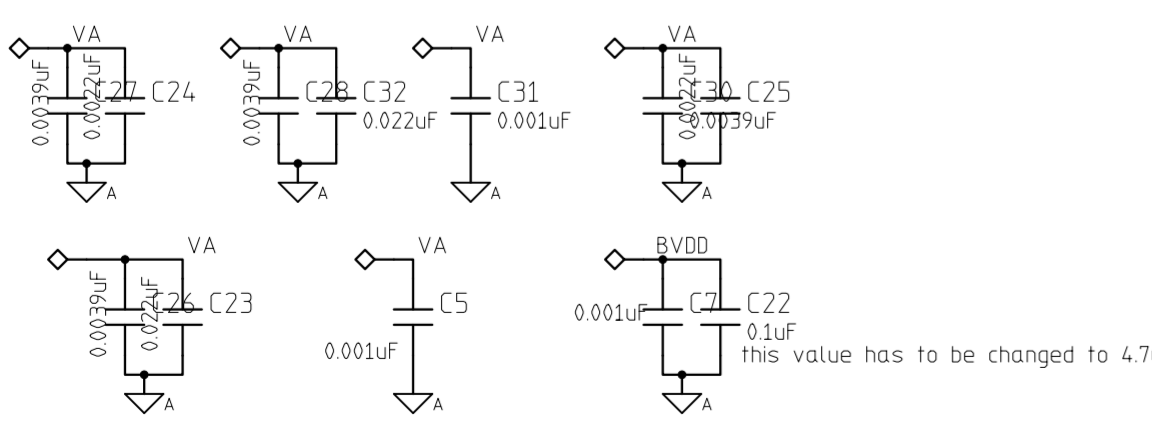
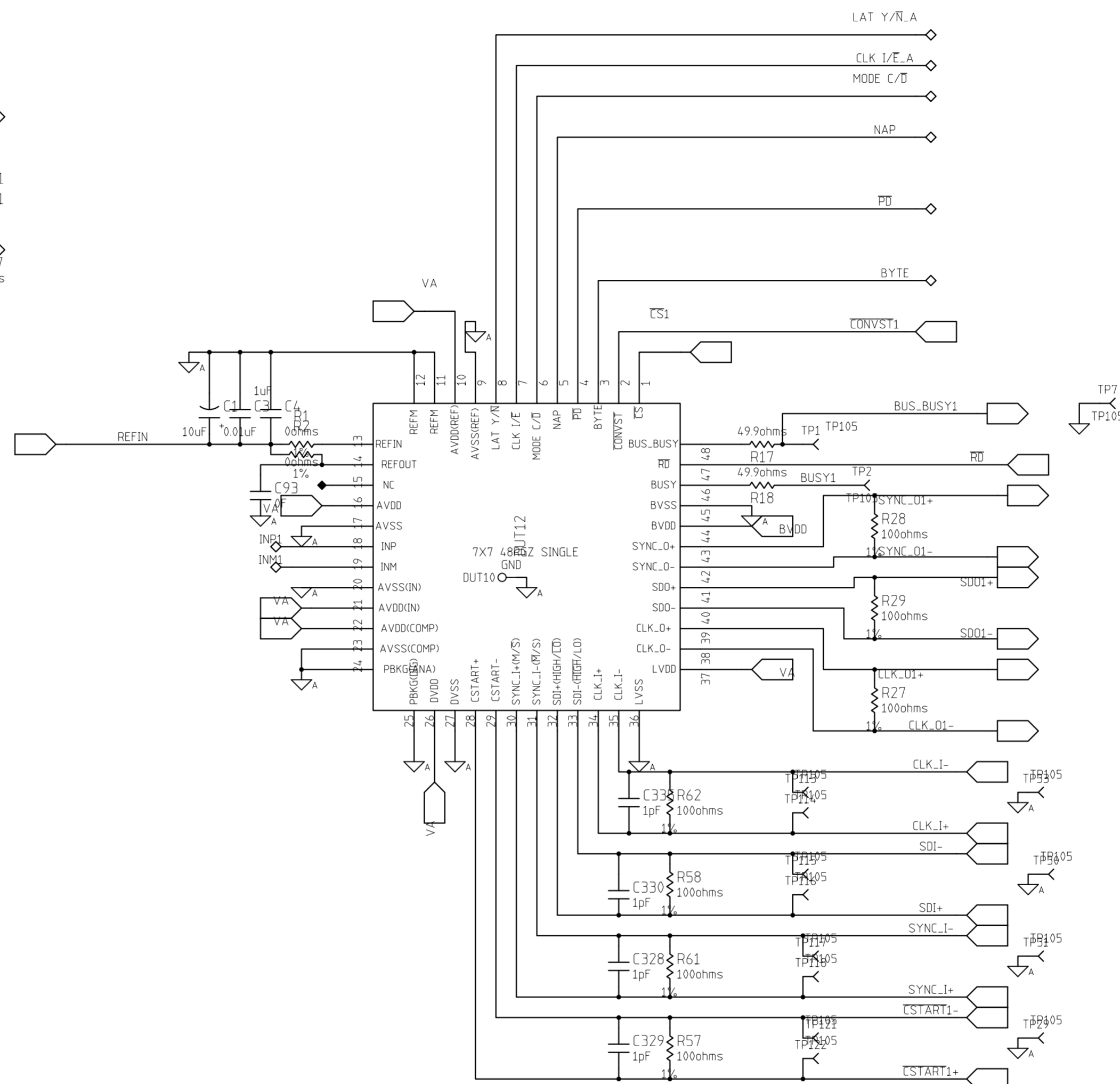
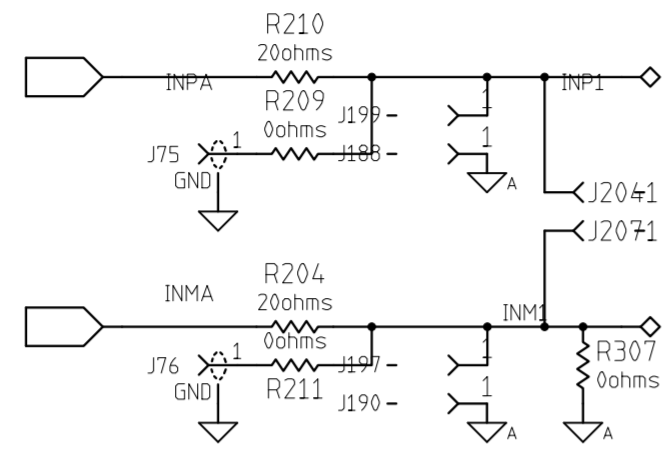
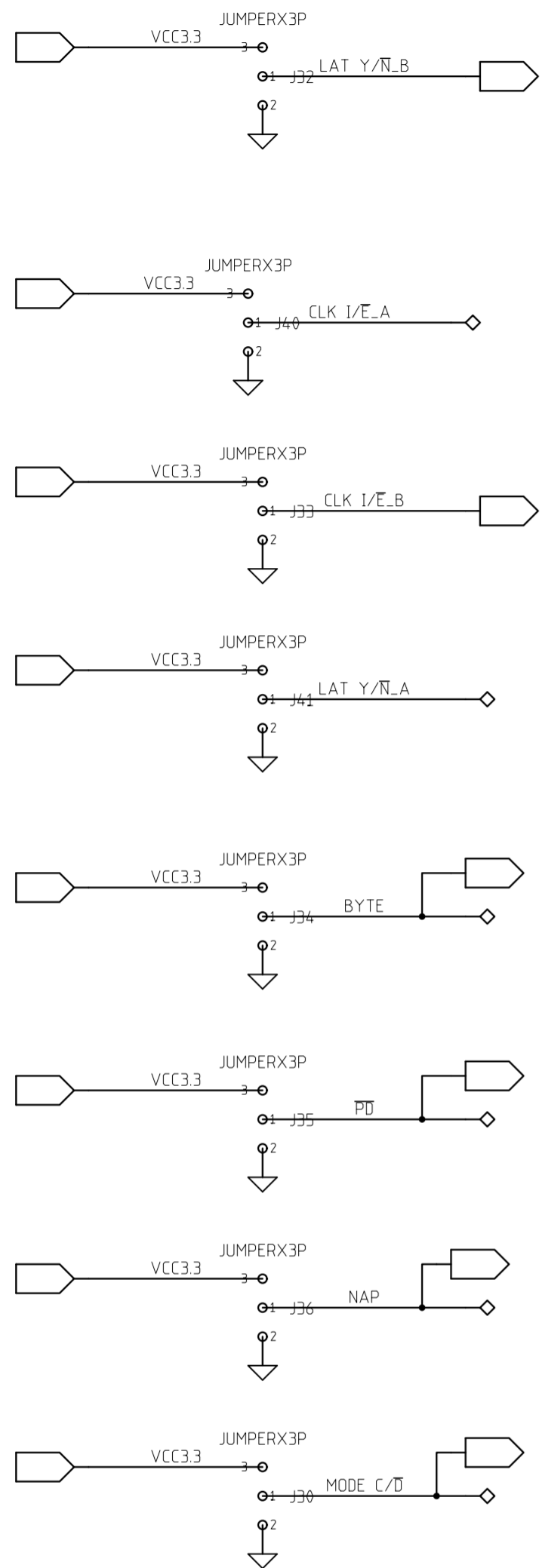
Daisy-chain mode offers a free-running clock which helps to synchronize digital circuitry easily. The free-running nature of the clock offers the flexibility to use a PLL in the digital system. This system can run with its own internal clock (clock is generated from the first device) or an external clock. The external clock should be a free-running clock. The full frame (conversion and acquisition) of the sampling time of the ADC is available for data transfer. This allows using four devices with a throughput of 2 MSPS. No performance degradation was seen with four devices in a daisy-chain configuration.

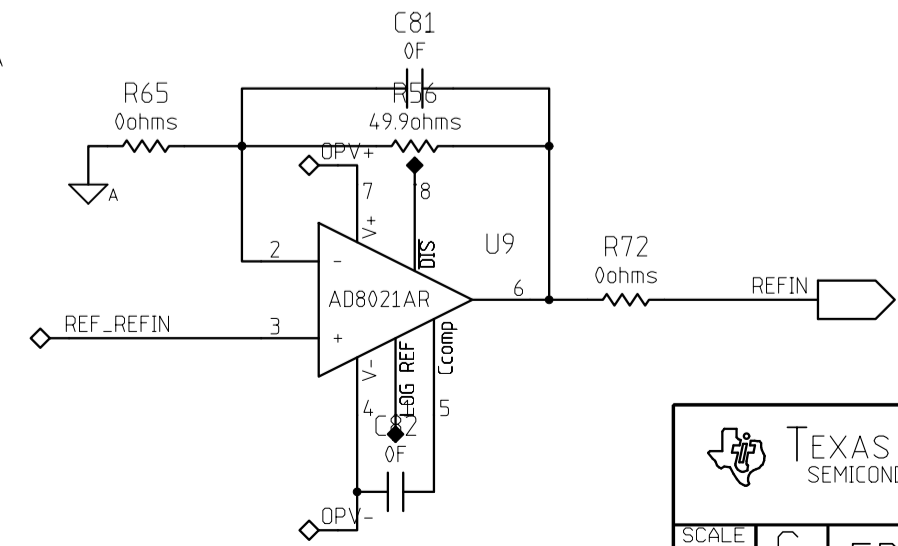
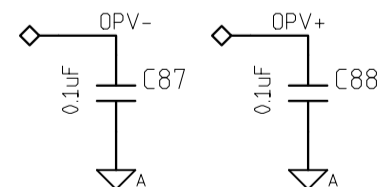
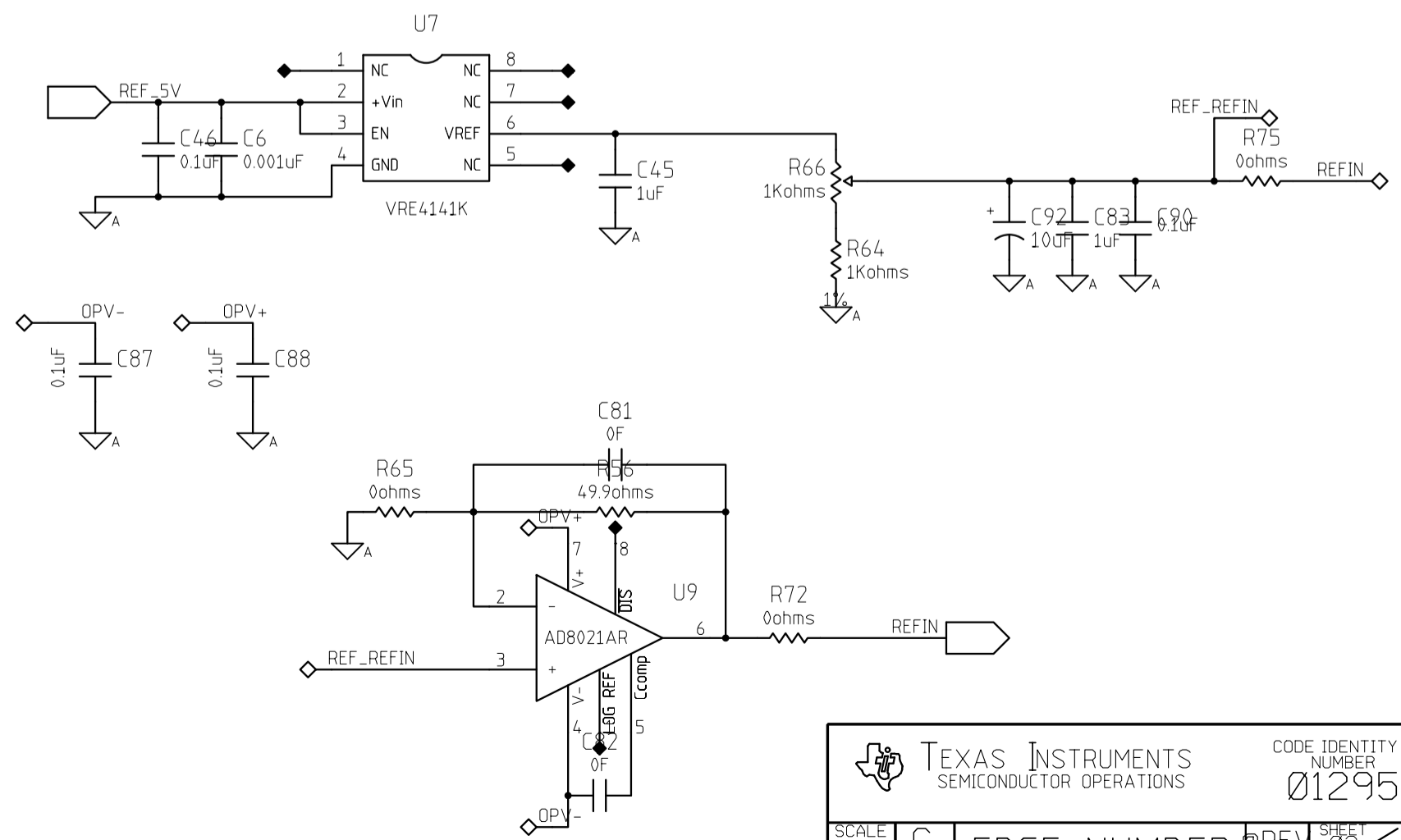
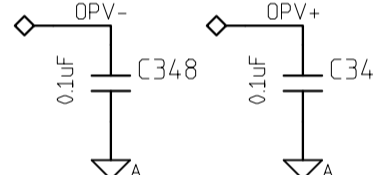
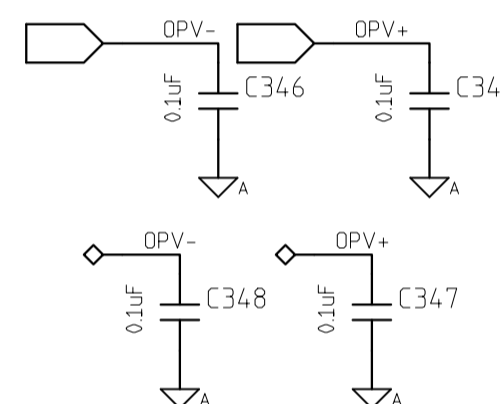
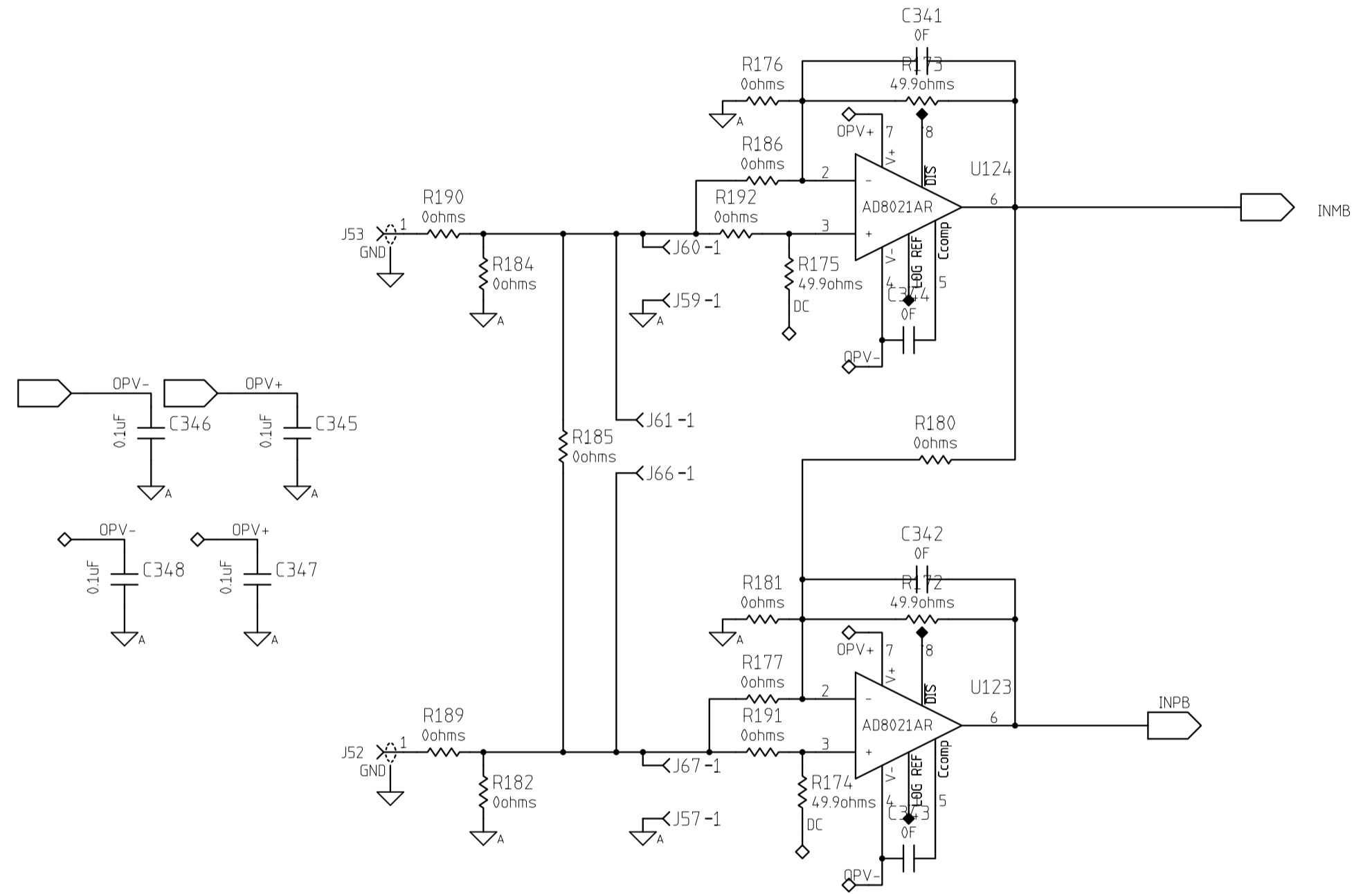
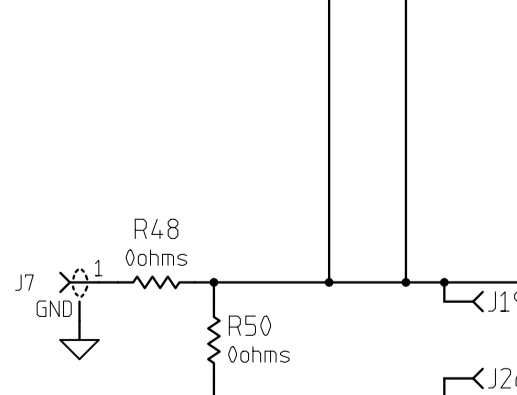
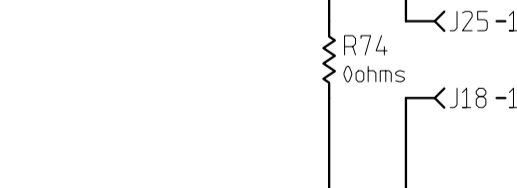
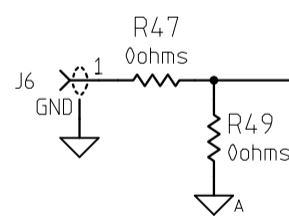
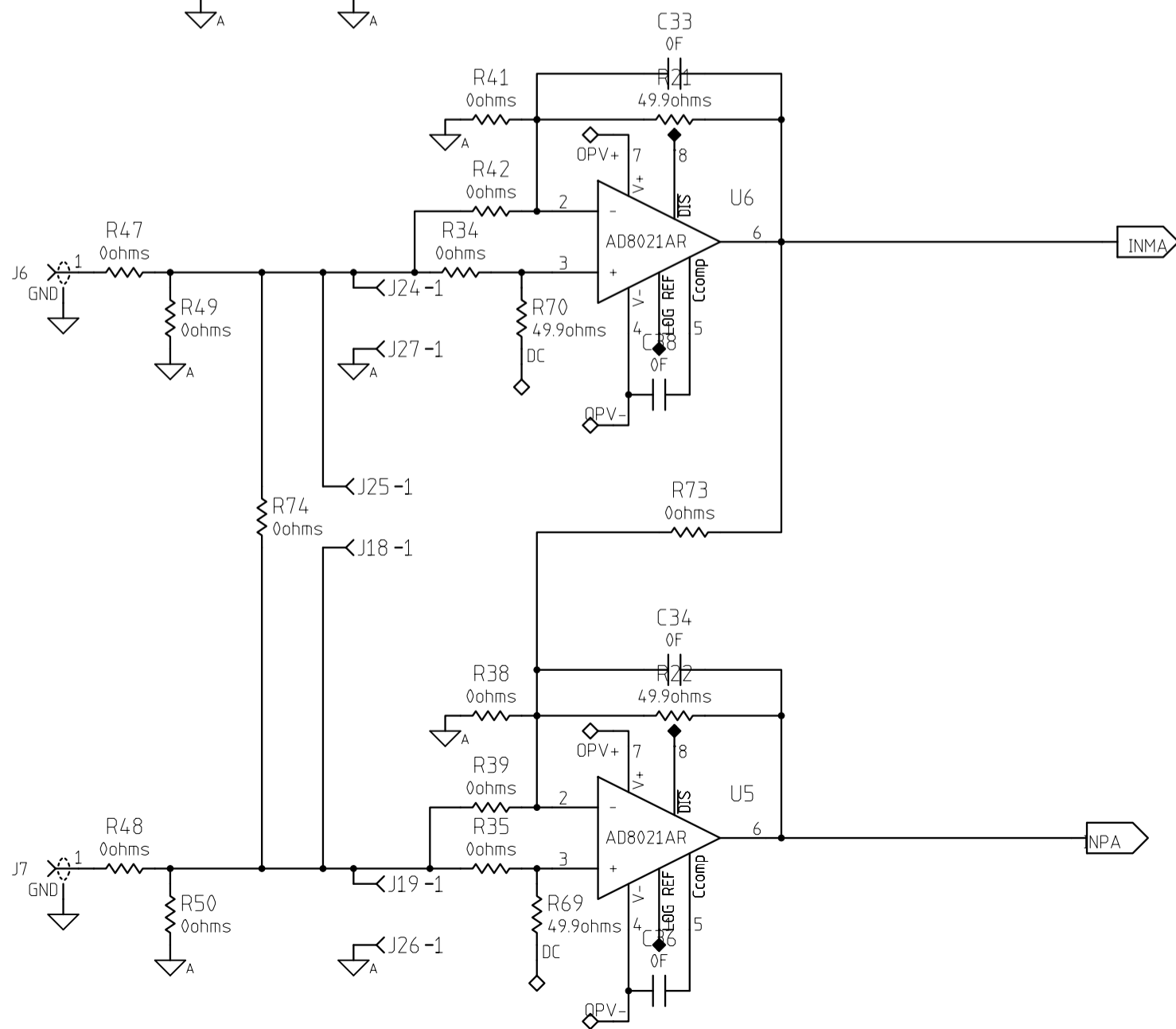
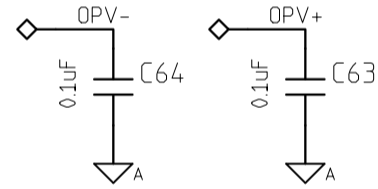
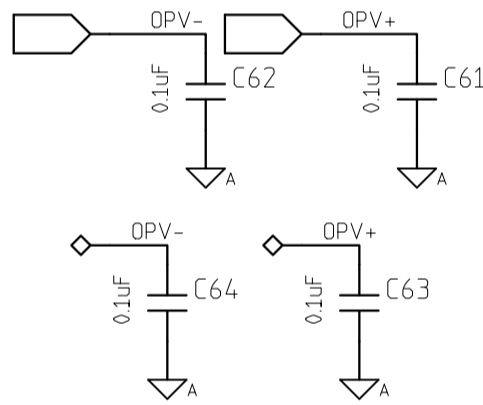
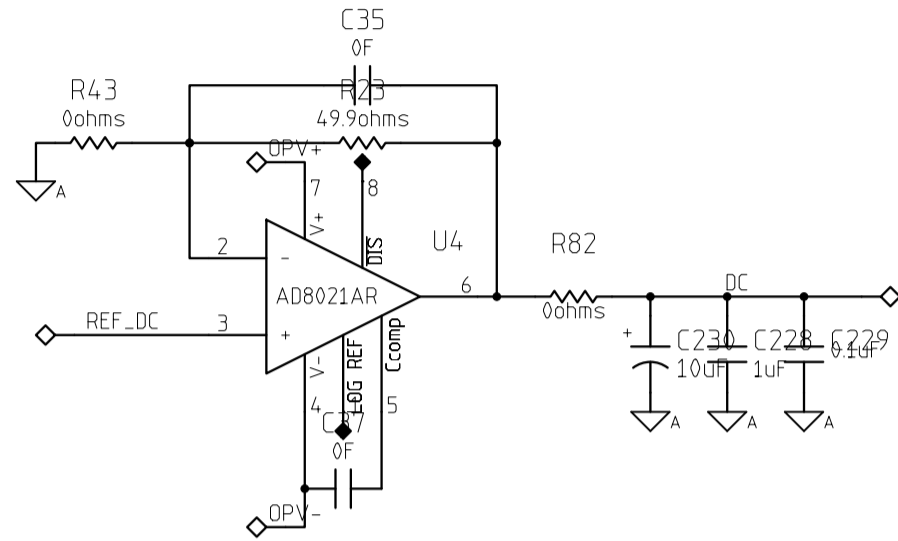
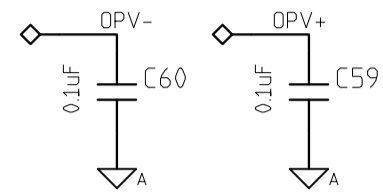
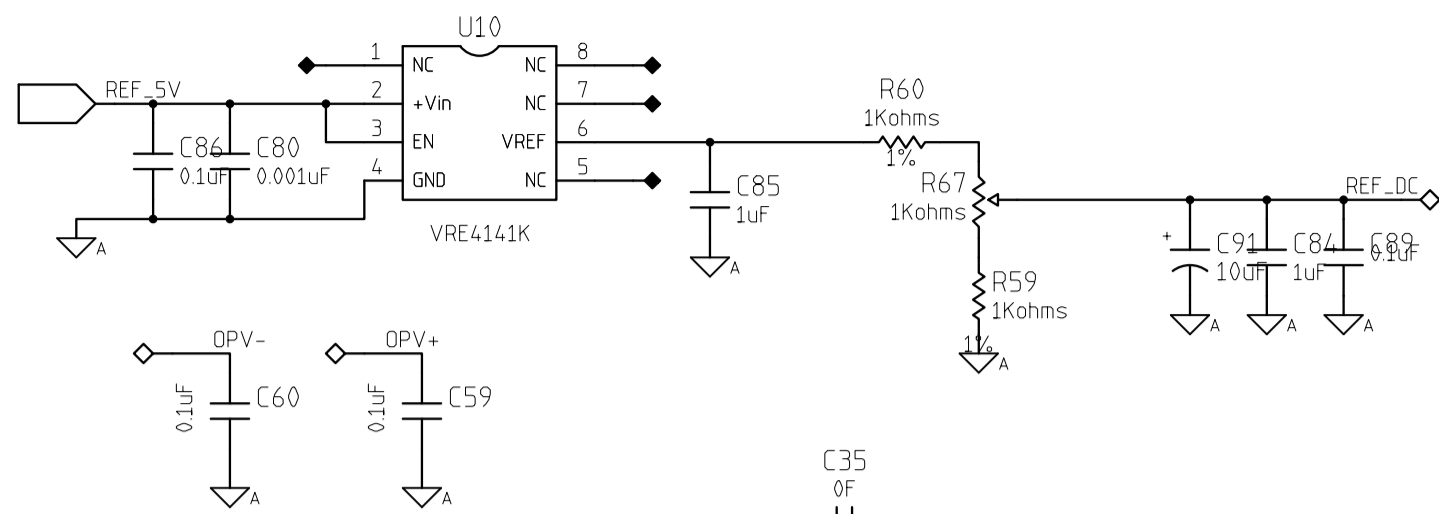


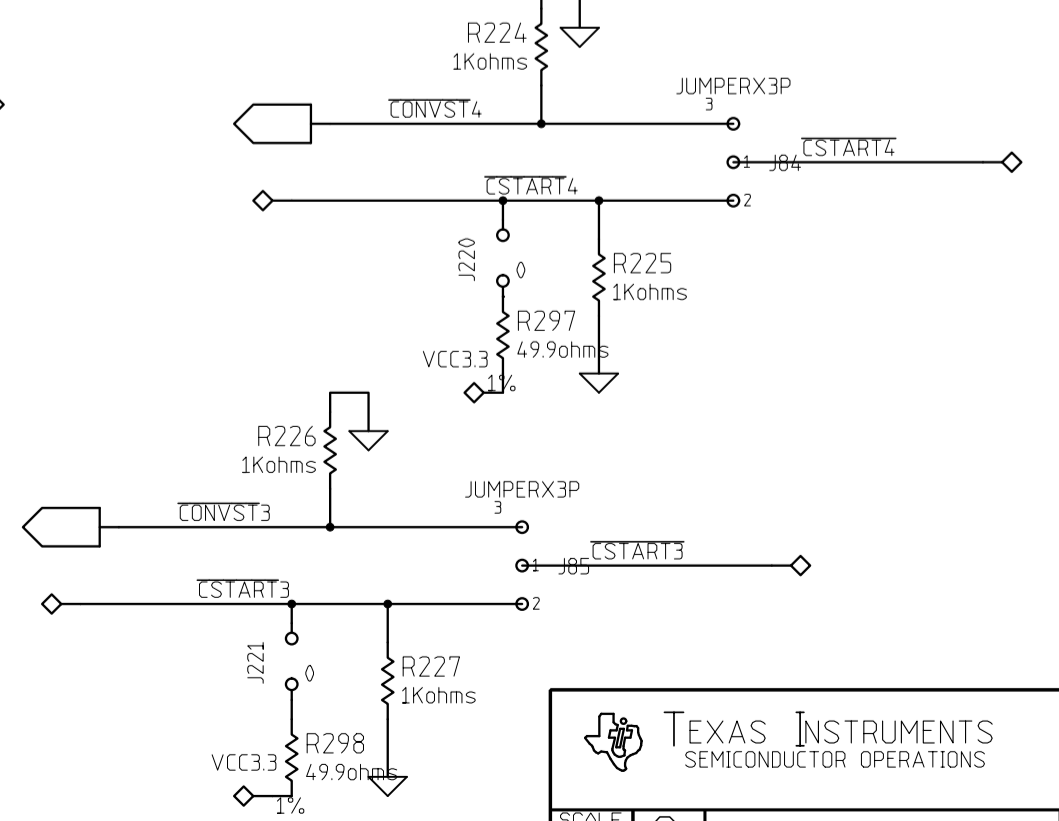
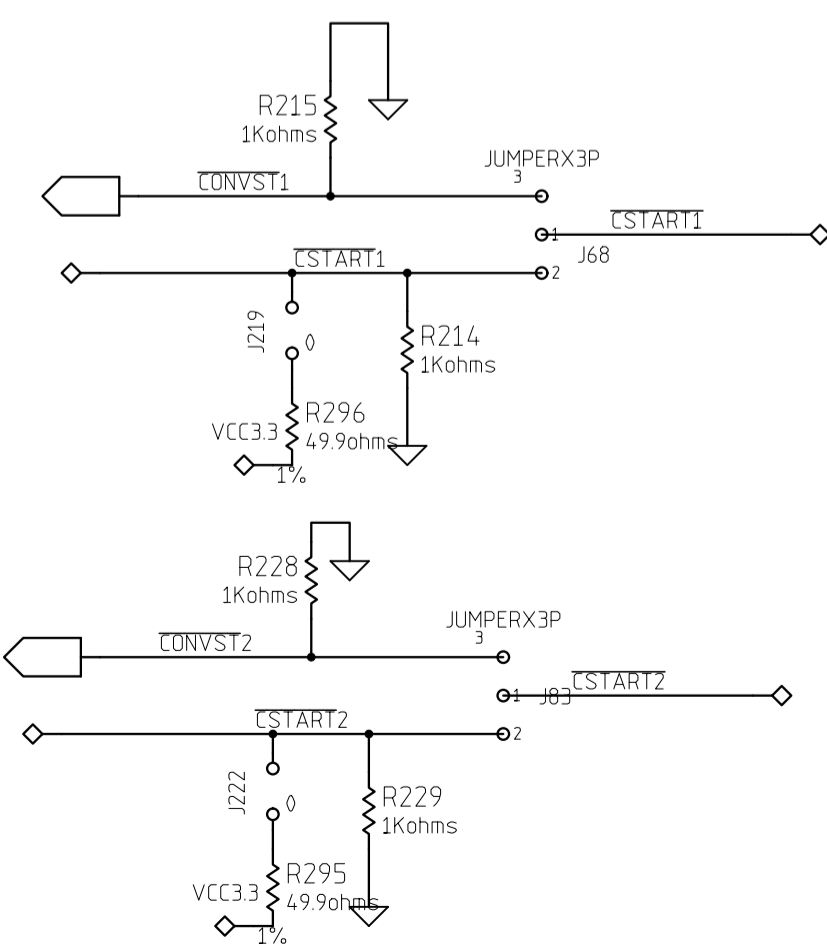
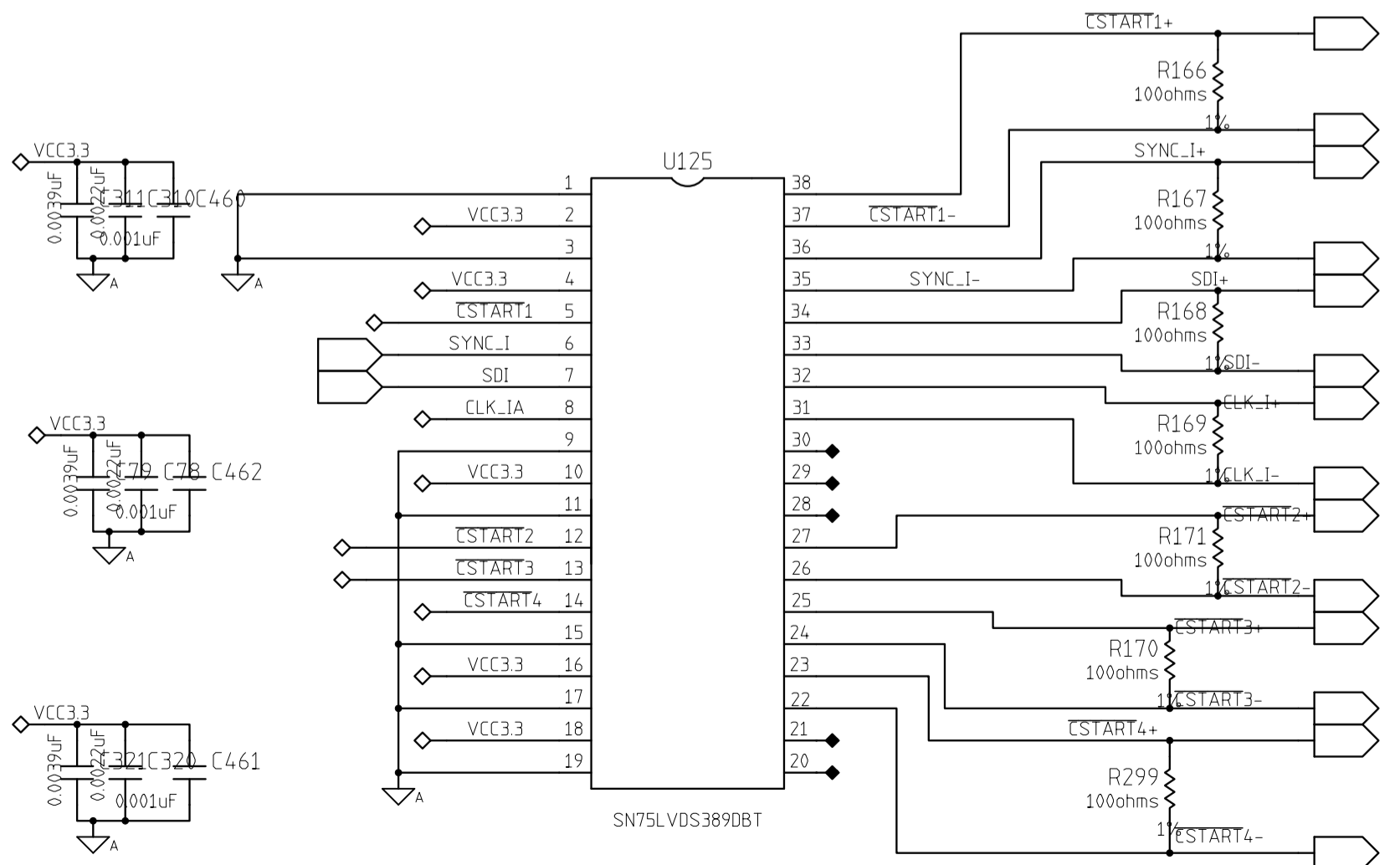
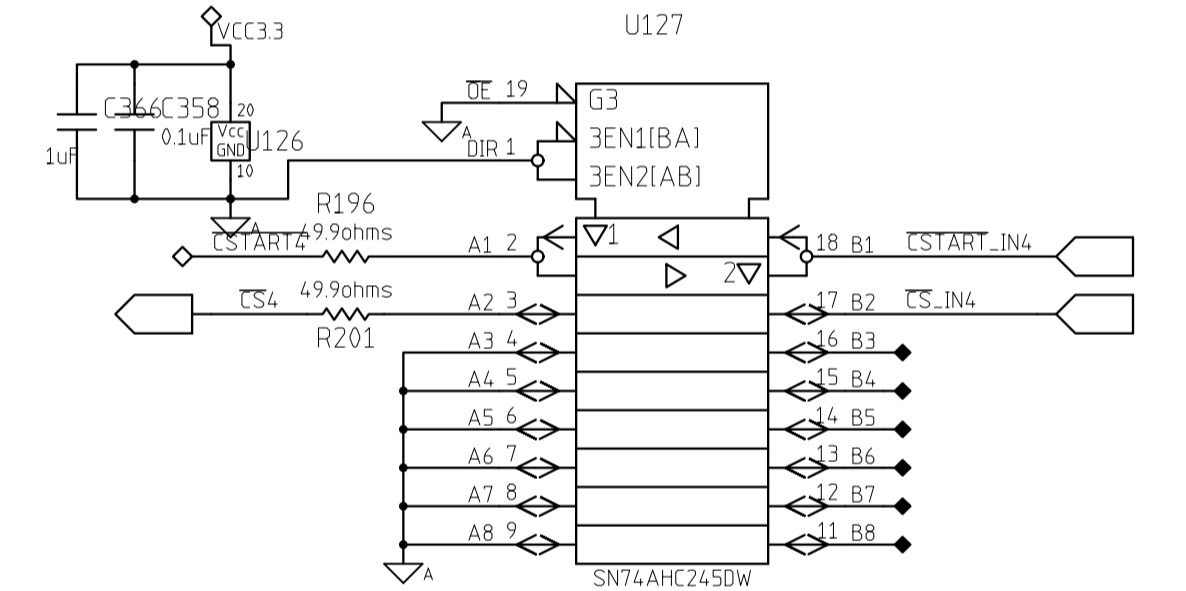
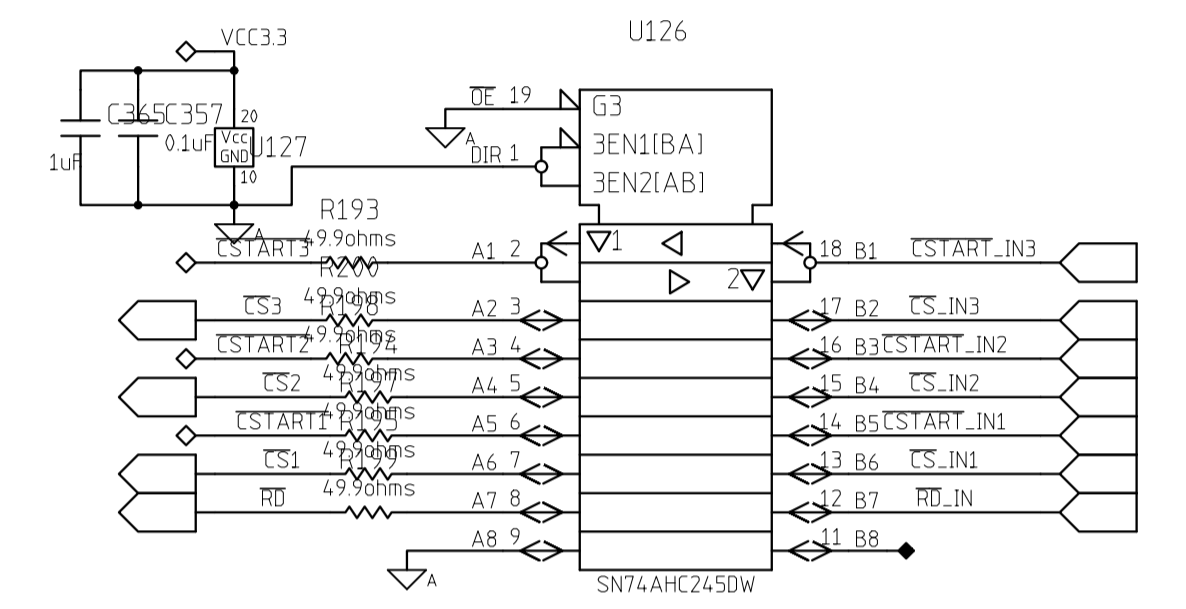
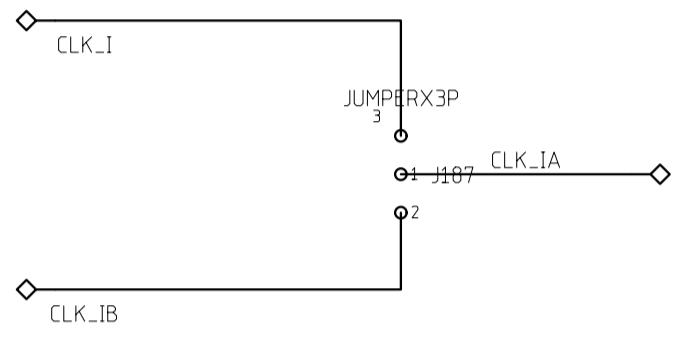
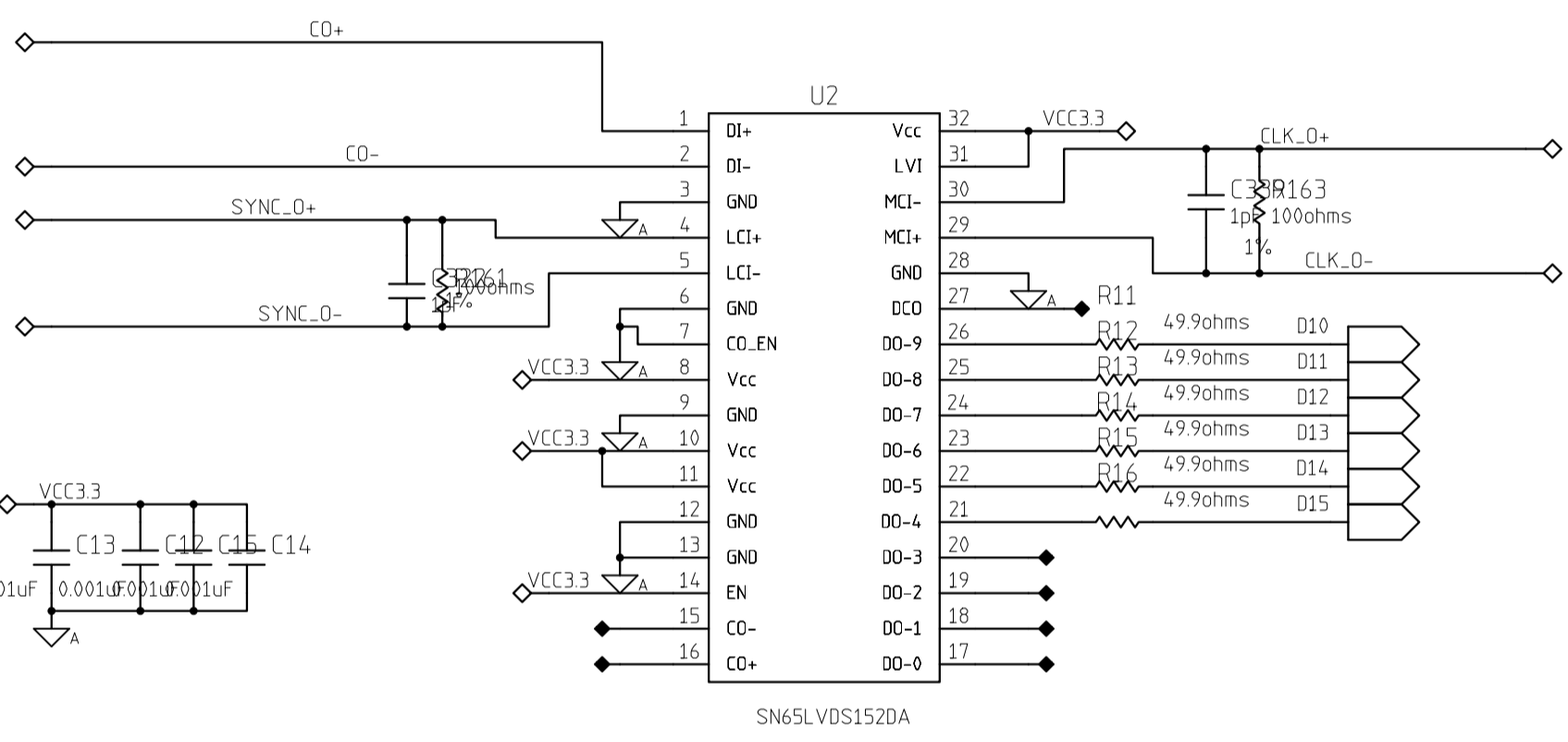
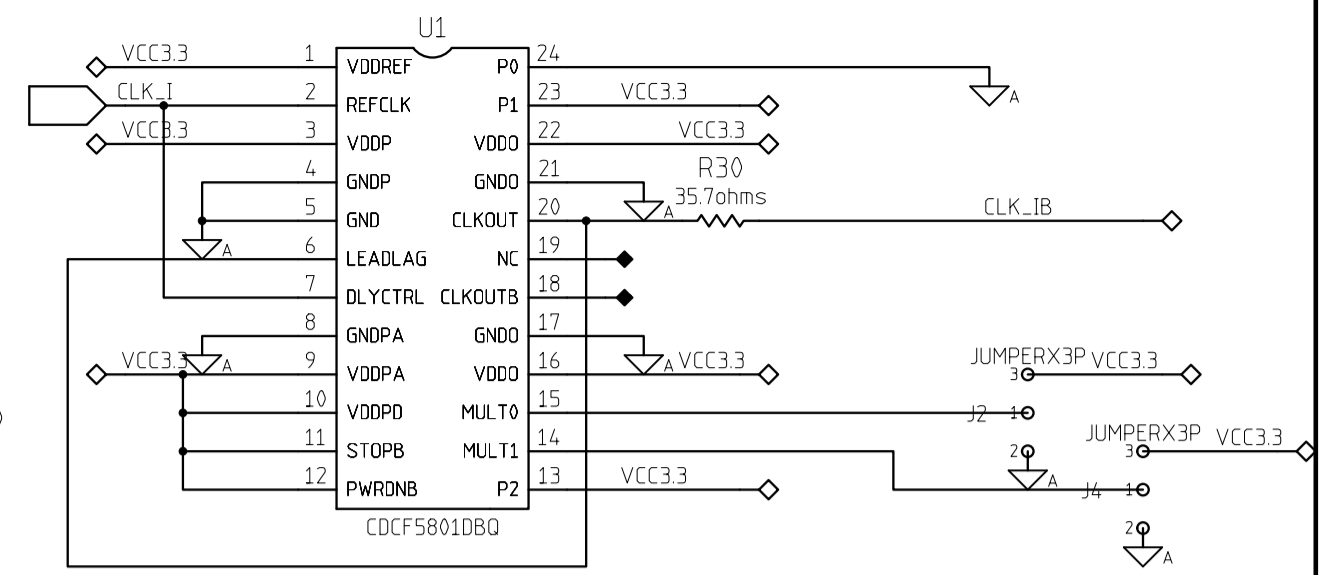
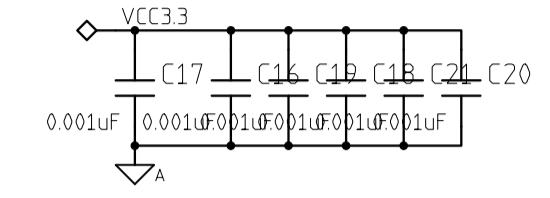
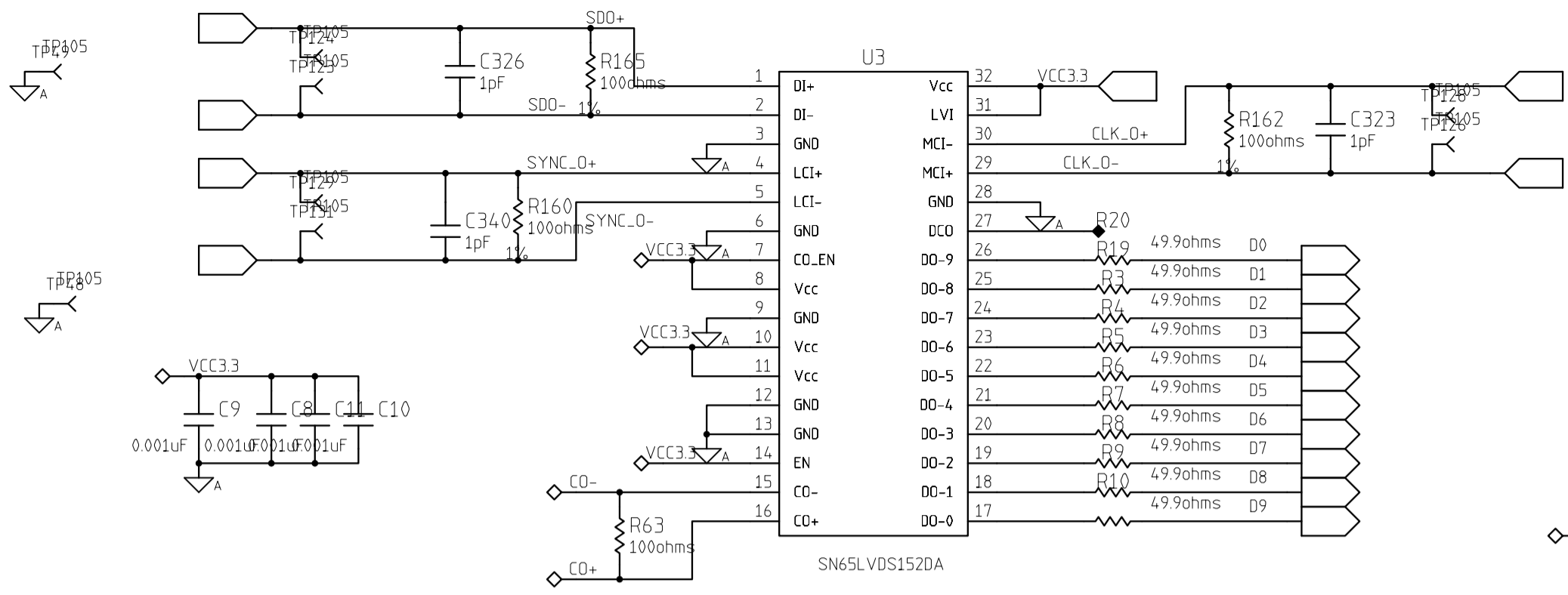
## **Appendix A ADS8413EVM Daisy Chain Schematics, Layout, and Photograph**

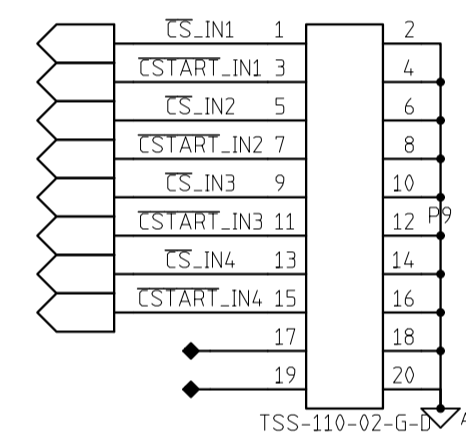
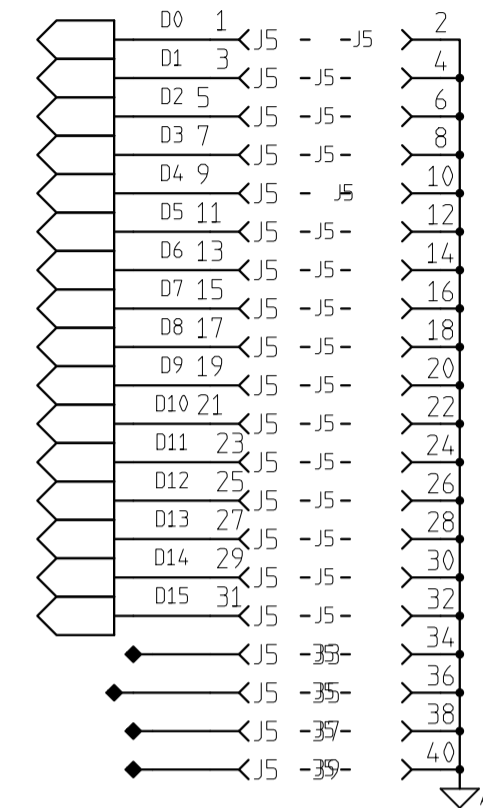
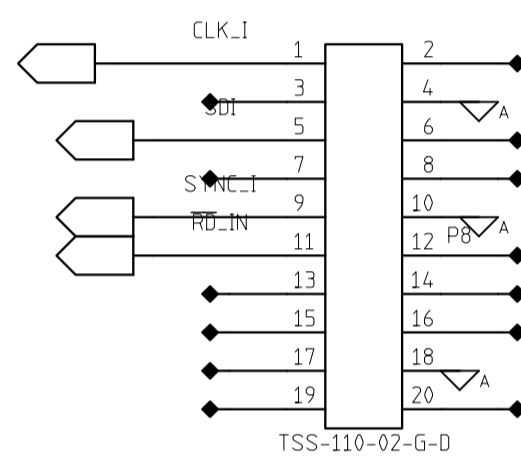
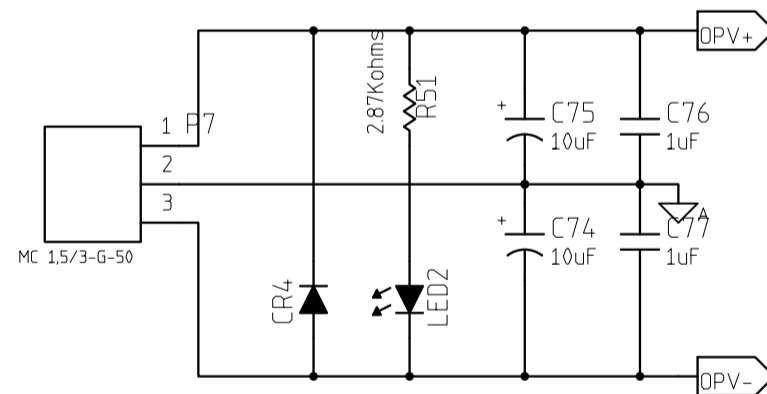
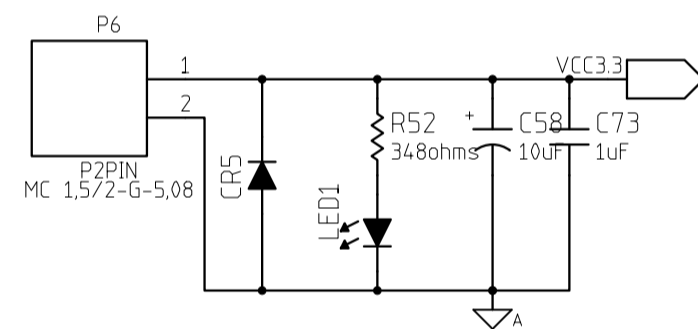
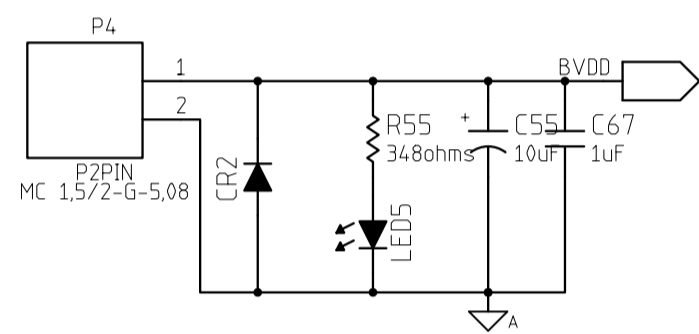
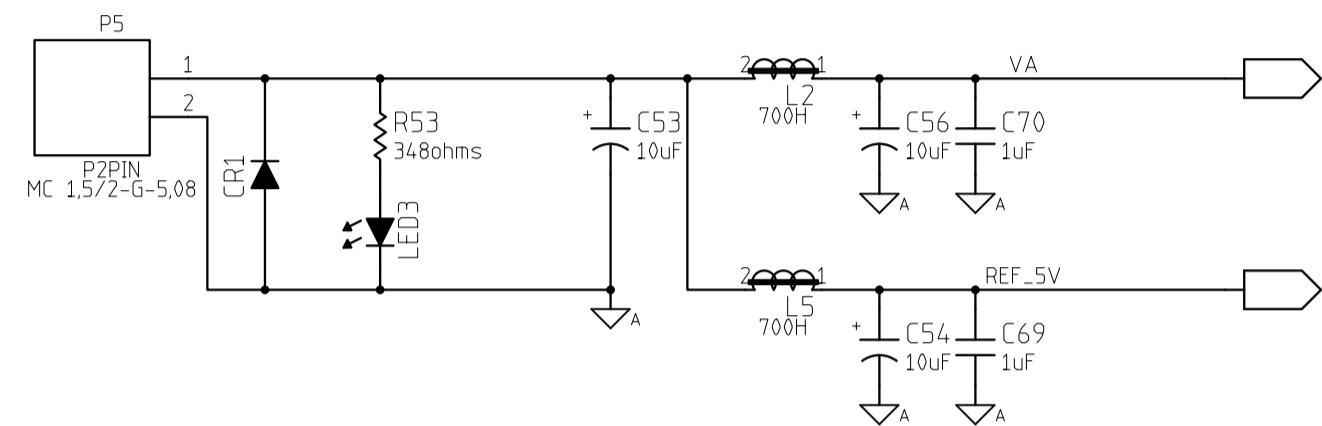
### **A.1 Schematics**

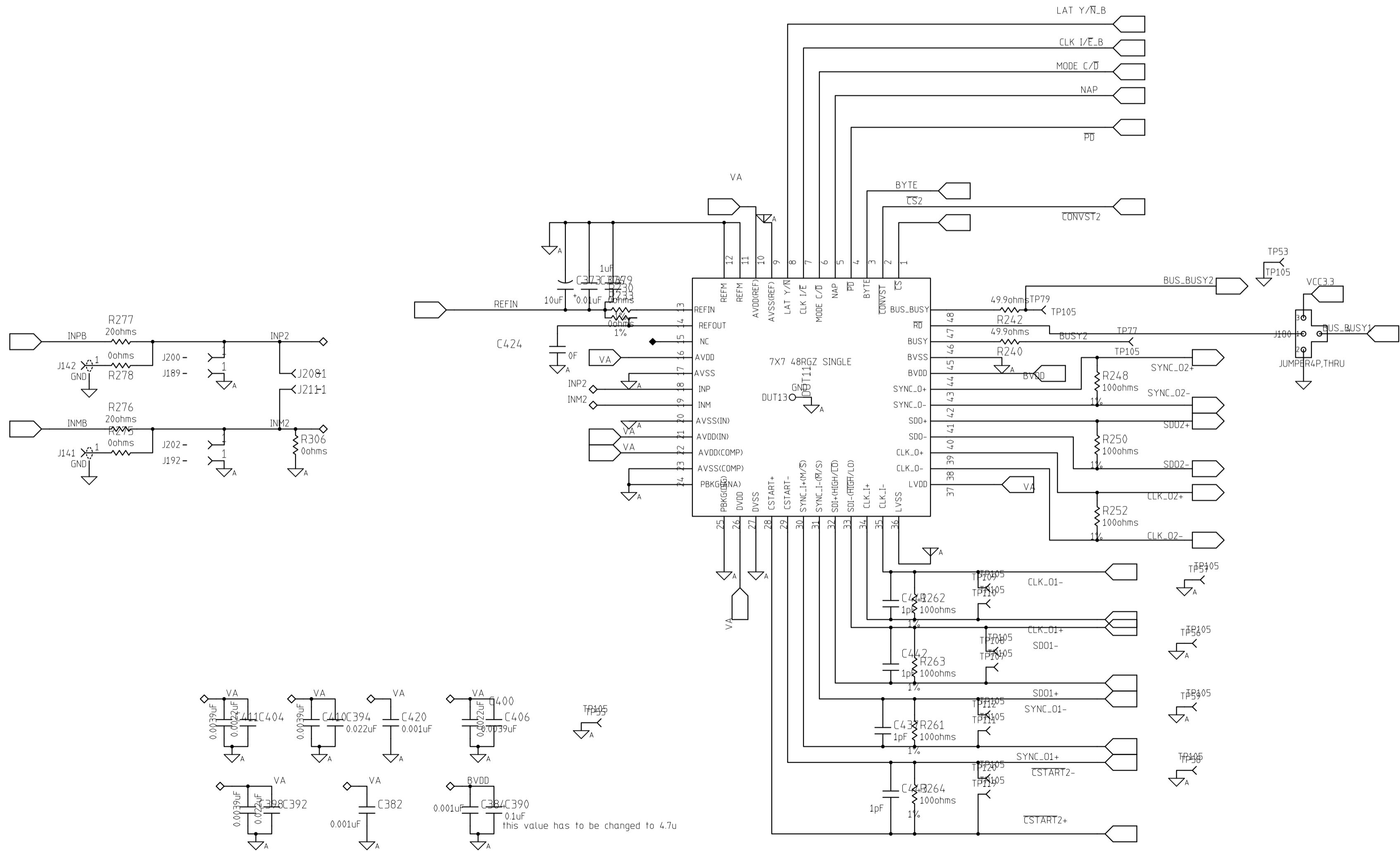
The daisy chain schematics are affixed to this page.

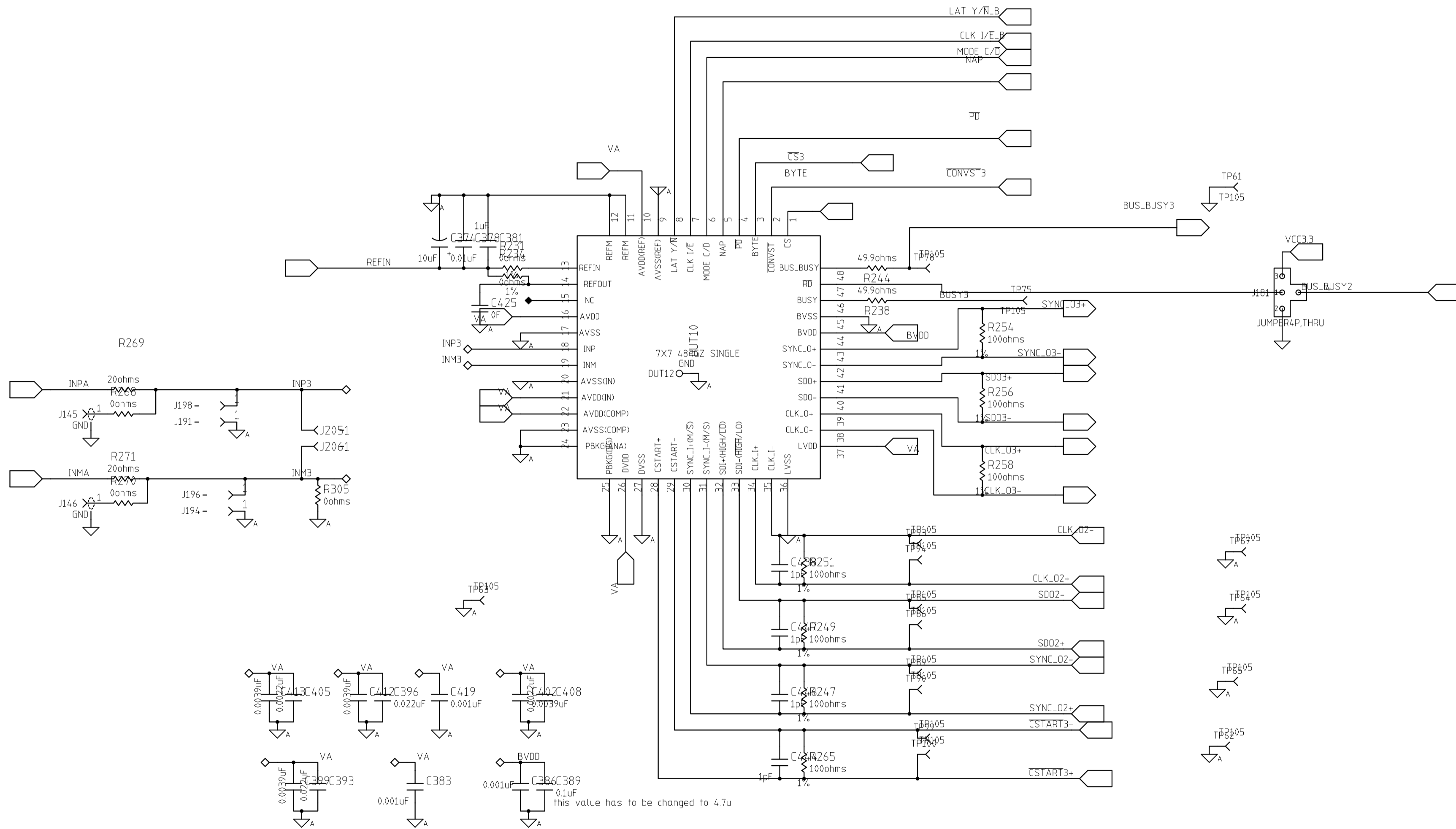


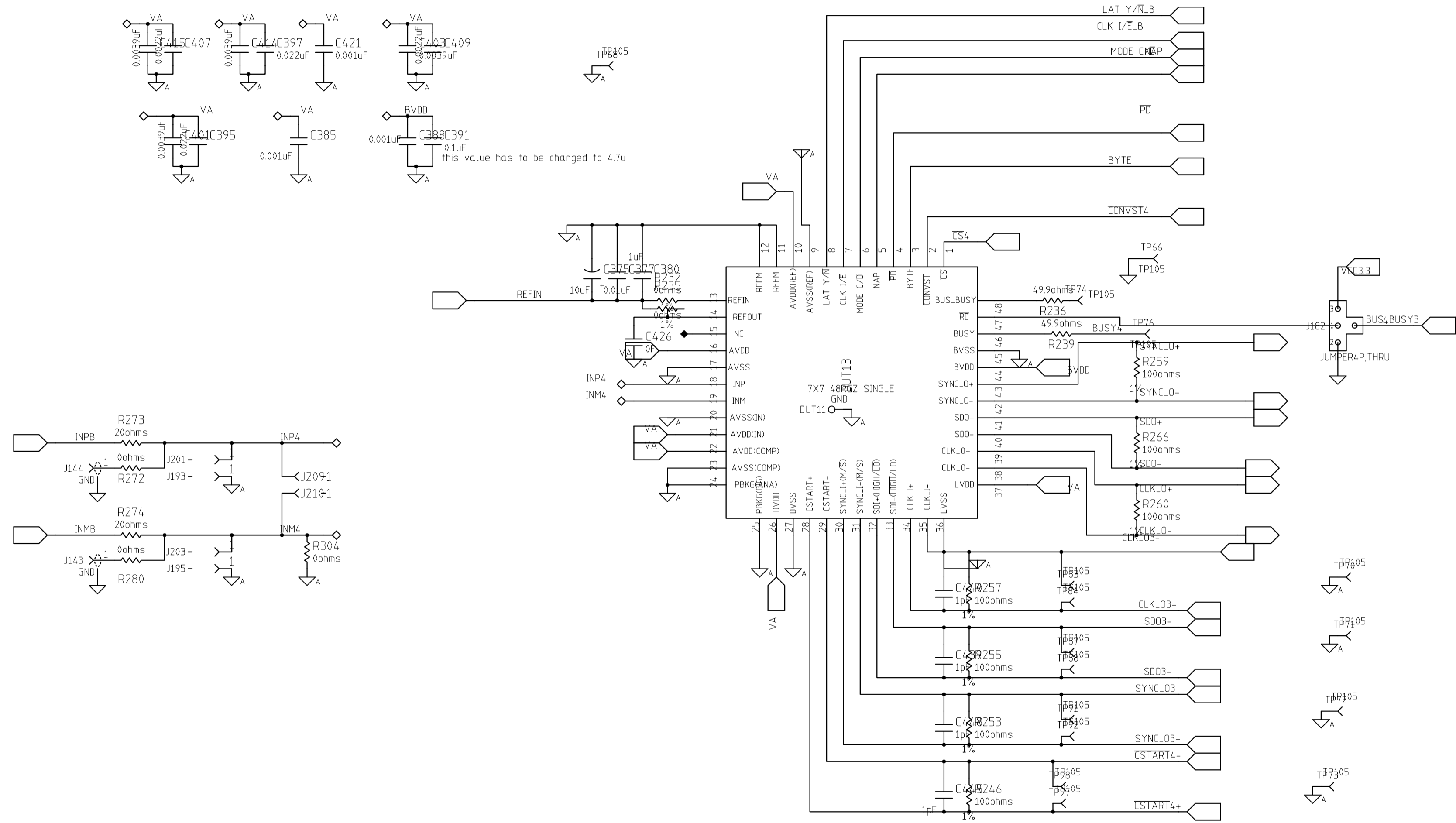








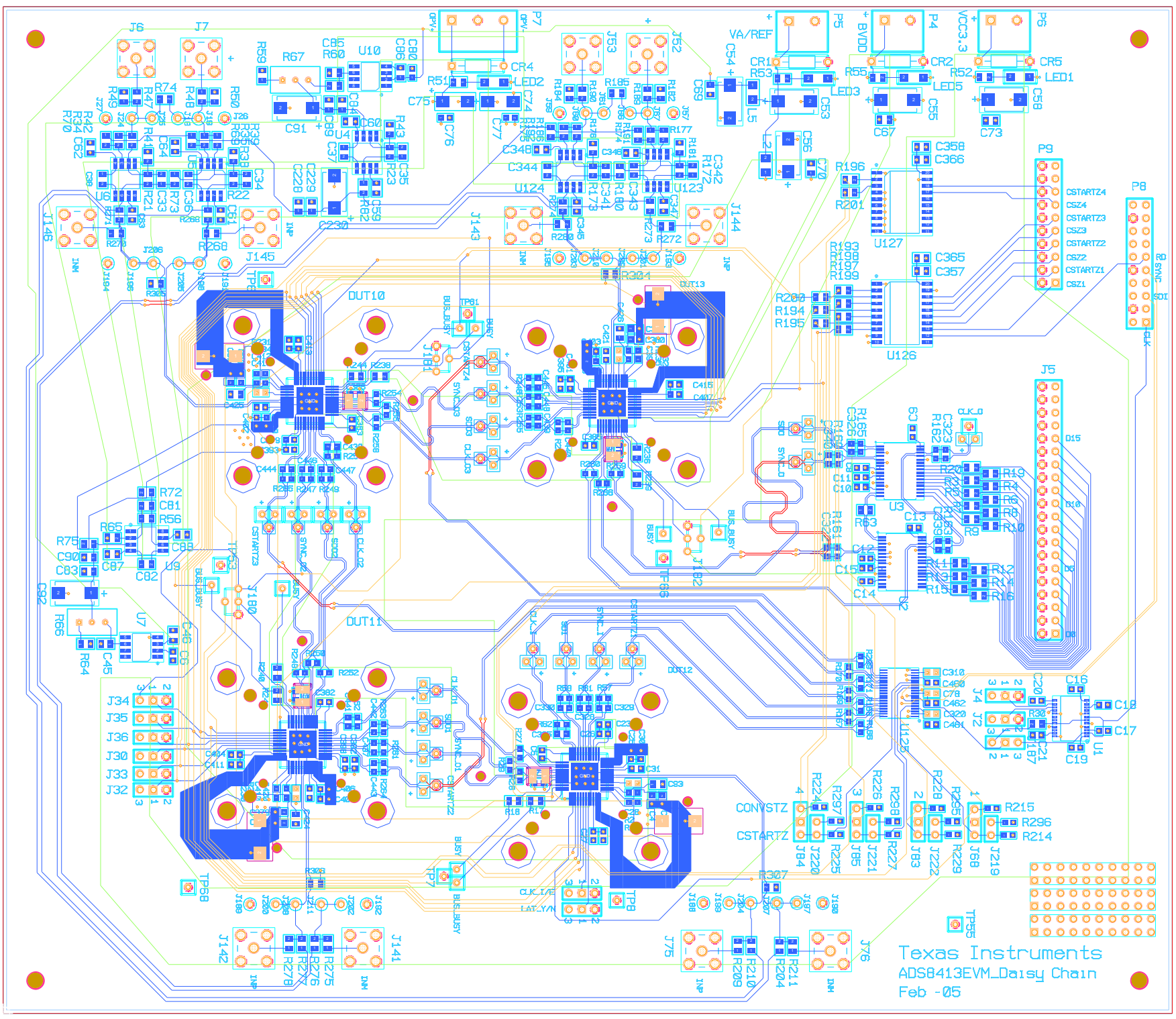






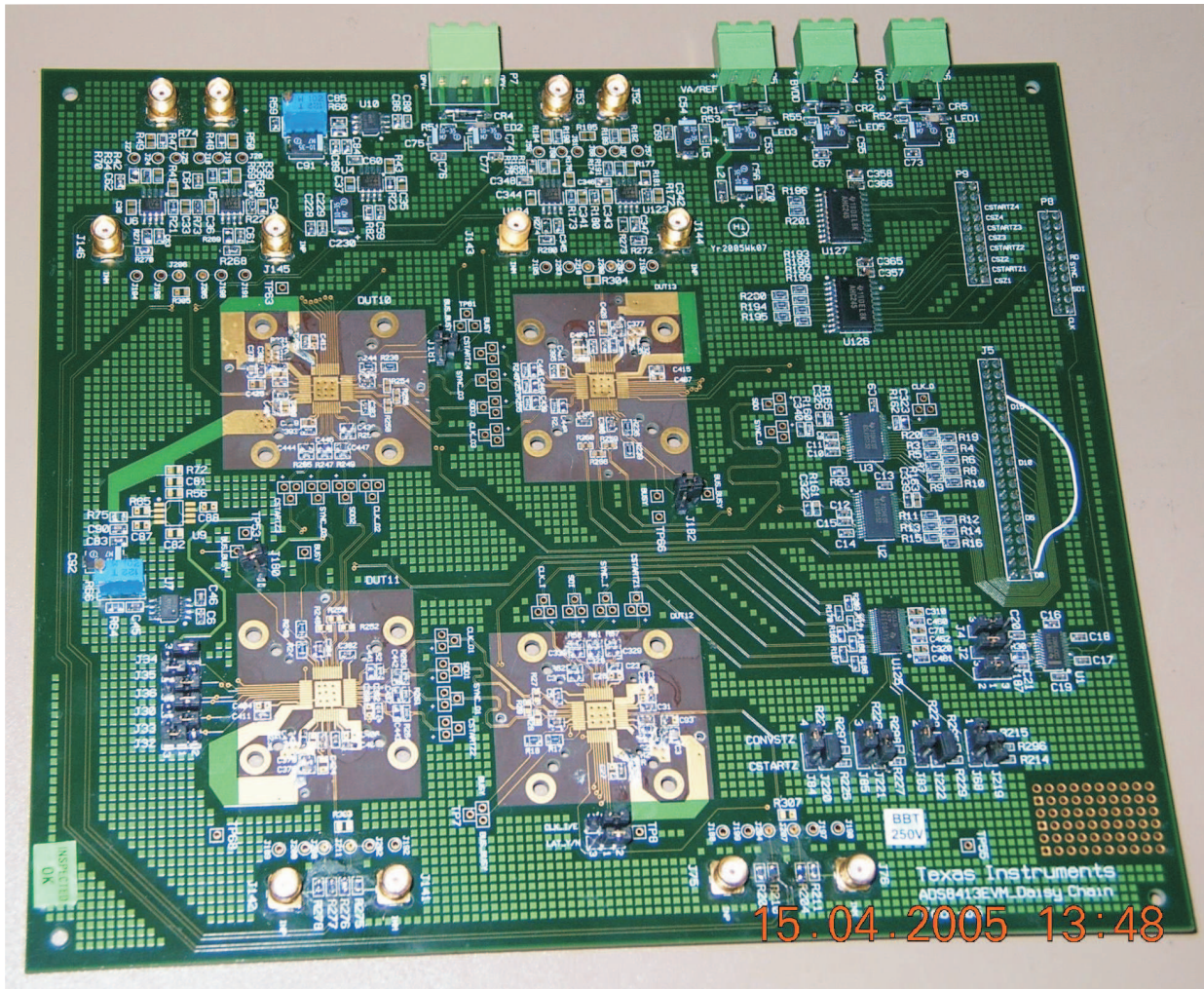
## **A.2 Daisy Chain Board Layout**

The daisy chain board layout is affixed to this page.



Texas Instruments  
ADS8413EVM\_Daisy Chain  
Feb -05

### A.3 Daisy Chain Board Photograph



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Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>

### Applications

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Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
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