

ADS8528, ADS8548, and ADS8568 Timing Considerations

The ADS8528, ADS8548, and ADS8568 are 12-, 14-, and 16-bit, bi-polar input, parallel or serial output analog-to-digital converters (ADC) which have a number of features that allow for easy interface to many of the TMS320 series of Digital Signal Processors (DSP) from Texas Instruments. This application note focuses on some of the specific timing requirements needed to achieve full-speed serial and parallel operation.

1 Introduction

The ADS8528, ADS8548, and ADS8568 devices are eight channel 12-, 14-, and 16-bit ADC, with bipolar inputs. The device features a frame sync/chip select (FS/CS) input, four convert start inputs (CONVST_x) and a user-selectable parallel or serial output. This provides flexible control signals that can interface directly to the C2000, C3000, C5000, and C6000 family of DSPs.

The ADS85x8 operates from 5-V analog core (AVdd) for the conversion process, it uses high voltage rails (HVdd and HVss) of up to ± 12 volts for the input stage, and features a digital input/output buffer rail (DVdd) of 2.7 to 5.5 V for interfacing to a variety of processors.

There are eight independent data converters within the package that operate in channel pairs – A0/1, B0/1, C0/1 and D0/1. The conversion process for each channel pair is controlled by applying the associated convert start input.

2 ADS85x8 Digital Interface

The four CONVST inputs to the ADS85x8 can be controlled independently, providing the user with two simultaneous sampled conversion results. The flexible interface also allows the user to combine all four CONVST input together in order to simultaneously sample up to eight input channels.

2.1 Simultaneous Sampling of Eight Inputs

When combining the four CONVST signals together, a logic high level opens the internal sample and hold switches and starts the conversion process. The BUSY output signal goes high, indicating that the conversion process is underway. As noted in the product data sheet ([SBAS543](#)) the conversion time t_{CONV} is stated as being 19 or 20 conversion clock periods. The conversion clock can be sourced from an internal oscillator (t_{CLK}) or an external clock (t_{XCLK}).

After the CONVST input goes high, the voltage acquired on the sample-and-hold capacitor begins to be converted with the next rising edge of the conversion clock (internal or externally sourced) meeting the minimum setup time of t_{SCVX} , which is 6 ns. [Figure 1](#) depicts the actual start of the conversion process.

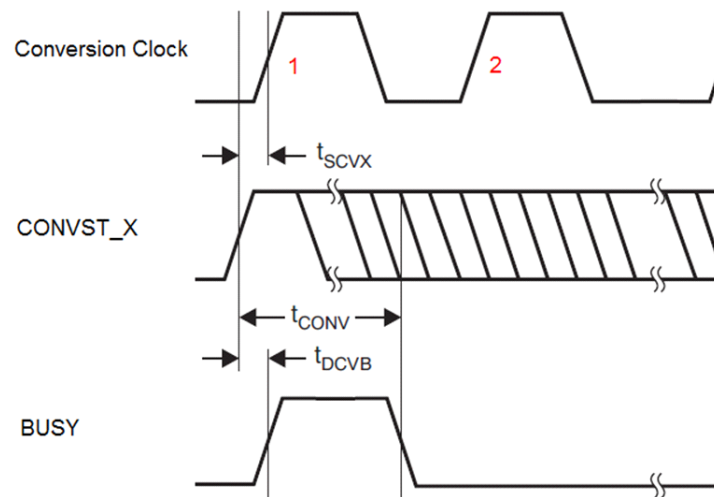


Figure 1. Conversion Timing

CONVST inputs which are applied with the minimum 6 ns setup time (t_{SCVX}) start being converted with the rising edge of clock cycle 1. If the minimum setup time is not met, the conversion process begins with clock cycle 2. This condition is true for either the internal or external conversion clock, which drives the minimum and maximum conversion time of 19 or 20 clock cycles to finish the conversion sequence. If the minimum setup time on conversion clock cycle 1 is not met, the conversion process takes 20 clock cycles to complete. Maximum throughput speed can be achieved by using an external conversion clock with a synchronized CONVST input. CONVST should be configured to go high with the falling edge of the conversion clock to ensure the appropriate setup time is always met.

If the CONVST input cannot be synchronized to the conversion clock, as would be the case when using the internal oscillator, reading of the conversion results should be delayed through the MAXIMUM number of conversion clock cycles to ensure each channel pair has been properly updated.

2.2 Reading Output Data in Serial Mode

When using the ADS85x8 in serial mode, an external serial clock (SCLK) must be applied to pin 21 in order to properly shift data from the output buffer. Care should be taken to ensure that the delay time of the most significant bit (t_{DMSB}) from the falling edge of FS/CS is met before applying the serial clock. This delay is specified as 12 ns MAX. Depending on the processor used to control the ADS85x8, additional setup time for valid data to be strobed to the serial data input channel would need to be added to the MSB output delay (t_{DMSB}) in order to properly interpret the data bit. Typical setup times on a serial peripheral input port are on the order of 3–5 ns.

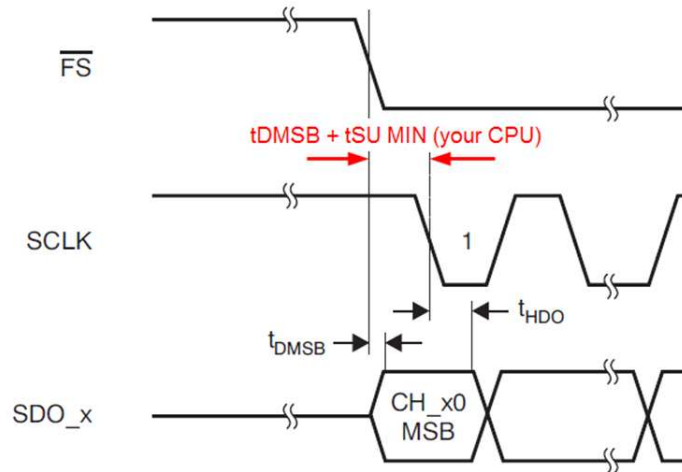


Figure 2. SCLK Delay for Proper Read Operation

Figure 2 depicts the minimum recommended time from the falling edge of FS/CS before applying the SCLK. To ensure proper operation, use the MAXIMUM delay associated with the MSB delay in addition to the MINIMUM time specified in your serial peripheral interface. The SCLK should dwell HIGH during the period when no transfer is taking place and data is to be considered valid on the falling SCLK edge.

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