Application Report
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Extending Input Voltage Range and Understanding Associated Errors for ADC With Integrated Front End

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ABSTRACT

A common input configuration for many analog to digital converters (ADC) uses an internal programmable gain amplifier (PGA) and a resistive attenuator network. This type of converter typically allows several different software configurable input ranges (for example, 0V to 5V, ±5V, and ±10V). These input ranges can be extended to wider input voltages using external resistors. Unfortunately, adding the external resistors will impact gain error, and gain drift. This paper will show how to select external resistor to extend the range, and how to estimate and minimize the errors introduced by the resistors.

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Trademarks

1 Introduction

Some modern data converters include an integrated Analog Front end, or AFE. Frequently, the AFE uses a Programmable Gain Amplifier (PGA) attenuator to reduce the applied voltage to a level that the ADC can read. Figure 1 shows a generic example where the input PGA can be configured to read a ±10.24V input voltage. For this input range the PGA internally attenuates the voltage from 10.24V to 4.096V to allow the internal ADC to read this signal level. The input voltage range can be extended by adding an external resistor. Adding the external resistor introduce a gain error and a gain error temperature drift. This application report will provide equations that estimate the system gain error and drift introduced by adding the series resistor. In the application report we will cover the theory behind the drift calculation as well as some measured results. This application report will develop equations and methods using the generic example. Although the internal values for this topologies will be different for different devices, these equations will apply to most devices in this category. The application report will also provide measured results for the ADS8688 ADC.

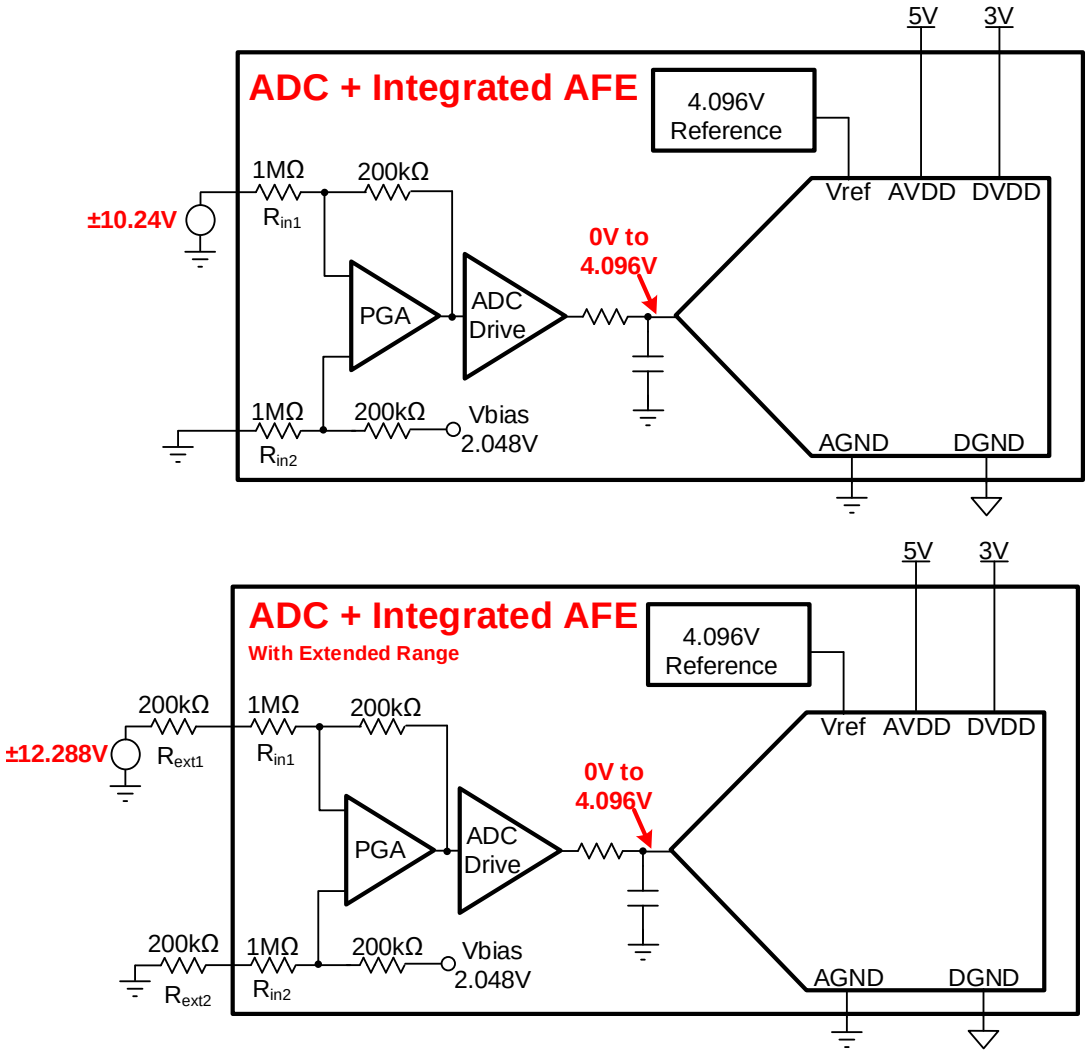


Figure 1. Expanding the Input Range Using an External Resistor

2 Gain Error and Gain Drift

Gain error is the error in the ADC transfer function slope as compared to the ideal slope. The slope can be calculated using any two points on the transfer function (see Equation 1). Gain error is calculated using Equation 2. Gain error drift measures how gain error changes over temperature (see Equation 3). Normally gain error is given in parts per million per degree Celsius (ppm/°C). This application report will explain gain error and gain drift with and without the external extended range resistor.

Measured Slope:

$$Slope_m = \frac{\Delta Code}{\Delta V_{in}} = \frac{Code_2 - Code_1}{V_{in2} - V_{in1}}$$

Where

$Code_1$ and $Code_2$ = are two output codes that corespond to V_{in1} and V_{in2}

V_{in1} and V_{in2} = are the input voltages. Choose voltages near zero and full scale, but in the linear range. (1)

Gain Error:

$$GE = \frac{(Slope_m - Slope_i)}{Slope_i}$$

Where

GE = Gain error. Multiply by 100 for percent, or 10^6 for ppm.

$Slope_m$ = measured slope

$Slope_i$ = ideal slope (2)

Gain Drift:

$$\frac{\Delta GE}{\Delta T} = \frac{GE_{High} - GE_{Low}}{T_{High} - T_{Low}} \cdot 10^6$$

Where

$\frac{\Delta GE}{\Delta T}$ = gain error drift in ppm/°C

GE_{High} and GE_{Low} = gain error tested at high and low temperatures

T_{High} and T_{Low} = High and low temperature (3)

2.1 Gain Error and Drift Without an Extended Range Resistor (R_{ext})

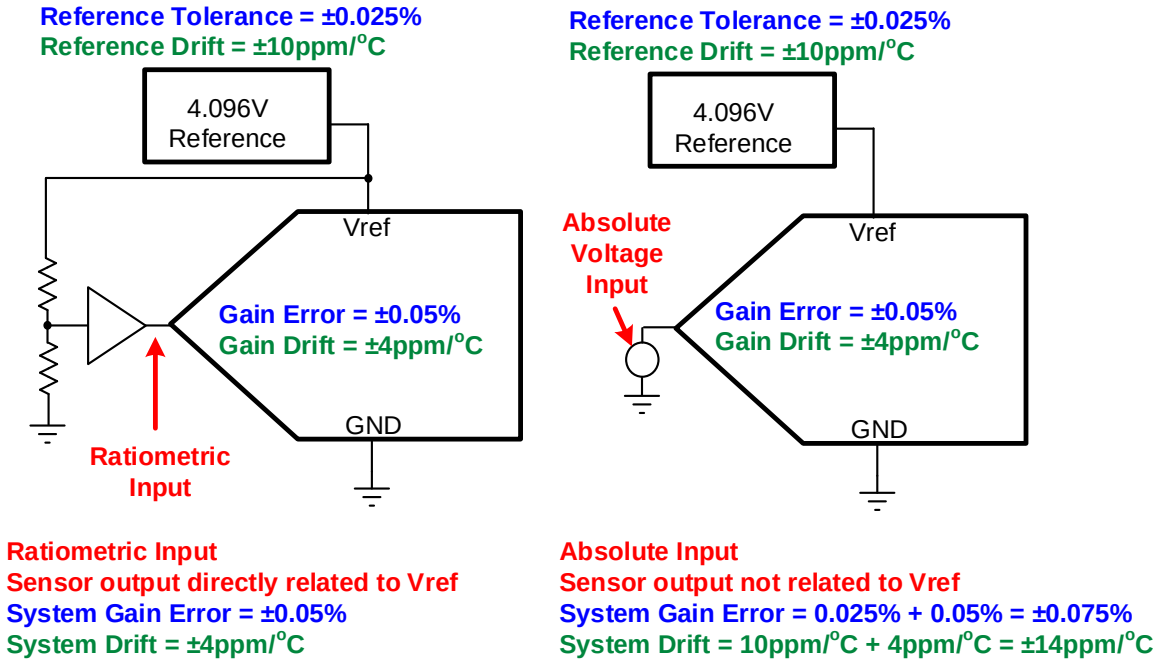
The input of the ADC with an integrated AFE is attenuated by the op amp resistor feedback network. This network is built internally using Silicon chromium (SiCr), resistors. Resistors on any given device are all fabricated at the same time, so the properties of these resistors closely match each other. Thus the resistance matching and temperature coefficient matching of resistors on any given devices match very well. Since the resistance matches across the die, the ratio of two different resistors will be very accurate. Gain error is set by resistor ratios, so gain error for these types of devices is very precise. For example, the ADS8688 gain error specification is ±0.05% maximum. On the other hand, the absolute resistance value or resistance temperature coefficient for SiCr resistors across different wafer fabrication lots will vary more than on a given device. For example the absolute resistance tolerance for a SiCr resistor is ±15%, and the absolute temperature coefficient is ±25ppm/°C. The absolute resistance and temperature coefficient are only important when external impedances are connected to the input as is covered in the next section.

Table 1. Absolute and Relative Errors and Drift for Typical ADC + Integrated AFE

	Internal ADC Resistance Maximum Error	Internal ADC Resistance Maximum Temperature Coefficient
Absolute	±15%	±25ppm/°C
Relative (matching)	±0.05%	±4ppm/°C

2.2 Effect of Reference on Drift

The reference initial accuracy and drift will inversely impact the system gain error drift of the ADC. For example, if the reference voltage has a +1% error this will introduce a -1% error in gain error. To estimate the worst case system gain error and drift for an ADC you can directly add the reference errors to the system error. One way to eliminate this error would be to use the reference in a ratiometric operation. In ratiometric operation, the ADC reference is also used for the excitation of the sensor being measured. In this case, when the reference drifts the sensor output and ADC gain error will track and cancel. Figure 2 compares the absolute and ratiometric input and the associated system drift calculation. The figure shows how the reference tolerance (shown in blue) and reference drift (shown in green) add to the ADC error for the absolute input case, and these errors cancel for the ratiometric case. The reminder of this paper will consider the absolute (non-ratiometric) input case in all error analysis.



Ratiometric Input
Sensor output directly related to Vref
System Gain Error = ±0.05%
System Drift = ±4ppm/°C

Absolute Input
Sensor output not related to Vref
System Gain Error = 0.025% + 0.05% = ±0.075%
System Drift = 10ppm/°C + 4ppm/°C = ±14ppm/°C

Figure 2. System Gain Drift for Ratiometric vs Absolute Reference

2.3 Extending the Input Range With R_{ext}

Placing a resistor in series with the ADC input will increase the voltage range for the ADC. The extended range can be calculated using the voltage divider equation (see Equation 4). This equation is used in an example where the ADS8688 input range is expanded from ±10.24V to ±12.288V (see Equation 5). Equation 6 shows the same relationship algebraically rearranged to solve for R_{ext}, and an example calculation for a 20.48V range is given.

$$V_{ExtRange} = V_{range} \cdot \frac{R_{ext} + R_{in}}{R_{in}}$$

Where

$V_{ExtRange}$ = extended range with external resistor

V_{range} = ADC specified range

R_{ext} = external resistor to increase range

R_{in} = input resistance on PGA input (typically 1MΩ) (4)

Example: Extended Range for R_{ext} = 200kΩ

$$V_{ExtRamge} = 10.24V \cdot \frac{200k\Omega + 1M\Omega}{1M\Omega} = 12.288V \quad (5)$$

Example: Solve for Rext to set extended range to 20.48V

$$R_{ext} = R_{int} \cdot \frac{\left(V_{ExtRange} - V_{range}\right)}{V_{range}}$$

$$R_{ext} = 1M\Omega \cdot \frac{\left(20.48V - 10.24\text{V}\right)}{10.24\text{V}} = 1M\Omega \quad (6)$$

2.4 Gain Error With an Extended Range Resistor

Connecting an external resistance can be used to extend the input voltage range to allow for a wider input voltage. The gain error is set by the tolerance of the internal and external resistors. As mentioned in Section 2.1, a common absolute tolerance of the internal resistor is ±15%. A common tolerance for the external resistor is 1% or 0.1%, which is substantially smaller than the internal tolerance, so generally the internal resistor tolerance will be the dominant factor in a gain error calculation. Equation 7 can be used to calculate the system gain error given the external resistance value, internal resistance, and tolerance of the internal resistor. Note that the tolerance of the external resistor is not included in this equation as this error is typically small (e.g. 0.1%).

The graph shown in Figure 3 shows the worst case system gain error for a wide range of external resistors as well as one measured example. This graph was generated using Equation 7. You can see that for large external resistors (i.e. R_{ext} > 10MΩ) the gain error converges to the internal resistor tolerance (15%). For small external resistors (R_{ext} < 10kΩ) the gain error is relatively low (0.1%). For this reason, it is generally required to calibrate the gain error when external resistors greater than 10kΩ are used.

$$TOL = \frac{PercentError}{100} + 1$$

$$GE_{System(\%)} \approx \left(\frac{TOL \cdot (R_{in} + R_{ext})}{TOL \cdot R_{in} + R_{ext}} - 1 \right) \cdot 100$$

Where

$GE_{System(\%)}$ = The gain error of the ADC + Rext.

Percent Error = The maximum error of the internal resistor (typically 15%)

TOL = The tolerance factor for the internal resistor (typically = 1.15)

R_{in} = The internal resistance (typically 1MΩ)

R_{ext} = The external resistance used to adjust the voltage range. This value depends on the range requirement. (e.g. 10kΩ to 10MΩ) (7)

Example: Worst Case System Gain Error for R_{ext} = 1MΩ

$$TOL = \frac{15\%}{100} + 1 = 1.15$$

$$GE_{System(\%)} = \left(\frac{1.15 \cdot (1M\Omega + 200k\Omega)}{1.15 \cdot 1M\Omega + 200k\Omega} - 1 \right) \cdot 100 = 2.2\% \quad (8)$$

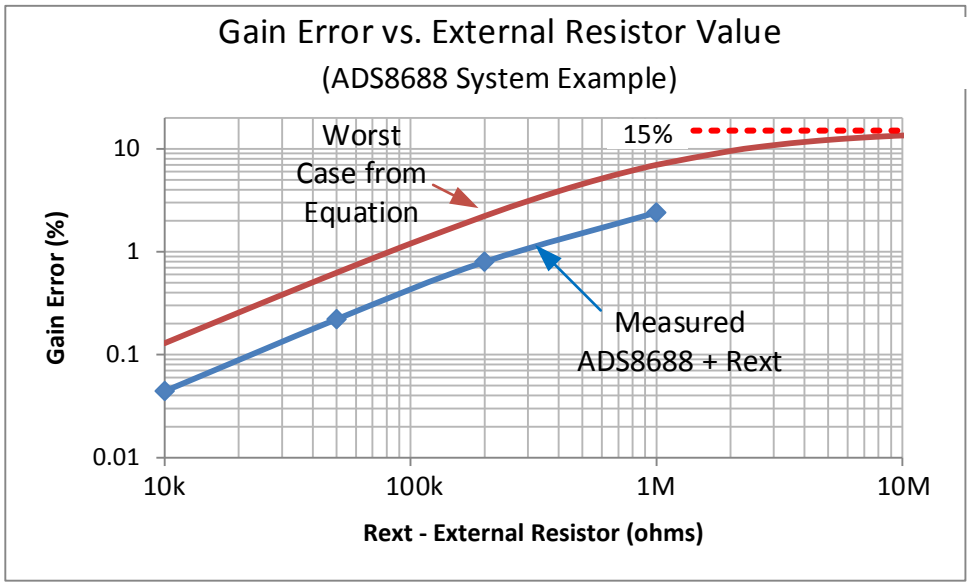


Figure 3. Maximum System Gain Error for a Range of External Resistors

2.5 Gain Error Drift With R_{ext}

In cases where an external resistor is added to expand the input range, the temperature coefficients of the internal and external resistors no longer match and do not cancel anymore. Equation 9 shows the system gain error drift relationship including the reference drift, internal gain error, and external temperature coefficient. This equation and worst case values for the ADS8688 are graphed in Figure 4. The figure illustrates that for small values of external resistance ($R_{ext} \leq 10k\Omega$), the reference drift and ADC gain drift are dominant and the external resistor has little effect on drift. For larger values of external resistance ($R_{ext} > 10k\Omega$), the system gain error is a combination of all the drift sources. Notice that the graph is given for two different temperature coefficients of external resistors (25ppm/°C and 100ppm/°C). As shown by the graph, a 25ppm/°C resistor or better is required for lowest drift.

$$\frac{GE_{SYSTEM}}{\Delta T} \approx -\frac{R_{ext}}{R_{ext}+R_{in}}TC_{ext} + \left(1-\frac{R_{in}}{R_{ext}+R_{in}}\right)TC_{int} + \frac{GE_{ADC}}{\Delta T} - \frac{Ref}{\Delta T} \quad (9)$$

Where

TC_{ext} = temperature coefficient of external resistor

TC_{int} = temperature coefficient of internal resistor. Typically ±25ppm/°C for SiCr resistors.

$\frac{GE_{ADC}}{\Delta T}$ = gain drift of the ADC not including the effects of the reference.

Typically very low $\left(\pm 4ppm/^{o}C \text{ for the ADS8688}\right)$.

$\frac{Ref}{\Delta T}$ = External resistance used to increase the system input voltage range.

R_{ext} = External resistance used to increase the system input voltage range.

R_{in} = Internal input resistance of the PGA gain network. Typically a 1MΩ resistor used to attenuate the input signal to match the internal ADC range.

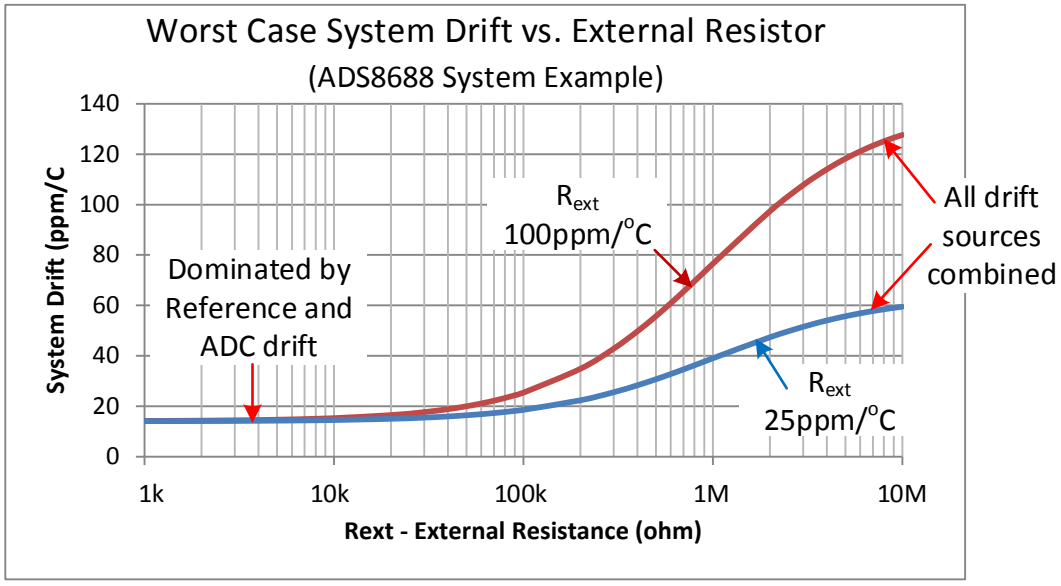


Figure 4. Worst Case Drift vs External Resistor

2.6 Measured Gain Error Drift vs R_{ext} and R_{ext} Temperature Coefficient

Figure 5 shows measured results for the ADS8688 with sample of twelve 200kΩ and twelve 1MΩ external resistors. The temperature coefficient specification for the resistors used was ±100ppm/°C. Notice that for this sample, the external resistor temperature coefficient ranged from 5ppm/°C to 60ppm/°C, but in for a larger sample size the actual drift could be as large as the specified ±100ppm/°C drift. Finding the best-fit straight line equation for the measured data, shows that the measured slope matches the expected slope from Equation 9. For example, the 200kΩ external resistor has an expected slope of -0.167 and a measured slope of -0.158 (expected slope = $-R_{ext}/(R_{ext} + R_{in})$ = -200k/(200kΩ+1MΩ) = -0.167). Figure 5 also reinforces the importance of using low TC external resistors to minimize total system drift. Notice that for this sample set the largest measured drift is significantly less than the theoretical worst case from Figure 4 (largest measured = 27ppm/°C, worst case for 1MΩ 100ppm/°C resistor = 77ppm/°C). One reason for this difference is that the sample size is relatively small, and in a larger sample we would come closer to the worst case limits given in Figure 4. Also, the worst case curve was generated by assuming that the sign and magnitude of all the drift components are simultaneously at worst case values. In reality, it is statistically unlikely that all the drift components will be at worst case simultaneously. Thus, the worst case given in Figure 4 is conservative. For more information covering the statistics of error analysis see Statistics Behind Error Analysis.

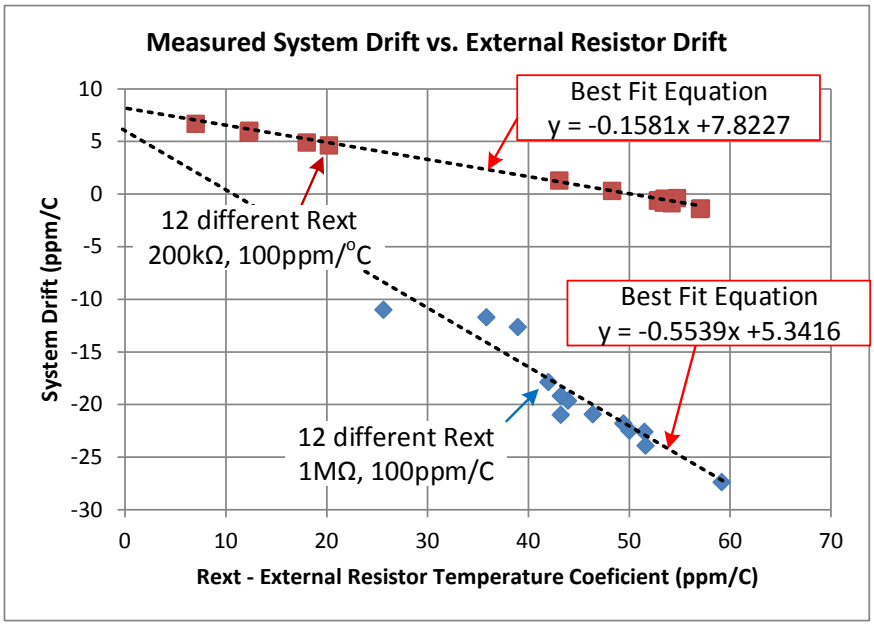


Figure 5. Measured System Drift vs External Resistor for the ADS8688

3 Offset Error and Offset Drift

This application report has focused on the effects external resistors have on gain drift. System offset and offset drift are also important error sources to consider. Fortunately, the external resistor has a relatively small effect on offset and offset drift. This section will step through an example of how external resistors effect offset and offset drift. Depending on the device selected or input range selected the internal scaling will be different. Nevertheless, the conclusion drawn here will apply to all devices with this type integrated PGA input.

The circuit shown in Figure 6 is a single ended ADC. The input signal is applied to the top resistor on the PGA (R_{ext1}), and the bottom resistor (R_{ext2}) is used to sense ground. R_{ext1} impacts gain error and gain drift, and R_{ext2} impacts offset error and offset drift. In this example, the network on the bottom of the PGA is designed to set the output of the PGA to midscale (2.048V) when 0V is applied to the input. Deviation from this midscale point is the ADC offset. Drift in the external resistor R_{ext2} will cause a drift in offset. In this calculation, a drift for R_{ext2} of 100ppm/°C over a 100°C temperature span is used for a worst case example. At 25°C, all the system components are ideal and the output is the expected 2.048V. At 125C, the external resistor R_{ext2} has drifted to 202kΩ so the output of the PGA drifts to 2.0485V. This drift corresponds to a 1.2ppm/°C drift in the offset. If the same example is calculated for a 20ppm/°C resistor the system drift will be 0.24ppm/°C (see Equation 10). Of course, depending on the ADC input network, ADC range, and external resistor value used the result will be different. The point is that for a worst case example the offset drift introduced is relatively small. By comparison, the offset drift specification for the ADS8688 is ±3ppm/°C. Figure 7 shows measured offset drift for a device with three different external resistors. The measured drift with the external resistor is significantly better than the device drift specification (±3ppm/°C) which agrees well with the assertion that the external resistor will have little impact on offset and offset drift.

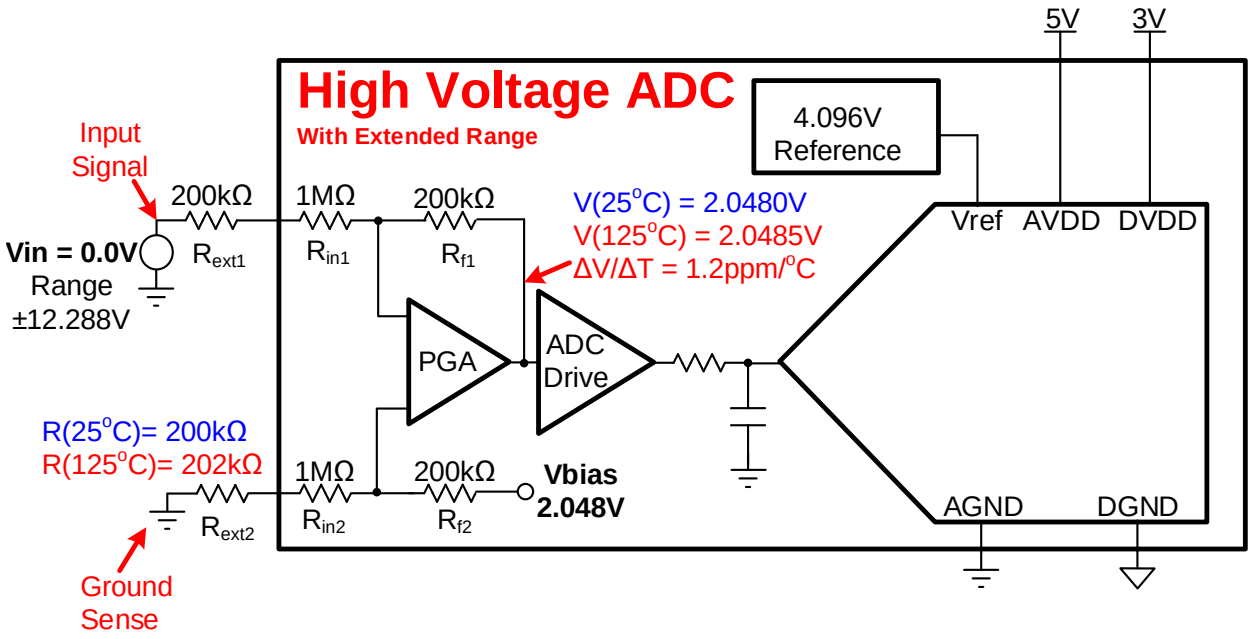


Figure 6. Offset Temperature Drift With an External Resistor

$$V_{PGA} = \left(\frac{R_{f1}}{R_{in1}+R_{ext1}}+1\right)\left(\frac{R_{in2}+R_{ext2}}{R_{f2}+R_{in2}+R_{ext2}}\right)V_{bias}$$

$$R_{ext2}(T) = \left(Drift\cdot(T-25°C)+1\right)R_{ext2}$$

$$V_{PGA}(T) = \left(\frac{R_{f1}}{R_{in1}+R_{ext1}}+1\right)\left(\frac{R_{in2}+R_{ext2}(T)}{R_{f2}+R_{in2}+R_{ext2}(T)}\right)V_{bias}$$

$$SystemDrift = \frac{V_{PGA}(125°C)-V_{PGA}(25°C)}{V_{FullScale}\cdot\Delta T} = \frac{2.0480V-2.0485V}{4.096V\cdot(125°C-25°C)} = 1.2ppm/°C \quad (10)$$

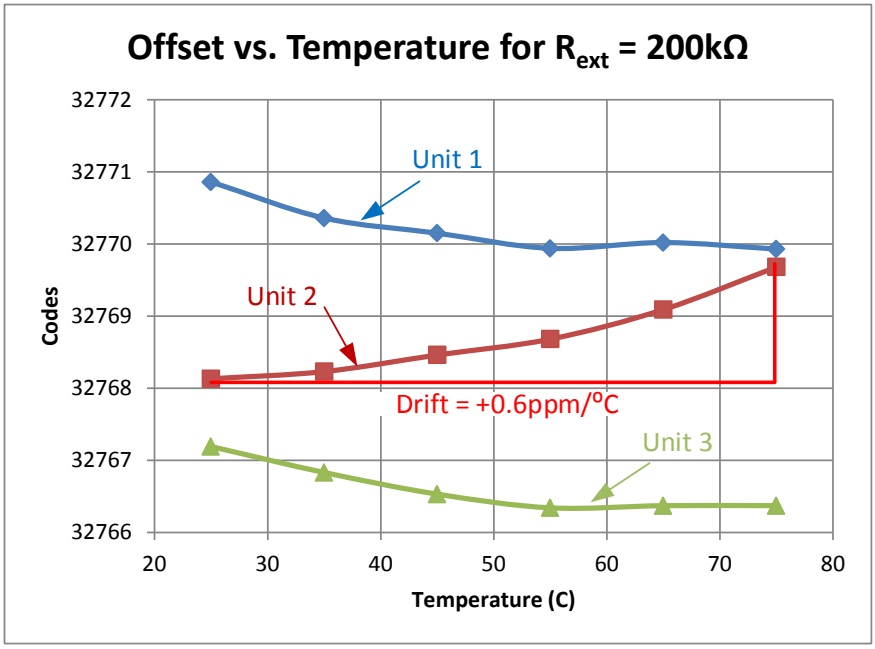


Figure 7. Measured Graph of Offset Drift With R_{ext} = 200 kΩ

4 Linearity of Errors Over Temperature

Figure 5 illustrates the measured relationship between the system drift and the external resistor value and temperature coefficient. The temperature data for Figure 5 was collected at 25°C and 60°C. Different applications require different temperature ranges, so it is natural to question if this relationship is the same for different temperature ranges. The purpose of this section is to show that the dominant drift terms are linear, so the overall gain drift in ppm/°C should be approximately the same regardless of the operating temperature range. Remember from Equation 9 that the system drift is related to the external resistor drift, internal resistor drift, ADC drift, and reference drift. The temperature drift of the internal and external resistors is linear, whereas the reference drift and ADC drift may be non-linear. For large external resistances the resistor drifts will dominate so the overall drift will be linear. Figure 8 shows the system gain drift across temperature for three different external resistors. Notice that the system gain drift is fairly linear. Thus the system gain drift in ppm/°C is approximately the same regardless of the operating temperature range. Figure 9 shows the that the change in resistance of typical metal film resistors is linear over temperature. Figure 10 shows that internal resistance change over temperature is fairly linear but does have some small nonlinearity. Figure 11 shows that the reference and ADC gain error drift may be nonlinear.

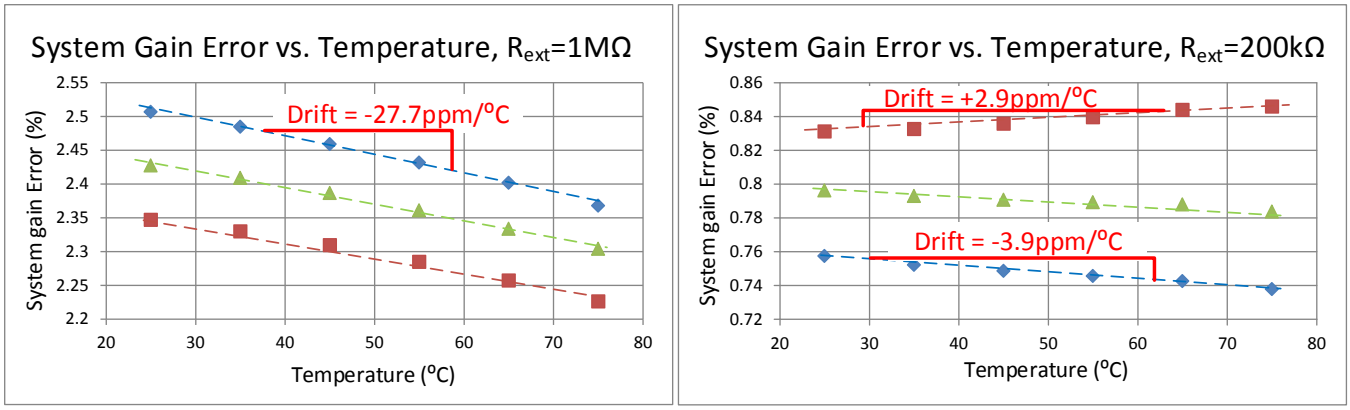


Figure 8. System Gain Error vs Temperature

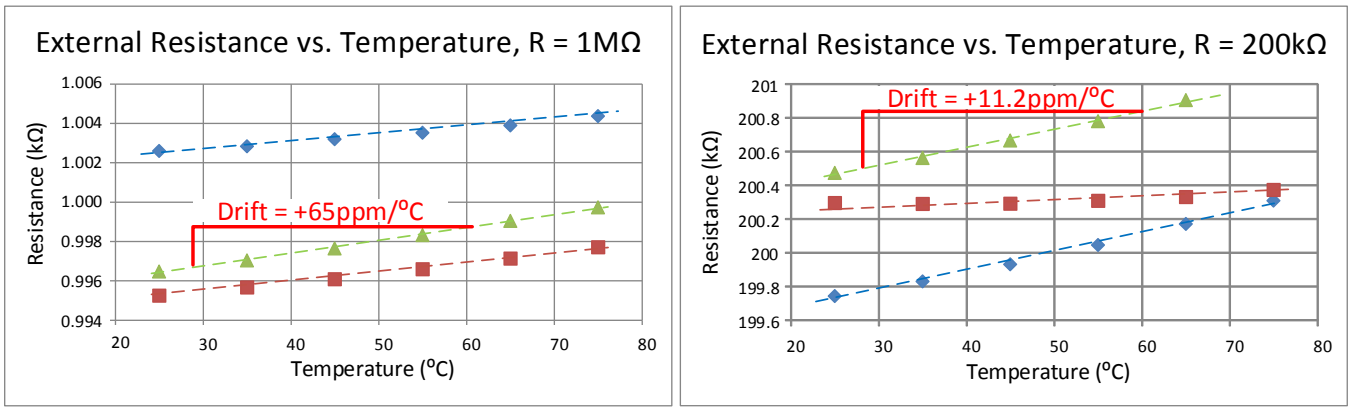


Figure 9. External Resistance vs Temperature

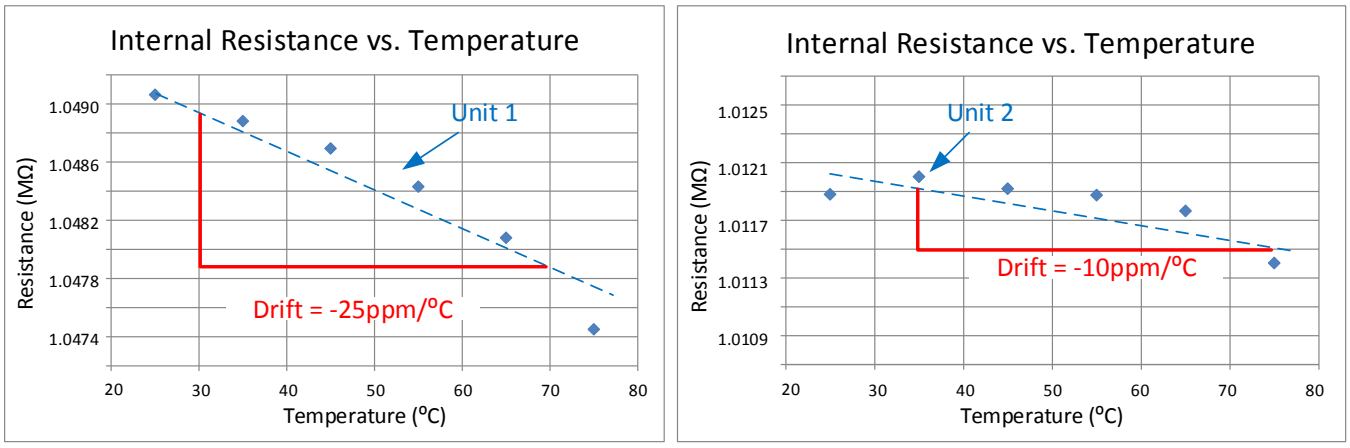


Figure 10. Internal Resistance (R_{in}) Drift

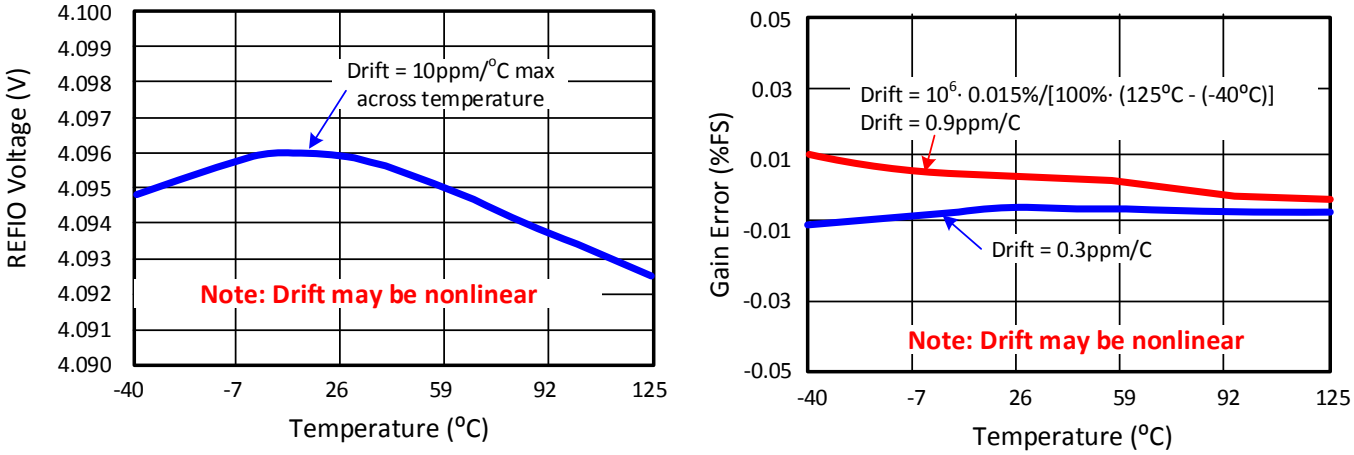


Figure 11. Reference and ADC Drift Shows Nonlinearity

5 Summary

This application report applies to a class of data converters with an Integrate Analog Front End (AFE) as shown in Figure 1. For this type of AFE the input voltage range can be expanded using external resistors. The goal of this report is to estimate the impact that external resistors have on gain error, offset error, gain drift, and offset drift. Also, understanding this relationship helps in the selection of components to minimize this error. Section 3 of the report shows that both offset and offset drift are not substantially impacted by the external resistance selection. Section 2.4 shows that values of external resistance greater than 10kΩ can introduce significant gain error (0.1% <Gain error< 15%, see Figure 4). Since the gain error is significant, it is common to calibrate the system (see Understanding and Calibrating the Offset and Gain for ADC Systems for an overview of calibration methods). Section 2.5 shows that the system drift is directly impacted by the drift of the external resistor (see Figure 4). For this reason, it is recommended to use low drift resistors (TC < 25ppm/°C) to minimize system drift.

6 References

- Texas Instruments, *Reducing Effects of External RC Filter on Gain and Drift Error for Integrated AFE* application report
- Texas Instruments, *Circuit to Increase Input Range on an Integrated Analog Front End (AFE)* application report

Table 2. Suggested Devices With an Integrated AFE

Device	Key Features	Link	Other Devices
ADS8688	16-Bit ADC with Integrated Analog Front-End, 8-Channel MUX, Programmable Input Ranges, Bipolar: ±10.24 V, ±5.12 V, and ±2.56 V, Unipolar: 10.24 V, 5.12 V, Constant Resistive Input Impedance: 1 MΩ, Input Overvoltage Protection: Up to ±20 V, On-Chip, 4.096-V Reference with Low Drift	http://www.ti.com/product/ADS8688	www.ti.com/adcs
ADS8588S	16-Bit ADC with Integrated Analog Front-End, Simultaneous Sampling: 8-Channels, Pin-Programmable Bipolar Inputs: ±10 V and ±5 V, High Input Impedance: 1 MΩ, Low-Drift, On-Chip Reference (2.5 V) and Buffer	http://www.ti.com/product/ADS8588S	www.ti.com/adcs
ADS8681	16-Bit ADC with Integrated Analog Front-End, Programmable Input Ranges, Bipolar: ±12.288 V, ±10.24 V, ±5.12 V, and ±2.56 V, Unipolar: 12.288 V, 10.24 V, 5.12 V, Constant Resistive Input Impedance: 1 MΩ, Input Overvoltage Protection: Up to ±20 V, On-Chip, 4.096-V Reference with Low Drift	http://www.ti.com/product/ADS8681	www.ti.com/adcs

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