Voltage-reference impact on total harmonic distortion

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Understanding the load presented by the reference pin of SAR ADCs is key when designing data-acquisition systems with low harmonic distortion.

The internal circuitry connected to the reference pin of most successive-approximation-register analog-to-digital converters (SAR ADCs) (and some wideband delta-sigma ADCs) consists of switched-capacitor loads. During the conversion process, a switched-capacitor load imposes a current demand that can cause the external system's reference-output voltage to fluctuate in time. Consequently, the SAR ADC reference-pin voltage also fluctuates.

Since the amount of switched-capacitor load depends on the input signal to the ADC, the amount of voltage-reference change also depends on that input signal. The phenomenon of voltage-reference fluctuation can directly translate into degradation of the system's total harmonic distortion (THD). Excessive voltage-reference fluctuations can completely run the otherwise stellar performance of a high-performance measurement-system ADC into the ground. It does not matter if the application is a motor-drive controller, a power-quality monitor or a medical instrument: All of the engineering effort that the system architect dedicated to choosing the proper ADC and synthesizing the optimal input-driver circuitry essentially goes to waste if the voltage on the reference fluctuates excessively.

In this white paper, I will explain how the voltage reference affects the THD of an 18-bit acquisition system and how adequate buffer circuitry solves the THD degradation problem. System architects and board-level designers can then effectively tackle the challenge of creating data-acquisition systems capable of achieving a high signal-to-noise ratio (SNR) while maintaining low distortion.

Data-acquisition system

Figure 1 shows a simplified schematic of a data-acquisition system based on a SAR ADC. The voltage reference provides a necessary level to perform conversions. The buffer circuitry may or may not be necessary depending on the characteristics of the ADC, the reference itself and the maximum acceptable level of harmonic distortion. The microcontroller provides both a clock and control signals to the ADC, and reads conversion results from the ADC communication bus.

Equation 1 shows the transfer function of an ideal SAR ADC with a true differential input range. The transfer function is ideal because it does not take into consideration offset error, gain error, nonlinearity or intrinsic semiconductor noise.

$$\text{Codeword}_{OUT} = \text{floor}\left[V_{IN}\left(\frac{2^N}{2V_{REF}}\right)\right] \quad (1)$$

where V_{IN} is the analog input to the data converter, N is the data-converter resolution and V_{REF} is the voltage difference between the data-converter reference pins.

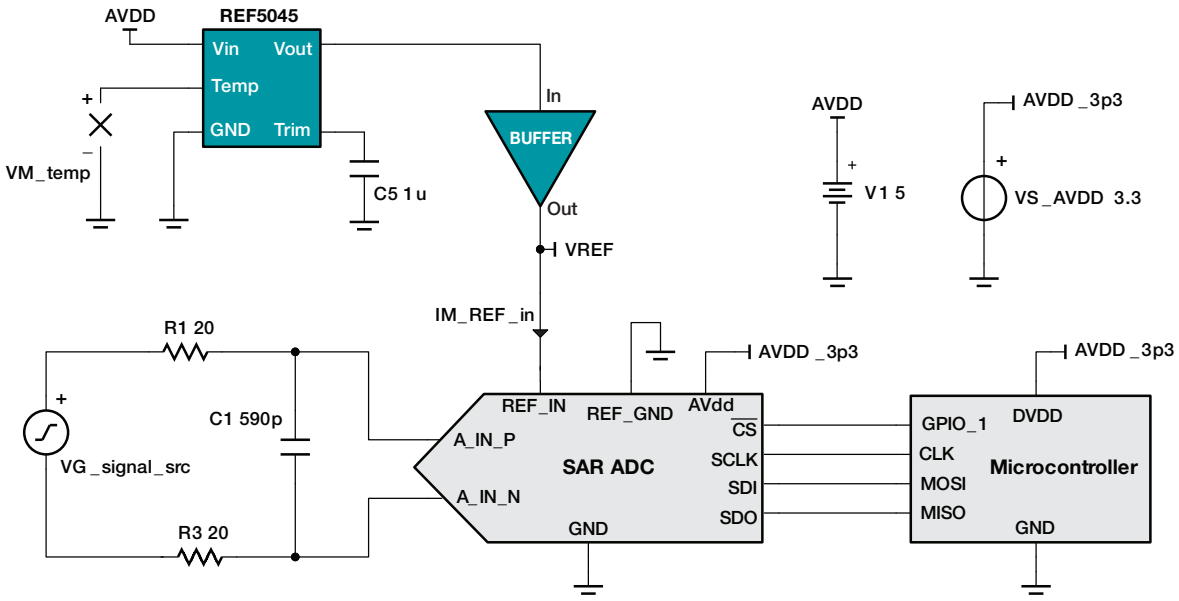

Figure 1. *Simplified schematic of a data-acquisition system based on a SAR ADC.*

The floor(·) function, also known as the integral part function, provides the largest integer no greater than its argument.

The floor(·) function in **Equation 1** represents the quantization process performed by the SAR ADC. Therefore, **Equation 1** takes into account quantization error introduced by the ADC.

How ADC output errors degrade THD

Equation 2 shows the output of a data-acquisition system similar to the one depicted in **Figure 1**, but with a key difference from **Equation 1**: the inclusion of an error term. Note that the error term could be caused by nonidealities internal to the ADC, or by nonidealities in the voltage reference and its associated buffer.

It is also possible for the buffer at the input of the SAR ADC to cause the error term in **Equation 2**; however, in this paper I only account for the effect of the voltage reference and its associated circuitry. The assumption throughout will be that the ADC input buffer provides an exact replica of the input signal, with no added distortion and no added noise.

$$\text{Codeword}_{\text{OUT}} = \text{floor}\left[v_{\text{IN}}\left(\frac{2^{N}}{2V_{\text{REF}}}\right) + \text{error}\right] \quad (2)$$

where V_{IN} is the analog input to the data converter, N is the data-converter resolution, V_{REF} is the voltage difference between the data-converter reference pins, and error is the term that accounts for all possible code errors caused by the ADC or other elements in the system.

Regardless of the error source, not every error term causes harmonic distortion in an acquisition system. For example, if the error term is constant with respect to time, then the output of the acquisition system has only a DC offset.

Figure 2 shows what goes on in the response of the data-acquisition system for a DC error case. The transfer function of the system is shown on the left side of **Figure 2**, the time-domain signals are in the center, and the frequency domain plot is on the right side. The blue traces correspond to **Equation 1** (an ideal system with no error), and the red traces correspond to **Equation 2** when the error term does not depend on time.

On the frequency-domain plot, both traces line up exactly, and the only feature visible in the red trace is its DC error. The rest of the red trace is occluded by the blue trace.

Since the transfer function of the whole system remains linear, a sinusoidal input comes out as a sinusoidal output, but with a DC offset and quantization error. Consequently, there is no harmonic distortion associated with error terms that are constant with respect to time.

The transfer functions shown in **Equation 2** and **Figure 2** are those of the entire data-acquisition system; they include the effect of the voltage reference, ADC and other system components. See reference [1] for more about quantization error.

Error terms that are directly proportional to the input signal constitute another example of error terms that do not cause distortion on the system output. **Equation 3** and **Figure 3** show how the system transfer function and output change when K_1 is a constant with respect to time.

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2V_{REF}}\right) + K_1 v_{IN}(t)\right] \quad (3)$$

where $V_{IN}(t)$ is the analog input to the data converter, N is the data-converter resolution, V_{REF} is the voltage difference between the data-converter reference pins, and K_1 is a constant with respect to time.

As **Figure 3** shows, the transfer function of the system is also linear in the case expressed via **Equation 3**. For the transfer function in **Equation 3**, a sinusoidal input comes out of the system as a sinusoidal, but with a higher (or lower) peak amplitude and with quantization error.

In **Figure 3**, note the absence of significant signals at any frequency not corresponding to the fundamental input sinusoidal. In a fast Fourier transform (FFT) plot, the lack of signals other than the fundamental shows the absence of harmonic distortion. Consequently, there is no harmonic distortion associated with error terms directly proportional to the input signal.

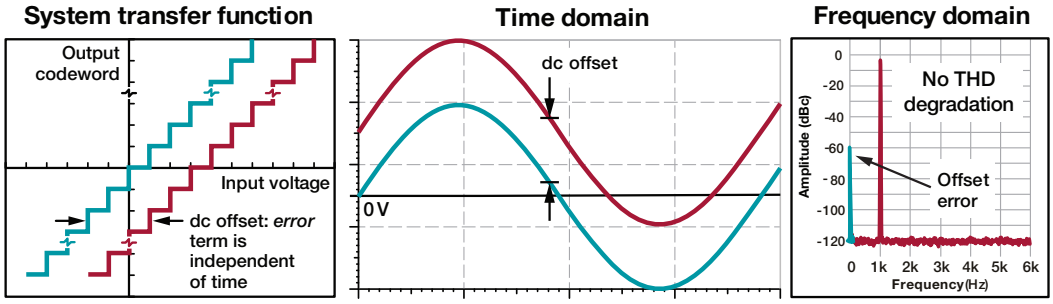

Figure 2. *Output of a system with DC error.*

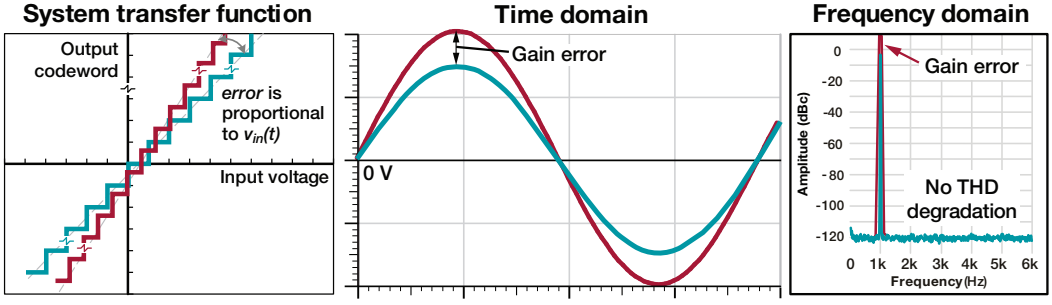

Figure 3. *Output of a system with gain error.*

Errors that are nonlinear functions of the input signal introduce harmonic distortion in a data-acquisition system. **Equation 4** expresses this phenomenon.

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2V_{REF}}\right) + f_2(v_{IN}(t))\right] \quad (4)$$

where $V_{IN}(t)$ is the analog input to the data converter, N is the data-converter resolution, V_{REF} is the voltage difference between the data converter reference pins, and f_2 is a nonlinear function of $V_{IN}(t)$.

Figure 4 shows the result of an error term whose dependency on the input signal is nonlinear. The transfer function of the overall system is no longer linear in **Figure 4**; harmonic distortion is therefore present at the output of the data-acquisition system. Harmonics at 2 kHz, 3 kHz, 4 kHz and 5 kHz indicate harmonic distortion in the system.

Three approaches for supplying the ADC reference

Armed with an intuitive understanding of which types of error influence harmonic distortion, you can proceed to study the specific effects of the voltage reference on an acquisition system.

The analysis begins with **Equation 1**. An idealized ADC model is necessary because the objective is to understand the effect that voltage references (and their associated buffering and conditioning circuits) have on data-converter performance.

Using the ideal ADC model from **Equation 1** ensures that offset error, gain error, ADC nonlinearity or intrinsic semiconductor noise are not causing performance degradation.

Of course, in a real data converter with nonidealities and possessing internal parasitic elements plus intrinsic noise, all of the factors that I mentioned above will play a role in overall system performance. In this paper, however, I will consider only linear, noiseless ADCs.

Causes of reference-voltage fluctuations: internal structure of SAR ADCs

The internal circuitry connected to a SAR ADC's reference and analog input pins will differ depending on the exact architecture of the device. Describing the exact topology of such internal circuitry is outside the scope of this paper. See references [2] and [3] for more details on specific charge-redistribution schemes used in SAR ADCs.

Figure 5 shows a simplified circuit for modeling the behavior of the reference input pin of some SAR ADCs The model in **Figure 5** is general and suitable for analyzing the performance of SAR-based systems because, regardless of the charge-redistribution architecture, one fact remains common to most SAR ADCs: the internal capacitor bank connected to the reference pin has a capacitance dependent on the input signal. As a result, the current sunk on the reference pin also depends on the input signal.

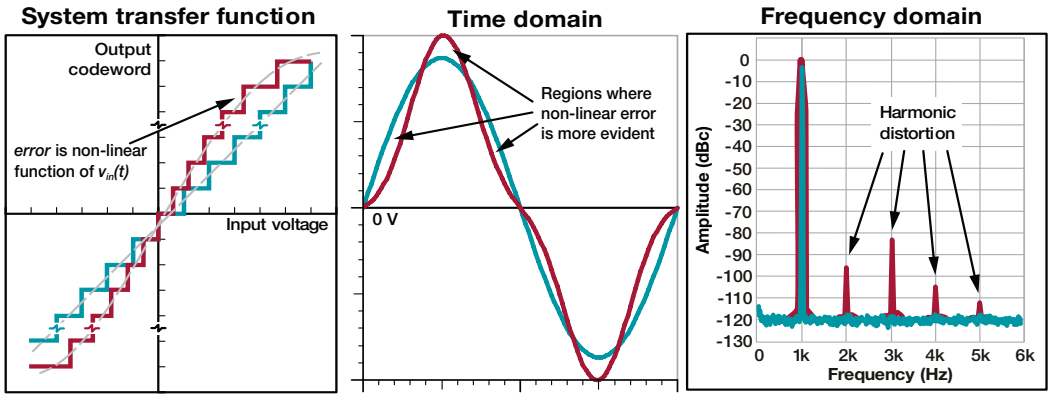

***Figure 4**. Output of a system with nonlinearities.*

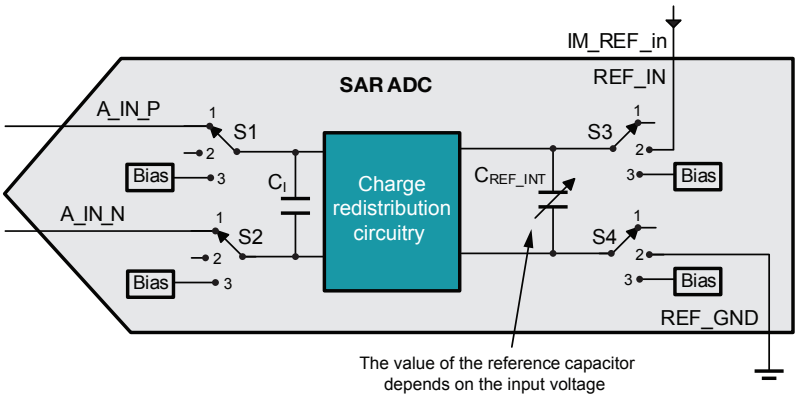

Figure 5. Simplified model of a SAR ADC.

There are two major time intervals in the operation of the SAR ADC: acquisition and conversion. During the acquisition time, all switches in **Figure 5** are in position 1; therefore, switches S1 and S2 connect the sampling capacitor CI to the analog input pins A_IN_P and A_IN_N, while the reference capacitor C_{REF_INT} is isolated from the REF_IN and REF_GND pins.

During the conversion time, all switches in **Figure 5** are in position 2. Switches S1 and S2 disconnect the sampling capacitor from the analog input pins, while S3 and S4 connect the reference capacitor C_{REF_INT} to the REF_IN and REF_GND pins.

Finally, toward the end of the conversion period (for a short time before the beginning of the next acquisition period), S1, S2, S3 and S4 move to position 3 and reset the voltages of the sampling and reference capacitors to an internal bias point. At the beginning of the subsequent acquisition cycle, all switches return to position 1 and the process repeats.

In a theoretical acquisition system, the V_{REF} term in **Equation 1** (corresponding to the voltage given to the reference capacitor C_{REF_INT}) would be a constant regardless of the input signal to the data converter. Appendix B discusses such an ideal system.

In a real system like the one depicted in **Figure 6**, the current demanded by the reference pin produces a voltage drop across the output impedance of the voltage reference circuitry.

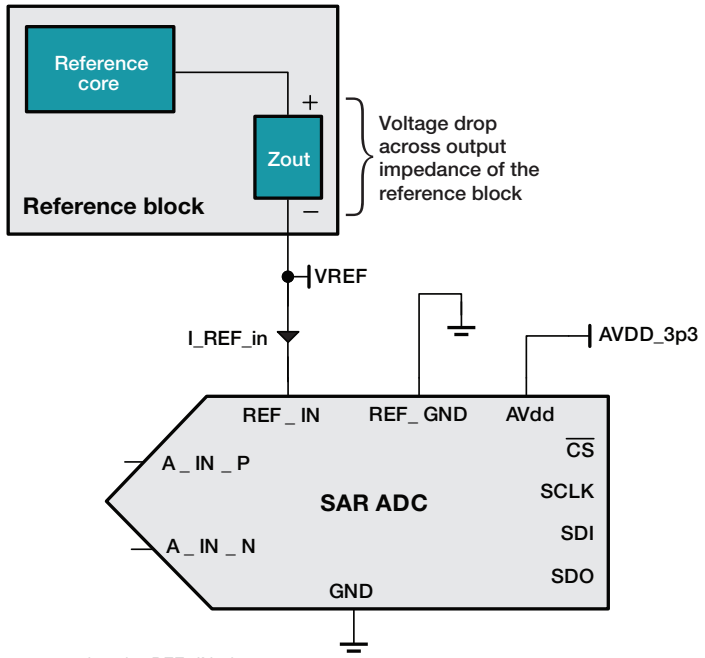

Figure 6. Voltage drop on the circuit connected to the REF_IN pin.

This drop across the output impedance of the reference block causes input-dependent variations on the voltage of the internal reference capacitor. Inevitably, there is a corresponding inaccuracy in the conversion, since it is the internal voltage on C_{REF_INT} that is used for analog-to-digital conversion.

Two key questions are how severe the voltage drop is and how you can mitigate it. I'll explore the answer to the first question in the sections "System without reference buffer," "System with reference buffer" and "System with REF6045."

Dispelling a common misconception

Many designers believe that if **Equation 5** and **Equation 6** express the voltage on the ADC reference pin (with V_{REF} and k both constants with respect to time), that you can then calibrate the error caused by reference-voltage fluctuations just as if it were part of a gain error term.

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2V_{REF}(t)}\right)\right] \quad (5)$$

where V_{IN} is the analog input to the data converter, N is the data-converter resolution, and $V_{REF}(t)$ is the time-varying voltage applied to the data-converter reference pin.

$$V_{REF}(t) = V_{REF} + kv_{IN}(t) \quad (6)$$

where V_{REF} is the DC portion of the reference pin voltage, V_{IN} is the analog input to the data converter, and k is a constant with respect to time.

Such a notion is false. **Equation 5** and **Equation 6** can be combined and rewritten as **Equation 7**. It is a misinterpretation to think that **Equation 7** can be factored into the right-hand side of **Equation 1** plus a linear error term.

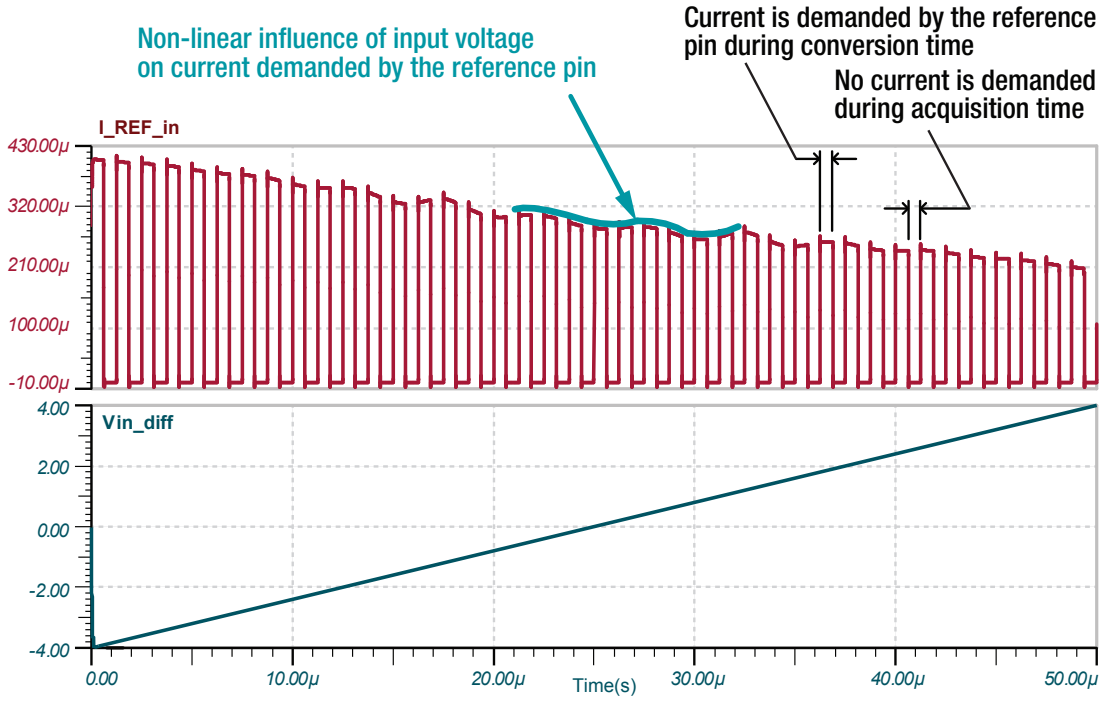

Figure 7. *Current demanded by the reference pin of an 18-bit SAR ADC.*

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2(V_{REF} + kv_{IN}(t))}\right)\right] \quad (7)$$

Equation 8 re-expresses **Equation 7**. Appendix A provides a proof that **Equation 7** and **Equation 8** are equivalent. **Equation 8** shows how ADC output code words have a nonlinear dependency on the input signal, even when the variation on the reference-pin voltage is directly proportional to the input signal.

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2V_{REF}}\right) - 2^{N-1}\left(\frac{k(v_{IN}(t))^2}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right)\right] \quad (8)$$

SPICE modeling

In order to study the effects of voltage references on the performance of data-acquisition systems, I created a SPICE model based on lab measurements of the current demanded by the reference pin of an 18-bit SAR ADC.

Figure 7 shows modeled current for a differential analog input ramping from –4 V to 4 V when the 18-bit ADC is running at 800 kSPS.

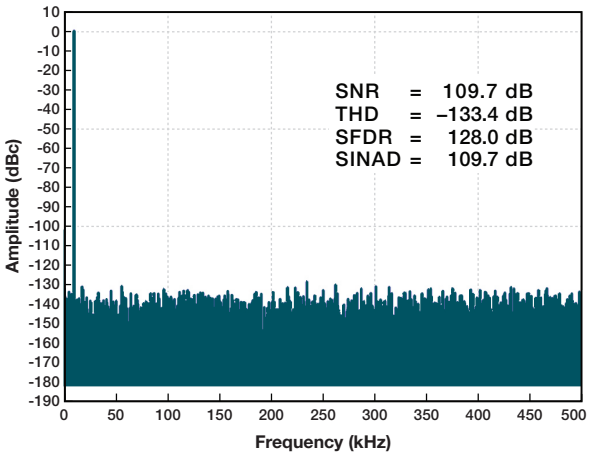

***Figure 8**. Key AC performance metrics and FFT for an ideal 18-bit SAR ADC.*

Note these features in **Figure 7**:

- The current demanded is 0 A during the acquisition phase.
- The input-voltage level is inversely related to the current drawn.
- The value of the peak current demanded by the ADC reference pin is a nonlinear function of the analog input signal; although the peak current decreases with the increasing differential input signal, this decrease is not perfectly linear. You will notice bumps in the current waveform.

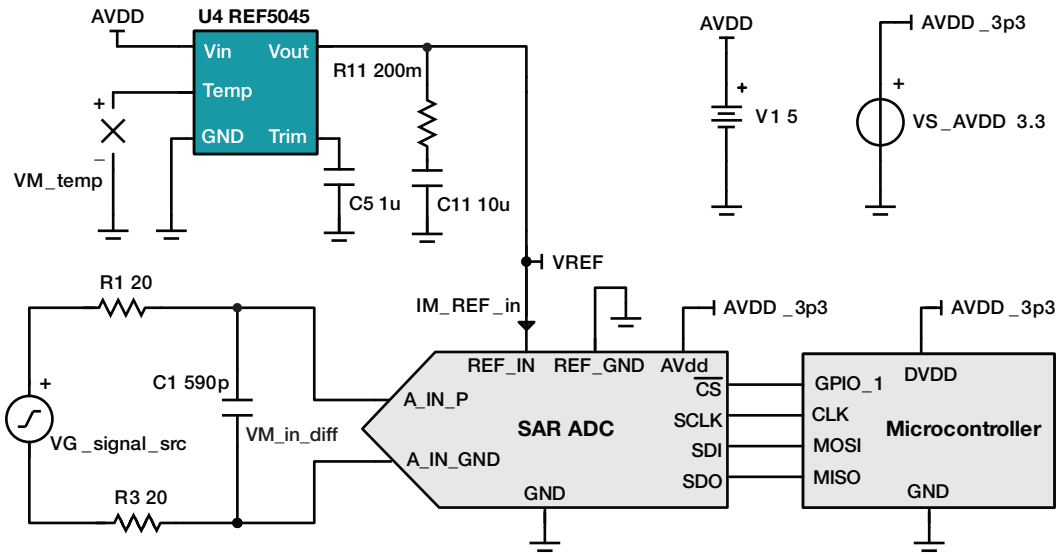

***Figure 9**. Schematic of a data-acquisition system without a reference buffer.*

Obtaining a closed-form algebraic expression for the voltage on the reference terminal of a SAR ADC as a function of ADC input voltage (and ADC architecture) is outside the scope of this paper. However, the SAR ADC output codes will contain some distortion due to the relationship between the reference-pin input current and ADC analog-input voltage.

This output distortion would be present even if the relationship between reference-pin input current and ADC input voltage were linear (an idealized case that does not match the behavior of integrated circuits [ICs]).

Figure 7 shows that in a physical SAR ADC, the reference-pin input current is a nonlinear function of the ADC input voltage; thus, the ADC output codes' distortion is further accentuated, especially when the voltage reference driving circuitry is not designed properly.

Upper-bound performance of an 18-bit SAR ADC

Before exploring the performance of various reference circuits, let us review the top performance metric values of the ideal case, for comparison.

The top performance of an 18-bit acquisition system is bounded by the ideal ADC transfer function given in **Equation 1**.

Figure 8 shows a 16,384-point FFT of the output code words for an ideal 18-bit SAR ADC running at 1 MSPS with a 10-kHz, 4.347-VPK differential-input sine wave. The nominal reference voltage is 4.5 V and the input-signal amplitude corresponds to 0.3 dB below full scale. Under these conditions, no 18-bit data-acquisition system can yield better performance than that shown in **Figure 8**.

Appendix B shows the circuit schematic used to obtain the results of **Figure 8**.

Appendix C shows how to calculate the key alternating current (AC) performance metrics of a data-acquisition system based on its FFT.

System without reference buffer

Figure 9 shows the first circuit analyzed. It essentially consists of the REF5045 and those passive elements around it feeding directly into the reference pin of an 18-bit SAR ADC.

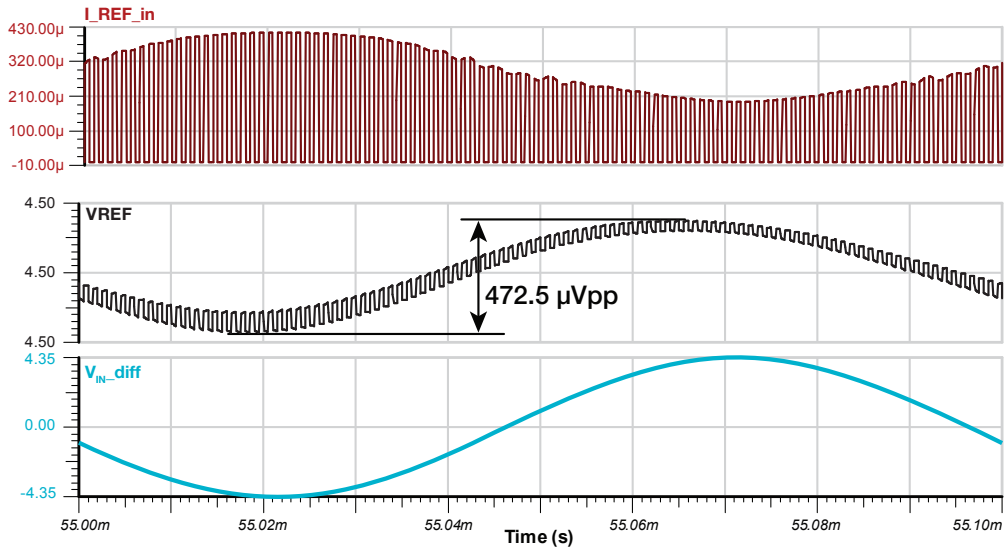

Figure 10. Simulation results for a system without a reference buffer.

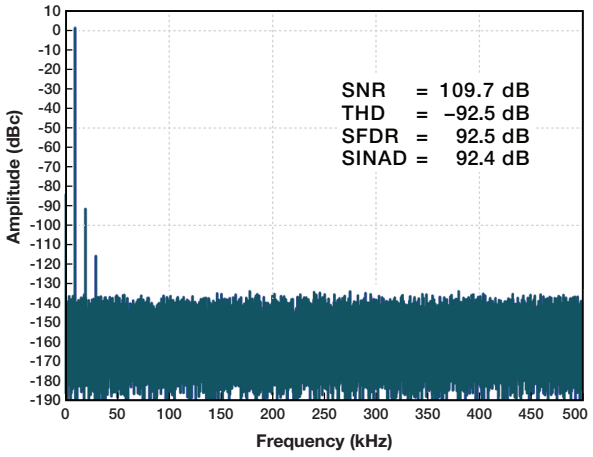

Figure 11. *Key AC performance metrics and FFT for a system without a reference buffer.*

This data converter has a linear transfer function and no intrinsic noise; however, the current drawn from the reference pin corresponds to that shown in **Figure 7**. The data converter is running at 1 MSPS and the input signal is a 10-kHz, 4.347-V_{PK} sine wave.

The differential input-signal amplitude corresponds to 0.3 dB below full scale, since the nominal reference voltage is 4.5 V.

Figure 10 shows the simulation results for the circuit in **Figure 9**.

The blue trace labeled V_{IN_diff} is the 10-kHz differential input signal connected to the SAR ADC.

The red trace labeled I_REF_IN is the current flowing into the REF_IN pin of the ADC. Just as in **Figure 7**, the current demanded by the REF_IN pin is a nonlinear function of the differential input signal.

The black trace labeled VREF is the voltage with respect to ground of the REF_IN pin of the ADC; ideally, this voltage would be 4.5 VDC.

In reality, the voltage on the REF_IN pin is approximately 4.502 VDC with a 472.5-µVpp ripple modulated by the differential input signal and the sampling clock of the ADC. The output of the REF5045 fluctuates because of the current drawn by the reference pin in conjunction with the REF5045 output impedance, plus the effects of R11 and C11.

A 16,384-point FFT of the ADC-acquired data better quantifies the effect of the ripple observed on the REF_IN pin. **Figure 11** shows the FFT and the critical AC performance metrics obtained.

See Appendix C for more information on how to calculate the key AC performance metrics of a data-acquisition system based on its FFT.

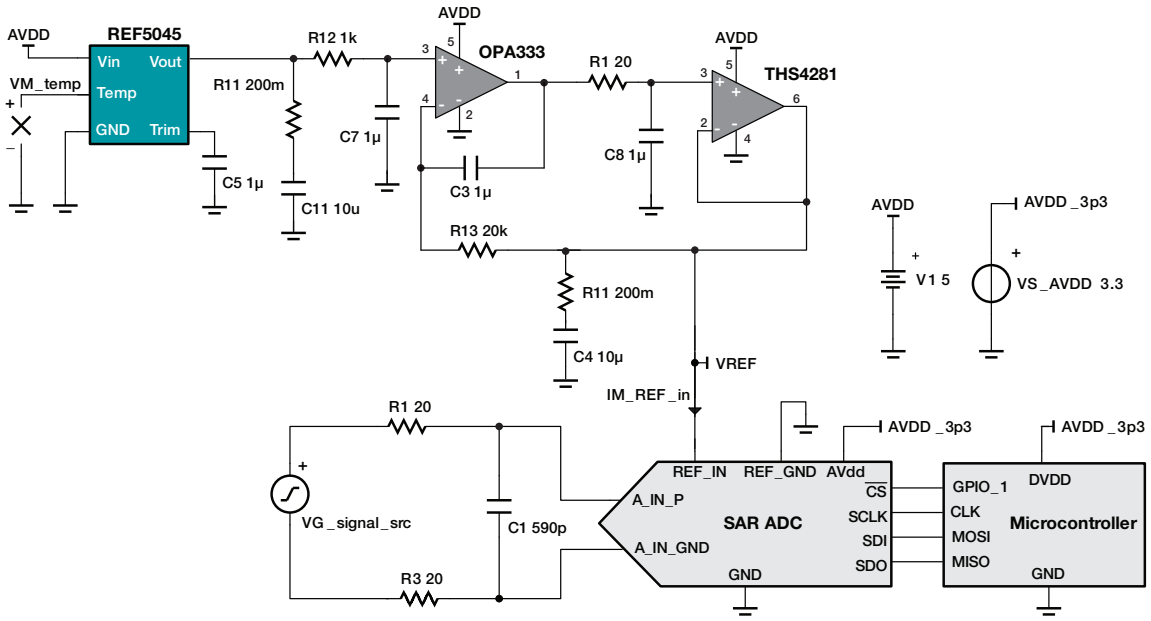

Figure 12. *Schematic of a data-acquisition system with a reference buffer.*

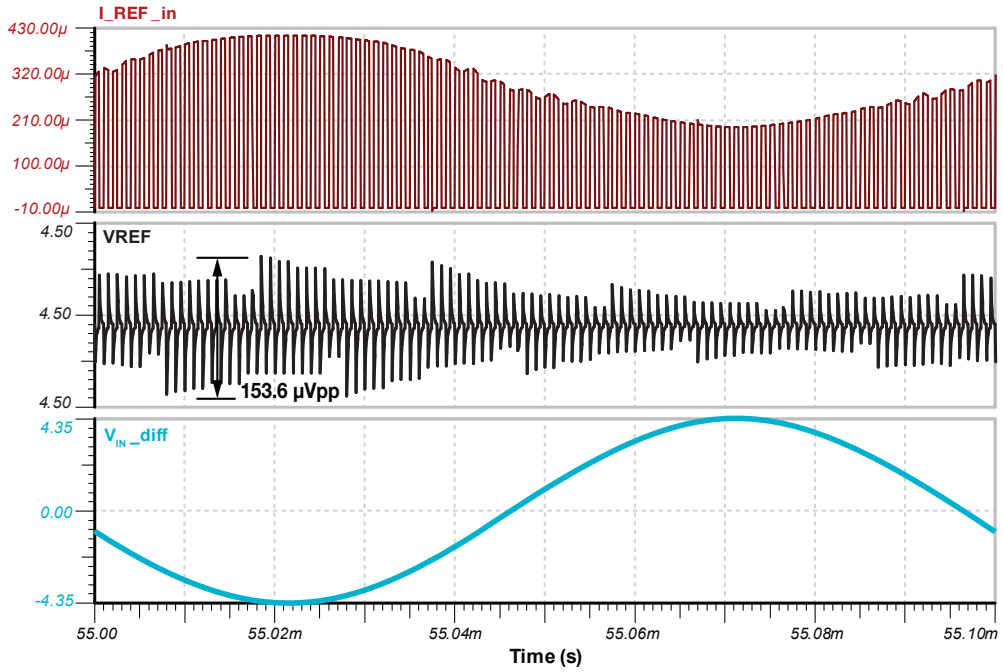

Figure 13. Simulation results for a system with a reference buffer.

System with reference buffer

The next circuit simulated consists of the REF5045 and a reference buffer constructed with two amplifiers (THS4281 and OPA333) in a composite double-feedback architecture, as shown in **Figure 12**.

Figure 13 shows the simulation results for the circuit in **Figure 12**. The SAR data converter is, once again, running at 1 MSPS, and the input signal is a 10-kHz, 4.347-V_{PK} sine wave. The input-signal amplitude corresponds to 0.3 dB below full scale, since the nominal reference voltage is 4.5 V.

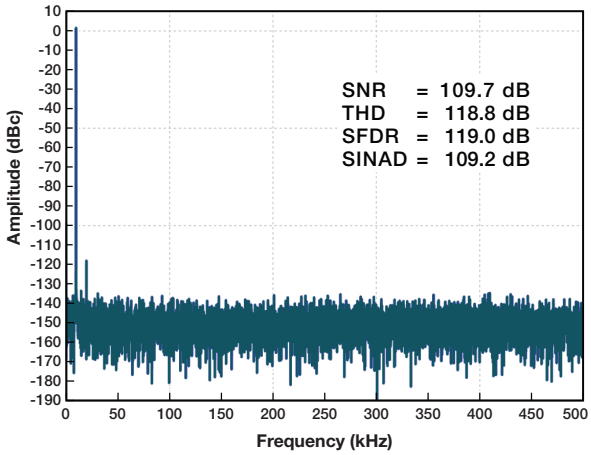

Figure 14. Key AC performance metrics and FFT for a system with a reference buffer.

The blue trace labeled Vin_diff is the 10-kHz differential input signal connected to the ideal SAR ADC.

The red trace labeled I_REF_IN is the current flowing into the ADC REF_IN pin. Note that, just as **Figure 7** shows, the current demanded by the REF_IN pin is a nonlinear function of the differential input signal.

The black trace labeled VREF is the ADC REF_IN pin voltage with respect to ground. The voltage on the REF_IN pin consists of a 4.502-VDC level plus a 153.6-µVpp ripple modulated by the differential input signal and the sampling clock of the ADC.

When using a buffer, the voltage ripple observed on the ADC REF_IN pin decreases by a factor of three compared to the ripple observed in **Figure 9**'s circuit.

A 16,384-point FFT of the ADC-acquired data better quantifies the effect of the ripple observed on the REF_IN pin.

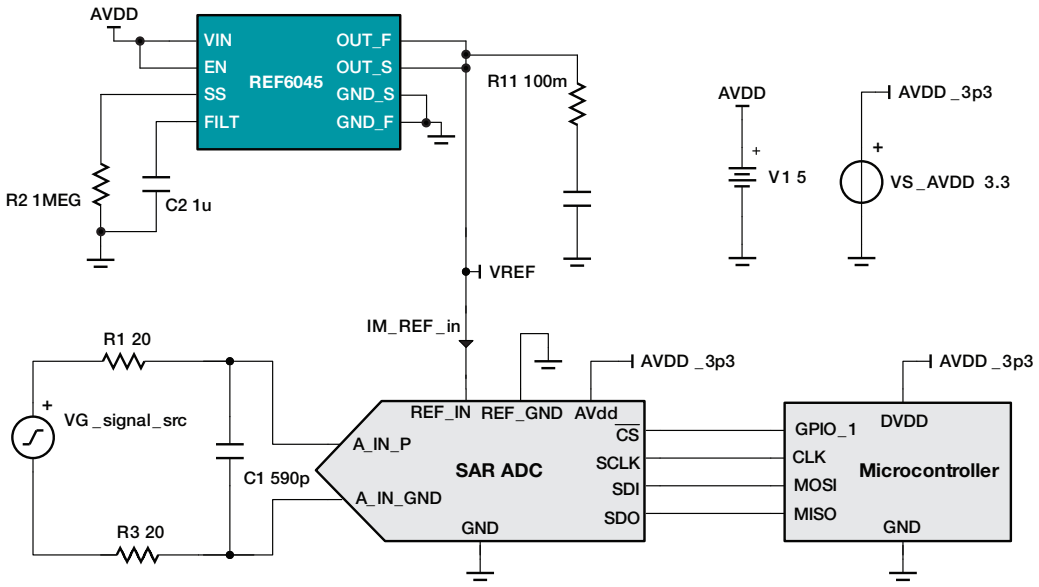

Figure 15. *Schematic of a data-acquisition system with the REF6045.*

Figure 14 shows the FFT and the critical AC performance metrics obtained. Note that the system in **Figure 12** performs better than the system in **Figure 9**. When using a buffer circuit, THD improves by 26.3 dB.

The system depicted in **Figure 12** performs much better than the system shown in **Figure 9** because the output impedance of the reference buffer used in **Figure 12** is lower than the REF5045 output impedance.

System with REF6045

The last circuit simulated consists of the REF6045 and those passive elements around it feeding directly into the reference pin of an ideal 18-bit SAR ADC.

The REF6045 is a voltage reference with an integrated output driver featuring ultra-low output impedance. The same conditions and assumptions used in the previous two cases apply for the circuit used to test the REF6045: a SAR ADC with a linear transfer function and no intrinsic noise, sampling at 1-MSPS and a 10-kHz, 4.347-VPK sine-wave input.

Figure 15 shows the circuit schematic and **Figure 16** shows the simulation results for the circuit based on the REF6045.

	Ideal ADC with no V_{REF} fluctuation	REF5045 by itself	REF5045 with driving buffer	REF6045
Average reference pin voltage (V)	4.5	4.502	4.502	4.501
Peak-to-peak variation in V_{REF} (uV)	0	472.5	153.6	76.8
SNR (dB)	109.7	109.7	109.6	109.8
THD (dB)	-133.4	-92.5	-118.8	-123.7
SFDR (dB)	128	92.5	119	124.5
SINAD (dB)	109.7	92.4	109.2	109.6
Maximum quiescent current of voltage reference and its buffer (mA)	N/A	1	1.925	0.7

Table 1. *Performance comparison.*

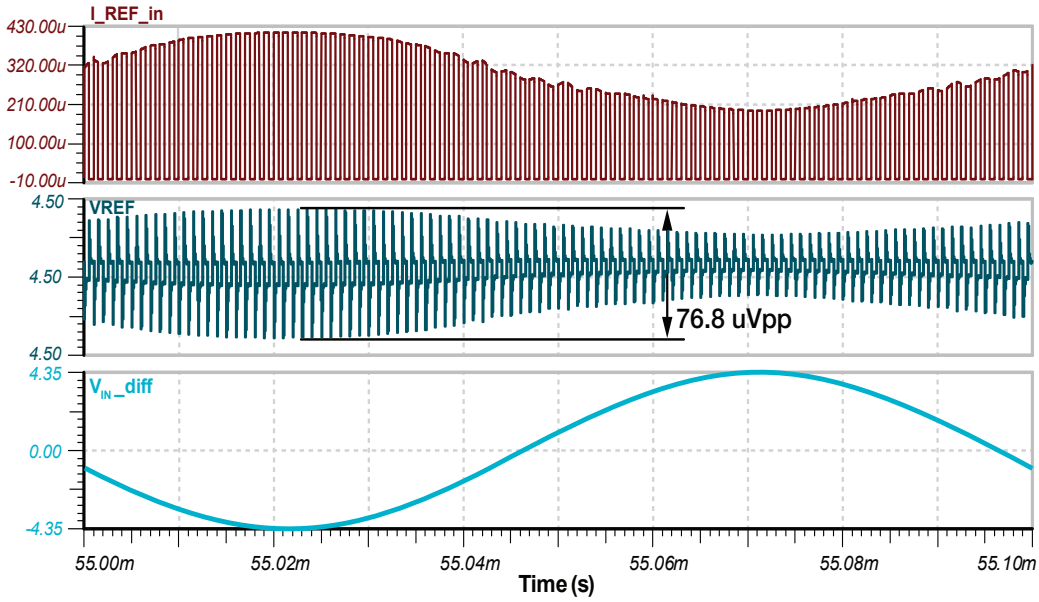

Figure 16. *Simulation results for a system with the REF6045.*

The blue trace labeled Vin_diff is the 10-kHz differential input signal connected to the ideal SAR ADC.

The red trace labeled I_REF_IN is the current flowing into the ADC REF_IN pin. Note that, just as **Figure 7** shows, the current demanded by the REF_IN pin is a nonlinear function of the differential input signal.

The black trace labeled VREF is the ADC REF_IN pin voltage with respect to ground. The voltage on the REF_IN pin consists of a 4.501-VDC level plus a 76.8-µVpp ripple modulated by the differential input signal and the sampling clock of the ADC.

A 16,384-point FFT of the ADC-acquired data better quantifies the effect of the ripple observed on the REF_IN pin.

Figure 17 shows the FFT and the critical AC performance metrics obtained. System performance improves even further from the second case simulated (REF5045 plus buffer circuit): THD improves by another 4.9 dB.

The system depicted in **Figure 15** performs better than the system in **Figure 12** because the output impedance of the internal buffer integrated into the REF6045 is lower than the output impedance of the buffer used in **Figure 12**.

Performance comparison

Table 1 provides a comparison of the four scenarios simulated. In summary, the system that uses the REF6045 (**Figure 15**) is the one that more closely approaches the upper boundary of 18-bit performance. The low output impedance of the REF6045's integrated output driver is the key parameter enabling the system in **Figure 15** to yield –123.7 dB of THD – which is 4.9 dB better than the system depicted in **Figure 12** and 31.2 dB better than a system with no voltage-reference buffer.

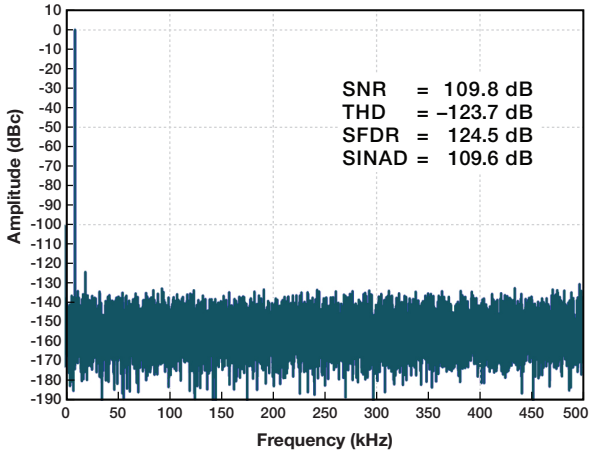

Figure 17. *Key AC performance metrics and FFT for a system with the REF6045.*

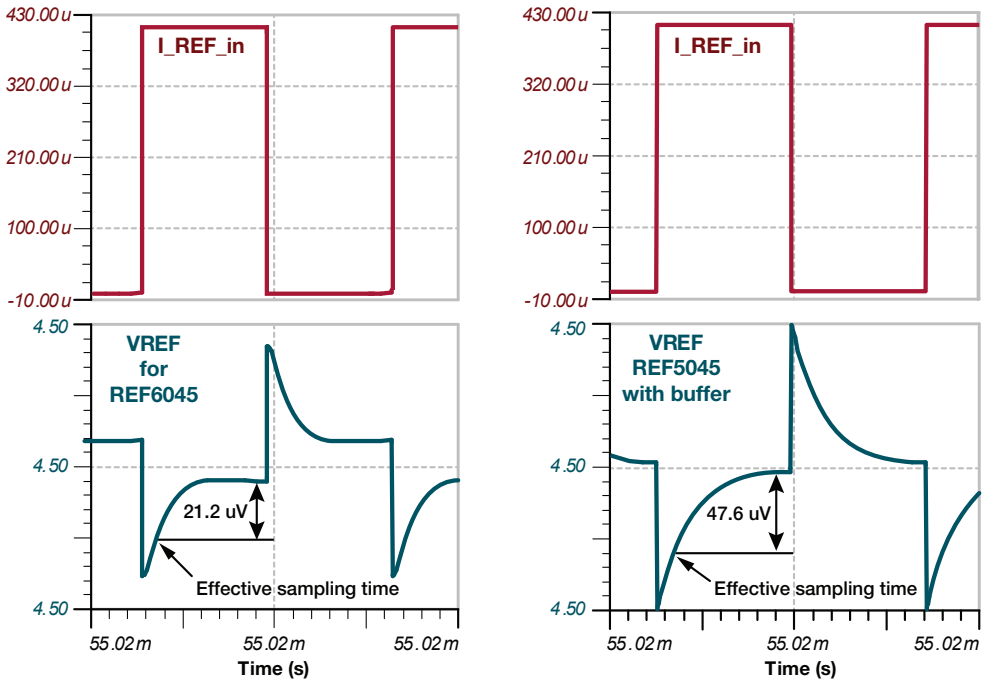

Figure 18. *Settling times for systems depicted in Figure 12 and Figure 15.*

In the time domain, the peak-to-peak voltage variation of the reference input pin provides a rough indicator of how much distortion a suboptimal voltage-reference buffer produces.

Another point of comparison is the settling time of the voltage on the REF_IN pin. **Figure 18** shows the settling behavior of the circuits depicted in **Figure 12** and **Figure 15**.

Note that the SAR ADC does not use the VREF value obtained exactly at the beginning of the conversion period; instead, the internal processing delay in the ADC allows the value of VREF to start advancing toward settling before the ADC uses the voltage for the first time at the point labeled "Effective sampling time" in **Figure 18** (which corresponds to the determination of the most significant bit in the conversion process).

Figure 18 shows that the integrated output driver in the REF6045 brings VREF closer to its fully settled value faster than the reference-buffer circuit used in **Figure 12**.

References

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Appendix A

Equations 9-16 are proof that **Equation 7** and **Equation 8** are equivalent.

Starting from **Equation 8** (repeated here for convenience as **Equation 9**):

$$\text{Codeword}_{OUT} = \text{floor}\left[v_{IN}\left(\frac{2^N}{2V_{REF}}\right) - 2^{N-1}\left(\frac{k(v_{IN}(t))^2}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right)\right] \quad (9)$$

Taking V_{IN} as a common factor:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\left[\left(\frac{2^N}{2V_{REF}}\right) - 2^{N-1}\left(\frac{k(v_{IN}(t))}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right)\right]\right\} \quad (10)$$

Expanding 2^{N-1}:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\left[\left(\frac{2^N}{2V_{REF}}\right) - \frac{2^N}{2}\left(\frac{k(v_{IN}(t))}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right)\right]\right\} \quad (11)$$

Taking $2^N/2$ as a common factor:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\frac{2^N}{2}\left[\frac{1}{V_{REF}} - \frac{k(v_{IN}(t))}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right]\right\} \quad (12)$$

Finding a common denominator for the terms inside the brackets:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\frac{2^N}{2}\left[\frac{V_{REF} + k(v_{IN}(t)) - k(v_{IN}(t))}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right]\right\} \quad (13)$$

Performing the sum of the numerator terms inside the brackets:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\frac{2^N}{2}\left[\frac{V_{REF}}{V_{REF}^2 + kV_{REF}v_{IN}(t)}\right]\right\} \quad (14)$$

Taking V_{REF} as a common factor in the denominator inside the brackets:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\frac{2^N}{2}\left[\frac{V_{REF}}{V_{REF}(V_{REF} + kv_{IN}(t))}\right]\right\} \quad (15)$$

Equation 7 follows by simplifying the fraction inside the brackets:

$$\text{Codeword}_{OUT} = \text{floor}\left\{v_{IN}(t)\frac{2^N}{2}\left[\frac{1}{V_{REF} + kv_{IN}(t)}\right]\right\} \quad (16)$$

Appendix B

Ideal case: Constant reference voltage

Figure 19 shows the schematic used to simulate an ideal 18-bit SAR ADC, running at 1 MSPS, with a 10-kHz, 4.347-V_{PK} differential-input sine wave. The input-signal amplitude corresponds to 0.3 dB below full scale, since the nominal reference voltage used is 4.5 V. An ideal voltage source that has no output impedance provides the reference voltage; therefore, the voltage-reference pin has no ripple voltage, despite the current drawn during the conversion process.

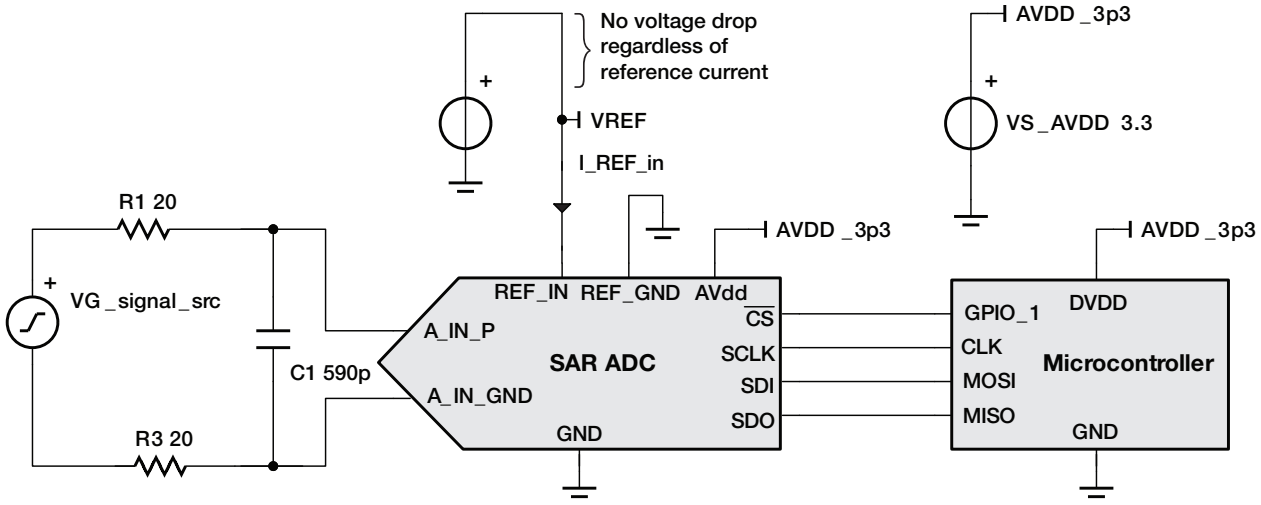

Figure 19. System schematic with constant voltage on C_{REF_IN}

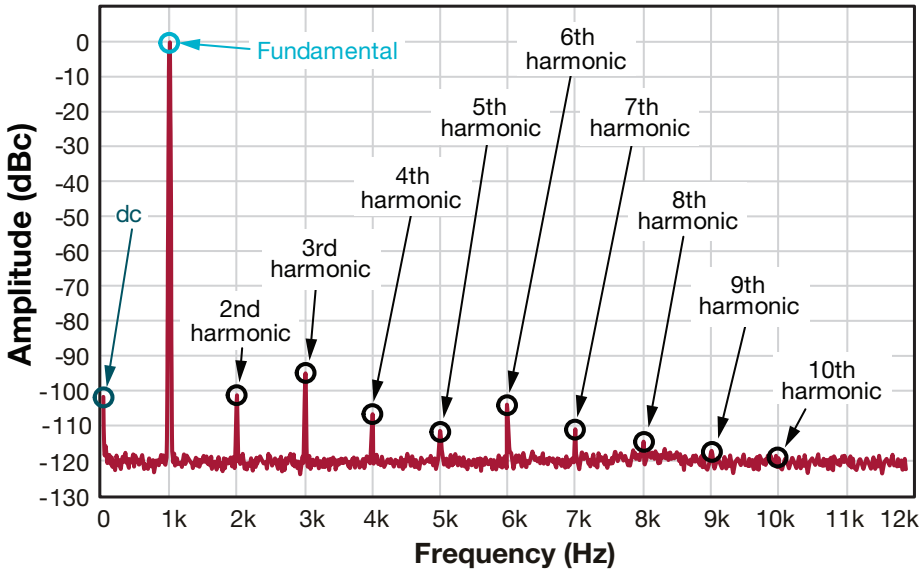

Figure 20. *Components of an FFT.*

The theoretical SNR expected for a full-scale signal in an 18-bit ADC is given by **Equation 17**:

$$\mathrm{SNR}_{\mathrm{theoretical}} = 6.02N + 1.76 = 6.02(18) + 1.76 = 110.12\ \mathrm{dB} \quad (17)$$

The SNR obtained in the four simulations hovers around 109.6 dB to 109.8 dB, which is roughly 0.3 dB below the theoretical SNR; this is due to the fact that the input signal used for simulation is not a full-scale signal (4.5 V_{PK}). Instead, the maximum input voltage applied is 4.347 V_{PK} (0.3 dB below full scale). Selecting a test input signal with some headroom below full scale is a common practice in ADC testing in order to avoid possible saturation or operation in the nonlinear region of the data converter.

Appendix C

Calculation of SNR, THD and SINAD

This section provides a basic tutorial on how to calculate the critical AC performance metrics in data-acquisition systems. The starting point is the FFT of the system output for a sinusoidal input.

A comprehensive treatment of the subject is outside the scope of this paper. See references [4] and [5] for more information and numerical examples.

According to IEEE standard 1241, THD is: "For a pure sine-wave input of specified amplitude and frequency, the root-sum-of-squares (RSS) of all the harmonic distortion components including their aliases in the spectral output of the analog-to-digital converter. Unless otherwise specified, THD is estimated by the RSS of the second through the tenth harmonics, inclusive."

Figure 20 shows an FFT plot and **Table 2** shows the corresponding harmonic values. The fundamental component is circled in blue, harmonics 2 through 10 are circled in black and the DC component is circled in green.

IEEE standard 1241 explains that "THD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency..."

If the amplitude of each harmonic component is expressed in decibels with respect to the input carrier frequency (dBc), then the THD can be calculated as shown in **Equation 18**:

$$\mathrm{THD} = 10\log_{10}\left(\sum_{i=2}^{10} 10^{\frac{D_i}{10}}\right) \quad (18)$$

Harmonic	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th
Amplitude (dBc)	0	-101	-95	-107	-111	-104	-111	-115	-117	-119
Variable	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}

Table 2. *Harmonic amplitudes.*

Evaluating **Equation 18** with the data from **Table 2** yields **Equations 19** and **Equation 20**:

$$\mathrm{THD} = 10\log_{10}\left(10^{\frac{-101}{10}} + 10^{\frac{-95}{10}} + 10^{\frac{-107}{10}} + 10^{\frac{-111}{10}} + 10^{\frac{-104}{10}} + 10^{\frac{-111}{10}} + 10^{\frac{-115}{10}} + 10^{\frac{-117}{10}} + 10^{\frac{-119}{10}}\right) \tag{19}$$

$$\mathrm{THD} = -93.21\ \mathrm{dB} \tag{20}$$

Equation 21 calculates the signal-to-noise-and-distortion ratio (SINAD). For example, suppose **Figure 21** shows the values obtained in an N-point FFT; suppose also that the fundamental tone lands at frequency f1, which corresponds to j times the frequency step Δf (for integer j). **Equation 21** requires the inclusion of all terms in the FFT except two terms: the DC term, X0, and the fundamental term, D1.

$$\mathrm{SINAD} = -10\log_{10}\left[\sum_{\substack{i=1\\ i=j}}^{\frac{N}{2}-1}\left(10^{\frac{X_i}{10}}\right)\right] \tag{21}$$

Equation 22 calculates the SNR. For example, suppose **Figure 22** shows the values obtained in an N-point FFT; suppose also that the fundamental tone lands at frequency f1, which corresponds to j times the frequency step Δf (for integer j).
Equation 22 requires the inclusion of all terms in the FFT except 11 terms: the DC term, X0; the fundamental term, D1; and all harmonic terms, from the second through the tenth.

$$\mathrm{SINAD} = -10\log_{10}\left[\sum_{\substack{i=1\\ i\neq j\\ X_i \neq D_2, D_3, \ldots, D_{10}}}^{\frac{N}{2}-1}\left(10^{\frac{X_i}{10}}\right)\right] \tag{22}$$

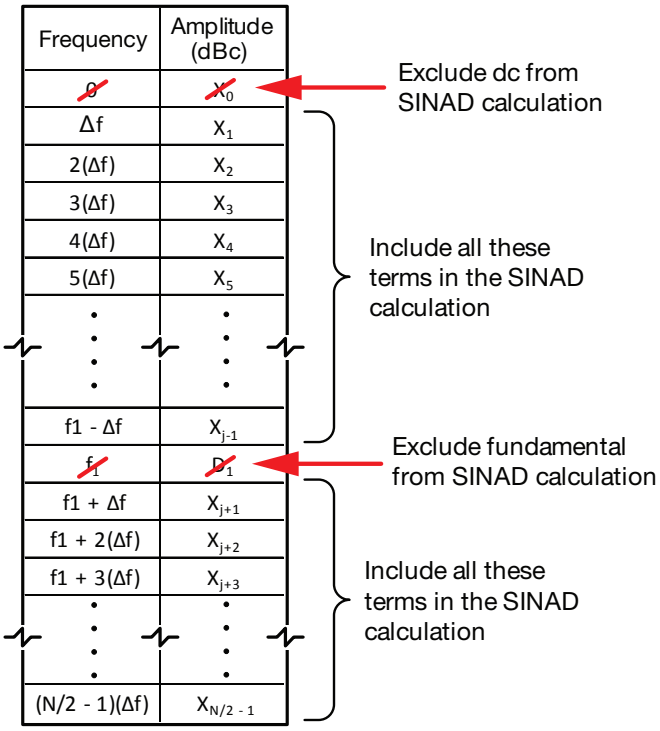

Figure 21. *Table of FFT components used in SINAD calculation*

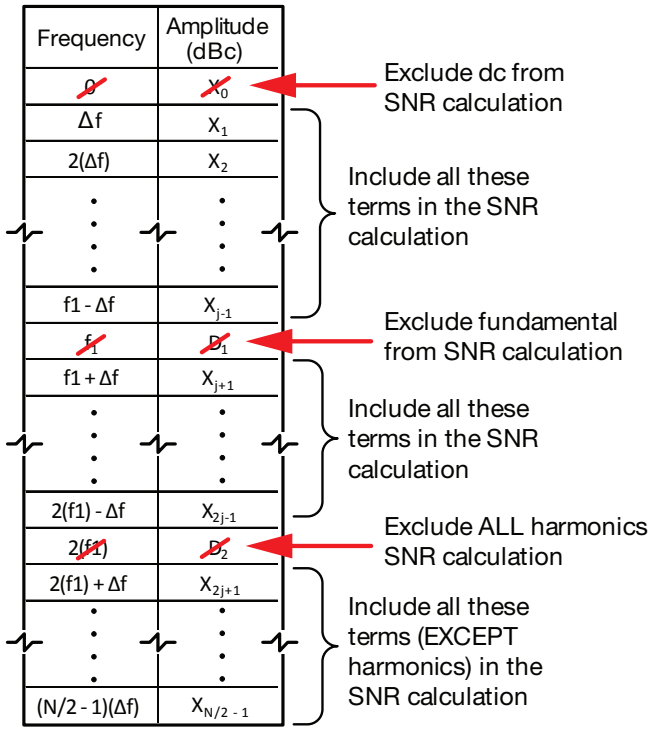

Figure 22. *Table of FFT components used in SNR calculation.*

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