Application Note

Cost-Optimized, High-Performance Front-End Design for Analog Input Modules

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ABSTRACT

Designing programmable logic controller (PLC) analog input modules requires the engineer to balance multiple, often conflicting parameters. Analog input module designs must offer flexibility to support different process signal types and ranges, include multiple inputs for high channel-count systems, enable high-accuracy measurements, and result in a cost-competitive design. This complete, pre-tested front-end design for analog input modules saves development time while demonstrating input flexibility and high-accuracy measurements. Additionally, comparing the 1000-unit cost of this discrete design (without the TPS26611 protection circuit) to a more integrated solution shows that the discrete solution cost is about half. The channel cost is about $0.89 for the discrete solution, which drops further if more analog input channels are added.

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Trademarks

1 Introduction

This analog input module front-end design features 8 channels with each channel that can be configured to measure bipolar, universal voltage, and current inputs with a resolution of 16 bits. The module supports a scan rate of 1 ms for all 8 channels. Multiple input voltage ranges are supported with a programmable gain amplifier (PGA). Input ranges supporting up to 20% overrange. Any common-mode voltage (V_{CM}) is effectively rejected. An open-wire detection feature identifies a broken connection to the sensor field transmitter. The design supports the extended industrial operating temperature range of –40°C to 125°C. Table 1-1 summarizes the key parameters of this design.

Table 1-1. Design Parameter

Parameter	Value
Input channel	8
Input type	Universal (Current, voltage), bipolar
Input mode	Differential or single-ended
Differential input signal (maximum)	±12.288 V
Common-mode input signal (maximum)	±12 V
Abs input voltage (each pin)	±12 V (referred to module ground)
Resolution	16 bit (15+1bit)
Sample rate	8 kSPS
Voltage input ranges (including 20% overrange) Voltage input ranges (no overrange) Current input ranges	±10 V ±5 V +10 V +5 V ±2.5 V 0/4...20 mA ±20 mA
Input impedance	Voltage mode: > 1 MΩ Current mode: 250 Ω
Open-wire detection	Yes
50 or 60 Hz rejection	No
Operating temperature	–40°C to 125°C

All terminals are fully protected against overcurrent up to ±30 mA and overvoltage up to ±33 VDC (permanent). Surges according to IEC61000-4-5 (±1 kV at 42 Ω) are effectively suppressed. Measurements on this reference design board demonstrate 16 bits of effective resolution (or ENOB) and 13–14 noise-free bits (NFB), depending on the selected voltage input range. The accuracy at room temperature is < 0.1%. Table 1-2 summarizes the performance specifications for this design.

Table 1-2. Design Performance

Parameter	Performance
Overvoltage protection	±33 V permanent
Overcurrent protection	±30 mA
Surge protection	IEC61000-4-5 (±1 kV/42 Ω)
Mis-wiring protection	Yes, voltage and current input mode
Effective number of bits (ENOB)	≥ 16.3 bit
Noise-free bits	≥ 13.7 bit
Accuracy error	< ±0.1% at room temp
Common-mode voltage rejection	> 80 dB

2 Circuit Description

The circuit consists of three main sections: the input stage that selects between voltage and current inputs while protecting against mis-wiring; the analog stage comprised of multiplexers, an instrumentation amplifier, and an ADC; and the power supply.

2.1 Input Stage

The input stage circuit protects against mis-wiring and surges. The following schematic shows the input stage for a single channel.

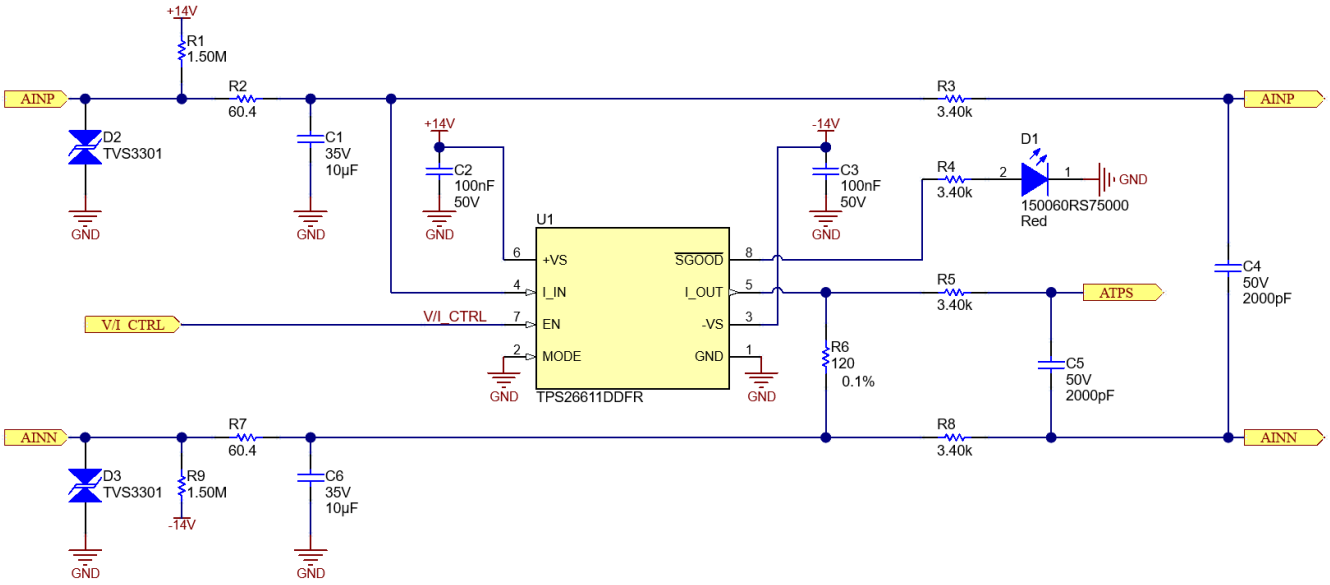

Figure 2-1. V/I Switch and Filter

The input stage tolerates up to ±33 V (permanent) at the terminals in both current and voltage mode. The input protection circuit also limits the input current to ±30 mA (maximum) in current mode only and suppresses surges of ±1 kV at 42 Ω in accordance to IEC61000-4-5 specifications using the TVS3301, a 33-V bidirectional flat-clamp surge protection device. Current or voltage inputs are selected by a 3.3-V digital control signal (*V/I CTRL* in Figure 2-1), which controls the switch inside the TPS26611 loop protector. In voltage mode, the TPS26611 switch is open and the input signal is directly fed to the next stage. In current mode, the TPS26611 switch is closed and connects both terminal pins through the shunt resistor. The voltage drop across the shunt is the sensor signal to be measured. For high-accuracy measurements, the TPS26611 switch must be excluded and an additional signal (*ATPS* in Figure 2-1) is introduced. Diode D1 is the indicator of overvoltage or overcurrent condition in current mode.

Open-wire detection (OWD) is implemented by pullup and pull-down resistors at the terminals. In voltage mode, the differential input voltage clips to the rails, which results in an invalid input signal. In current mode, OWD is detected by a 0-mA reading.

Simple passives result in low-pass common-mode and differential anti-aliasing filters (AAF) that limit the input signal bandwidth and thereby reducing noise. This design supports various configurable differential filter per use-case or design need. Figure 2-1 shows common-mode filters R2, C1 and R7, C6, which each have a 256-Hz cutoff frequency. The differential filter is implemented separately for voltage and current inputs, using R3, R8, C4 and R5, R8, C5, respectively. Each differential filter has a cutoff frequency of about 12 kHz for best common-mode rejection performance of the instrumentation amplifier INA826. The AAF resistors also protect the multiplexer from excessive current in mis-wiring and surge events.

2.2 Multiplexer Stage

The multiplexer stage consists of three MUX508 multiplexers (see left side of Figure 2-2). Multiplexer U5 switches signal AINN of the 8 input channels, multiplexer U4 switches the shunt voltage in current mode, and multiplexer U1 selects the input voltage in voltage mode. In this design, U5 is always enabled while U1 and U4 are enabled based on the input type of the selected input channel. This design can also be implemented by other 8:1 multiplexers like TMUX6208 or TMUX7208 or by a fault-protected multiplexer like the TMUX7308F. A fault-protected multiplexer includes active shutdown circuitry in case the input signal goes beyond the supply rails. Resistors R3 and R8 can be skipped by implementing the fault-protected multiplexer in this design.

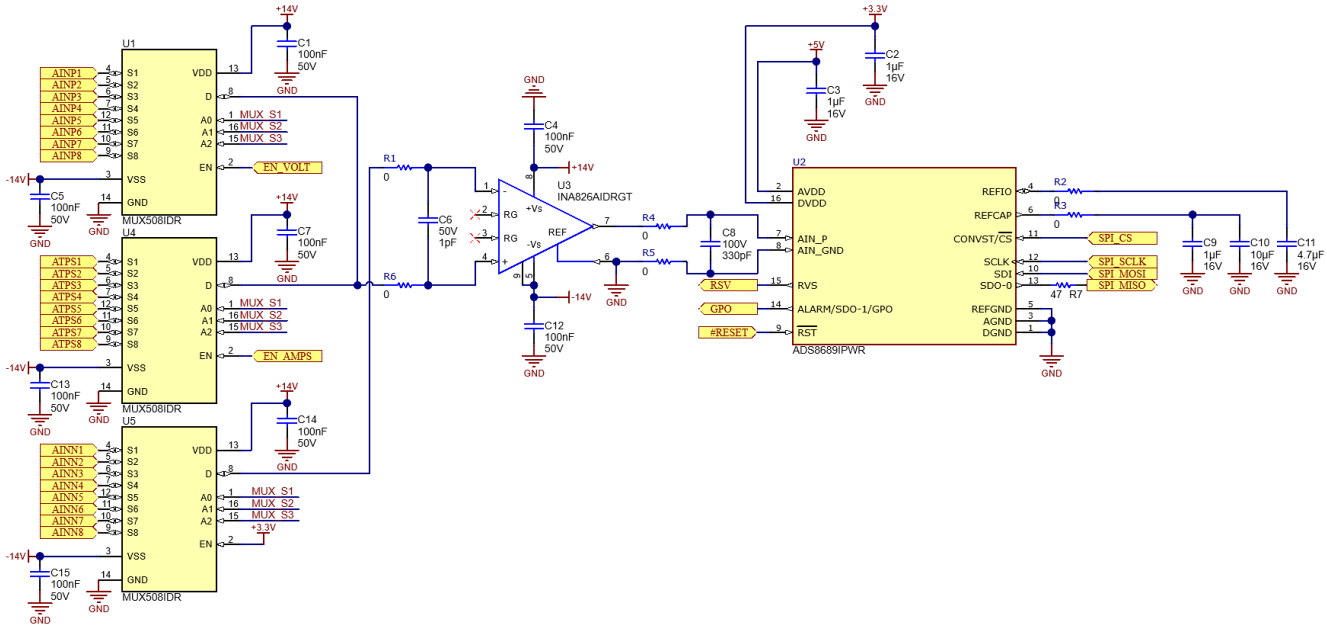

Figure 2-2. Multiplexer, Instrumentation Amplifier and Analog-to-Digital Converter

2.3 Instrumentation Amplifier

The differential output of the multiplexer stage is applied to an instrumentation amplifier. This circuit uses the INA826, which rejects any V_{CM} superimposed to the input signal. A maximum differential signal of ±12.288 V is supported and is not changed by the INA826 (fixed gain = 1 V/V). An alternative option is the INA823 with lower input offset and slightly higher gain error. The single-ended signal at the output of the INA is provided to the ADC.

2.4 Analog-to-Digital Converter

The ADC used in this design is the ADS8689, a 16-bit successive approximation register (SAR) converter with integrated signal-chain consisting of a programmable gain amplifier (PGA) and a 2nd-order low-pass filter (LPF). The ADS8689 accepts input voltages up ±12.288 V while only requiring a single 5-V power rail. The PGA allows a constant resolution across all voltage inputs ranges because its output always utilizes the entire ADC input range. The integrated LPF with a $f_{CUT\text{-}OFF\_\text{-}3dB}$ = 15 kHz limits signal settling time in a multiplexed design. The SAR converter can operate at a sample rate of up to 100 kSPS. The sampling rate is set by the processing unit via the serial interface CONVST/$\overline{CS}$ signal. The precision integrated 4.096-V voltage reference reduces board space and cost. The ADS8689 employs a simple SPI for seamless connection to standard microcontrollers and microprocessors. If isolation is required, refer to *Digitally-isolated ADS8689 circuit design*.

2.5 Power Supply

The power supply in Figure 2-3 generates three supply voltages (+5 V, –14 V, and +14 V) from a standard PLC field power supply (24 V, ±20%). The +5-V rail for the ADS8689 analog section is generated directly by the TPS560430 buck converter. The negative voltage is created by a discrete charge pump driven from the TPS560430 switch node. The negative voltage LDO LM337 regulates the voltage to –14 V. The LDO LM317L derives the +14-V supply voltage directly from the main +24-V input voltage. The wide +1.65-V to 5-V range for the ADS8689 digital supply is expected to be provided by the host controller power supply (not shown here). However, it is possibly to generate the digital supply voltage from the +5-V rail by a low-voltage LDO such as TLV740P. An isolated power supply design is outside the scope of this document.

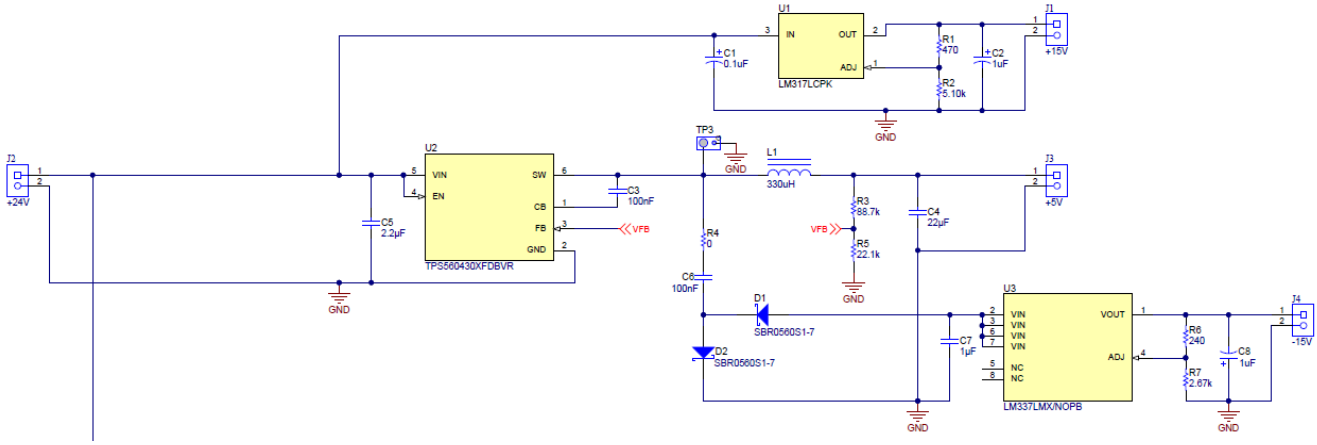

Figure 2-3. Power Supply for Analog Front End

3 Results

The performance of the analog signal-chain is verified with a custom board. The following subsections detail the results of each performance test.

3.1 Accuracy and Noise Performance

The following table shows accuracy and noise results of the hardware at 25°C. A differential DC voltage is applied to a random input. The result is compared against the expected value. The effective number of bits (N_{EFF}) and the noise-free bits (N_{NFREE}) are calculated by a histogram with 65535 samples at a sampling speed of 20 kSPS. The measured value is the mean of the histogram.

Table 3-1. Accuracy and Noise Performance

Input	VREF	Measured	Expected	|Δcode|	Sigma	N_{EFF}	N_{NFREE}
0 V	±12.288 V	32767	32768	1	0.56	16.8 bit	14.1 bit
0 V	±2.56 V	32765	32768	3	0.75	16.4 bit	13.7 bit
5.0 V	±6.144 V	59444	59434	10	0.74	16.4 bit	13.7 bit
10 V	±12.288 V	59442	59434	8	0.61	16.7 bit	14.0 bit
–10 V	±12.288 V	6092	6101	9	0.62	16.6 bit	13.9 bit
10.5 mA	5.12 V	16124	16128	4	0.73	16.4 bit	13.7 bit

As an example, the following histogram shows the 0-V differential input with ±12.288-V voltage input range using TI's ADS8681EVM-PDK ecosystem software.

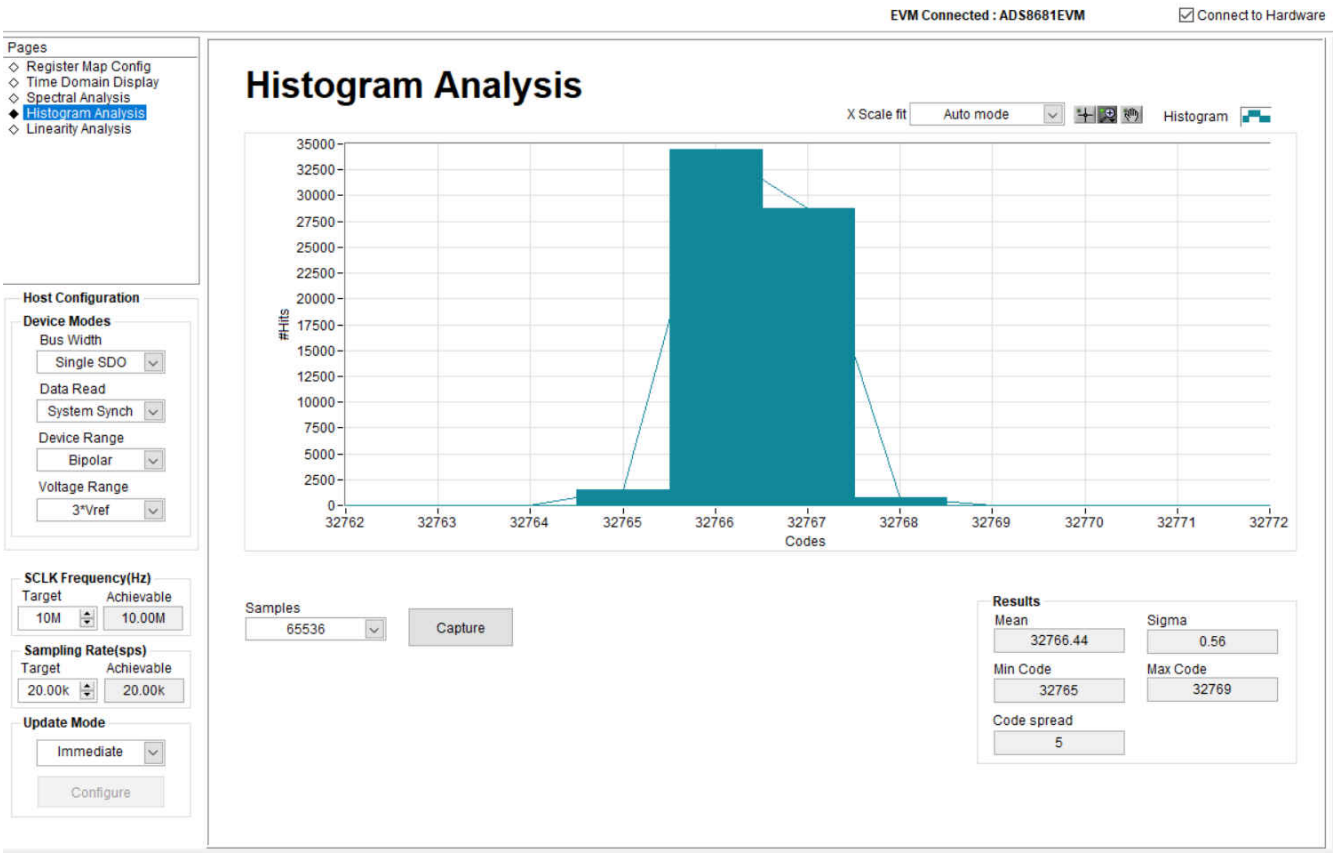

Figure 3-1. Histogram Screen Shot

3.2 Common-Mode Rejection of Input Signal

The common-mode rejection ratio (CMRR) is the ability to suppress unwanted common-mode signals superimposed to the differential signal. A CMRR test is performed by comparing the output codes for a 1-V differential voltage with and without a V_{CM} signal applied. The following table shows that with no V_{CM} signal, the system had an output code deviation of –1 code. Comparatively, the design showed a deviation of –4 to +3 codes with –11.5-V and +11.5-V V_{CM} , resulting in a measured V_{CM} rejection of > 81 dB.

Table 3-2. Common-Mode Rejection Performance

VCM	Input	VRANGE	Measured	Expected	Δcode
–11.5 V	1 V	±2.56 V	45563	45568	–5
0 V	1 V	±2.56 V	45567	45568	–1
+11.5 V	1 V	±2.56 V	45570	45568	+2

3.3 Input Impedance

Input impedance is an important design parameter in voltage-input mode. Analog input modules commonly require > 1-MΩ input impedance to minimize resistive loading when a signal is applied to the analog front end. The majority of the input current leakage shown in the following table is caused by the TPS26611 loop protector and is dependent on the absolute voltage at the inputs. With –5.2 µA, worst case at –10 V, the input impedance is 1.9 MΩ. This measured value is well above the required 1 MΩ.

Table 3-3. Input Leakage Current at Terminals (Voltage Mode)

VINx+	VINx–	IINx+	IINx–
+10 V	GND	–2.5 µA	–4.7 µA
–10 V	GND	–5.1 µA	–3.5 µA
GND	+10 V	–2.5 µA	–4.7 µA
GND	–10 V	–5.2 µA	–3.5 µA

3.4 Settling Time

Settling time specifies the time it takes to switch from one input channel (here: ch1) to another input channel (here: ch2) and the newly selected channel has settled across the analog front-end. The settling time is dictated mainly by the 2nd-order LPF inside the ADC. The preceding front-end should be fast enough not to influence the LPF settling time. This is achieved when a settled signal for each channel is available at the MUX input and settling after the MUX is reduced to a minimum.

Worst case, the input signal of the last channel is the opposite of the new channel, here $V_{IN\_DIFF\_CH1}$ = –10 V and $V_{IN\_DIFF\_CH2}$ = 10 V. Both channels are continuously and alternating converted. Only if both channels reach their steady state values (compare table 3 for steady state values for –10-V and +10-V input signals) the settling is considered complete. Due to demonstration software limitations, a sampling frequency of 24 kSPS (instead of 8 kSPS) was selected. Consequently, the 3rd conversion after each new channel selection is valid. The following image shows the proper settling within 115 µs (125µs (equals 8 kSPS) -10 µs (conversion time)) as the steady-state code for each channel (table 3) matches the codes in the lower-right corner.

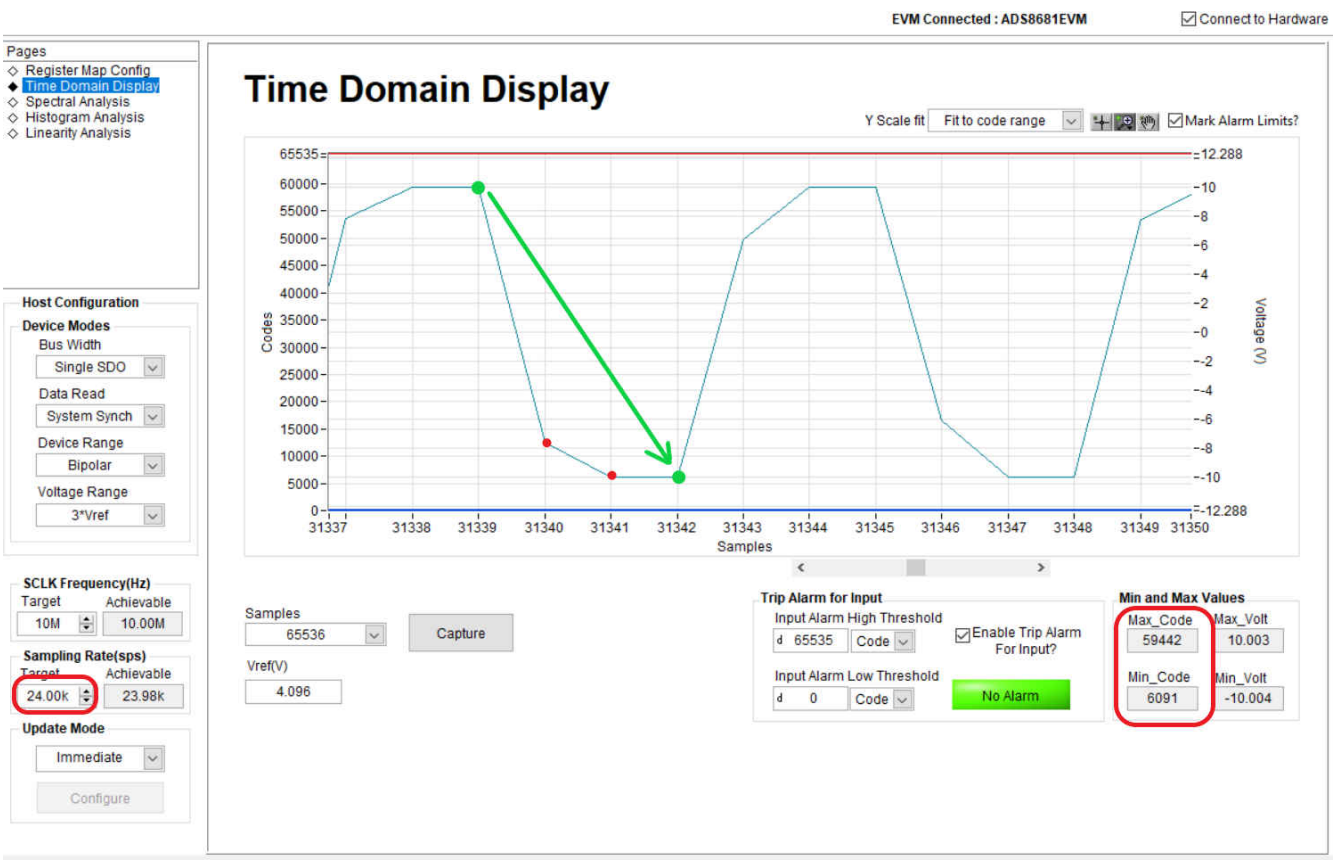

Figure 3-2. Settling Time Verification

3.5 Input Protection

Another important requirement of an analog input module is the ability to tolerate mis-wiring. A connection of the PLC supply voltage of up to ±33 V is tolerated (permanently) in voltage mode as the series resistors R3 and R8 (see Figure 2-1) limit the current into MUX. In current mode the TPS26611 limits the current to 30 mA, turns-off, and retries.

Table 3-4. Current Input During Overvoltage Due to Mis-wiring

Setup	INx+	IN0–	IIN INx+	Comment
Positive voltage input overdrive ch 0	+30 V	GND	4.1 mA	R3, R8 resistors limit current into MUX
Negative voltage input overdrive ch 0	-30 V	GND	-4.1 mA	R3, R8 resistors limit current into MUX
Positive current input overdrive ch 0	+30 V	GND	30 mA	TPS26611 limits, turns-off and retries
Negative current input overdrive ch 0	-30 V	GND	-30 mA	TPS26611 limits, turns-off and retries

4 Summary

This application note introduced a flexible analog-signal chain for analog input modules used in factory automation and control. The discrete approach offers high flexibility when making parameter changes for different specifications.

5 References

1. Texas Instruments, *ADS868x 16-Bit, High-Speed, Single-Supply, SAR ADC Data Acquisition System With Programmable, Bipolar Input Ranges*
2. Texas Instruments, *TPS2661x: 50-V, Universal 4–20 mA, ±20-mA Current Loop Protector With Input and Output Miswiring Protection*
3. Texas Instruments, *MUX50x 36-V, Low-Capacitance, Low-Charge-Injection, Precision, Analog Multiplexers*
4. Texas Instruments, *TMUX730xF ±60-V Fault-Protected, 8:1 and Dual 4:1 Multiplexers with Latch-Up Immunity and 1.8-V Logic*
5. Texas Instruments, *INA826 Precision, 200-µA Supply Current, 3-V to 36-V Supply Instrumentation Amplifier With Rail-to-Rail Output*
6. Texas Instruments, *INA823 Precision, Low-Power, Wide-Supply (2.7-V to 36-V) Instrumentation Amplifier*
7. Texas Instruments, *TPS560430 SIMPLE SWITCHER® 4-V to 36-V, 600-mA Synchronous Step-Down Converter*
8. Texas Instruments, *LM317L 3-Terminal Adjustable Regulator*
9. Texas Instruments, *LMx37 3-Terminal Adjustable Regulators*
10. Texas Instruments, *ADS8681 16-Bit 1MSPS Single-Supply SAR ADC EVM Performance Development Kit (PDK)*
11. Texas Instruments, *Digitally-isolated ADS8689 circuit design* Analog Engineer's Circuit

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