Improving Input Settling for Precision Data Converters

In high precision data acquisition applications the system's performance is susceptible to degradation from a variety of internal and external sources. For signal chains using a successive approximation register (SAR) analog to digital converter (ADC) such as those shown in Table 1, one noise source that can be easily overlooked is digital switching.

Table 1. Common Design Challenges with High-Speed, High-Resolution ADCs

Challenges	Example System(s)	Solution
Settled accuracy of high frequency signals	Motor and Servo control and encoders	Wide Read Cycle decreases required clock rate, enabling a longer quiet window and minimizes ground plane noise
System clock operates at lower speeds to conserve power	Patient Monitoring (ECG, EKG)	
Noisy ground causes voltage reference to be noisy and results in inaccurate conversions	ADC with internal reference voltage	

While communicating with the host processor, the ground plane can experience disturbances which couple into the analog input signal. However the impact of digital switching can be minimized by adjusting the period during which the conversion data is clocked out of the ADC. Transfer during this window of minimal interference is known as “Wide Read Cycle.” A typical SAR ADC ‘frame’ is broken into two cycles: conversion (t_{conv}) and acquisition (t_{acq}), as shown in Figure 1.

During the acquisition cycle, an internal capacitor is being charged to the same voltage as the input signal. At the same time the ADC is clocking out the results of the previous conversion. It is recommended that a ‘quiet time’ be observed at the end of the acquisition cycle, during which no digital communication occurs. If digital switching occurs during this time, it is possible for disturbances in the ground plane to couple back onto the analog input as noise. During the conversion cycle, the ADC will compare the voltage on capacitor to a reference voltage to determine the value of the input signal.

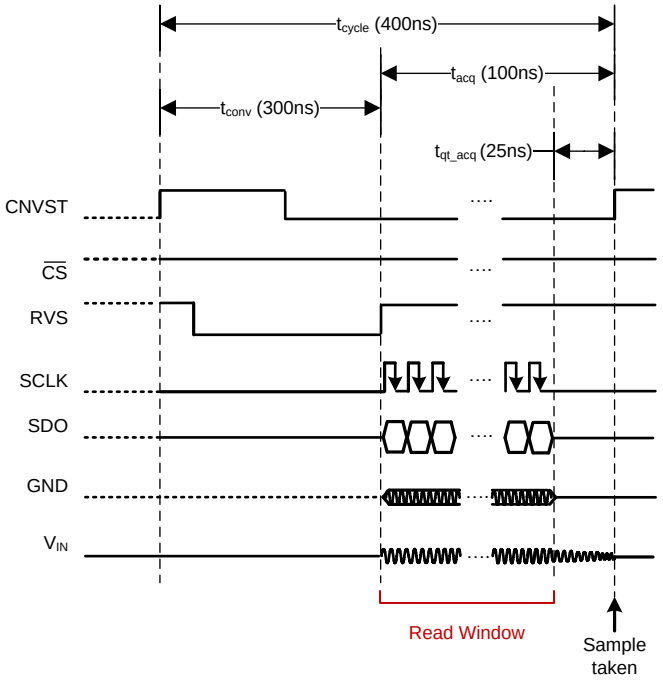

Figure 1. Conversion and Acquisition Cycle of a Typical SAR ADC

While the datasheet of a device specifies the minimum quiet time, some designs such as those with a sensitive ground layout will require a longer quiet period. In some cases, it is possible to increase the clock speed and read the data faster to create a longer quite time. For high-speed (≥1 mega sample per second) and/or high-resolution (≥16 bits) ADCs, this poses a challenge as the clock speed required may not be possible for the chosen host processor or would require a much more expensive one. For example, the ADS9120 is a 16-bit ADC with a cycle time of 400 ns (t_{cycle}), a conversion time of approximately 300 ns (t_{conv}) and a quiet time of 25 ns (t_{qt_acq}). The clock rate can be calculated with the following two equations, which at full throughput is 213.3 MHz.

$$t_{read} = t_{cycle} - t_{conv} - t_{qt\_acq} = 75 \text{ ns}$$

$$f_{sclk} = \frac{\text{resolution}}{t_{read}} = 213.3 \text{ MHz}$$

Not only is a 213.3 MHz clock beyond the capability of most SARs, including the ADS9120 which is limited to an SCLK speed of 75 MHz, it also requires an expensive host processor. However, ADCs enabled with Wide Read Cycle are capable of adjusting when the data is read and even the length of the read window. Specifically it can read the data during the conversion and/or acquisition cycles and change the length of the read window by adjusting the clock speed, as shown in Figure 2.

With Wide Read Cycle, it is possible to significantly increase the quiet time and decrease the clock speed. If the goal is to double the quiet time (50 ns) and decrease the clock speed as much as possible, then equation 1 is updated to equation 3 as t_{conv} is now a part of t_{read}:

$$t_{read} = t_{cycle} - t_{qt\_acq} = 350 \text{ ns}$$

Solving 2 with the new t_{read} value results in a clock rate of 45.7 MHz which is well within the SPI clock speeds of a typical MCU or FPGA.

Although ground sensitivity does not always impact the performance of a data acquisition system, increasing the quiet time will help to ensure more accurate settling and thus better performance. By changing when the data is clocked out of the ADC, Wide Read Cycle enables a longer quiet time and a slower clock rate. This enables high-speed, high-resolution SAR ADCs to be used at full throughput with host processors that otherwise would be unable to provide a fast enough clock speed. To learn more about wide read zone, as well as other features that enable more robust designs with high performance SAR ADCs, be sure to check out the resources section.

Resources

- More information on Wide Read Zone and Other Enhanced SPI Interface Features
- TI Precision Labs – Comprehensive ADC Training
- Analog Engineer Calculator

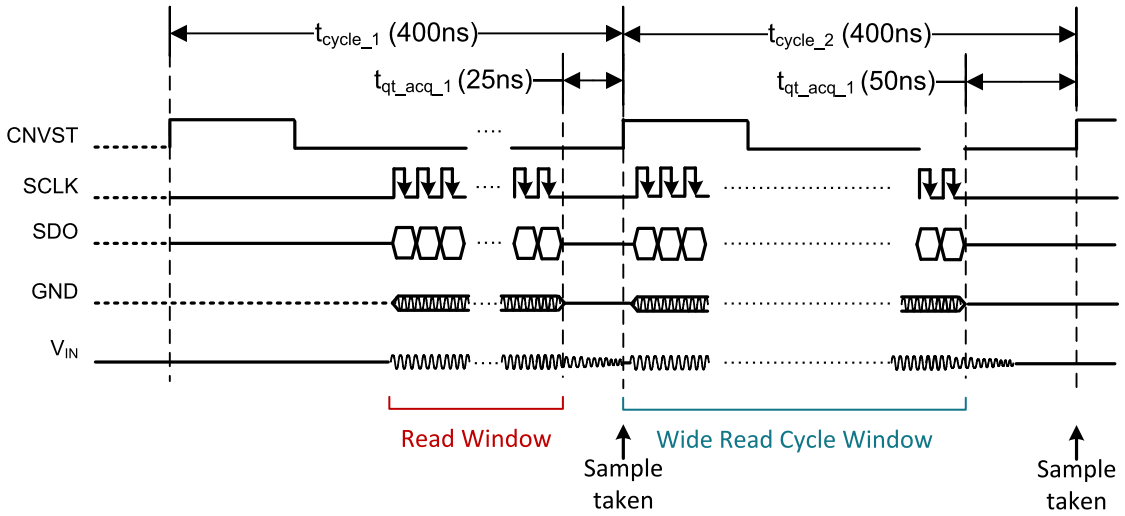

Figure 2. Wide Read Cycle Window versus Traditional Data Read Window

Table 2. High-Speed, High-Resolution SAR ADCs Supporting Wide Read Cycle

Device	Description	Full Throughput SCLK Speed without Wide Read Cycle	Lowest SCLK Speed with Wide Read Cycle
ADS8900B	20-Bit, 1-MSPS SAR ADC with Integrated Reference Buffer and enhanced SPI interface	75-MHz	21-MHz
ADS8910B	18-Bit, 1-MSPS SAR ADC with Integrated Reference Buffer and enhanced SPI interface	67-MHz	19-MHz
ADS8920B	16-Bit, 1-MSPS SAR ADC with Integrated Reference Buffer and enhanced SPI interface	60-MHz	17-MHz
ADS9110	18-Bit, 2-MSPS SAR ADC with enhanced SPI interface	144-MHz	38-MHz
ADS9120	16-Bit, 2.5-MSPS SAR ADC with enhanced SPI interface	214-MHz	43-MHz

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265