Application Report
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Small Cell and Repeater System Using Integrated RF Sampling Device

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ABSTRACT

Recent demand for increasing mobile bandwidth had fueled discussion for 5G wireless network environment which supports very large capacity with very low latency. The ultimate 5G wireless network is suppose to use an ultra wide-band spectrum close to 1GHz. However, reality shows that 5G services start with a relatively narrow bandwidth like 100 – 200MHz and are suppose to coexist with 4G networks for quite a while. Hence, a flexible and scalable platform design which can support a wide range of bandwidth from a few tenths of MHz to 1 GHz range, becomes critical for the future system needs by the Telecom industry.

TI's RF sampling data converter devices (AFE76xx families) integrate four DACs and four ADCs in a chip. The DAC paths modulate the digital stream directly to the RF channel frequency. Similarly, the ADC paths down-convert and sample a RF signal directly to the digital data stream with a high sample rate. Hence, various configurations supporting different bandwidths can be naturally supported by simply changing the configuration of the digital processing blocks.

This application report shows how TI's RF sampling SoC device can be used for a common platform design supporting a 4G and 5G wireless system.

Contents

1 Introduction 3
2 TSW4086 Reference Design 5
3 System Configuration for Small Cell and Repeater 8
4 AFE76xx Configuration or Usecases 11
5 Implementation Choice of Usecase 14
6 Test Results 19

List of Figures

1 AFE76xx with Integrated RF sampling ADCs and DACs 3
2 TSW4086 EVM 5
3 TSW0486 EVM Test Setup 6
4 AFE76xx GUI 7
5 2T2R Configuration 9
6 2T2RnFB FDD Configuration 9
7 4T4R2FB System Case 1 10
8 4T4R2FB System Case 2 10
9 6T6R2FB Diagram 11
10 2T2R2FB TDD Configuration 17
11 RX-to-FBRX Dynamic Switching 17
12 2T2R2FB Configuration for RF Repeater 18
13 RX Path Output with Single Tone at 1750MHz, -15dBFS 19
14 FBRX Path Output with Single Tone at 1750MHz, -15dBFs 19
15 TX Output : 2x20MHz LTE Signal at 2.6GHz 20

16 RX Output : 2x20MHz LTE signal (TX-RX Loopback) at 2.6GHz 20
17 Digital RX-to-TX Direct Loopback : RX input - CW at 450MHz, TX output at 3520MHz 21
18 TX Path Output with Wideband Signal (600MHz) 22
19 FBRX Path Output with Wideband Signal (600MHz) 22
20 RX Mode Output 23
21 FBRX Mode Output 23

List of Tables

1 Example Configurations for 4G Network 9
2 Example Configuration for 5G Repeater 9
3 24410 for 2 Uplink 12
4 14810 for 2 Uplink 12
5 44210 for 2 Uplink or 22210 for 1 Feedback Path 13
6 24410 for 2 Uplink 14
7 42220 for Auto-Switched Feedback Path 14
8 22420 for Auto-Switched Feedback Path 14
9 2T2R2FB 15
10 2T4R 15
11 2T2R 16
12 2T2FB 16
13 2T2R 1/2 Time-Shared FB for Wide Spectrum 16
14 2T2R 2FB for Wide Spectrum 18

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1 Introduction

The Telecom industry has tried to enlarge the coverage and capacity of the wireless network. Most commonly used and discussed technologies include repeater system and Small Cell.

A repeater system is generally used in the cell edge or in an area where the base-station is too far to provide strong enough coverage or where adequate line of sight between the base-station and the service area cannot be established due to some obstacles. The repeater system receives a weak signal from the base-station and re-transmits the amplified version of the received signal or performs signal processing required for communication in the opposite direction. An added repeater efficiently extends the cell coverage. A repeater receiving a RF signal through the air from a base-station is called a RF repeater. While an optic repeater communicates with a base-station through a fiber optic cable.

A Small Cell is an access point with lower transmission power and smaller coverage. Multiple small cells can be deployed under one macro cell. Adding small cells extends coverage as well as increases cell capacity. Depending on coverage and transmit power, small cells are categorized as femtocell, picocell, microcell. Small cells are expected to be widely used in the 5G network system in order to resolve the capacity issue.

The 5G network system standards discuss an ultra wideband spectrum which can be as wide as 1GHz. When the Telecom industry targets first deployment of the 5G network during 2019, systems supporting an intermediate bandwidth like 100MHz to 200MHz are frequently discussed. Long path is still waiting for the ultimate 5G system to become the dominant wireless network. During the transition from 4G to 5G, 4G will coexist with 5G. The wireless network system inevitably needs to support narrow and intermediate spectrums as well as a massively wide spectrum.

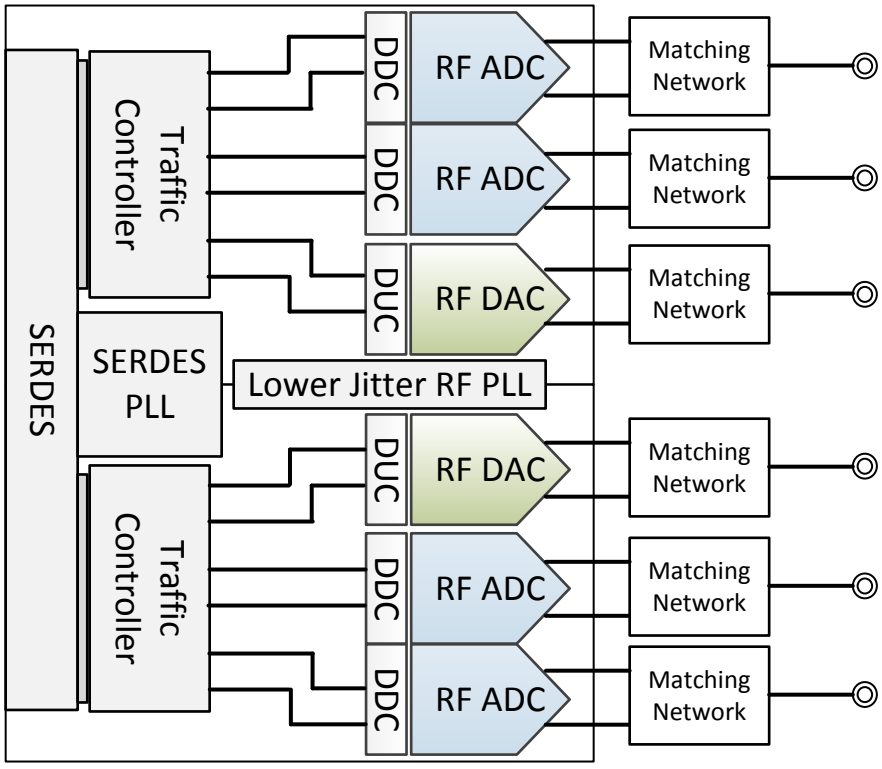

Figure 1. AFE76xx with Integrated RF sampling ADCs and DACs

TI's RF sampling data converter devices (AFE76xx families) integrate four DACs and four ADCs in a chip with two independent SERDES (Serializer/Deserializer) cores for each DAC and ADC pairs. Direct RF sampling technology is used for the DAC and ADC. This technology enables a single device to support different RF bands with different bandwidths flexibly thanks to the embedded digital NCO (Numerically Controlled Oscillator) and various digital filters for sample rate conversion and out-of-band filtering. An

AFE76xx adopts serialization and deserialization (SERDES) logics to deal with multiple data streams with various sample rates. Data from multiple receive paths are efficiently packed into a limited number of high speed serial data lanes. On the other side of the SERDES receiver, the serialized data are unpacked into a multi-bit parallel data stream with lower sample rate. These features make the AFE76xx well qualified for a scalable system design with different design and usecase requirements.

AFE76xx Features include:

- Integrated 14-bit DACs and ADCs
- Digital NCOs for up-conversion and down-conversion
- Digital filter for interpolation and decimation processing
- Eight independent SERDES lanes for DAC and ADC paths supporting SERDES lane rates up to 15Gbps
- Heterogeneous or homogeneous SERDES lane rate support between an ADC and DAC
- Heterogeneous or homogeneous SERDES lane rate support between ADC cores

1.1 AFE76xx Family Devices

Device	Supported Channels	# of DUC per TX Channel	# of DDC per Channel	Maximum Bandwidth
AFE7683	2T4R	1	1	<600MHz
AFE7684	2T4R	2	2	<1200MHz
AFE7685	4T4R	1	1	<600MHz
AFE7686	4T4R	2	2	<1200MHz

2 TSW4086 Reference Design

A TSW4086 design targets 2T2R, 2T2R1FB, or 2T2R2FB systems frequently used in small cell and repeater designs. The design has a small form factor compared to a reference EVM for a 4T4R system. Power for the TSW4086 is provided by a daughter board, TSW2086, which is attached at the bottom of the TSW4086 through a connector.

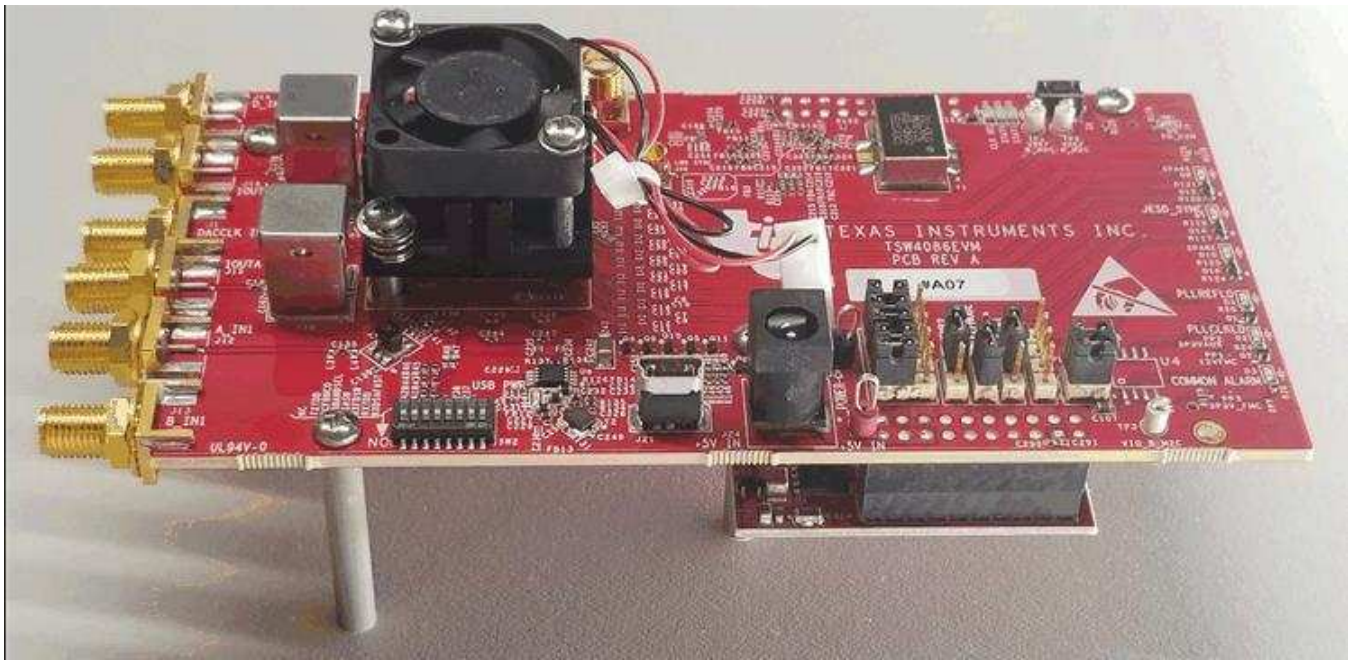

Figure 2. TSW4086 EVM

2.1 TSW4086 EVM Setup

A TSW4086 has a single AFE76xx device on board. A LMK04610 provides a JESD204B compliant clock with very low clock jitter using dual loop PLLs. The first PLL locks to an on-board VCXO frequency of 122.88MHz. The second PLL locks to a few GHz clock and reference clocks for the AFE76xx device as well as FPGA are generated. The internal RF PLL in an AFE76xx synthesizes a low noise 9-GHz or 6-GHz clock for the on-chip data converters and a divided clock is provided to the SERDES PLL as a reference clock.

Either a TSW14J56 or TSW14J57 is used to either capture ADC output data or feed data to the DAC. A LMK04610 also provides the reference clock and SYSREF signal to the FPGA on the TSW14J5x.

LMK04610 Features include:

- Dual loop PLL architecture for low jitter
- JESD204B support
- 10 differential output clocks in 8 frequency groups
- 2 selective reference clock inputs
- <1W typical power consumption

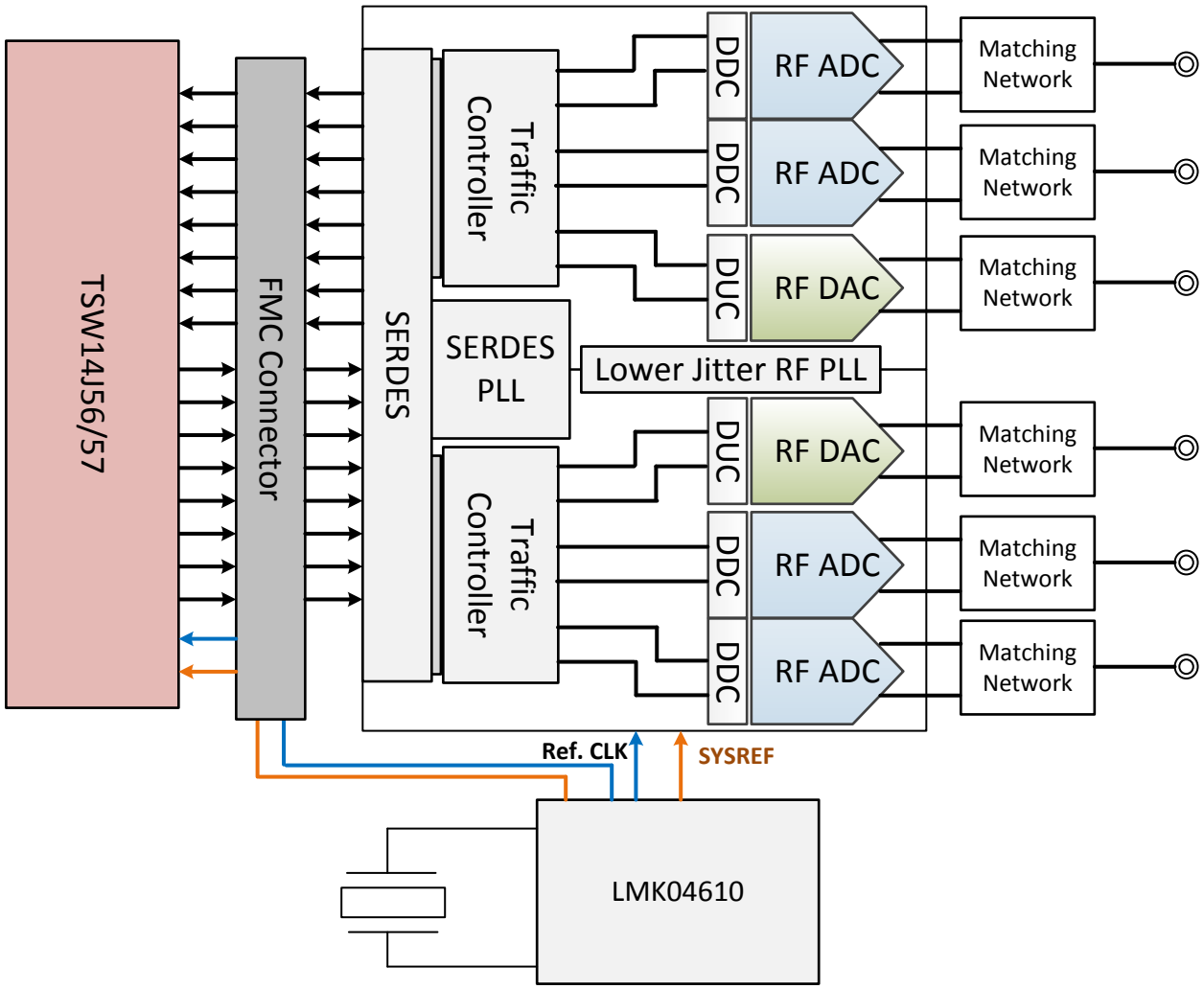

Figure 3. TSW0486 EVM Test Setup

2.2 TSW4086 Programming

The TSW4086 EVM is programmed through the AFE76xx GUI. This software supports both the AFE76xx EVM and TSW4086. The LMK04610 is programmed to generate a FREF clock of 368.64MHz to the AFE76xx. A reference clock to the FPGA in the TSW14J56/7 is also generated. The usecase of the AFE76xx can be programmed according to the settings in the 'RX/TX Dig Path Config' and 'JESD Settings' section. The number of DAC and ADC channels can be set through the AFE76xx RX and TX tabs especially for a 2T2RnFB configuration with lower power consumption. The Nyquist zone where the ADCs are supposed to be optimally trimmed can be set through the AFE76xx RX tab also.

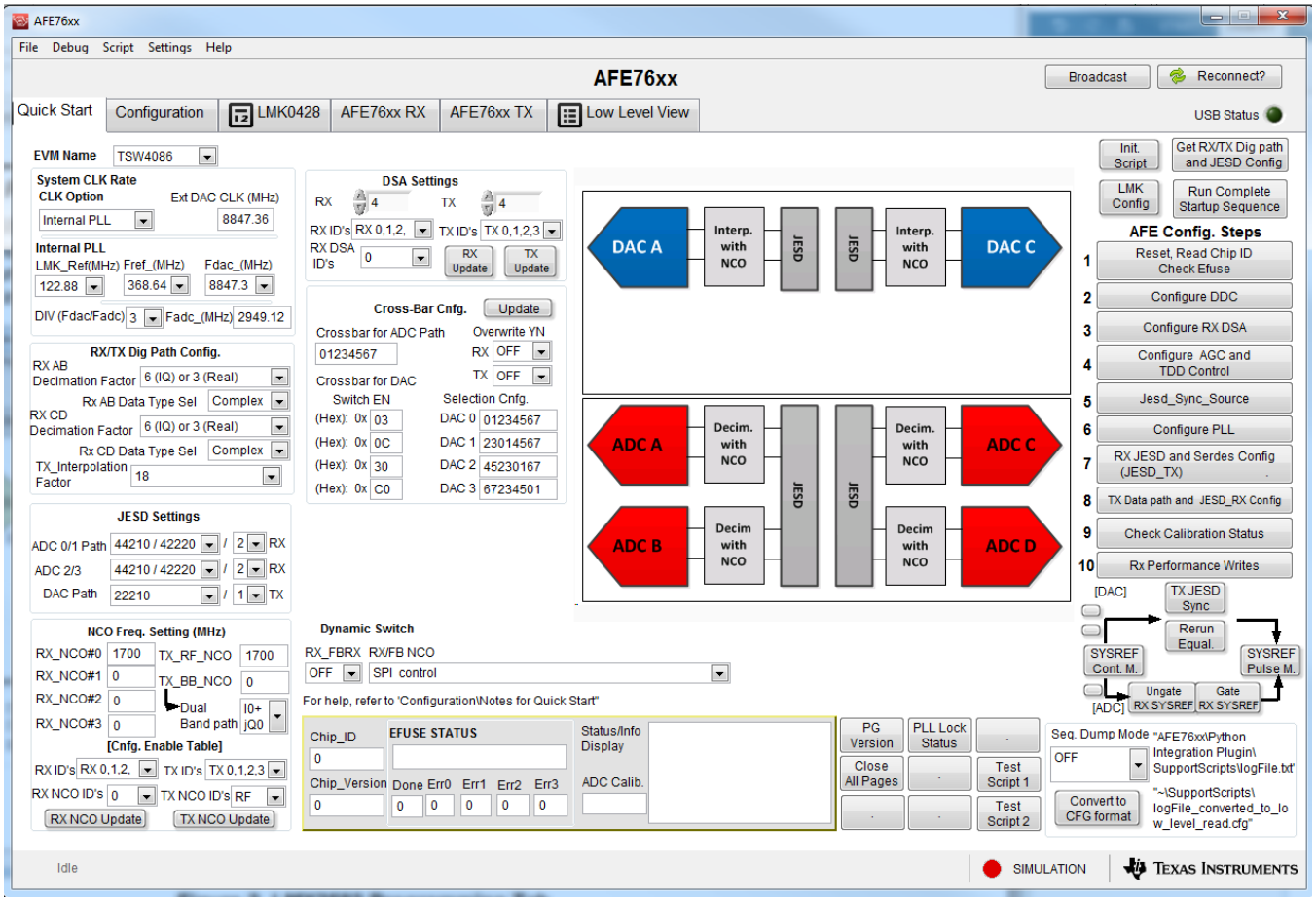

Figure 4. AFE76xx GUI

3 System Configuration for Small Cell and Repeater

For 4G and 5G small cell and repeater systems, the configurations mostly discussed are a 2T2R system. Depending on the target application, the integrated bandwidth can be as narrow as 20MHz and as wide as several hundreds MHz. Depending on the Transmit power level, DPD (Digital Pre-Distortion) may need to be used. Mostly, 3x bandwidth is considered for the spectral regrowth by PA (Power Amplifier).

4G LTE system

LTE is still the most widely adopted communication standard in the field. This standard supports a single carrier whose bandwidth ranges from 1.4MHz to 20MHz. In the advanced LTE network, two or three carriers can be aggregated to enhance the data rates. In these cases, the supported signal BW becomes 40 or 60MHz respectively. For the receive path, a sample rate of 122.88MHz is wide enough to support these signal bandwidths. While the transmit path may need to support a wider bandwidth, which is three or five times wider than the RX signal bandwidth depending on the DPD requirement. Mostly, the baseband sample rate of the transmit path can be either 368.64MHz or 491.52MHz to provide as wide a bandwidth as 300MHz. In a FDD system, a dedicated receiver (Feedback RX) needs to be allocated to monitor the TX output signal. In a TDD system, the same receive path can be time-shared for the TX monitoring purpose. The bandwidth requirement of the TX monitoring receiver should be the same as the bandwidth of TX. In a system with low transmit power, a PA linearization technique is not necessary. No receive path is supposed to be assigned for TX output monitoring.

5G System

For a 5G system, TDD platform supporting IBW of 100MHz or 200MHz is normally discussed for the first deployment during 2019 at 3.5GHz band. For outdoor applications with high transmit power, three times of IBW needs to be supported for DPD operation. This results in 600-MHz bandwidth support by the transmit and TX monitoring receive path. On top of the currently emerging system requirements, service providers prefer to make the platform flexible enough so that the system can be scaled up for wider IBW support in the future. For this system, the RX sampling rate needs to be at least 368.64MHz or higher. While the sampling rate of the TX path needs to be at least 737.28MHz or as high as 983.04MHz.

In the example for a LTE system, the sampling rate of the baseband data stream is low. Also, the data rate of the traffic receiver is four times slower than the data rates of other paths (TX and FBRX). The asymmetric bandwidth requirement between RX and TX and FBRX may give multiple options to a system engineer depending on the following design constraints:

- Required number of SERDES lanes for uplink and downlink
- Supportable SERDES lane rate on FPGA
- Supported JESD mode
- Board area available for SERDES lanes

One option for the SERDES interface of the uplink might be to use a lower SERDES lane rate, while using more SERDES lanes. Another option is to increase the SERDES lane rate so that more data can be packed into one lane resulting in a smaller number of SERDES lanes. Depending on board layout constraints and available features on the FPGA side, the system engineer is supposed to determine which option is preferred for the target platform.

While, a wideband system like a 5G system does not give many alternative options since a data stream with a high data rate inevitably requires many SERDES lanes. Even though a similar consideration can be applied.

In the following sections, example systems like 2T2R, 2T2RnFB, 4T4RnFB, and 6T6RnFB are selected to show how an AFE76xx can be used flexibly for both narrow and wide IBW systems.

3.1 Example Usecases

The table below shows a few configurations discussed for small cell or repeater applications for a 4G and 5G network. The first usecase is a 2T2R2FB system supporting up to 60MHz IBW. The other two usecases are extended versions for a 4T4R or 6T6R system using a variation of the 2T2RnFB configuration. Here, mainly a FDD usecase is discussed. For TDD operation, the same receive path can be time-shared for a TX monitoring path. This operation is seamlessly supported by AFE76xx devices according to the state of TDD triggers.

Table 1. Example Configurations for 4G Network

Usecase	Uplink	Downlink	Feedback RX	Duplex	IBW
2T2R2FB_NB	2	2	2	FDD	≤100MHz to cover x3 DPD BW or ≤60MHz to cover x5 DPD BW
4T4R2FB_NB	4	4	2	FDD	≤100MHz to cover x3 DPD BW or ≤60MHz to cover x5 DPD BW
6T6R2FB_NB	6	6	2	FDD	≤100MHz to cover x3 DPD BW or ≤60MHz to cover x5 DPD BW

The table below shows the two example systems for a 5G repeater application. As discussed earlier, 100-200 MHz IBW is supposed to be supported. Even though there are more discussion to support wider bandwidth, two example usecases below are discussed in this article.

Table 2. Example Configuration for 5G Repeater

Usecase	Application	Uplink	Downlink	Feedback RX	Duplex	IBW
2T2R2FB_WB	Optic Repeater	2	2	2	TDD	~200MHz
2T2R2FB_WB	RF Repeater	2	2	2	TDD	~200MHz

3.2 System Block Diagram for Example Usecases

In the previous section, multiple system usecases are introduced from 2T2R to 6T6R systems. Even though some systems like 6T6RnFB may require multiple AFE76xx devices, all of the usecases can be constructed using few baseline configurations like

- 2T2R or 2T2FB
- 2T4R
- 2T2R2FB
- 4T4R

Figure 5 - Figure 9 shows how each usecase can be implemented using one or two baseline configurations. In the following system block diagrams, blue colored SERDES IP shows the higher speed interface, while orange colored SERDES IP represents lower speed interface.

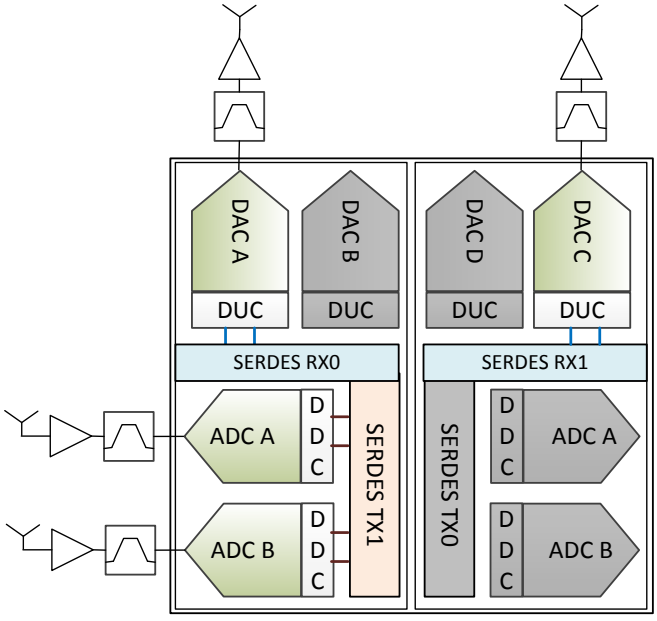

Figure 5. 2T2R Configuration

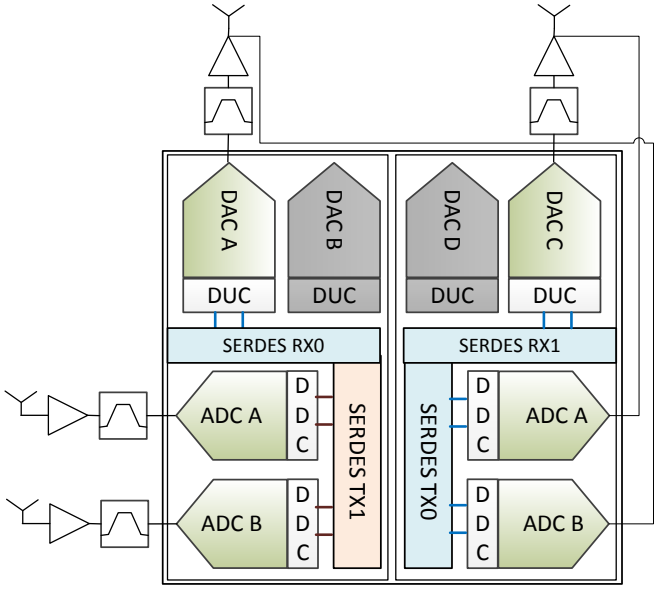

Figure 6. 2T2RnFB FDD Configuration

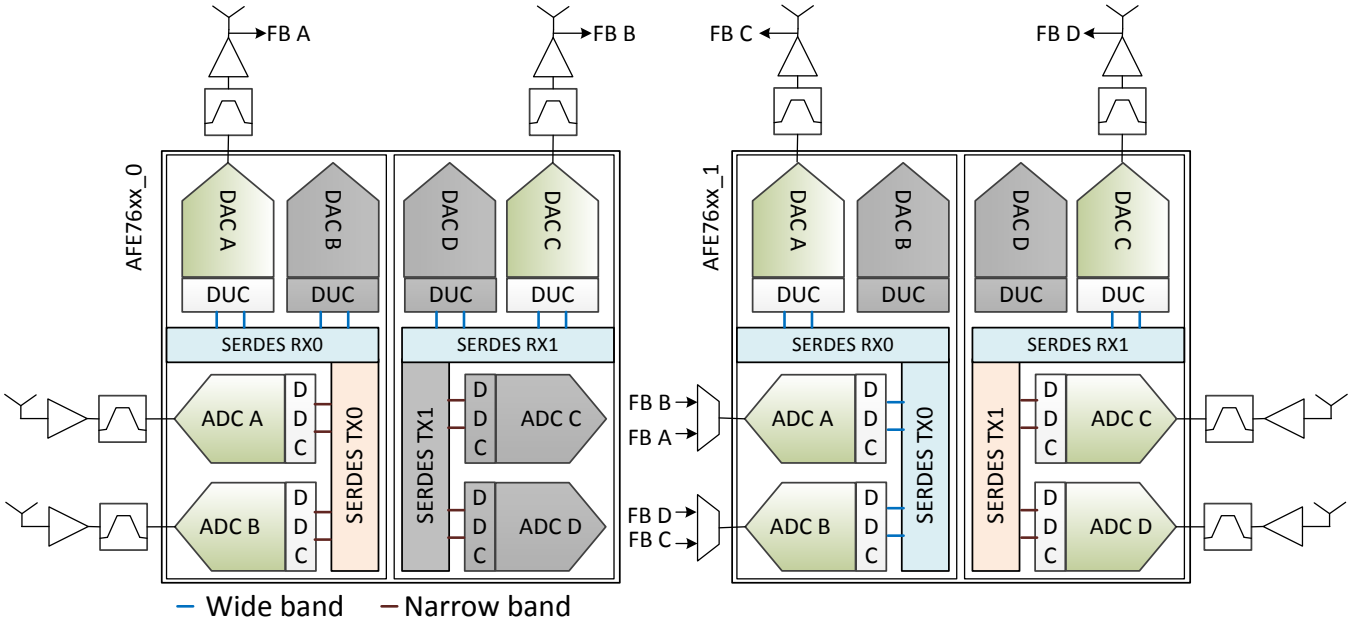

Figure 7. 4T4R2FB System Case 1

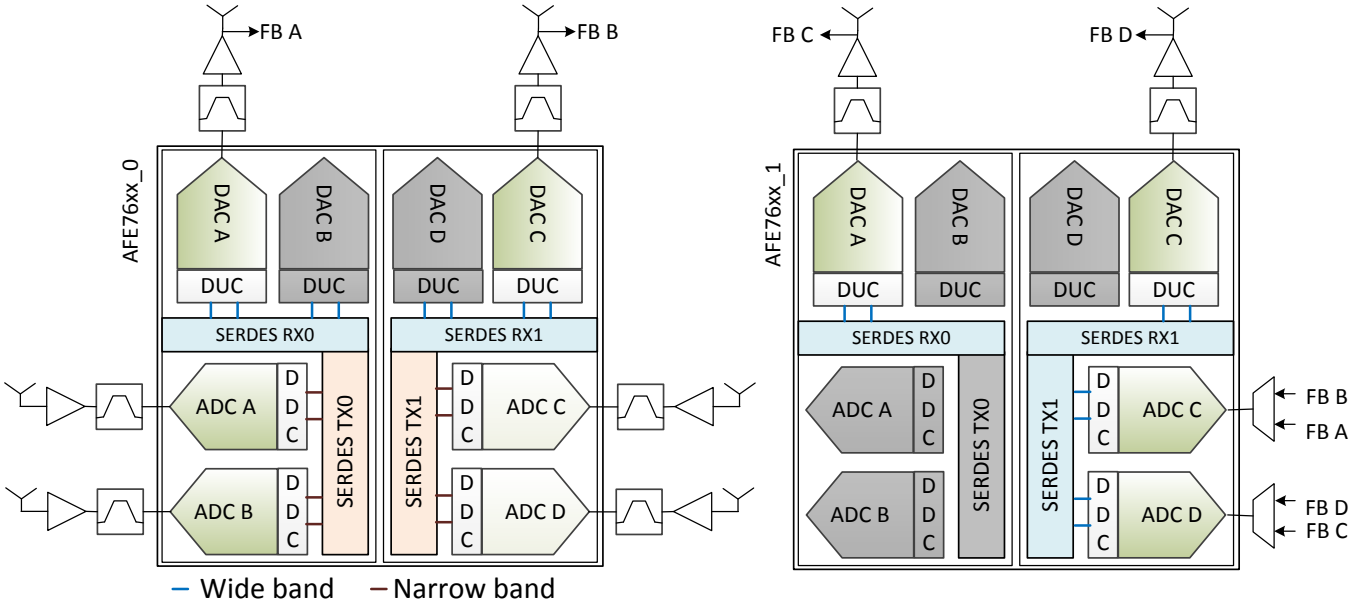

Figure 8. 4T4R2FB System Case 2

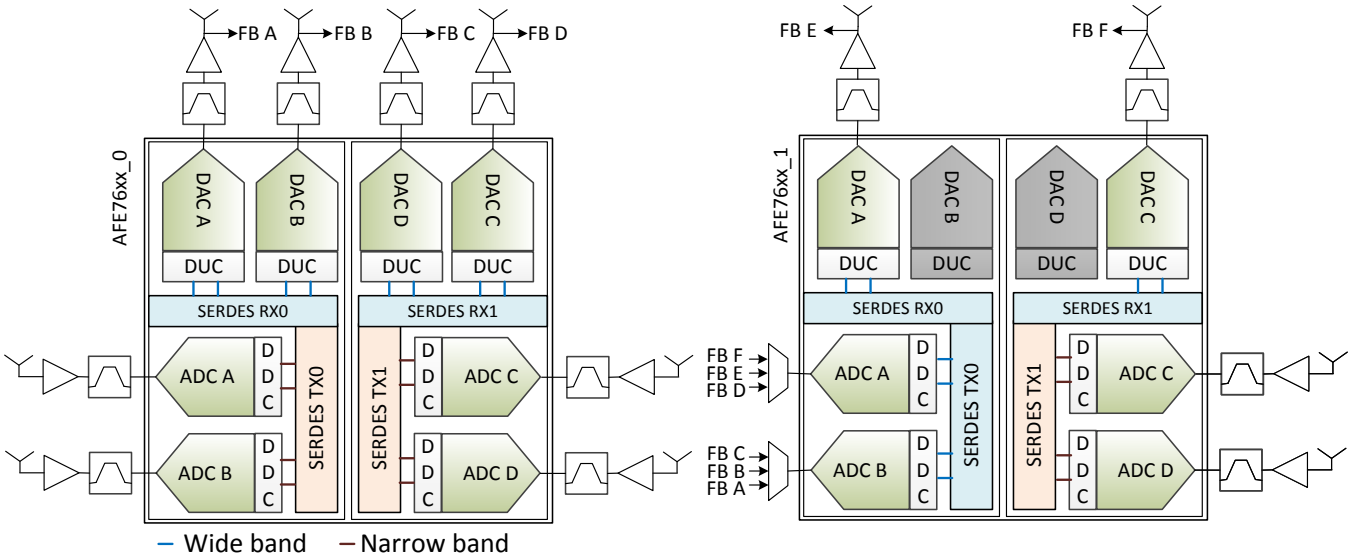

Figure 9. 6T6R2FB Diagram

Among above configurations, all 2TxRnFB configurations except 4T4R can be implemented with TSW4086 TI Design. In the following section, we will show how the baseline configurations having two transmitter can be implemented for each target applications.

- 2T2R
- 2T4R
- 2T2FB
- 2T2RnFB

4 AFE76xx Configuration or Usecases

4.1 Configuration Options for 4G Usecase

4.1.1 Clocks and Sampling rates

The RF sampling ADC and DAC in an AFE76xx have digital data path blocks providing decimation and interpolation features. These data paths only ensure a passband whose bandwidth is about 82% of the complex signal sampling rate. Hence, in order to ensure the following conditions,

- Maximum BW for Uplink = 100MHz when 3x BW is used for DPD operation
  or
- Maximum BW for Uplink = 60MHz when 5x BW is used for DPD operation

the sampling rate of uplink and downlink can be

- Sampling rate of Uplink data = 122.88MHz
- Sampling rate of Downlink data = 491.52MHz
- Sampling rate of feedback data path = 491.52MHz

As digital baseband sample rates are decided for the ADC and DAC, the sampling rates of the DAC and ADC are supposed to be determined. Since the RF sampling technique is different from the Nyquist DAC and ADC, the user needs to understand the limitations of the RF sampling DAC and ADC. The following items need to be considered to determine the sampling clock rate of the RF sampling data converters.

- The uplink and downlink band to be supported should not be placed across two Nyquist zones of ADC or DAC.
- To avoid image signal issues, the signal needs to be placed with a proper guard band between the edge of the signal band and Nyquist zone boundary.

- The folding of higher order distortion terms and their mixing components with clock and interleave spurs need to be placed away from the signal band.

The first condition comes from the real sampling operation of the RF sampling data converter. For example, consider a system which needs to down-convert a 40-MHz BW signal at the RF channel of 2.51GHz . If the RF sampling ADC is clocked by a 2.5-GHz clock, sampling theory says that all Nyquist zones are folded on to the 1st Nyquist zone which is DC to 1.5GHz. A 40-MHz BW signal exists across the Nyquist zone and some part of the signal itself is to be folded on top of another part of the signal by the sampling process. Hence, the entire signal needs to exist within a Nyquist zone.

The second condition is also required due to sampling operation. Assume a signal is up-converted to 3.5GHz and the DAC is running at 6GHz. Then, in addition to the up-converted 3.5GHz signal, the DAC will generate an image signal at 2.5GHz. To suppress this image, an RF bandpass filter is supposed to be used. Hence, the wider the frequency gap between the signal and image becomes, the easier to filter out the image signal. Similarly, ADC sampling is supposed to sample an undesired signal at the image frequency to the signal frequency. Hence, before RF ADC sampling, the image band needs to be suppressed enough.

The third condition is critical since high order distortions are also folded back to the 1st Nyquist zone by ADC operation. If higher order distortion terms are not low enough, these can be mixed with ADC clock spurs and undesired spurs can appear near the band. This issue can be avoided either by suppressing the high order distortions low enough or by using careful frequency planning so that folded spurs appear away from the signal band.

Here, the DAC is assumed to be run by a 8847.36-MHz clock and the ADC is supposed to be run by a clock which is divided by 3 from the DAC clock without loss of generality.

4.1.2 Digital Datapath and JESD Modes

The ADC is running at 2949.12MHz, while the sampling rate of the input data is 122.88MHz. This results in a decimation rate of 24 (ADC sampling rate / input data sampling rate). In a similar way, the required interpolation rate is computed to be 18 from 8847.36MHz/491.52MHz. While, the baseband data rate of the feedback receiver is the same as the input data rate of the transmitter. Hence, the decimation ratio for the feedback receiver needs to be 6 (2949.12MHz/491.52MHz).

For the downlink, JESD mode of 22210 for 1 TX (44210 for 2 TX) results in a SERDES lane rate of 9830.4Mbps. Since an AFE76xx supports a SERDES lane rate up to 15Gbps, 22210 for 1 TX is only one choice among the allowed JESD modes. In similar fashion, the feedback receive path is supposed to use the JESD mode of 44210/2RX.

The uplink data rate is four time lower than that of other paths. Hence, if the same number of SERDES lanes as other data paths is used, a 2.5Gbps SERDES lane rate can deliver a real data stream of each uplink data. If a SERDES lane is doubled, two SERDES lanes are enough to handle complex data streams from two uplink data paths. JESD mode of 24410/2RX can be used resulting in a 5Gbps SERDES lane rate. If only one SERDES lane is available for the uplink, the SERDES lane rate can again be doubled for 10Gbps. JESD mode of 12410/2RX corresponds to this configuration.

Table 3. 24410 for 2 Uplink

Octet	1	2	3	4
Lane STX0	Uplink A_i0		Uplink A_i1	
Lane STX1	Uplink B_i0		Uplink B_i0	

Table 4. 14810 for 2 Uplink

Octet	1	2	3	4
Lane STX0	Uplink A_i0	Uplink A_i1	Uplink B_i0	Uplink B_i0

In the previous section, a few generic usecases were introduced which are used to build a 4T4RnFB or 6T6RnFB system.

- 2T2R or 2T2FB
- 2T4R
- 2T2R2FB
- 4T4R

These usecases can be implemented by putting together the configurations described in following table.

Design Option	JESD Mode	SERDES Lane Rate
Uplink	24410 (/2RX)	5Gbps
	14810 (/2RX)	**10Gbps**
Downlink	44210 (/2TX)	10Gbps
Feeback Path	44210 (/2RX)	10Gbps

4.2 Configuration Options for 5G Usecase

4.2.1 Clocks and Sampling rates

For the 5G usecase, the difference comes from wide bandwidth support. Support of a 200-MHz bandwidth with DPD requires at least 600-MHz support. Since the sample rate is restricted to be an integer times 61.44MHz, the sampling rates of the uplink and downlink need to be:

- Sample rate of Uplink data = 368.64MHz or 491.52MHz
- Sample rate of Downlink data = 737.28MHz or 983.04MHz

The sample rate of the feedback path should be the same as the sample rate of the downlink.

For the 5G usecase also, the DAC is considered to be clocked at 8847.36MHz and the ADC clock rate is one third of the DAC clock rate.

4.2.2 Digital Datapath and JESD Modes

For the sample clock rate for the ADC as stated before, a decimation rate of 8 is used for a 368.64-MHz baseband sample rate. An interpolation rate of 12 for the DAC path results in a baseband sample rate of 737.28MHz.

For this wideband spectrum, eight SERDES lanes are supposed to be used for the downlink path. JESD mode of 84111 meets the requirements with JESD mode of 44210 for the uplink path. Since the ADC output sample rate is half of the DAC path, use of four SERDES lanes is supposed to result in the same SERDES lane rate which is 7.5Gbps. If the SERDES lane rate can be doubled to 15Gbps, only two SERDES lanes are enough for the complex data stream from two uplink paths.

For the TX monitoring path, there are two different cases. If 2T2R are operated in TDD, the same ADC path which is used for the uplink path, can be time-shared for the TX feedback path. The JESD mode is auto-switched to 42220 mode if the JESD mode of the uplink is 44210. The SERDES lane rate will still be 7.5Gbps. If the uplink path uses the JESD mode of 24410, the JESD setting is auto-switched to 22420 and the SERDES lane rate remains the same, 15Gbps. For both scenarios, the sample rate of the feedback RX is increased to 737.28MHz. This usecase can be used for an optic repeater.

While, uplink and downlink paths are seamlessly used for an RF repeater. Hence, the TX feedback path cannot be time-shared with the uplink ADC path. For this application, the JESD mode of 22210 needs to be used for one feedback path. The SERDES lane rate will be 15Gbps.

Table 5. 44210 for 2 Uplink or 22210 for 1 Feedback Path

Octet	1	2
Lane STX0	Uplink A_i0 or FBRX_A_i0	
Lane STX1	Uplink A_q0 or FBRX_A_q0	

Table 5. 44210 for 2 Uplink or 22210 for 1 Feedback Path (continued)

Octet	1	2
Lane STX2	Uplink B_i0	
Lane STX3	Uplink B_q0	

Table 6. 24410 for 2 Uplink

Octet	1	2	3	4
Lane STX0	Uplink A_i0		Uplink A_q0	
Lane STX1	Uplink B_i0		Uplink B_q0	

Table 7. 42220 for Auto-Switched Feedback Path

Octet	1	2
Lane STX0	FBRX_i0 from 1st sample 0	
Lane STX1	FBRX_i0 from 1st sample 1	
Lane STX2	FBRX_q0 from 1st sample 0	
Lane STX3	FBRX_q0 from 1st sample 1	

Table 8. 22420 for Auto-Switched Feedback Path

Octet	1	2	3	4
Lane STX0	FBRX_i0 from 1st sample 0		FBRX_i0 from 1st sample 1	
Lane STX1	FBRX_q0 from 1st sample 0		FBRX_q0 from 1st sample 1	

A 5G repeater application requires 2T2R with one or two Feedback paths. For mission mode, it will be operated in TDD. However, there is a difference between two usecases: Optic repeater and RF repeater An optic repeater operated in TDD mode can share receive path for TX monitoring purpose. While, an RF repeater is supposed to use a pair of a receiver and a transmitter simultaneously for uplink and downlink, a dedicated receiver for TX monitoring path might be preferred for simplicity of design.

These usecases can be implemented by putting together the configurations described in the following table.

Design Option	JESD Mode	SERDES Lane Rate	Note
Uplink	44210 (/2RX)	7.5Gbps	
	24410 (/2RX)	15Gbps	
Downlink	84111 (/2TX)	7.5Gbps	
Auto-switched Feedback Path	42220 (/1FB)	7.5Gbps	Paired with 44210
	22420 (/1FB)	15Gbps	Paired with 24410
Static Feedback Path	22210 (/1FB)	15Gbps	

5 Implementation Choice of Usecase

SERDES IP used by AFE76xx devices support the following usecases:

- Different SERDES lane rate between TX and RX paths
- Different SERDES alternate between ADC paths in different ADC Cores

Arbitrary SERDES lane rates cannot be matched for different data paths. Considering the ratio between the highest SERDES lane rate and another SERDES lane rate, there are few options supported. They are full rate, half rate, and quarter rate. Half rate mode means the slower SERDES lane rate is half of the fastest SERDES lane rate. For example, a TX SERDES lane rate of 10Gbps can be matched with a 5Gbps RX SERDES lane rate in half rate mode. Or, ADC path A and B can use a 10Gbps SERDES lane rate, while ADC path C and D can run at 5Gbps in half rate mode. Similar logics can be applied to full rate mode and quarter rate mode.

If any SERDES lane rate uses a rate mode other than full rate mode, the case is referred to as a 'heterogeneous SERDES usecase'. While 'homogeneous SERDES usecase' means all SERDES lane rates are the same meaning only full rate mode is used for both uplink and downlink paths. The platform designer needs to choose one of the two usecases while considering board layout and FPGA features.

5.1 2T2R2FB Narrowband Usecase

Since the downlink path normally requires wider bandwidth than the uplink path, there is only one option for the downlink path and feedback paths depending on the TX baseband sample rate. While there are two options for the uplink. One option uses two SERDES lanes for two uplink paths. In this usecase, the SERDES lane rate of the uplink uses half rate mode. On the other hand, the SERDES lane rate for the uplink can be increased so that the same SERDES lane rate of 10Gbps can be achieved. This configuration results in a lower number of SERDES lanes compared to Case 1.

Table 9. 2T2R2FB

Design Option	Case 1		Case 2	
	JESD Mode	SERDES Lane Rate	JESD Mode	SERDES Lane Rate
Uplink	24410	5Gbps	14810	10Gbps
Downlink	44210	10Gbps	44210	10Gbps
Feedback Path	44210	10Gbps	44210	10Gbps
Number of SERDES Lanes	10		9	

From the aspects of power consumption and board layout, a system designer may prefer Case 2 where a lower number of SERDES lanes are used. While, JESD mode of 14810 packs two complex data streams into a single SERDES lane, the FPGA should support correct unpacking in order to avoid a data swap between I and Q or between two uplink paths. Depending on the available features of JESD/SERDES on the FPGA side, a system engineer may prefer to implement Case 1 even though it is a heterogeneous SERDES case requiring more SERDES lanes.

5.2 2T4R Narrowband Usecase

The 2T4R usecase can be used when designing a 4T4R2FB system. Based on the same reasoning described for the 2T2R2FB usecase, there are two options as shown in the following table.

Table 10. 2T4R

Design Option	Case 1		Case 2	
	Jesd Mode	SERDES Lane Rate	Jesd Mode	SERDES Lane Rate
Uplink	24410	5Gbps	14810	10Gbps
Downlink	44210	10Gbps	44210	10Gbps
Number of SERDES Lanes	8		6	

5.3 2T2R Narrowband Usecase

Similar thought process also gives two implementation choices for 2T2R as shown below.

Table 11. 2T2R

Design Option	Case 1		Case 2	
	JESD Mode	SERDES Lane Rate	Jesd Mode	SERDES Lane Rate
Uplink	14810	10Gbps	24410	5Gbps
Downlink	44210	10Gbps	44210	10Gbps
Number of SERDES Lanes	5		6	

5.4 2T2FB Narrowband Usecase

For the 2T2FB usecase, only one option exists since both paths need to be run at the highest SERDES lane rate.

Table 12. 2T2FB

Design Option	JESD Mode	SERDES Lane Rate
Uplink	44210	10Gbps
Downlink	44210	10Gbps
Number of SERDES Lanes	8	

5.5 5G Optic Repeater Usecase (2T2R with 1/2 FB TDD Mode)

For the optic repeater usecase supporting a wideband spectrum up to 600MHz, the downlink path needs to use four SERDES lanes for each TX path. JESD mode of 84111 will satisfy this requirements. While the uplink path can use either 44210 or 24410 mode. As stated, 44210 results in the same SERDES lane rate as the TX path, 7.5Gbps. While 24410 will double the SERDES lane rate requiring 15Gbps support from the FPGA.

The 5G usecases that have been discussed are mostly TDD operation. For TDD operation, a user does not need to consider additional SERDES lanes for feedback paths. An AFE76xx supports 'dynamic switching' between RX and FBRX modes according to GPIO signals (RXTDD and RXFBSW). In RX mode, two data streams with lower sample rates are processed by JESDTX logic. For the example of optic repeater case 1, the baseband sample rate will be 368.64MHz and four SERDES lanes are occupied by two complex data streams from two ADC paths. If FBRX mode is triggered, one ADC path is set to inactive mode and only one path is activated with a lower decimation rate. Since FBRX needs to support a 737.28MHz sample rate for this application, the decimation rate is reduced to four from eight. While the complex data stream with a two-times higher sample rate will occupy all activated SERDES lanes. In this operation, there is no need for the SERDES lane rate to be changed.

As shown in the below table, use of a higher SERDES lane rate can reduce the number of SERDES lanes on board by two. Of course, FPGA should be able to support the compatible SERDES lane rate mode.

Table 13. 2T2R 1/2 Time-Shared FB for Wide Spectrum

Design Option	Case 1		Case 2	
	JESD Mode	SERDES Lane Rate	JESD Mode	SERDES Lane Rate
Uplink	44210	7.5Gbps	24410	15Gbps
Downlink	84111	7.5Gbps	84111	7.5Gbps
Number of SERDES Lanes	12		10	

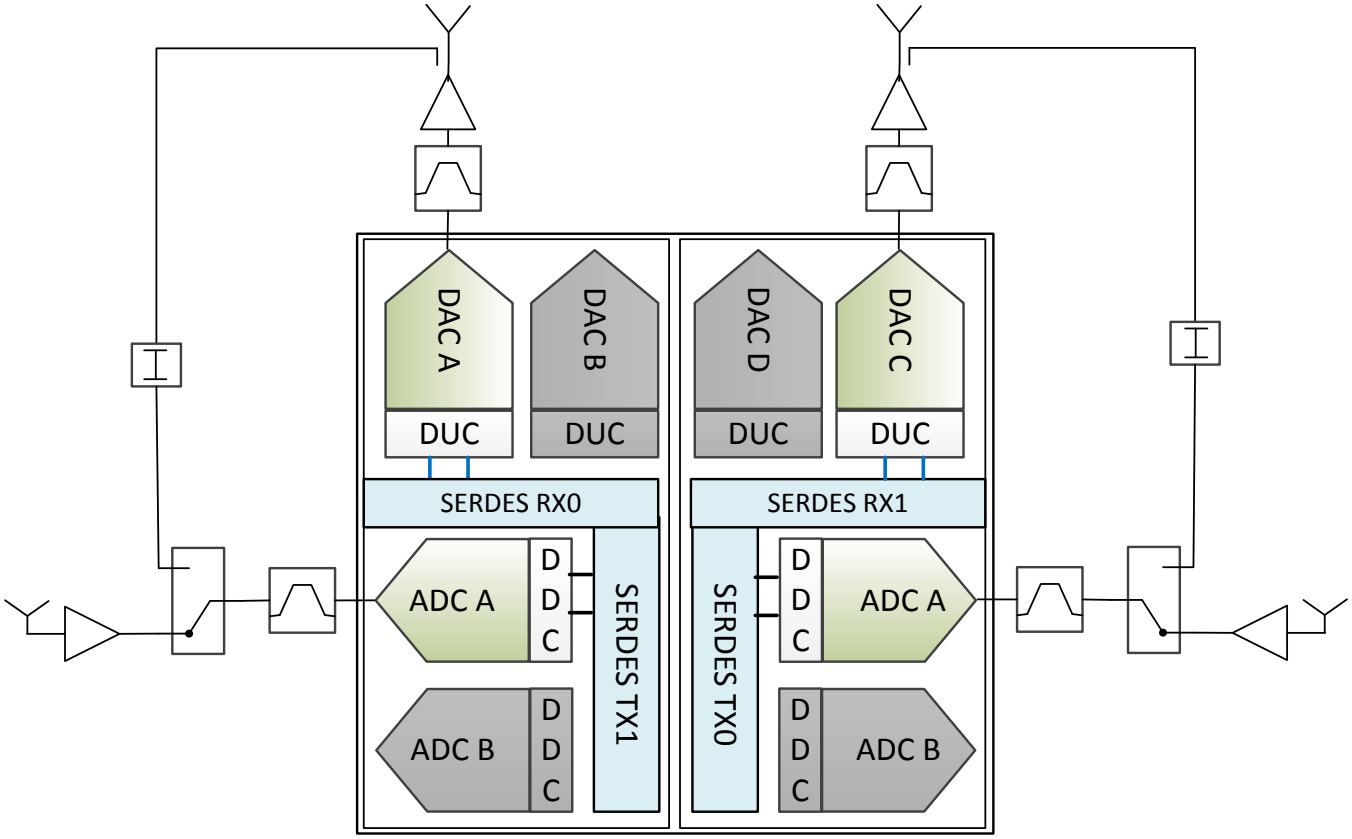

Figure 10. 2T2R2FB TDD Configuration

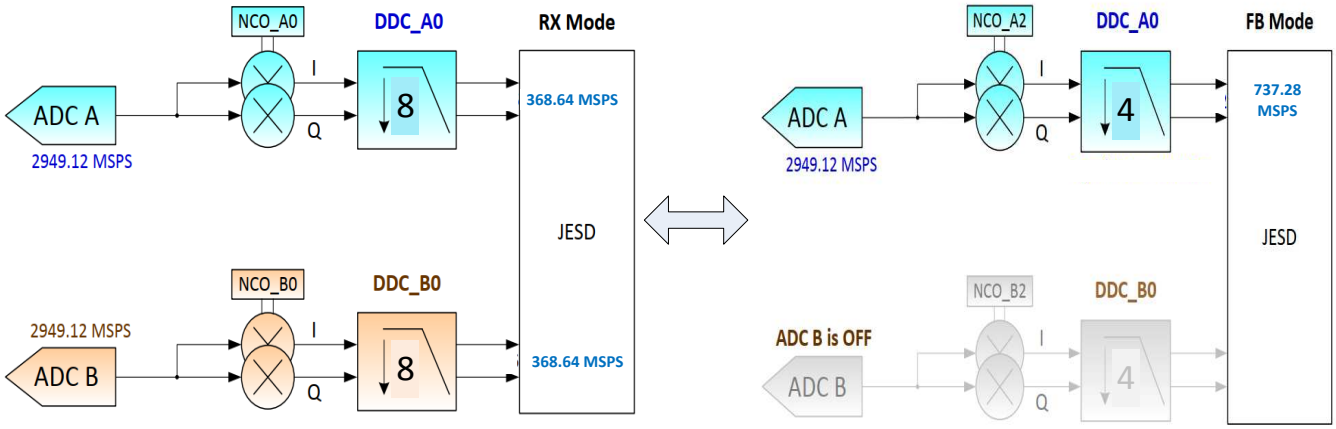

Figure 11. RX-to-FBRX Dynamic Switching

5.6 5G RF Repeater Usecase (2T2R 1/2 FB)

The 5G RF repeater usecase is similar to FDD operation since one pair of ADC paths needs to process the signal from the base station. While, the TX (DAC) paths and additional one or two ADC paths are used for re-transmitting of the received signal simultaneously. Hence, additional ADC paths need to be assigned as dedicated feedback paths. Since the feedback path is supposed to support 600-MHz bandwidth, the sample rate of the complex data stream is double that of the uplink data paths. Using the same JESD mode as the uplink path results in a two-times higher SERDES lane rate.

While the uplink paths have two options as shown in the following table. Case 1 shows a heterogeneous SERDES usecase among JESD TX cores. Case 2 shows a homogeneous SERDES usecase among receive paths.

For the 2T2R2FB usecase, case 1 requires 16 SERDES lanes and 14 SERDES lanes are used for case 2.

Table 14. 2T2R 2FB for Wide Spectrum

Design Option	Case 1		Case 2	
	JESD Mode	SERDES Lane Rate	JESD Mode	SERDES Lane Rate
Uplink	44210 (/ 2RX)	7.5Gbps	24410 (/ 2RX)	15Gbps
Downlink	84111	7.5Gbps	84111	7.5Gbps
Feedback Path	22210 (/ 1FB)	15Gbps	22210 (/ 1FB)	15Gbps
Number of SERDES Lanes	16		14	

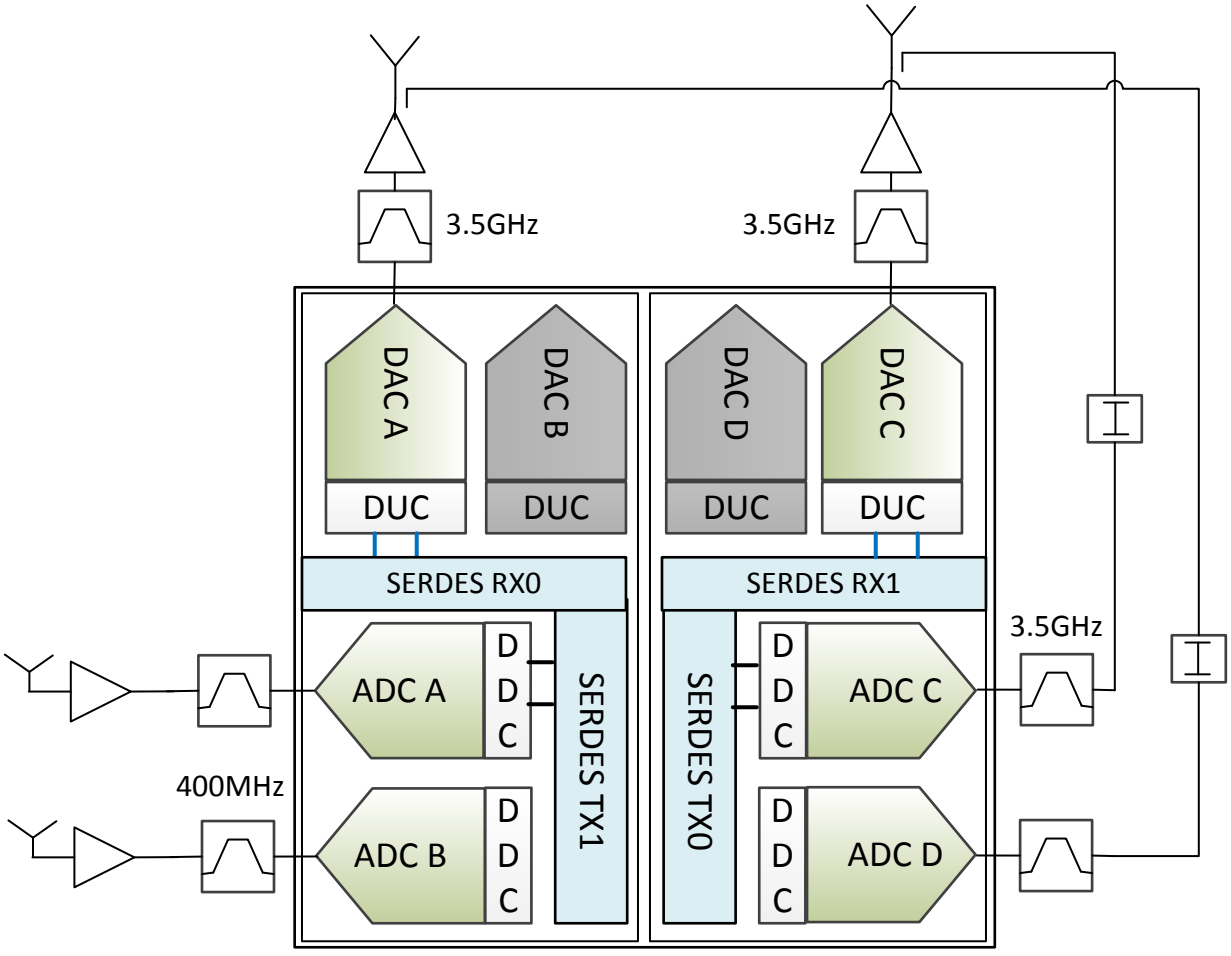

Figure 12. 2T2R2FB Configuration for RF Repeater

6 Test Results

This section shows the test results from few baseline configurations. TSW4086 with AFE7689 device was used for the measurements.

6.1 Test Results for Narrowband Configuration

A 2T2R2FB usecase configuration is selected and tested in FDD mode. The baseband sampling rate of TX and FBRX is 491.52MHz. The RX sampling rate is 122.88MHz.

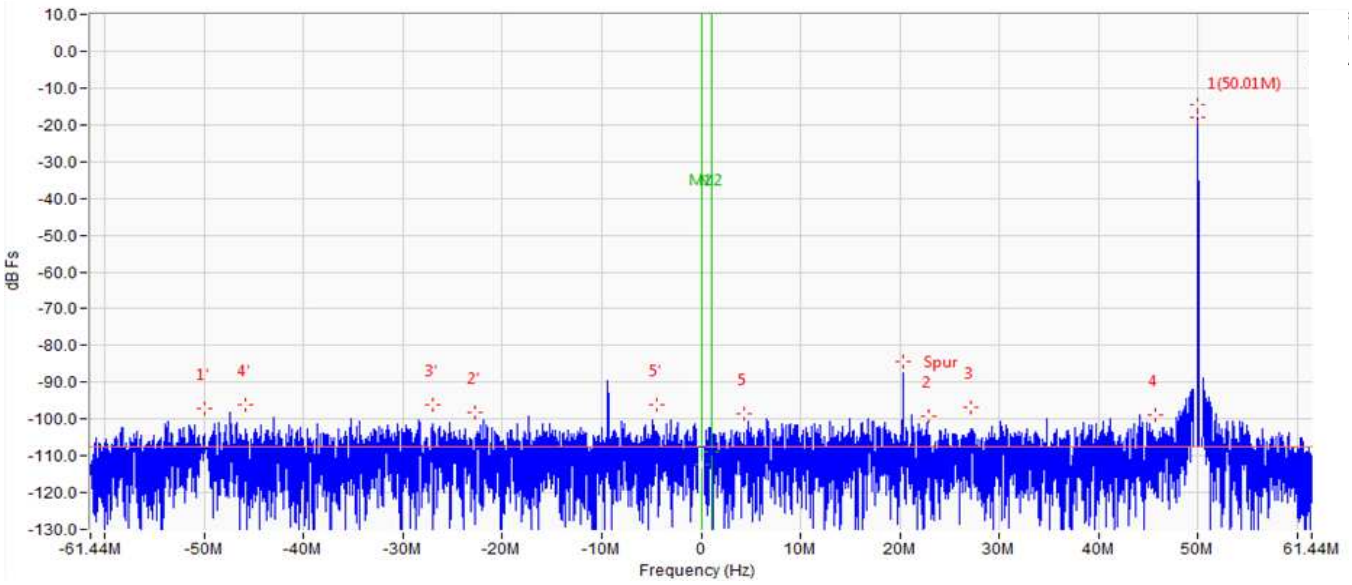

Figure 13. RX Path Output with Single Tone at 1750MHz, -15dBFS

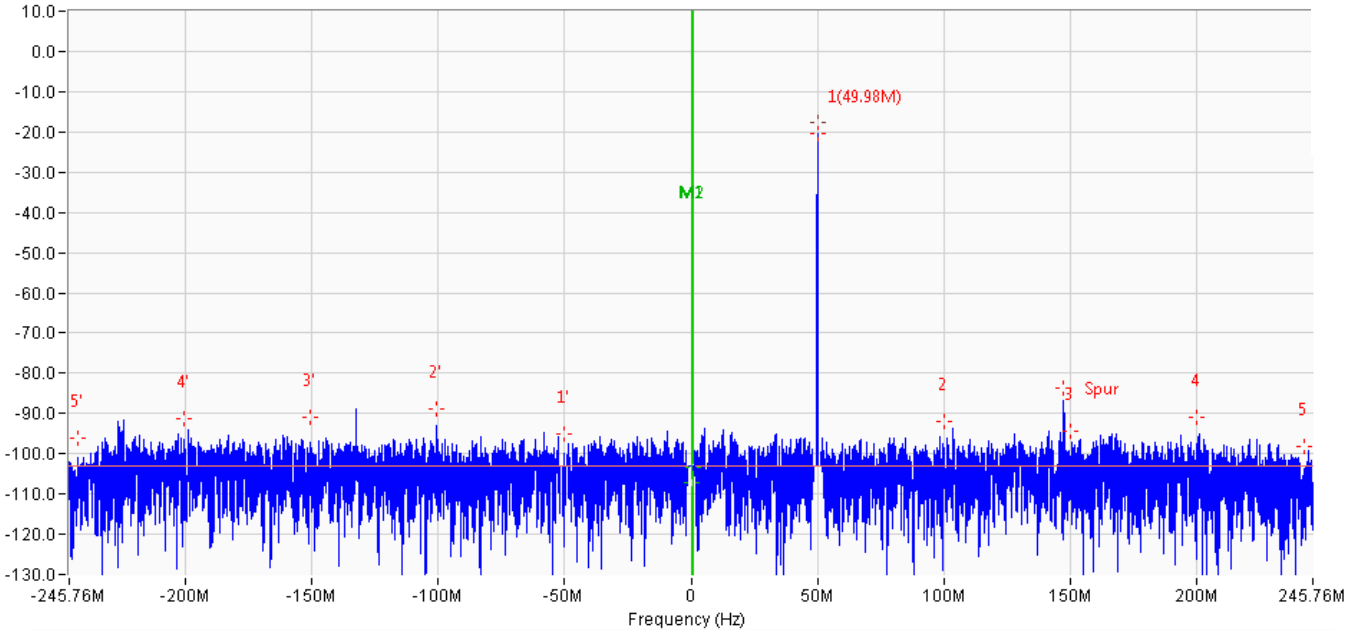

Figure 14. FBRX Path Output with Single Tone at 1750MHz, -15dBFs

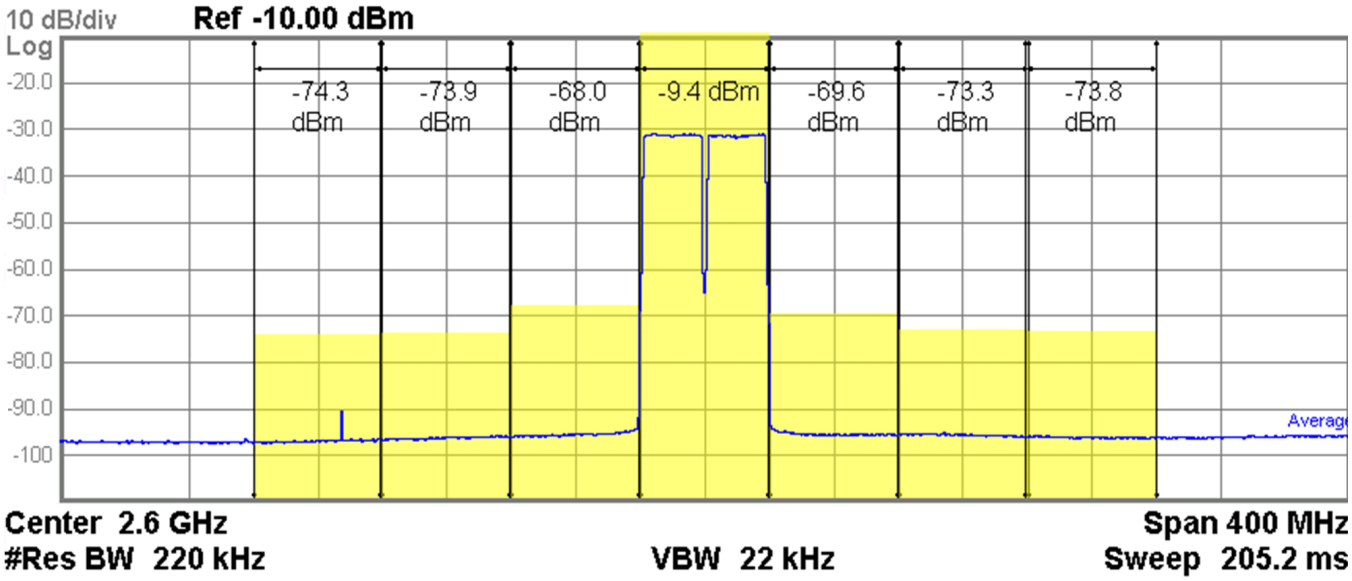

Figure 15. TX Output : 2x20MHz LTE Signal at 2.6GHz

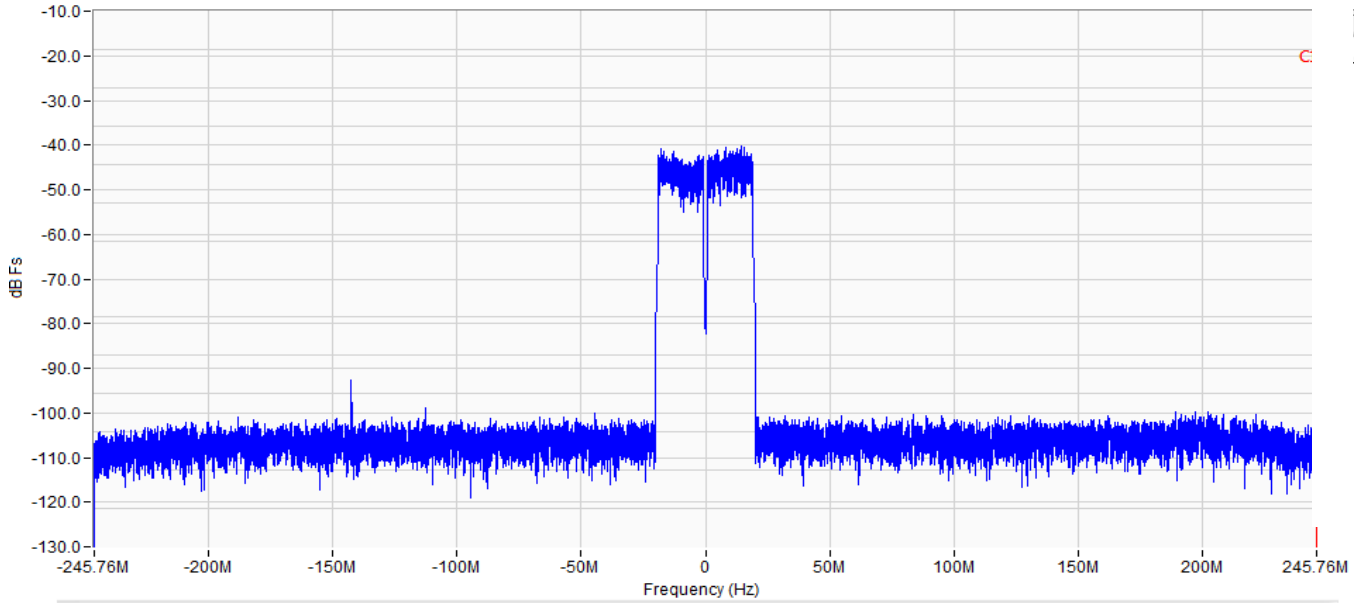

Figure 16. RX Output : 2x20MHz LTE signal (TX-RX Loopback) at 2.6GHz

6.2 Test Results for Wideband Configuration

As another example, a 5G RF repeater usecase is configured. RX paths C/D are trimmed for low band in the 1st Nyquist zone (<1GHz) and the matching circuits are also modified for a frequency below 1GHz. While RX paths A/B are trimmed for 3.5GHz which is in the 3rd Nyquist zone. RX A and B are used for the TX feedback paths. TX paths C/D are used for an easy implementation of the RX-to-TX direct loopback. TX and FBRX NCOs are configured to 3.5GHz and the RX NCOs are set for 430MHz.

For the RF repeater usecase with high transmit power, the direct loopback is not used normally. To demonstrate the direct loopback feature of an AFE76xx, the RX path is configured to have the same sampling rate at baseband as the TX paths. For the direct loopback test, a CW tone is put at 450MHz and the RX NCO is set at 430MHz. While the TX NCO is set to 3500MHz. Through the loopback path, slight SNR degradation is observed as shown in the measurement below.

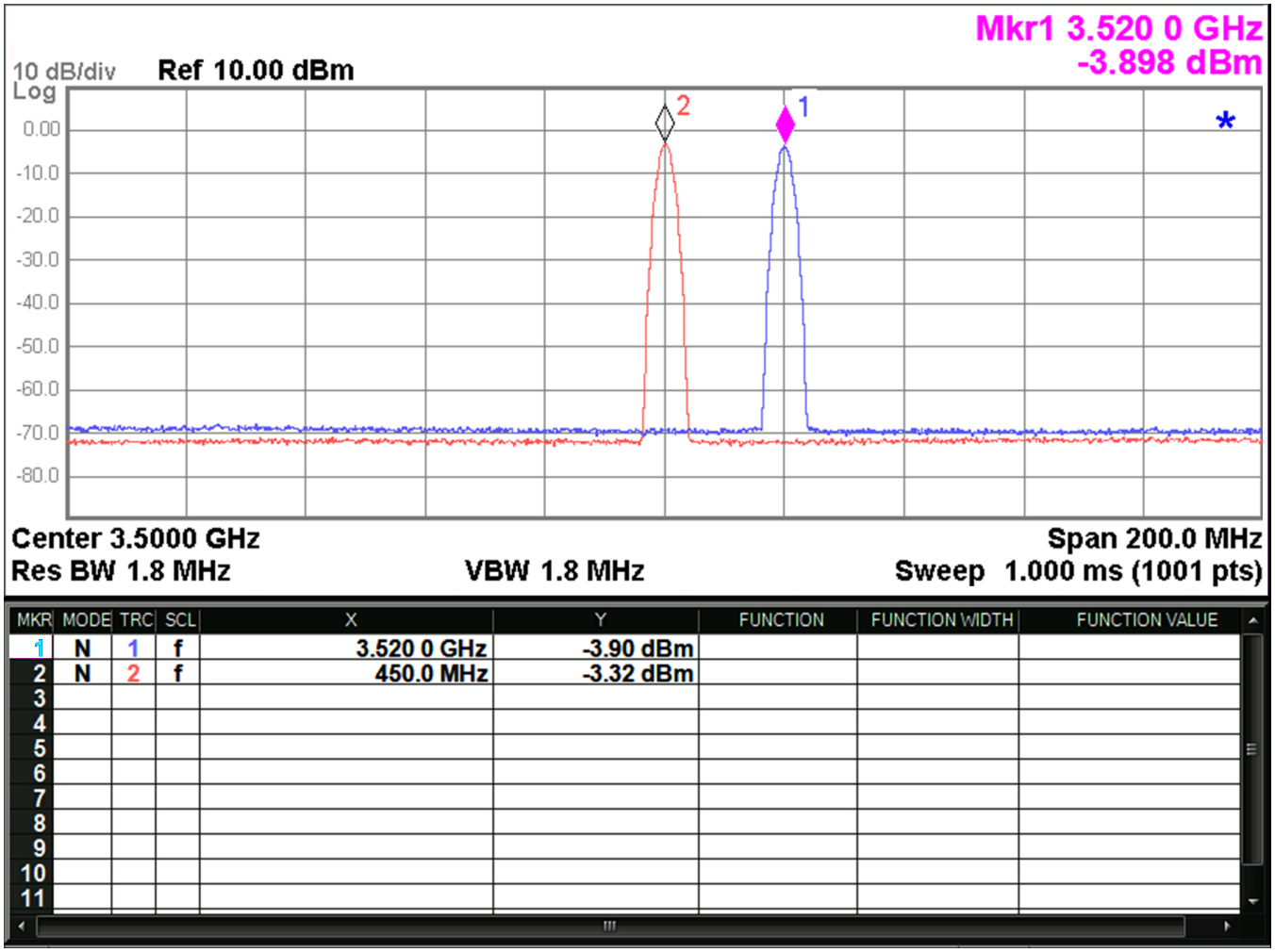

Figure 17. Digital RX-to-TX Direct Loopback : RX input - CW at 450MHz, TX output at 3520MHz

The usecase supports a bandwidth up to 600MHz. The two measurements below show the TX path and FBRX path responses for a wideband signal at 3.5GHz.

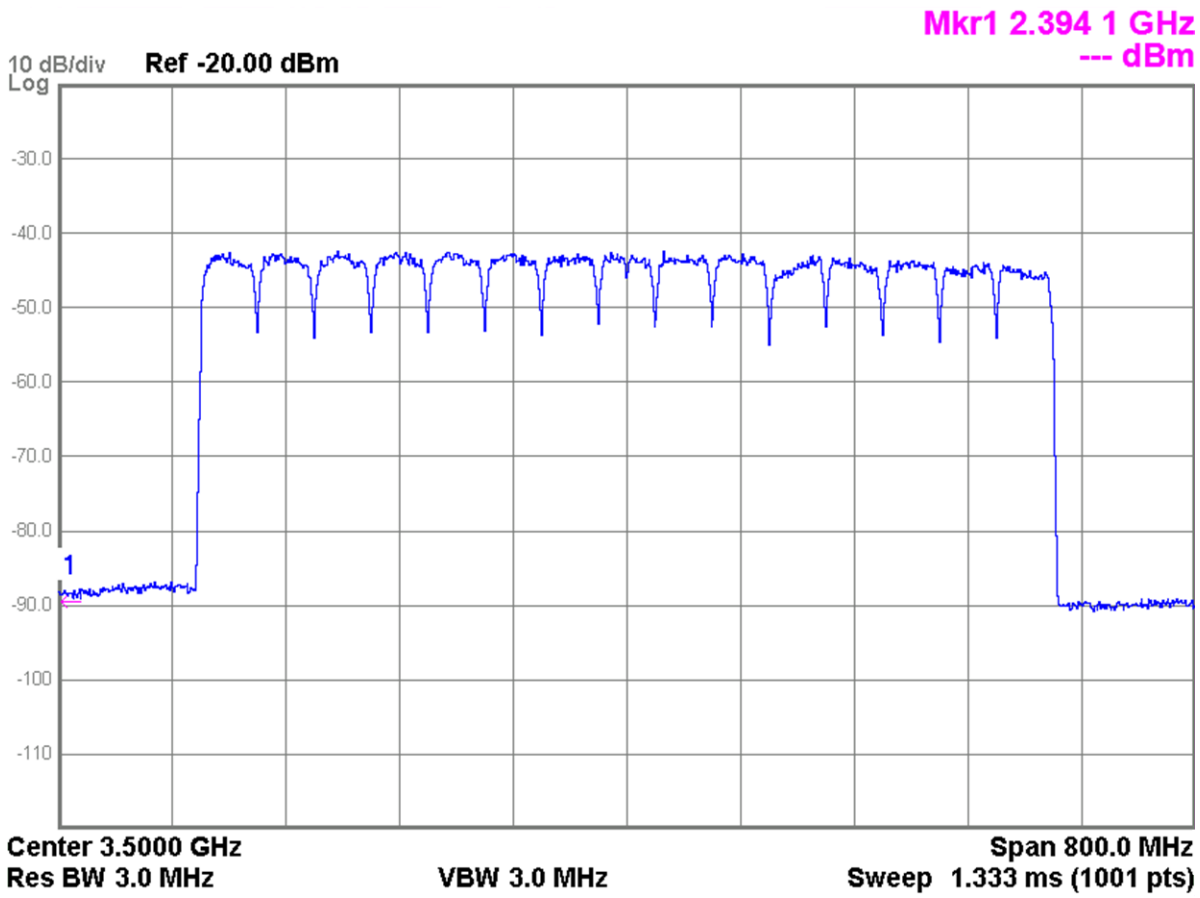

Figure 18. TX Path Output with Wideband Signal (600MHz)

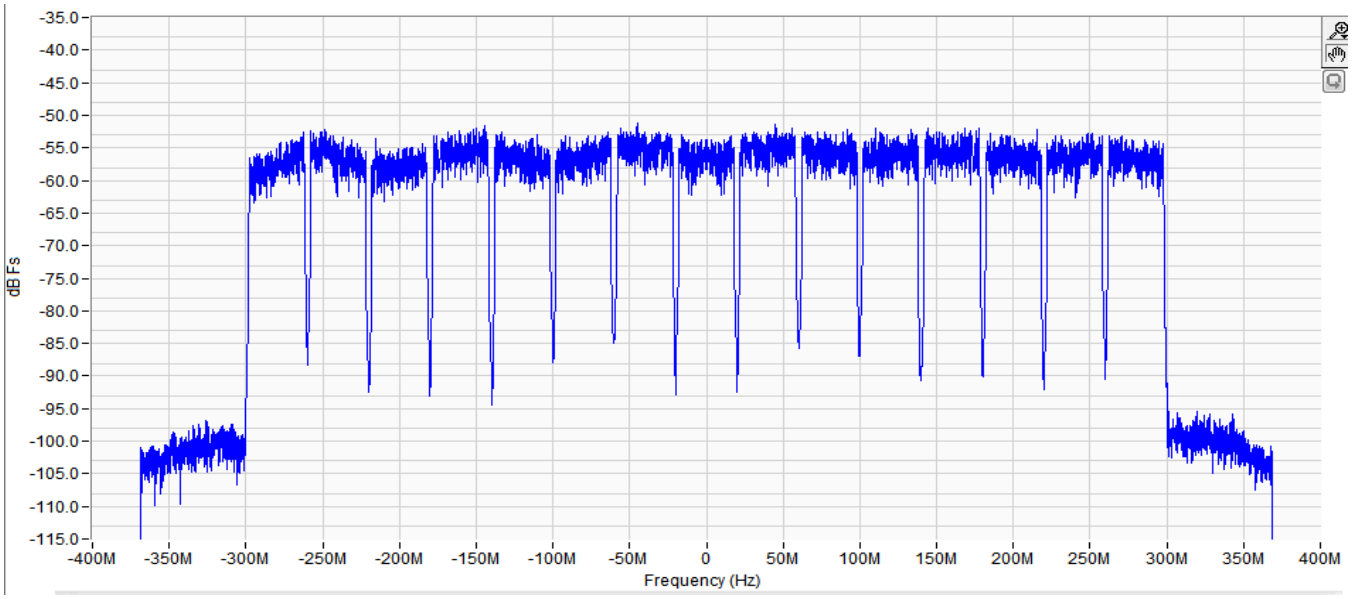

Figure 19. FBRX Path Output with Wideband Signal (600MHz)

The 2T2R2FB TDD configuration for an optic repeater application supports a time-shared receive mode between RX and FBRX modes. In the tests below, a CW tone is placed at 3525MHz. A NCO for RX mode is set at 3500MHz, while another NCO which is used for FBRX mode is set at 3550MHz. , RXTDD, and RXFBSW GPIO's are used to trigger the mode switch between two modes. By default, a 2x wider bandwidth is supported by FBRX mode compared with RX mode.

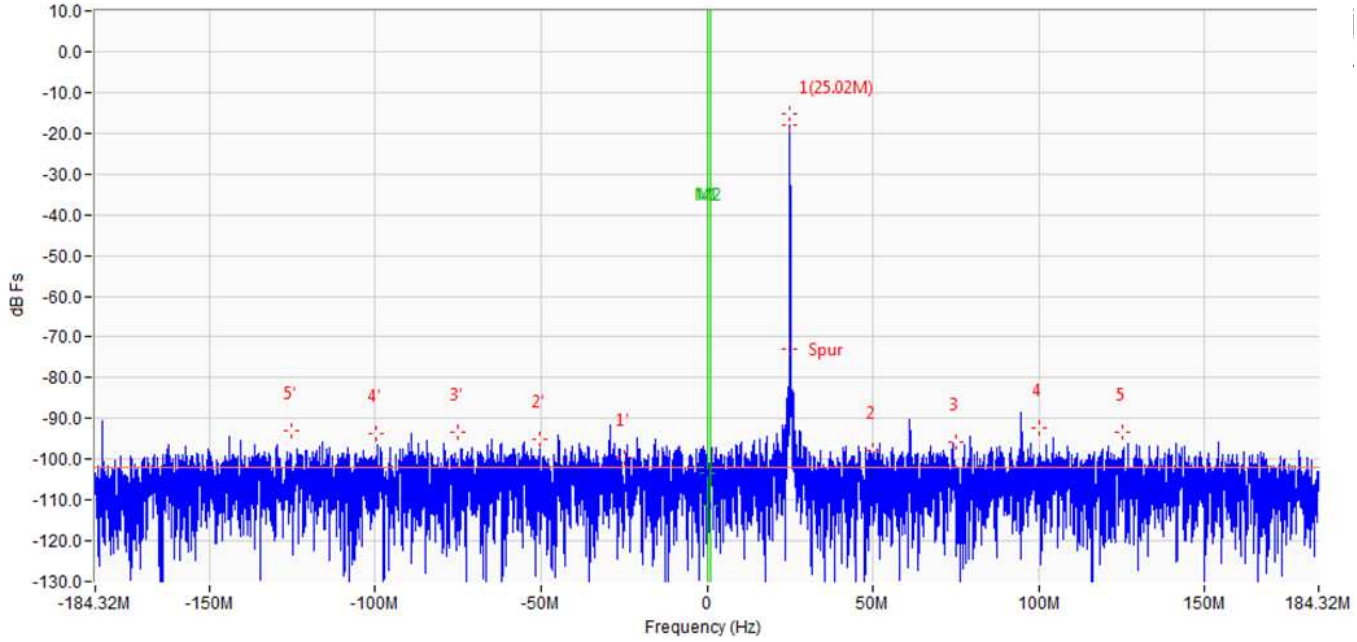

Figure 20. RX Mode Output

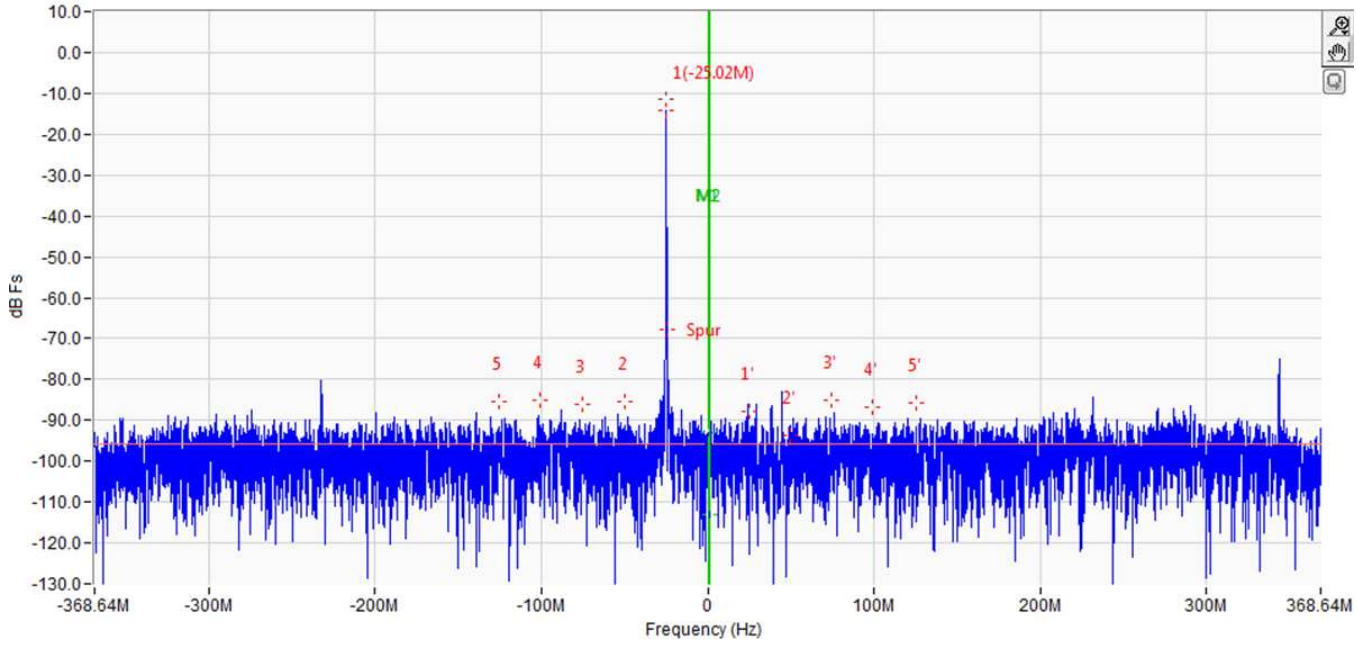

Figure 21. FBRX Mode Output

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