Application Report
SBAA422–April 2020

# AFE76xx, AFE77xx, and AFE79xx JESD204 Layer Testing

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**ABSTRACT**

The AFE76xx/AFE77xx/AFE79xx (AFE7xxx) family of RF sampling transceiver devices supports JESD204 link Subclass 1. The AFE7xxx has both JESD204B TX IP on the RXADC cores and also JESD204 RX IP on the TXDAC cores. To facilitate users with the AFE7xxx operation and also the JESD204B link bring-up process, there are various test modes to ensure each layer within the JESD204B stage are functional. Specifically, per the JESD204 standard, it supports both link layer testing and transport layer testing highlighted within JESD204B Standard, Section 5.1.6 and 5.3.3.8. The corresponding section on the updated JESD204C Standard is Section 6.6 and 8.4.8.

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# 1 Introduction

The overall signal chain of the JESD204B link for both the ADC and DAC are highlighted in Figure 1. The physical layer testing, link layer testing, and transport layer testing are highlighted in this JESD204 test capability overview. Completing these tests during customer end-product characterization can ensure robustness of the AFE7xxx JESD204 link.

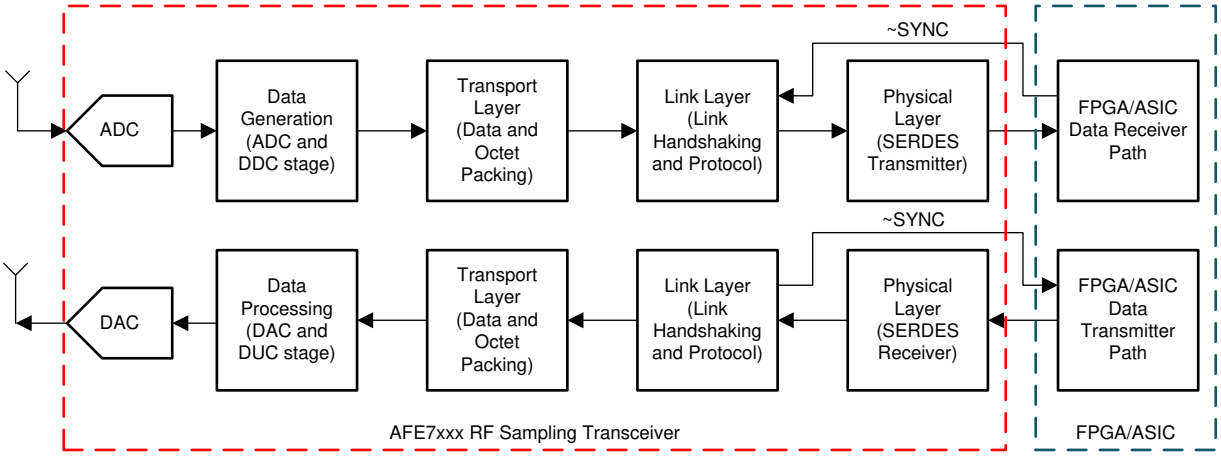


**Figure 1. Overall JESD204B Link Diagram for AFE76xx and FPGA/ASIC**

## *1.1 Acronyms and Descriptions*

**Table 1. Acronyms and Descriptions**

| ACRONYMS | DESCRIPTIONS |
|---|---|
| TXDAC | Digital-to-Analog Converter (Transmitter Downlink) |
| RXADC | Analog-to-Digital Converter (Receiver Uplink) |
| JESD204 | JEDEC Standard for Serial Link Transfer for Data Converters |
| SerDes | Serializer and De-serializer Circuits |
| STX | SerDes Transmitter |
| SRX | SerDex Receiver |
| PRBS | Pseudo Random Bit Sequence |

# 2 Physical Layer Testing

The AFE7xxx devices have eight lanes of SerDes (Serializer and De-serializer) transceivers. The SerDes transmitters, or STX, transmits the serialized JESD204B/C data streams from the ADC and DDC logics to the ASIC/FPGA. The SerDes receivers, or SRX, receives the serialized JESD204B/C data streams from the ASIC/FPGA devices to the DAC and DUC logics. Figure 2 shows the general block diagram for the SerDes transceivers.

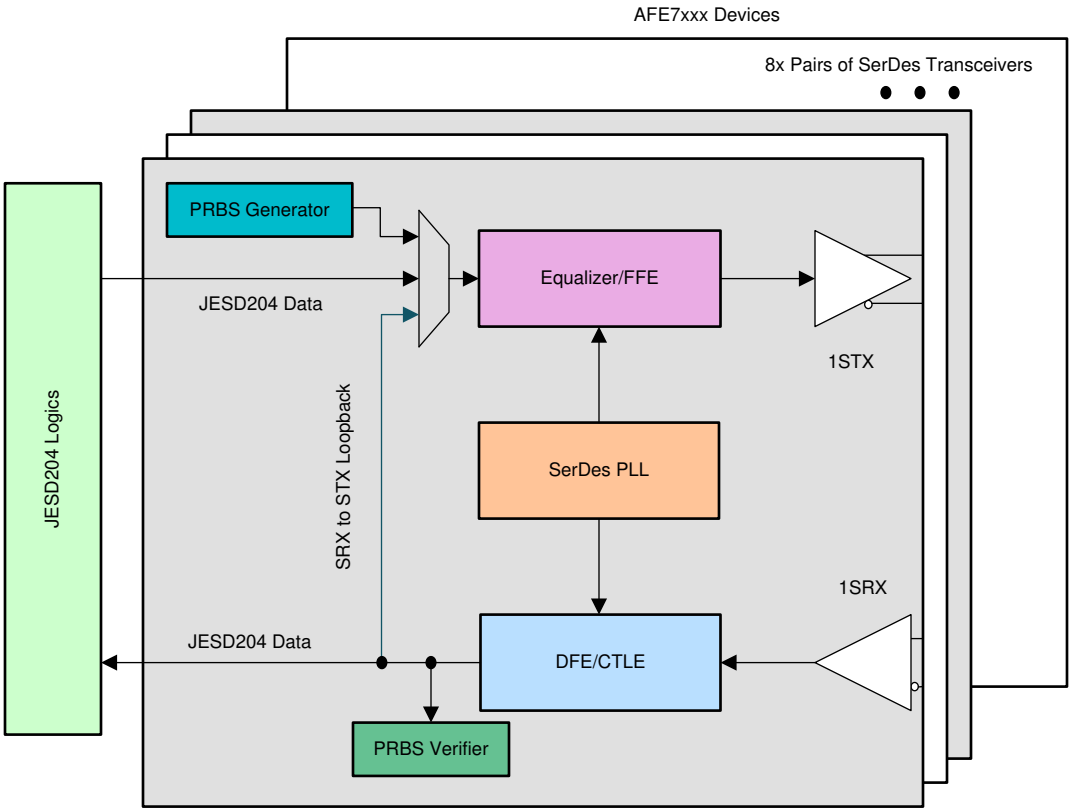


**Figure 2. General SerDes Block Diagram for the AFE7xxx Family**

For the SerDes based testing, the AFE7xxxx supports the generation and the verification of the PRBS patterns. A few example PRBS pattern supported are listed below:

- PRBS9 ($x^9 + x^5 + 1$)
- PRBS15 ($x^{15} + x^{14} + 1$)
- PRBS23 ($x^{23} + x^{18} + 1$)
- PRBS31 ($x^{31} + x^{28} + 1$)

The higher the order, the longer the pattern duration is before it repeats itself. For example, for PRBS31, it takes $2^{31}$ cycles before the pattern repeats itself.

The STX chain supports the generation of the PRBS pattern. This pattern generation can test the SRX chain at the FPGA/ASIC side for initial physical layer quality test.

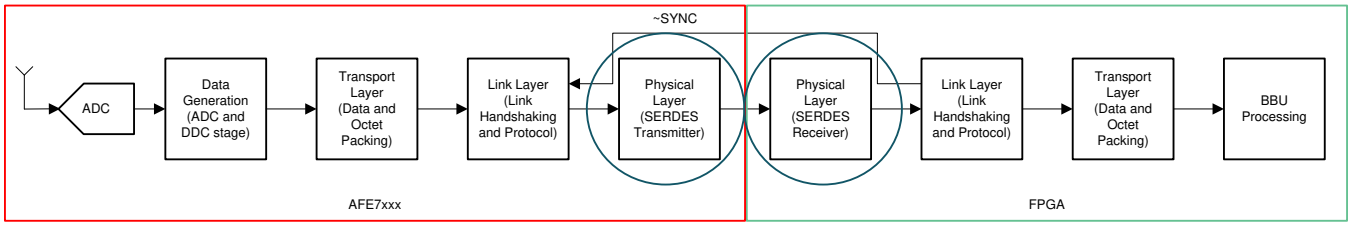


**Figure 3. Physical Layer of ADC to Send Pattern to Physical Layer of FPGA to Check**

The SerDes receiver chain integrates a checker for detecting the PRBS pattern error. It includes also an eye monitor to detect the eye height as well as generating more detailed eye diagrams, that can be read through the SPI.

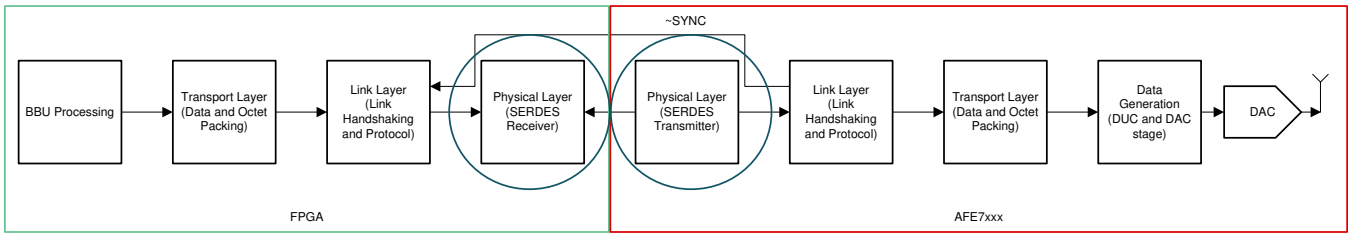


**Figure 4. Physical Layer of FPGA to Send Pattern to Physical Layer of DAC to Check**

The SerDes block within the AFE7xxx also supports loopback of the RX block recovered data to the TX block through a FIFO. This loop can be used to test the overall SerDes transmit and receive quality at the FPGA/ASIC side, as the FPGA/ASIC is responsible for generating the pattern and receiving the pattern. Any error detection is done on the FPGA/ASIC side. The routing of the bit error rate testing using loopback is shown in Figure 5.

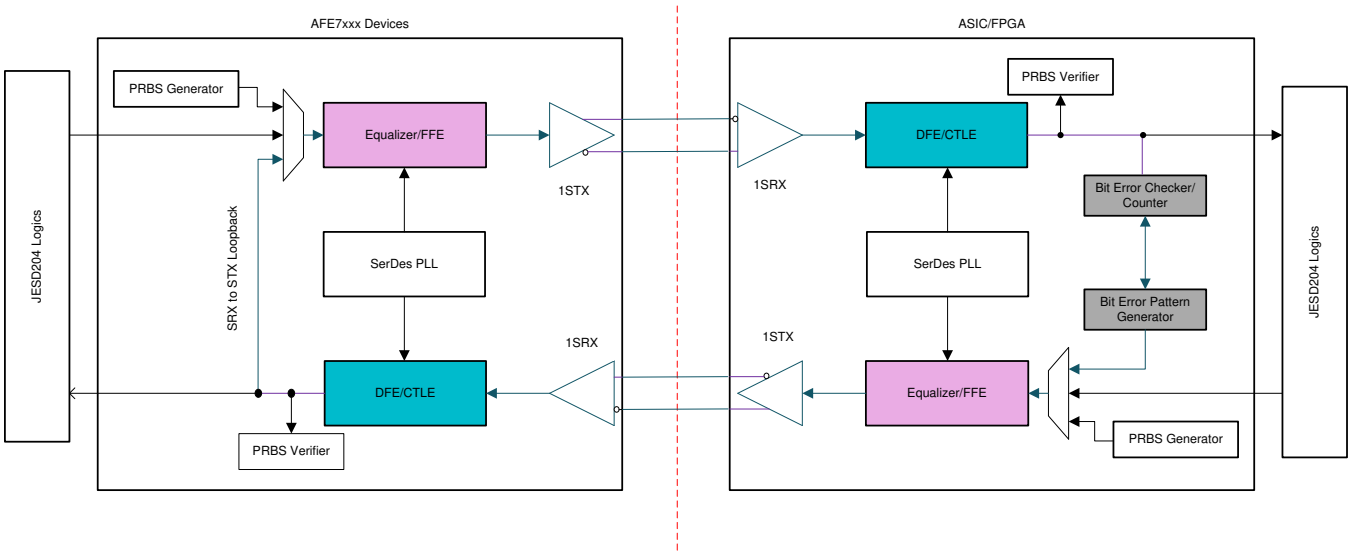


**Figure 5. General Block Diagram for the SerDes Loopback Testing From the ASIC/FPGA to the AFE7xxx Devices**

The SRX block also supports eye diagram and eye height margin. For training related to eye diagram, please visit the training portal, *TI Precision Labs – Signal Conditioning: What is an Eye Diagram?*

## 3 Link Layer Testing

Per JESD204B Standard Section 5.3.3.8, the AFE7xxx family of devices supports link layer test modes for the 8B/10B encoding. The corresponding JESD204C Standard is in Section 8.4.8. Link Layer testing is not defined for the 64B/66B and 64B/80B encoding within the JESD204C Standard. Per the standards, the link layer test mode is a state where predetermined 8B/10B characters are transmitted in all frames and on all lanes on the multipoint link.

### *3.1 JESD204B TX on the ADC Side*

The JESD204B TX side of the ADC supports the test sequence transmission specified by the JESD204B Standard 5.3.3.8.2. Each of the JESD204B TX lanes can support the following sequences:

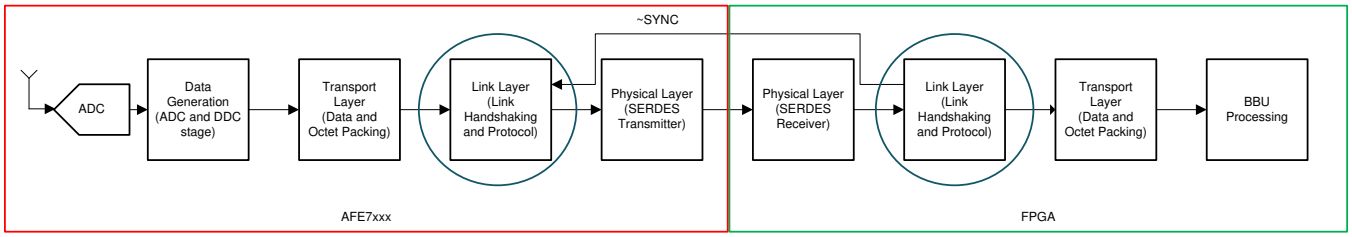


**Figure 6. Link Layer of ADC to Send Pattern to Link Layer of FPGA to Check**

The JESD204B TX side of the ADC supports the test sequence transmission specified by the JESD204B Standard 5.3.3.8.2. Each of the JESD204B TX lanes can support the following sequences:

**Table 2. JESD204B TX Link Layer Test Sequence**

| TEST SEQUENCE NUMBER | TEST SEQUENCE NAME |
|---|---|
| 0 | Test Sequence Disabled |
| 1 | Repeat /D21.5/ high frequency pattern for random jitter (RJ) |
| 2 | Repeat /K28.5/ mixed frequency pattern for deterministic jitter (DJ) |
| 3 | Repeat initial lane alignment sequence (ILAS) |
| 4 | Modified random pattern (RPAT/CRPAT) |
| 5 | Scrambled jitter pattern (JSPAT) |
| 6 | Repeat /K28.7/ low frequency pattern |

The most commonly used sequence for the JESD204B TX test is the repeating /K28.5/ pattern and the repeating ILAS sequence. The repeating /K28.5/ pattern is useful in analyzing the correct pattern is send during the code group synchronization (CGS) state of the JESD204B handshaking protocol, and the repeating ILAS sequence is useful in debugging the process of initial lane alignment state of the protocol.

## 3.2 JESD204B RX on the DAC Side

The JESD204B RX on the DAC side supports the test sequence pattern checking capability as described in the JESD204B standard. The standard specified the two main test sequences to be repeating /K28.5/ patterns and also repeating ILAS sequence. Other optional sequences will be covered in the 8B/10B decoder of the JESD204B RX IP. Each JESD204B RX IP on each TXDUC block has an independent test sequence verifier, and each verifier has the following capabilities.

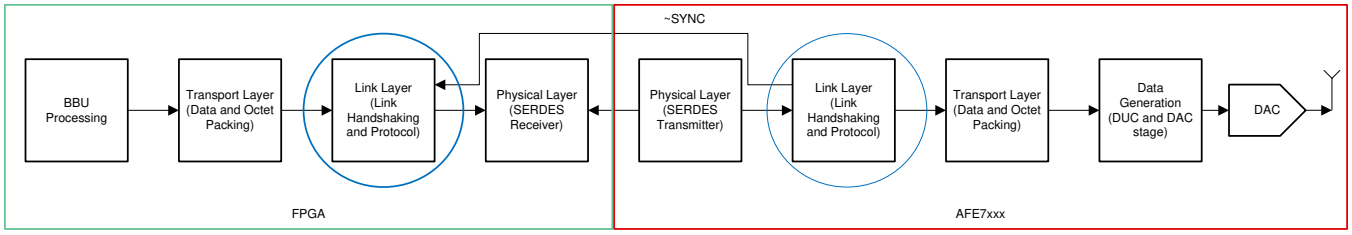


**Figure 7. Link Layer of FPGA to Send Pattern to Link Layer of DAC to Check**

**Table 3. JESD204B RX Link Layer Test Verifier**

| TEST SEQUENCE NUMBER | TEST SEQUENCE NAME |
|---|---|
| 0 | Test Sequence Disabled |
| 1 | Repeat /D21.5/ high frequency pattern for random jitter (RJ) |
| 2 | Repeat /K28.5/ mixed frequency pattern for deterministic jitter (DJ) |
| 3 | Repeat initial lane alignment sequence (ILAS) |

Besides configuring the test pattern verifier, the user will need to clear and read back certain alarm registers to confirm test result of the test pattern verifier. TI recommends the user first configure the test pattern generator on the JESD204B TX side (usually on the ASIC or FPGA), and then configure the test pattern verifier on the JESD204B RX side of the DAC. The clearing and reading of the test result should be done when both the JESD204B TX and JESD204B RX test pattern logics are stable.

# 4 Transport Layer Testing

Per JESD204B Standard Section 5.1.6.2, the AFE76xx family of devices supports short transport layer test pattern generator and verifier. Per the standard, the short test pattern has duration of one frame period and is repeated continuously for the duration of the test. Each sample shall have a unique value that can be identified with the position of the sample in the user data format.

## *4.1 JESD204B TX on the ADC Side*

The JESD204B TX side of the ADC supports the test sequence transmission. The test sequence generator is enabled through the configuration of the SPI registers.

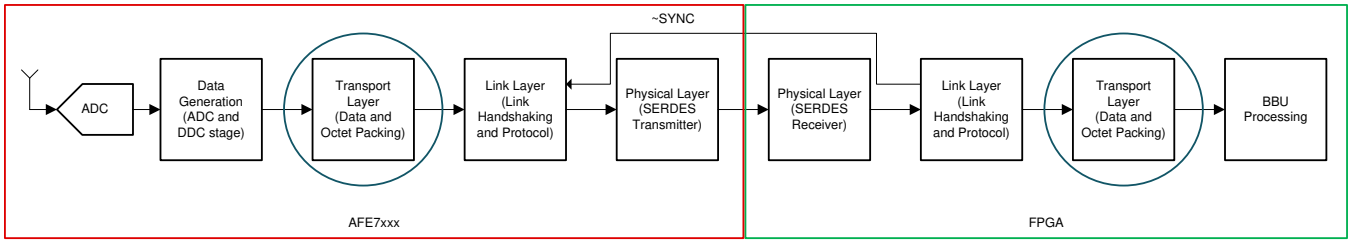


**Figure 8. Transport Layer of ADC to Send Pattern to Link Layer of FPGA to Check**

The mapping of the programming patterns is done in octets, and the mapping of the programmable octets in the SPI register and to the actual transport layer pattern is done in one to one fashion. Also, since the JESD204 TX programming groups either ADC-A and ADC-B together or ADC-C and ADC-D together, the transport layer packing is addressed in two ADC channel at the same time. For example, the 2RX of 24410 transport layer is shown in Table 4, while the programmable octets in short pattern test is shown in Table 5.

**Table 4. Transport Layer Mapping for 2RX of 24410 Mode**

| EXAMPLE | JESD204B TX 1x2RX_24410 MODE | | | |
|---|---|---|---|---|
| Octet | 1 | 2 | 3 | 4 |
| lane STX0 | RXA_i0[15:8] | RXA_i0[7:0] | RXA_q0[15:8] | RXA_q0[7:0] |
| lane STX1 | RXB_i0[15:8] | RXB_i0[7:0] | RXB_q0[15:8] | RXB_q0[7:0] |

**Table 5. Mapping of Transport Layer Octet to 24410 Mode**

| EXAMPLE | JESD204B TX 1x2RX_24410 MODE | | | |
|---|---|---|---|---|
| Octet | 1 | 2 | 3 | 4 |
| lane STX0 | Octet0 | Octet1 | Octet2 | Octet3 |
| lane STX1 | Octet4 | Octet5 | Octet6 | Octet7 |

Other transport layer pattern arrangement may also have the same octet mapping. For example, simple arrangement of the transport layer data packing shown that the same pattern for 1x2RX of 24410 is also valid for 1x2RX of 44210 mode, as shown in Table 6 and Table 7.

**Table 6. Transport Layer Mapping for 2RX of 44210 Mode**

| EXAMPLE | JESD204B X 1x2RX_44210 MODE | |
|---|---|---|
| Octet | 1 | 2 |
| lane STX0 | RXA_i0[15:8] RXA_i0[7:0] | RXA_i0[7:0] |
| lane STX1 | RXA_q0[15:8] | RXA_q0[7:0] |
| Lane STX2 | RXB_i0[15:8] | RXB_i0[7:0] |
| Lane STX3 | RXB_q0[15:8] | RXB_q0[7:0] |

**Table 7. Mapping of Transport Layer Octet to 44210 Mode**

| EXAMPLE | JESD204B X 1x2RX_44210 MODE | |
|---|---|---|
| Octet | 1 | 2 |
| lane STX0 | Octet0 | Octet1 |
| lane STX1 | Octet2 | Octet3 |
| Lane STX2 | Octet4 | Octet5 |
| Lane STX3 | Octet6 | Octet7 |

After configuring the pattern, engineers can change the patterns in the SPI register (i.e. Octet0, Octet1) to change the transmitted pattern on the JESD204 TX logic. They can then read back the patterns from JESD204 RX logic on the ASIC/FPGA to see if the value matches the programmed value.

## 4.2 JESD204B RX on the DAC Side

Besides JESD204B TX short pattern generator, the JESD204B RX short pattern verifier is also available on the DAC side. One slight difference is that since each DAC has its own JESD204B RX IP logic, the transport layer packing and the associated programmable octets are with respect to the DAC channel of its own. The user should find the transport layer packing that are addressed for 1TX topology.

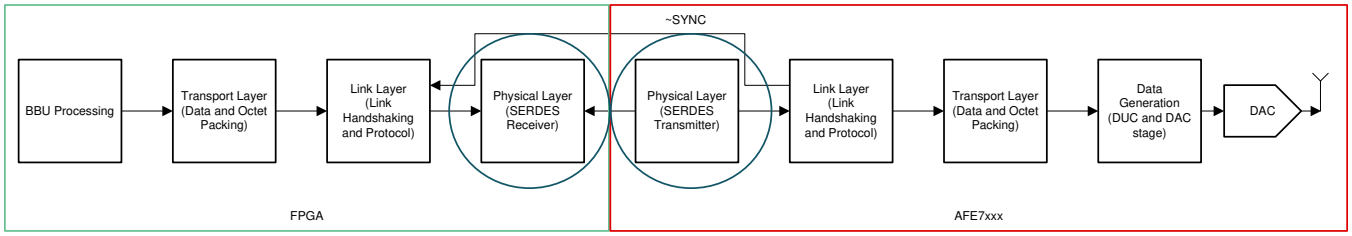


**Figure 9. Transport Layer of FPGA to Send Pattern to Link Layer of DAC to Check**

For example, the 1x1TX of 12410 mode (or 2TX of 24410 mode) has the transport layer mapping as shown in Table 8, with the short pattern verifier octet pattern as shown in Table 9.

**Table 8. Transport Layer Mapping for 1TX of 12410 Mode**

| EXAMPLE | JESD204B TX 1x2RX_24410 MODE | | | |
|---|---|---|---|---|
| Octet | 1 | 2 | 3 | 4 |
| lane STX0 | TXA_i0[15:8] | TXA_i0[7:0] | TXA_q0[15:8] | TXA_q0[7:0] |

**Table 9. Mapping of Transport Layer Octet to 1TX of 12410 Mode**

| EXAMPLE | JESD204B TX 1x2RX_24410 MODE | | | |
|---|---|---|---|---|
| Octet | 1 | 2 | 3 | 4 |
| lane STX0 | octet0 | octet1 | octet2 | octet3 |

The programming and checking of the JESD204 RX logic short pattern checker involves enabling the short pattern test verifier, programming the associated octet keys to check against the JESD204B TX short pattern generator, and the alarm clearing and read back of the verifier status. TI recommends clearing the alarm register after both the JESD204B TX and RX are stable to get the most up to date reading of the verifier status.

## 5 Summary

The AFE7xxx family of RF transceiver devices supports phyiscal layer testing of the SerDes link, and also the link layer and transport layer testing of the JESD204 link. These testing are essential to ensure link stability during the overall operation of the RF system with the AFE7xxx transceiver in the design. The details of the exact setup and configuration will be AFE7xxx device dependent, and separate documents are available to describe the setup and configuration for the individual device.

## 6 References


- Texas Instruments, AFE76xx Quad/Dual-Channel, RF Sampling Analog Front-End with 14-Bit 9GSPS DACs and 14-bit 3GSPS ADCs Data Sheet
- Texas Instruments, AFE7769 Quad-Channel RF Transceiver with Feedback Paths Data Sheet
- Texas Instruments, AFE7799 Quad-Channel RF Transceiver with Feedback Path Data Sheet
- Texas Instruments, AFE79xx Quad-Channel RF Transceiver with Feedback Path Data Sheet

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