Application Note

AFE79xx as Single Chip Wideband Repeater Solution

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ABSTRACT

This application note explains loopback function of AFE79xx TI transceiver. This application note highlights the features and performance of AFE79xx as indigenous single chip repeater function for achieving low latency signal loopback using normal RX, TX pair and fast signal loopback using RX feedback and TX pair.

The application note includes the following key points.

- Understanding and configuring internal loopback JESD and fast loopback modes of AFE79xx.
- Measuring Group delay and Gain response across different data rates highlighting minimum latency sub 2 us and flat passband response for applied wideband spectrum bandwidth.
- Measuring Fast Feedback Analog Loop response Group delay to achieve sub 50-ns group delay response for applications demanding lowest latency in wide bandwidth (1 GHz) repeater signal chain application

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Trademarks

1 Introduction

In mobile communication, multiband RF repeaters are deployed to extend the coverage of base station to the region uncovered by base station. This repeater needs to function indigenously without sacrificing signal quality and re-transmit at lowest group delay.

AFE79xx in-device loopback feature function is highlighted in this application note to demonstrate as a use case for repeater function. Its inherent single chip operation without requiring external FPGA or JESD link establishment achieves high instantaneous bandwidth and lowest latency meeting specification for RF repeater products.

1.1 Highlighted Products

The AFE79xx is a family of high performance, wide bandwidth multi-channel transceivers, integrating four RF sampling transmitter chains, four RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE79xx devices is designed for multi-band 4G and 5G base stations. Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog to-digital converter). The single or dual digital down converters (DDC) provide up to 600 MHz of combined signal BW. In TDD mode, the receiver channel can be configured to dynamically switch between the traffic receiver (TDD RX) and wideband feedback receiver (TDD FB), with the capability of re-using the same analog input for both purposes. Each transmitter chain includes a single or dual digital up converters (DUCs) supporting up to 1200-MHz combined signal bandwidth.

1.2 Device Loopback Modes

1.2.1 ADC to DAC JESD Loopback

AFE79xx supports internal digital JESD loopback as shown in Figure 1-1 without the need of external STX and SRX lane connection. The internal 20-bit digital stream loopback has been tested by driving RXD using vector network analyzer for gain and group delay parameter plot having 12-GSPS DAC output and multiple JESD data rate from 122.88 MSPS to 491.52 MSPS. The bandwidth is measured across signal tone of 3.4 GHz to demonstrate loopback function for 5G n78 band. The device can also be configured for different frequency bands by tuning external matching circuit accordingly.

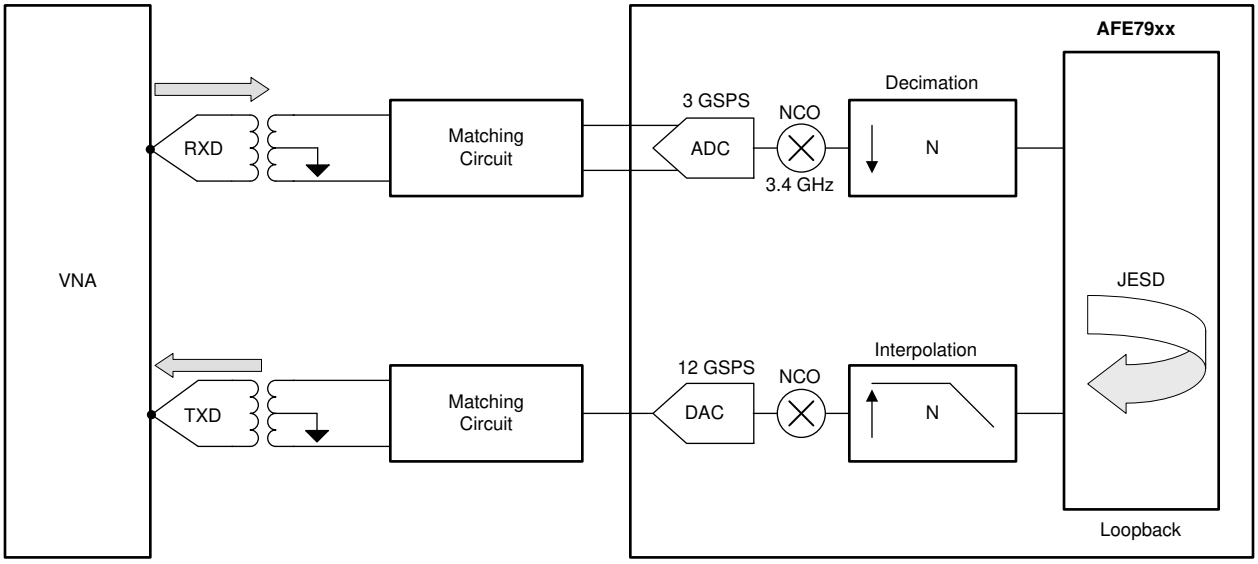

Figure 1-1. ADC to DAC JESD Loopback

Data sheet Switching Characteristics highlights expected latency across different SERDES rates as function of internal clock cycle as shown in Table 1-1.

Overall delay is total latency introduced in signal path due to matching element, RX input to JESD output latency, JESD to TX output latency and internal delay of VNA.

If we take 122.88 MSPS as an example, total internal delay of AFE79xx is 189 clock cycles at 122.88 MHz which approximates to 1.53 us. With external matching elements thus we can achieve sub 2-us group latency response.

Table 1-1. Switching Characteristics

at T_A= 25°C, full temperature range is $T_{A, MIN}$ = -40°C to $T_{J, MAX}$ = +110°C; TX Input Rate = 737.28 MSPS, f_{DAC}= 8847.36 MSPS; f_{ADC} = 2949.12 MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0 dB, SerDes rate = 24.33 Gbps; unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX CHANNEL LATENCY					
SerDes Receiver Analog Delay	Full Rate		2.8		ns
JESD to TX Ouput Latency	LMFSHd = 2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22 Gbps (JESD204C)		152		Interface Clock Cycles
	LMFSHd = 8-16-4-1, 491.52 MSPS input rate, 24x Interpolation, Serdes rate = 16.22 Gbps (JESD204C)		176		
	LMFSHd = 4-16-8-1, 245.76 MSPS input rate, 48x Interpolation, Serdes rate = 16.22 Gbps (JESD204C)		124		
	LMFSHd = 2-16-16-1, 122.88 MSPS input rate, 96x Interpolation, Serdes rate = 16.22 Gbps (JESD204C)		97		
RX CHANNEL LATENCY					
SerDes Transmitter Analog Delay			3.6		ns
RX Input to JESD Ouput Latency	LMFS = 2-8-8-1, 368.64 MSPS input rate, 8x Decimation, Serdes rate = 16.22 Gbps (JESD204C)		118		Interface Clock Cycles
	LMFS = 2-16-16-1, 122.88 MSPS input rate, 24x Decimation, Serdes rate = 16.22 Gbps (JESD204C)		92		
	LMFS = 4-16-8-1, 245.76 MSPS input rate, 12x Decimation, Serdes rate = 16.22 Gbps (JESD204C)		108		
	LMFS = 4-8-4-1, 491.52 MSPS input rate, 6x Decimation, Serdes rate = 16.22 Gbps (JESD204C)		153		
FB CHANNEL LATENCY					
SerDes Transmitter Analog Delay			3.6		ns
FB Input to JESD Ouput Latency	LMFS = 1-2-8-1, 368.64 MSPS, 8x Decimation		151		Interface Clock Cycles
	LMFS = 2-4-4-1, 491.52 MSPS, 6x Decimation		177		

1.2.2 ADC to DAC Low Latency Loopback

AFE79xx also supports internal analog loopback as shown in Figure 1-2 without need of internal JESD interface. The fast loopback has been tested by driving RX Feedback channel using vector network analyzer for gain and group delay having 12-GSPS DAC output connected with internal NCO for lowest latency in signal bandwidth. Internal dithering is disabled in this mode. The bandwidth is measured across signal tone of 3.4 GHz to demonstrate loopback function for 5G n78 band. The device can also configure for different frequency band by tuning external matching circuit accordingly.

Referring FB Channel Latency clock cycles as shown in Table 1-1, for 368.64 MSPS the internal delay will be approximately 41 ns thus achieving sub 50-ns latency for wide band spectrum.

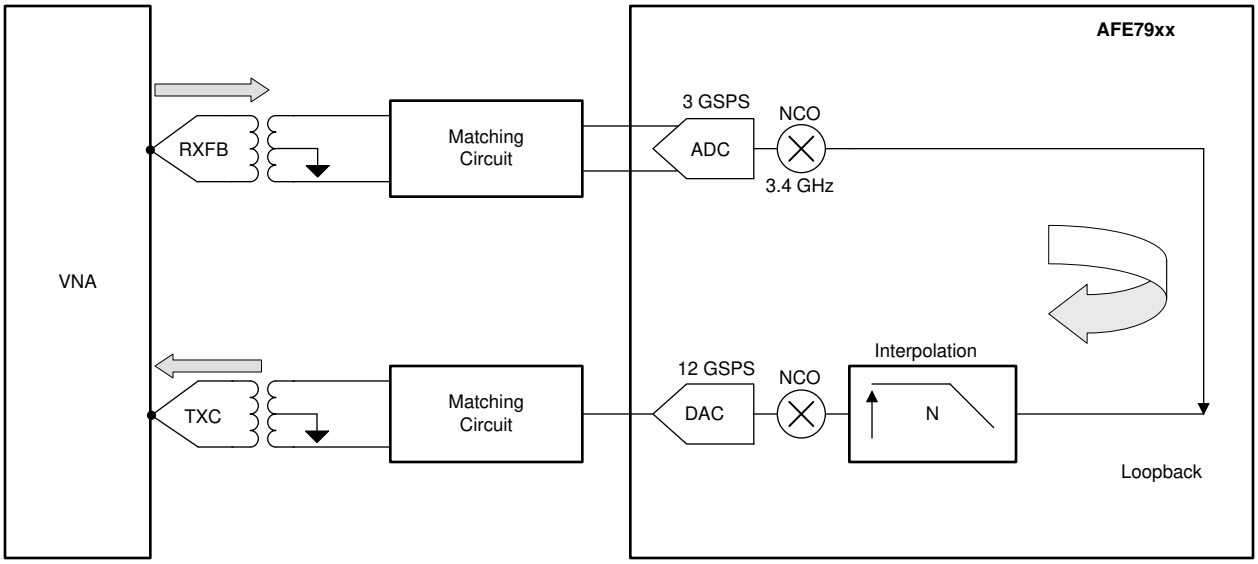

Figure 1-2. ADC to DAC Low Latency Loopback

2 Tests and Results

2.1 Test Methodology

2.1.1 Hardware Setup

2.1.1.1 ADC to DAC JESD Loopback

Vector Network Analyzer port 1 is connected to RXD channel of device, TXD channel is reconnected to port 2 of Vector Network Analyzer to capture group delay and loop gain. Vector Network Analyzer internally sweeps across bandwidth set relative to SERDES data rates.

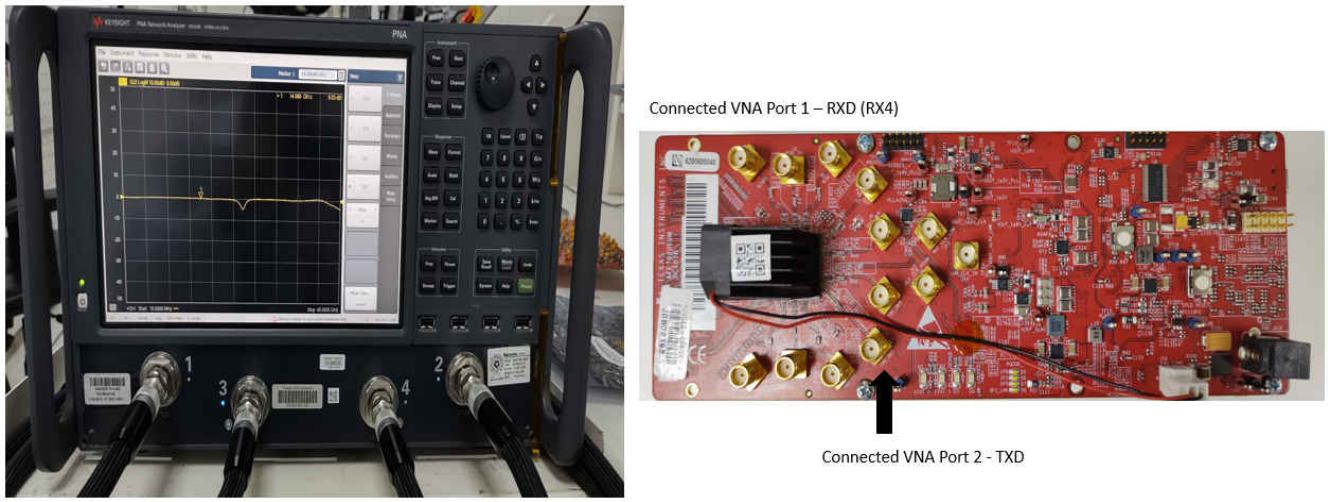

Figure 2-1. HW Block Diagram – JESD Loopback

2.1.1.2 ADC to DAC Low Latency Loopback

Vector Network Analyzer port 2 is connected to RXFB channel of device, TXC channel is reconnected to port 1 of Vector Network Analyzer to capture group delay and loop gain. Vector Network Analyzer internally sweeps across bandwidth relative to Impedance matching bandwidth.

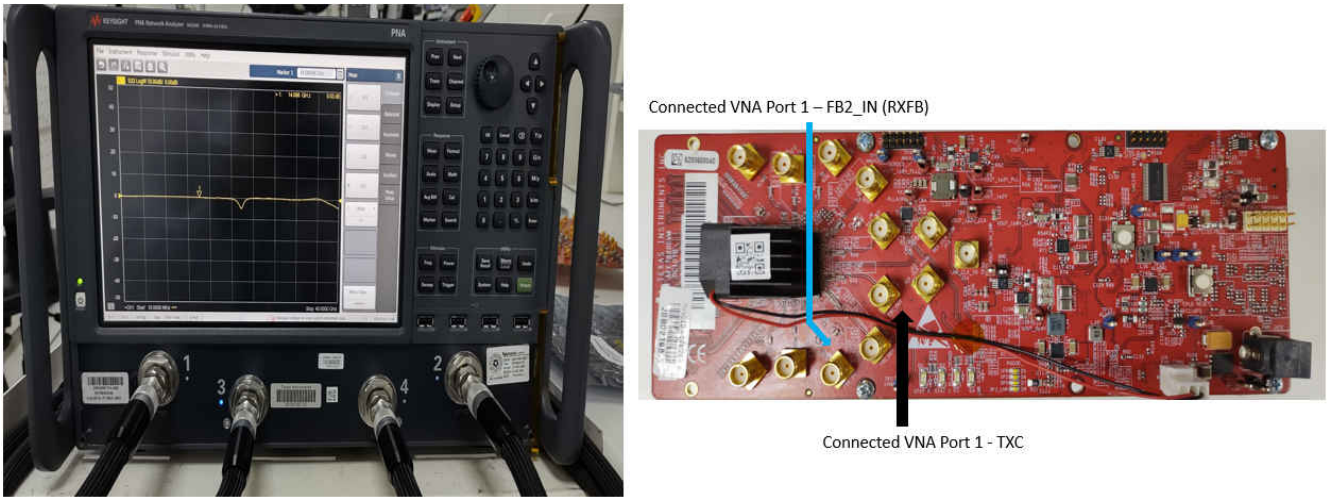

Figure 2-2. HW Block Diagram – Low Latency Loopback

2.1.2 GUI Setup

2.1.2.1 ADC to DAC JESD Loopback

AFE supports RX ADC to DAC loopback through the internal JESD block. This can be enabled by setting *jesdLoopBackEn* to True. Below are the conditions to be satisfied for using this feature.

1. The ADC and DAC interface rates must be same.
2. The JESD settings and the lane rates must be same for both RX and TX.
3. RXA must loop back to TXA, RXB must loop back to TXB, and so on.
4. Loopback mode is enabled using the check box as shown in Figure 2-3.

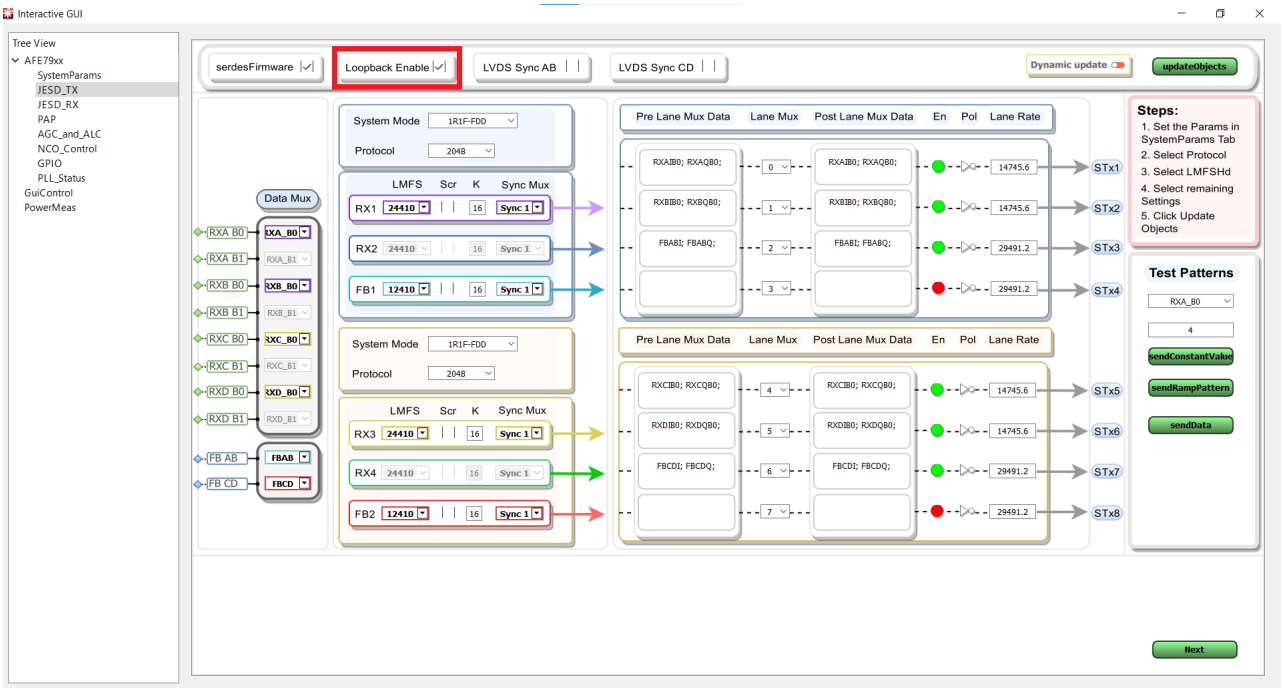

Figure 2-3. ADC to DAC JESD Loop Back Enable Mode

2.1.2.2 ADC to DAC Low Latency Loopback

This loops back the FB ADC output (before the decimation) to TX A/D, and therefore has very low loopback latency. This can be set using the parameter *enableTxFbLoopbackLowLatencyMode*. It is independent control for looping back FBAB to TXA and FBCD to TXC. For example, to loopback FBAB to TXA, and use FBCD and TXCD in straight mode, this parameter can be set as *sysParams.enableTxFbLoopbackLowLatencyMode* = [True, False]. The first value in the list is for FBAB and second is for FBCD.

2.1.3 Test Conditions

AFE79xx is configured for 12-GSPS DAC and 3-GSPS ADC sampling rate. NCO is internally configured for single band 3400 MHz to match the matching network and applied signal tone from vector network analyzer. SERDES data rate is changed internally across different settings of JESD interface rate accordingly.

2.1.4 Test Results

2.1.4.1 ADC to DAC JESD Loopback

2.1.4.1.1 JESD 122.88 MSPS

Internal JESD is set for 122.88-MSPS data rate to achieve 100-MHz signal bandwidth. Magnitude response has no ripple in pass band and group delay measures to 1.98-us without any ripple demonstration linear phase response of device.

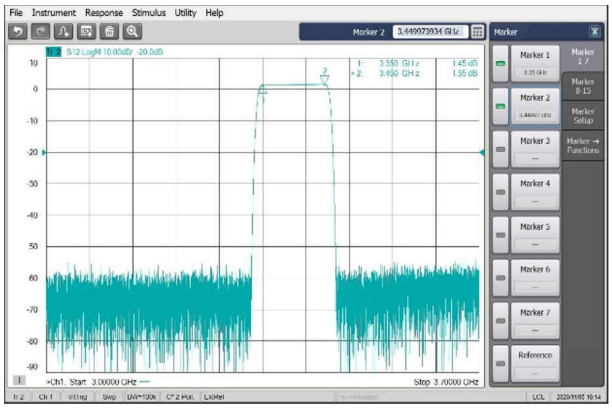

Figure 2-4. Magnitude Response 122.88 MSPS

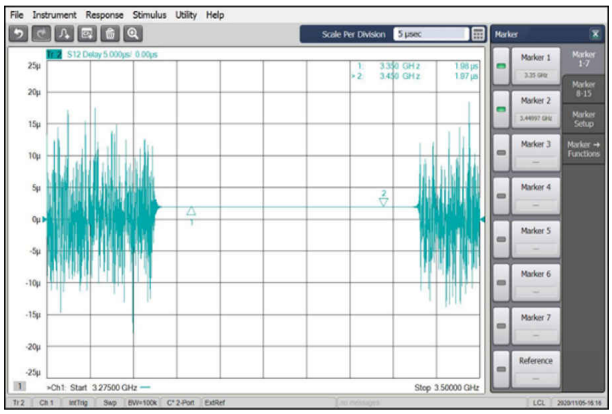

Figure 2-5. Group Delay 122.88 MSPS

2.1.4.1.2 JESD 184.32 MSPS

Internal JESD is set for 184.32 MSPS data rate to achieve 150-MHz signal bandwidth. Magnitude response has no ripple in pass band and group delay measures to 1.33 us without any ripple demonstration linear phase response of device.

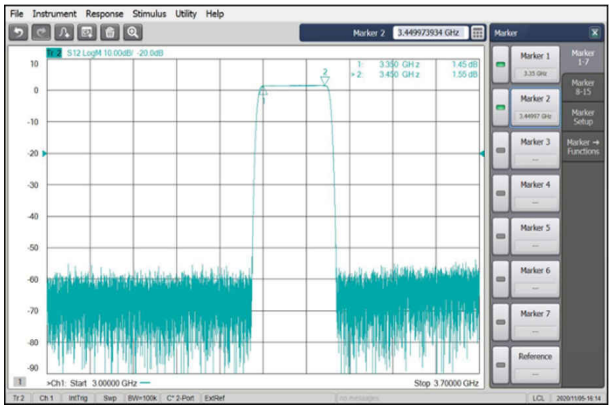

Figure 2-6. Magnitude Response 184.32 MSPS

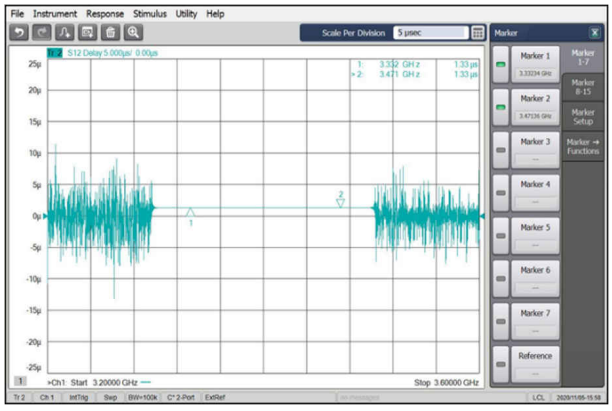

Figure 2-7. Group Delay 184.32 MSPS

2.1.4.1.3 JESD 245.76 MSPS

Internal JESD is set for 245.76-MSPS data rate to achieve 200-MHz signal bandwidth. Magnitude response has no ripple in pass band and group delay measures to 1.08 us without any ripple demonstration linear phase response of device.

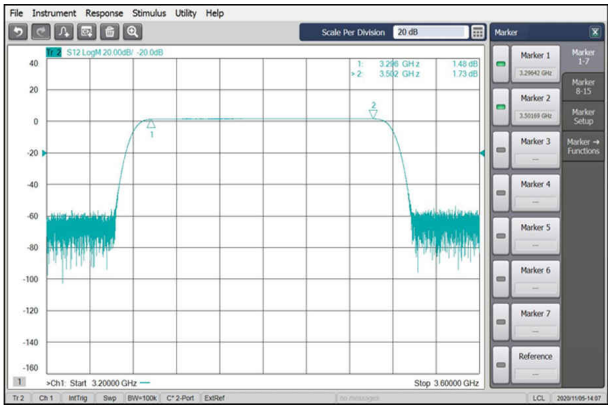

Figure 2-8. Magnitude Response 245.76 MSPS

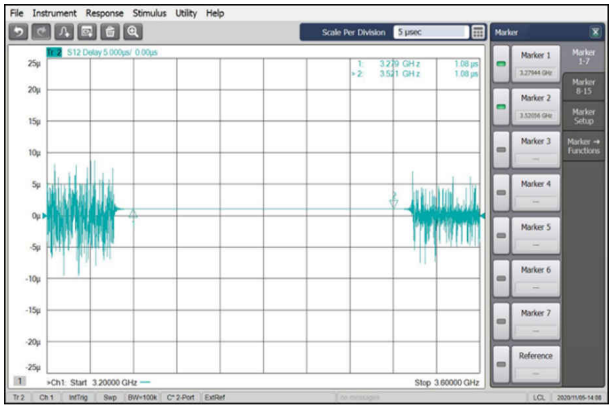

Figure 2-9. Group Delay 245.76 MSPS

2.1.4.1.4 JESD 368.64 MSPS

Internal JESD is set for 368.64-MSPS data rate to achieve 350-MHz signal bandwidth. Magnitude response has no ripple in pass band and group delay measures to 760 ns without any ripple demonstration linear phase response of device.

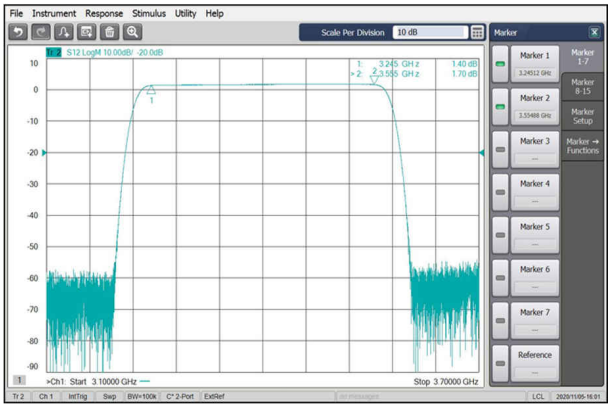

Figure 2-10. Magnitude Response 368.64 MSPS

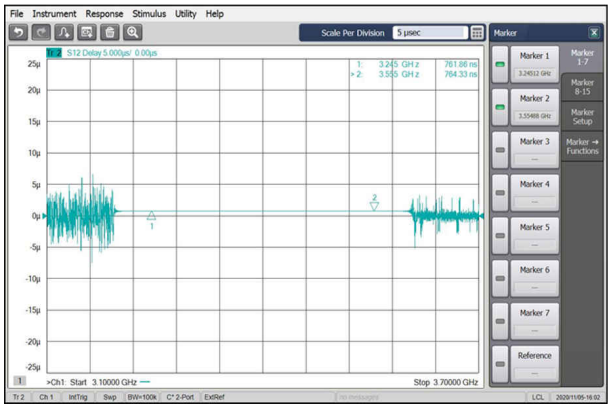

Figure 2-11. Group Delay 368.64 MSPS

2.1.4.1.5 JESD 491.52 MSPS

Internal JESD is set for 491.52-MSPS data rate to achieve 450-MHz signal bandwidth. Magnitude response has no ripple in pass band and group delay measures to 650 ns without any ripple linear phase response of device.

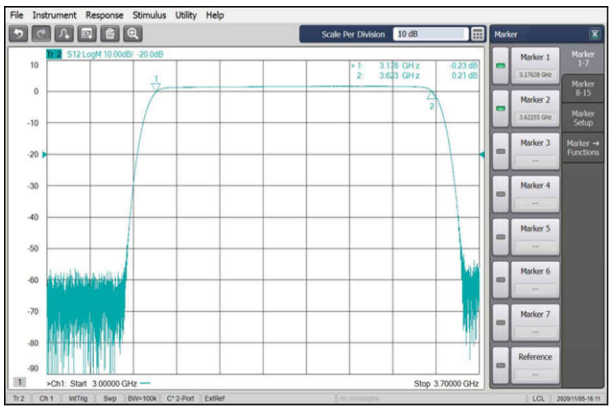

Figure 2-12. Magnitude Response 491.52 MSPS

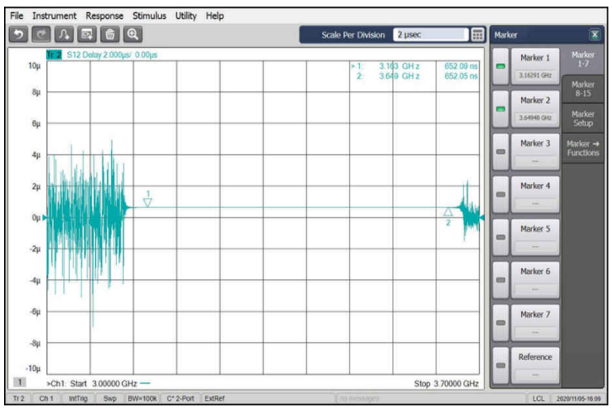

Figure 2-13. Group Delay 491.52 MSPS

2.1.4.2 ADC to DAC Low Latency Loopback

In this mode, the device is tested with loopback without DDC and JESD interface achieving high analog signal bandwidth (approximately 1 GHz). Magnitude response does not reflect any attenuation in pass band which is more dependent to external matching network loop response. Group Delay measures approximately 41 ns demonstrating lowest latency feedback signal chain.

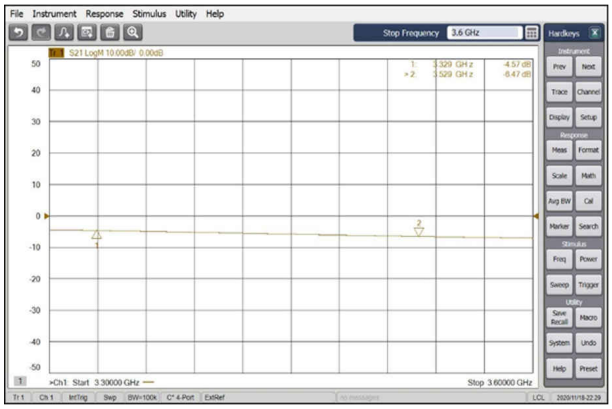

Figure 2-14. Magnitude Response ADC to DAC Low Latency Loopback

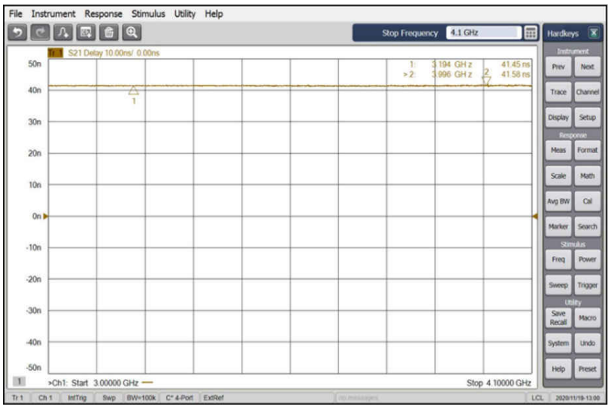

Figure 2-15. Group Delay ADC to DAC Low Latency Loopback

3 Conclusion

AFE79xx Direct RF sampling architecture with internal low latency (1.5 us) JESD loopback and high bandwidth 40-ns latency enables use of device as single chip solution in loopback application.

Flat Pass band magnitude response of device enables system solution to operate without additional gain stage. Ripple free pass band also indicates in-band spurious free leakage of device.

With emerging 5G NR wireless interface and need of long-range high bandwidth coverage, AFE79xx is a low-cost single chip solution to design low latency, high bandwidth repeater products.

4 References

- Texas Instruments, *AFE76xx, AFE77xx, and AFE79xx JESD204 Layer Testing application report*.
- Texas Instruments, *AFE79xx, LMH9xx EVM user guide*.

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