User's Guide

AM243x LaunchPad™ Development Kit User's Guide

ABSTRACT

The AM243x LaunchPad™ development kit is a simple and inexpensive hardware evaluation module (EVM) for the Texas Intruments Sitara™ AM243x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM243x MCUs with on-board emulation for programming and debugging as well as buttons and LEDs for a simple user interface. The LaunchPad also features two independent BoosterPack XL expansion connectors, on-board Controller Area Network (CAN) transciever, two RJ45 Ethernet ports, and an on-board XDS110 debug probe.

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1 Preface: Read This First

1.1 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM243x LaunchPad development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Section 5.1.

1.2 Important Usage Notes

Note

The AM243x LaunchPad requires a 5 V, 3A power supply in order to function. While a USB type-C cable is included, A 5 V, 3A power supply is **not** included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the LaunchPad and the supplied type-C cable. For more information on power requirements go to Section 3.1. If there is an error in the power input then the red LED (LD9) will glow continuously. For more information about the power status LED's, see Section 3.1.2.

Note

The JTAG connection through the micro-B USB port needs to be made after power is supplied to the LaunchPad by the USB type-C connection. The JTAG may not connect if the micro-B USB connection is made before the 5 V, 3A connection is made. For more information on JTAG emulation go to Section 4.15 .

Note

For E1 and E2 revisions of the AM243x LaunchPad, some output signals are not able to propagate to the BoosterPack headers. Any pinmux configuration that is an output signal for balls R21, T19, U18, U20, V20 of the SoC will be gated by the isolation buffer U32 because the DIR pin of the buffer is low (only allowing data transfer from side B to A). The signals that not able to propagate to the BoosterPack headers include: UART2_RTSn, EHRPWM2_A, EHRPWM2_B, as well as any GPIO signals on the listed pins.

2 Kit Overview

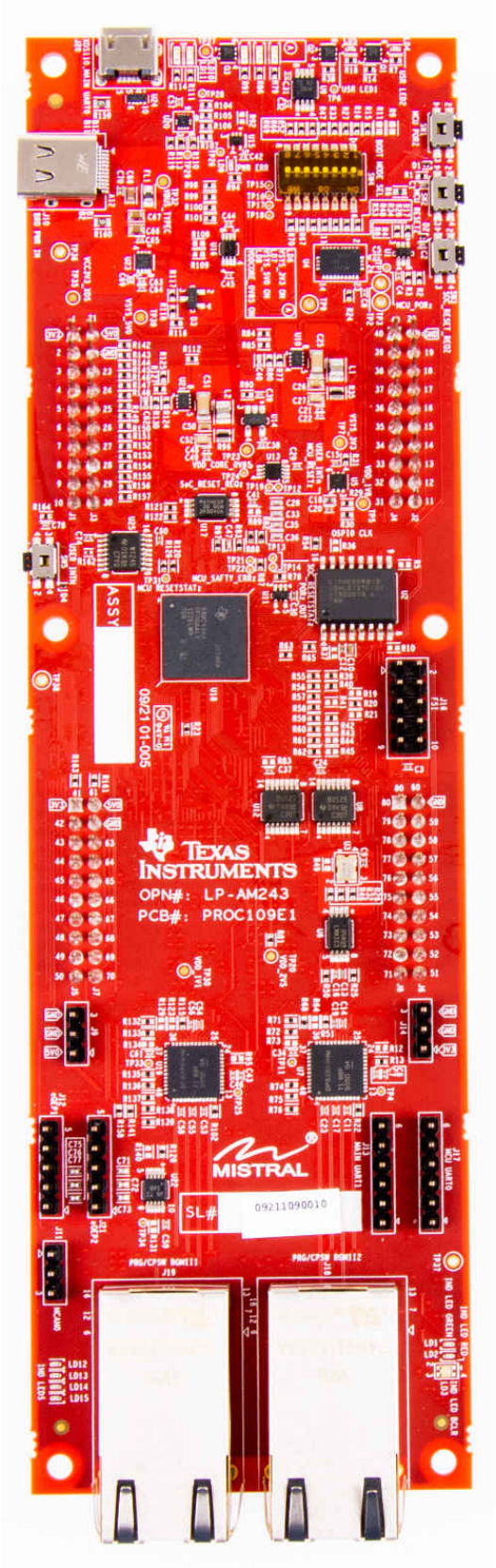

Figure 2-1. AM243x LaunchPad Board

Figure 2-2 shows the overall top level architecture of the AM243x LaunchPad.

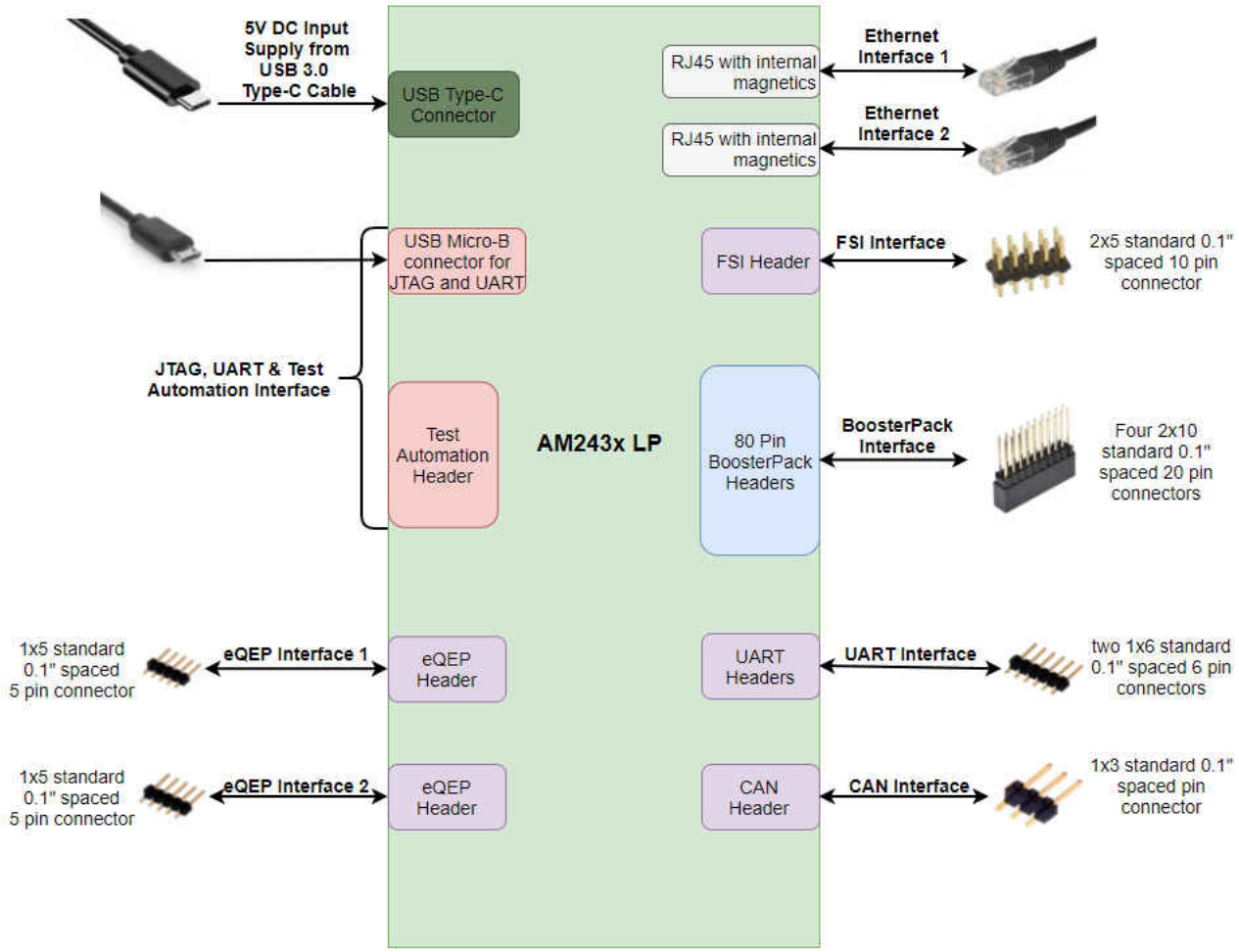

Figure 2-2. System Architecture

2.1 Kit Contents

The Sitara AM243x Series LaunchPad Development Kit contains the following items:

- AM243x Sitara Series LaunchPad development board
- USB type-C cable
- USB micro-B cable

2.2 Key Features

The AM243x LaunchPad has the following features:

- AM2434 (ALX) MCU
- PCB dimensions: 7.7 inch (195.58 mm) x 2.3 inch (58.42 mm)
- Powered through 5 V, 3A USB type-C input
- Two RJ45 Ethernet ports capable of 1Gb or 100Mb speeds
- On-board XDS110 debug probe
- Four push buttons:
  - PORz Reset
  - MCU warm reset
  - SoC warm reset
  - User interrupt

- LED indicators for:
  - Power status
  - User testing
  - Ethernet connection
  - Industrial application
- CAN connectivity with on-board CAN transceiver
- Two independent Enhanced Quadrature Encoder Pulse (QEP)-based encoder connectors
- Separate FSI connector
- Two independent BoosterPack XL (40 pin) standard connectors featuring stackable headers to maximize expansion through the BoosterPack ecosystem
- Test automation header
- On-Board Memory:
  - 512 Mb QSPI flash
  - 1 Mb I2C EEPROM

2.3 Component Identification

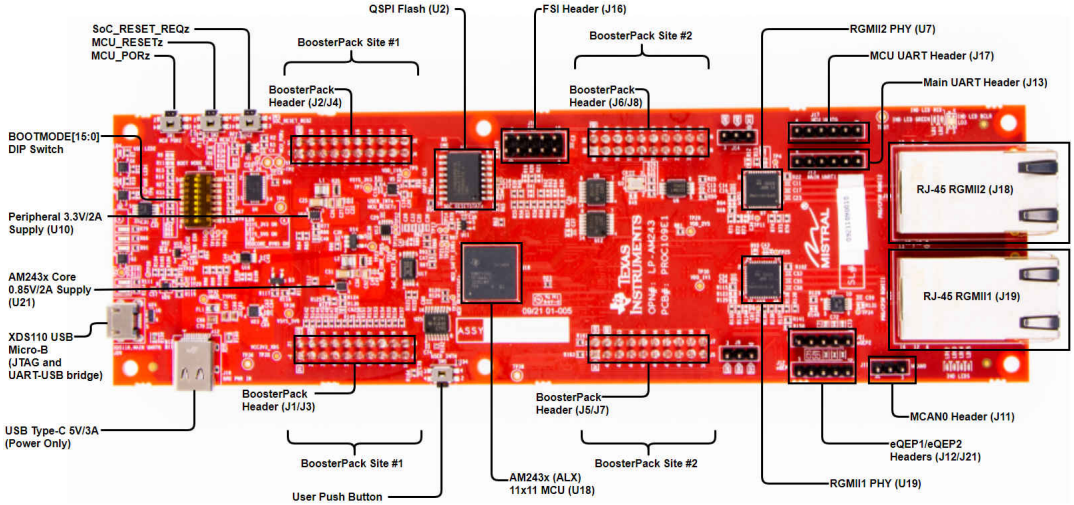

Figure 2-3. AM243x LaunchPad Top Component Identification

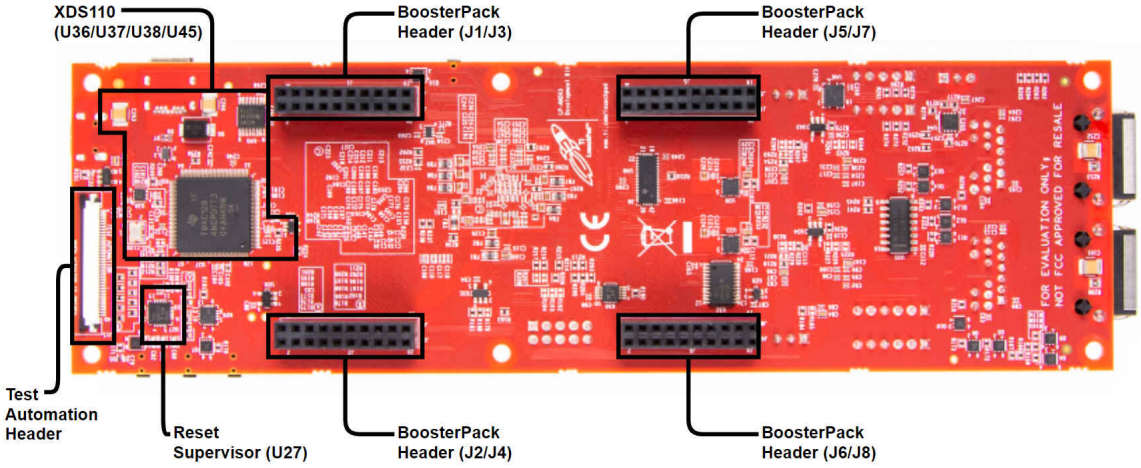

Figure 2-4. AM243x LaunchPad Bottom Component Identification

2.4 BoosterPacks

The AM243x LaunchPad development kit provides an easy and inexpensive way to develop applications with the AM243x Series microcontroller. BoosterPacks are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of BoosterPacks greatly expands the peripherals and potential applications that you can easily explore with the AM243x LaunchPad.

You can also build your own BoosterPack by following the design guidelines on TI's website. Texas Instruments even helps you promote your BoosterPack to other members of the community. TI offers a variety of avenues for you to reach potential customers with your solutions.

2.5 Compliance

All components selected meet RoHS and REACH compliance.

3 Board Setup

3.1 Power Requirements

The AM243x LaunchPad is powered from a 5 V, 3A USB type-C input. The following sections describe the power distribution network topology that supplied the AM243x LaunchPad, it is supporting components and the reference voltages.

3.1.1 Power Input Using USB Type-C Connector

The AM243x LaunchPad is powered through a USB type-C connection. The USB Type-C source should be capable of providing 3A at 5 V and should advertise the current sourcing capability through CC1 and CC2 signals. On AM243x LP, the CC1 and CC2 from USB type-C connector are interfaced to the port controller IC (TUSB320LAIRWBR). This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure it as upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the VUSB_5V0 power switch to provide the VSYS_5V0 supply which powers other regulators and LDOs.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM243x LP power requirement is 5 V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low that disables the VUSB_5V0 power switch. Therefore, if the power requirement is not met, all power supplies except VCC3V3_TA will remain in the off state. The board gets powered on completely only when the source can provide 5 V at 3A.

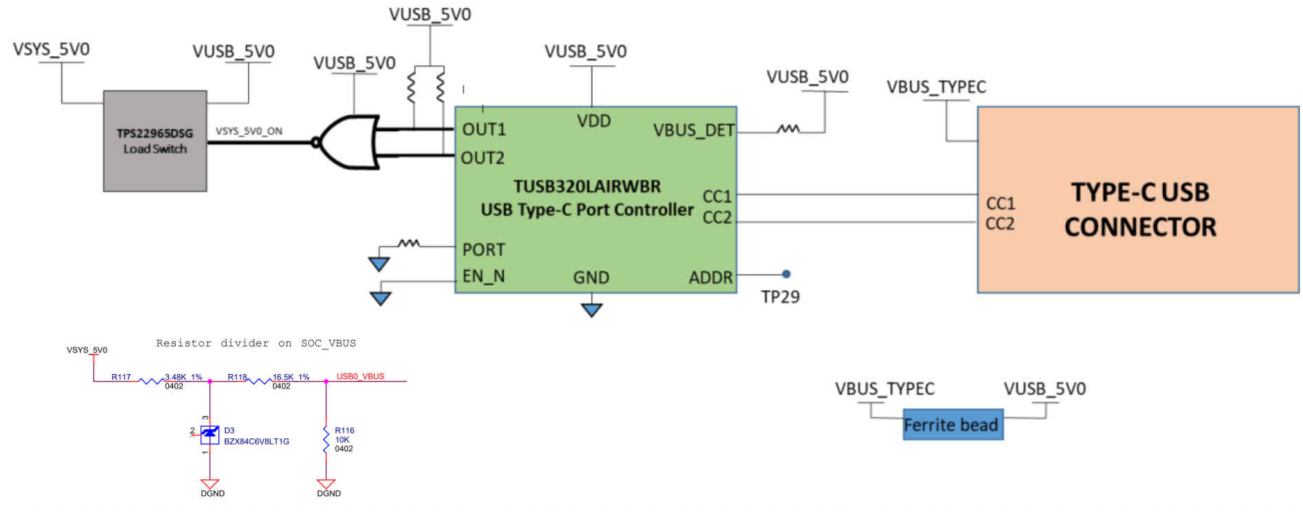

Figure 3-1. Type-C CC Configuration

Table 3-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM243x LaunchPad includes a power solution based on discrete regulators for each of the power rails. During the initial stage of the power supply, 5 V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the LaunchPad.

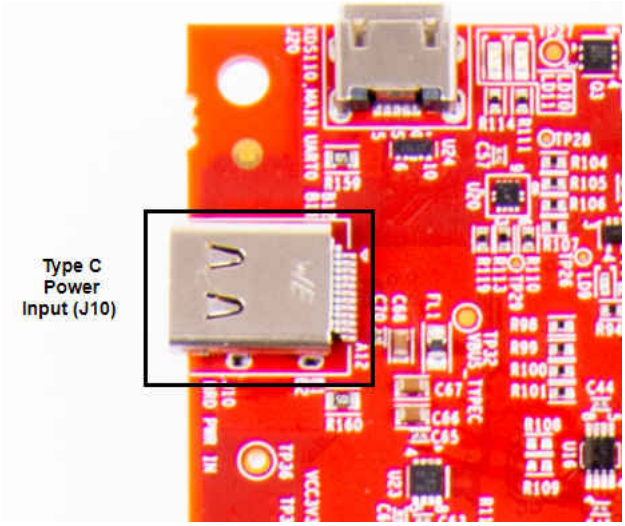

Figure 3-2. USB Type-C Power Input

Discrete DC-DC buck regulators and LDOs are used to generate the supplies required for the AM243x system on a chip (SoC) and other peripherals

Two DC-DC buck regulators (TPS62822) are used to generate the 3.3 V main supply and VDD_CORE_0V85 from the 5 V input supply.

3.1.2 Power Status LED's

Multiple power-indication LED's are provided on-board to indicate to users the output status of major supplies. The LED's indicate power across various domains as shown in Table 3-2.

Table 3-2. Power Status LED's

Name	Default Status	Operation	Function
LD9	OFF	VSYS_5V0_ERR	Power error indication for voltage - VUSB_5V0
LD7	ON	VSYS_5V0	Power indicator for voltage - VSYS_5V0
LD6	ON	VSYS_3V3	Power indicator for voltage -VSYS_3V3
LD8	ON	VDD_CORE_0V85	Power indicator for voltage - VDD_CORE_0V85
LD11	OFF	XDS110_PROG_STAZ1	LED will glow after XDS configuration
LD10	OFF	XDS110_PROG_STAZ2	

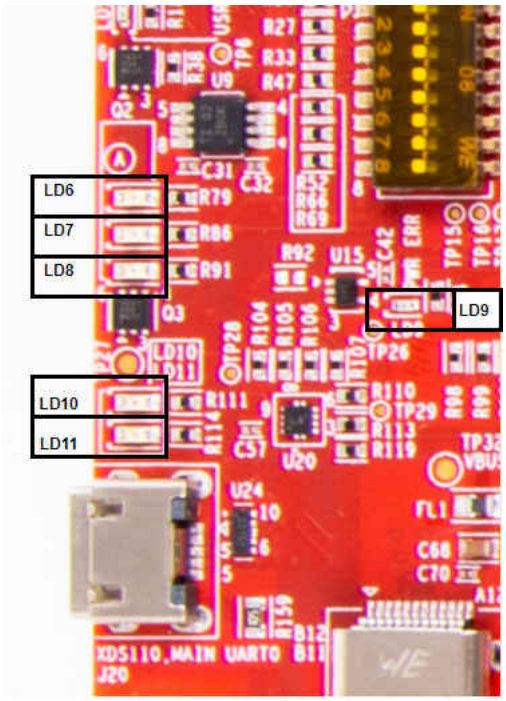

Figure 3-3. Power Status LED's

3.1.3 Power Tree

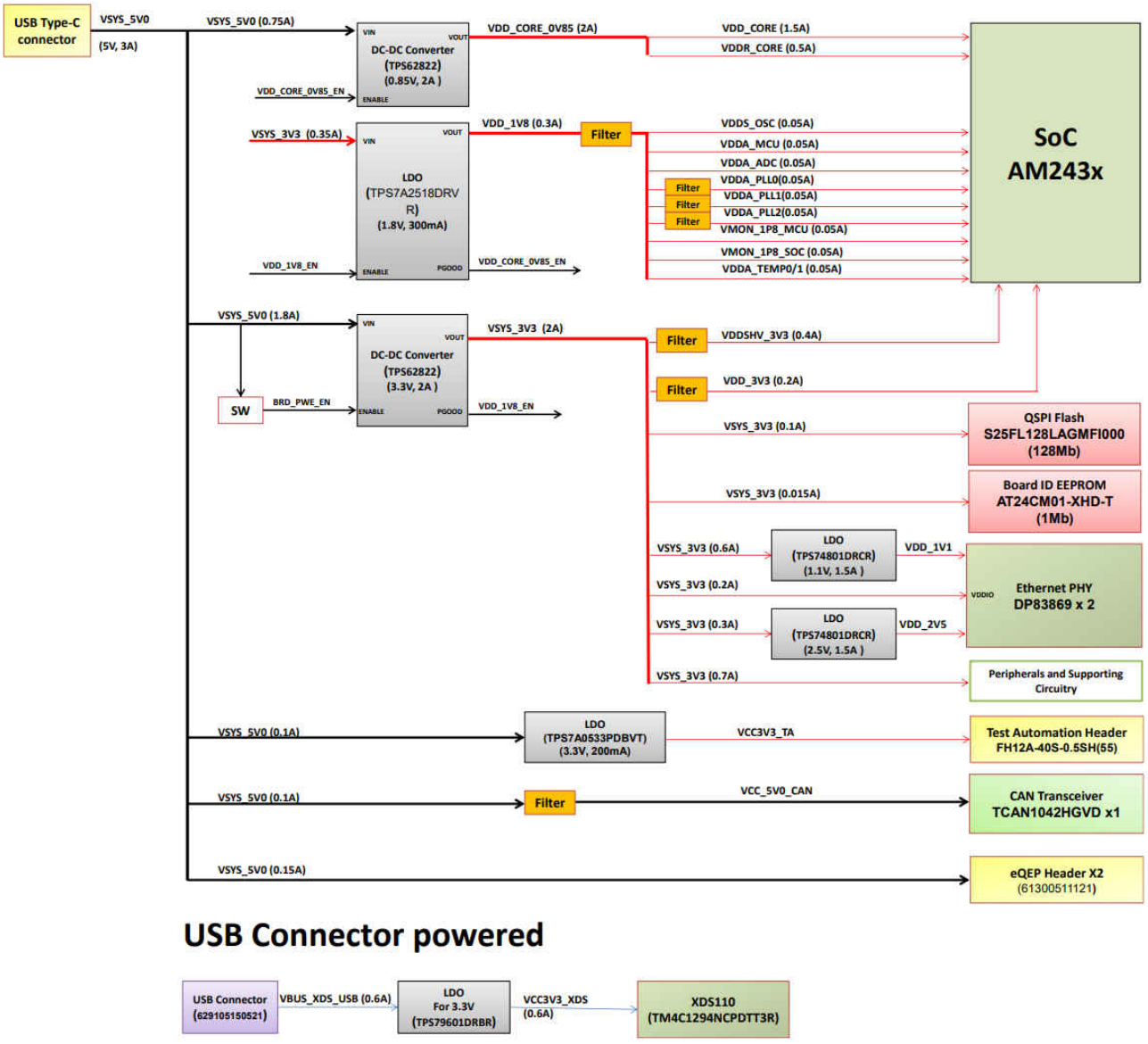

Figure 3-4. Power Tree Diagram of AM243x LaunchPad

3.1.4 Power Sequence

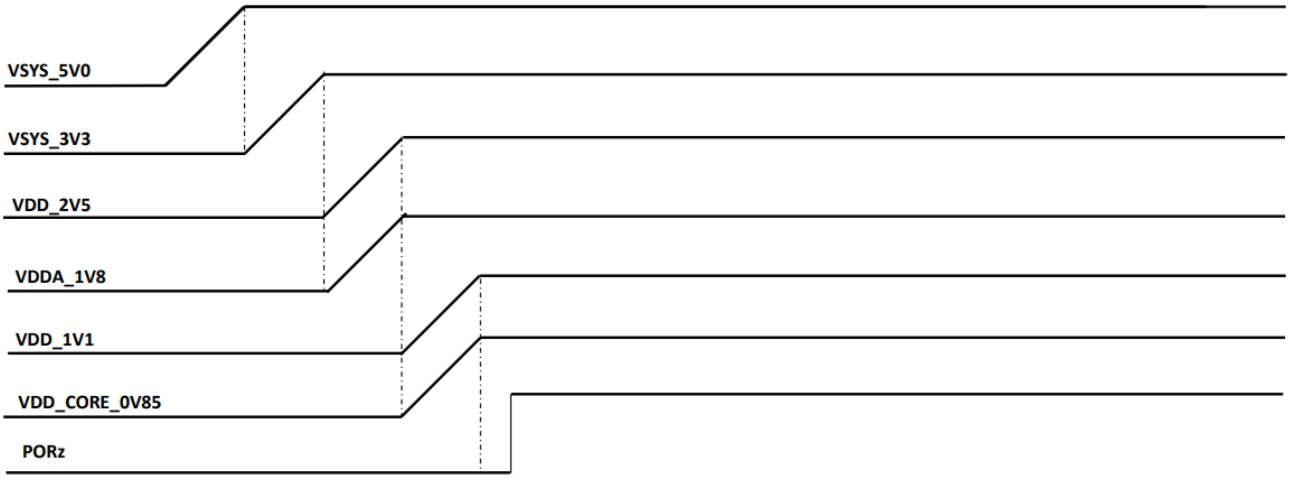

Figure 3-5. Power Sequence

3.2 Push Buttons

The LaunchPad supports multiple user push buttons that provide reset inputs and user interrupts to the processor.

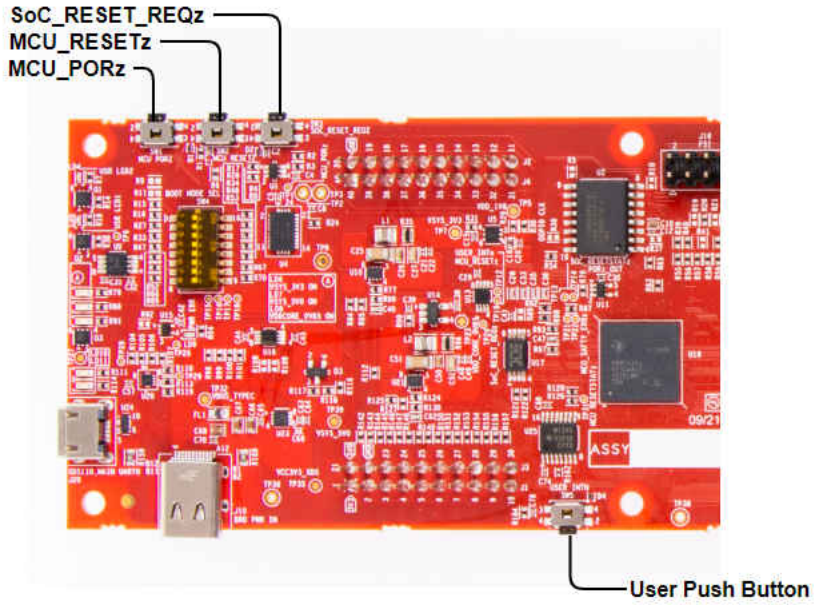

Table 3-3 lists the push buttons that are placed on the top side of the AM243x LaunchPad board.

Table 3-3. LaunchPad Push Buttons

SL #	Push Button	Signal	Function
1	SW1	MCU_PORz	PORz Reset input
2	SW2	MCU_RESETz	MCU warm reset input
3	SW3	SoC_RESET_REQz	SoC warm reset input
4	SW4	USER_INTn	User interrupt input

3.3 Boot Mode Selection

BOOTMODE[9:3] for the AM243x are selected by a DIP switch (SW4) or the test automation header. The remaining BOOTMODE[2:0] and BOOTMODE[12:10] are selected through the use of resistors. The test automation header uses an I2C IO expansion buffer to drive the bootmode when PORz is toggled. For more details about the test automation header, see Section 4.16. The supported boot modes are as follows:

- QSPI
- MMC - µSDCard (no direct support)
- Universal asynchronous receiver/transmitter (UART)
- USB-DFU
- No-boot

Table 3-4. Boot-Mode Selection Table

Boot Modes Supported	SW4.1	SW4.2	SW4.3	SW4.4	SW4.5	SW4.6	SW4.7
QSPI Flash	0	1	0	0	0	1	0
MMC1/SD Card	0	0	0	1	0	0	1
UART	1	1	1	0	0	0	0
USB -DFU	0	1	0	1	0	0	0
No Boot	1	1	1	1	0	0	0

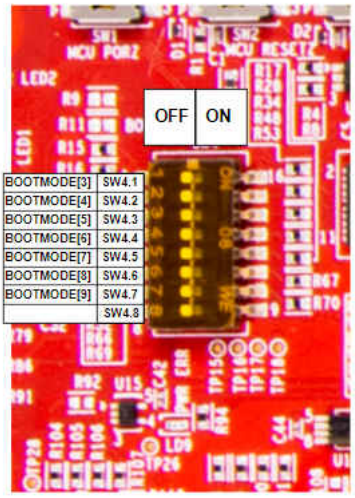

Figure 3-6. Boot-Mode DIP Switch

Note

SW4.8 of the DIP switch remains unused.

4 Hardware Description

4.1 Functional Block Diagram

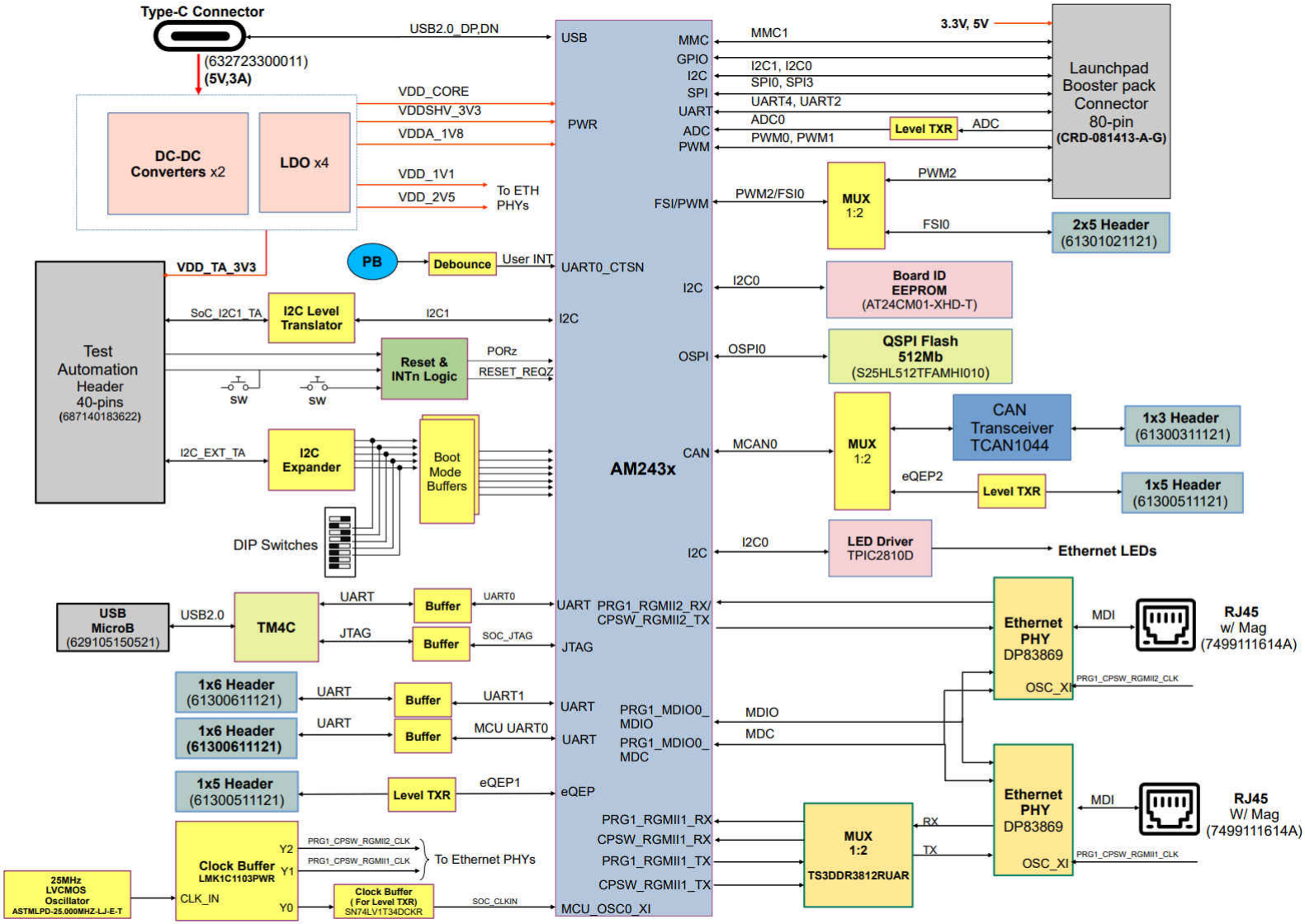

Figure 4-1. AM243x LaunchPad Functional Block Diagram

4.2 BoosterPack Headers

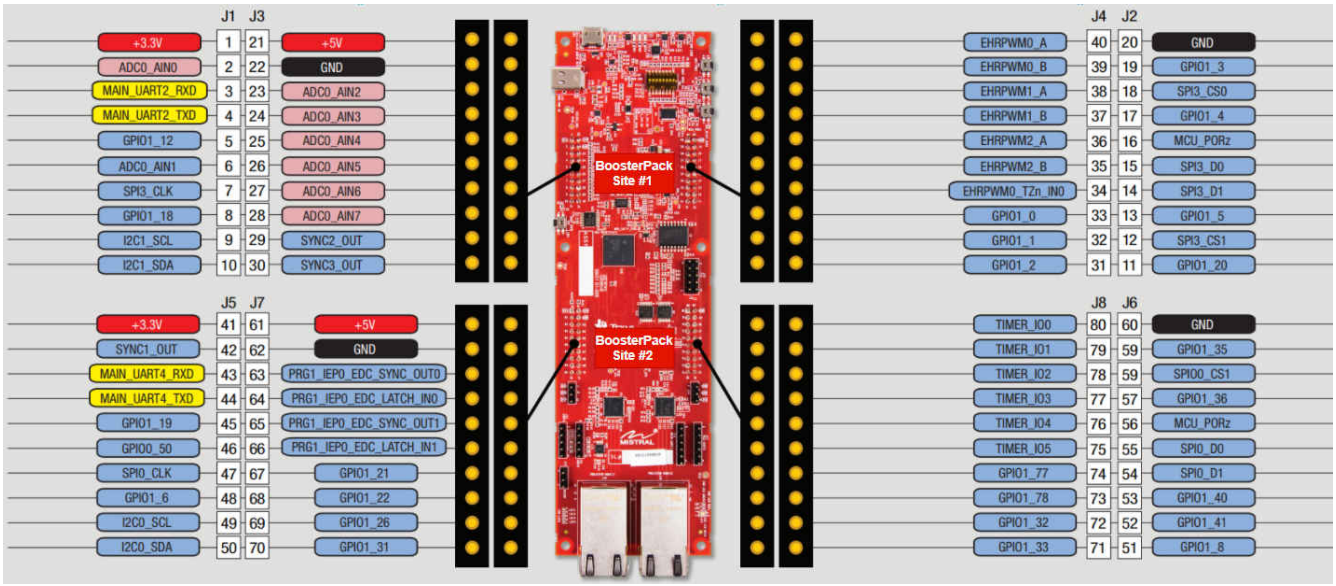

Figure 4-2. BoosterPack Header Pinout

The AM243x LaunchPad supports two fully independent BoosterPack XL connectors. BoosterPack site #1 (J1/J3, J2/J4) is located in between the SoC and the bootmode DIP switch. BoosterPack site #2 (J5/J7, J6/J8) is located in between the SoC and the RJ45 connectors. The GPIO pin numbers as well as the the BoosterPack compliant features are listed in Figure 4-2. Each GPIO has multiple functions available through the GPIO mux. The signals connected from the SoC to the BoosterPack headers include:

- SPI0 and SPI3
- UART0 and UART2
- I2C0 and I2C1
- MMC1
- ADC0
- EHRPWM0_A/B and EHRPWM1_A/B
- GPIO's
- 5 V and 3.3 V power supplies

A BoosterPack that is connected to site #1 will be powered by the AM243x. A BoosterPack that is connected to site #2 can either be powered by the AM243x or have it's power sourced from the Boosterpack itself depending on whether or not the 0Ω resistors (R161, R163) are mounted. The resistors are mounted by default as shown in Figure 4-3, the AM243x will provide the VSYS_3V3 and VSYS_5V0 source voltage for the BoosterPack. When left unpopulated, the BoosterPack will be required to source its own power.

Note

Sourcing power to the LaunchPad from the BoosterPack should not be attempted.

Table 4-1. BoosterPack Power Sourcing for BoosterPack Site #2

Function	Mount R161 and R163 (Default)	Unmount R161 and R163
Power to BoosterPack sourced from LaunchPad	✓	
Power to BoosterPack sourced from the BoosterPack		✓

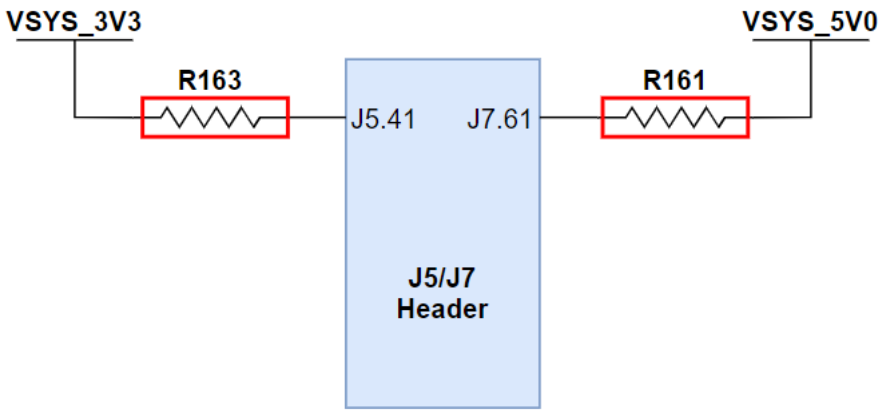

Figure 4-3. Site #2 BoosterPack Header

4.2.1 Pinmux for BoosterPack

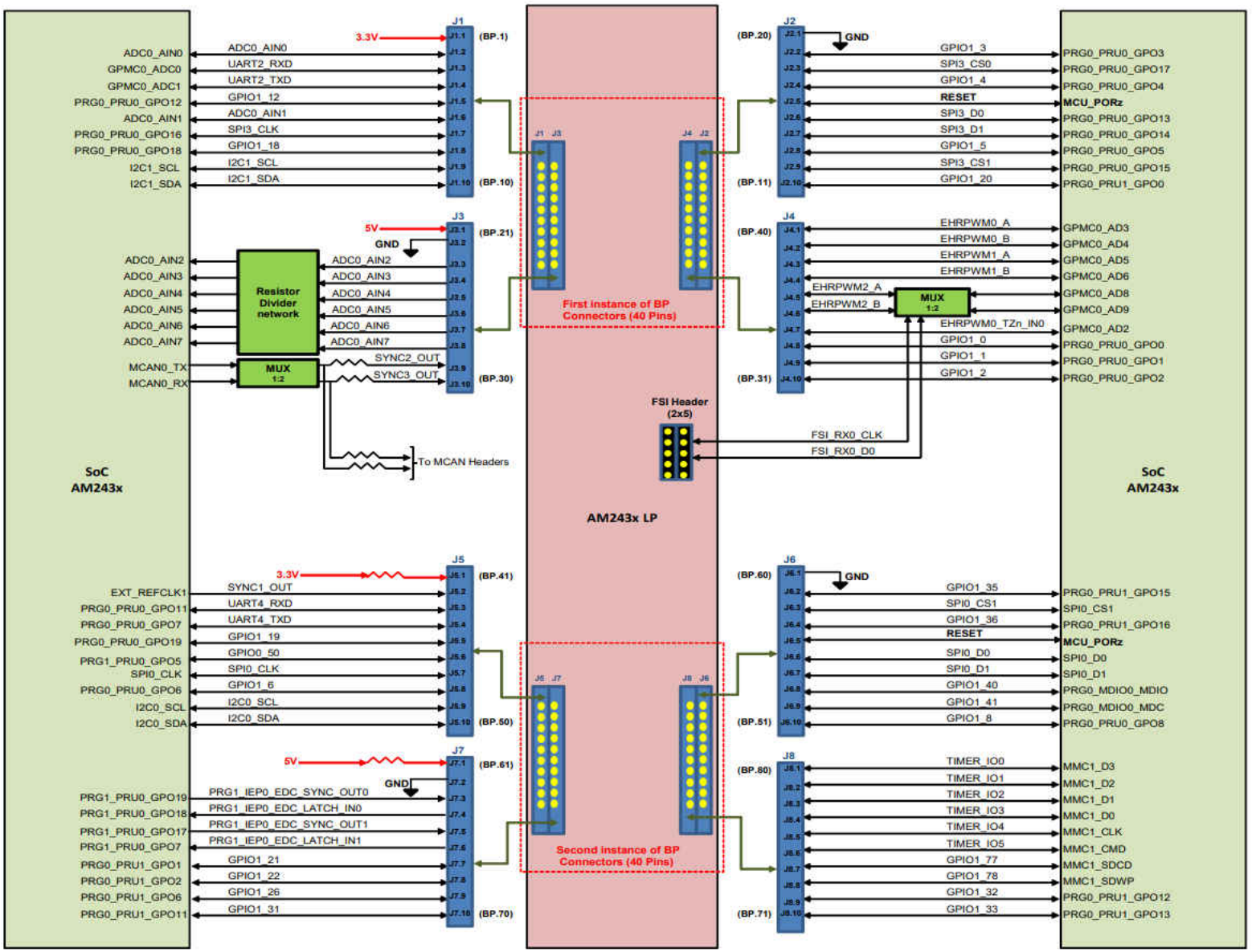

Figure 4-4. 80 Pin BoosterPack Pinout

The various pinmux options in different modes for Booterpack Connector pins are given below. The default modes of the pins are shown in Figure 4-2 and in **bold** in the tables below.

Table 4-2. Pinmux Options for J1/J3 Connector - Site 1

Connector Pinout	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J1.1											
J3.21											
J1.2	**ADC_AIN0**							GPIO1_80			
J3.22											
J1.3	GPMC0_ADC0	FSI_RX2_CLK	**UART2_RXD**	EHRPWM0_SYNCI			TRC_CLK	GPIO0_15			
J3.23	**ADC0_AIN2**							GPIO1_82			
J1.4	GPMC0_AD1	FSI_RX2_D0	**UART2_TXD**	EHRPWM0_SYNC0			TRC_CTL	GPIO0_16		PRG0_PWM2_TZ_OUT	
J3.24	**ADC0_AIN3**							GPIO1_83			
J1.5	PRG0_PRU0_GPO12	PRG0_PRU0_GPI12	PRG0_RGMII1_TD1	PRG0_PWM0_A0				**GPIO1_12**		GPMC0_A14	
J3.25	**ADC_AIN4**							GPIO1_84			
J1.6	**ADC0_AIN1**							GPIO1_81			
J3.26	**ADC0_AIN5**							GPIO1_85			
J1.7	PRG0_PRU0_GPO16	PRG0_PRU0_GPI16	PRG0_RGMII1_TXC	PRG0_PWM0_A2			**SPI3_CLK**	GPIO1_16		GPMC0_A4	
J3.27	**ADC0_AIN6**							GPIO1_86			
J1.8	PRG0_PRU0_GPO18	PRG0_PRU0_GPI18	PRG0_IEP0_EDC_LATCH_IN0	PRG0_PWM0_TZ_IN	CPTS0_HW1TSPUSH	CP_GEMAC_CPTS0_HW1TSPUSH	HRPWM8_A	**GPIO1_18**	UART4_CTSn	GPMC0_A5	UART2_RXD
J3.28	**ADC0_AIN7**							GPIO1_87			
J1.9	**I2C1_SCL**	CPTS0_HW1TSPUSH	TIMER_IO0	SPI2_CS1		DDR0_IO_PLL_TESTOUT0P	DDR0_IO_PLL_TESTOUT1P	GPIO1_66			
J3.29	MCAN0_TX	UART4_RXD	TIMER_IO2	**SYNC2_OUT**			SPI4_CS1	GPIO1_60	EQEP2_I	UART0_DTRn	
J1.10	**I2C1_SDA**	CPTS0_HW2TSPUSH	TIMER_IO1	SPI2_CS2		DDR0_IO_PLL_REFCLK_TEST0P	DDR0_IO_PLL_REFCLK_TEST1P	GPIO1_67			
J3.30	MCAN0_RX	UART4_TXD	TIMER_IO3	**SYNC3_OUT**			SPI4_CS2	GPIO1_61	EQEP2_S	UART0_RIn	

Table 4-3. Net Name in Schematic and Package Signal Name for J1/J3 Connector

Connector Pinout	Net Name in Schematic	Package Signal Name
J1.1	VSYS_3V3	
J3.21	VSYS_5V0	
J1.2	BP_ADC0_AINN0	ADC_AIN0
J3.22	DGND	
J1.3	MAIN_UART2_RXD	GPMC0_AD0
J3.23	BP_ADC0_AIN2	ADC0_AIN2
J1.4	MAIN_UART2_TXD	GPMC0_AD1
J3.24	BP_ADC0_AIN3	ADC0_AIN3
J1.5	GPIO1_12	PRG0_PRU0_GPO12
J3.25	BP_ADC0_AIN4	ADC0_AIN4
J1.6	BP_ADC0_AIN1	ADC0_AIN1
J3.26	BP_ADC0_AIN5	ADC0_AIN5
J1.7	SPI3_CLK	PRG0_PRU-_GPO16
J3.27	BP_ADC0_AIN6	ADC0_AIN6
J1.8	GPIO1_18	PRG0_PRU0_GPO18
J3.28	BP_ADC0_AIN7	ADC0_AIN7
J1.9	SOC_I2C1_SCL	I2C1_SCL
J3.29	SYNC2_OUT	MCAN0_TX
J1.10	SOC_I2C1_SDA	I2C1_SDA
J3.30	SYNC3_OUT	MCAN0_RX

Table 4-4. Pinmux Options for J2/J4 Connector - Site 1

Connector Pinout	Net Name in Schematic	Package Signal Name	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J4.40	EHRPWM0_A	GPMC0_AD3	GPMC0_AD3	FSI_RX3_CLK	UART3_RXD	**EHRPWM0_A**			TRC_DATA1	GPIO0_18		PRG0_PWM2_A0	
J2.20	DGND												
J4.39	EHRPWM0_B	GPMC0_AD4	GPMC0_AD4	FSI_RX3_D0	UART3_TXD	**EHRPWM0_B**			TRC_DATA2	GPIO0_82		PRG0_PWM2_B0	
J2.19	GPIO1_3	PRG0_PRU0_GPO3	PRG0_PRU0_GPO3	PRG0_PRU0_GPI3	PRG0_RGMII1_RD3	PRG0_PWM3_A2				**GPIO1_3**			UART3_CTSn
J4.38	EHRPWM1_A	GPMC0_AD5	GPMC0_AD5	FSI_RX3_D1	UART3_RTSn	**EHRPWM1_A**			TRC_DATA3	GPIO0_83		PRG0_PWM2_A1	
J2.18	SPI3_CS0	PRG0_PRU0_GPO17	PRG0_PRU0_GPO17	PRG0_PRU0_GPI17	PRG0_IEP0_EDC_SYNC_OUT1	PRG0_PWM0_B2	CPTS0_TS_SYNC	CP_GEMAC_CPTS0_TS_SYNC	**SPI3_CS0**	GPIO1_17	TIMER_IO11	GPMC0_A17	
J4.37	EHRPWM1_B	GPMC0_AD6	GPMC0_AD6	FSI_RX4_D0	UART4_RXD	**EHRPWM1_B**			TRC_DATA4	GPIO0_21		PRG0_PWM2_B1	
J2.17	GPIO1_4	PRG0_PRU0_GPO4	PRG0_PRU0_GPO4	PRG0_PRU0_GPI4	PRG0_RGMII1_RX_CTL	PRG0_PWM2_B0				**GPIO1_4**		GPMC0_A1	UART3_TXD
J4.36	EHRPWM2_A	GPMC0_AD8	GPMC0_AD8	FSI_RX0_CLK	UART2_CTSn	**EHRPWM2_A**			TRC_DATA6	GPIO0_23		PRG0_PWM2_A2	
J2.16	BP_CONN_1_PORZ												
J4.35	EHRPWM2_B	GPMC0_AD9	GPMC0_AD9	FSI_RX0_D0	UART3_CTSn	**EHRPWM2_B**			TRC_DATA7	GPIO0_24		PRG0_PWM2_B2	
J2.15	SPI3_D0	PRG0_PRU0_GPO13	PRG0_PRU0_GPO13	PRG0_PRU0_GPI13	PRG0_RGMII1_TD2	PRG0_PWM0_B0			**SPI3_D0**	GPIO1_13		GPMC0_A15	
J4.34	EHRPWM0_TZN_IN0	GPMC0_AD2	GPMC0_AD2	FSI_RX2_D1	UART2_RTSn	**EHRPWM_TZn_IN0**			TRC_DATA0	GPIO0_17		PRG0_PWM2_TZ_IN	
J2.14	SPI3_D1	PRG0_PRU0_GPO14	PRG0_PRU0_GPO14	PRG0_PRU0_GPI14	PRG0_RGMII1_TD3	PRG0_PWM0_A1			**SPI3_D1**	GPIO1_14		GPMC0_A3	
J4.33	GPIO1_0	PRG0_PRU0_GPO0	PRG0_PRU0_GPO0	PRG0_PRU0_GPI0	PRG0_RGMII1_RD0	PRG0_PWM3_A0				**GPIO1_0**			UART2_CTSn
J2.13	GPIO1_5	PRG0_PRU0_GPO5	PRG0_PRU0_GPO5	PRG0_PRU0_GPI5	PRG0_PWM3_B2					**GPIO1_5**			UART3_RTSn
J4.32	GPIO1_1	PRG0_PRU0_GPO1	PRG0_PRU0_GPO1	PRG0_PRU0_GPI1	PRG0_RGMII1_RD1	PRG0_PWM3_B0				**GPIO1_1**			UART2_TXD
J2.12	SPI3_CS1	PRG0_PRU0_GPO15	PRG0_PRU0_GPO15	PRG0_PRU0_GPI15	PRG0_RGMII1_TX_CTL	PRG0_PWM0_B1			**SPI3_CS1**	GPIO1_15			GPMC0_A16
J4.31	GPIO1_2	PRG0_PRU0_GPO2	PRG0_PRU0_GPO2	PRG0_PRU0_GPI2	PRG0_RGMII1_RD2	PRG0_PWM2_A0				**GPIO1_2**		GPMC0_A0	UART2_RTSn
J2.11	GPIO1_20	PRG0_PRU1_GPO0	PRG0_PRU1_GPO0	PRG0_PRU1_GPI0	PRG0_RGMII2_RD0					**GPIO1_20**	EQEP0_A		UART5_CTSn

Table 4-5. Net Name in Schematic and Package Signal Name for J2/J4 Connector

Connector Pinout	Net Name in Schematic	Package Signal Name
J4.40	EHRPWM0_A	GPMC0_AD3
J2.20	DGND	
J4.39	EHRPWM0_B	GPMC0_AD4
J2.19	GPIO1_3	PRG0_PRU0_GPO3
J4.38	EHRPWM1_A	GPMC0_AD5
J2.18	SPI3_CS0	PRG0_PRU0_GPO17
J4.37	EHRPWM1_B	GPMC0_AD6
J2.17	GPIO1_4	PRG0_PRU0_GPO4
J4.36	EHRPWM2_A	GPMC0_AD8
J2.16	BP_CONN_1_PORZ	
J4.35	EHRPWM2_B	GPMC0_AD9
J2.15	SPI3_D0	PRG0_PRU0_GPO13
J4.34	EHRPWM0_TZN_IN0	GPMC0_AD2
J2.14	SPI3_D1	PRG0_PRU0_GPO14
J4.33	GPIO1_0	PRG0_PRU0_GPO0
J2.13	GPIO1_5	PRG0_PRU0_GPO5
J4.32	GPIO1_1	PRG0_PRU0_GPO1
J2.12	SPI3_CS1	PRG0_PRU0_GPO15
J4.31	GPIO1_2	PRG0_PRU0_GPO2
J2.11	GPIO1_20	PRG0_PRU1_GPO0

Table 4-6. Pinmux Options for J5/J7 Connector - Site 2

Connector Pinout	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J5.41											
J7.61											
J5.42	EXT_REFCLK1	**SYNC1_OUT**	SPI2_CS3			CLKOUT0		GPIO1_69			
J7.62											
J5.43	PRG0_PRU0_GPO11	PRG0_PRU0_GPI11	PRG0_RGMII1_TD0	PRG0_PWM3_TZ_OUT				GPIO1_11			**UART4_RXD**
J7.63	PRG1_PRU0_GPO19	PRG1_PRU0_GPI19	**PRG1_IEP0_EDC_SYNC_OUT0**	PRG1_PWM0_TZ_OUT	CPTS0_TS_COMP		TIMER_IO9	GPIO0_64	GPMC0_A2		
J5.44	PRG0_PRU0_GPO7	PRG0_PRU0_GPI7	PRG0_IEP0_EDC_LATCH_IN1	PRG0_PWM3_B1	CPTS0_HW2TSPUSH	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO6	GPIO1_7			**UART4_TXD**
J7.64	PRG1_PRU0_GPO18	PRG1_PRU0_GPI18	**PRG1_IEP0_EDC_LATCH_IN0**	PRG1_PWM0_TZ_IN	CPTS0_HW1TSPUSH		TIMER_IO8	GPIO0_63	GPMC0_A1		
J5.45	PRG0_PRU0_GPO19	PRG0_PRU0_GPI19	PRG0_IEP0_EDC_SYNC_OUT0	PRG0_PWM0_TZ_OUT	CPTS0_TS_COMP	CP_GEMAC_CPTS0_TS_COMP	EHRPWM8_B	**GPIO1_19**	UART4_RTSn	GPMC0_A6	UART3_RXD
J7.65	PRG1_PRU0_GPO17	PRG1_PRU0_GPI17	**PRG1_IEP0_EDC_SYNC_OUT1**	PRG1_PWM0_B2	CPTS0_TS_SYNC		TIMER_IO7	GPIO0_62	GPMC0_A0		
J5.46	PRG1_PRU0_GPO5	PRG1_PRU0_GPI5		PRG1_PWM3_B2	RGMII1_RX_CTL			**GPIO0_50**	GPMC0_AD21		
J7.66	PRG1_PRU0_GPO7	PRG1_PRU0_GPI7	**PRG1_IEP0_EDC_LATCH_IN1**	PRG1_PWM3_B1	CPTS0_HW2TSPUSH	CLKOUT0	TIMER_IO10	GPIO0_52	GPMC0_AD23		
J5.47	**SPI0_CLK**							GPIO1_44			
J7.67	PRG0_PRU1_GPO1	PRG0_PRU1_GPI1	PRG0_RGMII2_RD1					**GPIO1_21**	EQEP0_B		UART5_TXD
J5.48	PRG0_PRU0_GPO6	PRG0_PRU0_GPI6	PRG0_RGMII1_RXC	PRG0_PWM3_A1				**GPIO1_6**			UART4_CTSn
J7.68	PRG0_PRU1_GPO2	PRG0_PRU1_GPI2	PRG0_RGMII2_RD2	PRG0_PWM2_A2				**GPIO1_22**	EQEP0_S		UART5_RTSn
J5.49	**I2C0_SCL**				UART6_CTSn			GPIO1_64			
J7.69	PRG0_PRU1_GPO6	PRG0_PRU1_GPI6	PRG0_RGMII2_RXC					**GPIO1_26**	EQEP2_A	GPMC0_A19	UART4_CTSn
J5.50	**I2C0_SDA**				UART6_RTSn			GPIO1_65			
J7.70	PRG0_PRU1_GPO11	PRG0_PRU1_GPI11	PRG0_RGMII2_TD0					**GPIO1_31**	EQEP2_I		UART4_RXD

Table 4-7. Net Name in Schematic and Package Signal Name for J5/J7 Connector

Connector Pinout	Net Name in Schematic	Package Signal Name
J5.41	BP_3V3	
J7.61	B5_5V0	
J5.42	SYNC1_OUT	EXT_REFCLK1
J7.62	DGND	
J5.43	MAIN_UART4_RXD	PRG0_PRU0_GPO11
J7.63	PRG1_IEP0_EDC_SYNC_OUT0	PRG1_PRU0_GPO19
J5.44	MAIN_UART4_TXD	PRG0_PRU0_GPO7
J7.64	PRG1_IEP0_EDC_LATCH_IN0	PRG1_PRU0_GPO18
J5.45	GPIO1_19	PRG0_PRU0_GPO19
J7.65	PRG1_IEP0_EDC_SYNC_OUT1	PRG1_PRU0_GPO17
J5.46	GPIO0_50	PRG1_PRU0_GPO5
J7.66	PRG1_IEP0_EDC_LATCH_IN1	PRG1_PRU0_GPO7
J5.47	SPI0_CLK	SPI0_CLK
J7.67	GPIO1_21	PRG0_PRU1_GPO1
J5.48	GPIO1_6	PRG0_PRU0_GPO6
J7.68	GPIO1_22	PRG0_PRU1_GPO2
J5.49	SOC_I2C0_SCL_BP	I2C0_SCL
J7.69	GPIO1_26	PRG0_PRU1_GPO6
J5.50	SOC_I2C0_SDA_BP	I2C0_SDA
J7.70	GPIO1_31	PRG0_PRU1_GPO11

Table 4-8. Pinmux Options for J6/J8 Connector - Site 2

Connector Pinout	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J8.80	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	**TIMER_IO0**	UART2_RXD				GPIO1_71			
J6.60											
J8.79	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	**TIMER_IO1**	UART2_TXD				GPIO1_72			
J6.59	PRG0_PRU1_GPO15	PRG0_PRU1_GPI15	PRG0_RGMII2_TX_CTL	PRG0_PWM1_B1				**GPIO1_35**		GPMC0_A10	PRG0_ECAP0_IN_APWM_OUT
J8.78	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	**TIMER_IO2**	UART3_RXD				GPIO1_73			
J6.58	**SPI0_CS1**	CPTS0_TS_COMP	I2C2_SCL	TIMER_IO10	PRG0_IEP0_EDIO_OUTVALID	UART6_RXD	ADC_EXT_TRIGGER0	GPIO1_43			
J8.77	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	**TIMER_IO3**	UART3_TXD				GPIO1_74			
J6.57	PRG0_PRU1_GPO16	PRG0_PRU1_GPI16	PRG0_RGMII2_TXC	PRG0_PWM1_A2				**GPIO1_36**		GPMC0_A11	PRG0_ECAP0_SYNC_OUT
J8.76	MMC1_CLK	UART2_CTSn	**TIMER_IO4**	UART4_RXD				GPIO1_75			
J6.56	BP_CONN_2_PORZ										
J8.75	MMC1_CMD	UART2_RTSn	**TIMER_IO5**	UART4_TXD				GPIO1_76			
J6.55	**SPI0_D0**							GPIO1_45			
J8.74	MMC1_SDCD	UART3_CTSn	TIMER_IO6	UART5_RXD				**GPIO1_77**			
J6.54	**SPI0_D1**							GPIO1_46			
J8.73	MMC1_SDWP	UART3_RTSn	TIMER_IO7	UART5_TXD				**GPIO1_78**			
J6.53	PRG0_MDIO0_MDIO							**GPIO1_40**		GPMC0_A12	
J8.72	PRG0_PRU1_GPO12	PRG0_PRU1_GPI12	PRG0_RGMII2_TD1	PRG0_PWM1_A0				**GPIO1_32**	EQEP2_B	GPMC0_A7	UART4_TXD
J6.52	PRG0_MDIO0_MDC							**GPIO1_41**		GPMC0_A13	
J8.71	PRG0_PRU1_GPO13	PRG0_PRU1_GPI13	PRG0_RGMII2_TD2	PRG0_PWM1_B0				**GPIO1_33**	EQEP0_I	GPMC0_A8	UART5_RXD
J6.51	PRG0_PRU0_GPO8	PRG0_PRU0_GPI8	PRG0_PWM2_A1					**GPIO1_8**		GPMC0_A2	UART4_RTSn

Table 4-9. Net Name in Schematic and Package Signal Name for J6/J8 Connector

Connector Pinout	Net Name in Schematic	Package Signal Name
J8.80	TIMER_IO0	MMC1_DAT3
J6.60	DGND	
J8.79	TIMER_IO1	MMC1_DAT2
J6.59	GPIO1_35	PRG0_PRU1_GPO15
J8.78	TIMER_IO2	MMC1_DAT1
J6.58	SPI0_CS1	SPI0_CS1
J8.77	TIMER_IO3	MMC1_DAT0
J6.57	GPIO1_36	PRG0_PRU1_GPO16
J8.76	TIMER_IO4	MMC1_CLK
J6.56	BP_CONN_2_PORZ	
J8.75	TIMER_IO5	MMC1_CMD
J6.55	SPI0_D0	SPI0_D0
J8.74	GPIO1_77	MMC1_SDCD
J6.54	SPI0_D1	SPI0_D1
J8.73	GPIO1_78	MMC1_SDWP
J6.53	GPIO1_40	PRG0_MDIO0_MDIO
J8.72	GPIO1_32	PRG0_PRU1_GPO12
J6.52	GPIO1_41	PRG0_MDIO0_MDC
J8.71	GPIO1_33	PRG0_PRU1_GPO13
J6.51	GPIO1_8	PRG0_PRU0_GPO8

4.3 GPIO Mapping

Table 4-10 describes the detailed GPIO mapping of the SoC with the LaunchPad peripherals.

Table 4-10. GPIO Mapping Table

Net Name	Package Signal Name	GPIO Number	Input or Output	Default	State	Function
TEST_LED1_GREEN	GPMC0_AD7	GPIO0_22	Output	PD	Active High	To turn on the green test LED
TEST_LED2_RED	UART0_RTSN	GPIO1_55	Output	PD	Active High	To turn on the red test LED
TEST_LED3_RED	PRG1_PRU1_GPO18	GPIO1_39	Output	PD	Active High	To turn the bicolor LED red
TEST_LED4_GREEN	PRG1_PRU1_GPO19	GPIO1_38	Output	PD	Active High	To turn the bicolor LED green
USER_LED1	GPMC0_AD11	GPIO0_26	Output	PD	Active High	To turn on the green user LED1
USER_LED2	GPMC0_AD15	GPIO0_30	Output	PD	Active High	to turn on the green user LED2
USER_INTn	UART_CTSN	GPIO1_54	Input	PU	Active Low	User interrupt input from push button switch
OSPI0_RESET_N	OSPI0_CSN1	GPIO0_12	Ouput	PU	Active Low	To reset the QSPI FLASH on OSPI0 interface
MCAN/eQEP_MUX_SEL	PRG0_PRU1_GPO8	GPIO1_28	Output	PD	N/A	To select the functionality of MCAN0_RX pin as MCAN0_RX or eQEP_I
FSI/BP_MUX_SEL	GPMC0_AD13	GPIO0_28	Output	PD	N/A	To select the functionality of GPMC0_AD8 and GPMC0_AD9 pins as FSI_RX or PWM
MCAN0_STB	PRG0_PRU1_GPO5	GPIO1_25	Output	PU	Active Low	To put the CAN transceiver out of standby
PRG_CPSW_RGMII1_MUX_SEL	PRG1_PRU1_GPO5	GPIO0_70	Output	PD	N/A	To select the RGMII1 path between PRG and CPSW
GPIO_RGMII1_PHY_RSTn	PRG1_PRU1_GPO8	GPIO0_73	Output	PU	Active Low	To reset the RGMII1 Ethernet PHY
GPIO_RGMII2_PHY_RSTn	PRG1_PRU1_GPO18	GPIO0_20	Output	PU	Active Low	To reset the RGMII2 Ethernet PHY
PRG1_CPSW_RGMII_INTn	PRG1_PRU1_GP19	GPIO0_84	Input	PU	Active Low	Interrupt signal from both RGMII1 & RGMII2 Ethernet PHY's
GPIO0_50	PRG1_PRU0_GPO5	GPIO0_50	IO	NA	NA	GPIO connected to BoosterPack header

Table 4-10. GPIO Mapping Table (continued)

Net Name	Package Signal Name	GPIO Number	Input or Output	Default	State	Function
VPP_1V8_REG_EN	PRG1_PRU0_GPO8	GPIO0_53	Output	PD	Active High	To enable the VPP Regulator for eFUSE Programming

4.4 Reset

Figure 4-5 shows the reset architecture of the AM243x LaunchPad.

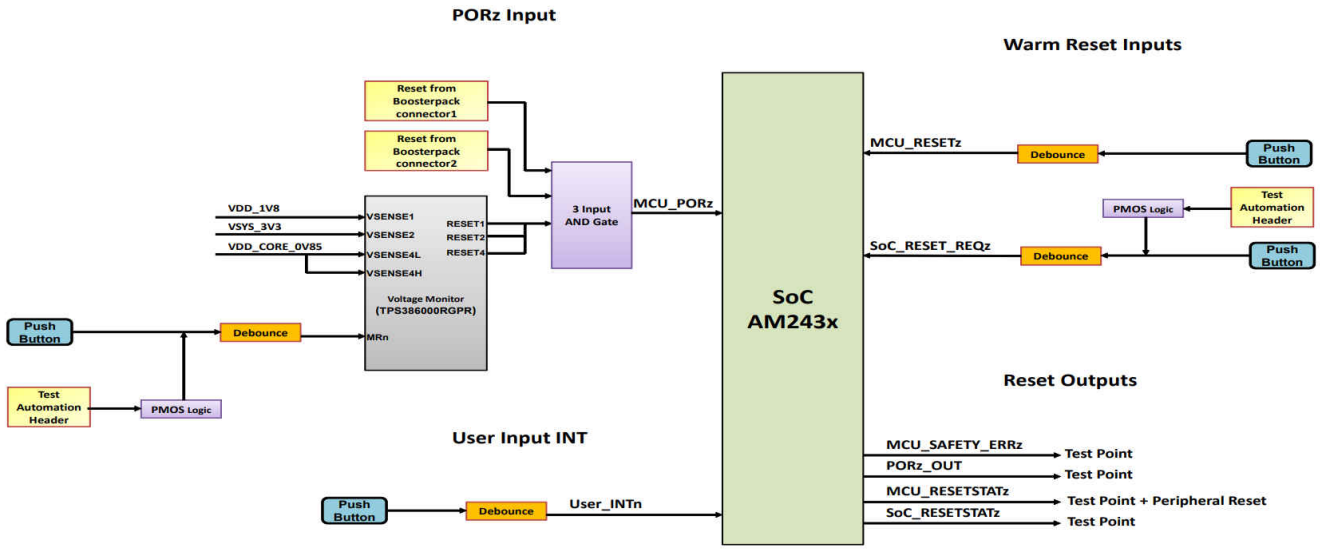

Figure 4-5. Reset Architecture

The SoC has the following resets:

- MCU_PORz is the power ON/Cold Reset input for MCU and MAIN domain
- PORz_OUT is the power ON reset status output from MAIN and MCU domain
- MCU_RESETz is the warm reset input for MCU domain
- MCU_RESETSTATz is the warm reset status output for the MCU domain
- RESET_REQz is the warm reset input for the MAIN domain
- RESETSTATz is the warm reset status output for the MAIN domain

Three push button switches are available to provide reset for MCU_PORz, MCU_RESETz and RESET_REQz as seen in Section 3.2.

MCU_PORz signal is provided by the outputs of a voltage monitor IC (TPS386000RGPR) for the core and peripheral voltages where the enable of this voltage monitor is controlled by the PORz signal from the test automation header or push button switch (SW1).

MCU domain warm reset (MCU_RESETz) is provided from a push button switch (SW2)

Main domain warm reset (SoC_RESET_REQz) is provided by the Warm Reset signal from the test automation header or a push button switch (SW3).

Upon Power on Reset, all peripheral devices connected to MCU domain get reset by MCU_RESETSTATz.

One User input interrupt is connected to one of the GPIO of SoC.

4.5 Clock

All reference clocks required for the SoC and two Ethernet PHY's are generated from a single three-output clock buffer (LMK1C1103PWR), which is sourced from a single 25 MHz LVCMOS Oscillator. A single output clock buffer (SN74LV1TT34DCKR) is used to level translate from 3.3 V to 1.8 V. An optional clock is provided to RGMII2 Ethernet PHY by the OBSCLK0 output of the SoC by mounting R240 and R185 while isolating R244 and R13.

The reference clock required for XDS110 is generated locally using a 16 MHz crystal.

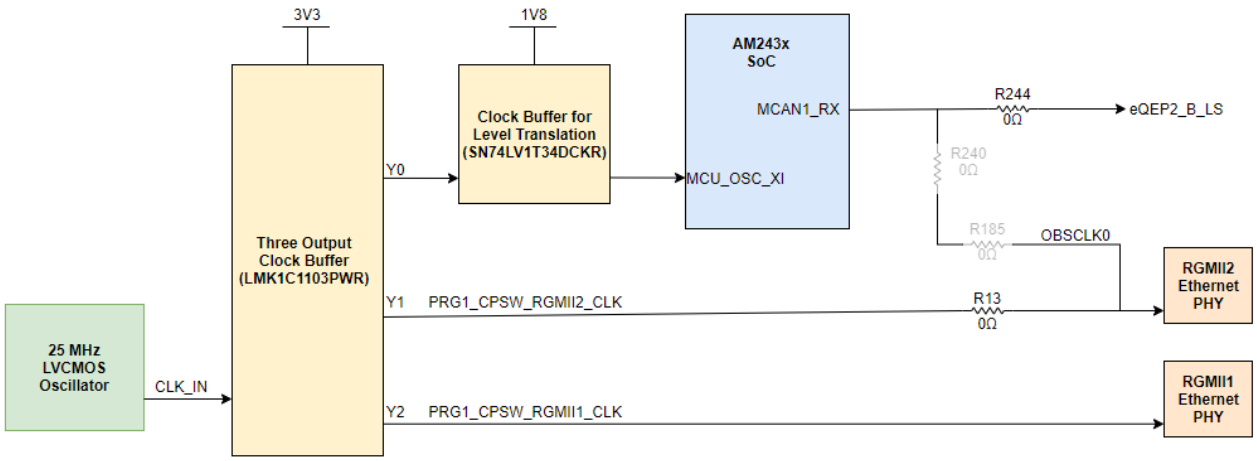

Figure 4-6. Clock Architecture

Table 4-11. Clock Frequency Table

Sl #	Signal Name	Reference	Expected Frequency
1	SOC_CLKIN	U11.4	25.000 MHz
2	SOC_CLKIN_BUFF	R46	25.000 MHz
3	PRG1_CPSW_RGMII1_CLK	R25	25.000 MHz
4	PRG1_CPSW_RGMII2_CLK	R50	25.000 MHz
5	OSC0	Y1.3	16.000 MHz

Note

The 16 MHz clock will only become active after power is supplied to the micro-B USB connector after insertion of a cable into the micro-B USB port.

4.6 Memory Interface

4.6.1 QSPI Interface

The AM243x LaunchPad board has 512 Mbit QSPI memory device (S25HL512TFAMHI010 from Cypress), which is connected to the OSPI0 interface of the AM243x SoC. The QSPI interface supports memory speed up to 166 MHz. External loopback is provided between OSPI0_LBCLKO and OSPI0_DQS.

Reset: The reset for the flash is connected to a circuit that performs an AND operation to MCU_RESETSTATz and a GPIO from the SoC.

Power: The QSPI flash is powered by the 3.3 V IO supply. The 3.3 V supply is provided to both the VCC and VCCQ pins of the flash memory. The OSPI0 interface of the SoC is powered by the VDDSHV_3V3 supply.

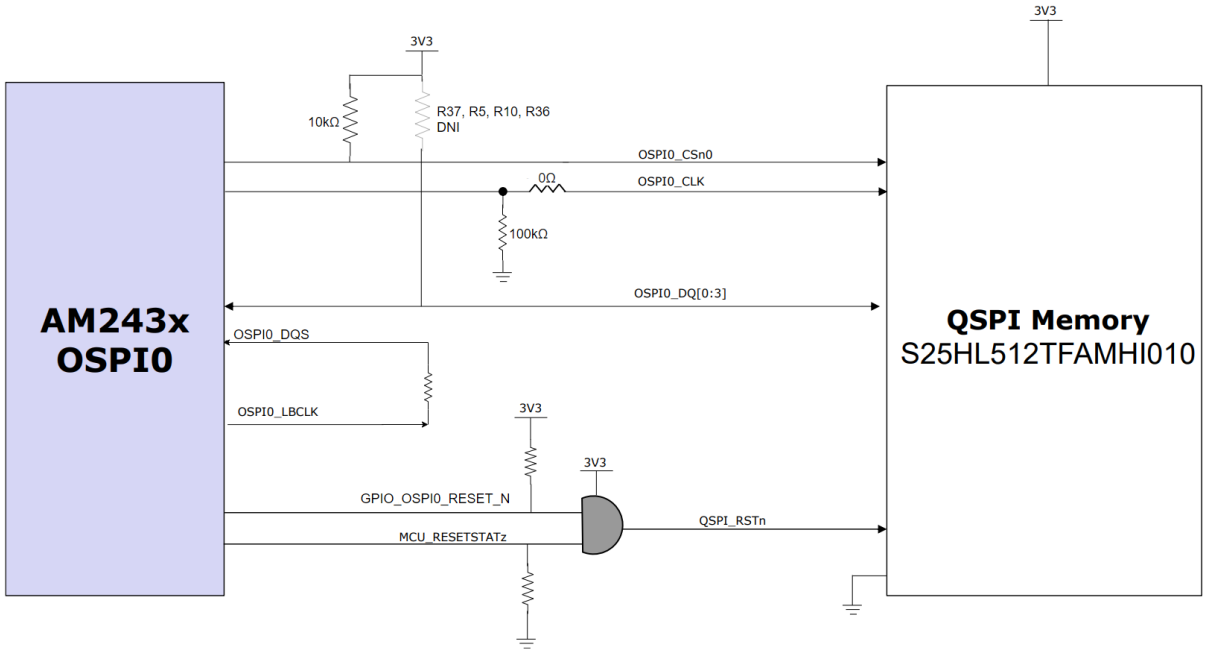

Figure 4-7. QSPI Interface

4.6.2 Board ID EEPROM

The AM243x LaunchPad has a 1 Mbit I2C EEPROM for board ID information. The board ID memory is configured to respond to the I2C address 0X50 by connecting the address pins (A0, A1) to ground and programmed with the header description. This EEPROM (AT24CM01-XHD-T from Microchip) is interfaced to the I2C0 port of the SoC. When the WP pin is connected directly to VCC then all write operations to the protected memory are inhibited. The mounted resistor is shown inside of the red box in Figure 4-8. For normal operation, the WP pin can be left floating by isolating the resistor shown in the red box (R89).

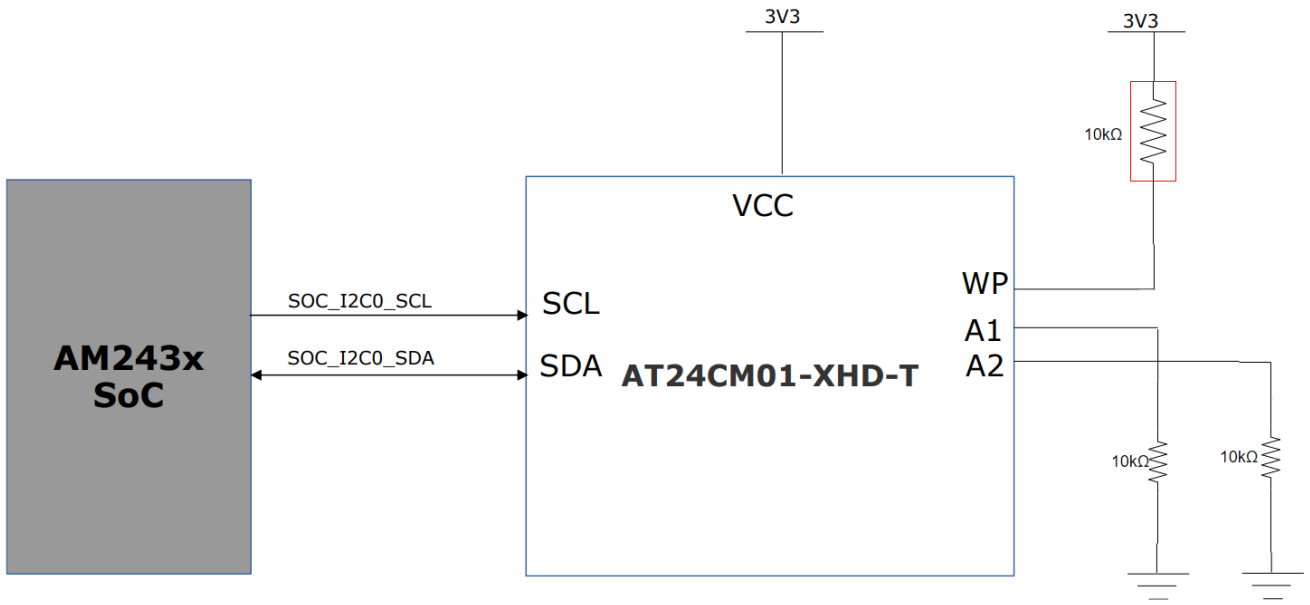

Figure 4-8. Board ID EEPROM

Table 4-12. Board ID Memory Header Information

Header	Field Name	# Bytes	Offset	Field Value	Field Type	Description
EE3355AA	MAGIC	4	0000	0xEE3355AA	HEX	Magic Number
	TYPE	1	0004	0x01	HEX	Fixed length and variable position board ID header
		2	0005	F7	HEX	Size of payload bytes following this field including end_list byte
BRD_INFO	TYPE	1	0007	0x10	HEX	Board Info header identifier
	Length	2	0008	2E	HEX	offset to next header
	Board_Name	16	000A	AM243-LPEVM	CHAR	
	Design_Rev	2	001A	E2	CHAR	
	PROC_Nbr	4	001C	109	CHAR	PROC number from central EVM
	Variant	2	0020	01	CHAR	
	PCB_Rev	2	0022	E2	CHAR	
	SCHBOM_Rev	2	0024	00	CHAR	Used for schematic revision extension - A, B, C etc. Schematic/BoM revision will be Design_Rev+SCHBOM_Rev
	SWR_Rev	2	0026	01	CHAR	1 is first software release
	VendorID	2	0028	01	CHAR	1 is Mistral
	Build_Week	2	002A	20	CHAR	Filled in by Mistral
	Build_Year	2	002C	21	CHAR	2021

Table 4-12. Board ID Memory Header Information (continued)

Header	Field Name	# Bytes	Offset	Field Value	Field Type	Description
	BoardID	6	002E	0	CHAR	Legacy apps part number. Not used for recent boards. Will be marked as 0
	Serial_Nbr	4	0034	xxxx	CHAR	Filled in by Mistral
MAC_ADDR	TYPE	1	0038	0x13	HEX	MAC address header identifier
	LENGTH	2	0039	0xC2	HEX	Size of payload
	MAC control	2	003B	0x10	HEX	MAC header control word
	MAC_adrs	192	003D	xxxx	HEX	Will have three valid MAC addresses
END_LIST	TYPE	1	00FD	0xFE	HEX	End Marker

4.7 Ethernet Interface

The LaunchPad supports two Ethernet PHYs that are terminated to RJ45 connectors with integrated magnetics for external communication.

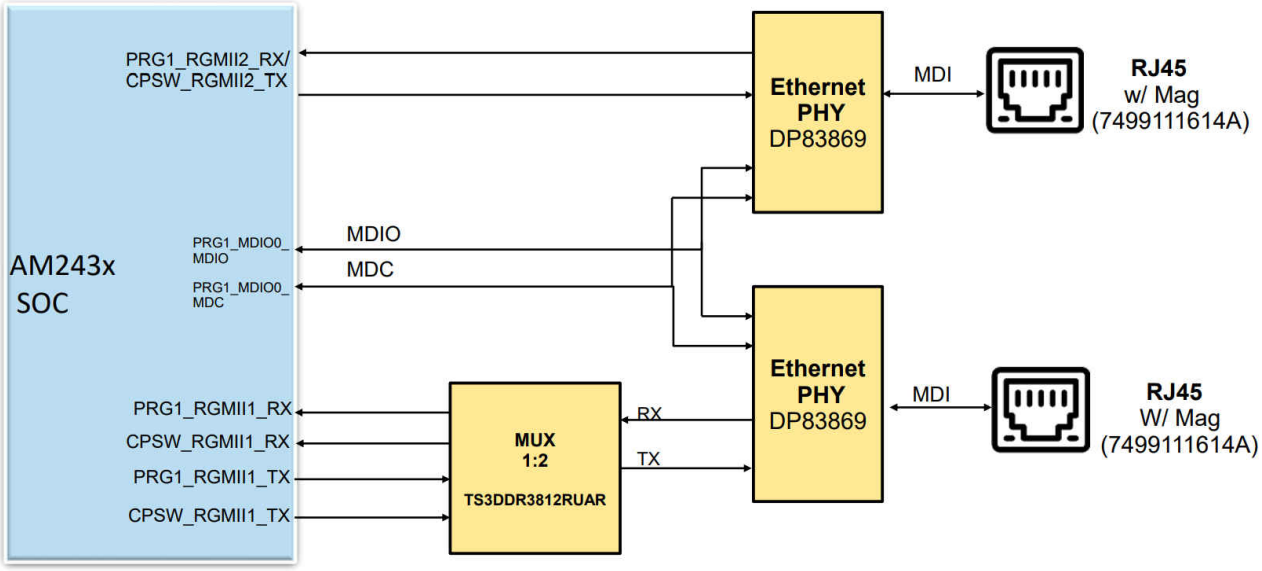

Figure 4-9. Ethernet Connection

The 48 pin PHY (DP83869) is configured to advertise gigabit operation with the internal delay set to accommodate the internal delay of the AM243x SoC.

The first PHY is interfaced to the PRG1/CPSW RGMII2 ports of the SoC that are internally multiplexed in the SoC and the MDI interface from the same PHY is terminated to a RJ45 connector with integrated magnetics.

The second PHY is interfaced to the PRG1/CPSW RGMII1 ports of the SoC that are multiplexed using an external on-board MUX whose select line is be controlled from a GPIO (PRG_CPSW_RGMII1_MUX_SEL) of the SoC and the MDI interface from the same PHY is terminated to a RJ45 connector with integrated magnetics. A 1:2 mux (TS3DDR3812RUAR) is used to select between the PRG1 and CPSW RGMII1 ports.

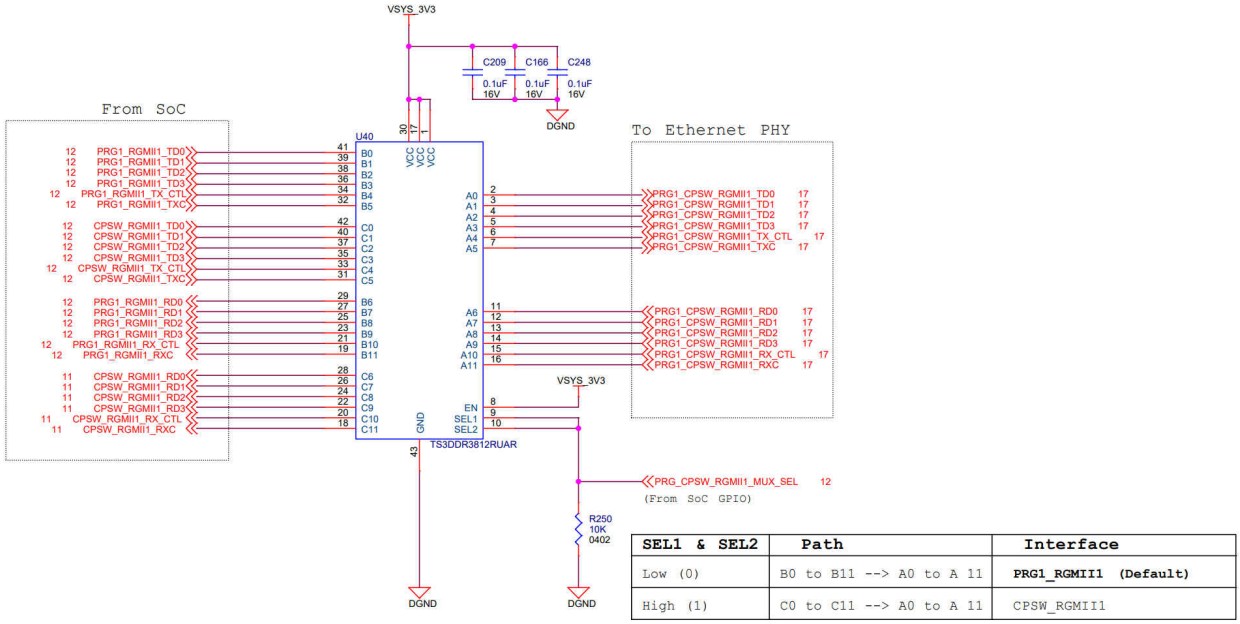

Figure 4-10. CPSW or PRG RGMII1 Ethernet Data Mux

To select between the PRG and CPSW operation for both PHYs, the MDIO and MDC signals, which are internally multiplexed in the SoC, must be selected from each controller.

Two RJ45 connectors with integrated magnetics and status LEDs (7499111614A from Wurth) are used on the board for Ethernet 10Mb/100Mb/1Gb connectivity.

4.7.1 Ethernet PHY Strapping

The DP83869 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. RX_D0 and RX_D1 pins are 4-level strap pins and all other strap pins have two levels.

The Ethernet PHY includes an internal pull-down resistor. The value for the external pull resistors are selected to provide voltage at the pins of the AM243x as close to ground or 3.3 V as possible.

Address strapping is provided for the RGMII1 PHY and RGMII2 PHY to set the address to 00011 (03h) and 0111 (0Fh), respectively, using strap resistors. Footprint for both pull up and pull down is provided on all the strapping pins.

Both PHY modes are selected as RGMII to copper with auto-negotiation advertised for 1000 Base-T, 100 Base-Tx, and 10 Base-Te speeds.

The strapping configurations for both Ethernet PHYs are shown in Figure 4-11 and Figure 4-12.

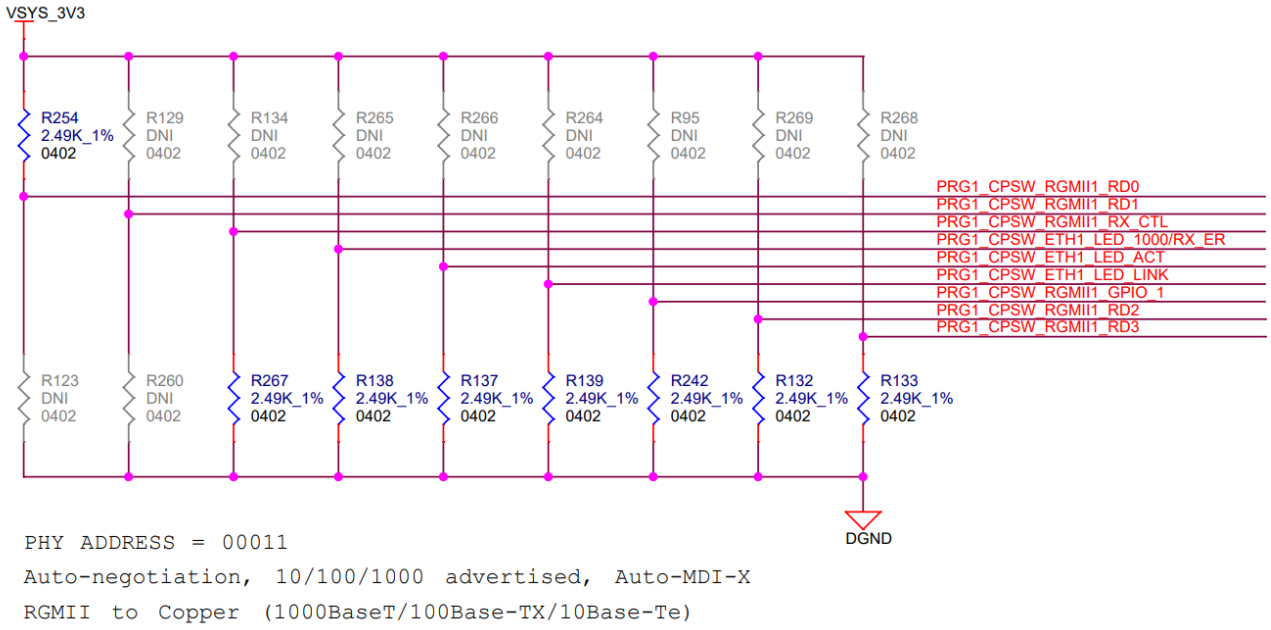

Figure 4-11. Ethernet PHY Strapping for RGMII1 PHY

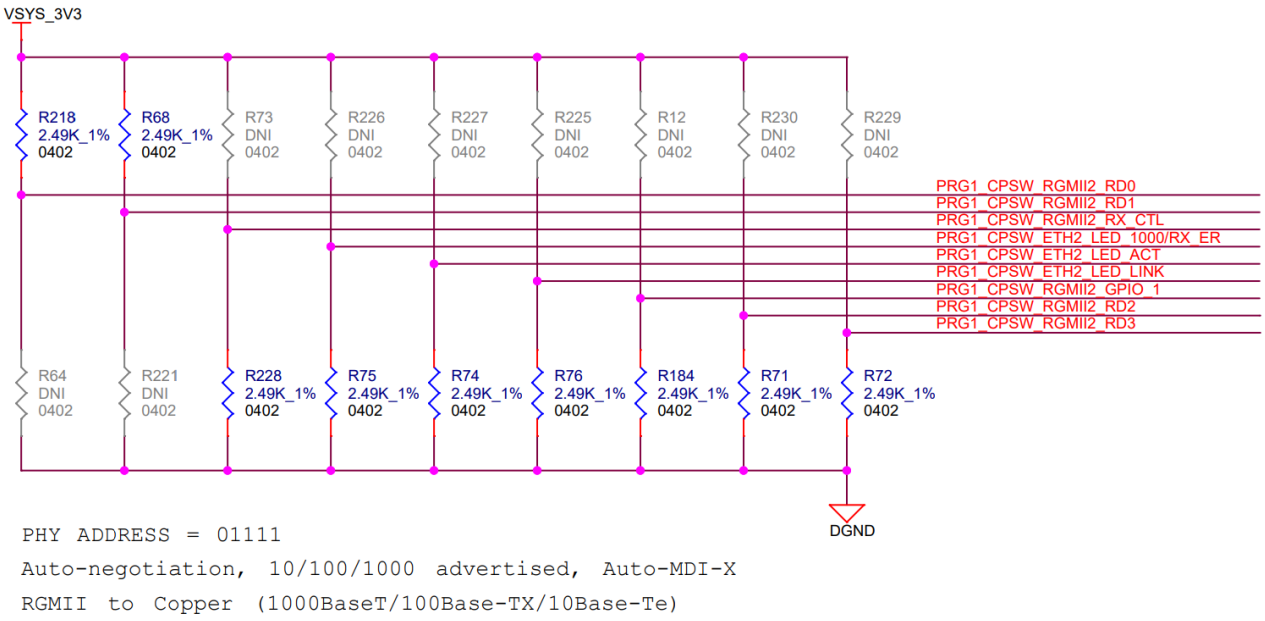

Figure 4-12. Ethernet PHY Strapping for RGMII2 PHY

Table 4-13 shows the strapping description for both Ethernet PHYs.

Table 4-13. Ethernet PHY Strapping Values

Strap Setting	Pin Name	Strap Function	Value of Strap Function for RGMII1	Value of Strap Function for RGMII2	Description
PHY Address	RX_D1	PHY_AD3	1	1	ICSSG1 PHY Address 00011
		PHY_AD2	1	1	
	RX_D0	PHY_AD1	0	1	ICSSG2PHY Address: 01111
		PHY_AD0	0	0	
Modes of Operation	RX_CNTL	Mirror Enable	0	0	Mirror Enabled/Disabled
	LED_2	ANEGSEL_1	0	0	Auto-negotiation, 10/100/1000 advertissed, Auto-MDI-X
	LED_1	ANEGSEL_0	0	0	
	LED_0	ANEG_DIS	0	0	
	JTAG_TDO/GPIO_1	OPMODE_0	0	0	RGMII to Copper (1000 Base-T, 100 Base-Tx, 10 Base-Te)
	RX_D2	OPMODE_1	0	0	
	RX_D3	OPMODE_2	0	0	

4.7.2 Ethernet PHY - Power, Clock, Reset, Interrupt

Power: Since the RGMII signals from the PRG1 and CPSW domain of the SoC are at 3.3 V I/O level, the Gigabit Ethernet PHY device (DP83869) is powered with I/O voltage of 3.3 V and an analog supply of 2.5 V and 1.1 V.

Clock: The 25 MHz clock is sourced from the output of the clock buffer to both Ethernet PHYs. Alternatively, RGMII2 PHY can be sourced by the OBSCLK0 output of the SoC as shown in the Clock Architecture.

Reset: The reset signal for the PHYs is driven by an AND operation between PORz_OUT and an SoC GPIO.

Interrupt: The interrupts from the two Ethernet PHYs are shorted and connect to a single GPIO of the AM243x SoC.

4.7.3 LED indication in Ethernet RJ45 Connector

RJ45 Connector (J19) LED indication for PRG1/CPSW RGMII1 port:

- LED0 is connected to RJ45 LED (yellow) to indicate link up.
- LED1 is connected to RJ45 LED (orange) to indicated 1000 MHz link or receive error.
- LED2 is connected to RJ45 LED (green) to indicate transmit/receive activity.

RJ45 Connector (J18) LED indication for PRG1/CPSW RGMII2 port:

- LED0 is connected to RJ45 LED (yellow) to indicate link up.
- LED1 is connected to RJ45 LED (orange) to indicated 1000 MHz link or receive error.
- LED2 is connected to RJ45 LED (green) to indicate transmit/receive activity.

4.8 USB 2.0 Interface

On the LaunchPad, a USB 2.0 interface is offered through a USB Type-C connector (J10). the USB DP and DM signals connect the USB0 port of the SoC through an ESD protection diode. The DP and DM sinals are shorted to the A and B option for DP and DM on the connector side in order to support the flip action in the cable.

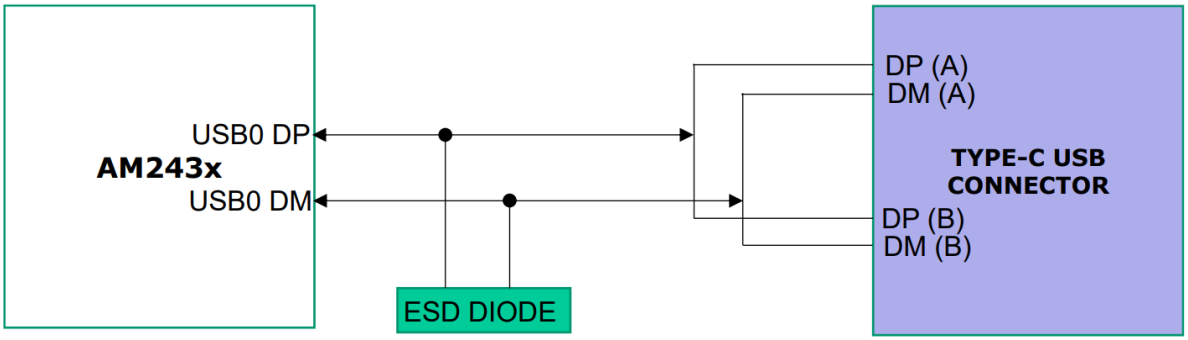

Figure 4-13. USB 2.0 Interface

4.9 I2C Interface

The AM243x SoC supports two I2C interfaces that are used to connect BoosterPack headers, test automation header, LED driver for ethernet LEDs, and Board ID EEPROM to the LaunchPad.

- **SoC_I2C0 Interface:** SoC_I2C0 is connected to each of the following:
  - I2C0 interface is used by the software to identify the LaunchPad through the Board ID memory device (AT24CM01-XHD-T) which is configured to respond to the address 0x50.
  - I2C0 on the LaunchPad is also used to control the 8 bit LED driver (TPIC2810) configured to respond to address 0x60 which is used to conrol the Industrial LEDs.
  - I2C0 is also connected to the BoosterPack (J5.9, J5.10) expansion connector.
- **SoC_I2C1 Interface:** SoC_I2C1 is connected to each of the following:
  - Test automation header (687140183622 from Wurth)
  - I2C1 is also connected to the BoosterPack (J1.9, J1.10) expansion connector

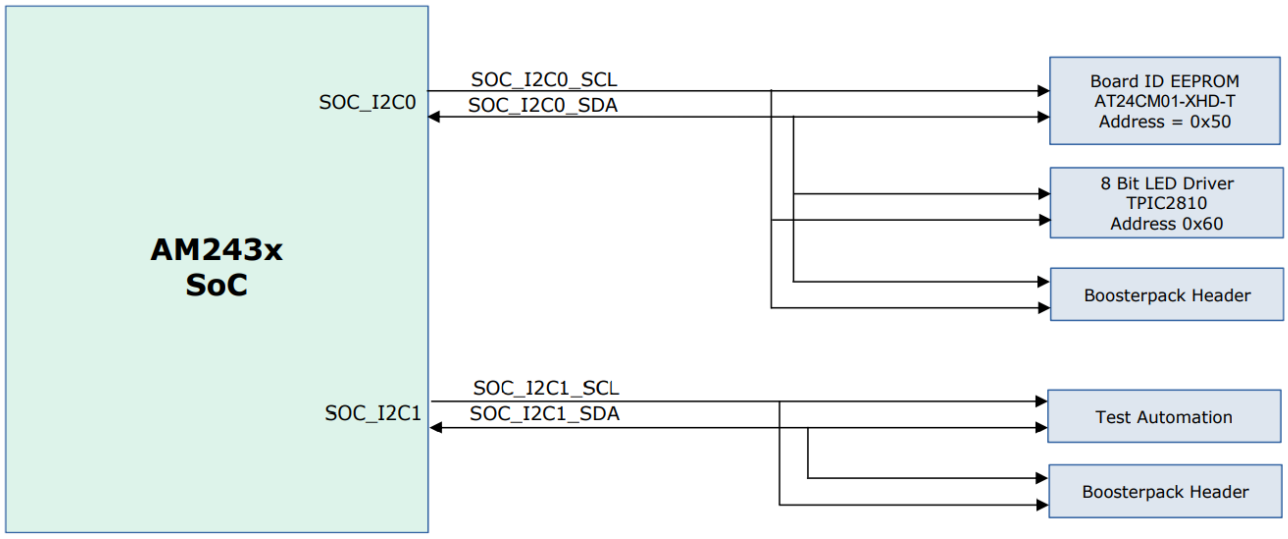

Figure 4-14. I2C Interface

4.10 Industrial Application LEDs

The Industrial application LEDs consist of five green, one red, and two bi-color LEDs.

- Four green LEDs are connected to the I2C-based LED driver (TPIC2810D) at the address 0x60 that is controlled by the SoC at the SoC_I2C0 port. These LEDs are to be toggled based on the Industrial application.
- The other green LED, as well as the red and two bi-color LEDs, are connected to SoC GPIO's such that they can be toggled based on the application.

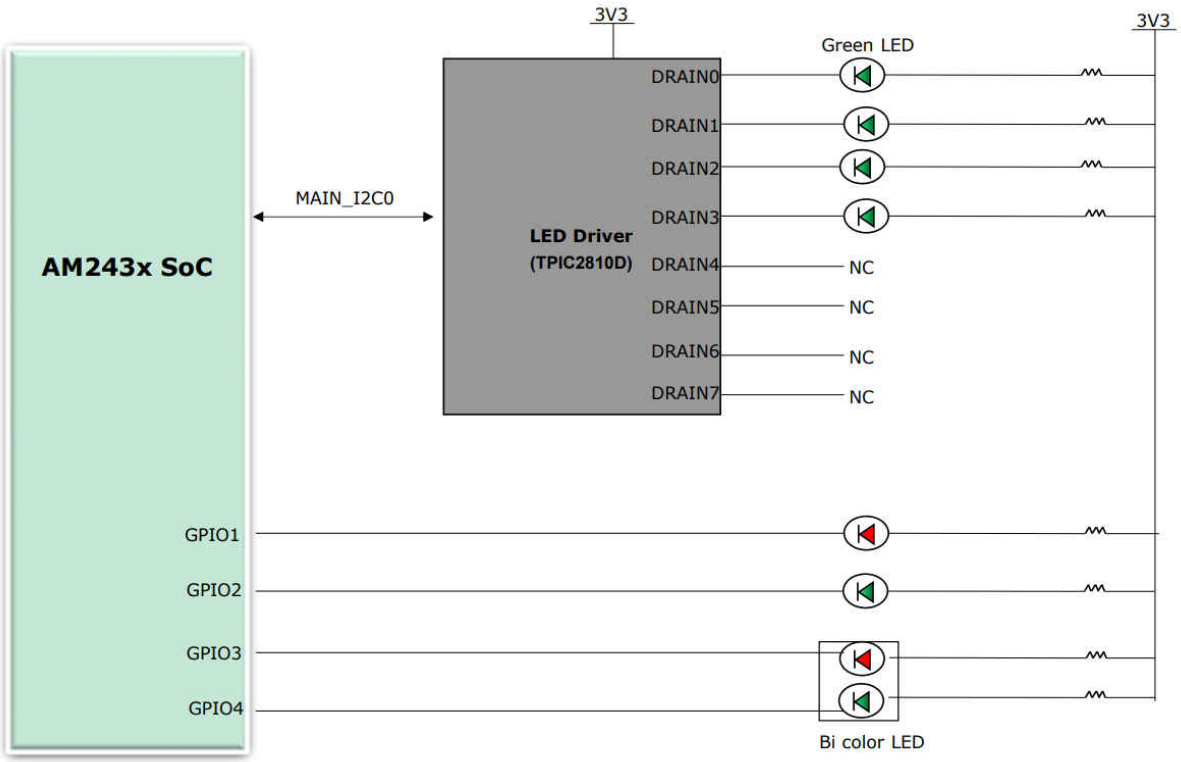

Figure 4-15. Industrial Application LEDs

4.11 UART Interface

The LaunchPad consists of five UART interfaces where four of the interfaces come from the main domain of the SoC and one comes from the MCU domain.

- Two UART ports from the main domain of the SoC (Main_UART2 and Main_UART4) are terminated on the BoosterPack expansion connectors.
- Two UART, one from the MCU domain (MCU_UART0) and one from the main domain of the SoC (MAIN_UART1) are terminated on two on-board 1x6 headers. There is a buffer (SN74CB3Q3125PWR) used to isolate between the connectors and the SoC.
- One UART port from the main domain of the SoC (Main_UART0) is connected to a buffer (SN74AVC4T245PW) isolated between the SoC and the on-board emulator XDS110 (TM4C1294NCPDTT3R)

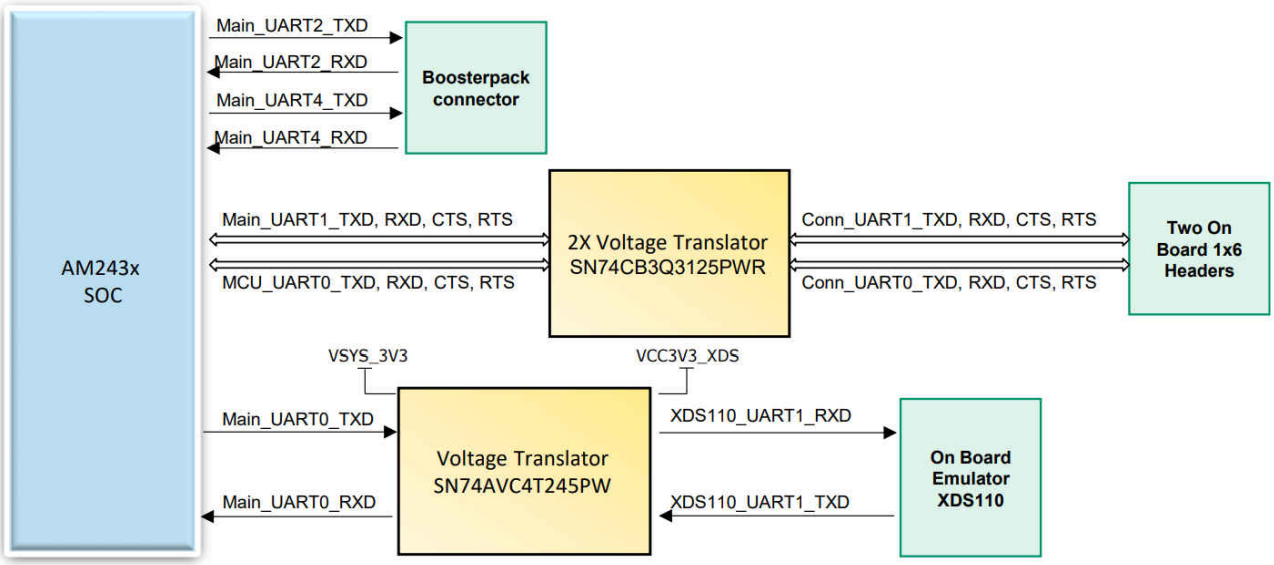

Figure 4-16. UART Interface

4.12 eQEP Interface

The AM243x LaunchPad supports two eQEP interfaces. eQEP1 and eQEP2 of the AM243x SoC are connected to the eQEP headers. Both eQEP1 and eQEP2 headers need a voltage translation circuit (TXB0106RGYR) to level shift the IO's to 5 V from 3.3 V.

- eQEP1_A, eQEP1_B, and eQEP1_I are directly connected to the eQEP header (J12) after voltage translation .
- eQEP2_A, eQEP2_B are directly connected to the eQEP header (J21) after voltage translation. eQEP2_I requires an external 1:2 mux (TMUX154EDGSR) since eQEP2_I and MCAN0_TX come from the same pin (B13). Mux channel selection is done using SoC GPIO.

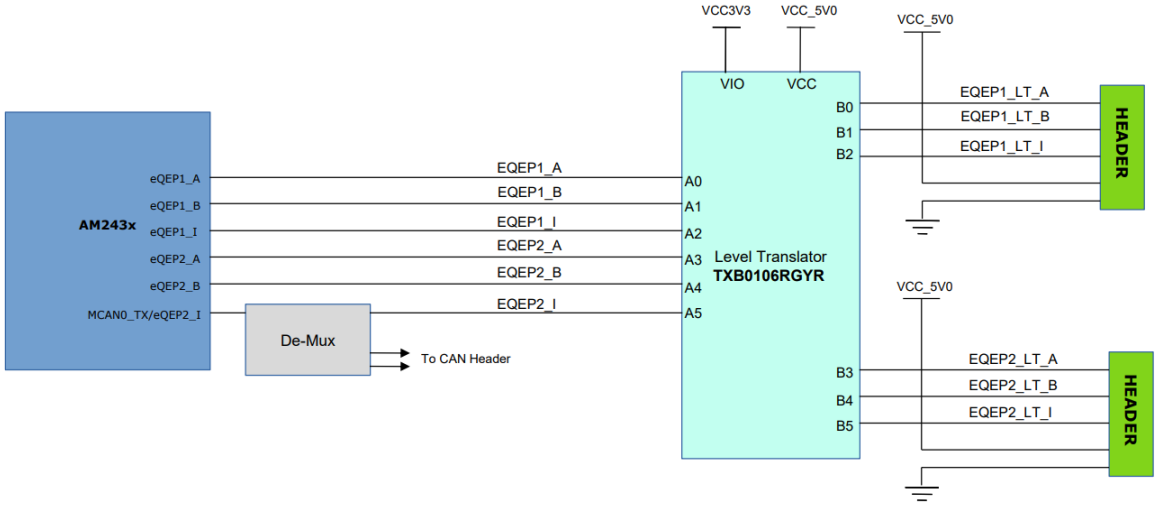

Figure 4-17. eQEP Interface

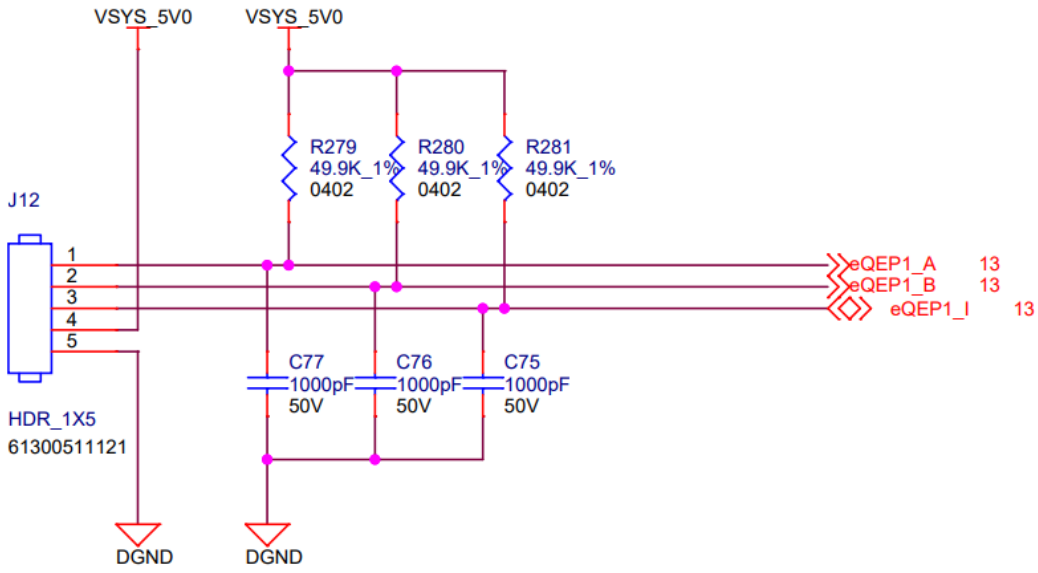

Figure 4-18. eQEP1 Header

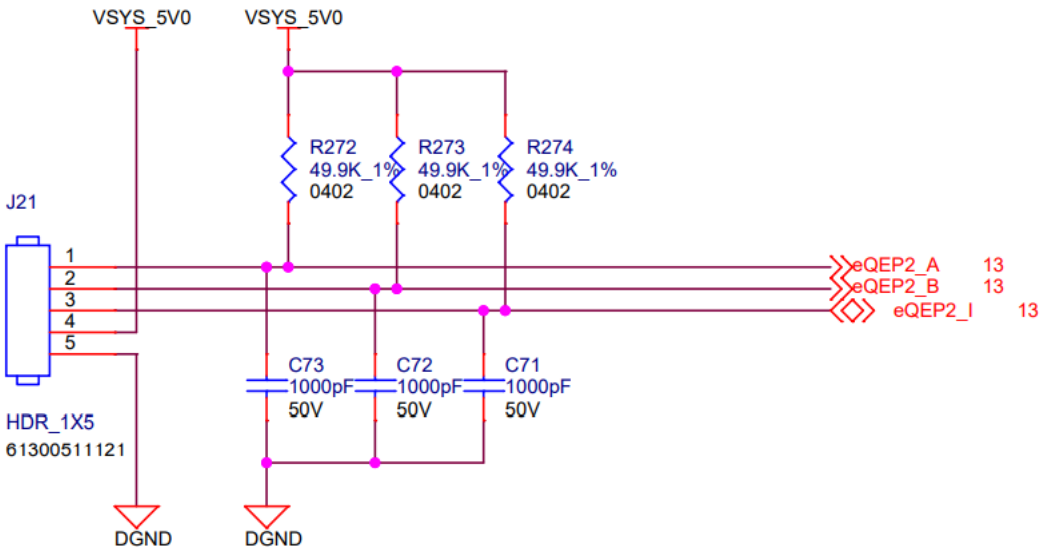

Figure 4-19. eQEP2 Header

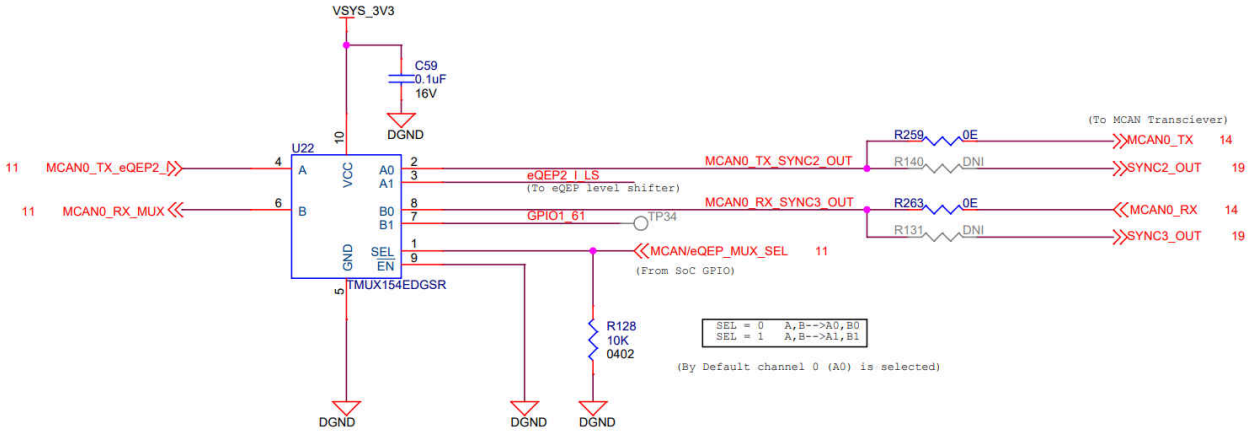

Figure 4-20. eQEP2 or MCAN0 Mux Selection Circuit

4.13 CAN Interface

The AM243x LaunchPad supports one CAN interface. MCAN0 signals are multiplexed with eQEP signals internally. These signals are connected to an on-board demultiplexer, whose select line is controlled by a GPIO from the SoC, to route the signal to either the MCAN transceiver or the eQEP header. Figure 4-21 depicts the implementation of the CAN interface using a CAN interface IC (TCAN1044VDRBRQ1). The TXD and RXD pins of the CAN interface IC are connected to the MCAN0_RX and MCAN0_TX pins of the AM243x, respectively. The STB pin can be directly driven by the AM243x to enable standby mode. When not directly driven by the AM243x, the 10kΩ pulldown resistor puts the CAN interface IC into normal operation mode. The output of signals for the CAN transceiver's high and low are connected to the 3-pin header (J11).

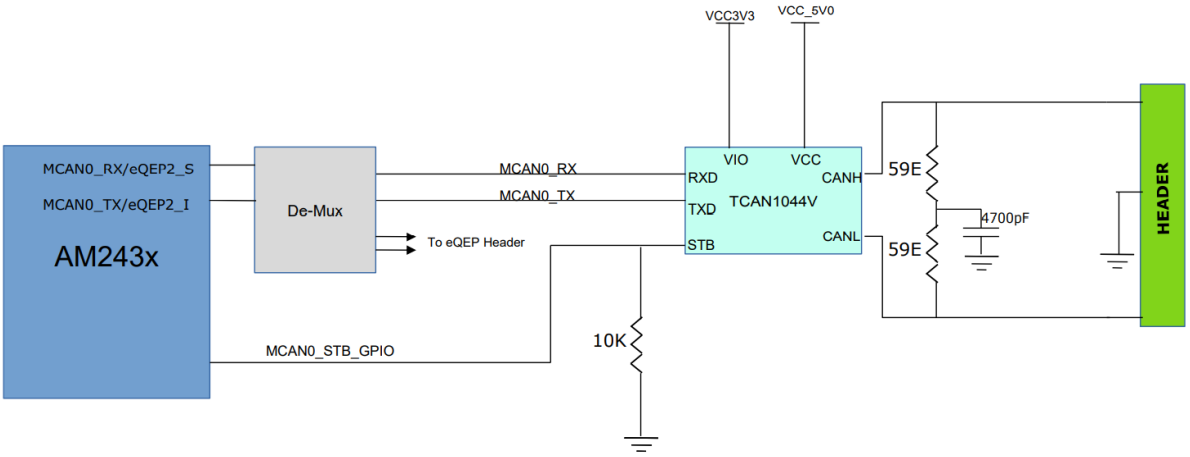

Figure 4-21. CAN Interface

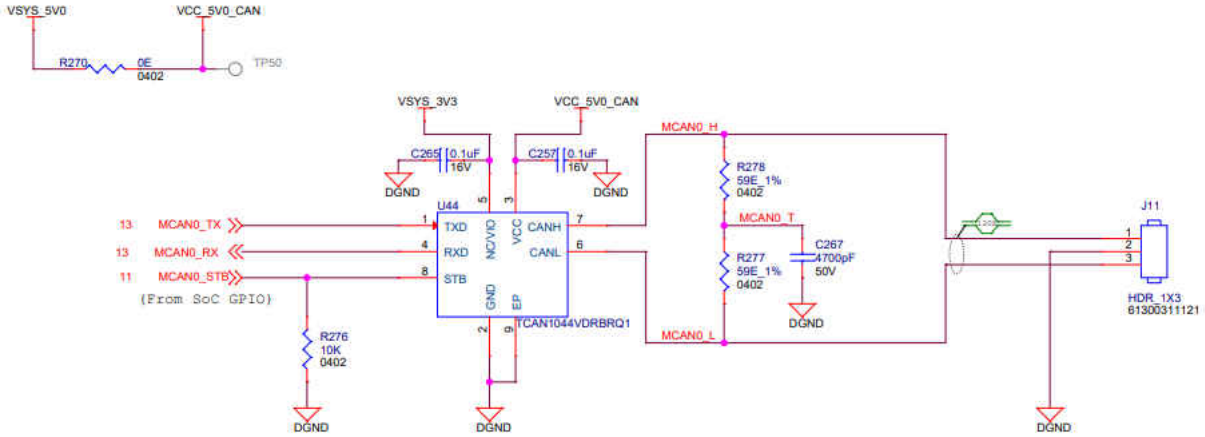

Figure 4-22. MCAN Transceiver and Header

4.14 FSI Interface

The LaunchPad supports one FSI Interface from the SoC that terminatets to a 2x5 header (J16). The 2x5 header has a 3.3 V supply. A 1:2 active mux IC (TMUX154EDGSR) is used to interface the signals between the FSI header and the BoosterPack header as both the FSI and EHRPWM signals are internally muxed inside the SoC.

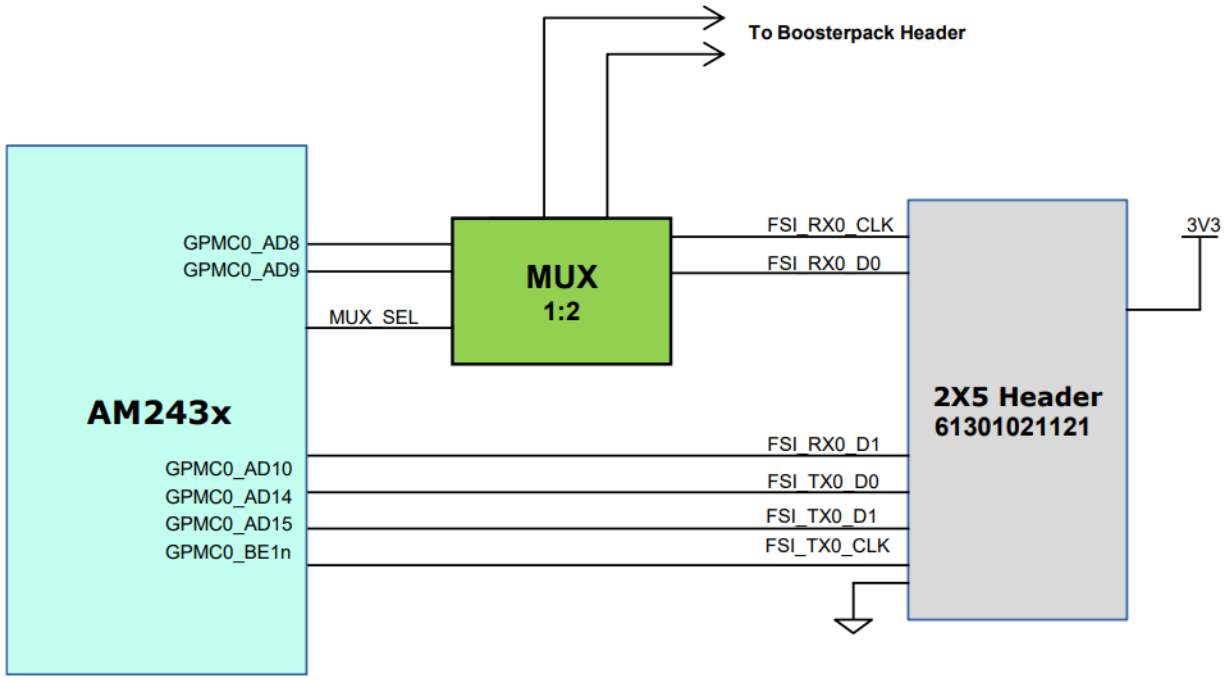

Figure 4-23. FSI Interface

Table 4-14. FSI Header Pin Description

Pin Number	Signal
J16.1	FSI_RX0_CLK
J16.2	FSI_TX0_CLK
J16.3	GND
J16.4	GND
J16.5	FSI_RX0_D0
J16.6	FSI_TX0_D0
J16.7	FSI_RX0_D1
J16.8	FSI_TX0_D1
J16.9	No connection
J16.10	VSYS_3V3

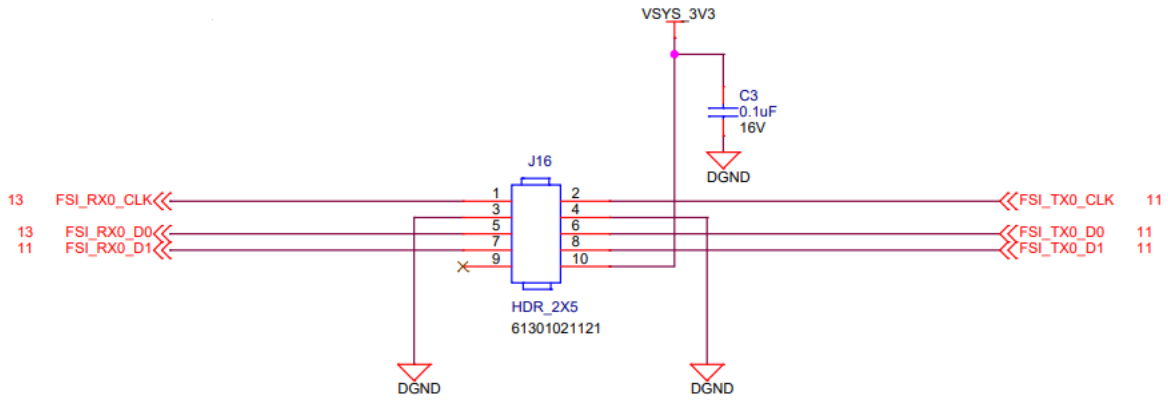

Figure 4-24. FSI Header

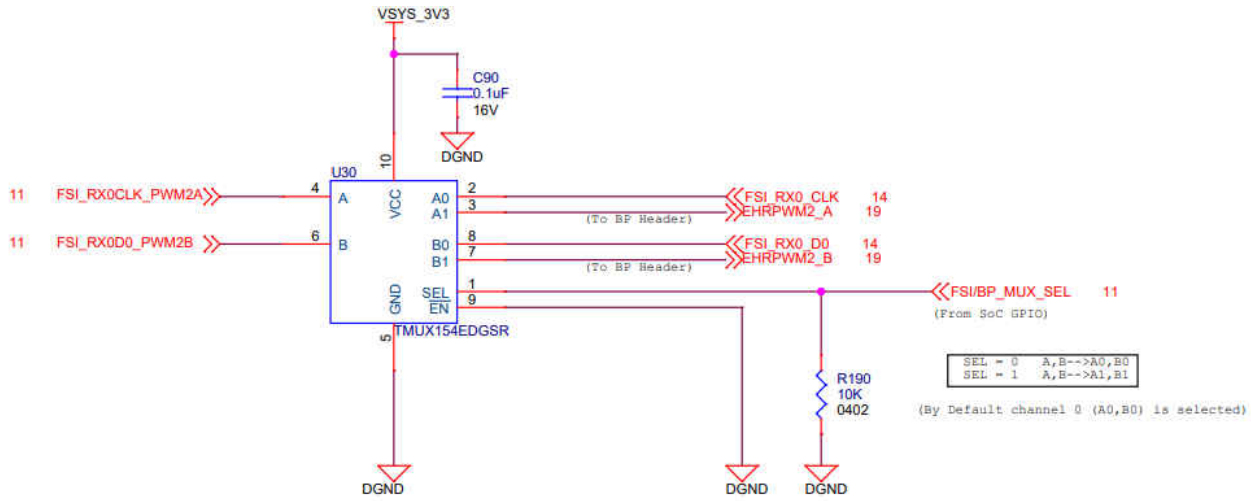

Figure 4-25. FSI or BoosterPack Mux Selection Circuit

4.15 JTAG Emulation

The following sequence should be followed for proper functioning of JTAG:

1. Power the board by connecting the Type-C USB connector with 5 V at 3A.
2. Connect the micro-B USB cable for JTAG emulation into J20 once after powering the board (Hot Plug).

The AM243x LaunchPad includes the necessary circuitry for XDS110 emulation. The XDS110 class on-board emulation is used to support testing of software builds. The connection for the emulator uses a USB 2.0 micro-B connection (J20) and the circuit acts as a powered USB peripheral device. The VBUS power from the connector is used to power the emulation circuit such that the connection to the emulator is not lost when power to the LaunchPad is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the LaunchPad.

An ESD protection diode (TPDE02B04DQAR) is provided on the USB signals to steer ESD current pulses to VCC or GND. The ESD protection diode protects against ESD pulses up to ±2.5 kV Human-Body Model (HBM) as specified in ANSI/ESDA/JEDEC JS-001 and provides ±12 kV contact discharge as well as ±15 kV air-gap discharge as specified in IEC 61000-4-2.

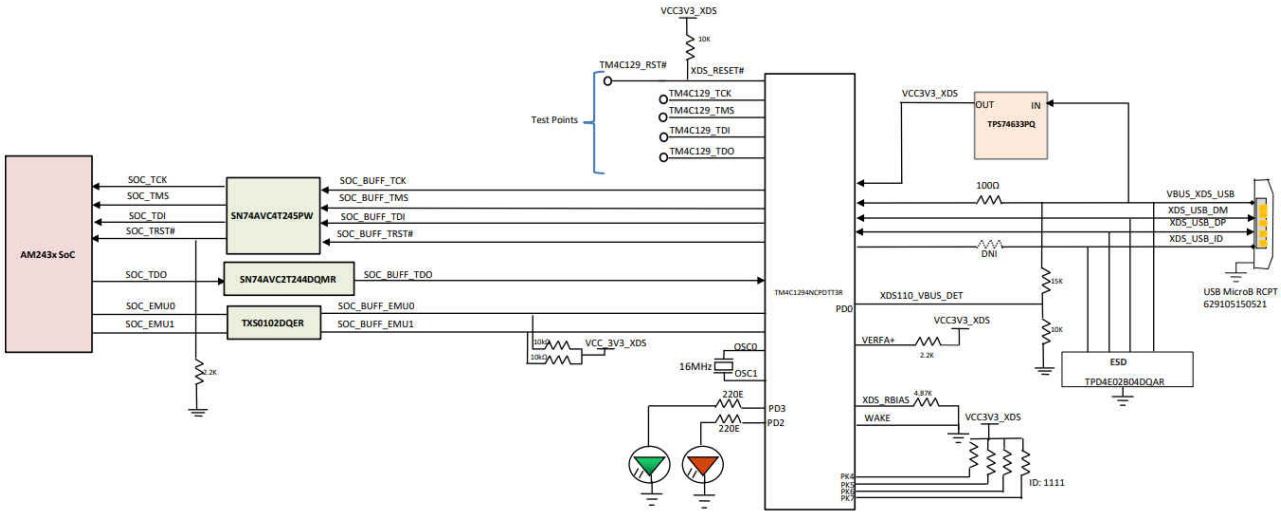

Figure 4-26. JTAG Interface

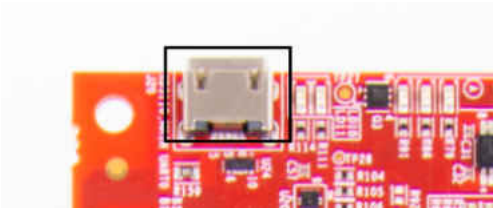

Figure 4-27. Micro-B USB Connection for JTAG

4.16 Test Automation Interface

The LaunchPad supports a 40-pin test automation header (687140183622 from Wurth) that allows an external controller to manipulate some basic operations like power down, power on reset (POR), warm reset, boot mode control and other functions.

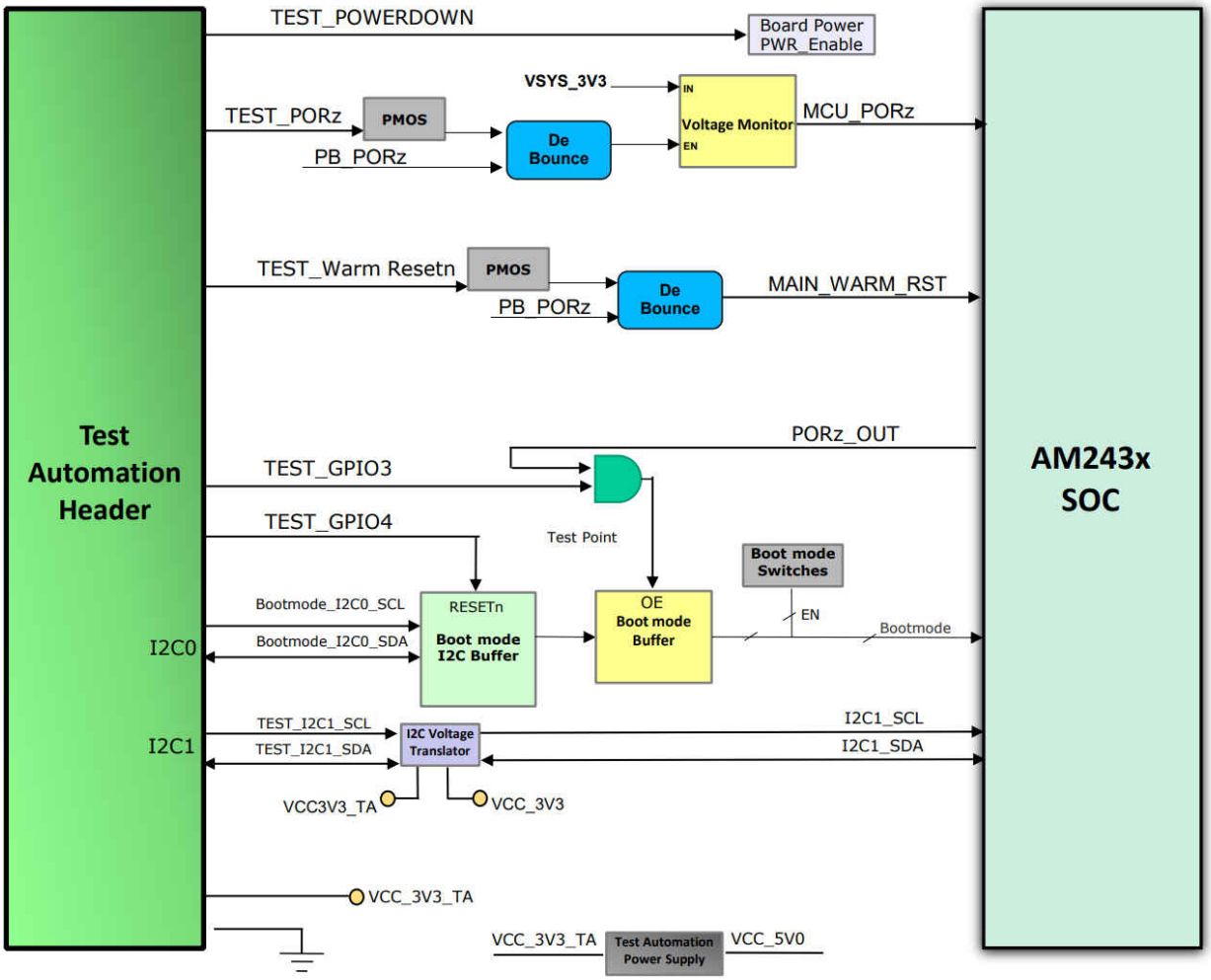

Figure 4-28. Test Automation Header

Table 4-15. Test Automation Signal Description

Signal	Signal Type	Function
POWER_DOWN	GPIO	Instructs the LaunchPad to power down all circuits
PORZn	GPIO	Creates a PORz into the AM243x
WARM_RESETn	GPIO	Creates a RESETz into the AM243x
GPIO3	GPIO	Disables the boot mode buffer
GPIO4	GPIO	Resets the bootmode IO expander
Bootmode_I2C	I2C	communicates with bootmode I2C buffer
I2C1	I2C	For internal testing

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM243x. Boot mode for the AM243x can be controlled by either the DIP switch or the test automation header through the I2C IO expander.

A boot mode buffer (SN74AVC8T245RHL) is used to isolate the boot mode controls that are driven through either the DIP switch or the I2C IO expander. The test automation circuit is powered by an always on supply that is generated from a dedicated regulator (TPS7A0533PDBVT).

The test automation header supports two I2C interfaces. Bootmode_I2C connects to the boot mode buffer to control the bootmode of the AM243x while the other I2C interface is connected to the I2C1 port of the AM243x.

Table 4-16. Test Automation Header Pinout

Pin #	IO Direction	Signal	Description
1	Power	VCC3V3_TA	Power for test automation header
2	Power	VCC3V3_TA	
3	Power	VCC3V3_TA	
4	N/A	Reserved	
5	N/A	Reserved	
6	N/A	Reserved	
7	Ground	DGND	
8	N/A	Reserved	
9	N/A	Reserved	
10	N/A	Reserved	
11	N/A	Reserved	
12	N/A	Reserved	
13	N/A	Reserved	
14	N/A	Reserved	
15	N/A	Reserved	
16	Ground	DGND	
17	N/A	Reserved	
18	N/A	Reserved	
19	N/A	Reserved	
20	N/A	Reserved	
21	N/A	Reserved	
22	N/A	Reserved	
23	N/A	Reserved	
24	N/A	Reserved	
25	Ground	DGND	
26	Output	TEST_POWERDOWN	Used to power down the board
27	Output	TEST_PORZn	Used to reset the SoC PORz
28	Output	TEST_WARMRESETn	Used to reset the SoC Warm Reset
29	N/A	Reserved	
30	Output	TA_SOC_INTn	Interrupt to SoC
31	Bidirectional	TEST_GPIO2	
32	Output	TEST_GPIO3	Used to disable the BOOTMODE buffer
33	Outpu	TEST_GPIO4	Used to Reset the BOOTMODE IO Expander
34	Ground	DGND	
35	N/A	Reserved	
36	Bidirectional	SOC_I2C1_TA_SCL	Clock signal for SoC I2C
37	Bidirectional	BOOTMODE_I2C_SCL	Clock signal for I2C IO expander for boot mode
38	Bidirectional	SOC_I2C1_TA_SDA	Data signal for SoC I2C
39	Bidirectional	BOOTMODE_I2C_SDA	Data signal for I2C IO expander for boot mode
40	Ground	DGND	
41	Ground	DGND	

Table 4-16. Test Automation Header Pinout (continued)

Pin #	IO Direction	Signal	Description
42	Ground	DGND	

Note

All pins designated as "Reserved" should be left unconnected/floating.

4.17 SPI Interface

The LaunchPad supports two SPI interfaces (SPI0 and SPI3) that are terminated to BoosterPack header connectors. The SPI connections between the SoC and the BoosterPack connectors are show in Figure 4-29.

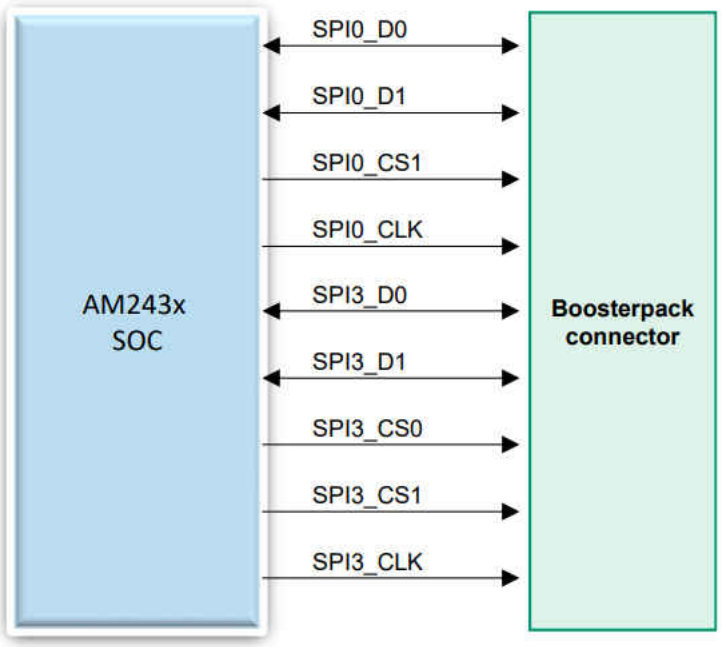

Figure 4-29. SPI Connection From SoC to BoosterPack Connector

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM2434 Sitara™ Microcontrollers*
- *AM243x Sitara™ Microcontrollers Data Sheet*
- *AM243x Sitara™ Microcontrollers Technical Reference Manual*
- *AM243x Sitara™ Microcontrollers Silicon Errata*
- *AM243x Sitara™ LaunchPad™ MCU Pinout Map*
- *AM243x Sitara™ LaunchPad™ Out-of-Box Experience*
- *Texas Instruments Code Composer Studio*
- *Texas Instruments LaunchPad Development Environment*

5.2 Other TI Components Used in This Design

This LaunchPad uses various other TI components for its functions. A consolidated list of these components with links to their TI product pages is shown below.

- *TXB0106RGYR 6-bit Bidirectional Voltage-Level Translator*
- *TMUX154E 2-Channel, 2:1 Switch*
- *TPD4E02B04DQAR ESD Protection Diode for USB 3.0*
- *XDS110 JTAG Debug Probe*
- *TUSB320LAI USB Type-C Configuration Channel Port Controller*
- *LMK1C1103PWR 3-Channel Output LVCMOS 1.8V Buffer*
- *TS3DDR3812RUAR 12-Channel Switch for DDR3 Applications*
- *TCAN1044-Q1 Automotive High-Speed CAN Tranceiver*
- *TPIC2810D 8-bit LED Driver with I2C Interface*
- *DP83869HM Gigabit Ethernet PHY Transceiver*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2021) to Revision A (September 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3
• Updates were made in Section 1.2	3
• Altered description of BoosterPack to not include recommendation of sourcing power to LP from BoosterPack	14

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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