Application Report

AM64x/AM243x Schematic Checklist

ABSTRACT

This application report highlights board design recommendations when using the AM64x and AM243x families of devices. The recommendations are intended to supplement the information provided in the device-specific technical reference manual and data sheet. It is not an all-encompassing list, but rather a succinct reference for board designers that highlights certain caveats and care-abouts related to different use cases. Links for additional AM64x and AM243x product pages and reference documents will be added as they become available.

Table of Contents

Trademarks

1 Introduction

This article applies to the following devices:

- AM6442
- AM6441
- AM6421
- AM6412
- AM6411
- AM2434
- AM2432
- AM2431

Links to TI hardware designs based on AM64x:

- AM64x General Purpose EVM
- AM243x General Purpose EVM
- AM64x/AM243x Silicon Errata

Check the relevant Sitara Processors Silicon Errata document when designing a board. This document contains important information on silicon issues that affect your board design.

Other useful links:

- High-Speed Interface Layout Guidelines
- AM64x/AM243x PCB Escape Routing Guidelines
- TI System Configuration Tool

2 Recommendations for AM64x and AM243x

2.1 EVM versus Data Sheet

In case of any discrepancy between the TI EVMs and the device data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification. Thus, the EVM designs should not be considered as reference designs to be blindly reused.

2.2 Power

- **Have you used the output of the power model and estimates from the rest of your design to determine the power solution needed?**

  The power needed for each rail of the SoC will vary based on the interfaces used and the environment in which it is operating. Power requirements must be determined using the power model.
- **Have you confirmed your system design will apply the correct power supply voltages to each power pin?**

  The SoC includes a number of power rails which must be powered with the correct voltage for proper operation.
- **Have you confirmed the I/O supply of all attached devices and their respective signals are operating from the same I/O power supply as their respective AM64x I/Os?**

  The AM64x and AM243x SoCs includes six dual-voltage I/O power domains, where each provides power to a fixed set of I/Os. Each I/O power domain can be configured to operate at 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of I/Os powered by the respective I/O power domain. All signals connected to I/Os associated with a I/O power domain must operate from the same power source that is being used to power the respective VDDSHVx supply rail. The AM64x I/O buffers are not failsafe. The VDDSHVx I/O supply must be present before any voltage is applied to associated I/Os.
- **Do you have the proper de-coupling capacitor connected to the output of each internal LDOs?**

  The SoC includes eight internal LDOs with the output of each connected to a pin on the device. The LDOs require an output de-coupling capacitor connected between each of these pins. Each CAP_VDDS_x pin requires a 1 µF capacitor and CAP_VDDSHV_MMC1 requires a 3.3 µF capacitor. Low inductance capacitors and low loop inductance connectivity is required for these capacitors.

- **Does your design meet the power sequencing requirement defined in the data sheet?**

  Proper power supply sequencing in proper correlation with resets and clocks is required. For the recommended power sequencing requirements, see the device-specific data sheet.
- **Are the filters specified in the Technical Reference Manual included for the VDDA_x supply pins?**

  AM64x and AM243x devices contain multiple analog power pins that provide power to sensitive analog circuitry such as PLLs, DLLs, and SERDES. These must be attached to low-noise or filtered power sources.
- **Does your design include the correct termination for your selected DDR interface type?**

  Ensure that you have implemented all recommendations found in *AM64x/AM243x DDR Board Design and Layout Guidelines* for your specific DDR interface type.
- **Has the PDN analysis been performed and are the proper values and number of bypass capacitors included in your design?**

  Use low ESL capacitors and mount them with short traces to keep the mounting inductance very low. This is required to meet the specified PDN impedance. For more details, see *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

2.3 Unused Signals

Signals of unused interfaces can typically be left unconnected, unless otherwise stated.. Many of the I/Os have a Pad Configuration Register that gives control over the input capabilities of the I/O (INPUTENABLE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the *AM64x/AM243x Technical Reference Manual*. Software should disable the I/O receive buffers (that is, INPUTENABLE=0) that are not connected in the design as soon as possible during initialization.

Note

For specific guidance on certain unused pins, see the *Connections for Unused Pins* section in the *AM64x Sitara™ Processors Data Sheet* and *AM243x Sitara™ Processors Data Sheet*.

Note

For specific guidance configuring I/Os, see the *Pad Configuration Registers* chapter in the *AM64x/AM243x Technical Reference Manual*.

2.4 Reset

- **Do you have a reset circuit that generates the proper reset signals into MCU_PORz, MCU_RESETz and RESET_REQz?**

  The reset signals into MCU_PORz, MCU_RESETz and RESET_REQz must meet the requirements for pulse length and must be held low during power sequencing.
- **Are all control/configuration pins held in the proper state until reset is released?**

  These inputs are used to configure the device and must be held in the desired known state until after the rising edge of the MCU_PORz. This applies to both the SoC as well as any attached peripherals that have such configuration pins such as the Ethernet PHYs.

2.5 Boot Modes

- **Do all BOOTMODE inputs require external pulling resistors or a circuit to drive these inputs to a valid state that defines the desired boot mode?**

  BOOTMODE inputs do not have internal pull-up or pull-down resistors that are active during power up and reset. External pull resistors must be used to set the boot mode. Alternatively, a buffer that is only driven when reset is active can be used to present the boot mode. MCU_RESETSTATz can be used to enable this buffer when it is low.

- **Is the expected boot configuration present on the BOOTMODE pins when PORz_OUT is active (low)?**

  PORz_OUT should be used as an enable signal for any bootmode buffers on signals that are also used for I/O. If the I/Os associated with boot mode inputs are redefined for another signal function during operation, they must be released and set back to the proper logic levels to select the boot mode whenever the SoC enters the cold reset state. This problem may occur when an external device may attempt to drive the bootmode signals.
- **Are you using Ethernet Boot and RGMII?**

  You must implement a PHY that enables RGMII_ID mode on the PHY RX data path and disables RGMII_ID mode on the TX data path by default (the SoC implements RGMII_ID on the TX channel). The SoC ROM is PHY agnostic and will not programatically enable/disable RGMII_ID mode on attached PHYs. Typically this is accomplished via pin strapping option provided by the PHY.

2.6 Clocking

- **Do you have a clock source for MCU_OSC0_XI?**

  A clock source for MCU_OSC0_XI is required for proper operation of the SoC.
- **Is the frequency for MCU_OSC0_XI 25MHz?**

  25MHz is the only supported input clock frequency.
- **Did you implement passive components around the crystal?**

  For more details, see the *MCU_OSC0 Internal Oscillator Clock Source* section in the device *AM64x Sitara™ Processors Data Sheet* or *AM243x Sitara™ Processors Data Sheet*.

2.7 System Issues

Pull-up resistors:

- **Are all pullups connected to the AM64x/AM243x device pulled up to the correct I/O voltage?**

  Pulling a signal to the wrong I/O voltage can cause leakage between the I/O rails of the device. Each terminal has an associated supply voltage used to power its I/O cell. This can be found in the *Ball Characteristics* table in the *AM64x Sitara™ Processors Data Sheet* or *AM243x Sitara™ Processors Data Sheet* respectively.

Peripheral clock outputs:

- **Do you have series termination resistors on the clock outputs?**

  Put 22-Ω series resistors (close to processor) on the output clocks of the SPI module.

General Debug:

- **Have you added visibility for the internal clocks MCU_SYSCLKOUT0, SYSCLKOUT0 and CLKOUT0?**

  Output clocks MCU_SYSCLKOUT0, SYSCLKOUT0 and CLKOUT0 are available on pins. You should consider attaching short signal traces with test points to allow monitoring of internal clocks to enable hardware and software debug if the pins/signals are not muxed to other signal functions in your design.
- **Have you added the ability to probe the MCU_RESETSTATz, RESETSTATz and PORz_OUT signals?**

  Accessible test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT may be useful for debug.

2.8 DDR

Ensure that you have implemented all recommendations found in AM64x/AM243x DDR Board Design and Layout Guidelines for your specific DDR interface type.

2.9 MMC

- **Have you included a series resistor on the MMC0_CLK to dampen reflections?**

  Include a 0Ω series resistor on MMC0_CLK (as close to the processor as possible) in case additional series resistance needs to be inserted. The MMC0_CLK pin is configured to operate as a clock output and input simultaneously and additional series resistance may be required to resolve signal distortion that occurs on the source end of the signal trace, which may cause the MMC0_CLK input buffer to see false clock transitions.

- **Have you included the correct pull resistors for the MMC1 interface ?**

  An approximately 50 KΩ Pull-down resistor is recommended for SD-CARD implementations on the MMC1_CLK pin. Pull-ups of approximately 50 KΩ should be used for each of the CMD and DAT signals as per the SD Card specification.
- **Are you supporting UHS-I using the internal SDIO LDO?**

  The SoC provides an internal SDIO_LDO function which can be used to source the MMC1 IO power rail (VDDSHV5) when providing support for UHS-I SD Cards. SDIO_LDO has a 3.3 V input pin (VDDA_3P3_SDIO) and a 1.8 V or 3.3 V output pin (CAP_VDDS_MMC1), where the output voltage is determined by the MMC1 host controller.

  Make sure you have the proper connectivity for SDIO_LDO, VDDSHV5, SD Card, and external pull-ups when supporting faster data transfer speeds provided by UHS-I SD Cards, which switch to 1.8 V IO signaling after negotiating with the host.

  The SDIO_LDO input must be connected to the same 3.3 V power source that is powering the SD Card. The 3.3 V power source for the SD Card and SDIO_LDO needs to be routed through an external power switch that can be controlled by software. This software controlled power switch is required to reset the SD Card since cycling power to the card is the only way to reset the card back to its default state.

  The SDIO_LDO output should be used to power VDDSHV5, which is the IO Supply for MMC1. The proper decoupling capacitor for the net connecting CAP_VDDS_MMC1 to VDDSHV5 is 3.3 µF.

  If you plan to use MMC1 as a boot device, you must ensure that the external power switch sourcing the SD Card and SDIO_LDO defaults to ON so these devices receive 3.3 V as soon as power is applied. Additionally, all external pull-up resistors connected to the SD Card signals must be connected to the same power source that powers VDDSHV5. An example of such an implementation can be observed on the AM64x GP EVM.
- **Have you connected the SD-CARD's VDD signal to a 3.3 V I/O supply?**

  While the I/O voltage for the SD-CARD interface can be either 1.8 V or 3.3 V, the SD card's VDD signal should be connected to a fixed 3.3 V rail. In other words, the card's VDD must remain at 3.3 V even for the UHS-I modes of operation. Only the signaling levels change in these modes, not VDD.

2.10 OSPI and QSPI

- **Is the OSPI0_LBCLKO signal connected correctly for the device you have selected?**

  The OSPI0_LBCLKO signal is used differently depending on what type of device you are using and whether internal pad loopback is used. For more information, see the *AM64x/AM243x Technical Reference Manual*.
- **Are the OSPI/QSPI data bits connected in the proper order?**

  D0 and D1 of the OSPI peripheral must be connected to D0 and D1 of the QSPI/OSPI memory to support legacy x1 commands. Data swapping is not allowed.

2.11 GPMC NAND

- **Does your design use the NAND R/B# signal?**

  Typically the active high ready / active low busy (R/B#) output from the NAND is open drain and connected to the GPMC0_WAIT0 signal. A 4.7K pullup must be connected between this signal and the respective I/O power source if the R/B# output is open-drain.

2.12 I2C

- **Do you have the I2C pull-ups connected to the correct voltage?**

  I2C interfaces require a pull-up resistor on both the data and the clock lines. 4.7K-Ω pull-up resistors must be attached on both I2C signals (x_SDA and x_SCL). Ensure the pull-up resistors connect to the correct I/O voltage rail. For more information, see the note on the *Pull-up Resistors* bullet in Section 2.7

- **Do you need a fully compliant I2C buffer?**

  The WKUP_I2C0 and MCU_I2C0 use true open-drain buffers that are fully compliant to the I2C specifications. These support 100-kHz and 400-kHz operation. The remaining I2C interfaces, I2C0-I2C2, use LVCMOS to emulate an open-drain buffer. These can support 3.4-Mbps I2C operations; however, these ports are not fully compliant with the I2C specification, in particular falling edges are too fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time.

2.13 CPSW Ethernet

- **Have you correctly configured the initial configuration for your PHY?**

  Most PHYs configure their outputs as inputs during reset, and captures configuration information on theses I/Os when the device is released from reset. Therefore, it may be necessary to apply appropriate pull-up/pull-down resistors on these I/Os which also connect to AM64x/AM243x I/Os. The TI PHYs used on the GP EVM use a combination of pull-up and pull-down resistors to generate a mid-level voltage, allowing multiple configuration bits to be encoded on each pin. By default, the AM64x/AM243x input buffers and internal pull-up/pull-down resistors are disabled, which eliminates any concern with a mid-supply potential being applied to the AM64x/AM243x input buffer when required by the PHY. The PHYs should be removed from reset before enabling any of the associated AM64x/AM243x input buffers to ensure the PHY is driving a valid logic state before enabling the AM64x/AM243x input buffers.
- **Have you terminated your RGMII signals correctly?**

  A 22-Ω series termination resistor is recommended (but optional) to be placed on each of the 12 RGMII interface signals as close as possible to the sourcing pin.

2.14 ICSSG

- **Have you selected the correct pins for your industrial application?**

  ICSSG pins allow muxing at the ICSSG IP level and at the SoC level using the PADCONFx registers. Carefully check that you have connected your schematic correctly for your application. In particular, review the differences between the RGMII connections and the MII connections for the TX pins.
- **Are you using an MII interface to an Ethernet PHY?**

  Some industrial protocols require the use of a 10/100-Mbit Ethernet. MII may be required to operate these protocols correctly. Check with your PHY manufacturer to determine if MII is needed.
- **Have you terminated your RGMII signals correctly?**

  A 22-Ω series termination resistor is recommended (but optional) to be placed on each of the 12 RGMII interface signals as close as possible to the sourcing pin.

2.15 USB2 - High Speed

- **Have you planned for the routing in the USB interface?**

  For detailed recommendations on proper USB signal connection and routing, see the *High-Speed Interface Layout Guidelines*. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you included the correct VBUS decoupling for your configuration?**

  USB device operation requires decoupling capacitance of less than 10 µF connected to the USB VBUS. USB host operation requires decoupling capacitance of greater than 120 µF connected to the USB VBUS. VBUS decoupling capacitance should be connected close to the USB connector.
- **Have you connected the USB_DP and USB_DM signals directly to the connector?**

  USB_DP and USB_DM should never have any series resistors or capacitors on these signals. These signals should be routed with traces that do not include stubs or test points. These traces should be connected directly between the AM64x and the connector, unless EMI control is needed.

- **If you are operating in USB Host mode, have you connected the USB signals correctly?**

  USB_ID should be grounded. The USB_DRVVBUS should be connected to enable the 5-V VBUS power source. The VBUS pin on the USB connector should be connected to the output of the 5-V VBUS power from the power switch controlled by USB_DRVVBUS. **Be sure to implement the recommended circuit shown in the Data Manual on the VBUS pin to make it failsafe and 5V tolerant.**
- **If you are including a USB hub, have you connected the USB signals correctly?**

  USB_DP and USB_DM should be connected directly to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. The connector ID should be grounded to enable host mode. As each hub has different implementation requirements, the customer should seek implementation advice from the hub manufacturer.
- **Do you need components for EMI and ESD protection?**

  Common-mode chokes may be needed for EMI/EMC control. These may reduce the signal amplitude and degrade performance. In addition, ESD suppression may also be required. If necessary, these components should be included in the design.

2.16 USB3 - Super Speed

- **Have you planned for the routing in the USB3 interface?**

  For detailed recommendations for proper USB3 SERDES signal connection and routing, see the *High-Speed Interface Layout Guidelines*. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you included DC-blocking capacitors in the correct location?**

  DC-blocking capacitors are required for USB3 transmit and receive pairs, but the capacitors should be placed closer to the USB3 transmitter. If a USB3 connector is used in the design, the receive pair will be connected directly to the connector. The DC-blocking caps for the receive pair are present on the device connected to the USB3 connector.
- **Have you connected the correct USB2 signals for the USB2 compatibility?**

  USB3 connectors include both the USB3 and USB2 connections for compatibility with older USB devices. The USB_DP and USB_DM signals **must** be connected to the USB3 connector along with the USB3 pairs if USB3 is used. USB2 can be used without USB3, but if USB3 is used, USB2 must also be routed to the same connector. Splitting USB2 and USB3 to different connectors is not permitted in the USB specification.

2.17 PCIe

- **Have you planned for the routing in the PCIE interface?**

  For detailed recommendations on proper PCIE SERDES signal connection and routing, see the *High-Speed Interface Layout Guidelines*. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you included DC-blocking capacitors in the correct location?**

  DC-blocking capacitors are required for PCIE transmit and receive pairs, but the capacitors should be placed closer to the PCIE transmitter. If a PCIE connector is used in the design, the receive pair will be connected directly to the connector. The DC-blocking caps for the receive pair are present on the device connected to the PCIE connector.

2.18 JTAG and EMU

To ensure a proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

- **Have you included a JTAG connection?**

  If the JTAG and EMU interface is not used, all pins except TRSTn, TCK, and TMS can be left floating. TRSTn must be pulled low to ground through a 4.7k-Ω resistor. TCK and TMS must be pulled separately to VDDSHV_MCU through a 4.7k-Ω resistor. However, TI strongly recommends that all board designs contain at least a minimal JTAG port connection to test points or a header footprint to support early prototype debugging. The minimum connections are TCK, TMS, TDI, TDO, and TRSTn. JTAG routes and component footprints (except the PD on TRSTn and the PU on TMS and TCK) can be deleted in the production version of the board, if desired.
- **Have you provided the proper buffering for robust JTAG operation?**

  For more details, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.
- **Are you connecting the TRC_x signals for trace operation?**

  If trace operation is needed, the TRC_x signals must be connected to the emulation connector. All TRC_x signals are pin-muxed with other signals. If the trace connections are needed, the connections for GPMC interface may not be used. Routes for TRC_x signals used for trace must be short and skew matched. Trace signals are on a separate power domain, VDDSHV3, and can be at a different voltage from the other JTAG signals. For more recommendations on TRC/EMU routing, see the *Emulation and Trace Headers Technical Reference Manual* A similar summary of this information is available at *XDS Target Connection Guide*

3 References

- Texas Instruments: *AM64x Sitara™ Processors Data Sheet*
- Texas Instruments: *AM243x Sitara™ Processors Data Sheet*
- Texas Instruments: *AM64x/AM243x Technical Reference Manual*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *AM64x/AM243x DDR Board Design and Layout Guidelines*
- Texas Instruments: *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2021) to Revision B (June 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updates were made in Section 2.9	4

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265