TEXAS INSTRUMENTS

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ADVANCE INFORMATION

1 Device Memory Map

This section describes the device memory map.

Note

The memory locations not shown are either unallocated or reserved and not used.

Accesses to these locations are not recommended and should be avoided.

Table 1-1. AM263x Memory Map

Region Name	Start Address	End Address	Size
Core-specific Internal Memory Map[1]	0x0000 0000	0x1FFF FFFF	~537 MB
MCRC0	0x3500 0000	0x3500 03FF	1 KB
STM_STIM	0x3900 0000	0x39FF FFFF	16 MB
MPU_L2OCRAM_BANK0	0x4002 0000	0x4002 0FFF	4 KB
MPU_L2OCRAM_BANK1	0x4004 0000	0x4004 0FFF	4 KB
MPU_L2OCRAM_BANK2	0x4006 0000	0x4006 0FFF	4 KB
MPU_L2OCRAM_BANK3	0x4008 0000	0x4008 0FFF	4 KB
MPU_R5SS0_CORE0_AXIS	0x400A 0000	0x400A 0FFF	4 KB
MPU_R5SS0_CORE1_AXIS	0x400C 0000	0x400C 0FFF	4 KB
MPU_R5SS1_CORE0_AXIS	0x400E 0000	0x400E 0FFF	4 KB
MPU_R5SS1_CORE1_AXIS	0x4010 0000	0x4010 0FFF	4 KB
MPU_HSM_DTHE	0x401 20000	0x4012 0FFF	4 KB
MPU_MBOX_SRAM	0x4014 0000	0x4014 0FFF	4 KB
MPU_QSPI0	0x4016 0000	0x4016 0FFF	4 KB
MPU_SCRM2SCRP0	0x4018 0000	0x4018 0FFF	4 KB
MPU_SCRM2SCRP1	0x401A 0000	0x401A 0FFF	4 KB
MPU_R5SS0_CORE0_AHB	0x401C 0000	0x401C 0FFF	4 KB
MPU_R5SS0_CORE1_AHB	0x401E 0000	0x401E 0FFF	4 KB
MPU_R5SS1_CORE0_AHB	0x4020 0000	0x4020 0FFF	4 KB
MPU_R5SS1_CORE1_AHB	0x4022 0000	0x4022 0FFF	4 KB
MPU_HSM	0x4024 0000	0x4024 0FFF	4 KB
HSM_INTERNAL[1]	0x40F7 8000	0x47FF FFFF	118 MB
ICSSM0_INTERNAL[1]	0x4800 0000	0x4803 FFFF	256 KB
ICSSM0_ECC	0x4810 0000	0x4810 03FF	1 KB
QSPI0	0x4820 0000	0x4820 01FF	512 Bytes
MMC0	0x4830 0000	0x4830 1FFF	8 KB
GPMC0_CFG	0x4840 0000	0x4840 03FF	1 KB
CONTROLSS_G0_EPWM0	0x5000 0000	0x5000 0FFF	4 KB
CONTROLSS_G0_EPWM1	0x5000 1000	0x5000 1FFF	4 KB
CONTROLSS_G0_EPWM2	0x5000 2000	0x5000 2FFF	4 KB
CONTROLSS_G0_EPWM3	0x5000 3000	0x5000 3FFF	4 KB
CONTROLSS_G0_EPWM4	0x5000 4000	0x5000 4FFF	4 KB
CONTROLSS_G0_EPWM5	0x5000 5000	0x5000 5FFF	4 KB
CONTROLSS_G0_EPWM6	0x50006000	0x5000 6FFF	4 KB
CONTROLSS_G0_EPWM7	0x5000 7000	0x5000 7FFF	4 KB
CONTROLSS_G0_EPWM8	0x5000 8000	0x5000 8FFF	4 KB
CONTROLSS_G0_EPWM9	0x5000 9000	0x5000 9FFF	4 KB
CONTROLSS_G0_EPWM10	0x5000 A000	0x5000 AFFF	4 KB
CONTROLSS_G0_EPWM11	0x5000 B000	0x5000 BFFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G0_EPWM12	0x5000 C000	0x5000 CFFF	4 KB
CONTROLSS_G0_EPWM13	0x5000 D000	0x5000 DFFF	4 KB
CONTROLSS_G0_EPWM14	0x5000 E000	0x5000 EFFF	4 KB
CONTROLSS_G0_EPWM15	0x5000 F000	0x5000 FFFF	4 KB
CONTROLSS_G0_EPWM16	0x5001 0000	0x5001 0FFF	4 KB
CONTROLSS_G0_EPWM17	0x5001 1000	0x5001 1FFF	4 KB
CONTROLSS_G0_EPWM18	0x5001 2000	0x5001 2FFF	4 KB
CONTROLSS_G0_EPWM19	0x5001 3000	0x5001 3FFF	4 KB
CONTROLSS_G0_EPWM20	0x5001 4000	0x5001 4FFF	4 KB
CONTROLSS_G0_EPWM21	0x5001 5000	0x5001 5FFF	4 KB
CONTROLSS_G0_EPWM22	0x5001 6000	0x5001 6FFF	4 KB
CONTROLSS_G0_EPWM23	0x5001 7000	0x5001 7FFF	4 KB
CONTROLSS_G0_EPWM24	0x5001 8000	0x5001 8FFF	4 KB
CONTROLSS_G0_EPWM25	0x5001 9000	0x5001 9FFF	4 KB
CONTROLSS_G0_EPWM26	0x5001 A000	0x5001 AFFF	4 KB
CONTROLSS_G0_EPWM27	0x5001 B000	0x5001 BFFF	4 KB
CONTROLSS_G0_EPWM28	0x5001 C000	0x5001 CFFF	4 KB
CONTROLSS_G0_EPWM29	0x5001 D000	0x5001 DFFF	4 KB
CONTROLSS_G0_EPWM30	0x5001 E000	0x5001 EFFF	4 KB
CONTROLSS_G0_EPWM31	0x5001 F000	0x5001 FFFF	4 KB
CONTROLSS_G1_EPWM0	0x5004 0000	0x5004 0FFF	4 KB
CONTROLSS_G1_EPWM1	0x5004 1000	0x5004 1FFF	4 KB
CONTROLSS_G1_EPWM2	0x5004 2000	0x5004 2FFF	4 KB
CONTROLSS_G1_EPWM3	0x5004 3000	0x5004 3FFF	4 KB
CONTROLSS_G1_EPWM4	0x5004 4000	0x5004 4FFF	4 KB
CONTROLSS_G1_EPWM5	0x5004 5000	0x5004 5FFF	4 KB
CONTROLSS_G1_EPWM6	0x5004 6000	0x5004 6FFF	4 KB
CONTROLSS_G1_EPWM7	0x5004 7000	0x5004 7FFF	4 KB
CONTROLSS_G1_EPWM8	0x5004 8000	0x5004 8FFF	4 KB
CONTROLSS_G1_EPWM9	0x5004 9000	0x5004 9FFF	4 KB
CONTROLSS_G1_EPWM10	0x5004 A000	0x5004 AFFF	4 KB
CONTROLSS_G1_EPWM11	0x5004 B000	0x5004 BFFF	4 KB
CONTROLSS_G1_EPWM12	0x5004 C000	0x5004 CFFF	4 KB
CONTROLSS_G1_EPWM13	0x5004 D000	0x5004 DFFF	4 KB
CONTROLSS_G1_EPWM14	0x5004 E000	0x5004 EFFF	4 KB
CONTROLSS_G1_EPWM15	0x5004 F000	0x5004 FFFF	4 KB
CONTROLSS_G1_EPWM16	0x5005 0000	0x5005 0FFF	4 KB
CONTROLSS_G1_EPWM17	0x5005 1000	0x5005 1FFF	4 KB
CONTROLSS_G1_EPWM18	0x5005 2000	0x5005 2FFF	4 KB
CONTROLSS_G1_EPWM19	0x5005 3000	0x5005 3FFF	4 KB
CONTROLSS_G1_EPWM20	0x5005 4000	0x5005 4FFF	4 KB
CONTROLSS_G1_EPWM21	0x5005 5000	0x5005 5FFF	4 KB
CONTROLSS_G1_EPWM22	0x5005 6000	0x5005 6FFF	4 KB
CONTROLSS_G1_EPWM23	0x5005 7000	0x5005 7FFF	4 KB
CONTROLSS_G1_EPWM24	0x5005 8000	0x5005 8FFF	4 KB
CONTROLSS_G1_EPWM25	0x5005 9000	0x5005 9FFF	4 KB
CONTROLSS_G1_EPWM26	0x5005 A000	0x5005 AFFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G1_EPWM27	0x5005 B000	0x5005 BFFF	4 KB
CONTROLSS_G1_EPWM28	0x5005 C000	0x5005 CFFF	4 KB
CONTROLSS_G1_EPWM29	0x5005 D000	0x5005 DFFF	4 KB
CONTROLSS_G1_EPWM30	0x5005 E000	0x5005 EFFF	4 KB
CONTROLSS_G1_EPWM31	0x5005 F000	0x5005 FFFF	4 KB
CONTROLSS_G2_EPWM0	0x5008 0000	0x5008 0FFF	4 KB
CONTROLSS_G2_EPWM1	0x5008 1000	0x5008 1FFF	4 KB
CONTROLSS_G2_EPWM2	0x5008 2000	0x5008 2FFF	4 KB
CONTROLSS_G2_EPWM3	0x5008 3000	0x5008 3FFF	4 KB
CONTROLSS_G2_EPWM4	0x5008 4000	0x5008 4FFF	4 KB
CONTROLSS_G2_EPWM5	0x5008 5000	0x5008 5FFF	4 KB
CONTROLSS_G2_EPWM6	0x5008 6000	0x5008 6FFF	4 KB
CONTROLSS_G2_EPWM7	0x5008 7000	0x5008 7FFF	4 KB
CONTROLSS_G2_EPWM8	0x5008 8000	0x5008 8FFF	4 KB
CONTROLSS_G2_EPWM9	0x5008 9000	0x5008 9FFF	4 KB
CONTROLSS_G2_EPWM10	0x5008 A000	0x5008 AFFF	4 KB
CONTROLSS_G2_EPWM11	0x5008 B000	0x5008 BFFF	4 KB
CONTROLSS_G2_EPWM12	0x5008 C000	0x5008 CFFF	4 KB
CONTROLSS_G2_EPWM13	0x5008 D000	0x5008 DFFF	4 KB
CONTROLSS_G2_EPWM14	0x5008 E000	0x5008 EFFF	4 KB
CONTROLSS_G2_EPWM15	0x5008 F000	0x5008 FFFF	4 KB
CONTROLSS_G2_EPWM16	0x5009 0000	0x5009 0FFF	4 KB
CONTROLSS_G2_EPWM17	0x5009 1000	0x5009 1FFF	4 KB
CONTROLSS_G2_EPWM18	0x5009 2000	0x5009 2FFF	4 KB
CONTROLSS_G2_EPWM19	0x5009 3000	0x5009 3FFF	4 KB
CONTROLSS_G2_EPWM20	0x5009 4000	0x5009 4FFF	4 KB
CONTROLSS_G2_EPWM21	0x5009 5000	0x5009 5FFF	4 KB
CONTROLSS_G2_EPWM22	0x5009 6000	0x5009 6FFF	4 KB
CONTROLSS_G2_EPWM23	0x5009 7000	0x5009 7FFF	4 KB
CONTROLSS_G2_EPWM24	0x5009 8000	0x5009 8FFF	4 KB
CONTROLSS_G2_EPWM25	0x5009 9000	0x5009 9FFF	4 KB
CONTROLSS_G2_EPWM26	0x5009 A000	0x5009 AFFF	4 KB
CONTROLSS_G2_EPWM27	0x5009 B000	0x5009 BFFF	4 KB
CONTROLSS_G2_EPWM28	0x5009 C000	0x5009 CFFF	4 KB
CONTROLSS_G2_EPWM29	0x5009 D000	0x5009 DFFF	4 KB
CONTROLSS_G2_EPWM30	0x5009 E000	0x5009 EFFF	4 KB
CONTROLSS_G2_EPWM31	0x5009 F000	0x5009 FFFF	4 KB
CONTROLSS_G3_EPWM0	0x500C 0000	0x500C 0FFF	4 KB
CONTROLSS_G3_EPWM1	0x500C 1000	0x500C 1FFF	4 KB
CONTROLSS_G3_EPWM2	0x500C 2000	0x500C 2FFF	4 KB
CONTROLSS_G3_EPWM3	0x500C 3000	0x500C 3FFF	4 KB
CONTROLSS_G3_EPWM4	0x500C 4000	0x500C 4FFF	4 KB
CONTROLSS_G3_EPWM5	0x500C 5000	0x500C 5FFF	4 KB
CONTROLSS_G3_EPWM6	0x500C 6000	0x500C 6FFF	4 KB
CONTROLSS_G3_EPWM7	0x500C 7000	0x500C 7FFF	4 KB
CONTROLSS_G3_EPWM8	0x500C 8000	0x500C 8FFF	4 KB
CONTROLSS_G3_EPWM9	0x500C 9000	0x500C 9FFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G3_EPWM10	0x500C A000	0x500C AFFF	4 KB
CONTROLSS_G3_EPWM11	0x500C B000	0x500C BFFF	4 KB
CONTROLSS_G3_EPWM12	0x500C C000	0x500C CFFF	4 KB
CONTROLSS_G3_EPWM13	0x500C D000	0x500C DFFF	4 KB
CONTROLSS_G3_EPWM14	0x500C E000	0x500C EFFF	4 KB
CONTROLSS_G3_EPWM15	0x500C F000	0x500C FFFF	4 KB
CONTROLSS_G3_EPWM16	0x500D 0000	0x500D 0FFF	4 KB
CONTROLSS_G3_EPWM17	0x500D 1000	0x500D 1FFF	4 KB
CONTROLSS_G3_EPWM18	0x500D 2000	0x500D 2FFF	4 KB
CONTROLSS_G3_EPWM19	0x500D 3000	0x500D 3FFF	4 KB
CONTROLSS_G3_EPWM20	0x500D 4000	0x500D 4FFF	4 KB
CONTROLSS_G3_EPWM21	0x500D 5000	0x500D 5FFF	4 KB
CONTROLSS_G3_EPWM22	0x500D 6000	0x500D 6FFF	4 KB
CONTROLSS_G3_EPWM23	0x500D 7000	0x500D 7FFF	4 KB
CONTROLSS_G3_EPWM24	0x500D 8000	0x500D 8FFF	4 KB
CONTROLSS_G3_EPWM25	0x500D 9000	0x500D 9FFF	4 KB
CONTROLSS_G3_EPWM26	0x500D A000	0x500D AFFF	4 KB
CONTROLSS_G3_EPWM27	0x500D B000	0x500D BFFF	4 KB
CONTROLSS_G3_EPWM28	0x500D C000	0x500D CFFF	4 KB
CONTROLSS_G3_EPWM29	0x500DD000	0x500D DFFF	4 KB
CONTROLSS_G3_EPWM30	0x500D E000	0x500D EFFF	4 KB
CONTROLSS_G3_EPWM31	0x500D F000	0x500D FFFF	4 KB
CONTROLSS_ADC0_RESULT	0x5010 0000	0x5010 0FFF	4 KB
CONTROLSS_ADC1_RESULT	0x5010 1000	0x5010 1FFF	4 KB
CONTROLSS_ADC2_RESULT	0x5010 2000	0x5010 2FFF	4 KB
CONTROLSS_ADC3_RESULT	0x5010 3000	0x5010 3FFF	4 KB
CONTROLSS_ADC4_RESULT	0x5010 4000	0x5010 4FFF	4 KB
CONTROLSS_CMPSSA0	0x5020 0000	0x5020 0FFF	4 KB
CONTROLSS_CMPSSA1	0x5020 1000	0x5020 1FFF	4 KB
CONTROLSS_CMPSSA2	0x5020 2000	0x5020 2FFF	4 KB
CONTROLSS_CMPSSA3	0x5020 3000	0x5020 3FFF	4 KB
CONTROLSS_CMPSSA4	0x5020 4000	0x5020 4FFF	4 KB
CONTROLSS_CMPSSA5	0x5020 5000	0x5020 5FFF	4 KB
CONTROLSS_CMPSSA6	0x5020 6000	0x5020 6FFF	4 KB
CONTROLSS_CMPSSA7	0x5020 7000	0x5020 7FFF	4 KB
CONTROLSS_CMPSSA8	0x5020 8000	0x5020 8FFF	4 KB
CONTROLSS_CMPSSA9	0x5020 9000	0x5020 9FFF	4 KB
CONTROLSS_CMPSSB0	0x5022 0000	0x5022 0FFF	4 KB
CONTROLSS_CMPSSB1	0x5022 1000	0x5022 1FFF	4 KB
CONTROLSS_CMPSSB2	0x5022 2000	0x5022 2FFF	4 KB
CONTROLSS_CMPSSB3	0x5022 3000	0x5022 3FFF	4 KB
CONTROLSS_CMPSSB4	0x5022 4000	0x5022 4FFF	4 KB
CONTROLSS_CMPSSB5	0x5022 5000	0x5022 5FFF	4 KB
CONTROLSS_CMPSSB6	0x5022 6000	0x5022 6FFF	4 KB
CONTROLSS_CMPSSB7	0x5022 7000	0x5022 7FFF	4 KB
CONTROLSS_CMPSSB8	0x5022 8000	0x5022 8FFF	4 KB
CONTROLSS_CMPSSB9	0x5022 9000	0x5022 9FFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_ECAP0	0x5024 0000	0x5024 0FFF	4 KB
CONTROLSS_ECAP1	0x5024 1000	0x5024 1FFF	4 KB
CONTROLSS_ECAP2	0x5024 2000	0x5024 2FFF	4 KB
CONTROLSS_ECAP3	0x5024 3000	0x5024 3FFF	4 KB
CONTROLSS_ECAP4	0x5024 4000	0x5024 4FFF	4 KB
CONTROLSS_ECAP5	0x5024 5000	0x5024 5FFF	4 KB
CONTROLSS_ECAP6	0x5024 6000	0x5024 6FFF	4 KB
CONTROLSS_ECAP7	0x5024 7000	0x5024 7FFF	4 KB
CONTROLSS_ECAP8	0x5024 8000	0x5024 8FFF	4 KB
CONTROLSS_ECAP9	0x5024 9000	0x5024 9FFF	4 KB
CONTROLSS_DAC0	0x5026 0000	0x5026 0FFF	4 KB
CONTROLSS_SDFM0	0x5026 8000	0x5026 8FFF	4 KB
CONTROLSS_SDFM1	0x5026 9000	0x5026 9FFF	4 KB
CONTROLSS_EQEP0	0x5027 0000	0x5027 0FFF	4 KB
CONTROLSS_EQEP1	0x5027 1000	0x5027 1FFF	4 KB
CONTROLSS_EQEP2	0x50272000	0x5027 2FFF	4 KB
CONTROLSS_FSI0_TX0	0x5028 0000	0x5028 0FFF	4 KB
CONTROLSS_FSI0_TX1	0x5028 1000	0x5028 1FFF	4 KB
CONTROLSS_FSI0_RX0	0x5029 0000	0x5029 0FFF	4 KB
CONTROLSS_FSI0_RX1	0x5029 1000	0x5029 1FFF	4 KB
CONTROLSS_FSI1_TX2	0x502A 0000	0x502A 0FFF	4 KB
CONTROLSS_FSI1_TX3	0x502A 1000	0x502A 1FFF	4 KB
CONTROLSS_FSI1_RX2	0x502B 0000	0x502B 0FFF	4 KB
CONTROLSS_FSI1_RX3	0x502B 1000	0x502B 1FFF	4 KB
CONTROLSS_ADC0_CFG	0x502C 0000	0x502C 0FFF	4 KB
CONTROLSS_ADC1_CFG	0x502C 1000	0x502C 1FFF	4 KB
CONTROLSS_ADC2_CFG	0x502C 2000	0x502C 2FFF	4 KB
CONTROLSS_ADC3_CFG	0x502C 3000	0x502C 3FFF	4 KB
CONTROLSS_ADC4_CFG	0x502C 4000	0x502C 4FFF	4 KB
CONTROLSS_INPUTXBAR	0x502D 0000	0x502D 0FFF	4 KB
CONTROLSS_PWMXBAR	0x502D 1000	0x502D 1FFF	4 KB
CONTROLSS_PWMSYNCOUTXBAR	0x502D 2000	0x502D 2FFF	4 KB
CONTROLSS_INTXBAR	0x502D 5000	0x502D 5FFF	4 KB
CONTROLSS_DMAXBAR	0x502D 6000	0x502D 6FFF	4 KB
CONTROLSS_OUTPUTXBAR	0x502D 8000	0x502D 8FFF	4 KB
CONTROLSS_OTTOCAL0	0x502E 0000	0x502E 0FFF	4 KB
CONTROLSS_OTTOCAL1	0x502E 1000	0x502E 1FFF	4 KB
CONTROLSS_OTTOCAL2	0x502E 2000	0x502E 2FFF	4 KB
CONTROLSS_OTTOCAL3	0x502E 3000	0x502E 3FFF	4 KB
CONTROLSS_CTRL	0x502F 0000	0x502F 7FFF	32 KB
DEBUGSS	0x5080 0000	0x508F FFFF	1024 KB
MSS_CTRL	0x50D0 0000	0x50D3 FFFF	256 KB
TOP_CTRL	0x50D8 0000	0x50D8 7FFF	32 KB
SPINLOCK0	0x50E0 0000	0x50E0 7FFF	32 KB
VIM	0x50F0 0000	0x50F0 3FFF	16 KB
GPIO0	0x5200 0000	0x5200 00FF	256 Bytes
GPIO1	0x5200 1000	0x5200 10FF	256 Bytes

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
GPIO2	0x5200 2000	0x5200 20FF	256 Bytes
GPIO3	0x5200 3000	0x5200 30FF	256 Bytes
WDT0	0x5210 0000	0x5210 00FF	256 Bytes
WDT1	0x5210 1000	0x5210 10FF	256 Bytes
WDT2	0x5210 2000	0x5210 20FF	256 Bytes
WDT3	0x5210 3000	0x5210 30FF	256 Bytes
RTI0	0x5218 0000	0x5218 03FF	1 KB
RTI1	0x5218 1000	0x5218 13FF	1 KB
RTI2	0x5218 2000	0x5218 23FF	1 KB
RTI3	0x5218 3000	0x5218 33FF	1 KB
MCSPI0	0x5220 0000	0x5220 01FF	512 Bytes
MCSPI1	0x5220 1000	0x5220 11FF	512 Bytes
MCSPI2	0x5220 2000	0x5220 21FF	512 Bytes
MCSPI3	0x5220 3000	0x5220 31FF	512 Bytes
MCSPI4	0x5220 4000	0x5220 41FF	512 Bytes
UART0	0x5230 0000	0x5230 01FF	512 Bytes
UART1	0x5230 1000	0x5230 11FF	512 Bytes
UART2	0x5230 2000	0x5230 21FF	512 Bytes
UART3	0x5230 3000	0x5230 31FF	512 Bytes
UART4	0x5230 4000	0x5230 41FF	512 Bytes
UART5	0x5230 5000	0x5230 51FF	512 Bytes
LIN0	0x5240 0000	0x5240 00FF	256 Bytes
LIN1	0x5240 1000	0x5240 10FF	256 Bytes
LIN2	0x5240 2000	0x5240 20FF	256 Bytes
LIN3	0x5240 3000	0x5240 30FF	256 Bytes
LIN4	0x5240 4000	0x5240 40FF	256 Bytes
I2C0	0x5250 0000	0x5250 00FF	256 Bytes
I2C1	0x5250 1000	0x5250 10FF	256 Bytes
I2C2	0x5250 2000	0x5250 20FF	256 Bytes
I2C3	0x5250 3000	0x5250 30FF	256 Bytes
MCAN0_MSG_RAM	0x5260 0000	0x5260 7FFF	32 KB
MCAN0_CFG	0x5260 8000	0x5260 83FF	1 KB
MCAN1_MSG_RAM	0x52610000	0x5261 7FFF	32 KB
MCAN1_CFG	0x5261 8000	0x5261 83FF	1 KB
MCAN2_MSG_RAM	0x5262 0000	0x5262 7FFF	32 KB
MCAN2_CFG	0x5262 8000	0x5262 83FF	1 KB
MCAN3_MSG_RAM	0x5263 0000	0x5263 7FFF	32 KB
MCAN3_CFG	0x5263 8000	0x5263 83FF	1 KB
MCAN0_ECC	0x5270 0000	0x5270 03FF	1 KB
MCAN1_ECC	0x5270 1000	0x5270 13FF	1 KB
MCAN2_ECC	0x5270 2000	0x5270 23FF	1 KB
MCAN3_ECC	0x5270 3000	0x5270 33FF	1 KB
ELM0	0x527F 0000	0x527F 0FFF	4 KB
CPSW0	0x5280 0000	0x529F FFFF	2 MB
TPCC0	0x52A0 0000	0x52A0 7FFF	32 KB
TPTC00	0x52A40000	0x52A4 0FFF	4 KB
TPTC01	0x52A6 0000	0x52A6 0FFF	4 KB

Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
DCC0	0x52B0 0000	0x52B0 00FF	256 Bytes
DCC1	0x52B0 1000	0x52B0 10FF	256 Bytes
DCC2	0x52B0 2000	0x52B0 20FF	256 Bytes
DCC3	0x52B0 3000	0x52B0 30FF	256 Bytes
TOP_ESM	0x52D0 0000	0x52D0 0FFF	4 KB
SOC_TIMESYNC_XBAR0	0x52E0 0000	0x52E0 00FF	256 Bytes
EDMA_TRIG_XBAR	0x52E0 1000	0x52E0 11FF	512 Bytes
GPIO_INTR_XBAR	0x52E0 2000	0x52E0 23FF	1 KB
ICSSM_INTR_XBAR	0x52E0 3000	0x52E0 30FF	256 Bytes
SOC_TIMESYNC_XBAR1	0x52E0 4000	0x52E0 43FF	1 KB
ECC_AGG_R5SS0_CORE0	0x5300 0000	0x5300 03FF	1 KB
ECC_AGG_R5SS0_CORE1	0x5300 3000	0x5300 33FF	1 KB
ECC_AGG_R5SS1_CORE0	0x5300 4000	0x5300 43FF	1 KB
ECC_AGG_R5SS1_CORE1	0x5300 7000	0x5300 73FF	1 KB
ECC_AGG_TOP	0x5301 0000	0x5301 03FF	1 KB
IOMUX	0x5310 0000	0x5310 0FFF	4 KB
TOP_RCM	0x5320 0000	0x5320 7FFF	32 KB
MSS_RCM	0x5320 8000	0x5320 FFFF	32 KB
R5SS0_CCMR	0x5321 0000	0x5321 0FFF	4 KB
R5SS1_CCMR	0x5321 1000	0x5321 1FFF	4 KB
TOP_PBIST	0x5330 0000	0x5330 03FF	1 KB
R5SS0_STC	0x5350 0000	0x5350 01FF	512 Bytes
R5SS1_STC	0x5351 0000	0x5351 01FF	512 Bytes
TOP_EFUSE_FARM	0x5360 0000	0x5360 00FF	256 Bytes
EXT_FLASH0	0x6000 0000	0x61FF FFFF	32 MB
EXT_FLASH1	0x6200 0000	0x63FF FFFF	32 MB
GPMC0_MEM	0x6800 0000	0x6FFF FFFF	128 MB
L2OCRAM	0x7000 0000	0x701F FFFF	2 MB
MBOX_SRAM	0x7200 0000	0x7200 3FFF	16 KB
R5SS0_CORE0_ICACHE[4]	0x7400 0000	0x747F FFFF	8 MB
R5SS0_CORE0_DCACHE[4]	0x7480 0000	0x74FF FFFF	8 MB
R5SS0_CORE1_ICACHE[2 4]	0x7500 0000	0x757F FFFF	8 MB
R5SS0_CORE1_DCACHE[2 4]	0x7580 0000	0x75FF FFFF	8 MB
R5SS1_CORE0_ICACHE[4]	0x7600 0000	0x767F FFFF	8 MB
R5SS1_CORE0_DCACHE[4]	0x7680 0000	0x76FF FFFF	8 MB
R5SS1_CORE1_ICACHE[2 4]	0x7700 0000	0x777F FFFF	8 MB
R5SS1_CORE1_DCACHE[2 4]	0x7780 0000	0x77FF FFFF	8 MB
R5SS0_CORE0_TCMA[3 4]	0x7800 0000	0x7800 FFFF	64 KB
R5SS0_CORE0_TCMB[3 4]	0x7810 0000	0x7810 FFFF	64 KB
R5SS0_CORE1_TCMA[2 4]	0x7820 0000	0x7820 7FFF	32 KB
R5SS0_CORE1_TCMB[2 4]	0x7830 0000	0x7830 7FFF	32 KB
R5SS1_CORE0_TCMA[3 4]	0x7840 0000	0x7840 FFFF	64 KB
R5SS1_CORE0_TCMB[3 4]	0x7850 0000	0x7850 FFFF	64 KB
R5SS1_CORE1_TCMA[2 4]	0x7860 0000	0x7860 7FFF	32 KB
R5SS1_CORE1_TCMB[2 4]	0x7870 0000	0x7870 7FFF	32 KB

1. See core-specific chapter for the internal memory map.

2. In Lockstep mode the R5FSS*x* CORE**1** memory region is not accessible.
3. The size of these memories will change based on Dual-Core vs Lockstep operation.
   For more information about Dual-Core and Lockstep modes see the *R5FSS* chapter.
   For more information about ATCM and BTCM, see the *Tightly-Coupled Memories (TCM)* section within the *R5FSS* chapter.
4. This memory region is used by each CPU core to access the TCM/Cache memory space of other CPU cores.

2 AM263x Control Module Registers (CTRLMMR)

The Control module is the main controller for top-level device behavior in various states. It contains registers for configuration, bootstrap signals, I/O pad multiplexing, clock selection, and many others. There are various CTRLMMR modules in this device:

General SoC Control Modules

- CTRLMMR0 (TOP_CTRL) : Contains SoC-level configuration options
- CTRLMMR1 (MSS_CTRL) : Contains Peripheral-level (non-CONTROLSS) configuration options
- CTRLMMR2 (CONTROLSS_GLOBAL_CTRL): Contains CONTROLSS-level configuration options (General control, reset, and clocking-related functions)

Pad Configuration Control Modules

- PADCFG_CTRLMMR0 (MSS_IOMUX) : Controls the SoC-level terminal configuration options

Reset and Clocking Control Modules

- RCM_CTRLMMR0 (MSS_TOPRCM) : Contains SoC-level Clock and Reset controls
- RCM_CTRLMMR1 (MSS_RCM) : Contains Peripheral-level Clock and Reset controls

2.1 TOP_CTRL Registers

Address Offset	Register	Register Name	Description
0x500	MAC_ID0	MAC Address Lo Register	Ethernet MAC address lower 32-bits.
0x504	MAC_ID1	MAC Address Hi Register	Ethernet MAC address upper 16-bits.
0x538	TSHUT_HOT	TSHUT Hot Temperature	This register provides the factory calibrated Tempcode for theTshut hot Condition
0x53C	TSHUT_COLD	Tshut Cold Temperature	This register provides the factory calibrated Tempcode for theTshut Cold Condition
0x8C0	EFUSE_OVERRIDE_PLL_TRIM	Reserved	Reserved
0xC00	ADC_REFBUF0_CTRL	ADC Reference Buffer 0 Enable Register	This register is used to enable or disable ADC Reference buffer 0
0xC04	ADC_REFBUF1_CTRL	ADC Reference Buffer 1 Enable Register	This register is used to enable or disable ADC Reference buffer 1
0xC08	ADC_REF_COMP_CTRL	ADC Reference Voltage monitor enable Register	This register is used to enable or disable the voltage monitors which measure if the ADC reference voltage is good or not
0xC0C	ADC_REF_GOOD_STATUS	ADC Reference Status	This register shows the status of ADC reference voltages as measured by the ADC Reference OK voltage monitors
0xC10	VMON_CTRL	Voltage monitor enable Register	This register is used to enable or disable the power supply voltage monitors present on the device
0xC14	VMON_STAT	Voltage monitor Status Register	This register shows the status output from the voltage monitors present on the device
0xC18	PMU_COARSE_STAT	Coarse Voltage monitor Status Register	This register shows the status of coarse voltage monitors present in the device
0xC20	MASK_VMON_ERROR_ESM_H	Voltage monitor Error Mask Register0	This register is used to select the voltage monitors whose Error staus should triggering the ESM High Interrupt
0xC24	MASK_VMON_ERROR_ESM_L	Voltage monitor Error Mask Register1	This register is used to select the voltage monitors whose Error staus should triggering the ESM Low Interrupt
0xC30	MASK_ANA_ISO	PMU Reset Mask register	This register is used to prevent the Coarse voltage monitor from triggering a faulty SOC reset due to a momentary supply glitch caused when enabling ADC reference buffers
0xC34	VMON_FILTER_CTRL	Voltage monitor Filter control Register	This register is used to configure the filter present on the Voltage monitor outputs
0xD00	TSENSE_CFG	Temperature Sensor Configuration Register	This register is used to enableand configure the Teperature sensors present in the device
0xD04	TSENSE_STATUS	Temperature Sensor events Status Regster	This register shows the status of Temperature comparator events which are unmasked

Address Offset	Register	Register Name	Description
0xD08	TSENSE_STATUS_RAW	Temperature Sensor events Raw Status Regster	This register shows the status of all Temperature comparators events including masked events
0xD10	TSENSE0_TSHUT	Temp Sensor 0 Tshut temperature override register	This register is used to override the factory specified Tshut temperature with an application specific Tshut temperature for Temperature sensor 0
0xD14	TSENSE0_ALERT	Temp Sensor 0 Alert threshold register	This register is used to configure the temperature thresholds for Temp Sensor 0 for generating Alert Interrupts
0xD18	TSENSE0_CNTL	Temp Sensor 0 control register	This register is used to control and configure Temperature sensor 0
0xD1C	TSENSE0_RESULT	Temp Sensor 0 Result Register	This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 0
0xD20	TSENSE0_DATA0	Temp Sensor 0 Result FIFO Register 0	Temp Sensor 0 Result FIFO Register 0
0xD24	TSENSE0_DATA1	Temp Sensor 0 Result FIFO Register 1	Temp Sensor 0 Result FIFO Register 1
0xD28	TSENSE0_DATA2	Temp Sensor 0 Result FIFO Register 2	Temp Sensor 0 Result FIFO Register 2
0xD2C	TSENSE0_DATA3	Temp Sensor 0 Result FIFO Register 3	Temp Sensor 0 Result FIFO Register 3
0xD30	TSENSE0_ACCU	Temp Sensor 0 Result Accumulator Register	Temp Sensor 0 Result Accumulator Register
0xD40	TSENSE1_TSHUT	Temp Sensor 1 Tshut temperature override register	This register is used to override the factory specified Tshut temperature with an application specific Tshut temperature for Temperature sensor 1
0xD44	TSENSE1_ALERT	Temp Sensor 1 Alert threshold register	This register is used to configure the temperature thresholds for Temp Sensor 1 for generating Alert Interrupts
0xD48	TSENSE1_CNTL	Temp Sensor 1 control register	This register is used to control and configure Temperature sensor 1
0xD4C	TSENSE1_RESULT	Temp Sensor 1 Result Register	This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 1
0xD50	TSENSE1_DATA0	Temp Sensor 1 Result FIFO Register 0	Temp Sensor 1 Result FIFO Register 0
0xD54	TSENSE1_DATA1	Temp Sensor 1 Result FIFO Register 1	Temp Sensor 1 Result FIFO Register 1
0xD58	TSENSE1_DATA2	Temp Sensor 1 Result FIFO Register 2	Temp Sensor 1 Result FIFO Register 2
0xD5C	TSENSE1_DATA3	Temp Sensor 1 Result FIFO Register 3	Temp Sensor 1 Result FIFO Register 3
0xD60	TSENSE1_ACCU	Temp Sensor 1 Result Accumulator Register	Temp Sensor 1 Result Accumulator Register
0xD7C	TSENSE2_RESULT	Temp Sensor 2 Result Register	This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 2
0xDAC	TSENSE3_RESULT	Temp Sensor 3 Result Register	This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 3

2.2 MSS_CTRL Registers

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x20	R5SS0_CONTROL		R5SS0 Lock Step configure register	This register is used to configure R5SS0 in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x024	R5SS0_COREA_HALT	R5SS0_CORE0_HALT	R5SS0 Core 0 Halt Register	This register is used to Halt or Unhalt R5SS0 Core 0
0x028	R5SS0_COREB_HALT	R5SS0_CORE1_HALT	R5SS0 Core 1 Halt Register	This register is used to Halt or Unhalt R5SS0 Core 1
0x02C	R5SS0_STATUS_REG		R5SS0 Lock step Status register	This register shows whether R5SS0 is in Lock step or Dual core mode
0x030	R5SS0_CORE0_STAT		R5SS0 Core 0 Idle Status register	This register shows the WFI WFE status of R5SS0 Core 0
0x034	R5SS0_CORE1_STAT		R5SS0 Core 1 Idle Status register	This register shows the WFI WFE status of R5SS0 Core 1
0x038	MSS_STC_CONTROL0	R5SS0_FORCE_WFI	R5SS0 Force WFI register	This register is used to override and force WFI from R5SS0 to RCM
0x040	R5SS1_CONTROL		R5SS1 Lock Step configure register	This register is used to configure R5SS1 in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle
0x044	R5SS1_COREA_HALT	R5SS1_CORE0_HALT	R5SS1 Core 0 Halt Register	This register is used to Halt or Unhalt R5SS1 Core 0
0x048	R5SS1_COREB_HALT	R5SS1_CORE1_HALT	R5SS1 Core 1 Halt Register	This register is used to Halt or Unhalt R5SS1 Core 1
0x04C	R5SS1_STATUS_REG		R5SS1 Lock step Status register	This register shows whether R5SS1 is in Lock step or Dual core mode
0x050	R5SS1_CORE0_STAT		R5SS1 Core 0 Idle Status register	This register shows the WFI WFE status of R5SS1 Core 0
0x054	R5SS1_CORE1_STAT		R5SS1 Core 1 Idle Status register	This register shows the WFI WFE status of R5SS1 Core 1
0x058	MSS_STC_CONTROL1	R5SS1_FORCE_WFI	R5SS1 Force WFI register	This register is used to override and force WFI from R5SS1 to RCM
0x090	R5SS[0]_GLOBAL_CONFIG	R5SS[0]_TEINIT	R5SS[0] Default exception state Register	This register is used to set the Exception state of R5SS[0] at reset
0x200	MSS_ATCM0_MEM_INIT	R5SS0_ATCM_MEM_INIT	R5SS0 ATCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of ATCM memory of R5SS0
0x204	MSS_ATCM0_MEM_INIT_DONE	R5SS0_ATCM_MEM_INIT_DONE	R5SS0 ATCM Memory Initialisation Completion Register	This register is used to indicate the ATCM memory initialisation completion for R5SS0
0x208	MSS_ATCM0_MEM_INIT_STATUS	R5SS0_ATCM_MEM_INIT_STATUS	R5SS0 ATCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for ATCM memory of R5SS0
0x210	MSS_BTCM0_MEM_INIT	R5SS0_BTCM_MEM_INIT	R5SS0 BTCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of BTCM memory of R5SS0
0x214	MSS_BTCM0_MEM_INIT_DONE	R5SS0_BTCM_MEM_INIT_DONE	R5SS0 BTCM Memory Initialisation Completion Register	This register is used to indicate the BTCM memory initialisation completion for R5SS0
0x218	MSS_BTCM0_MEM_INIT_STATUS	R5SS0_BTCM_MEM_INIT_STATUS	R5SS0 BTCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for BTCM memory of R5SS0
0x220	MSS_ATCM1_MEM_INIT	R5SS1_ATCM_MEM_INIT	R5SS1 ATCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of ATCM memory of R5SS1
0x224	MSS_ATCM1_MEM_INIT_DONE	R5SS1_ATCM_MEM_INIT_DONE	R5SS1 ATCM Memory Initialisation Completion Register	This register is used to indicate the ATCM memory initialisation completion for R5SS1
0x228	MSS_ATCM1_MEM_INIT_STATUS	R5SS1_ATCM_MEM_INIT_STATUS	R5SS1 ATCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for ATCM memory of R5SS1

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x230	MSS_BTCM1_MEM_INIT	R5SS1_BTCM_MEM_INIT	R5SS1 BTCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of BTCM memory of R5SS1
0x234	MSS_BTCM1_MEM_INIT_DONE	R5SS1_BTCM_MEM_INIT_DONE	R5SS1 BTCM Memory Initialisation Completion Register	This register is used to indicate the BTCM memory initialisation completion for R5SS1
0x238	MSS_BTCM1_MEM_INIT_STATUS	R5SS1_BTCM_MEM_INIT_STATUS	R5SS1 BTCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for BTCM memory of R5SS1
0x240	MSS_L2_MEM_INIT	L2IOCRAM_MEM_INIT	L2OCRAM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of L2OCRAM
0x244	MSS_L2_MEM_INIT_DONE	L2OCRAM_MEM_INIT_DONE	L2OCRAM Memory Initialisation Completion Register	This register is used to indicate the L2OCRAM memory initialisation completion
0x248	MSS_L2_MEM_INIT_STATUS	L2OCRAM_MEM_INIT_STATUS	L2OCRAM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for L2OCRAM
0x250	MSS_MAILBOX_MEM_INIT	MAILBOXRAM_MEM_INIT	MBOX_SRAM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of MBOX_SRAM
0x254	MSS_MAILBOX_MEM_INIT_DONE	MAILBOXRAM_MEM_INIT_DONE	MBOX_SRAM Memory Initialisation Completion Register	This register is used to indicate the MBOX_SRAM memory initialisation completion
0x258	MSS_MAILBOX_MEM_INIT_STATUS	MAILBOXRAM_MEM_INIT_STATUS	MBOX_SRAM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for MBOX_SRAM
0x260	MSS_TPCC_MEMINIT_START	TPCC_MEM_INIT	EDMA_TPCC Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of EDMA_TPCC RAM
0x264	MSS_TPCC_MEMINIT_DONE	TPCC_MEM_INIT_DONE	EDMA_TPCC Memory Initialisation Completion Register	This register is used to indicate the EDMA_TPCC memory initialisation completion
0x268	MSS_TPCC_MEMINIT_STATUS	TPCC_MEMINIT_STATUS	EDMA_TPCC Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for EDMA_TPCC RAM
0x300	MSS_PBIST_KEY_RST	TOP_PBIST_KEY_RST	TOP Pbist Enable Register	This register is used to enable Top Pbist module
0x400	MSS_R5SS[0]_CTI_TRIG_SEL	R5SS[0]_CTI_TRIG_SEL	R5SS[0] CTI Trigger Selection Register	This register is used to select the two CTI trigger sources for R5SS[0]
0x408	MSS_DBGSS_CTI_TRIG_SEL	DBGSS_CTI_TRIG_SEL	DBGSS CTI Trigger Selection Register	This register is used to select thefour CTI trigger sources for DEBUGSS
0x40C	DEBUGSS_CSETB_FLUSH		ETB Control and Status Register	This register is used to generte the ETB flush request and indicate the ETB status
0x410	DEBUGSS_STM_NSGUAREN		STM Non Secure Gaurenteted Access Register	This register controls the behaviour of STM for Non secure guarenteed AXI access
0x420	CAN[0]_HALTEN	MCAN[0]_HALTEN	CAN[0] Halt Control Register	This register selects which R5 CPU when debug halted shall halt MCAN[0] Peripheral
0x430	LIN[0]_HALTEN		LIN[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt LIN[0] Peripheral
0x444	I2C[0]_HALTEN		I2C[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt I2C[0] Peripheral
0x454	RTI[0]_HALTEN		RTI[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt RTI[0] Peripheral
0x474	CPSW_HALTEN		CPSW_HALTEN	This register selects which R5 CPU when debug halted shall halt CPSW Peripheral
0x478	CRC_HALTEN	MCRC0_HALTEN	CRC_HALTEN	This register selects which R5 CPU when debug halted shall halt MCRC Peripheral

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x800	TPTC_DBS_CONFIG		EDMA TCTC Default Burst size configuration Register	This register controls the default burst size of EDMA TPTC
0x810	CPSW_CONTROL		CPSW Mode Register	This register is used to control the CPSW Ethernet modes and additional controls on the IO
0x818	GLOBAL_CONTROLS	ICSSM_IDLE_CONTROL	ICSSM Idle Config Register	This register cofigures the Idle mode behaviour of ICSSM
0x81C	ICSSM_PRU0_GPI_SEL		PRU0 GPI SEL	Selects b/w Chip input or Control peripheral for ICSSM PRU0 GPI source
0x820	ICSSM_PRU1_GPI_SEL		PRU1 GPI SEL	Selects b/w Chip input or Control peripheral for ICSSM PRU1 GPI source
0x824	ICSSM_PRU0_GPIO_OUT_CTRL		ICSSM_PRU0_GPIO_OUT_CTRL	Controls the Output enable of the ICSSM PRU0 GPIO pins
0x828	ICSSM_PRU1_GPIO_OUT_CTRL		ICSSM_PRU1_GPIO_OUT_CTRL	Controls the Output enable of the ICSSM PRU1 GPIO pins
0x82C	GPMC_CONTROL		GPMC Clock Configuration Register	This register is used to configure the GPMC Clock source and Loop Back clock Source
0x830	MSS_TPCC_A_INTAGG_MASK	TPCC0_INTAGG_MASK	TPCC0 Aggregated Interrupt Mask Register	This register Masks selected interrupt soures from the Aggregated TPCC0 interrupt
0x834	MSS_TPCC_A_INTAGG_STATUS	TPCC0_INTAGG_STATUS	TPCC0 Aggregated Interrupt Status Register	This register shows the Status of Unmasked Interrupts from TPCC0
0x838	MSS_TPCC_A_INTAGG_STATUS_RAW	TPCC0_INTAGG_STATUS_RAW	TPCC0 Aggregated Interrupt Raw Status Register	This register shows the Status of all Interrupts from TPCC0
0x0	MSS_CR5A0_MBOX_WRITE_DONE	R5SS0_CORE0_MBOX_WRITE_DONE	R5SS0 CORE0 Mailbox Write Done Register	This register is used by R5SS0 Core 0 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5A0_MBOX_READ_REQ	R5SS0_CORE0_MBOX_READ_REQ	R5SS0 CORE0 Mailbox Read Request Register	This register is used by R5SS0 Core 0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5A0_MBOX_READ_DONE_ACK	R5SS0_CORE0_MBOX_READ_DONE_ACK	R5SS0 CORE0 Mailbox Read Acknowledge Register	This register is used by R5SS0 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5A0_MBOX_READ_DONE	R5SS0_CORE0_MBOX_READ_DONE	R5SS0 CORE0 Mailbox Read Completed Register	This register is used by R5SS0 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS0_CORE0	R5SS0_CORE0_SW_INT	R5SS0 CORE0 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core0
0x20	MPU_ADDR_INTR_ERRAGG0_MASK	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK	MPU Aggregated Addr Error to R5SS0 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS0 CORE0
0x24	MPU_ADDR_INTR_ERRAGG0_STATUS	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS	MPU Aggregated Addr Error to R5SS0 CORE0 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS0 Core0
0x28	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW	MPU Aggregated Addr Error to R5SS0 CORE0 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG0_MASK	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK	MPU Aggregated Prot Error to R5SS0 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS0 CORE0
0x34	MPU_PROT_INTR_ERRAGG0_STATUS	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS	MPU Aggregated Prot Error to R5SS0 CORE0 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS0 Core0

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x38	MPU_PROT_INTR_ERRAGG0_STATUS_RAW	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW	MPU Aggregated Prot Error to R5SS0 CORE0 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	MSS_CR5B0_MBOX_WRITE_DONE	R5SS0_CORE1_MBOX_WRITE_DONE	R5SS0 CORE1 Mailbox Write Done Register	This register is used by R5SS0 Core 1 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5B0_MBOX_READ_REQ	R5SS0_CORE1_MBOX_READ_REQ	R5SS0 CORE1 Mailbox Read Request Register	This register is used by R5SS0 Core 1 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5B0_MBOX_READ_DONE_ACK	R5SS0_CORE1_MBOX_READ_DONE_ACK	R5SS0 CORE1 Mailbox Read Acknowledge Register	This register is used by R5SS0 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5B0_MBOX_READ_DONE	R5SS0_CORE1_MBOX_READ_DONE	R5SS0 CORE1 Mailbox Read Completed Register	This register is used by R5SS0 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS0_CORE1	R5SS0_CORE1_SW_INT	R5SS0 CORE1 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core1
0x20	MPU_ADDR_INTR_ERRAGG1_MASK	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK	MPU Aggregated Addr Error to R5SS0 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS0 CORE1
0x24	MPU_ADDR_INTR_ERRAGG1_STATUS	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS	MPU Aggregated Addr Error to R5SS0 CORE1 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS0 CORE1
0x28	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW	MPU Aggregated Addr Error to R5SS0 CORE1 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG1_MASK	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK	MPU Aggregated Prot Error to R5SS0 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS0 CORE1
0x34	MPU_PROT_INTR_ERRAGG1_STATUS	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS	MPU Aggregated Prot Error to R5SS0 CORE1 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS0 CORE1
0x38	MPU_PROT_INTR_ERRAGG1_STATUS_RAW	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW	MPU Aggregated Prot Error to R5SS0 CORE1 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	MSS_CR5A1_MBOX_WRITE_DONE	R5SS1_CORE0_MBOX_WRITE_DONE	R5SS1 CORE0 Mailbox Write Done Register	This register is used by R5SS1 Core 0 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5A1_MBOX_READ_REQ	R5SS1_CORE0_MBOX_READ_REQ	R5SS1 CORE0 Mailbox Read Request Register	This register is used by R5SS1 Core 0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5A1_MBOX_READ_DONE_ACK	R5SS1_CORE0_MBOX_READ_DONE_ACK	R5SS1 CORE0 Mailbox Read Acknowledge Register	This register is used by R5SS1 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5A1_MBOX_READ_DONE	R5SS1_CORE0_MBOX_READ_DONE	R5SS1 CORE0 Mailbox Read Completed Register	This register is used by R5SS1 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS1_CORE0	R5SS1_CORE0_SW_INT	R5SS1 CORE0 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core0
0x20	MPU_ADDR_INTR_ERRAGG2_MASK	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK	MPU Aggregated Addr Error to R5SS1 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS1 CORE0
0x24	MPU_ADDR_INTR_ERRAGG2_STATUS	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS	MPU Aggregated Addr Error to R5SS1 CORE0 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS1 Core0

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x28	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW	MPU Aggregated Addr Error to R5SS1 CORE0 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG2_MASK	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK	MPU Aggregated Prot Error to R5SS1 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS1 CORE0
0x34	MPU_PROT_INTR_ERRAGG2_STATUS	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS	MPU Aggregated Prot Error to R5SS1 CORE0 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS1 Core0
0x38	MPU_PROT_INTR_ERRAGG2_STATUS_RAW	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW	MPU Aggregated Prot Error to R5SS1 CORE0 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	MSS_CR5B1_MBOX_WRITE_DONE	R5SS1_CORE1_MBOX_WRITE_DONE	R5SS1 CORE1 Mailbox Write Done Register	This register is used by R5SS1 Core 1 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5B1_MBOX_READ_REQ	R5SS1_CORE1_MBOX_READ_REQ	R5SS1 CORE1 Mailbox Read Request Register	This register is used by R5SS1 Core 1 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5B1_MBOX_READ_DONE_ACK	R5SS1_CORE1_MBOX_READ_DONE_ACK	R5SS1 CORE1 Mailbox Read Acknowledge Register	This register is used by R5SS1 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5B1_MBOX_READ_DONE	R5SS1_CORE1_MBOX_READ_DONE	R5SS1 CORE1 Mailbox Read Completed Register	This register is used by R5SS1 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS1_CORE1	R5SS1_CORE1_SW_INT	R5SS1 CORE1 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core1
0x20	MPU_ADDR_INTR_ERRAGG3_MASK	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK	MPU Aggregated Addr Error to R5SS1 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS1 CORE1
0x24	MPU_ADDR_INTR_ERRAGG3_STATUS	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS	MPU Aggregated Addr Error to R5SS1 CORE1 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS1 CORE1
0x28	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW	MPU Aggregated Addr Error to R5SS1 CORE1 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG3_MASK	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK	MPU Aggregated Prot Error to R5SS1 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS1 CORE1
0x34	MPU_PROT_INTR_ERRAGG3_STATUS	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS	MPU Aggregated Prot Error to R5SS1 CORE1 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS1 CORE1
0x38	MPU_PROT_INTR_ERRAGG3_STATUS_RAW	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW	MPU Aggregated Prot Error to R5SS1 CORE1 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	ICSSM_PRU0_MBOX_WRITE_DONE	ICSSM_PRU0_MBOX_WRITE_DONE	ICSSM PRU0 Mailbox Write Done Register	This register is used by ICSSM PRU0 to generate Mailbox interrupt to Recipent CPU
0x04	ICSSM_PRU0_MBOX_READ_REQ	ICSSM_PRU0_MBOX_READ_REQ	ICSSM PRU0 Mailbox Read Request Register	This register is used by ICSSM PRU0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	ICSSM_PRU0_MBOX_READ_DONE_ACK	ICSSM_PRU0_MBOX_READ_DONE_ACK	ICSSM PRU0 Mailbox Read Acknowledge Register	This register is used by ICSSM PRU0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	ICSSM_PRU0_MBOX_READ_DONE	ICSSM_PRU0_MBOX_READ_DONE	ICSSM PRU0 Mailbox Read Completed Register	This register is used by ICSSM PRU0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x10	ICSSM_PRU1_MBOX_WRITE_DONE	ICSSM_PRU1_MBOX_WRITE_DONE	ICSSM PRU1 Mailbox Write Done Register	This register is used by ICSSM PRU1 to generate Mailbox interrupt to Recipent CPU
0x14	ICSSM_PRU1_MBOX_READ_REQ	ICSSM_PRU1_MBOX_READ_REQ	ICSSM PRU1 Mailbox Read Request Register	This register is used by ICSSM PRU1 to know the Sender of Mailbox Interrupt as well as clear it
0x18	ICSSM_PRU1_MBOX_READ_DONE_ACK	ICSSM_PRU1_MBOX_READ_DONE_ACK	ICSSM PRU1 Mailbox Read Acknowledge Register	This register is used by ICSSM PRU1 to generate Mailbox Read acknowledgement to the Sender CPU
0x1C	ICSSM_PRU1_MBOX_READ_DONE	ICSSM_PRU1_MBOX_READ_DONE	ICSSM PRU1 Mailbox Read Completed Register	This register is used by ICSSM PRU1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x0	MSS_TPCC_A_ERRAGG_MASK	TPCC0_ERRAGG_MASK	TPCC0 Aggregated Error Mask Register	This register Masks selected interrupt soures from generating the Aggregated TPCC0 Error Interrupt
0x04	MSS_TPCC_A_ERRAGG_STATUS	TPCC0_ERRAGG_STATUS	TPCC0 Aggregated Error Status Register	This register shows the Status of Unmasked Errors from TPCC0
0x08	MSS_TPCC_A_ERRAGG_STATUS_RAW	TPCC0_ERRAGG_STATUS_RAW	TPCC0 Aggregated Error Raw Status Register	This register shows the Status of all Errors from TPCC0
0x10	MSS_PERIPH_ERRAGG_MASK0	MMR_ACCESS_ERRAGG_MASK	Aggregated MMR Access Error Mask Register	This register Masks selected interrupt soures from generating the Aggregated MMR Access Error Interrupt
0x14	MSS_PERIPH_ERRAGG_STATUS0	MMR_ACCESS_ERRAGG_STATUS	Aggregated MMR Access Error Status Register	This register shows the Status of Unmasked MMR Access Errors
0x18	MSS_PERIPH_ERRAGG_STATUS_RAW0	MMR_ACCESS_ERRAGG_STATUS_RAW	Aggregated MMR Access Error Raw Status Register	This register shows the Status of all MMR Access Errors
0x80	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK	R5SS0_CORE0_ECC_CORR_ERRAGG_MASK	R5SS0 CORE0 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS0 CORE0 Memories
0x84	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS	R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS	R5SS0 CORE0 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS0 CORE0 Memories
0x88	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0 CORE0 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS0 CORE0 Memories
0x90	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK	R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK	R5SS0 CORE0 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS0 CORE0 Memories
0x94	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS	R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS	R5SS0 CORE0 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS0 CORE0 Memories
0x98	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0 CORE0 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS0 CORE0 Memories
0xA0	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK	R5SS0_CORE1_ECC_CORR_ERRAGG_MASK	R5SS0 CORE1 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS0 CORE1 Memories
0xA4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS	R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS	R5SS0 CORE1 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS0 CORE1 Memories

Address Offset	ShortName	Alternate Software Name	LongName	Description
0xA8	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0 CORE1 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS0 CORE1 Memories
0xB0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK	R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK	R5SS0 CORE1 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS0 CORE1 Memories
0xB4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS	R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS	R5SS0 CORE1 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS0 CORE1 Memories
0xB8	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0 CORE1 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS0 CORE1 Memories
0xC0	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK	R5SS1_CORE0_ECC_CORR_ERRAGG_MASK	R5SS1 CORE0 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS1 CORE0 Memories
0xC4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS	R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS	R5SS1 CORE0 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS1 CORE0 Memories
0xC8	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1 CORE0 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS1 CORE0 Memories
0xD0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK	R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK	R5SS1 CORE0 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS1 CORE0 Memories
0xD4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS	R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS	R5SS1 CORE0 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS1 CORE0 Memories
0xD8	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1 CORE0 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS1 CORE0 Memories
0xE0	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK	R5SS1_CORE1_ECC_CORR_ERRAGG_MASK	R5SS1 CORE1 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS1 CORE1 Memories
0xE4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS	R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS	R5SS1 CORE1 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS1 CORE1 Memories
0xE8	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1 CORE1 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS1 CORE1 Memories
0xF0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK	R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK	R5SS1 CORE1 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS1 CORE1 Memories
0xF4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS	R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS	R5SS1 CORE1 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS1 CORE1 Memories

Address Offset	ShortName	Alternate Software Name	LongName	Description
0xF8	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1 CORE1 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS1 CORE1 Memories
0x100	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0 CORE0 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS0 CORE0
0x104	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0 CORE0 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS0 CORE0
0x108	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0 CORE0 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS0 CORE0
0x110	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0 CORE1 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS0 CORE1
0x114	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0 CORE1 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS0 CORE1
0x118	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0 CORE1 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS0 CORE1
0x120	TCM0_PARITY_CTRL	R5SS0_TCM_ADDRPARITY_CLR	R5SS0 TCM Address Parity Error Clear Register	This register clears the TCM Address Parity Errors of R5SS0
0x124	ERR_PARITY_ATCM0_R5SS0	R5SS0_CORE0_ADDRPARITY_ERR_ATCM	R5SS0 CORE0 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x128	ERR_PARITY_ATCM1_R5SS0	R5SS0_CORE1_ADDRPARITY_ERR_ATCM	R5SS0 CORE1 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x12C	ERR_PARITY_B0TCM0_R5SS0	R5SS0_CORE0_ERR_ADDRPARITY_B0TCM	R5SS0 CORE0 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x130	ERR_PARITY_B0TCM1_R5SS0	R5SS0_CORE1_ERR_ADDRPARITY_B0TCM	R5SS0 CORE1 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x134	ERR_PARITY_B1TCM0_R5SS0	R5SS0_CORE0_ERR_ADDRPARITY_B1TCM	R5SS0 CORE0 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x138	ERR_PARITY_B1TCM1_R5SS0	R5SS0_CORE1_ERR_ADDRPARITY_B1TCM	R5SS0 CORE1 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x13C	TCM0_PARITY_ERRFRC	R5SS0_TCM_ADDRPARITY_ERRFORCE	R5SS0 TCM Address Parity Error Force Register	This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS0
0x140	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1 CORE0 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS1 CORE0
0x144	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1 CORE0 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS1 CORE0

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x148	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1 CORE0 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS1 CORE0
0x150	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1 CORE1 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS1 CORE1
0x154	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1 CORE1 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS1 CORE1
0x158	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1 CORE1 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS1 CORE1
0x160	TCM1_PARITY_CTRL	R5SS1_TCM_ADDRPARITY_CLR	R5SS1 TCM Address Parity Error Clear Register	This register clears the TCM Address Parity Errors of R5SS1
0x164	ERR_PARITY_ATCM0_R5SS1	R5SS1_CORE0_ADDRPARITY_ERR_ATCM	R5SS1 CORE0 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x168	ERR_PARITY_ATCM1_R5SS1	R5SS1_CORE1_ADDRPARITY_ERR_ATCM	R5SS1 CORE1 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x16C	ERR_PARITY_B0TCM0_R5SS1	R5SS1_CORE0_ERR_ADDRPARITY_B0TCM	R5SS1 CORE0 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x170	ERR_PARITY_B0TCM1_R5SS1	R5SS1_CORE1_ERR_ADDRPARITY_B0TCM	R5SS1 CORE1 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x174	ERR_PARITY_B1TCM0_R5SS1	R5SS1_CORE0_ERR_ADDRPARITY_B1TCM	R5SS1 CORE0 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x178	ERR_PARITY_B1TCM1_R5SS1	R5SS1_CORE1_ERR_ADDRPARITY_B1TCM	R5SS1 CORE1 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x17C	TCM1_PARITY_ERRFRC	R5SS1_TCM_ADDRPARITY_ERRFORCE	R5SS1 TCM Address Parity Error Force Register	This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS1
0x180	TPCC_PARITY_CTRL	TPCC0_PARITY_CTRL	EDMA TPCC0 Memory Parity Error Control Register	This register Controls the Parity Error detection logic of EDMA TPCC0 Memories
0x184	TPCC_PARITY_STATUS	TPCC0_PARITY_STATUS	EDMA TPCC0 Memory Parity Error Status Register	This register indicates the Address where the Parity Error occurred in TPCC0 Memory
0x200	MSS_BUS_SAFETY_CTRL	BUS_SAFETY_CTRL	Interconnect Safety Enable Register	This register is used to Globally enable Interconnect Safety
0x220	MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI RD Initiator Port
0x224	MSS_CR5A0_AXI_RD_BUS_SAFETY_FI	R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI	R5SS0 CORE0 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI RD Initiator Port
0x228	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator port
0x22C	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port

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0x230	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port
0x234	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE0 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port
0x240	MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI RD Initiator Port
0x244	MSS_CR5B0_AXI_RD_BUS_SAFETY_FI	R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI	R5SS0 CORE1 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI RD Initiator Port
0x248	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator port
0x24C	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x250	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x254	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE1 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x260	MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI RD Initiator Port
0x264	MSS_CR5A1_AXI_RD_BUS_SAFETY_FI	R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI	R5SS1 CORE0 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI RD Initiator Port
0x268	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator port
0x26C	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x270	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x274	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE0 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x280	MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI RD Initiator Port
0x284	MSS_CR5B1_AXI_RD_BUS_SAFETY_FI	R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI	R5SS1 CORE1 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI RD Initiator Port
0x288	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x28C	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port
0x290	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port
0x294	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE1 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port
0x2A0	MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI WR Initiator Port
0x2A4	MSS_CR5A0_AXI_WR_BUS_SAFETY_FI	R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI	R5SS0 CORE0 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2A8	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator port
0x2AC	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B0	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B4	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE0 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B8	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE0 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2C0	MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI WR Initiator Port
0x2C4	MSS_CR5B0_AXI_WR_BUS_SAFETY_FI	R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI	R5SS0 CORE1 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2C8	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator port
0x2CC	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2D0	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2D4	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE1 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x2D8	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE1 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2E0	MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI WR Initiator Port
0x2E4	MSS_CR5A1_AXI_WR_BUS_SAFETY_FI	R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI	R5SS1 CORE0 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2E8	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator port
0x2EC	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F0	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F4	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE0 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F8	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE0 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x300	MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI WR Initiator Port
0x304	MSS_CR5B1_AXI_WR_BUS_SAFETY_FI	R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI	R5SS1 CORE1 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI WR Initiator Port
0x308	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator port
0x30C	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x310	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x314	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE1 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x318	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE1 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x320	MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x324	MSS_CR5A0_AXI_S_BUS_SAFETY_FI	R5SS0_CORE0_AXI_S_BUS_SAFETY_FI	R5SS0 CORE0 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI Target Port
0x328	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x32C	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x330	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x334	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE0 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x338	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE0 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x33C	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE0 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x340	MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI Target Port
0x344	MSS_CR5B0_AXI_S_BUS_SAFETY_FI	R5SS0_CORE1_AXI_S_BUS_SAFETY_FI	R5SS0 CORE1 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI Target Port
0x348	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x34C	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x350	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x354	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE1 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x358	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE1 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x35C	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE1 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x360	MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x364	MSS_CR5A1_AXI_S_BUS_SAFETY_FI	R5SS1_CORE0_AXI_S_BUS_SAFETY_FI	R5SS1 CORE0 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI Target Port
0x368	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x36C	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x370	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x374	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE0 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x378	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE0 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x37C	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE0 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x380	MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI Target Port
0x384	MSS_CR5B1_AXI_S_BUS_SAFETY_FI	R5SS1_CORE1_AXI_S_BUS_SAFETY_FI	R5SS1 CORE1 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI Target Port
0x388	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x38C	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x390	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x394	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE1 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x398	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE1 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x39C	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE1 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x3A0	MSS_TPTC_A0_RD_BUS_SAFETY_CTRL	TPTC00_RD_BUS_SAFETY_CTRL	TPTC00_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00_RD Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x3A4	MSS_TPTC_A0_RD_BUS_SAFETY_FI	TPTC00_RD_BUS_SAFETY_FI	TPTC00_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC00_RD Initiator Port
0x3A8	MSS_TPTC_A0_RD_BUS_SAFETY_ERR	TPTC00_RD_BUS_SAFETY_ERR	TPTC00_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC00_RD Initiator Port
0x3AC	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00_RD Initiator Port
0x3B0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC00_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00_RD Initiator Port
0x3B4	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ	TPTC00_RD_BUS_SAFETY_ERR_STAT_READ	TPTC00_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC00_RD Initiator Port
0x3C0	MSS_TPTC_A1_RD_BUS_SAFETY_CTRL	TPTC01_RD_BUS_SAFETY_CTRL	TPTC01_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01_RD Initiator Port
0x3C4	MSS_TPTC_A1_RD_BUS_SAFETY_FI	TPTC01_RD_BUS_SAFETY_FI	TPTC01_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC01_RD Initiator Port
0x3C8	MSS_TPTC_A1_RD_BUS_SAFETY_ERR	TPTC01_RD_BUS_SAFETY_ERR	TPTC01_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC01_RD Initiator Port
0x3CC	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3D0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC01_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3D4	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ	TPTC01_RD_BUS_SAFETY_ERR_STAT_READ	TPTC01_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3E0	MSS_TPTC_A0_WR_BUS_SAFETY_CTRL	TPTC00_WR_BUS_SAFETY_CTRL	TPTC00_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00_WR Initiator Port
0x3E4	MSS_TPTC_A0_WR_BUS_SAFETY_FI	TPTC00_WR_BUS_SAFETY_FI	TPTC00_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC00_WR Initiator Port
0x3E8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR	TPTC00_WR_BUS_SAFETY_ERR	TPTC00_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC00_WR Initiator Port
0x3EC	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x3F0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC00_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x3F4	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC00_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC00_WR Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x3F8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC00_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x400	MSS_TPTC_A1_WR_BUS_SAFETY_CTRL	TPTC01_WR_BUS_SAFETY_CTRL	TPTC01_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01_WR Initiator Port
0x404	MSS_TPTC_A1_WR_BUS_SAFETY_FI	TPTC01_WR_BUS_SAFETY_FI	TPTC01_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC01_WR Initiator Port
0x408	MSS_TPTC_A1_WR_BUS_SAFETY_ERR	TPTC01_WR_BUS_SAFETY_ERR	TPTC01_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC01_WR Initiator Port
0x40C	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x410	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC01_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x414	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC01_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x418	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC01_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x420	HSM_TPTC_A0_RD_BUS_SAFETY_CTRL	HSM_TPTC0_RD_BUS_SAFETY_CTRL	HSM_TPTC0_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC0_RD Initiator Port
0x424	HSM_TPTC_A0_RD_BUS_SAFETY_FI	HSM_TPTC0_RD_BUS_SAFETY_FI	HSM_TPTC0_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC0_RD Initiator Port
0x428	HSM_TPTC_A0_RD_BUS_SAFETY_ERR	HSM_TPTC0_RD_BUS_SAFETY_ERR	HSM_TPTC0_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x42C	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x430	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x434	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC0_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x440	HSM_TPTC_A1_RD_BUS_SAFETY_CTRL	HSM_TPTC1_RD_BUS_SAFETY_CTRL	HSM_TPTC1_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC1_RD Initiator Port
0x444	HSM_TPTC_A1_RD_BUS_SAFETY_FI	HSM_TPTC1_RD_BUS_SAFETY_FI	HSM_TPTC1_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC1_RD Initiator Port
0x448	HSM_TPTC_A1_RD_BUS_SAFETY_ERR	HSM_TPTC1_RD_BUS_SAFETY_ERR	HSM_TPTC1_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC1_RD Initiator Port

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0x44C	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x450	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x454	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC1_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x460	HSM_TPTC_A0_WR_BUS_SAFETY_CTRL	HSM_TPTC0_WR_BUS_SAFETY_CTRL	HSM_TPTC0_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC0_WR Initiator Port
0x464	HSM_TPTC_A0_WR_BUS_SAFETY_FI	HSM_TPTC0_WR_BUS_SAFETY_FI	HSM_TPTC0_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC0_WR Initiator Port
0x468	HSM_TPTC_A0_WR_BUS_SAFETY_ERR	HSM_TPTC0_WR_BUS_SAFETY_ERR	HSM_TPTC0_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x46C	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x470	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x474	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC0_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x478	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC0_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x480	HSM_TPTC_A1_WR_BUS_SAFETY_CTRL	HSM_TPTC1_WR_BUS_SAFETY_CTRL	HSM_TPTC1_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC1_WR Initiator Port
0x484	HSM_TPTC_A1_WR_BUS_SAFETY_FI	HSM_TPTC1_WR_BUS_SAFETY_FI	HSM_TPTC1_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC1_WR Initiator Port
0x488	HSM_TPTC_A1_WR_BUS_SAFETY_ERR	HSM_TPTC1_WR_BUS_SAFETY_ERR	HSM_TPTC1_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x48C	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x490	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x494	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC1_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x498	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC1_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x4A0	MSS_QSPI_BUS_SAFETY_CTRL	QSPI0_BUS_SAFETY_CTRL	QSPI Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of QSPI Target Port
0x4A4	MSS_QSPI_BUS_SAFETY_FI	QSPI0_BUS_SAFETY_FI	QSPI Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of QSPI Target Port
0x4A8	MSS_QSPI_BUS_SAFETY_ERR	QSPI0_BUS_SAFETY_ERR	QSPI Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of QSPI Target Port
0x4AC	MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0	QSPI0_BUS_SAFETY_ERR_STAT_DATA0	QSPI Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of QSPI Target Port
0x4B0	MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD	QSPI0_BUS_SAFETY_ERR_STAT_CMD	QSPI Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of QSPI Target Port
0x4B4	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE	QSPI0_BUS_SAFETY_ERR_STAT_WRITE	QSPI Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of QSPI Target Port
0x4B8	MSS_QSPI_BUS_SAFETY_ERR_STAT_READ	QSPI0_BUS_SAFETY_ERR_STAT_READ	QSPI Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of QSPI Target Port
0x4BC	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP	QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP	QSPI Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of QSPI Target Port
0x4C0	HSM_DTHE_BUS_SAFETY_CTRL		HSM_DTHE Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_DTHE Target Port
0x4C4	HSM_DTHE_BUS_SAFETY_FI		HSM_DTHE Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_DTHE Target Port
0x4C8	HSM_DTHE_BUS_SAFETY_ERR		HSM_DTHE Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_DTHE Target Port
0x4CC	HSM_DTHE_BUS_SAFETY_ERR_STAT_DATA0		HSM_DTHE Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D0	HSM_DTHE_BUS_SAFETY_ERR_STAT_CMD		HSM_DTHE Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D4	HSM_DTHE_BUS_SAFETY_ERR_STAT_WRITE		HSM_DTHE Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D8	HSM_DTHE_BUS_SAFETY_ERR_STAT_READ		HSM_DTHE Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4DC	HSM_DTHE_BUS_SAFETY_ERR_STAT_WRITERESP		HSM_DTHE Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4E0	MSS_CPSW_BUS_SAFETY_CTRL		CPSW Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of CPSW Initiator Port
0x4E4	MSS_CPSW_BUS_SAFETY_FI		CPSW Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of CPSW Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x4E8	MSS_CPSW_BUS_SAFETY_ERR		CPSW Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of CPSW Initiator Port
0x4EC	MSS_CPSW_BUS_SAFETY_ERR_STAT_DATA0		CPSW Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of CPSW Initiator Port
0x4F0	MSS_CPSW_BUS_SAFETY_ERR_STAT_CMD		CPSW Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of CPSW Initiator Port
0x4F4	MSS_CPSW_BUS_SAFETY_ERR_STAT_WRITE		CPSW Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of CPSW Initiator Port
0x4F8	MSS_CPSW_BUS_SAFETY_ERR_STAT_READ		CPSW Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of CPSW Initiator Port
0x4FC	MSS_CPSW_BUS_SAFETY_ERR_STAT_WRITERESP		CPSW Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of CPSW Initiator Port
0x500	ICSSM_PDSP0_BUS_SAFETY_CTRL		ICSSM_PDSP0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM_PDSP0 Initiator Port
0x504	ICSSM_PDSP0_BUS_SAFETY_FI		ICSSM_PDSP0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM_PDSP0 Initiator Port
0x508	ICSSM_PDSP0_BUS_SAFETY_ERR		ICSSM_PDSP0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x50C	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_DATA0		ICSSM_PDSP0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x510	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_CMD		ICSSM_PDSP0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x514	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_WRITE		ICSSM_PDSP0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x518	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_READ		ICSSM_PDSP0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x51C	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_WRITERESP		ICSSM_PDSP0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x520	ICSSM_PDSP1_BUS_SAFETY_CTRL		ICSSM_PDSP1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM_PDSP1 Initiator Port
0x524	ICSSM_PDSP1_BUS_SAFETY_FI		ICSSM_PDSP1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM_PDSP1 Initiator Port
0x528	ICSSM_PDSP1_BUS_SAFETY_ERR		ICSSM_PDSP1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM_PDSP1 Initiator Port

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0x52C	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_DATA0		ICSSM_PDSP1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x530	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_CMD		ICSSM_PDSP1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x534	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_WRITE		ICSSM_PDSP1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x538	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_READ		ICSSM_PDSP1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x53C	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_WRITERESP		ICSSM_PDSP1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x540	MSS_MCRC_BUS_SAFETY_CTRL	MCRC0_BUS_SAFETY_CTRL	MCRC Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MCRC Target Port
0x544	MSS_MCRC_BUS_SAFETY_FI	MCRC0_BUS_SAFETY_FI	MCRC Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MCRC Target Port
0x548	MSS_MCRC_BUS_SAFETY_ERR	MCRC0_BUS_SAFETY_ERR	MCRC Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MCRC Target Port
0x54C	MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0	MCRC0_BUS_SAFETY_ERR_STAT_DATA0	MCRC Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MCRC Target Port
0x550	MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD	MCRC0_BUS_SAFETY_ERR_STAT_CMD	MCRC Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MCRC Target Port
0x554	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE	MCRC0_BUS_SAFETY_ERR_STAT_WRITE	MCRC Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MCRC Target Port
0x558	MSS_MCRC_BUS_SAFETY_ERR_STAT_READ	MCRC0_BUS_SAFETY_ERR_STAT_READ	MCRC Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MCRC Target Port
0x55C	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP	MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP	MCRC Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MCRC Target Port
0x560	SCRM2SCRP_0_BUS_SAFETY_CTRL		M2P0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of M2P0 Bridge Target Port
0x564	SCRM2SCRP_0_BUS_SAFETY_FI		M2P0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of M2P0 Bridge Target Port
0x568	SCRM2SCRP_0_BUS_SAFETY_ERR		M2P0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of M2P0 Bridge Target Port
0x56C	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_DATA0		M2P0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of M2P0 Bridge Target Port

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0x570	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_CMD		M2P0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x574	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_WRITE		M2P0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x578	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_READ		M2P0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x57C	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_WRITERESP		M2P0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x580	SCRM2SCRP_1_BUS_SAFETY_CTRL		M2P1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of M2P1 Bridge Target Port
0x584	SCRM2SCRP_1_BUS_SAFETY_FI		M2P1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of M2P1 Bridge Target Port
0x588	SCRM2SCRP_1_BUS_SAFETY_ERR		M2P1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of M2P1 Bridge Target Port
0x58C	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_DATA0		M2P1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x590	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_CMD		M2P1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x594	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_WRITE		M2P1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x598	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_READ		M2P1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x59C	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_WRITERESP		M2P1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x5A0	HSM_M_BUS_SAFETY_CTRL		HSM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM Initiator Port
0x5A4	HSM_M_BUS_SAFETY_FI		HSM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM Initiator Port
0x5A8	HSM_M_BUS_SAFETY_ERR		HSM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM Initiator Port
0x5AC	HSM_M_BUS_SAFETY_ERR_STAT_DATA0		HSM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM Initiator Port
0x5B0	HSM_M_BUS_SAFETY_ERR_STAT_CMD		HSM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM Initiator Port
0x5B4	HSM_M_BUS_SAFETY_ERR_STAT_WRITE		HSM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x5B8	HSM_M_BUS_SAFETY_ERR_STAT_READ		HSM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM Initiator Port
0x5BC	HSM_M_BUS_SAFETY_ERR_STAT_WRITERESP		HSM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM Initiator Port
0x5C0	HSM_S_BUS_SAFETY_CTRL		HSM_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM Target Port
0x5C4	HSM_S_BUS_SAFETY_FI		HSM_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM Target Port
0x5C8	HSM_S_BUS_SAFETY_ERR		HSM_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM Target Port
0x5CC	HSM_S_BUS_SAFETY_ERR_STAT_DATA0		HSM_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM Target Port
0x5D0	HSM_S_BUS_SAFETY_ERR_STAT_CMD		HSM_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM Target Port
0x5D4	HSM_S_BUS_SAFETY_ERR_STAT_WRITE		HSM_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM Target Port
0x5D8	HSM_S_BUS_SAFETY_ERR_STAT_READ		HSM_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM Target Port
0x5DC	HSM_S_BUS_SAFETY_ERR_STAT_WRITERESP		HSM_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM Target Port
0x5E0	ICSSMSLAVE_BUS_SAFETY_CTRL	ICSSM_S_BUS_SAFETY_CTRL	ICSSM_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM Target Port
0x5E4	ICSSMSLAVE_BUS_SAFETY_FI	ICSSM_S_BUS_SAFETY_FI	ICSSM_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM Target Port
0x5E8	ICSSMSLAVE_BUS_SAFETY_ERR	ICSSM_S_BUS_SAFETY_ERR	ICSSM_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM Target Port
0x5EC	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_DATA0	ICSSM_S_BUS_SAFETY_ERR_STAT_DATA0	ICSSM_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM Target Port
0x5F0	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_CMD	ICSSM_S_BUS_SAFETY_ERR_STAT_CMD	ICSSM_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM Target Port
0x5F4	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_WRITE	ICSSM_S_BUS_SAFETY_ERR_STAT_WRITE	ICSSM_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM Target Port
0x5F8	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_READ	ICSSM_S_BUS_SAFETY_ERR_STAT_READ	ICSSM_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM Target Port
0x5FC	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP	ICSSM_S_BUS_SAFETY_ERR_STAT_WRITERESP	ICSSM_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM Target Port
0x600	DAP_BUS_SAFETY_CTRL		DAP Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of DAP Initiator Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x604	DAP_BUS_SAFETY_FI		DAP Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of DAP Initiator Port
0x608	DAP_BUS_SAFETY_ERR		DAP Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of DAP Initiator Port
0x60C	DAP_BUS_SAFETY_ERR_STAT_DATA0		DAP Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of DAP Initiator Port
0x610	DAP_BUS_SAFETY_ERR_STAT_CMD		DAP Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of DAP Initiator Port
0x614	DAP_BUS_SAFETY_ERR_STAT_WRITE		DAP Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of DAP Initiator Port
0x618	DAP_BUS_SAFETY_ERR_STAT_READ		DAP Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of DAP Initiator Port
0x61C	DAP_BUS_SAFETY_ERR_STAT_WRITERESP		DAP Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of DAP Initiator Port
0x620	MSS_L2_A_BUS_SAFETY_CTRL	L2OCRAM_BANK0_BUS_SAFETY_CTRL	L2 BANK0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK0 Target Port
0x624	MSS_L2_A_BUS_SAFETY_FI	L2OCRAM_BANK0_BUS_SAFETY_FI	L2 BANK0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK0 Target Port
0x628	MSS_L2_A_BUS_SAFETY_ERR	L2OCRAM_BANK0_BUS_SAFETY_ERR	L2 BANK0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK0 Target Port
0x62C	MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK0 Target Port
0x630	MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD	L2 BANK0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK0 Target Port
0x634	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK0 Target Port
0x638	MSS_L2_A_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ	L2 BANK0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK0 Target Port
0x63C	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK0 Target Port
0x640	MSS_L2_B_BUS_SAFETY_CTRL	L2OCRAM_BANK1_BUS_SAFETY_CTRL	L2 BANK1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK1 Target Port
0x644	MSS_L2_B_BUS_SAFETY_FI	L2OCRAM_BANK1_BUS_SAFETY_FI	L2 BANK1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK1 Target Port
0x648	MSS_L2_B_BUS_SAFETY_ERR	L2OCRAM_BANK1_BUS_SAFETY_ERR	L2 BANK1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK1 Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x64C	MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK1 Target Port
0x650	MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD	L2 BANK1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK1 Target Port
0x654	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK1 Target Port
0x658	MSS_L2_B_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ	L2 BANK1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK1 Target Port
0x65C	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK1 Target Port
0x660	MSS_L2_C_BUS_SAFETY_CTRL	L2OCRAM_BANK2_BUS_SAFETY_CTRL	L2 BANK2 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK2 Target Port
0x664	MSS_L2_C_BUS_SAFETY_FI	L2OCRAM_BANK2_BUS_SAFETY_FI	L2 BANK2 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK2 Target Port
0x668	MSS_L2_C_BUS_SAFETY_ERR	L2OCRAM_BANK2_BUS_SAFETY_ERR	L2 BANK2 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK2 Target Port
0x66C	MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK2 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK2 Target Port
0x670	MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD	L2 BANK2 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK2 Target Port
0x674	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK2 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK2 Target Port
0x678	MSS_L2_C_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ	L2 BANK2 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK2 Target Port
0x67C	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK2 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK2 Target Port
0x680	MSS_L2_D_BUS_SAFETY_CTRL	L2OCRAM_BANK3_BUS_SAFETY_CTRL	L2 BANK3 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK3 Target Port
0x684	MSS_L2_D_BUS_SAFETY_FI	L2OCRAM_BANK3_BUS_SAFETY_FI	L2 BANK3 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK3 Target Port
0x688	MSS_L2_D_BUS_SAFETY_ERR	L2OCRAM_BANK3_BUS_SAFETY_ERR	L2 BANK3 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK3 Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x68C	MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK3 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK3 Target Port
0x690	MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD	L2 BANK3 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK3 Target Port
0x694	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK3 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK3 Target Port
0x698	MSS_L2_D_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ	L2 BANK3 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK3 Target Port
0x69C	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK3 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK3 Target Port
0x6A0	MSS_MBOX_BUS_SAFETY_CTRL	MBOX_SRAM_BUS_SAFETY_CTRL	MBOX SRAM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MBOX SRAM Target Port
0x6A4	MSS_MBOX_BUS_SAFETY_FI	MBOX_SRAM_BUS_SAFETY_FI	MBOX SRAM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MBOX SRAM Target Port
0x6A8	MSS_MBOX_BUS_SAFETY_ERR	MBOX_SRAM_BUS_SAFETY_ERR	MBOX SRAM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MBOX SRAM Target Port
0x6AC	MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0	MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0	MBOX SRAM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B0	MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD	MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD	MBOX SRAM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B4	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE	MBOX SRAM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B8	MSS_MBOX_BUS_SAFETY_ERR_STAT_READ	MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ	MBOX SRAM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6BC	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP	MBOX SRAM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6C0	MSS_STM_STIM_BUS_SAFETY_CTRL	STM_STIM_BUS_SAFETY_CTRL	STM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of STM Target Port
0x6C4	MSS_STM_STIM_BUS_SAFETY_FI	STM_STIM_BUS_SAFETY_FI	STM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of STM Target Port
0x6C8	MSS_STM_STIM_BUS_SAFETY_ERR	STM_STIM_BUS_SAFETY_ERR	STM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of STM Target Port
0x6CC	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0	STM_STIM_BUS_SAFETY_ERR_STAT_DATA0	STM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of STM Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x6D0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD	STM_STIM_BUS_SAFETY_ERR_STAT_CMD	STM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of STM Target Port
0x6D4	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE	STM_STIM_BUS_SAFETY_ERR_STAT_WRITE	STM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of STM Target Port
0x6D8	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ	STM_STIM_BUS_SAFETY_ERR_STAT_READ	STM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of STM Target Port
0x6DC	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP	STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP	STM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of STM Target Port
0x6E0	MSS_MMC_BUS_SAFETY_CTRL	MMC0_BUS_SAFETY_CTRL	MMC0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MMC0 Target Port
0x6E4	MSS_MMC_BUS_SAFETY_FI	MMC0_BUS_SAFETY_FI	MMC0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MMC0 Target Port
0x6E8	MSS_MMC_BUS_SAFETY_ERR	MMC0_BUS_SAFETY_ERR	MMC0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MMC0 Target Port
0x6EC	MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0	MMC0_BUS_SAFETY_ERR_STAT_DATA0	MMC0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MMC0 Target Port
0x6F0	MSS_MMC_BUS_SAFETY_ERR_STAT_CMD	MMC0_BUS_SAFETY_ERR_STAT_CMD	MMC0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MMC0 Target Port
0x6F4	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE	MMC0_BUS_SAFETY_ERR_STAT_WRITE	MMC0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MMC0 Target Port
0x6F8	MSS_MMC_BUS_SAFETY_ERR_STAT_READ	MMC0_BUS_SAFETY_ERR_STAT_READ	MMC0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MMC0 Target Port
0x6FC	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP	MMC0_BUS_SAFETY_ERR_STAT_WRITERESP	MMC0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MMC0 Target Port
0x700	MSS_GPMC_BUS_SAFETY_CTRL	GPMC0_BUS_SAFETY_CTRL	GPMC0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of GPMC0 Target Port
0x704	MSS_GPMC_BUS_SAFETY_FI	GPMC0_BUS_SAFETY_FI	GPMC0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of GPMC0 Target Port
0x708	MSS_GPMC_BUS_SAFETY_ERR	GPMC0_BUS_SAFETY_ERR	GPMC0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of GPMC0 Target Port
0x70C	MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0	GPMC0_BUS_SAFETY_ERR_STAT_DATA0	GPMC0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of GPMC0 Target Port
0x710	MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD	GPMC0_BUS_SAFETY_ERR_STAT_CMD	GPMC0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of GPMC0 Target Port
0x714	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE	GPMC0_BUS_SAFETY_ERR_STAT_WRITE	GPMC0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of GPMC0 Target Port

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x718	MSS_GPMC_BUS_SAFETY_ERR_STAT_READ	GPMC0_BUS_SAFETY_ERR_STAT_READ	GPMC0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of GPMC0 Target Port
0x71C	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP	GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP	GPMC0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of GPMC0 Target Port
0x720	MAIN_VBUSP_BUS_SAFETY_CTRL		Main Vbusp Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of Main VBUSP Interconnect
0x724	MAIN_VBUSP_BUS_SAFETY_FI		Main Vbusp Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of Main VBUSP Interconnect
0x728	MAIN_VBUSP_BUS_SAFETY_ERR		Main Vbusp Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of Main VBUSP Interconnect
0x740	MSS_CR5A0_AHB_BUS_SAFETY_CTRL	R5SS0_CORE0_AHB_BUS_SAFETY_CTRL	R5SS0 CORE0 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 Peripheral Port
0x744	MSS_CR5A0_AHB_BUS_SAFETY_FI	R5SS0_CORE0_AHB_BUS_SAFETY_FI	R5SS0 CORE0 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 Peripheral Port
0x748	MSS_CR5A0_AHB_BUS_SAFETY_ERR	R5SS0_CORE0_AHB_BUS_SAFETY_ERR	R5SS0 CORE0 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 Peripheral Port
0x760	MSS_CR5B0_AHB_BUS_SAFETY_CTRL	R5SS0_CORE1_AHB_BUS_SAFETY_CTRL	R5SS0 CORE1 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 Peripheral Port
0x764	MSS_CR5B0_AHB_BUS_SAFETY_FI	R5SS0_CORE1_AHB_BUS_SAFETY_FI	R5SS0 CORE1 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 Peripheral Port
0x768	MSS_CR5B0_AHB_BUS_SAFETY_ERR	R5SS0_CORE1_AHB_BUS_SAFETY_ERR	R5SS0 CORE1 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 Peripheral Port
0x780	MSS_CR5A1_AHB_BUS_SAFETY_CTRL	R5SS1_CORE0_AHB_BUS_SAFETY_CTRL	R5SS1 CORE0 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 Peripheral Port
0x784	MSS_CR5A1_AHB_BUS_SAFETY_FI	R5SS1_CORE0_AHB_BUS_SAFETY_FI	R5SS1 CORE0 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 Peripheral Port
0x788	MSS_CR5A1_AHB_BUS_SAFETY_ERR	R5SS1_CORE0_AHB_BUS_SAFETY_ERR	R5SS1 CORE0 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 Peripheral Port
0x7A0	MSS_CR5B1_AHB_BUS_SAFETY_CTRL	R5SS1_CORE1_AHB_BUS_SAFETY_CTRL	R5SS1 CORE1 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 Peripheral Port
0x7A4	MSS_CR5B1_AHB_BUS_SAFETY_FI	R5SS1_CORE1_AHB_BUS_SAFETY_FI	R5SS1 CORE1 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 Peripheral Port
0x7A8	MSS_CR5B1_AHB_BUS_SAFETY_ERR	R5SS1_CORE1_AHB_BUS_SAFETY_ERR	R5SS1 CORE1 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 Peripheral Port
0x7C0	PERI_VBUSP_BUS_SAFETY_CTRL		Peri Vbusp Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of Peri VBUSP Interconnect
0x7C4	PERI_VBUSP_BUS_SAFETY_FI		Peri Vbusp Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of Peri VBUSP Interconnect

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x7C8	PERI_VBUSP_BUS_SAFETY_ERR		Peri Vbusp Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of Peri VBUSP Interconnect
0x820	NERROR_MASK		ESM Error Mask Register	This register is used to Mask ESM Error signaling on the nERROR IO
0x834	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK	VBUSM_SAFETY_H_ERRAGG_MASK0	VBUSM Safety High Error Mask Register0	Register to Mask VBUSM Safety High errors
0x838	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS	VBUSM_SAFETY_H_ERRAGG_STATUS0	VBUSM Safety High Error Status Register0	Status register based on mask for VBUSM Safey High Errors
0x83C	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW	VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0	VBUSM Safety High Error Raw Status Register0	Raw status Register for VBUSM Safety High Errors
0x844	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK	VBUSM_SAFETY_H_ERRAGG_MASK1	VBUSM Safety High Error Mask Register1	Register to Mask VBUSM Safety High errors
0x848	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS	VBUSM_SAFETY_H_ERRAGG_STATUS1	VBUSM Safety High Error Status Register1	Status register based on mask for VBUSM Safety High Errors
0x84C	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW	VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1	VBUSM Safety High Error Raw Status Register1	Raw status Register for VBUSM Safety High Errors
0x854	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK	VBUSM_SAFETY_L_ERRAGG_MASK0	VBUSM Safety Low Error Mask Register0	Register to Mask VBUSM Safety Low errors
0x858	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS	VBUSM_SAFETY_L_ERRAGG_STATUS0	VBUSM Safety Low Error Status Register0	Status register based on mask for VBUSM Safety Low Errors
0x85C	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW	VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0	VBUSM Safety Low Error Raw Status Register0	Raw status Register for VBUSM Safety Low Errors
0x864	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK	VBUSM_SAFETY_L_ERRAGG_MASK1	VBUSM Safety Low Error Mask Register1	Register to Mask VBUSM Safety Low errors
0x868	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS	VBUSM_SAFETY_L_ERRAGG_STATUS1	VBUSM Safety Low Error Status Register1	Status register based on mask for VBUSM Safety Low Errors
0x86C	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW	VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1	VBUSM Safety Low Error Raw Status Register1	Raw status Register for VBUSM Safety Low Errors
0x874	MSS_VBUSP_SAFETY_H_ERRAGG_MASK	VBUSP_SAFETY_H_ERRAGG_MASK	VBUSP Safety High Error Mask Register	Register to Mask VBUSP Interconnect Safety High errors
0x878	MSS_VBUSP_SAFETY_H_ERRAGG_STATUS	VBUSP_SAFETY_H_ERRAGG_STATUS	VBUSP Safety High Error Status Register	Status register based on mask for VBUSP Interconnect Safey High Errors
0x87C	MSS_VBUSP_SAFETY_H_ERRAGG_STATUS_RAW	VBUSP_SAFETY_H_ERRAGG_STATUS_RAW	VBUSP Safety High Error Raw Status Register	Raw status Register for VBUSP Interconnect Safety High Errors

2.3 MSS_IOMUX Registers

Table 2-1. IOMUX, IOMUX_IOMUX Registers, Base Address=5310 0000H, Length=6

Offset	Length	Acronym	Register Name	IOMUX Physical Address
0h	32	IOMUX_QSPI0_CSN0_CFG_REG	RW	5310 0000h
4h	32	IOMUX_QSPI0_CSN1_CFG_REG	RW	5310 0004h
8h	32	IOMUX_QSPI0_CLK_CFG_REG	RW	5310 0008h
Ch	32	IOMUX_QSPI0_D0_CFG_REG	RW	5310 000Ch
10h	32	IOMUX_QSPI0_D1_CFG_REG	RW	5310 0010h
14h	32	IOMUX_QSPI0_D2_CFG_REG	RW	5310 0014h
18h	32	IOMUX_QSPI0_D3_CFG_REG	RW	5310 0018h
1Ch	32	IOMUX_MCAN0_RX_CFG_REG	RW	5310 001Ch
20h	32	IOMUX_MCAN0_TX_CFG_REG	RW	5310 0020h
24h	32	IOMUX_MCAN1_RX_CFG_REG	RW	5310 0024h
28h	32	IOMUX_MCAN1_TX_CFG_REG	RW	5310 0028h
2Ch	32	IOMUX_SPI0_CS0_CFG_REG	RW	5310 002Ch
30h	32	IOMUX_SPI0_CLK_CFG_REG	RW	5310 0030h
34h	32	IOMUX_SPI0_D0_CFG_REG	RW	5310 0034h
38h	32	IOMUX_SPI0_D1_CFG_REG	RW	5310 0038h
3Ch	32	IOMUX_SPI1_CS0_CFG_REG	RW	5310 003Ch
40h	32	IOMUX_SPI1_CLK_CFG_REG	RW	5310 0040h
44h	32	IOMUX_SPI1_D0_CFG_REG	RW	5310 0044h
48h	32	IOMUX_SPI1_D1_CFG_REG	RW	5310 0048h
4Ch	32	IOMUX_LIN1_RXD_CFG_REG	RW	5310 004Ch
50h	32	IOMUX_LIN1_TXD_CFG_REG	RW	5310 0050h
54h	32	IOMUX_LIN2_RXD_CFG_REG	RW	5310 0054h
58h	32	IOMUX_LIN2_TXD_CFG_REG	RW	5310 0058h
5Ch	32	IOMUX_I2C1_SCL_CFG_REG	RW	5310 005Ch
60h	32	IOMUX_I2C1_SDA_CFG_REG	RW	5310 0060h
64h	32	IOMUX_UART0_RTSN_CFG_REG	RW	5310 0064h
68h	32	IOMUX_UART0_CTSN_CFG_REG	RW	5310 0068h
6Ch	32	IOMUX_UART0_RXD_CFG_REG	RW	5310 006Ch
70h	32	IOMUX_UART0_TXD_CFG_REG	RW	5310 0070h
74h	32	IOMUX_RGMII1_RXC_CFG_REG	RW	5310 0074h
78h	32	IOMUX_RGMII1_RX_CTL_CFG_REG	RW	5310 0078h
7Ch	32	IOMUX_RGMII1_RD0_CFG_REG	RW	5310 007Ch
80h	32	IOMUX_RGMII1_RD1_CFG_REG	RW	5310 0080h
84h	32	IOMUX_RGMII1_RD2_CFG_REG	RW	5310 0084h
88h	32	IOMUX_RGMII1_RD3_CFG_REG	RW	5310 0088h
8Ch	32	IOMUX_RGMII1_TXC_CFG_REG	RW	5310 008Ch
90h	32	IOMUX_RGMII1_TX_CTL_CFG_REG	RW	5310 0090h
94h	32	IOMUX_RGMII1_TD0_CFG_REG	RW	5310 0094h
98h	32	IOMUX_RGMII1_TD1_CFG_REG	RW	5310 0098h
9Ch	32	IOMUX_RGMII1_TD2_CFG_REG	RW	5310 009Ch
A0h	32	IOMUX_RGMII1_TD3_CFG_REG	RW	5310 00A0h
A4h	32	IOMUX_MDIO0_MDIO_CFG_REG	RW	5310 00A4h
A8h	32	IOMUX_MDIO0_MDC_CFG_REG	RW	5310 00A8h
ACh	32	IOMUX_EPWM0_A_CFG_REG	RW	5310 00ACh
B0h	32	IOMUX_EPWM0_B_CFG_REG	RW	5310 00B0h
B4h	32	IOMUX_EPWM1_A_CFG_REG	RW	5310 00B4h
B8h	32	IOMUX_EPWM1_B_CFG_REG	RW	5310 00B8h

Table 2-1. IOMUX, IOMUX_IOMUX Registers, Base Address=5310 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	IOMUX Physical Address
BCh	32	IOMUX_EPWM2_A_CFG_REG	RW	5310 00BCh
C0h	32	IOMUX_EPWM2_B_CFG_REG	RW	5310 00C0h
C4h	32	IOMUX_EPWM3_A_CFG_REG	RW	5310 00C4h
C8h	32	IOMUX_EPWM3_B_CFG_REG	RW	5310 00C8h
CCh	32	IOMUX_EPWM4_A_CFG_REG	RW	5310 00CCh
D0h	32	IOMUX_EPWM4_B_CFG_REG	RW	5310 00D0h
D4h	32	IOMUX_EPWM5_A_CFG_REG	RW	5310 00D4h
D8h	32	IOMUX_EPWM5_B_CFG_REG	RW	5310 00D8h
DCh	32	IOMUX_EPWM6_A_CFG_REG	RW	5310 00DCh
E0h	32	IOMUX_EPWM6_B_CFG_REG	RW	5310 00E0h
E4h	32	IOMUX_EPWM7_A_CFG_REG	RW	5310 00E4h
E8h	32	IOMUX_EPWM7_B_CFG_REG	RW	5310 00E8h
ECh	32	IOMUX_EPWM8_A_CFG_REG	RW	5310 00ECh
F0h	32	IOMUX_EPWM8_B_CFG_REG	RW	5310 00F0h
F4h	32	IOMUX_EPWM9_A_CFG_REG	RW	5310 00F4h
F8h	32	IOMUX_EPWM9_B_CFG_REG	RW	5310 00F8h
FCh	32	IOMUX_EPWM10_A_CFG_REG	RW	5310 00FCh
100h	32	IOMUX_EPWM10_B_CFG_REG	RW	5310 0100h
104h	32	IOMUX_EPWM11_A_CFG_REG	RW	5310 0104h
108h	32	IOMUX_EPWM11_B_CFG_REG	RW	5310 0108h
10Ch	32	IOMUX_EPWM12_A_CFG_REG	RW	5310 010Ch
110h	32	IOMUX_EPWM12_B_CFG_REG	RW	5310 0110h
114h	32	IOMUX_EPWM13_A_CFG_REG	RW	5310 0114h
118h	32	IOMUX_EPWM13_B_CFG_REG	RW	5310 0118h
11Ch	32	IOMUX_EPWM14_A_CFG_REG	RW	5310 011Ch
120h	32	IOMUX_EPWM14_B_CFG_REG	RW	5310 0120h
124h	32	IOMUX_EPWM15_A_CFG_REG	RW	5310 0124h
128h	32	IOMUX_EPWM15_B_CFG_REG	RW	5310 0128h
12Ch	32	IOMUX_UART1_RXD_CFG_REG	RW	5310 012Ch
130h	32	IOMUX_UART1_TXD_CFG_REG	RW	5310 0130h
134h	32	IOMUX_MMC0_CLK_CFG_REG	RW	5310 0134h
138h	32	IOMUX_MMC0_CMD_CFG_REG	RW	5310 0138h
13Ch	32	IOMUX_MMC0_D0_CFG_REG	RW	5310 013Ch
140h	32	IOMUX_MMC0_D1_CFG_REG	RW	5310 0140h
144h	32	IOMUX_MMC0_D2_CFG_REG	RW	5310 0144h
148h	32	IOMUX_MMC0_D3_CFG_REG	RW	5310 0148h
14Ch	32	IOMUX_MMC0_WP_CFG_REG	RW	5310 014Ch
150h	32	IOMUX_MMC0_CD_CFG_REG	RW	5310 0150h
154h	32	IOMUX_PR0_MDIO0_MDIO_CFG_REG	RW	5310 0154h
158h	32	IOMUX_PR0_MDIO0_MDC_CFG_REG	RW	5310 0158h
15Ch	32	IOMUX_PR0_PRU0_GPO5_CFG_REG	RW	5310 015Ch
160h	32	IOMUX_PR0_PRU0_GPO9_CFG_REG	RW	5310 0160h
164h	32	IOMUX_PR0_PRU0_GPO10_CFG_REG	RW	5310 0164h
168h	32	IOMUX_PR0_PRU0_GPO8_CFG_REG	RW	5310 0168h
16Ch	32	IOMUX_PR0_PRU0_GPO6_CFG_REG	RW	5310 016Ch
170h	32	IOMUX_PR0_PRU0_GPO4_CFG_REG	RW	5310 0170h
174h	32	IOMUX_PR0_PRU0_GPO0_CFG_REG	RW	5310 0174h

Table 2-1. IOMUX, IOMUX_IOMUX Registers, Base Address=5310 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	IOMUX Physical Address
178h	32	IOMUX_PR0_PRU0_GPO1_CFG_REG	RW	5310 0178h
17Ch	32	IOMUX_PR0_PRU0_GPO2_CFG_REG	RW	5310 017Ch
180h	32	IOMUX_PR0_PRU0_GPO3_CFG_REG	RW	5310 0180h
184h	32	IOMUX_PR0_PRU0_GPO16_CFG_REG	RW	5310 0184h
188h	32	IOMUX_PR0_PRU0_GPO15_CFG_REG	RW	5310 0188h
18Ch	32	IOMUX_PR0_PRU0_GPO11_CFG_REG	RW	5310 018Ch
190h	32	IOMUX_PR0_PRU0_GPO12_CFG_REG	RW	5310 0190h
194h	32	IOMUX_PR0_PRU0_GPO13_CFG_REG	RW	5310 0194h
198h	32	IOMUX_PR0_PRU0_GPO14_CFG_REG	RW	5310 0198h
19Ch	32	IOMUX_PR0_PRU1_GPO5_CFG_REG	RW	5310 019Ch
1A0h	32	IOMUX_PR0_PRU1_GPO9_CFG_REG	RW	5310 01A0h
1A4h	32	IOMUX_PR0_PRU1_GPO10_CFG_REG	RW	5310 01A4h
1A8h	32	IOMUX_PR0_PRU1_GPO8_CFG_REG	RW	5310 01A8h
1ACh	32	IOMUX_PR0_PRU1_GPO6_CFG_REG	RW	5310 01ACh
1B0h	32	IOMUX_PR0_PRU1_GPO4_CFG_REG	RW	5310 01B0h
1B4h	32	IOMUX_PR0_PRU1_GPO0_CFG_REG	RW	5310 01B4h
1B8h	32	IOMUX_PR0_PRU1_GPO1_CFG_REG	RW	5310 01B8h
1BCh	32	IOMUX_PR0_PRU1_GPO2_CFG_REG	RW	5310 01BCh
1C0h	32	IOMUX_PR0_PRU1_GPO3_CFG_REG	RW	5310 01C0h
1C4h	32	IOMUX_PR0_PRU1_GPO16_CFG_REG	RW	5310 01C4h
1C8h	32	IOMUX_PR0_PRU1_GPO15_CFG_REG	RW	5310 01C8h
1CCh	32	IOMUX_PR0_PRU1_GPO11_CFG_REG	RW	5310 01CCh
1D0h	32	IOMUX_PR0_PRU1_GPO12_CFG_REG	RW	5310 01D0h
1D4h	32	IOMUX_PR0_PRU1_GPO13_CFG_REG	RW	5310 01D4h
1D8h	32	IOMUX_PR0_PRU1_GPO14_CFG_REG	RW	5310 01D8h
1DCh	32	IOMUX_PR0_PRU1_GPO19_CFG_REG	RW	5310 01DCh
1E0h	32	IOMUX_PR0_PRU1_GPO18_CFG_REG	RW	5310 01E0h
1E4h	32	IOMUX_EXT_REFCLK0_CFG_REG	RW	5310 01E4h
1E8h	32	IOMUX_SDFM0_CLK0_CFG_REG	RW	5310 01E8h
1ECh	32	IOMUX_SDFM0_D0_CFG_REG	RW	5310 01ECh
1F0h	32	IOMUX_SDFM0_CLK1_CFG_REG	RW	5310 01F0h
1F4h	32	IOMUX_SDFM0_D1_CFG_REG	RW	5310 01F4h
1F8h	32	IOMUX_SDFM0_CLK2_CFG_REG	RW	5310 01F8h
1FCh	32	IOMUX_SDFM0_D2_CFG_REG	RW	5310 01FCh
200h	32	IOMUX_SDFM0_CLK3_CFG_REG	RW	5310 0200h
204h	32	IOMUX_SDFM0_D3_CFG_REG	RW	5310 0204h
208h	32	IOMUX_EQEP0_A_CFG_REG	RW	5310 0208h
20Ch	32	IOMUX_EQEP0_B_CFG_REG	RW	5310 020Ch
210h	32	IOMUX_EQEP0_STROBE_CFG_REG	RW	5310 0210h
214h	32	IOMUX_EQEP0_INDEX_CFG_REG	RW	5310 0214h
218h	32	IOMUX_I2C0_SDA_CFG_REG	RW	5310 0218h
21Ch	32	IOMUX_I2C0_SCL_CFG_REG	RW	5310 021Ch
220h	32	IOMUX_MCAN2_TX_CFG_REG	RW	5310 0220h
224h	32	IOMUX_MCAN2_RX_CFG_REG	RW	5310 0224h
228h	32	IOMUX_CLKOUT0_CFG_REG	RW	5310 0228h
22Ch	32	IOMUX_WARMRSTN_CFG_REG	RW	5310 022Ch
230h	32	IOMUX_SAFETY_ERRORN_CFG_REG	RW	5310 0230h

Table 2-1. IOMUX, IOMUX_IOMUX Registers, Base Address=5310 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	IOMUX Physical Address
234h	32	IOMUX_TDI_CFG_REG	RW	5310 0234h
238h	32	IOMUX_TDO_CFG_REG	RW	5310 0238h
23Ch	32	IOMUX_TMS_CFG_REG	RW	5310 023Ch
240h	32	IOMUX_TCK_CFG_REG	RW	5310 0240h
244h	32	IOMUX_QSPI0_CLKLB_CFG_REG	RW	5310 0244h
248h	32	IOMUX_QUAL_GRP_0_CFG_REG	RW	5310 0248h
24Ch	32	IOMUX_QUAL_GRP_1_CFG_REG	RW	5310 024Ch
250h	32	IOMUX_QUAL_GRP_2_CFG_REG	RW	5310 0250h
254h	32	IOMUX_QUAL_GRP_3_CFG_REG	RW	5310 0254h
258h	32	IOMUX_QUAL_GRP_4_CFG_REG	RW	5310 0258h
25Ch	32	IOMUX_QUAL_GRP_5_CFG_REG	RW	5310 025Ch
260h	32	IOMUX_QUAL_GRP_6_CFG_REG	RW	5310 0260h
264h	32	IOMUX_QUAL_GRP_7_CFG_REG	RW	5310 0264h
268h	32	IOMUX_QUAL_GRP_8_CFG_REG	RW	5310 0268h
26Ch	32	IOMUX_QUAL_GRP_9_CFG_REG	RW	5310 026Ch
270h	32	IOMUX_QUAL_GRP_10_CFG_REG	RW	5310 0270h
274h	32	IOMUX_QUAL_GRP_11_CFG_REG	RW	5310 0274h
278h	32	IOMUX_QUAL_GRP_12_CFG_REG	RW	5310 0278h
27Ch	32	IOMUX_QUAL_GRP_13_CFG_REG	RW	5310 027Ch
280h	32	IOMUX_QUAL_GRP_14_CFG_REG	RW	5310 0280h
284h	32	IOMUX_QUAL_GRP_15_CFG_REG	RW	5310 0284h
288h	32	IOMUX_QUAL_GRP_16_CFG_REG	RW	5310 0288h
28Ch	32	IOMUX_QUAL_GRP_17_CFG_REG	RW	5310 028Ch
290h	32	IOMUX_USER_MODE_EN	RW	5310 0290h
294h	32	IOMUX_PADGLBL_CFG_REG	RW	5310 0294h
298h	32	IOMUX_IO_CFG_KICK0	RW	5310 0298h
29Ch	32	IOMUX_IO_CFG_KICK1	RW	5310 029Ch

2.3.1 IOMUX_QSPI0_CSN0_CFG_REG Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-2. Instance Table

Instance Name	Physical Address
IOMUX	5310 0000h

Figure 2-1. IOMUX_QSPI0_CSN0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-3. QSPI0_CSN0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.2 IOMUX_QSPI0_CSN1_CFG_REG Register (Offset = 4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-4. Instance Table

Instance Name	Physical Address
IOMUX	5310 0004h

Figure 2-2. IOMUX_QSPI0_CSN1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-5. QSPI0_CSN1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.3 IOMUX_QSPI0_CLK_CFG_REG Register (Offset = 8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-6. Instance Table

Instance Name	Physical Address
IOMUX	5310 0008h

Figure 2-3. IOMUX_QSPI0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-7. QSPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.4 IOMUX_QSPI0_D0_CFG_REG Register (Offset = Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-8. Instance Table

Instance Name	Physical Address
IOMUX	5310 000Ch

Figure 2-4. IOMUX_QSPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	0	1	111			

Access Types Legend

Table 2-9. QSPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.5 IOMUX_QSPI0_D1_CFG_REG Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-10. Instance Table

Instance Name	Physical Address
IOMUX	5310 0010h

Figure 2-5. IOMUX_QSPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	0	1	111			

Access Types Legend

Table 2-11. QSPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.6 IOMUX_QSPI0_D2_CFG_REG Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-12. Instance Table

Instance Name	Physical Address
IOMUX	5310 0014h

Figure 2-6. IOMUX_QSPI0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-13. QSPI0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.7 IOMUX_QSPI0_D3_CFG_REG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-14. Instance Table

Instance Name	Physical Address
IOMUX	5310 0018h

Figure 2-7. IOMUX_QSPI0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-15. QSPI0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.8 IOMUX_MCAN0_RX_CFG_REG Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-16. Instance Table

Instance Name	Physical Address
IOMUX	5310 001Ch

Figure 2-8. IOMUX_MCAN0_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-17. MCAN0_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.9 IOMUX_MCAN0_TX_CFG_REG Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-18. Instance Table

Instance Name	Physical Address
IOMUX	5310 0020h

Figure 2-9. IOMUX_MCAN0_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-19. MCAN0_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.10 IOMUX_MCAN1_RX_CFG_REG Register (Offset = 24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-20. Instance Table

Instance Name	Physical Address
IOMUX	5310 0024h

Figure 2-10. IOMUX_MCAN1_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-21. MCAN1_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.11 IOMUX_MCAN1_TX_CFG_REG Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-22. Instance Table

Instance Name	Physical Address
IOMUX	5310 0028h

Figure 2-11. IOMUX_MCAN1_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-23. MCAN1_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.12 IOMUX_SPI0_CS0_CFG_REG Register (Offset = 2Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-24. Instance Table

Instance Name	Physical Address
IOMUX	5310 002Ch

Figure 2-12. IOMUX_SPI0_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-25. SPI0_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.13 IOMUX_SPI0_CLK_CFG_REG Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-26. Instance Table

Instance Name	Physical Address
IOMUX	5310 0030h

Figure 2-13. IOMUX_SPI0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	0	1	111			

Access Types Legend

Table 2-27. SPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.14 IOMUX_SPI0_D0_CFG_REG Register (Offset = 34h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-28. Instance Table

Instance Name	Physical Address
IOMUX	5310 0034h

Figure 2-14. IOMUX_SPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	0	1	111			

Access Types Legend

Table 2-29. SPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.15 IOMUX_SPI0_D1_CFG_REG Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-30. Instance Table

Instance Name	Physical Address
IOMUX	5310 0038h

Figure 2-15. IOMUX_SPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-31. SPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.16 IOMUX_SPI1_CS0_CFG_REG Register (Offset = 3Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-32. Instance Table

Instance Name	Physical Address
IOMUX	5310 003Ch

Figure 2-16. IOMUX_SPI1_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-33. SPI1_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.17 IOMUX_SPI1_CLK_CFG_REG Register (Offset = 40h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-34. Instance Table

Instance Name	Physical Address
IOMUX	5310 0040h

Figure 2-17. IOMUX_SPI1_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-35. SPI1_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.18 IOMUX_SPI1_D0_CFG_REG Register (Offset = 44h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-36. Instance Table

Instance Name	Physical Address
IOMUX	5310 0044h

Figure 2-18. IOMUX_SPI1_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-37. SPI1_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.19 IOMUX_SPI1_D1_CFG_REG Register (Offset = 48h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-38. Instance Table

Instance Name	Physical Address
IOMUX	5310 0048h

Figure 2-19. IOMUX_SPI1_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-39. SPI1_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.20 IOMUX_LIN1_RXD_CFG_REG Register (Offset = 4Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-40. Instance Table

Instance Name	Physical Address
IOMUX	5310 004Ch

Figure 2-20. IOMUX_LIN1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-41. LIN1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.21 IOMUX_LIN1_TXD_CFG_REG Register (Offset = 50h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-42. Instance Table

Instance Name	Physical Address
IOMUX	5310 0050h

Figure 2-21. IOMUX_LIN1_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-43. LIN1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.22 IOMUX_LIN2_RXD_CFG_REG Register (Offset = 54h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-44. Instance Table

Instance Name	Physical Address
IOMUX	5310 0054h

Figure 2-22. IOMUX_LIN2_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-45. LIN2_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.23 IOMUX_LIN2_TXD_CFG_REG Register (Offset = 58h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-46. Instance Table

Instance Name	Physical Address
IOMUX	5310 0058h

Figure 2-23. IOMUX_LIN2_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-47. LIN2_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.24 IOMUX_I2C1_SCL_CFG_REG Register (Offset = 5Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-48. Instance Table

Instance Name	Physical Address
IOMUX	5310 005Ch

Figure 2-24. IOMUX_I2C1_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-49. I2C1_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.25 IOMUX_I2C1_SDA_CFG_REG Register (Offset = 60h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-50. Instance Table

Instance Name	Physical Address
IOMUX	5310 0060h

Figure 2-25. IOMUX_I2C1_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-51. I2C1_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.26 IOMUX_UART0_RTSN_CFG_REG Register (Offset = 64h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-52. Instance Table

Instance Name	Physical Address
IOMUX	5310 0064h

Figure 2-26. IOMUX_UART0_RTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-53. UART0_RTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.27 IOMUX_UART0_CTSN_CFG_REG Register (Offset = 68h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-54. Instance Table

Instance Name	Physical Address
IOMUX	5310 0068h

Figure 2-27. IOMUX_UART0_CTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-55. UART0_CTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.28 IOMUX_UART0_RXD_CFG_REG Register (Offset = 6Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-56. Instance Table

Instance Name	Physical Address
IOMUX	5310 006Ch

Figure 2-28. IOMUX_UART0_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-57. UART0_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.29 IOMUX_UART0_TXD_CFG_REG Register (Offset = 70h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-58. Instance Table

Instance Name	Physical Address
IOMUX	5310 0070h

Figure 2-29. IOMUX_UART0_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-59. UART0_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.30 IOMUX_RGMII1_RXC_CFG_REG Register (Offset = 74h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-60. Instance Table

Instance Name	Physical Address
IOMUX	5310 0074h

Figure 2-30. IOMUX_RGMII1_RXC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-61. RGMII1_RXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.31 IOMUX_RGMII1_RX_CTL_CFG_REG Register (Offset = 78h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-62. Instance Table

Instance Name	Physical Address
IOMUX	5310 0078h

Figure 2-31. IOMUX_RGMII1_RX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-63. RGMII1_RX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.32 IOMUX_RGMII1_RD0_CFG_REG Register (Offset = 7Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-64. Instance Table

Instance Name	Physical Address
IOMUX	5310 007Ch

Figure 2-32. IOMUX_RGMII1_RD0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-65. RGMII1_RD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.33 IOMUX_RGMII1_RD1_CFG_REG Register (Offset = 80h) [reset = h]

Short Description: RW

Long Description:

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Table 2-66. Instance Table

Instance Name	Physical Address
IOMUX	5310 0080h

Figure 2-33. IOMUX_RGMII1_RD1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-67. RGMII1_RD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.34 IOMUX_RGMII1_RD2_CFG_REG Register (Offset = 84h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-68. Instance Table

Instance Name	Physical Address
IOMUX	5310 0084h

Figure 2-34. IOMUX_RGMII1_RD2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-69. RGMII1_RD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.35 IOMUX_RGMII1_RD3_CFG_REG Register (Offset = 88h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-70. Instance Table

Instance Name	Physical Address
IOMUX	5310 0088h

Figure 2-35. IOMUX_RGMII1_RD3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-71. RGMII1_RD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.36 IOMUX_RGMII1_TXC_CFG_REG Register (Offset = 8Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-72. Instance Table

Instance Name	Physical Address
IOMUX	5310 008Ch

Figure 2-36. IOMUX_RGMII1_TXC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-73. RGMII1_TXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.37 IOMUX_RGMII1_TX_CTL_CFG_REG Register (Offset = 90h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-74. Instance Table

Instance Name	Physical Address
IOMUX	5310 0090h

Figure 2-37. IOMUX_RGMII1_TX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-75. RGMII1_TX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.38 IOMUX_RGMII1_TD0_CFG_REG Register (Offset = 94h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-76. Instance Table

Instance Name	Physical Address
IOMUX	5310 0094h

Figure 2-38. IOMUX_RGMII1_TD0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-77. RGMII1_TD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.39 IOMUX_RGMII1_TD1_CFG_REG Register (Offset = 98h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-78. Instance Table

Instance Name	Physical Address
IOMUX	5310 0098h

Figure 2-39. IOMUX_RGMII1_TD1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-79. RGMII1_TD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.40 IOMUX_RGMII1_TD2_CFG_REG Register (Offset = 9Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-80. Instance Table

Instance Name	Physical Address
IOMUX	5310 009Ch

Figure 2-40. IOMUX_RGMII1_TD2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-81. RGMII1_TD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.41 IOMUX_RGMII1_TD3_CFG_REG Register (Offset = A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-82. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A0h

Figure 2-41. IOMUX_RGMII1_TD3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-83. RGMII1_TD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.42 IOMUX_MDIO0_MDIO_CFG_REG Register (Offset = A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-84. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A4h

Figure 2-42. IOMUX_MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-85. MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.43 IOMUX_MDIO0_MDC_CFG_REG Register (Offset = A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-86. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A8h

Figure 2-43. IOMUX_MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-87. MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.44 IOMUX_EPWM0_A_CFG_REG Register (Offset = ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-88. Instance Table

Instance Name	Physical Address
IOMUX	5310 00ACh

Figure 2-44. IOMUX_EPWM0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-89. EPWM0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.45 IOMUX_EPWM0_B_CFG_REG Register (Offset = B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-90. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B0h

Figure 2-45. IOMUX_EPWM0_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-91. EPWM0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.46 IOMUX_EPWM1_A_CFG_REG Register (Offset = B4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-92. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B4h

Figure 2-46. IOMUX_EPWM1_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-93. EPWM1_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.47 IOMUX_EPWM1_B_CFG_REG Register (Offset = B8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-94. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B8h

Figure 2-47. IOMUX_EPWM1_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-95. EPWM1_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.48 IOMUX_EPWM2_A_CFG_REG Register (Offset = BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-96. Instance Table

Instance Name	Physical Address
IOMUX	5310 00BCh

Figure 2-48. IOMUX_EPWM2_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-97. EPWM2_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.49 IOMUX_EPWM2_B_CFG_REG Register (Offset = C0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-98. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C0h

Figure 2-49. IOMUX_EPWM2_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-99. EPWM2_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.50 IOMUX_EPWM3_A_CFG_REG Register (Offset = C4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-100. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C4h

Figure 2-50. IOMUX_EPWM3_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-101. EPWM3_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.51 IOMUX_EPWM3_B_CFG_REG Register (Offset = C8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-102. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C8h

Figure 2-51. IOMUX_EPWM3_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-103. EPWM3_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.52 IOMUX_EPWM4_A_CFG_REG Register (Offset = CCh) [reset = h]

Short Description: RW

Long Description:

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Table 2-104. Instance Table

Instance Name	Physical Address
IOMUX	5310 00CCh

Figure 2-52. IOMUX_EPWM4_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-105. EPWM4_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.53 IOMUX_EPWM4_B_CFG_REG Register (Offset = D0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-106. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D0h

Figure 2-53. IOMUX_EPWM4_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-107. EPWM4_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.54 IOMUX_EPWM5_A_CFG_REG Register (Offset = D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-108. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D4h

Figure 2-54. IOMUX_EPWM5_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-109. EPWM5_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.55 IOMUX_EPWM5_B_CFG_REG Register (Offset = D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-110. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D8h

Figure 2-55. IOMUX_EPWM5_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-111. EPWM5_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.56 IOMUX_EPWM6_A_CFG_REG Register (Offset = DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-112. Instance Table

Instance Name	Physical Address
IOMUX	5310 00DCh

Figure 2-56. IOMUX_EPWM6_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-113. EPWM6_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.57 IOMUX_EPWM6_B_CFG_REG Register (Offset = E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-114. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E0h

Figure 2-57. IOMUX_EPWM6_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-115. EPWM6_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.58 IOMUX_EPWM7_A_CFG_REG Register (Offset = E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-116. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E4h

Figure 2-58. IOMUX_EPWM7_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-117. EPWM7_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.59 IOMUX_EPWM7_B_CFG_REG Register (Offset = E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-118. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E8h

Figure 2-59. IOMUX_EPWM7_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-119. EPWM7_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.60 IOMUX_EPWM8_A_CFG_REG Register (Offset = ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-120. Instance Table

Instance Name	Physical Address
IOMUX	5310 00ECh

Figure 2-60. IOMUX_EPWM8_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-121. EPWM8_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.61 IOMUX_EPWM8_B_CFG_REG Register (Offset = F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-122. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F0h

Figure 2-61. IOMUX_EPWM8_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-123. EPWM8_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.62 IOMUX_EPWM9_A_CFG_REG Register (Offset = F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-124. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F4h

Figure 2-62. IOMUX_EPWM9_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-125. EPWM9_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.63 IOMUX_EPWM9_B_CFG_REG Register (Offset = F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-126. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F8h

Figure 2-63. IOMUX_EPWM9_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-127. EPWM9_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.64 IOMUX_EPWM10_A_CFG_REG Register (Offset = FCh) [reset = h]

Short Description: RW

Long Description:

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Table 2-128. Instance Table

Instance Name	Physical Address
IOMUX	5310 00FCh

Figure 2-64. IOMUX_EPWM10_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-129. EPWM10_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.65 IOMUX_EPWM10_B_CFG_REG Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-130. Instance Table

Instance Name	Physical Address
IOMUX	5310 0100h

Figure 2-65. IOMUX_EPWM10_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-131. EPWM10_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.66 IOMUX_EPWM11_A_CFG_REG Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

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Table 2-132. Instance Table

Instance Name	Physical Address
IOMUX	5310 0104h

Figure 2-66. IOMUX_EPWM11_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-133. EPWM11_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.67 IOMUX_EPWM11_B_CFG_REG Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-134. Instance Table

Instance Name	Physical Address
IOMUX	5310 0108h

Figure 2-67. IOMUX_EPWM11_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-135. EPWM11_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.68 IOMUX_EPWM12_A_CFG_REG Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-136. Instance Table

Instance Name	Physical Address
IOMUX	5310 010Ch

Figure 2-68. IOMUX_EPWM12_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-137. EPWM12_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.69 IOMUX_EPWM12_B_CFG_REG Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

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Table 2-138. Instance Table

Instance Name	Physical Address
IOMUX	5310 0110h

Figure 2-69. IOMUX_EPWM12_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-139. EPWM12_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.70 IOMUX_EPWM13_A_CFG_REG Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

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Table 2-140. Instance Table

Instance Name	Physical Address
IOMUX	5310 0114h

Figure 2-70. IOMUX_EPWM13_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-141. EPWM13_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.71 IOMUX_EPWM13_B_CFG_REG Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

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Table 2-142. Instance Table

Instance Name	Physical Address
IOMUX	5310 0118h

Figure 2-71. IOMUX_EPWM13_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-143. EPWM13_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.72 IOMUX_EPWM14_A_CFG_REG Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-144. Instance Table

Instance Name	Physical Address
IOMUX	5310 011Ch

Figure 2-72. IOMUX_EPWM14_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-145. EPWM14_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.73 IOMUX_EPWM14_B_CFG_REG Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

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Table 2-146. Instance Table

Instance Name	Physical Address
IOMUX	5310 0120h

Figure 2-73. IOMUX_EPWM14_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-147. EPWM14_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.74 IOMUX_EPWM15_A_CFG_REG Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-148. Instance Table

Instance Name	Physical Address
IOMUX	5310 0124h

Figure 2-74. IOMUX_EPWM15_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-149. EPWM15_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.75 IOMUX_EPWM15_B_CFG_REG Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-150. Instance Table

Instance Name	Physical Address
IOMUX	5310 0128h

Figure 2-75. IOMUX_EPWM15_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-151. EPWM15_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.76 IOMUX_UART1_RXD_CFG_REG Register (Offset = 12Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-152. Instance Table

Instance Name	Physical Address
IOMUX	5310 012Ch

Figure 2-76. IOMUX_UART1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-153. UART1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.77 IOMUX_UART1_TXD_CFG_REG Register (Offset = 130h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-154. Instance Table

Instance Name	Physical Address
IOMUX	5310 0130h

Figure 2-77. IOMUX_UART1_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-155. UART1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.78 IOMUX_MMC0_CLK_CFG_REG Register (Offset = 134h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-156. Instance Table

Instance Name	Physical Address
IOMUX	5310 0134h

Figure 2-78. IOMUX_MMC0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-157. MMC0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.79 IOMUX_MMC0_CMD_CFG_REG Register (Offset = 138h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-158. Instance Table

Instance Name	Physical Address
IOMUX	5310 0138h

Figure 2-79. IOMUX_MMC0_CMD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-159. MMC0_CMD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.80 IOMUX_MMC0_D0_CFG_REG Register (Offset = 13Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-160. Instance Table

Instance Name	Physical Address
IOMUX	5310 013Ch

Figure 2-80. IOMUX_MMC0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-161. MMC0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.81 IOMUX_MMC0_D1_CFG_REG Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-162. Instance Table

Instance Name	Physical Address
IOMUX	5310 0140h

Figure 2-81. IOMUX_MMC0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-163. MMC0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.82 IOMUX_MMC0_D2_CFG_REG Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-164. Instance Table

Instance Name	Physical Address
IOMUX	5310 0144h

Figure 2-82. IOMUX_MMC0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-165. MMC0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.83 IOMUX_MMC0_D3_CFG_REG Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

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Table 2-166. Instance Table

Instance Name	Physical Address
IOMUX	5310 0148h

Figure 2-83. IOMUX_MMC0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-167. MMC0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.84 IOMUX_MMC0_WP_CFG_REG Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-168. Instance Table

Instance Name	Physical Address
IOMUX	5310 014Ch

Figure 2-84. IOMUX_MMC0_WP_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-169. MMC0_WP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.85 IOMUX_MMC0_CD_CFG_REG Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-170. Instance Table

Instance Name	Physical Address
IOMUX	5310 0150h

Figure 2-85. IOMUX_MMC0_CD_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-171. MMC0_CD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.86 IOMUX_PR0_MDIO0_MDIO_CFG_REG Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-172. Instance Table

Instance Name	Physical Address
IOMUX	5310 0154h

Figure 2-86. IOMUX_PR0_MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-173. PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.87 IOMUX_PR0_MDIO0_MDC_CFG_REG Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-174. Instance Table

Instance Name	Physical Address
IOMUX	5310 0158h

Figure 2-87. IOMUX_PR0_MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-175. PR0_MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.88 IOMUX_PR0_PRU0_GPO5_CFG_REG Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-176. Instance Table

Instance Name	Physical Address
IOMUX	5310 015Ch

Figure 2-88. IOMUX_PR0_PRU0_GPO5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-177. PR0_PRU0_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.89 IOMUX_PR0_PRU0_GPO9_CFG_REG Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-178. Instance Table

Instance Name	Physical Address
IOMUX	5310 0160h

Figure 2-89. IOMUX_PR0_PRU0_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-179. PR0_PRU0_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.90 IOMUX_PR0_PRU0_GPO10_CFG_REG Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-180. Instance Table

Instance Name	Physical Address
IOMUX	5310 0164h

Figure 2-90. IOMUX_PR0_PRU0_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-181. PR0_PRU0_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.91 IOMUX_PR0_PRU0_GPO8_CFG_REG Register (Offset = 168h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-182. Instance Table

Instance Name	Physical Address
IOMUX	5310 0168h

Figure 2-91. IOMUX_PR0_PRU0_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-183. PR0_PRU0_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.92 IOMUX_PR0_PRU0_GPO6_CFG_REG Register (Offset = 16Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-184. Instance Table

Instance Name	Physical Address
IOMUX	5310 016Ch

Figure 2-92. IOMUX_PR0_PRU0_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-185. PR0_PRU0_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.93 IOMUX_PR0_PRU0_GPO4_CFG_REG Register (Offset = 170h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-186. Instance Table

Instance Name	Physical Address
IOMUX	5310 0170h

Figure 2-93. IOMUX_PR0_PRU0_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-187. PR0_PRU0_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.94 IOMUX_PR0_PRU0_GPO0_CFG_REG Register (Offset = 174h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-188. Instance Table

Instance Name	Physical Address
IOMUX	5310 0174h

Figure 2-94. IOMUX_PR0_PRU0_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-189. PR0_PRU0_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.95 IOMUX_PR0_PRU0_GPO1_CFG_REG Register (Offset = 178h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-190. Instance Table

Instance Name	Physical Address
IOMUX	5310 0178h

Figure 2-95. IOMUX_PR0_PRU0_GPO1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-191. PR0_PRU0_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.96 IOMUX_PR0_PRU0_GPO2_CFG_REG Register (Offset = 17Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-192. Instance Table

Instance Name	Physical Address
IOMUX	5310 017Ch

Figure 2-96. IOMUX_PR0_PRU0_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-193. PR0_PRU0_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.97 IOMUX_PR0_PRU0_GPO3_CFG_REG Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-194. Instance Table

Instance Name	Physical Address
IOMUX	5310 0180h

Figure 2-97. IOMUX_PR0_PRU0_GPO3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-195. PR0_PRU0_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.98 IOMUX_PR0_PRU0_GPO16_CFG_REG Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-196. Instance Table

Instance Name	Physical Address
IOMUX	5310 0184h

Figure 2-98. IOMUX_PR0_PRU0_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-197. PR0_PRU0_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.99 IOMUX_PR0_PRU0_GPO15_CFG_REG Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-198. Instance Table

Instance Name	Physical Address
IOMUX	5310 0188h

Figure 2-99. IOMUX_PR0_PRU0_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-199. PR0_PRU0_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.100 IOMUX_PR0_PRU0_GPO11_CFG_REG Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-200. Instance Table

Instance Name	Physical Address
IOMUX	5310 018Ch

Figure 2-100. IOMUX_PR0_PRU0_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-201. PR0_PRU0_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.101 IOMUX_PR0_PRU0_GPO12_CFG_REG Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-202. Instance Table

Instance Name	Physical Address
IOMUX	5310 0190h

Figure 2-101. IOMUX_PR0_PRU0_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-203. PR0_PRU0_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.102 IOMUX_PR0_PRU0_GPO13_CFG_REG Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-204. Instance Table

Instance Name	Physical Address
IOMUX	5310 0194h

Figure 2-102. IOMUX_PR0_PRU0_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-205. PR0_PRU0_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.103 IOMUX_PR0_PRU0_GPO14_CFG_REG Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-206. Instance Table

Instance Name	Physical Address
IOMUX	5310 0198h

Figure 2-103. IOMUX_PR0_PRU0_GPO14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-207. PR0_PRU0_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.104 IOMUX_PR0_PRU1_GPO5_CFG_REG Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-208. Instance Table

Instance Name	Physical Address
IOMUX	5310 019Ch

Figure 2-104. IOMUX_PR0_PRU1_GPO5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-209. PR0_PRU1_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.105 IOMUX_PR0_PRU1_GPO9_CFG_REG Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-210. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A0h

Figure 2-105. IOMUX_PR0_PRU1_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-211. PR0_PRU1_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.106 IOMUX_PR0_PRU1_GPO10_CFG_REG Register (Offset = 1A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-212. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A4h

Figure 2-106. IOMUX_PR0_PRU1_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-213. PR0_PRU1_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.107 IOMUX_PR0_PRU1_GPO8_CFG_REG Register (Offset = 1A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-214. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A8h

Figure 2-107. IOMUX_PR0_PRU1_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-215. PR0_PRU1_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.108 IOMUX_PR0_PRU1_GPO6_CFG_REG Register (Offset = 1ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-216. Instance Table

Instance Name	Physical Address
IOMUX	5310 01ACh

Figure 2-108. IOMUX_PR0_PRU1_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-217. PR0_PRU1_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.109 IOMUX_PR0_PRU1_GPO4_CFG_REG Register (Offset = 1B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-218. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B0h

Figure 2-109. IOMUX_PR0_PRU1_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-219. PR0_PRU1_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.110 IOMUX_PR0_PRU1_GPO0_CFG_REG Register (Offset = 1B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-220. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B4h

Figure 2-110. IOMUX_PR0_PRU1_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-221. PR0_PRU1_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.111 IOMUX_PR0_PRU1_GPO1_CFG_REG Register (Offset = 1B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-222. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B8h

Figure 2-111. IOMUX_PR0_PRU1_GPO1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-223. PR0_PRU1_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.112 IOMUX_PR0_PRU1_GPO2_CFG_REG Register (Offset = 1BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-224. Instance Table

Instance Name	Physical Address
IOMUX	5310 01BCh

Figure 2-112. IOMUX_PR0_PRU1_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-225. PR0_PRU1_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.113 IOMUX_PR0_PRU1_GPO3_CFG_REG Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-226. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C0h

Figure 2-113. IOMUX_PR0_PRU1_GPO3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-227. PR0_PRU1_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.114 IOMUX_PR0_PRU1_GPO16_CFG_REG Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-228. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C4h

Figure 2-114. IOMUX_PR0_PRU1_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-229. PR0_PRU1_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.115 IOMUX_PR0_PRU1_GPO15_CFG_REG Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-230. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C8h

Figure 2-115. IOMUX_PR0_PRU1_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-231. PR0_PRU1_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.116 IOMUX_PR0_PRU1_GPO11_CFG_REG Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-232. Instance Table

Instance Name	Physical Address
IOMUX	5310 01CCh

Figure 2-116. IOMUX_PR0_PRU1_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-233. PR0_PRU1_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.117 IOMUX_PR0_PRU1_GPO12_CFG_REG Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-234. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D0h

Figure 2-117. IOMUX_PR0_PRU1_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-235. PR0_PRU1_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.118 IOMUX_PR0_PRU1_GPO13_CFG_REG Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-236. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D4h

Figure 2-118. IOMUX_PR0_PRU1_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-237. PR0_PRU1_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.119 IOMUX_PR0_PRU1_GPO14_CFG_REG Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-238. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D8h

Figure 2-119. IOMUX_PR0_PRU1_GPO14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-239. PR0_PRU1_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.120 IOMUX_PR0_PRU1_GPO19_CFG_REG Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-240. Instance Table

Instance Name	Physical Address
IOMUX	5310 01DCh

Figure 2-120. IOMUX_PR0_PRU1_GPO19_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-241. PR0_PRU1_GPO19_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.121 IOMUX_PR0_PRU1_GPO18_CFG_REG Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-242. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E0h

Figure 2-121. IOMUX_PR0_PRU1_GPO18_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-243. PR0_PRU1_GPO18_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.122 IOMUX_EXT_REFCLK0_CFG_REG Register (Offset = 1E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-244. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E4h

Figure 2-122. IOMUX_EXT_REFCLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-245. EXT_REFCLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.123 IOMUX_SDFM0_CLK0_CFG_REG Register (Offset = 1E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-246. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E8h

Figure 2-123. IOMUX_SDFM0_CLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-247. SDFM0_CLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.124 IOMUX_SDFM0_D0_CFG_REG Register (Offset = 1ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-248. Instance Table

Instance Name	Physical Address
IOMUX	5310 01ECh

Figure 2-124. IOMUX_SDFM0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-249. SDFM0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.125 IOMUX_SDFM0_CLK1_CFG_REG Register (Offset = 1F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-250. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F0h

Figure 2-125. IOMUX_SDFM0_CLK1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-251. SDFM0_CLK1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.126 IOMUX_SDFM0_D1_CFG_REG Register (Offset = 1F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-252. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F4h

Figure 2-126. IOMUX_SDFM0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-253. SDFM0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.127 IOMUX_SDFM0_CLK2_CFG_REG Register (Offset = 1F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-254. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F8h

Figure 2-127. IOMUX_SDFM0_CLK2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-255. SDFM0_CLK2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.128 IOMUX_SDFM0_D2_CFG_REG Register (Offset = 1FCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-256. Instance Table

Instance Name	Physical Address
IOMUX	5310 01FCh

Figure 2-128. IOMUX_SDFM0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-257. SDFM0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.129 IOMUX_SDFM0_CLK3_CFG_REG Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-258. Instance Table

Instance Name	Physical Address
IOMUX	5310 0200h

Figure 2-129. IOMUX_SDFM0_CLK3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-259. SDFM0_CLK3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.130 IOMUX_SDFM0_D3_CFG_REG Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-260. Instance Table

Instance Name	Physical Address
IOMUX	5310 0204h

Figure 2-130. IOMUX_SDFM0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-261. SDFM0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.131 IOMUX_EQEP0_A_CFG_REG Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-262. Instance Table

Instance Name	Physical Address
IOMUX	5310 0208h

Figure 2-131. IOMUX_EQEP0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-263. EQEP0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.132 IOMUX_EQEP0_B_CFG_REG Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-264. Instance Table

Instance Name	Physical Address
IOMUX	5310 020Ch

Figure 2-132. IOMUX_EQEP0_B_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-265. EQEP0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.133 IOMUX_EQEP0_STROBE_CFG_REG Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-266. Instance Table

Instance Name	Physical Address
IOMUX	5310 0210h

Figure 2-133. IOMUX_EQEP0_STROBE_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-267. EQEP0_STROBE_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.134 IOMUX_EQEP0_INDEX_CFG_REG Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-268. Instance Table

Instance Name	Physical Address
IOMUX	5310 0214h

Figure 2-134. IOMUX_EQEP0_INDEX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-269. EQEP0_INDEX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.135 IOMUX_I2C0_SDA_CFG_REG Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-270. Instance Table

Instance Name	Physical Address
IOMUX	5310 0218h

Figure 2-135. IOMUX_I2C0_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-271. I2C0_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.136 IOMUX_I2C0_SCL_CFG_REG Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-272. Instance Table

Instance Name	Physical Address
IOMUX	5310 021Ch

Figure 2-136. IOMUX_I2C0_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-273. I2C0_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.137 IOMUX_MCAN2_TX_CFG_REG Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-274. Instance Table

Instance Name	Physical Address
IOMUX	5310 0220h

Figure 2-137. IOMUX_MCAN2_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-275. MCAN2_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

ADVANCE INFORMATION

2.3.138 IOMUX_MCAN2_RX_CFG_REG Register (Offset = 224h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-276. Instance Table

Instance Name	Physical Address
IOMUX	5310 0224h

Figure 2-138. IOMUX_MCAN2_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	1	1	1	1	111			

Access Types Legend

Table 2-277. MCAN2_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Function select

2.3.139 IOMUX_CLKOUT0_CFG_REG Register (Offset = 228h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-278. Instance Table

Instance Name	Physical Address
IOMUX	5310 0228h

Figure 2-139. IOMUX_CLKOUT0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSMASTER	HSMODE	RESERVED									INP_INV_SEL	QUAL_SEL		GPIO_SEL	
RW	RW	NONE									RW	RW		RW	
0	0	0									0	0		0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
NONE					RW	RW	RW	RW	RW	RW	RW	RW			
0					1	0	1	0	1	1	1	0			

Access Types Legend

Table 2-279. CLKOUT0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	select value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19 - 18	QUAL_SEL	RW	0h	select value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	0h	Function select

2.3.140 IOMUX_WARMRSTN_CFG_REG Register (Offset = 22Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-280. Instance Table

Instance Name	Physical Address
IOMUX	5310 022Ch

Figure 2-140. IOMUX_WARMRSTN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	0	1	0	0	0	1	0			

Access Types Legend

Table 2-281. WARMRSTN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.141 IOMUX_SAFETY_ERRORN_CFG_REG Register (Offset = 230h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-282. Instance Table

Instance Name	Physical Address
IOMUX	5310 0230h

Figure 2-141. IOMUX_SAFETY_ERRORN_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					RESERVED										
RO					NONE										
0					0										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	0	0	0	0	0	1	0			

Access Types Legend

Table 2-283. SAFETY_ERRORN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.142 IOMUX_TDI_CFG_REG Register (Offset = 234h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-284. Instance Table

Instance Name	Physical Address
IOMUX	5310 0234h

Figure 2-142. IOMUX_TDI_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	1	0	1	1	0	1	0			

Access Types Legend

Table 2-285. TDI_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.143 IOMUX_TDO_CFG_REG Register (Offset = 238h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-286. Instance Table

Instance Name	Physical Address
IOMUX	5310 0238h

Figure 2-143. IOMUX_TDO_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	1	0	0	0	1	1	0			

Access Types Legend

Table 2-287. TDO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.144 IOMUX_TMS_CFG_REG Register (Offset = 23Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-288. Instance Table

Instance Name	Physical Address
IOMUX	5310 023Ch

Figure 2-144. IOMUX_TMS_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	1	0	0	0	0	1	0			

Access Types Legend

Table 2-289. TMS_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.145 IOMUX_TCK_CFG_REG Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-290. Instance Table

Instance Name	Physical Address
IOMUX	5310 0240h

Figure 2-145. IOMUX_TCK_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					0	1	0	0	0	0	1	0			

Access Types Legend

Table 2-291. TCK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	0h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	1h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.146 IOMUX_QSPI0_CLKLB_CFG_REG Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-292. Instance Table

Instance Name	Physical Address
IOMUX	5310 0244h

Figure 2-146. IOMUX_QSPI0_CLKLB_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SC1	PUPDSEL	PI	OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
NONE					RW	RW	RW	RW	RW	RW	RW	NONE			
0					1	0	1	1	1	1	1	0			

Access Types Legend

Table 2-293. QSPI0_CLKLB_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control : 0 : higher slew rate. 1: Lower slew rate.
9	PUPDSEL	RW	0h	Pullup/PullDown Selection 0 -- Pull Down 1 - Pull Up
8	PI	RW	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

2.3.147 IOMUX_QUAL_GRP_0_CFG_REG Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-294. Instance Table

Instance Name	Physical Address
IOMUX	5310 0248h

Figure 2-147. IOMUX_QUAL_GRP_0_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-295. QUAL_GRP_0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.148 IOMUX_QUAL_GRP_1_CFG_REG Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-296. Instance Table

Instance Name	Physical Address
IOMUX	5310 024Ch

Figure 2-148. IOMUX_QUAL_GRP_1_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-297. QUAL_GRP_1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.149 IOMUX_QUAL_GRP_2_CFG_REG Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-298. Instance Table

Instance Name	Physical Address
IOMUX	5310 0250h

Figure 2-149. IOMUX_QUAL_GRP_2_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-299. QUAL_GRP_2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.150 IOMUX_QUAL_GRP_3_CFG_REG Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-300. Instance Table

Instance Name	Physical Address
IOMUX	5310 0254h

Figure 2-150. IOMUX_QUAL_GRP_3_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-301. QUAL_GRP_3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.151 IOMUX_QUAL_GRP_4_CFG_REG Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-302. Instance Table

Instance Name	Physical Address
IOMUX	5310 0258h

Figure 2-151. IOMUX_QUAL_GRP_4_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-303. QUAL_GRP_4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.152 IOMUX_QUAL_GRP_5_CFG_REG Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-304. Instance Table

Instance Name	Physical Address
IOMUX	5310 025Ch

Figure 2-152. IOMUX_QUAL_GRP_5_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-305. QUAL_GRP_5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.153 IOMUX_QUAL_GRP_6_CFG_REG Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-306. Instance Table

Instance Name	Physical Address
IOMUX	5310 0260h

Figure 2-153. IOMUX_QUAL_GRP_6_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-307. QUAL_GRP_6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.154 IOMUX_QUAL_GRP_7_CFG_REG Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-308. Instance Table

Instance Name	Physical Address
IOMUX	5310 0264h

Figure 2-154. IOMUX_QUAL_GRP_7_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-309. QUAL_GRP_7_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.155 IOMUX_QUAL_GRP_8_CFG_REG Register (Offset = 268h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-310. Instance Table

Instance Name	Physical Address
IOMUX	5310 0268h

Figure 2-155. IOMUX_QUAL_GRP_8_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-311. QUAL_GRP_8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.156 IOMUX_QUAL_GRP_9_CFG_REG Register (Offset = 26Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-312. Instance Table

Instance Name	Physical Address
IOMUX	5310 026Ch

Figure 2-156. IOMUX_QUAL_GRP_9_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-313. QUAL_GRP_9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.157 IOMUX_QUAL_GRP_10_CFG_REG Register (Offset = 270h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-314. Instance Table

Instance Name	Physical Address
IOMUX	5310 0270h

Figure 2-157. IOMUX_QUAL_GRP_10_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-315. QUAL_GRP_10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.158 IOMUX_QUAL_GRP_11_CFG_REG Register (Offset = 274h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-316. Instance Table

Instance Name	Physical Address
IOMUX	5310 0274h

Figure 2-158. IOMUX_QUAL_GRP_11_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-317. QUAL_GRP_11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.159 IOMUX_QUAL_GRP_12_CFG_REG Register (Offset = 278h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-318. Instance Table

Instance Name	Physical Address
IOMUX	5310 0278h

Figure 2-159. IOMUX_QUAL_GRP_12_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-319. QUAL_GRP_12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.160 IOMUX_QUAL_GRP_13_CFG_REG Register (Offset = 27Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-320. Instance Table

Instance Name	Physical Address
IOMUX	5310 027Ch

Figure 2-160. IOMUX_QUAL_GRP_13_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-321. QUAL_GRP_13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.161 IOMUX_QUAL_GRP_14_CFG_REG Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-322. Instance Table

Instance Name	Physical Address
IOMUX	5310 0280h

Figure 2-161. IOMUX_QUAL_GRP_14_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-323. QUAL_GRP_14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.162 IOMUX_QUAL_GRP_15_CFG_REG Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-324. Instance Table

Instance Name	Physical Address
IOMUX	5310 0284h

Figure 2-162. IOMUX_QUAL_GRP_15_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-325. QUAL_GRP_15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.163 IOMUX_QUAL_GRP_16_CFG_REG Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-326. Instance Table

Instance Name	Physical Address
IOMUX	5310 0288h

Figure 2-163. IOMUX_QUAL_GRP_16_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RESERVED							
RO								NONE							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-327. QUAL_GRP_16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.164 IOMUX_QUAL_GRP_17_CFG_REG Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-328. Instance Table

Instance Name	Physical Address
IOMUX	5310 028Ch

Figure 2-164. IOMUX_QUAL_GRP_17_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUAL_PERIOD_PER_SAMPLE							
NONE								RW							
0								0							

Access Types Legend

Table 2-329. QUAL_GRP_17_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

2.3.165 IOMUX_USER_MODE_EN Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-330. Instance Table

Instance Name	Physical Address
IOMUX	5310 0290h

Figure 2-165. IOMUX_USER_MODE_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
USER_MODE_EN															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_MODE_EN															
RW															
0															

Access Types Legend

Table 2-331. USER_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	USER_MODE_EN	RW	0h	Write 0XADADADAD to enable user mode write access to IO CFG space

2.3.166 IOMUX_PADGLBL_CFG_REG Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

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Table 2-332. Instance Table

Instance Name	Physical Address
IOMUX	5310 0294h

Figure 2-166. IOMUX_PADGLBL_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PADGLBL_CFG_REG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PADGLBL_CFG_REG															
RW															
0															

Access Types Legend

Table 2-333. PADGLBL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PADGLBL_CFG_REG	RW	0h	2:0 : global_ie_n_ctl - Write 3'b111 to pass global_ie_n_val to IE_N/RXACTIVE_N pin of all the IOs.3 : global_ie_n_val - Active low10:8 : global_oe_n_ctl - Write 3'b111 to pass global_oe_n_val to OE_N/GZ pin of all the IOs.11 : global_oe_n_val - Active low18:16 : global_pi_ctl - Write 3'b111 to pass global_pi_val and global_pu_val to all the IOs19 : global_pi_val20 : global_pu_val

2.3.167 IOMUX_IO_CFG_KICK0 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

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Table 2-334. Instance Table

Instance Name	Physical Address
IOMUX	5310 0298h

Figure 2-167. IOMUX_IO_CFG_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IO_CFG_KICK0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_CFG_KICK0															
RW															
0															

Access Types Legend

Table 2-335. IO_CFG_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IO_CFG_KICK0	RW	0h	Kicker 0 Register. The value 83E7 0B13h must be written to KICK0 as part of the process to unlock the CPU.write access to the above PIN MUX registers (including IOCFGKICK1)

2.3.168 IOMUX_IO_CFG_KICK1 Register (Offset = 29Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-336. Instance Table

Instance Name	Physical Address
IOMUX	5310 029Ch

Figure 2-168. IOMUX_IO_CFG_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IO_CFG_KICK1															
RW															
11000001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_CFG_KICK1															
RW															
11000001															

Access Types Legend

Table 2-337. IO_CFG_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IO_CFG_KICK1	RW	A7D8C1h	Kicker 1 Register. The value 95A4 F1E0h must be written to the KICK1 as part of the process to unlock the CPU write access to above PINMUX registers (excluding IOCFGKICK0). IOCFGKICK0 has to be written with 83E70B13h to enable access to IOCFGKICK1.

Table 2-338. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined

2.4 MSS_TOPRCM Registers

Table 2-339. TOP_RCM, TOP_RCM_TOP_RCM Registers, Base Address=5320 0000H, Length=4

Offset	Length	Acronym	Register Name	TOP_RCM Physical Address
0h	32	TOP_RCM_PID	PID register	5320 0000h
4h	32	TOP_RCM_WARM_RESET_CONFIG	RW	5320 0004h
8h	8	TOP_RCM_WARM_RESET_REQ	RW	5320 0008h
Ch	16	TOP_RCM_WARM_RST_CAUSE	RO	5320 000Ch
10h	8	TOP_RCM_WARM_RST_CAUSE_CLR	RW	5320 0010h
14h	8	TOP_RCM_RCOSC32K_CTRL	RW	5320 0014h
18h	16	TOP_RCM_LIMP_MODE_EN	RW	5320 0018h
1Ch	8	TOP_RCM_PLL_REF_CLK_SRC_SEL	RW	5320 001Ch
20h	8	TOP_RCM_PAD_XTAL_CTRL	RW	5320 0020h
24h	32	TOP_RCM_SOP_MODE_VALUE	RO	5320 0024h
28h	8	TOP_RCM_CLK_LOSS_STATUS	RO	5320 0028h
30h	16	TOP_RCM_WARM_RSTTIME1	RW	5320 0030h
34h	16	TOP_RCM_WARM_RSTTIME2	RW	5320 0034h
38h	16	TOP_RCM_WARM_RSTTIME3	RW	5320 0038h
400h	8	TOP_RCM_PLL_CORE_PWRCTRL	RW	5320 0400h
404h	32	TOP_RCM_PLL_CORE_CLKCTRL	RW	5320 0404h
408h	0	TOP_RCM_PLL_CORE_TENABLE	RW	5320 0408h
40Ch	0	TOP_RCM_PLL_CORE_TENABLEDIV	RW	5320 040Ch
410h	24	TOP_RCM_PLL_CORE_M2NDIV	RW	5320 0410h
414h	24	TOP_RCM_PLL_CORE_MN2DIV	RW	5320 0414h
418h	32	TOP_RCM_PLL_CORE_FRACDIV	RW	5320 0418h
41Ch	8	TOP_RCM_PLL_CORE_BWCTRL	RW	5320 041Ch
420h	32	TOP_RCM_PLL_CORE_FRACCTRL	RW	5320 0420h
424h	32	TOP_RCM_PLL_CORE_STATUS	RO	5320 0424h
428h	24	TOP_RCM_PLL_CORE_HSDIVIDER	RW	5320 0428h
42Ch	16	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0	RW	5320 042Ch
430h	16	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1	RW	5320 0430h
434h	16	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2	RW	5320 0434h
43Ch	8	TOP_RCM_PLL_CORE_RSTCTRL	RW	5320 043Ch
440h	8	TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL	RW	5320 0440h
500h	16	TOP_RCM_R5SS_CLK_SRC_SEL	RW	5320 0500h
504h	8	TOP_RCM_R5SS_CLK_STATUS	RO	5320 0504h
510h	8	TOP_RCM_R5SS0_CLK_DIV_SEL	RW	5320 0510h
514h	8	TOP_RCM_R5SS1_CLK_DIV_SEL	RW	5320 0514h
518h	8	TOP_RCM_R5SS0_CLK_GATE	RW	5320 0518h
51Ch	8	TOP_RCM_R5SS1_CLK_GATE	RW	5320 051Ch
520h	16	TOP_RCM_SYS_CLK_DIV_VAL	RW	5320 0520h

Table 2-339. TOP_RCM, TOP_RCM_TOP_RCM Registers, Base Address=5320 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	TOP_RCM Physical Address
524h	8	TOP_RCM_SYS_CLK_GATE	RW	5320 0524h
528h	16	TOP_RCM_SYS_CLK_STATUS	RO	5320 0528h
800h	8	TOP_RCM_PLL_PER_PWRCTRL	RW	5320 0800h
804h	32	TOP_RCM_PLL_PER_CLKCTRL	RW	5320 0804h
808h	0	TOP_RCM_PLL_PER_TENABLE	RW	5320 0808h
80Ch	0	TOP_RCM_PLL_PER_TENABLEDIV	RW	5320 080Ch
810h	24	TOP_RCM_PLL_PER_M2NDIV	RW	5320 0810h
814h	24	TOP_RCM_PLL_PER_MN2DIV	RW	5320 0814h
818h	32	TOP_RCM_PLL_PER_FRACDIV	RW	5320 0818h
81Ch	8	TOP_RCM_PLL_PER_BWCTRL	RW	5320 081Ch
820h	32	TOP_RCM_PLL_PER_FRACCTRL	RW	5320 0820h
824h	32	TOP_RCM_PLL_PER_STATUS	RO	5320 0824h
828h	24	TOP_RCM_PLL_PER_HSDIVIDER	RW	5320 0828h
82Ch	16	TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0	RW	5320 082Ch
830h	16	TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1	RW	5320 0830h
83Ch	8	TOP_RCM_PLL_PER_RSTCTRL	RW	5320 083Ch
840h	8	TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL	RW	5320 0840h
C00h	16	TOP_RCM_CLKOUT0_CLK_SRC_SEL	RW	5320 0C00h
C04h	16	TOP_RCM_CLKOUT1_CLK_SRC_SEL	RW	5320 0C04h
C08h	16	TOP_RCM_CLKOUT0_DIV_VAL	RW	5320 0C08h
C0Ch	16	TOP_RCM_CLKOUT1_DIV_VAL	RW	5320 0C0Ch
C10h	8	TOP_RCM_CLKOUT0_CLK_GATE	RW	5320 0C10h
C14h	8	TOP_RCM_CLKOUT1_CLK_GATE	RW	5320 0C14h
C18h	16	TOP_RCM_CLKOUT0_CLK_STATUS	RO	5320 0C18h
C1Ch	16	TOP_RCM_CLKOUT1_CLK_STATUS	RO	5320 0C1Ch
C20h	16	TOP_RCM_TRCCLKOUT_CLK_SRC_SEL	RW	5320 0C20h
C24h	16	TOP_RCM_TRCCLKOUT_DIV_VAL	RW	5320 0C24h
C28h	8	TOP_RCM_TRCCLKOUT_CLK_GATE	RW	5320 0C28h
C2Ch	16	TOP_RCM_TRCCLKOUT_CLK_STATUS	RO	5320 0C2Ch
D00h	32	TOP_RCM_DFT_DMLED_EXEC	RW	5320 0D00h
D04h	32	TOP_RCM_DFT_DMLED_STATUS	RW	5320 0D04h
E00h	32	TOP_RCM_HW_REG0	RW	5320 0E00h
E04h	32	TOP_RCM_HW_REG1	RW	5320 0E04h
E08h	32	TOP_RCM_HW_REG2	RW	5320 0E08h
E0Ch	32	TOP_RCM_HW_REG3	RW	5320 0E0Ch
FD0h	32	TOP_RCM_HW_SPARE_RW0	RW	5320 0FD0h
FD4h	32	TOP_RCM_HW_SPARE_RW1	RW	5320 0FD4h
FD8h	32	TOP_RCM_HW_SPARE_RW2	RW	5320 0FD8h
FDCh	32	TOP_RCM_HW_SPARE_RW3	RW	5320 0FDCh
FE0h	32	TOP_RCM_HW_SPARE_RO0	RO	5320 0FE0h
FE4h	32	TOP_RCM_HW_SPARE_RO1	RO	5320 0FE4h
FE8h	32	TOP_RCM_HW_SPARE_RO2	RO	5320 0FE8h
FECh	32	TOP_RCM_HW_SPARE_RO3	RO	5320 0FECh
FF0h	32	TOP_RCM_HW_SPARE_WPH	RW	5320 0FF0h

Table 2-339. TOP_RCM, TOP_RCM_TOP_RCM Registers, Base Address=5320 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	TOP_RCM Physical Address
FF4h	32	TOP_RCM_HW_SPARE_REC	RW	5320 0FF4h
1008h	32	TOP_RCM_LOCK0_KICK0	- KICK0 component	5320 1008h
100Ch	32	TOP_RCM_LOCK0_KICK1	- KICK1 component	5320 100Ch
1010h	8	TOP_RCM_INTR_RAW_STATUS	Interrupt Raw Status/Set Register	5320 1010h
1014h	8	TOP_RCM_INTR_ENABLED_STATUS_CLEAR	Interrupt Enabled Status/Clear register	5320 1014h
1018h	8	TOP_RCM_INTR_ENABLE	Interrupt Enable register	5320 1018h
101Ch	8	TOP_RCM_INTR_ENABLE_CLEAR	Interrupt Enable Clear register	5320 101Ch
1020h	8	TOP_RCM_EOI	EOI register	5320 1020h
1024h	32	TOP_RCM_FAULT_ADDRESS	Fault Address register	5320 1024h
1028h	8	TOP_RCM_FAULT_TYPE_STATUS	Fault Type Status register	5320 1028h
102Ch	32	TOP_RCM_FAULT_ATTR_STATUS	Fault Attribute Status register	5320 102Ch
1030h	0	TOP_RCM_FAULT_CLEAR	Fault Clear register	5320 1030h

2.4.1 TOP_RCM_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 2-340. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0000h

Figure 2-169. TOP_RCM_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 2-341. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

2.4.2 TOP_RCM_WARM_RESET_CONFIG Register (Offset = 4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-342. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0004h

Figure 2-170. TOP_RCM_WARM_RESET_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	WDOG3_RST_EN			RESERVED	WDOG2_RST_EN			RESERVED	WDOG1_RST_EN			RESERVED	WDOG0_RST_EN		
NONE	RW			NONE	RW			NONE	RW			NONE	RW		
0	111			0	111			0	111			0	111		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	TSENSE1_RST_EN			RESERVED	TSENSE0_RST_EN			RESERVED	DEBUGSS_RST_EN			RESERVED	PAD_BYPASS		
NONE	RW			NONE	RW			NONE	RW			NONE	RW		
0	111			0	111			0	111			0	111		

Access Types Legend

Table 2-343. WARM_RESET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	WDOG3_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
26 - 24	WDOG2_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
22 - 20	WDOG1_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
18 - 16	WDOG0_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
14 - 12	TSENSE1_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable temperature sensor 1 on Warm reset Write 3'b111 to enable temperature sensor 1l on Warm reset
	RESERVED	NONE		Reserved
10 - 8	TSENSE0_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable temperature sensor 0 control on Warm reset Write 3'b111 to enable temperature sensor 0 control on Warm reset
	RESERVED	NONE		Reserved
6 - 4	DEBUGSS_RST_EN	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to disable debugger control on Warm reset Write 3'b111 enable debugger to control Warm reset
	RESERVED	NONE		Reserved

Table 2-343. WARM_RESET_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	PAD_BYPASS	RW	6Fh	Bypass the Warm reset from Pad InputData should be loaded as multibit. Write 3'b000 : Pad Warm Reset pin has control over warm resetWrite 3'b111 : Pad warm reset pin has no control on warm reset

2.4.3 TOP_RCM_WARM_RESET_REQ Register (Offset = 8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-344. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0008h

Figure 2-171. TOP_RCM_WARM_RESET_REQ Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SW_RST	
NONE						RW	
0						111	

Access Types Legend

Table 2-345. WARM_RESET_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SW_RST	RW	6Fh	Data should be loaded as multibit. Write 3'b000 to assert warm reset from SWWrite 3'b111 to deassert warm reset from SW if this is the only source of warm reset

2.4.4 TOP_RCM_WARM_RST_CAUSE Register (Offset = Ch) [reset = h]

Short Description: RO

Long Description:

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Table 2-346. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 000Ch

Figure 2-172. TOP_RCM_WARM_RST_CAUSE Name Register

15	14	13	12	11	10	9	8
RESERVED				CAUSE			
NONE				RO			
0				1000001			
7	6	5	4	3	2	1	0
CAUSE							
RO							
1000001							

Access Types Legend

Table 2-347. WARM_RST_CAUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CAUSE	RO	F4241h	System Reset Cause register12'b0000_0100_0001 - POR reset12'b0000_0100_0010 - Warm reset due to MSS_WDT012'b0000_0100_0100 - Warm reset due to MSS_WDT112'b0000_0100_1000 - Warm reset due to MSS_WDT212'b0000_0101_0000 - Warm reset due to MSS_WDT312'b0000_0110_0000 - Warm reset due to TOP_RMC:WARM_RESET_REQ12'b0000_0100_0000 - External Pad reset12'b0000_1100_0000 - Warm reset due to HSM_WDT12'b0001_0100_0000 - Warm Reset due to Deugger reset12'b0010_0100_0000 - Warm Reset due to Temp Sense0 Reset12'b0100_0100_0000 - Warm Reset due to Temp Sense1 Reset

2.4.5 TOP_RCM_WARM_RST_CAUSE_CLR Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

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Table 2-348. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0010h

Figure 2-173. TOP_RCM_WARM_RST_CAUSE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLEAR	
NONE						RW	
0						0	

Access Types Legend

Table 2-349. WARM_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLEAR	RW	0h	Write pulse bit field: Data should be loaded as multibit. System Reset Cause register Clear

2.4.6 TOP_RCM_RCOSC32K_CTRL Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

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Table 2-350. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0014h

Figure 2-174. TOP_RCM_RCOSC32K_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					STOPOSC		
NONE					RW		
0					0		

Access Types Legend

Table 2-351. RCOSC32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	STOPOSC	RW	0h	Stop 32KHz RCOSC. Write 3'b111 to stop clock

2.4.7 TOP_RCM_LIMP_MODE_EN Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

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Table 2-352. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0018h

Figure 2-175. TOP_RCM_LIMP_MODE_EN Name Register

15	14	13	12	11	10	9	8
RESERVED						COREPLL_LOSS_EN	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
RESERVED	XTALCLK_LOSS_EN			RESERVED	DCC0_ERROR_EN		
NONE	RW			NONE	RW		
0	0			0	0		

Access Types Legend

Table 2-353. LIMP_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	COREPLL_LOSS_EN	RW	0h	Enable for core pll phase lock loss to generate Limp mode3'b000: will not generate Limp mode (multibit 000)3'b111 : will generate Limp mode (multibit 111)
	RESERVED	NONE		Reserved
6 - 4	XTALCLK_LOSS_EN	RW	0h	Enable for crystal_clock_loss to generate Limp mode3'b000: will not generate Limp mode (multibit 000)3'b111 : will generate Limp mode (multibit 111)
	RESERVED	NONE		Reserved
2 - 0	DCC0_ERROR_EN	RW	0h	Enable DCC0 Error to generate Limp mode 3'b000: DCC0 Error will not generate Limp mode (multibit 000)3'b111 : DCC0 Error will generate Limp mode (multibit 111)

2.4.8 TOP_RCM_PLL_REF_CLK_SRC_SEL Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-354. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 001Ch

Figure 2-176. TOP_RCM_PLL_REF_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	PLL_PERI_REF_CLK_SRC_SEL			RESERVED	PLL_CORE_REF_CLK_SRC_SEL		
NONE	RW			NONE	RW		
0	0			0	0		

Access Types Legend

Table 2-355. PLL_REF_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6 - 4	PLL_PERI_REF_CLK_SRC_SEL	RW	0h	Mux selct for PERI PLL REF clockWrite 3'b111 : to select external reference clock as PLL reference clockWrite 3'b000 : to select on-die clock as PLL reference clock
	RESERVED	NONE		Reserved
2 - 0	PLL_CORE_REF_CLK_SRC_SEL	RW	0h	Mux selct for CORE PLL REF clockWrite 3'b111 : to select external reference clock as PLL reference clockWrite 3'b000 : to select on-die clock as PLL reference clock

2.4.9 TOP_RCM_PAD_XTAL_CTRL Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

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Table 2-356. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0020h

Figure 2-177. TOP_RCM_PAD_XTAL_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				XTAL_XI_OE_N	XTAL_XO_RESSELECT	XTAL_XO_SW2	XTAL_XO_SW1
NONE				RW	RW	RW	RW
0				0	0	0	1

Access Types Legend

Table 2-357. PAD_XTAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	XTAL_XI_OE_N	RW	0h	When gz is low, the padxo output is enabled, padxi to padxo is a single stage inverter, and the oscillator can oscillate with an external crystal plus capacitors/resistor. When gz is high, padxo is in high impedance mode, padxi and Y are driven low, and the oscillator is disabled. With gz high, the internal bias resistor between padxi and padxo is disconnected regardless of the state of resselect.
2	XTAL_XO_RESSELECT	RW	0h	When resselect is low, an internal 1Meg Ohm resistor is connected between padxi and padxo for oscillator bias. When resselect is asserted (high), the internal resistor is disconnected. For oscillation with a crystal while resselect is high, an external resistor must be connected between padxi and padxo to provide bias.
1	XTAL_XO_SW2	RW	0h	XTAL pad control bit frequency selection pin SW2 Based on table belowsw2 sw1 Freq of operation0 0 5 20 MHz0 1 15 35 MHz1 0 30 40 MHz1 1 40 55 MHz
0	XTAL_XO_SW1	RW	1h	XTAL pad control bit frequency selection pin SW1 Based on table belowsw2 sw1 Freq of operation0 0 5 20 MHz0 1 15 35 MHz1 0 30 40 MHz1 1 40 55 MHz

2.4.10 TOP_RCM_SOP_MODE_VALUE Register (Offset = 24h) [reset = h]

Short Description: RO

Long Description:

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Table 2-358. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0024h

Figure 2-178. TOP_RCM_SOP_MODE_VALUE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RO															
0															

Access Types Legend

Table 2-359. SOP_MODE_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	See below table SOP_MODE values and its corresponding mappingSOP_PAD3 SOP_PAD2 SOP_PAD1 SOP_PAD0 bootmode 0 0 0 0 QSPI Functional mode(4S) 0 0 0 1 UART Functional mode 0 0 1 0 QSPI Functional mode(1S) values from 3 to 7 is reserved for future use 1 0 0 0 THB(test) mode 1 0 0 1 ATPG mode 1 0 1 0 FLED mode (Debug SoP mode) values from B to F is reserved for future use reset value of MMR is 0 but it will latch on to the SOP mode values after reset is released. when CPU reads the MMR it will show the latched SOP mode value only

2.4.11 TOP_RCM_CLK_LOSS_STATUS Register (Offset = 28h) [reset = h]

Short Description: RO

Long Description:

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Table 2-360. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0028h

Figure 2-179. TOP_RCM_CLK_LOSS_STATUS Name Register

15	14	13	12	11	10	9	8
RC_GOOD_BOOT							
RO							
1							

7	6	5	4	3	2	1	0
RESERVED			RC_CLOCK_LOSS	RESERVED			CRYSTAL_CLOCK_LOSS
NONE			RO	NONE			RO
0			0	0			0

Access Types Legend

Table 2-361. CLK_LOSS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RC_GOOD_BOOT	RO	1h	Clock status of RC clock at boot. Reset value will reflect the actual status1 --> clock present at boot0 --> clock not present at boot
	RESERVED	NONE		Reserved
4	RC_CLOCK_LOSS	RO	0h	Coarse detection clock loss status for RC clock. Reset value will reflect the actual status1 --> clock lost0 --> clock good
	RESERVED	NONE		Reserved
0	CRYSTAL_CLOCK_LOSS	RO	0h	Coarse detection clock loss status for Crystal clock. Reset value will reflect the actual status1 --> clock lost0 --> clock good

2.4.12 TOP_RCM_WARM_RSTTIME1 Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-362. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0030h

Figure 2-180. TOP_RCM_WARM_RSTTIME1 Name Register

15	14	13	12	11	10	9	8
RESERVED				DELAY			
NONE				RW			
0				100010001000			
7	6	5	4	3	2	1	0
DELAY							
RW							
100010001000							

Access Types Legend

Table 2-363. WARM_RSTTIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	17490F8268h	programing Output delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.13 TOP_RCM_WARM_RSTTIME2 Register (Offset = 34h) [reset = h]

Short Description: RW

Long Description:

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Table 2-364. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0034h

Figure 2-181. TOP_RCM_WARM_RSTTIME2 Name Register

15	14	13	12	11	10	9	8
RESERVED				DELAY			
NONE				RW			
0				100010001000			
7	6	5	4	3	2	1	0
DELAY							
RW							
100010001000							

Access Types Legend

Table 2-365. WARM_RSTTIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	17490F8268h	programing input Rise delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.14 TOP_RCM_WARM_RSTTIME3 Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-366. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0038h

Figure 2-182. TOP_RCM_WARM_RSTTIME3 Name Register

15	14	13	12	11	10	9	8
RESERVED				DELAY			
NONE				RW			
0				100010001			
7	6	5	4	3	2	1	0
DELAY							
RW							
100010001							

Access Types Legend

Table 2-367. WARM_RSTTIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	5F60811h	programing Input Fall delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.15 TOP_RCM_PLL_CORE_PWRCTRL Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-368. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0400h

Figure 2-183. TOP_RCM_PLL_CORE_PWRCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED		PONIN	PGOODIN	RET	ISORET	ISOSCAN	OFFMODE
NONE		RW	RW	RW	RW	RW	RW
0		1	1	0	0	0	0

Access Types Legend

Table 2-369. PLL_CORE_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	PONIN	RW	1h	ON/OFF control of the weak power switch digital. For functionalmode it should be 1
4	PGOODIN	RW	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1
3	RET	RW	0h	Save/Restore control for Retention mode. For functional mode itshould be 0
2	ISORET	RW	0h	Save/Restore control for Isolation of output pins For functional modeit should be 0
1	ISOSCAN	RW	0h	Save/Restore control for Isolation of the Scanout pins. For functionalmode it should be 0
0	OFFMODE	RW	0h	Used to switch OFF the logic on VDDA. For functional mode itshould be 0

2.4.16 TOP_RCM_PLL_CORE_CLKCTRL Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

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Table 2-370. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0404h

Figure 2-184. TOP_RCM_PLL_CORE_CLKCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CYCLESLIPEN	ENSSC	CLKDCOLDOEN	RESERVED					IDLE	BYPASSACKZ	STBYRET	CLKOUTEN	CLKOUTLDOEN	ULOWCLKEN	CLKDCOLDOPWDNZ	M2PWDNZ
RW	RW	RW	NONE					RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0					1	0	0	0	1	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	STOPMODE	RESERVED	SELFREQDCO			RESERVED	RELAXED_LOCK	RESERVED						SSCTYPE	TINTZ
NONE	RW	NONE	RW			NONE	RW	NONE						RW	RW
0	1	0	100			0	0	0						0	0

Access Types Legend

Table 2-371. PLL_CORE_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CYCLESLIPEN	RW	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK.
30	ENSSC	RW	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading.
29	CLKDCOLDOEN	RW	0h	Synchronously enables/disables CLKDCOLDO0x0 : synchronously disables CLKDCOLDO0x1 : synchronously enables CLKDCOLDO
	RESERVED	NONE		Reserved
23	IDLE	RW	1h	Sets PLL to Idle mode0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go toActive and Locked0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go toIdle Bypass low powe
22	BYPASSACKZ	RW	0h	BYPASSACKZ is a special purpose input to the module. In generalthis input is expected to be tied to static low. For the output clocks ofthe module that do not have an internal bypass mux viz.CLKDCOLDO and CLKOUTLDO, a bypass mux could beimplemented external to the module.
21	STBYRET	RW	0h	Standby retention control0x0 : prepares ADPLLLJ for relock when out of retention byremoving the gating on all internal clocks.0x1 : prepares ADPLLLJ for retention by gating all the internalclocks.
20	CLKOUTEN	RW	0h	CLKOUT enable or disable0x0 : synchronously disables CLKOUT0x1 : synchronously enables CLKOUT
19	CLKOUTLDOEN	RW	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	ULOWCLKEN	RW	0h	Select CLKOUT source in bypass0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1)0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	CLKDCOLDOPWDNZ	RW	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	M2PWDNZ	RW	1h	M2 divider power down mode0x0: Asynchronous power down for M2 divider0x1 : M2 divider is functional

Table 2-371. PLL_CORE_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
14	STOPMODE	RW	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
	RESERVED	NONE		Reserved
12 - 10	SELFREQDCO	RW	64h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency rangeselector.0x0: Reserved0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz0x3: Reserved0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz0x5: Reserved
	RESERVED	NONE		Reserved
8	RELAXED_LOCK	RW	0h	Decides when FREQLOCK asserted0x0: FREQLOCK asserted when DC frequency error less than 1%0x1: FREQLOCK asserted when DC frequency error less than 2%
	RESERVED	NONE		Reserved
1	SSCTYPE	RW	0h	SSC Type
0	TINTZ	RW	0h	PLL core soft reset

2.4.17 TOP_RCM_PLL_CORE_TENABLE Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

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Table 2-372. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0408h

Figure 2-185. TOP_RCM_PLL_CORE_TENABLE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
TENABLE							
RW							
0							

Access Types Legend

Table 2-373. PLL_CORE_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLE	RW	0h	M, N. SD and SELFREQDCO latch (active rise edge)

2.4.18 TOP_RCM_PLL_CORE_TENABLEDIV Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-374. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 040Ch

Figure 2-186. TOP_RCM_PLL_CORE_TENABLEDIV Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
TENABLEDIV							
RW							
0							

Access Types Legend

Table 2-375. PLL_CORE_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLEDIV	RW	0h	M2 and N2 latch (active rise edge)

2.4.19 TOP_RCM_PLL_CORE_M2NDIV Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-376. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0410h

Figure 2-187. TOP_RCM_PLL_CORE_M2NDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	M2														
NONE	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								N							
NONE								RW							
0								10011							

Access Types Legend

Table 2-377. PLL_CORE_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 16	M2	RW	0h	Post-divider is REGM2
	RESERVED	NONE		Reserved
7 - 0	N	RW	271Bh	Pre-divider is REGN+1

2.4.20 TOP_RCM_PLL_CORE_MN2DIV Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

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Table 2-378. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0414h

Figure 2-188. TOP_RCM_PLL_CORE_MN2DIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				N2											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				M											
NONE				RW											
0				11001000000											

Access Types Legend

Table 2-379. PLL_CORE_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 16	N2	RW	0h	Bypass divider is REGN2+1
	RESERVED	NONE		Reserved
11 - 0	M	RW	28FB5F040h	Feedback Multiplier is REGM

2.4.21 TOP_RCM_PLL_CORE_FRACDIV Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

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Table 2-380. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0418h

Figure 2-189. TOP_RCM_PLL_CORE_FRACDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REGSD								RESERVED						FRACTIONALM	
RW								NONE						RW	
1000								0						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACTIONALM															
RW															
0															

Access Types Legend

Table 2-381. PLL_CORE_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	REGSD	RW	3E8h	Sigma-Delta DividerShould be set by s/w to provide optimum jitter performance.DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz
	RESERVED	NONE		Reserved
17 - 0	FRACTIONALM	RW	0h	Fractional part of the M divider.

2.4.22 TOP_RCM_PLL_CORE_BWCTRL Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-382. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 041Ch

Figure 2-190. TOP_RCM_PLL_CORE_BWCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					BWCONTROL		BW_INCR_DECRZ
NONE					RW		RW
0					0		0

Access Types Legend

Table 2-383. PLL_CORE_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 1	BWCONTROL	RW	0h	Change Loop Bandwidth
0	BW_INCR_DECRZ	RW	0h	Direction of Loop Bandwidth0x0 : decrease BW0x1 : increase BW

2.4.23 TOP_RCM_PLL_CORE_FRACCTRL Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

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Table 2-384. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0420h

Figure 2-191. TOP_RCM_PLL_CORE_FRACCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DOWNSPREAD	MODFREQDIVIDEREXPONENT			MODFREQDIVIDERMANTISSA							DELTAMSTEPINTEGER			DELTAMSTEPFRACTION	
RW	RW			RW							RW			RW	
0	0			0							0			0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELTAMSTEPFRACTION															
RW															
0															

Access Types Legend

Table 2-385. PLL_CORE_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DOWNSPREAD	RW	0h	Controls frequency spread0x0 : enables both side frequency spread about the programmed frequency.0x1 : enables low frequency spread only
30 - 28	MODFREQDIVIDEREXPONENT	RW	0h	Exponent of the REFCLK divider to define the modulation frequency.
27 - 21	MODFREQDIVIDERMANTISSA	RW	0h	Mantissa of the REFCLK divider to define the modulation frequency
20 - 18	DELTAMSTEPINTEGER	RW	0h	Integer part of Frequency Spread control
17 - 0	DELTAMSTEPFRACTION	RW	0h	The fraction part of Frequency Spread control

2.4.24 TOP_RCM_PLL_CORE_STATUS Register (Offset = 424h) [reset = h]

Short Description: RO

Long Description:

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Table 2-386. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0424h

Figure 2-192. TOP_RCM_PLL_CORE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PONOUT	PGOODOUT	LDOPWDN	RECAL_BSTATUS3	RECAL_OPPIN	RESERVED										
RO	RO	RO	RO	RO	NONE										
1	1	1	0	0	0										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CLKOUTLDOENACK	CLKDCOLDOACK	PHASELOCK	FREQLOCK	BYPASSACK	STBYRETACK	LOSSREF	CLKOUTENACK	LOCK2	M2CHANGEACK	SSCACK	HIGHJITTER	BYPASS
NONE			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0			1	0	0	0	1	0	1	0	0	0	0	0	1

Access Types Legend

Table 2-387. PLL_CORE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PONOUT	RO	1h	Status of the weak power-switch0x0 : indicates the/OFF status of the weak power-switch in digital toSOC.0x1 : ndicates the ON status of the weak power-switch in digital toSOC.
30	PGOODOUT	RO	1h	Status of the strong power-switch0x0 : indicates the/OFF status of the strong power-switch in digital toSOC.0x1 : ndicates the ON status of the strong power-switch in digital toSOC.
29	LDOPWDN	RO	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT willbe un-defined in this condition
28	RECAL_BSTATUS3	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
27	RECAL_OPPIN	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
	RESERVED	NONE		Reserved
12	CLKOUTLDOENACK	RO	1h	Indicates the enable/disable condition of CLKOUTLDOEN0x0 = CLKOUTLDO gating completed0x1 = CLKOUTLDO enabling completed
11	CLKDCOLDOACK	RO	0h	Indicates the enable/disable condition of CLKDCOLDOEN0x0 = CLKDCOLDO gating completed0x1 = CLKDCOLOD enabling completed
10	PHASELOCK	RO	0h	Status on PHASELOCK output pin
9	FREQLOCK	RO	0h	Status on FREQLOCK output pin
8	BYPASSACK	RO	1h	Status of BYPASSACK output pin
7	STBYRETACK	RO	0h	Standby and retention status0x0: indicates to SOC that all internal clocks in ADPLLLJ are activeand it is starting the relock process.0x1: indicates to SOC that all internal clocks in ADPLLLJ are gatedand it is ready for retention.
6	LOSSREF	RO	1h	Reference input loss
5	CLKOUTENACK	RO	0h	Indicates the enable/disable condition of CLKOUTEN0x0 = CLKOUT gating completed0x1 = CLKOUT enabling completed

Table 2-387. PLL_CORE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOCK2	RO	0h	ADPLL internal loop lock status
3	M2CHANGEACK	RO	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1(depending on current value) once CLKOUT frequency change hascompleted.
2	SSCACK	RO	0h	Spread Spectrum status0x0 : Spread-spectrum Clocking is disabled on output clocks0x1 : Spread-spectrum Clocking is enabled on output clocks
1	HIGHJITTER	RO	0h	1 indicates jitter. After PHASELOCK is asserted high, theHIGHJITTER flag is asserted high if phase error between REFCLKand FBCLK greater than 24%.
0	BYPASS	RO	1h	Bypass status signal. 1 CLKOUT in bypass

2.4.25 TOP_RCM_PLL_CORE_HSDIVIDER Register (Offset = 428h) [reset = h]

Short Description: RW

Long Description:

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Table 2-388. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0428h

Figure 2-193. TOP_RCM_PLL_CORE_HSDIVIDER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						LDOPWDNACK	BYPASSACKZ								
NONE						RO	RO								
0						0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TENABLEDIV	LDOPWDN	BYPASS
NONE													RW	RW	RW
0													0	0	0

Access Types Legend

Table 2-389. PLL_CORE_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	LDOPWDNACK	RO	0h	LDO Power Down Ack
16	BYPASSACKZ	RO	0h	HSDIVIDER Bypass Ack
	RESERVED	NONE		Reserved
2	TENABLEDIV	RW	0h	Tenable Div
1	LDOPWDN	RW	0h	LDO Power Down
0	BYPASS	RW	0h	HSDIVIDER Bypass

2.4.26 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Register (Offset = 42Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-390. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 042Ch

Figure 2-194. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Name Register

15	14	13	12	11	10	9	8
RESERVED			PWDN	RESERVED		STATUS	GATE_CTRL
NONE			RW	NONE		RO	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
RESERVED		DIVCHACK	DIV				
NONE		RO	RW				
0		0	100				

Access Types Legend

Table 2-391. PLL_CORE_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output0h (R/W) = CLKOUT0 divider active1h (R/W) = CLKOUT0 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT0 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT00h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	64h	DPLL post-divider factor, M4, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

2.4.27 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Register (Offset = 430h) [reset = h]

Short Description: RW

Long Description:

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Table 2-392. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0430h

Figure 2-195. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Name Register

15	14	13	12	11	10	9	8
RESERVED			PWDN	RESERVED		STATUS	GATE_CTRL
NONE			RW	NONE		RO	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
RESERVED		DIVCHACK	DIV				
NONE		RO	RW				
0		0	11				

Access Types Legend

Table 2-393. PLL_CORE_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output0h (R/W) = CLKOUT1 divider active1h (R/W) = CLKOUT1 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT1 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT10h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	Bh	DPLL post-divider factor, M5, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

2.4.28 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Register (Offset = 434h) [reset = h]

Short Description: RW

Long Description:

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Table 2-394. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0434h

Figure 2-196. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Name Register

15	14	13	12	11	10	9	8
RESERVED			PWDN	RESERVED		STATUS	GATE_CTRL
NONE			RW	NONE		RO	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
RESERVED		DIVCHACK	DIV				
NONE		RO	RW				
0		0	100				

Access Types Legend

Table 2-395. PLL_CORE_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M6 divider and hence CLKOUT2 output0h (R/W) = CLKOUT2 divider active1h (R/W) = CLKOUT2 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT2 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT20h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	64h	DPLL post-divider factor, M6, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

2.4.29 TOP_RCM_PLL_CORE_RSTCTRL Register (Offset = 43Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-396. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 043Ch

Figure 2-197. TOP_RCM_PLL_CORE_RSTCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-397. PLL_CORE_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the PLLWrite 3'b111 : Override is enabled and Reset is asserted

2.4.30 TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-398. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0440h

Figure 2-198. TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-399. PLL_CORE_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the HSDIVIDERWrite 3'b111 : Override is enabled and Reset is asserted

2.4.31 TOP_RCM_R5SS_CLK_SRC_SEL Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-400. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0500h

Figure 2-199. TOP_RCM_R5SS_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-401. R5SS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS Coretex R5 and System bus Clock.Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

2.4.32 TOP_RCM_R5SS_CLK_STATUS Register (Offset = 504h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-402. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0504h

Figure 2-200. TOP_RCM_R5SS_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-403. R5SS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Root clock for CortexR5 and Sysclk

2.4.33 TOP_RCM_R5SS0_CLK_DIV_SEL Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-404. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0510h

Figure 2-201. TOP_RCM_R5SS0_CLK_DIV_SEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKDIVSEL		
NONE					RW		
0					0		

Access Types Legend

Table 2-405. R5SS0_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKDIVSEL	RW	0h	writing 3'b000 Sets R5 clock = R5SS Root clockWriting 3'b111 Sets R5 Clock = SYSCLK

2.4.34 TOP_RCM_R5SS1_CLK_DIV_SEL Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-406. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0514h

Figure 2-202. TOP_RCM_R5SS1_CLK_DIV_SEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKDIVSEL		
NONE					RW		
0					0		

Access Types Legend

Table 2-407. R5SS1_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKDIVSEL	RW	0h	writing 3'b000 Sets R5 clock = R5SS Root clockWriting 3'b111 Sets R5 Clock = SYSCLK

2.4.35 TOP_RCM_R5SS0_CLK_GATE Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-408. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0518h

Figure 2-203. TOP_RCM_R5SS0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-409. R5SS0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5.Data should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.36 TOP_RCM_R5SS1_CLK_GATE Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-410. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 051Ch

Figure 2-204. TOP_RCM_R5SS1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-411. R5SS1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5.Data should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.37 TOP_RCM_SYS_CLK_DIV_VAL Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-412. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0520h

Figure 2-205. TOP_RCM_SYS_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIV			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIV							
RW							
0							

Access Types Legend

Table 2-413. SYS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for System Clock selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.38 TOP_RCM_SYS_CLK_GATE Register (Offset = 524h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-414. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0524h

Figure 2-206. TOP_RCM_SYS_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-415. SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for System ClockData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.39 TOP_RCM_SYS_CLK_STATUS Register (Offset = 528h) [reset = h]

Short Description: RO

Long Description:

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Table 2-416. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0528h

Figure 2-207. TOP_RCM_SYS_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0							

Access Types Legend

Table 2-417. SYS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Sys Clock
	RESERVED	NONE		Reserved

2.4.40 TOP_RCM_PLL_PER_PWRCTRL Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-418. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0800h

Figure 2-208. TOP_RCM_PLL_PER_PWRCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED		PONIN	PGOODIN	RET	ISORET	ISOSCAN	OFFMODE
NONE		RW	RW	RW	RW	RW	RW
0		1	1	0	0	0	0

Access Types Legend

Table 2-419. PLL_PER_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	PONIN	RW	1h	ON/OFF control of the weak power switch digital. For functionalmode it should be 1
4	PGOODIN	RW	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1
3	RET	RW	0h	Save/Restore control for Retention mode. For functional mode itshould be 0
2	ISORET	RW	0h	Save/Restore control for Isolation of output pins For functional modeit should be 0
1	ISOSCAN	RW	0h	Save/Restore control for Isolation of the Scanout pins. For functionalmode it should be 0
0	OFFMODE	RW	0h	Used to switch OFF the logic on VDDA. For functional mode itshould be 0

2.4.41 TOP_RCM_PLL_PER_CLKCTRL Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

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Table 2-420. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0804h

Figure 2-209. TOP_RCM_PLL_PER_CLKCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CYCLESLIPEN	ENSSC	CLKDCOLDOEN	RESERVED					IDLE	BYPASSACKZ	STBYRET	CLKOUTEN	CLKOUTLDOEN	ULOWCLKEN	CLKDCOLDOPWDNZ	M2PWDNZ
RW	RW	RW	NONE					RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0					1	0	0	0	1	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	STOPMODE	RESERVED	SELFREQDCO			RESERVED	RELAXED_LOCK	RESERVED						SSCTYPE	TINTZ
NONE	RW	NONE	RW			NONE	RW	NONE						RW	RW
0	1	0	100			0	0	0						0	0

Access Types Legend

Table 2-421. PLL_PER_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CYCLESLIPEN	RW	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK.
30	ENSSC	RW	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading.
29	CLKDCOLDOEN	RW	0h	Synchronously enables/disables CLKDCOLDO0x0 : synchronously disables CLKDCOLDO0x1 : synchronously enables CLKDCOLDO
	RESERVED	NONE		Reserved
23	IDLE	RW	1h	Sets PLL to Idle mode0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go toActive and Locked0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go toIdle Bypass low powe
22	BYPASSACKZ	RW	0h	BYPASSACKZ is a special purpose input to the module. In generalthis input is expected to be tied to static low. For the output clocks ofthe module that do not have an internal bypass mux viz.CLKDCOLDO and CLKOUTLDO, a bypass mux could beimplemented external to the module.
21	STBYRET	RW	0h	Standby retention control0x0 : prepares ADPLLLJ for relock when out of retention byremoving the gating on all internal clocks.0x1 : prepares ADPLLLJ for retention by gating all the internalclocks.
20	CLKOUTEN	RW	0h	CLKOUT enable or disable0x0 : synchronously disables CLKOUT0x1 : synchronously enables CLKOUT
19	CLKOUTLDOEN	RW	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	ULOWCLKEN	RW	0h	Select CLKOUT source in bypass0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1)0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	CLKDCOLDOPWDNZ	RW	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	M2PWDNZ	RW	1h	M2 divider power down mode0x0: Asynchronous power down for M2 divider0x1 : M2 divider is functional

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Table 2-421. PLL_PER_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
14	STOPMODE	RW	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
	RESERVED	NONE		Reserved
12 - 10	SELFREQDCO	RW	64h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency rangeselector.0x0: Reserved0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz0x3: Reserved0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz0x5: Reserved
	RESERVED	NONE		Reserved
8	RELAXED_LOCK	RW	0h	Decides when FREQLOCK asserted0x0: FREQLOCK asserted when DC frequency error less than 1%0x1: FREQLOCK asserted when DC frequency error less than 2%
	RESERVED	NONE		Reserved
1	SSCTYPE	RW	0h	SSC Type
0	TINTZ	RW	0h	PLL core soft reset

2.4.42 TOP_RCM_PLL_PER_TENABLE Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-422. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0808h

Figure 2-210. TOP_RCM_PLL_PER_TENABLE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
TENABLE							
RW							
0							

Access Types Legend

Table 2-423. PLL_PER_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLE	RW	0h	M, N. SD and SELFREQDCO latch (active rise edge)

2.4.43 TOP_RCM_PLL_PER_TENABLEDIV Register (Offset = 80Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-424. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 080Ch

Figure 2-211. TOP_RCM_PLL_PER_TENABLEDIV Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
TENABLEDIV							
RW							
0							

Access Types Legend

Table 2-425. PLL_PER_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLEDIV	RW	0h	M2 and N2 latch (active rise edge)

2.4.44 TOP_RCM_PLL_PER_M2NDIV Register (Offset = 810h) [reset = h]

Short Description: RW

Long Description:

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Table 2-426. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0810h

Figure 2-212. TOP_RCM_PLL_PER_M2NDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	M2														
NONE	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								N							
NONE								RW							
0								10011							

Access Types Legend

Table 2-427. PLL_PER_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 16	M2	RW	0h	Post-divider is REGM2
	RESERVED	NONE		Reserved
7 - 0	N	RW	271Bh	Pre-divider is REGN+1

2.4.45 TOP_RCM_PLL_PER_MN2DIV Register (Offset = 814h) [reset = h]

Short Description: RW

Long Description:

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Table 2-428. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0814h

Figure 2-213. TOP_RCM_PLL_PER_MN2DIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				N2											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				M											
NONE				RW											
0				11000000000											

Access Types Legend

Table 2-429. PLL_PER_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 16	N2	RW	0h	Bypass divider is REGN2+1
	RESERVED	NONE		Reserved
11 - 0	M	RW	28FA6AE00h	Feedback Multiplier is REGM

2.4.46 TOP_RCM_PLL_PER_FRACDIV Register (Offset = 818h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-430. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0818h

Figure 2-214. TOP_RCM_PLL_PER_FRACDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REGSD								RESERVED						FRACTIONALM	
RW								NONE						RW	
1000								0						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACTIONALM															
RW															
0															

Access Types Legend

Table 2-431. PLL_PER_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	REGSD	RW	3E8h	Sigma-Delta DividerShould be set by s/w to provide optimum jitter performance.DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz
	RESERVED	NONE		Reserved
17 - 0	FRACTIONALM	RW	0h	Fractional part of the M divider.

2.4.47 TOP_RCM_PLL_PER_BWCTRL Register (Offset = 81Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-432. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 081Ch

Figure 2-215. TOP_RCM_PLL_PER_BWCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					BWCONTROL		BW_INCR_DECRZ
NONE					RW		RW
0					0		0

Access Types Legend

Table 2-433. PLL_PER_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 1	BWCONTROL	RW	0h	Change Loop Bandwidth
0	BW_INCR_DECRZ	RW	0h	Direction of Loop Bandwidth0x0 : decrease BW0x1 : increase BW

2.4.48 TOP_RCM_PLL_PER_FRACCTRL Register (Offset = 820h) [reset = h]

Short Description: RW

Long Description:

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Table 2-434. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0820h

Figure 2-216. TOP_RCM_PLL_PER_FRACCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DOWNSPREAD	MODFREQDIVIDEREXPONENT			MODFREQDIVIDERMANTISSA							DELTAMSTEPINTEGER			DELTAMSTEPFRACTION	
RW	RW			RW							RW			RW	
0	0			0							0			0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELTAMSTEPFRACTION															
RW															
0															

Access Types Legend

Table 2-435. PLL_PER_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DOWNSPREAD	RW	0h	Controls frequency spread0x0 : enables both side frequency spread about the programmed frequency.0x1 : enables low frequency spread only
30 - 28	MODFREQDIVIDEREXPONENT	RW	0h	Exponent of the REFCLK divider to define the modulation frequency.
27 - 21	MODFREQDIVIDERMANTISSA	RW	0h	Mantissa of the REFCLK divider to define the modulation frequency
20 - 18	DELTAMSTEPINTEGER	RW	0h	Integer part of Frequency Spread control
17 - 0	DELTAMSTEPFRACTION	RW	0h	The fraction part of Frequency Spread control

2.4.49 TOP_RCM_PLL_PER_STATUS Register (Offset = 824h) [reset = h]

Short Description: RO

Long Description:

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Table 2-436. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0824h

Figure 2-217. TOP_RCM_PLL_PER_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PONOUT	PGOODOUT	LDOPWDN	RECAL_BSTATUS3	RECAL_OPPIN	RESERVED										
RO	RO	RO	RO	RO	NONE										
1	1	1	0	0	0										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CLKOUTLDOENACK	CLKDCOLDOACK	PHASELOCK	FREQLOCK	BYPASSACK	STBYRETACK	LOSSREF	CLKOUTENACK	LOCK2	M2CHANGEACK	SSCACK	HIGHJITTER	BYPASS
NONE			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0			1	0	0	0	1	0	1	0	0	0	0	0	1

Access Types Legend

Table 2-437. PLL_PER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PONOUT	RO	1h	Status of the weak power-switch0x0 : indicates the/OFF status of the weak power-switch in digital toSOC.0x1 : ndicates the ON status of the weak power-switch in digital toSOC.
30	PGOODOUT	RO	1h	Status of the strong power-switch0x0 : indicates the/OFF status of the strong power-switch in digital toSOC.0x1 : ndicates the ON status of the strong power-switch in digital toSOC.
29	LDOPWDN	RO	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT willbe un-defined in this condition
28	RECAL_BSTATUS3	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
27	RECAL_OPPIN	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
	RESERVED	NONE		Reserved
12	CLKOUTLDOENACK	RO	1h	Indicates the enable/disable condition of CLKOUTLDOEN0x0 = CLKOUTLDO gating completed0x1 = CLKOUTLDO enabling completed
11	CLKDCOLDOACK	RO	0h	Indicates the enable/disable condition of CLKDCOLDOEN0x0 = CLKDCOLDO gating completed0x1 = CLKDCOLDO enabling completed
10	PHASELOCK	RO	0h	Status on PHASELOCK output pin
9	FREQLOCK	RO	0h	Status on FREQLOCK output pin
8	BYPASSACK	RO	1h	Status of BYPASSACK output pin
7	STBYRETACK	RO	0h	Standby and retention status0x0: indicates to SOC that all internal clocks in ADPLLLJ are activeand it is starting the relock process.0x1: indicates to SOC that all internal clocks in ADPLLLJ are gatedand it is ready for retention.
6	LOSSREF	RO	1h	Reference input loss
5	CLKOUTENACK	RO	0h	Indicates the enable/disable condition of CLKOUTEN0x0 = CLKOUT gating completed0x1 = CLKOUT enabling completed

Table 2-437. PLL_PER_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LOCK2	RO	0h	ADPLL internal loop lock status
3	M2CHANGEACK	RO	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1(depending on current value) once CLKOUT frequency change hascompleted.
2	SSCACK	RO	0h	Spread Spectrum status0x0 : Spread-spectrum Clocking is disabled on output clocks0x1 : Spread-spectrum Clocking is enabled on output clocks
1	HIGHJITTER	RO	0h	1 indicates jitter. After PHASELOCK is asserted high, theHIGHJITTER flag is asserted high if phase error between REFCLKand FBCLK greater than 24%.
0	BYPASS	RO	1h	Bypass status signal. 1 CLKOUT in bypass

2.4.50 TOP_RCM_PLL_PER_HSDIVIDER Register (Offset = 828h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-438. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0828h

Figure 2-218. TOP_RCM_PLL_PER_HSDIVIDER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						LDOPWDNACK	BYPASSACKZ								
NONE						RO	RO								
0						0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TENABLEDIV	LDOPWDN	BYPASS
NONE													RW	RW	RW
0													0	0	0

Access Types Legend

Table 2-439. PLL_PER_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	LDOPWDNACK	RO	0h	LDO Power Down Ack
16	BYPASSACKZ	RO	0h	HSDIVIDER Bypass Ack
	RESERVED	NONE		Reserved
2	TENABLEDIV	RW	0h	Tenable Div
1	LDOPWDN	RW	0h	LDO Power Down
0	BYPASS	RW	0h	HSDIVIDER Bypass

2.4.51 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Register (Offset = 82Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-440. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 082Ch

Figure 2-219. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Name Register

15	14	13	12	11	10	9	8
RESERVED			PWDN	RESERVED		STATUS	GATE_CTRL
NONE			RW	NONE		RO	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
RESERVED		DIVCHACK	DIV				
NONE		RO	RW				
0		0	1011				

Access Types Legend

Table 2-441. PLL_PER_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output0h (R/W) = CLKOUT0 divider active1h (R/W) = CLKOUT0 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT0 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT00h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	3F3h	DPLL post-divider factor, M4, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

2.4.52 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Register (Offset = 830h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-442. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0830h

Figure 2-220. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Name Register

15	14	13	12	11	10	9	8
RESERVED			PWDN	RESERVED		STATUS	GATE_CTRL
NONE			RW	NONE		RO	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
RESERVED		DIVCHACK	DIV				
NONE		RO	RW				
0		0	1001				

Access Types Legend

Table 2-443. PLL_PER_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output0h (R/W) = CLKOUT1 divider active1h (R/W) = CLKOUT1 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT1 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT10h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	3E9h	DPLL post-divider factor, M5, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

2.4.53 TOP_RCM_PLL_PER_RSTCTRL Register (Offset = 83Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-444. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 083Ch

Figure 2-221. TOP_RCM_PLL_PER_RSTCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-445. PLL_PER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the PLLWrite 3'b111 : Override is enabled and Reset is asserted

2.4.54 TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Register (Offset = 840h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-446. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0840h

Figure 2-222. TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-447. PLL_PER_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the HSDIVIDERWrite 3'b111 : Override is enabled and Reset is asserted

2.4.55 TOP_RCM_CLKOUT0_CLK_SRC_SEL Register (Offset = C00h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-448. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C00h

Figure 2-223. TOP_RCM_CLKOUT0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-449. CLKOUT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS CLKOUT .Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

2.4.56 TOP_RCM_CLKOUT1_CLK_SRC_SEL Register (Offset = C04h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-450. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C04h

Figure 2-224. TOP_RCM_CLKOUT1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-451. CLKOUT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS CLKOUT .Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

2.4.57 TOP_RCM_CLKOUT0_DIV_VAL Register (Offset = C08h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-452. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C08h

Figure 2-225. TOP_RCM_CLKOUT0_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIV			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIV							
RW							
0							

Access Types Legend

Table 2-453. CLKOUT0_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for CLKOUT selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.58 TOP_RCM_CLKOUT1_DIV_VAL Register (Offset = C0Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-454. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C0Ch

Figure 2-226. TOP_RCM_CLKOUT1_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIV			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIV							
RW							
0							

Access Types Legend

Table 2-455. CLKOUT1_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for CLKOUT selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.59 TOP_RCM_CLKOUT0_CLK_GATE Register (Offset = C10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-456. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C10h

Figure 2-227. TOP_RCM_CLKOUT0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-457. CLKOUT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUTData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.60 TOP_RCM_CLKOUT1_CLK_GATE Register (Offset = C14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-458. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C14h

Figure 2-228. TOP_RCM_CLKOUT1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-459. CLKOUT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUTData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.61 TOP_RCM_CLKOUT0_CLK_STATUS Register (Offset = C18h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-460. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C18h

Figure 2-229. TOP_RCM_CLKOUT0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-461. CLKOUT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CLKOUT Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CLKOUT Clock

2.4.62 TOP_RCM_CLKOUT1_CLK_STATUS Register (Offset = C1Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-462. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C1Ch

Figure 2-230. TOP_RCM_CLKOUT1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-463. CLKOUT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CLKOUT Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CLKOUT Clock

2.4.63 TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Register (Offset = C20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-464. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C20h

Figure 2-231. TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-465. TRCCLKOUT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for TRC ClkoutData should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

2.4.64 TOP_RCM_TRCCLKOUT_DIV_VAL Register (Offset = C24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-466. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C24h

Figure 2-232. TOP_RCM_TRCCLKOUT_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIV			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIV							
RW							
0							

Access Types Legend

Table 2-467. TRCCLKOUT_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for TRC Clkout selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

2.4.65 TOP_RCM_TRCCLKOUT_CLK_GATE Register (Offset = C28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-468. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C28h

Figure 2-233. TOP_RCM_TRCCLKOUT_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-469. TRCCLKOUT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Clock gatring config for TRC ClkoutData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

2.4.66 TOP_RCM_TRCCLKOUT_CLK_STATUS Register (Offset = C2Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-470. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C2Ch

Figure 2-234. TOP_RCM_TRCCLKOUT_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-471. TRCCLKOUT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for PMIC Clkout Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for PMIC Clkout Clock

2.4.67 TOP_RCM_DFT_DMLED_EXEC Register (Offset = D00h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-472. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0D00h

Figure 2-235. TOP_RCM_DFT_DMLED_EXEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 2-473. DFT_DMLED_EXEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	SW mapping for DMLED ExecutionBit 0 : HSM CM4 Execution Bit 1 : HWA CM4 Execution Bit 2 : MSS CR5undefined Execution

2.4.68 TOP_RCM_DFT_DMLED_STATUS Register (Offset = D04h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-474. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0D04h

Figure 2-236. TOP_RCM_DFT_DMLED_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 2-475. DFT_DMLED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	SW mapping for DMLED StatusBit 0 : HSM CM4 Status Bit 1 : HWA CM4 Status Bit 2 : MSS CR5undefined Status

2.4.69 TOP_RCM_HW_REG0 Register (Offset = E00h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-476. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0E00h

Figure 2-237. TOP_RCM_HW_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-477. HW_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser. Reserved for HW RnD

2.4.70 TOP_RCM_HW_REG1 Register (Offset = E04h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-478. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0E04h

Figure 2-238. TOP_RCM_HW_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-479. HW_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser. Reserved for HW RnD

2.4.71 TOP_RCM_HW_REG2 Register (Offset = E08h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-480. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0E08h

Figure 2-239. TOP_RCM_HW_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-481. HW_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser. Reserved for HW RnD

2.4.72 TOP_RCM_HW_REG3 Register (Offset = E0Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-482. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0E0Ch

Figure 2-240. TOP_RCM_HW_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-483. HW_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser. Reserved for HW RnD

2.4.73 TOP_RCM_HW_SPARE_RW0 Register (Offset = FD0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-484. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FD0h

Figure 2-241. TOP_RCM_HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW0															
RW															
0															

Access Types Legend

Table 2-485. HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW0	RW	0h	Reserved for HW R&D

2.4.74 TOP_RCM_HW_SPARE_RW1 Register (Offset = FD4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-486. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FD4h

Figure 2-242. TOP_RCM_HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW1															
RW															
0															

Access Types Legend

Table 2-487. HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW1	RW	0h	Reserved for HW R&D

2.4.75 TOP_RCM_HW_SPARE_RW2 Register (Offset = FD8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-488. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FD8h

Figure 2-243. TOP_RCM_HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW2															
RW															
0															

Access Types Legend

Table 2-489. HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW2	RW	0h	Reserved for HW R&D

2.4.76 TOP_RCM_HW_SPARE_RW3 Register (Offset = FDCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-490. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FDCh

Figure 2-244. TOP_RCM_HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW3															
RW															
0															

Access Types Legend

Table 2-491. HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW3	RW	0h	Reserved for HW R&D

2.4.77 TOP_RCM_HW_SPARE_RO0 Register (Offset = FE0h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-492. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FE0h

Figure 2-245. TOP_RCM_HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO0															
RO															
0															

Access Types Legend

Table 2-493. HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO0	RO	0h	Reserved for HW R&D

2.4.78 TOP_RCM_HW_SPARE_RO1 Register (Offset = FE4h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-494. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FE4h

Figure 2-246. TOP_RCM_HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO1															
RO															
0															

Access Types Legend

Table 2-495. HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO1	RO	0h	Reserved for HW R&D

2.4.79 TOP_RCM_HW_SPARE_RO2 Register (Offset = FE8h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-496. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FE8h

Figure 2-247. TOP_RCM_HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO2															
RO															
0															

Access Types Legend

Table 2-497. HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO2	RO	0h	Reserved for HW R&D

2.4.80 TOP_RCM_HW_SPARE_RO3 Register (Offset = FECh) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-498. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FECh

Figure 2-248. TOP_RCM_HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO3															
RO															
0															

Access Types Legend

Table 2-499. HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO3	RO	0h	Reserved for HW R&D

2.4.81 TOP_RCM_HW_SPARE_WPH Register (Offset = FF0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-500. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FF0h

Figure 2-249. TOP_RCM_HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_WPH															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_WPH															
RW															
0															

Access Types Legend

Table 2-501. HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_WPH	RW	0h	Reserved for HW R&D

2.4.82 TOP_RCM_HW_SPARE_REC Register (Offset = FF4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-502. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0FF4h

Figure 2-250. TOP_RCM_HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_REC31	HW_SPARE_REC30	HW_SPARE_REC29	HW_SPARE_REC28	HW_SPARE_REC27	HW_SPARE_REC26	HW_SPARE_REC25	HW_SPARE_REC24	HW_SPARE_REC23	HW_SPARE_REC22	HW_SPARE_REC21	HW_SPARE_REC20	HW_SPARE_REC19	HW_SPARE_REC18	HW_SPARE_REC17	HW_SPARE_REC16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_REC15	HW_SPARE_REC14	HW_SPARE_REC13	HW_SPARE_REC12	HW_SPARE_REC11	HW_SPARE_REC10	HW_SPARE_REC9	HW_SPARE_REC8	HW_SPARE_REC7	HW_SPARE_REC6	HW_SPARE_REC5	HW_SPARE_REC4	HW_SPARE_REC3	HW_SPARE_REC2	HW_SPARE_REC1	HW_SPARE_REC0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 2-503. HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC31	RW	0h	Reserved for HW R&D
30	HW_SPARE_REC30	RW	0h	Reserved for HW R&D
29	HW_SPARE_REC29	RW	0h	Reserved for HW R&D
28	HW_SPARE_REC28	RW	0h	Reserved for HW R&D
27	HW_SPARE_REC27	RW	0h	Reserved for HW R&D
26	HW_SPARE_REC26	RW	0h	Reserved for HW R&D
25	HW_SPARE_REC25	RW	0h	Reserved for HW R&D
24	HW_SPARE_REC24	RW	0h	Reserved for HW R&D
23	HW_SPARE_REC23	RW	0h	Reserved for HW R&D
22	HW_SPARE_REC22	RW	0h	Reserved for HW R&D
21	HW_SPARE_REC21	RW	0h	Reserved for HW R&D
20	HW_SPARE_REC20	RW	0h	Reserved for HW R&D
19	HW_SPARE_REC19	RW	0h	Reserved for HW R&D
18	HW_SPARE_REC18	RW	0h	Reserved for HW R&D
17	HW_SPARE_REC17	RW	0h	Reserved for HW R&D
16	HW_SPARE_REC16	RW	0h	Reserved for HW R&D
15	HW_SPARE_REC15	RW	0h	Reserved for HW R&D
14	HW_SPARE_REC14	RW	0h	Reserved for HW R&D
13	HW_SPARE_REC13	RW	0h	Reserved for HW R&D
12	HW_SPARE_REC12	RW	0h	Reserved for HW R&D
11	HW_SPARE_REC11	RW	0h	Reserved for HW R&D
10	HW_SPARE_REC10	RW	0h	Reserved for HW R&D
9	HW_SPARE_REC9	RW	0h	Reserved for HW R&D
8	HW_SPARE_REC8	RW	0h	Reserved for HW R&D

Table 2-503. HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	HW_SPARE_REC7	RW	0h	Reserved for HW R&D
6	HW_SPARE_REC6	RW	0h	Reserved for HW R&D
5	HW_SPARE_REC5	RW	0h	Reserved for HW R&D
4	HW_SPARE_REC4	RW	0h	Reserved for HW R&D
3	HW_SPARE_REC3	RW	0h	Reserved for HW R&D
2	HW_SPARE_REC2	RW	0h	Reserved for HW R&D
1	HW_SPARE_REC1	RW	0h	Reserved for HW R&D
0	HW_SPARE_REC0	RW	0h	Reserved for HW R&D

2.4.83 TOP_RCM_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

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Table 2-504. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1008h

Figure 2-251. TOP_RCM_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
RW															
0															

Access Types Legend

Table 2-505. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

2.4.84 TOP_RCM_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-506. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 100Ch

Figure 2-252. TOP_RCM_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
RW															
0															

Access Types Legend

Table 2-507. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

2.4.85 TOP_RCM_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

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Table 2-508. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1010h

Figure 2-253. TOP_RCM_INTR_RAW_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-509. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

2.4.86 TOP_RCM_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

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Table 2-510. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1014h

Figure 2-254. TOP_RCM_INTR_ENABLED_STATUS_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-511. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

2.4.87 TOP_RCM_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

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Table 2-512. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1018h

Figure 2-255. TOP_RCM_INTR_ENABLE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-513. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

2.4.88 TOP_RCM_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 2-514. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 101Ch

Figure 2-256. TOP_RCM_INTR_ENABLE_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-515. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

2.4.89 TOP_RCM_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-516. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1020h

Figure 2-257. TOP_RCM_EOI Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_VECTOR							
RW							
0							

Access Types Legend

Table 2-517. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

2.4.90 TOP_RCM_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

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Table 2-518. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1024h

Figure 2-258. TOP_RCM_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
RO															
0															

Access Types Legend

Table 2-519. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

2.4.91 TOP_RCM_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 2-520. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1028h

Figure 2-259. TOP_RCM_FAULT_TYPE_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	RO	RO					
0	0	0					

Access Types Legend

Table 2-521. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

2.4.92 TOP_RCM_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

Return to Summary Table

Table 2-522. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 102Ch

Figure 2-260. TOP_RCM_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
RO								RO							
0								0							

Access Types Legend

Table 2-523. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

2.4.93 TOP_RCM_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 2-524. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1030h

Figure 2-261. TOP_RCM_FAULT_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
FAULT_CLR							
WO							
0							

Access Types Legend

Table 2-525. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

Table 2-526. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

2.5 MSS_RCM Registers

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
0h	32	MSS_RCM_PID	PID register	5320 8000h
10h	16	MSS_RCM_R5SS0_RST_STATUS	RO	5320 8010h
14h	8	MSS_RCM_R5SS0_RST_CAUSE_CLR	RW	5320 8014h
18h	24	MSS_RCM_R5SS0_DBG_RST_EN	RW	5320 8018h
1Ch	8	MSS_RCM_R5SS0_RST_ASSERDLY	RW	5320 801Ch
20h	32	MSS_RCM_R5SS0_RST2ASSERTDLY	RW	5320 8020h
24h	32	MSS_RCM_R5SS0_RST_WFICHECK	RW	5320 8024h
30h	16	MSS_RCM_R5SS1_RST_STATUS	RO	5320 8030h
34h	8	MSS_RCM_R5SS1_RST_CAUSE_CLR	RW	5320 8034h
38h	24	MSS_RCM_R5SS1_DBG_RST_EN	RW	5320 8038h
3Ch	8	MSS_RCM_R5SS1_RST_ASSERDLY	RW	5320 803Ch
40h	32	MSS_RCM_R5SS1_RST2ASSERTDLY	RW	5320 8040h
44h	32	MSS_RCM_R5SS1_RST_WFICHECK	RW	5320 8044h
100h	16	MSS_RCM_MCAN0_CLK_SRC_SEL	RW	5320 8100h
104h	16	MSS_RCM_MCAN1_CLK_SRC_SEL	RW	5320 8104h
108h	16	MSS_RCM_MCAN2_CLK_SRC_SEL	RW	5320 8108h
10Ch	16	MSS_RCM_MCAN3_CLK_SRC_SEL	RW	5320 810Ch
110h	16	MSS_RCM_QSPI0_CLK_SRC_SEL	RW	5320 8110h
114h	16	MSS_RCM_RTI0_CLK_SRC_SEL	RW	5320 8114h
118h	16	MSS_RCM_RTI1_CLK_SRC_SEL	RW	5320 8118h
11Ch	16	MSS_RCM_RTI2_CLK_SRC_SEL	RW	5320 811Ch
120h	16	MSS_RCM_RTI3_CLK_SRC_SEL	RW	5320 8120h
128h	16	MSS_RCM_WDT0_CLK_SRC_SEL	RW	5320 8128h
12Ch	16	MSS_RCM_WDT1_CLK_SRC_SEL	RW	5320 812Ch
130h	16	MSS_RCM_WDT2_CLK_SRC_SEL	RW	5320 8130h
134h	16	MSS_RCM_WDT3_CLK_SRC_SEL	RW	5320 8134h
13Ch	16	MSS_RCM_MCSPI0_CLK_SRC_SEL	RW	5320 813Ch
140h	16	MSS_RCM_MCSPI1_CLK_SRC_SEL	RW	5320 8140h
144h	16	MSS_RCM_MCSPI2_CLK_SRC_SEL	RW	5320 8144h
148h	16	MSS_RCM_MCSPI3_CLK_SRC_SEL	RW	5320 8148h
14Ch	16	MSS_RCM_MCSPI4_CLK_SRC_SEL	RW	5320 814Ch
150h	16	MSS_RCM_MMC0_CLK_SRC_SEL	RW	5320 8150h
154h	16	MSS_RCM_ICSSM0_UART0_CLK_SRC_SEL	RW	5320 8154h
158h	16	MSS_RCM_CPTS_CLK_SRC_SEL	RW	5320 8158h
15Ch	16	MSS_RCM_GPMC_CLK_SRC_SEL	RW	5320 815Ch
160h	16	MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL	RW	5320 8160h
164h	16	MSS_RCM_I2C_CLK_SRC_SEL	RW	5320 8164h

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
174h	16	MSS_RCM_LIN0_UART0_CLK_SRC_SEL	RW	5320 8174h
178h	16	MSS_RCM_LIN1_UART1_CLK_SRC_SEL	RW	5320 8178h
17Ch	16	MSS_RCM_LIN2_UART2_CLK_SRC_SEL	RW	5320 817Ch
180h	16	MSS_RCM_LIN3_UART3_CLK_SRC_SEL	RW	5320 8180h
184h	16	MSS_RCM_LIN4_UART4_CLK_SRC_SEL	RW	5320 8184h
188h	16	MSS_RCM_LIN5_UART5_CLK_SRC_SEL	RW	5320 8188h
200h	16	MSS_RCM_MCAN0_CLK_DIV_VAL	RW	5320 8200h
204h	16	MSS_RCM_MCAN1_CLK_DIV_VAL	RW	5320 8204h
208h	16	MSS_RCM_MCAN2_CLK_DIV_VAL	RW	5320 8208h
20Ch	16	MSS_RCM_MCAN3_CLK_DIV_VAL	RW	5320 820Ch
210h	16	MSS_RCM_QSPI0_CLK_DIV_VAL	RW	5320 8210h
214h	16	MSS_RCM_RTI0_CLK_DIV_VAL	RW	5320 8214h
218h	16	MSS_RCM_RTI1_CLK_DIV_VAL	RW	5320 8218h
21Ch	16	MSS_RCM_RTI2_CLK_DIV_VAL	RW	5320 821Ch
220h	16	MSS_RCM_RTI3_CLK_DIV_VAL	RW	5320 8220h
228h	16	MSS_RCM_WDT0_CLK_DIV_VAL	RW	5320 8228h
22Ch	16	MSS_RCM_WDT1_CLK_DIV_VAL	RW	5320 822Ch
230h	16	MSS_RCM_WDT2_CLK_DIV_VAL	RW	5320 8230h
234h	16	MSS_RCM_WDT3_CLK_DIV_VAL	RW	5320 8234h
23Ch	16	MSS_RCM_MCSPI0_CLK_DIV_VAL	RW	5320 823Ch
240h	16	MSS_RCM_MCSPI1_CLK_DIV_VAL	RW	5320 8240h
244h	16	MSS_RCM_MCSPI2_CLK_DIV_VAL	RW	5320 8244h
248h	16	MSS_RCM_MCSPI3_CLK_DIV_VAL	RW	5320 8248h
24Ch	16	MSS_RCM_MCSPI4_CLK_DIV_VAL	RW	5320 824Ch
250h	16	MSS_RCM_MMC0_CLK_DIV_VAL	RW	5320 8250h
254h	16	MSS_RCM_ICSSM0_UART_CLK_DIV_VAL	RW	5320 8254h
258h	16	MSS_RCM_CPTS_CLK_DIV_VAL	RW	5320 8258h
25Ch	16	MSS_RCM_GPMC_CLK_DIV_VAL	RW	5320 825Ch
260h	16	MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL	RW	5320 8260h
264h	16	MSS_RCM_I2C_CLK_DIV_VAL	RW	5320 8264h
274h	16	MSS_RCM_LIN0_UART0_CLK_DIV_VAL	RW	5320 8274h
278h	16	MSS_RCM_LIN1_UART1_CLK_DIV_VAL	RW	5320 8278h
27Ch	16	MSS_RCM_LIN2_UART2_CLK_DIV_VAL	RW	5320 827Ch
280h	16	MSS_RCM_LIN3_UART3_CLK_DIV_VAL	RW	5320 8280h
284h	16	MSS_RCM_LIN4_UART4_CLK_DIV_VAL	RW	5320 8284h
288h	16	MSS_RCM_LIN5_UART5_CLK_DIV_VAL	RW	5320 8288h
28Ch	16	MSS_RCM_RGMII_250_CLK_DIV_VAL	RW	5320 828Ch
290h	16	MSS_RCM_RGMII_50_CLK_DIV_VAL	RW	5320 8290h
294h	24	MSS_RCM_RGMII_5_CLK_DIV_VAL	RW	5320 8294h
298h	32	MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL	RW	5320 8298h
29Ch	32	MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL	RW	5320 829Ch
2A0h	16	MSS_RCM_MSS_ELM_CLK_DIV_VAL	RW	5320 82A0h
300h	8	MSS_RCM_MCAN0_CLK_GATE	RW	5320 8300h
304h	8	MSS_RCM_MCAN1_CLK_GATE	RW	5320 8304h

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
308h	8	MSS_RCM_MCAN2_CLK_GATE	RW	5320 8308h
30Ch	8	MSS_RCM_MCAN3_CLK_GATE	RW	5320 830Ch
310h	8	MSS_RCM_QSPI0_CLK_GATE	RW	5320 8310h
314h	8	MSS_RCM_RTI0_CLK_GATE	RW	5320 8314h
318h	8	MSS_RCM_RTI1_CLK_GATE	RW	5320 8318h
31Ch	8	MSS_RCM_RTI2_CLK_GATE	RW	5320 831Ch
320h	8	MSS_RCM_RTI3_CLK_GATE	RW	5320 8320h
328h	8	MSS_RCM_WDT0_CLK_GATE	RW	5320 8328h
32Ch	8	MSS_RCM_WDT1_CLK_GATE	RW	5320 832Ch
330h	8	MSS_RCM_WDT2_CLK_GATE	RW	5320 8330h
334h	8	MSS_RCM_WDT3_CLK_GATE	RW	5320 8334h
33Ch	8	MSS_RCM_MCSPI0_CLK_GATE	RW	5320 833Ch
340h	8	MSS_RCM_MCSPI1_CLK_GATE	RW	5320 8340h
344h	8	MSS_RCM_MCSPI2_CLK_GATE	RW	5320 8344h
348h	8	MSS_RCM_MCSPI3_CLK_GATE	RW	5320 8348h
34Ch	8	MSS_RCM_MCSPI4_CLK_GATE	RW	5320 834Ch
350h	8	MSS_RCM_MMC0_CLK_GATE	RW	5320 8350h
354h	8	MSS_RCM_ICSSM0_UART_CLK_GATE	RW	5320 8354h
358h	8	MSS_RCM_CPTS_CLK_GATE	RW	5320 8358h
35Ch	8	MSS_RCM_GPMC_CLK_GATE	RW	5320 835Ch
360h	8	MSS_RCM_CONTROLSS_PLL_CLK_GATE	RW	5320 8360h
364h	8	MSS_RCM_I2C0_CLK_GATE	RW	5320 8364h
368h	8	MSS_RCM_I2C1_CLK_GATE	RW	5320 8368h
36Ch	8	MSS_RCM_I2C2_CLK_GATE	RW	5320 836Ch
370h	8	MSS_RCM_I2C3_CLK_GATE	RW	5320 8370h
374h	8	MSS_RCM_LIN0_CLK_GATE	RW	5320 8374h
378h	8	MSS_RCM_LIN1_CLK_GATE	RW	5320 8378h
37Ch	8	MSS_RCM_LIN2_CLK_GATE	RW	5320 837Ch
380h	8	MSS_RCM_LIN3_CLK_GATE	RW	5320 8380h
384h	8	MSS_RCM_LIN4_CLK_GATE	RW	5320 8384h
38Ch	8	MSS_RCM_UART0_CLK_GATE	RW	5320 838Ch
390h	8	MSS_RCM_UART1_CLK_GATE	RW	5320 8390h
394h	8	MSS_RCM_UART2_CLK_GATE	RW	5320 8394h
398h	8	MSS_RCM_UART3_CLK_GATE	RW	5320 8398h
39Ch	8	MSS_RCM_UART4_CLK_GATE	RW	5320 839Ch
3A0h	8	MSS_RCM_UART5_CLK_GATE	RW	5320 83A0h
3A4h	8	MSS_RCM_RGMII_250_CLK_GATE	RW	5320 83A4h
3A8h	8	MSS_RCM_RGMII_50_CLK_GATE	RW	5320 83A8h
3ACh	8	MSS_RCM_RGMII_5_CLK_GATE	RW	5320 83ACh
3B0h	8	MSS_RCM_MMC0_32K_CLK_GATE	RW	5320 83B0h
3B4h	8	MSS_RCM_TEMPSENSE_32K_CLK_GATE	RW	5320 83B4h
3B8h	8	MSS_RCM_CPSW_CLK_GATE	RW	5320 83B8h
3BCh	8	MSS_RCM_ICSSM0_IEP_CLK_GATE	RW	5320 83BCh
3C0h	8	MSS_RCM_ICSSM0_CORE_CLK_GATE	RW	5320 83C0h
3C4h	8	MSS_RCM_MSS_ICSSM_SYS_CLK_GATE	RW	5320 83C4h
3C8h	8	MSS_RCM_MSS_ELM_CLK_GATE	RW	5320 83C8h

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
3CCh	8	MSS_RCM_R5SS0_CORE0_GATE	RW	5320 83CCh
3D0h	8	MSS_RCM_R5SS1_CORE0_GATE	RW	5320 83D0h
3D4h	8	MSS_RCM_R5SS0_CORE1_GATE	RW	5320 83D4h
3D8h	8	MSS_RCM_R5SS1_CORE1_GATE	RW	5320 83D8h
400h	16	MSS_RCM_MCAN0_CLK_STATUS	RO	5320 8400h
404h	16	MSS_RCM_MCAN1_CLK_STATUS	RO	5320 8404h
408h	16	MSS_RCM_MCAN2_CLK_STATUS	RO	5320 8408h
40Ch	16	MSS_RCM_MCAN3_CLK_STATUS	RO	5320 840Ch
410h	16	MSS_RCM_QSPI0_CLK_STATUS	RO	5320 8410h
414h	16	MSS_RCM_RTI0_CLK_STATUS	RO	5320 8414h
418h	16	MSS_RCM_RTI1_CLK_STATUS	RO	5320 8418h
41Ch	16	MSS_RCM_RTI2_CLK_STATUS	RO	5320 841Ch
420h	16	MSS_RCM_RTI3_CLK_STATUS	RO	5320 8420h
428h	16	MSS_RCM_WDT0_CLK_STATUS	RO	5320 8428h
42Ch	16	MSS_RCM_WDT1_CLK_STATUS	RO	5320 842Ch
430h	16	MSS_RCM_WDT2_CLK_STATUS	RO	5320 8430h
434h	16	MSS_RCM_WDT3_CLK_STATUS	RO	5320 8434h
43Ch	16	MSS_RCM_MCSPI0_CLK_STATUS	RO	5320 843Ch
440h	16	MSS_RCM_MCSPI1_CLK_STATUS	RO	5320 8440h
444h	16	MSS_RCM_MCSPI2_CLK_STATUS	RO	5320 8444h
448h	16	MSS_RCM_MCSPI3_CLK_STATUS	RO	5320 8448h
44Ch	16	MSS_RCM_MCSPI4_CLK_STATUS	RO	5320 844Ch
450h	16	MSS_RCM_MMC0_CLK_STATUS	RO	5320 8450h
454h	16	MSS_RCM_ICSSM0_UART_CLK_STATUS	RO	5320 8454h
458h	16	MSS_RCM_CPTS_CLK_STATUS	RO	5320 8458h
45Ch	16	MSS_RCM_GPMC_CLK_STATUS	RO	5320 845Ch
460h	16	MSS_RCM_CONTROLSS_PLL_CLK_STATUS	RO	5320 8460h
464h	16	MSS_RCM_I2C_CLK_STATUS	RO	5320 8464h
474h	16	MSS_RCM_LIN0_UART0_CLK_STATUS	RO	5320 8474h
478h	16	MSS_RCM_LIN1_UART1_CLK_STATUS	RO	5320 8478h
47Ch	16	MSS_RCM_LIN2_UART2_CLK_STATUS	RO	5320 847Ch
480h	16	MSS_RCM_LIN3_UART3_CLK_STATUS	RO	5320 8480h
484h	16	MSS_RCM_LIN4_UART4_CLK_STATUS	RO	5320 8484h
488h	16	MSS_RCM_LIN5_UART5_CLK_STATUS	RO	5320 8488h
48Ch	16	MSS_RCM_RGMII_250_CLK_STATUS	RO	5320 848Ch
490h	16	MSS_RCM_RGMII_50_CLK_STATUS	RO	5320 8490h
494h	16	MSS_RCM_RGMII_5_CLK_STATUS	RO	5320 8494h
49Ch	24	MSS_RCM_MMC0_32K_CLK_STATUS	RO	5320 849Ch
4A0h	24	MSS_RCM_TEMPSENSE_32K_CLK_STATUS	RO	5320 84A0h
4A4h	16	MSS_RCM_MSS_ELM_CLK_STATUS	RO	5320 84A4h
500h	8	MSS_RCM_R5SS0_POR_RST_CTRL	RW	5320 8500h
504h	8	MSS_RCM_R5SS1_POR_RST_CTRL	RW	5320 8504h
508h	8	MSS_RCM_R5SS0_CORE0_GRST_CTRL	RW	5320 8508h
50Ch	8	MSS_RCM_R5SS1_CORE0_GRST_CTRL	RW	5320 850Ch
510h	8	MSS_RCM_R5SS0_CORE1_GRST_CTRL	RW	5320 8510h

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
514h	8	MSS_RCM_R5SS1_CORE1_GRST_CTRL	RW	5320 8514h
518h	8	MSS_RCM_R5SS0_CORE0_LRST_CTRL	RW	5320 8518h
51Ch	8	MSS_RCM_R5SS1_CORE0_LRST_CTRL	RW	5320 851Ch
520h	8	MSS_RCM_R5SS0_CORE1_LRST_CTRL	RW	5320 8520h
524h	8	MSS_RCM_R5SS1_CORE1_LRST_CTRL	RW	5320 8524h
528h	8	MSS_RCM_R5SS0_VIM0_RST_CTRL	RW	5320 8528h
52Ch	8	MSS_RCM_R5SS1_VIM0_RST_CTRL	RW	5320 852Ch
530h	8	MSS_RCM_R5SS0_VIM1_RST_CTRL	RW	5320 8530h
534h	8	MSS_RCM_R5SS1_VIM1_RST_CTRL	RW	5320 8534h
538h	8	MSS_RCM_MCRC0_RST_CTRL	RW	5320 8538h
53Ch	8	MSS_RCM_RTI0_RST_CTRL	RW	5320 853Ch
540h	8	MSS_RCM_RTI1_RST_CTRL	RW	5320 8540h
544h	8	MSS_RCM_RTI2_RST_CTRL	RW	5320 8544h
548h	8	MSS_RCM_RTI3_RST_CTRL	RW	5320 8548h
54Ch	8	MSS_RCM_WDT0_RST_CTRL	RW	5320 854Ch
550h	8	MSS_RCM_WDT1_RST_CTRL	RW	5320 8550h
554h	8	MSS_RCM_WDT2_RST_CTRL	RW	5320 8554h
558h	8	MSS_RCM_WDT3_RST_CTRL	RW	5320 8558h
55Ch	8	MSS_RCM_TOP_ESM_RST_CTRL	RW	5320 855Ch
560h	8	MSS_RCM_DCC0_RST_CTRL	RW	5320 8560h
564h	8	MSS_RCM_DCC1_RST_CTRL	RW	5320 8564h
568h	8	MSS_RCM_DCC2_RST_CTRL	RW	5320 8568h
56Ch	8	MSS_RCM_DCC3_RST_CTRL	RW	5320 856Ch
570h	8	MSS_RCM_MCSPI0_RST_CTRL	RW	5320 8570h
574h	8	MSS_RCM_MCSPI1_RST_CTRL	RW	5320 8574h
578h	8	MSS_RCM_MCSPI2_RST_CTRL	RW	5320 8578h
57Ch	8	MSS_RCM_MCSPI3_RST_CTRL	RW	5320 857Ch
580h	8	MSS_RCM_MCSPI4_RST_CTRL	RW	5320 8580h
584h	8	MSS_RCM_QSPI0_RST_CTRL	RW	5320 8584h
588h	8	MSS_RCM_MCAN0_RST_CTRL	RW	5320 8588h
58Ch	8	MSS_RCM_MCAN1_RST_CTRL	RW	5320 858Ch
590h	8	MSS_RCM_MCAN2_RST_CTRL	RW	5320 8590h
594h	8	MSS_RCM_MCAN3_RST_CTRL	RW	5320 8594h
598h	8	MSS_RCM_I2C0_RST_CTRL	RW	5320 8598h
59Ch	8	MSS_RCM_I2C1_RST_CTRL	RW	5320 859Ch
5A0h	8	MSS_RCM_I2C2_RST_CTRL	RW	5320 85A0h
5A4h	8	MSS_RCM_I2C3_RST_CTRL	RW	5320 85A4h
5A8h	8	MSS_RCM_UART0_RST_CTRL	RW	5320 85A8h
5ACh	8	MSS_RCM_UART1_RST_CTRL	RW	5320 85ACh
5B0h	8	MSS_RCM_UART2_RST_CTRL	RW	5320 85B0h
5B4h	8	MSS_RCM_UART3_RST_CTRL	RW	5320 85B4h
5B8h	8	MSS_RCM_UART4_RST_CTRL	RW	5320 85B8h
5BCh	8	MSS_RCM_UART5_RST_CTRL	RW	5320 85BCh
5C0h	8	MSS_RCM_LIN0_RST_CTRL	RW	5320 85C0h
5C4h	8	MSS_RCM_LIN1_RST_CTRL	RW	5320 85C4h
5C8h	8	MSS_RCM_LIN2_RST_CTRL	RW	5320 85C8h

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
5CCh	8	MSS_RCM_LIN3_RST_CTRL	RW	5320 85CCh
5D0h	8	MSS_RCM_LIN4_RST_CTRL	RW	5320 85D0h
5D8h	16	MSS_RCM_EDMA_RST_CTRL	RW	5320 85D8h
5DCh	8	MSS_RCM_INFRA_RST_CTRL	RW	5320 85DCh
5E0h	8	MSS_RCM_CPSW_RST_CTRL	RW	5320 85E0h
5E4h	8	MSS_RCM_ICSSM0_RST_CTRL	RW	5320 85E4h
5E8h	8	MSS_RCM_MMC0_RST_CTRL	RW	5320 85E8h
5ECh	8	MSS_RCM_GPIO0_RST_CTRL	RW	5320 85ECh
5F0h	8	MSS_RCM_GPIO1_RST_CTRL	RW	5320 85F0h
5F4h	8	MSS_RCM_GPIO2_RST_CTRL	RW	5320 85F4h
5F8h	8	MSS_RCM_GPIO3_RST_CTRL	RW	5320 85F8h
5FCh	8	MSS_RCM_SPINLOCK0_RST_CTRL	RW	5320 85FCh
600h	8	MSS_RCM_GPMC_RST_CTRL	RW	5320 8600h
604h	8	MSS_RCM_TEMPSENSE_32K_RST_CTRL	RW	5320 8604h
608h	8	MSS_RCM_MSS_ELM_RST_CTRL	RW	5320 8608h
700h	16	MSS_RCM_L2OCRAM_BANK0_PD_CTRL	RW	5320 8700h
704h	16	MSS_RCM_L2OCRAM_BANK1_PD_CTRL	RW	5320 8704h
708h	16	MSS_RCM_L2OCRAM_BANK2_PD_CTRL	RW	5320 8708h
70Ch	16	MSS_RCM_L2OCRAM_BANK3_PD_CTRL	RW	5320 870Ch
710h	8	MSS_RCM_L2OCRAM_BANK0_PD_STATUS	RO	5320 8710h
714h	8	MSS_RCM_L2OCRAM_BANK1_PD_STATUS	RO	5320 8714h
718h	8	MSS_RCM_L2OCRAM_BANK2_PD_STATUS	RO	5320 8718h
71Ch	8	MSS_RCM_L2OCRAM_BANK3_PD_STATUS	RO	5320 871Ch
720h	32	MSS_RCM_HW_REG0	RW	5320 8720h
724h	32	MSS_RCM_HW_REG1	RW	5320 8724h
728h	32	MSS_RCM_HW_REG2	RW	5320 8728h
72Ch	32	MSS_RCM_HW_REG3	RW	5320 872Ch
800h	16	MSS_RCM_HSM_RTIA_CLK_SRC_SEL	RW	5320 8800h
804h	16	MSS_RCM_HSM_WDT_CLK_SRC_SEL	RW	5320 8804h
808h	16	MSS_RCM_HSM_RTC_CLK_SRC_SEL	RW	5320 8808h
80Ch	16	MSS_RCM_HSM_DMTA_CLK_SRC_SEL	RW	5320 880Ch
810h	16	MSS_RCM_HSM_DMTB_CLK_SRC_SEL	RW	5320 8810h
814h	16	MSS_RCM_HSM_RTI_CLK_DIV_VAL	RW	5320 8814h
818h	16	MSS_RCM_HSM_WDT_CLK_DIV_VAL	RW	5320 8818h
81Ch	16	MSS_RCM_HSM_RTC_CLK_DIV_VAL	RW	5320 881Ch
820h	16	MSS_RCM_HSM_DMTA_CLK_DIV_VAL	RW	5320 8820h
824h	16	MSS_RCM_HSM_DMTB_CLK_DIV_VAL	RW	5320 8824h
828h	8	MSS_RCM_HSM_RTI_CLK_GATE	RW	5320 8828h
82Ch	8	MSS_RCM_HSM_WDT_CLK_GATE	RW	5320 882Ch
830h	8	MSS_RCM_HSM_RTC_CLK_GATE	RW	5320 8830h
834h	8	MSS_RCM_HSM_DMTA_CLK_GATE	RW	5320 8834h
838h	8	MSS_RCM_HSM_DMTB_CLK_GATE	RW	5320 8838h
83Ch	16	MSS_RCM_HSM_RTI_CLK_STATUS	RO	5320 883Ch

Table 2-527. MSS_RCM, MSS_RCM_MSS_RCM Registers, Base Address=5320 8000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
840h	16	MSS_RCM_HSM_WDT_CLK_STATUS	RO	5320 8840h
844h	16	MSS_RCM_HSM_RTC_CLK_STATUS	RO	5320 8844h
848h	16	MSS_RCM_HSM_DMTA_CLK_STATUS	RO	5320 8848h
84Ch	16	MSS_RCM_HSM_DMTB_CLK_STATUS	RO	5320 884Ch
FD0h	32	MSS_RCM_HW_SPARE_RW0	RW	5320 8FD0h
FD4h	32	MSS_RCM_HW_SPARE_RW1	RW	5320 8FD4h
FD8h	32	MSS_RCM_HW_SPARE_RW2	RW	5320 8FD8h
FDCh	32	MSS_RCM_HW_SPARE_RW3	RW	5320 8FDCh
FE0h	32	MSS_RCM_HW_SPARE_RO0	RO	5320 8FE0h
FE4h	32	MSS_RCM_HW_SPARE_RO1	RO	5320 8FE4h
FE8h	32	MSS_RCM_HW_SPARE_RO2	RO	5320 8FE8h
FECh	32	MSS_RCM_HW_SPARE_RO3	RO	5320 8FECh
FF0h	32	MSS_RCM_HW_SPARE_WPH	RW	5320 8FF0h
FF4h	32	MSS_RCM_HW_SPARE_REC	RW	5320 8FF4h
1008h	32	MSS_RCM_LOCK0_KICK0	- KICK0 component	5320 9008h
100Ch	32	MSS_RCM_LOCK0_KICK1	- KICK1 component	5320 900Ch
1010h	8	MSS_RCM_INTR_RAW_STATUS	Interrupt Raw Status/Set Register	5320 9010h
1014h	8	MSS_RCM_INTR_ENABLED_STATUS_CLEAR	Interrupt Enabled Status/Clear register	5320 9014h
1018h	8	MSS_RCM_INTR_ENABLE	Interrupt Enable register	5320 9018h
101Ch	8	MSS_RCM_INTR_ENABLE_CLEAR	Interrupt Enable Clear register	5320 901Ch
1020h	8	MSS_RCM_EOI	EOI register	5320 9020h
1024h	32	MSS_RCM_FAULT_ADDRESS	Fault Address register	5320 9024h
1028h	8	MSS_RCM_FAULT_TYPE_STATUS	Fault Type Status register	5320 9028h
102Ch	32	MSS_RCM_FAULT_ATTR_STATUS	Fault Attribute Status register	5320 902Ch
1030h	0	MSS_RCM_FAULT_CLEAR	Fault Clear register	5320 9030h

2.5.1 MSS_RCM_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 2-528. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8000h

Figure 2-262. MSS_RCM_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 2-529. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

2.5.2 MSS_RCM_R5SS0_RST_STATUS Register (Offset = 10h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-530. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8010h

Figure 2-263. MSS_RCM_R5SS0_RST_STATUS Name Register

15	14	13	12	11	10	9	8
RESERVED					CAUSE		
NONE					RO		
0					11		
7	6	5	4	3	2	1	0
CAUSE							
RO							
11							

Access Types Legend

Table 2-531. R5SS0_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	CAUSE	RO	Bh	Has the status because of which reset has happened. Bit0: POR ResetBit1: Warm Reset (ALso set during POR Reset)Bit2: CR5SS0 STC ResetBit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRLBit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRLBit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRLBit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRLBit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0

2.5.3 MSS_RCM_R5SS0_RST_CAUSE_CLR Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-532. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8014h

Figure 2-264. MSS_RCM_R5SS0_RST_CAUSE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLR	
NONE						RW	
0						0	

Access Types Legend

Table 2-533. R5SS0_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLR	RW	0h	Write pulse bit field:Clear bit for rst cause register (writing '111' will clear the rst cause register)

2.5.4 MSS_RCM_R5SS0_DBG_RST_EN Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-534. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8018h

Figure 2-265. MSS_RCM_R5SS0_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					EN_CORE1										
NONE					RW										
0					0										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EN_CORE0		
NONE													RW		
0													0		

Access Types Legend

Table 2-535. R5SS0_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18 - 16	EN_CORE1	RW	0h	writing '111' will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
	RESERVED	NONE		Reserved
2 - 0	EN_CORE0	RW	0h	writing '111' will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

2.5.5 MSS_RCM_R5SS0_RST_ASSERDLY Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-536. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 801Ch

Figure 2-266. MSS_RCM_R5SS0_RST_ASSERDLY Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
COUNT							
RW							
1111							

Access Types Legend

Table 2-537. R5SS0_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	COUNT	RW	457h	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this registerThe actual duration is count + 2 cycles. S/W Recommended value for this is 0x0FThe COUNT is applicable to both CPU cores

2.5.6 MSS_RCM_R5SS0_RST2ASSERTDLY Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-538. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8020h

Figure 2-267. MSS_RCM_R5SS0_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R5_CORE1_COUNT								R5_CORE0_COUNT							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5SS_CORE1_COUNT								R5SS_CORE0_COUNT							
RW								RW							
0								0							

Access Types Legend

Table 2-539. R5SS0_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	R5_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23 - 16	R5_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15 - 8	R5SS_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7 - 0	R5SS_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

2.5.7 MSS_RCM_R5SS0_RST_WFICHECK Register (Offset = 24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-540. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8024h

Figure 2-268. MSS_RCM_R5SS0_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					EN_R5_CORE1			RESERVED					EN_R5_CORE0		
NONE					RW			NONE					RW		
0					111			0					111		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					EN_R5SS_CORE1			RESERVED					EN_R5SS_CORE0		
NONE					RW			NONE					RW		
0					111			0					111		

Access Types Legend

Table 2-541. R5SS0_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	EN_R5_CORE1	RW	6Fh	writing '000' will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
18 - 16	EN_R5_CORE0	RW	6Fh	writing '000' will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
10 - 8	EN_R5SS_CORE1	RW	6Fh	writing '000' will disable check for WFI before global reset assertion of CORE1
	RESERVED	NONE		Reserved
2 - 0	EN_R5SS_CORE0	RW	6Fh	writing '000' will disable check for WFI before global reset assertion of CORE0

2.5.8 MSS_RCM_R5SS1_RST_STATUS Register (Offset = 30h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-542. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8030h

Figure 2-269. MSS_RCM_R5SS1_RST_STATUS Name Register

15	14	13	12	11	10	9	8
RESERVED					CAUSE		
NONE					RO		
0					11		
7	6	5	4	3	2	1	0
CAUSE							
RO							
11							

Access Types Legend

Table 2-543. R5SS1_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	CAUSE	RO	Bh	Has the status because of which reset has happened. Bit0: POR ResetBit1: Warm Reset (ALso set during POR Reset)Bit2: CR5SS1 STC ResetBit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRLBit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRLBit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRLBit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRLBit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0

2.5.9 MSS_RCM_R5SS1_RST_CAUSE_CLR Register (Offset = 34h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-544. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8034h

Figure 2-270. MSS_RCM_R5SS1_RST_CAUSE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLR	
NONE						RW	
0						0	

Access Types Legend

Table 2-545. R5SS1_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLR	RW	0h	Write pulse bit field:Clear bit for rst cause register (writing '111' will clear the rst cause register)

2.5.10 MSS_RCM_R5SS1_DBG_RST_EN Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

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Table 2-546. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8038h

Figure 2-271. MSS_RCM_R5SS1_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					EN_CORE1										
NONE					RW										
0					0										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EN_CORE0		
NONE													RW		
0													0		

Access Types Legend

Table 2-547. R5SS1_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18 - 16	EN_CORE1	RW	0h	writing '111' will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
	RESERVED	NONE		Reserved
2 - 0	EN_CORE0	RW	0h	writing '111' will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

2.5.11 MSS_RCM_R5SS1_RST_ASSERDLY Register (Offset = 3Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-548. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 803Ch

Figure 2-272. MSS_RCM_R5SS1_RST_ASSERDLY Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
COUNT							
RW							
1111							

Access Types Legend

Table 2-549. R5SS1_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	COUNT	RW	457h	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this registerThe actual duration is count + 2 cycles. S/W Recommended value for this is 0x0FThe COUNT is applicable to both CPU cores

2.5.12 MSS_RCM_R5SS1_RST2ASSERTDLY Register (Offset = 40h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-550. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8040h

Figure 2-273. MSS_RCM_R5SS1_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R5_CORE1_COUNT								R5_CORE0_COUNT							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5SS_CORE1_COUNT								R5SS_CORE0_COUNT							
RW								RW							
0								0							

Access Types Legend

Table 2-551. R5SS1_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	R5_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23 - 16	R5_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15 - 8	R5SS_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7 - 0	R5SS_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

2.5.13 MSS_RCM_R5SS1_RST_WFICHECK Register (Offset = 44h) [reset = h]

Short Description: RW

Long Description:

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Table 2-552. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8044h

Figure 2-274. MSS_RCM_R5SS1_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					EN_R5_CORE1			RESERVED					EN_R5_CORE0		
NONE					RW			NONE					RW		
0					111			0					111		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					EN_R5SS_CORE1			RESERVED					EN_R5SS_CORE0		
NONE					RW			NONE					RW		
0					111			0					111		

Access Types Legend

Table 2-553. R5SS1_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	EN_R5_CORE1	RW	6Fh	writing '000' will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
18 - 16	EN_R5_CORE0	RW	6Fh	writing '000' will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
10 - 8	EN_R5SS_CORE1	RW	6Fh	writing '000' will disable check for WFI before global reset assertion of CORE1
	RESERVED	NONE		Reserved
2 - 0	EN_R5SS_CORE0	RW	6Fh	writing '000' will disable check for WFI before global reset assertion of CORE0

2.5.14 MSS_RCM_MCAN0_CLK_SRC_SEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-554. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8100h

Figure 2-275. MSS_RCM_MCAN0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-555. MCAN0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.15 MSS_RCM_MCAN1_CLK_SRC_SEL Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-556. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8104h

Figure 2-276. MSS_RCM_MCAN1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-557. MCAN1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.16 MSS_RCM_MCAN2_CLK_SRC_SEL Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-558. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8108h

Figure 2-277. MSS_RCM_MCAN2_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-559. MCAN2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.17 MSS_RCM_MCAN3_CLK_SRC_SEL Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-560. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 810Ch

Figure 2-278. MSS_RCM_MCAN3_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-561. MCAN3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.18 MSS_RCM_QSPI0_CLK_SRC_SEL Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-562. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8110h

Figure 2-279. MSS_RCM_QSPI0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-563. QSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for QSPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.19 MSS_RCM_RTI0_CLK_SRC_SEL Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-564. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8114h

Figure 2-280. MSS_RCM_RTI0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-565. RTI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.20 MSS_RCM_RTI1_CLK_SRC_SEL Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-566. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8118h

Figure 2-281. MSS_RCM_RTI1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-567. RTI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.21 MSS_RCM_RTI2_CLK_SRC_SEL Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-568. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 811Ch

Figure 2-282. MSS_RCM_RTI2_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-569. RTI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.22 MSS_RCM_RTI3_CLK_SRC_SEL Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-570. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8120h

Figure 2-283. MSS_RCM_RTI3_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-571. RTI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.23 MSS_RCM_WDT0_CLK_SRC_SEL Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

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Table 2-572. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8128h

Figure 2-284. MSS_RCM_WDT0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-573. WDT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.24 MSS_RCM_WDT1_CLK_SRC_SEL Register (Offset = 12Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-574. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 812Ch

Figure 2-285. MSS_RCM_WDT1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-575. WDT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.25 MSS_RCM_WDT2_CLK_SRC_SEL Register (Offset = 130h) [reset = h]

Short Description: RW

Long Description:

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Table 2-576. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8130h

Figure 2-286. MSS_RCM_WDT2_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-577. WDT2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.26 MSS_RCM_WDT3_CLK_SRC_SEL Register (Offset = 134h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-578. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8134h

Figure 2-287. MSS_RCM_WDT3_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-579. WDT3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.27 MSS_RCM_MCSPI0_CLK_SRC_SEL Register (Offset = 13Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-580. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 813Ch

Figure 2-288. MSS_RCM_MCSPI0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-581. MCSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.28 MSS_RCM_MCSPI1_CLK_SRC_SEL Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-582. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8140h

Figure 2-289. MSS_RCM_MCSPI1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-583. MCSPI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.29 MSS_RCM_MCSPI2_CLK_SRC_SEL Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-584. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8144h

Figure 2-290. MSS_RCM_MCSPI2_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-585. MCSPI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.30 MSS_RCM_MCSPI3_CLK_SRC_SEL Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-586. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8148h

Figure 2-291. MSS_RCM_MCSPI3_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-587. MCSPI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.31 MSS_RCM_MCSPI4_CLK_SRC_SEL Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-588. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 814Ch

Figure 2-292. MSS_RCM_MCSPI4_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-589. MCSPI4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.32 MSS_RCM_MMC0_CLK_SRC_SEL Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-590. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8150h

Figure 2-293. MSS_RCM_MMC0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-591. MMC0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MMCSD.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.33 MSS_RCM_ICSSM0_UART0_CLK_SRC_SEL Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-592. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8154h

Figure 2-294. MSS_RCM_ICSSM0_UART0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-593. ICSSM0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for ICSSM_UCLK.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.34 MSS_RCM_CPTS_CLK_SRC_SEL Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-594. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8158h

Figure 2-295. MSS_RCM_CPTS_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-595. CPTS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for CPTS.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.35 MSS_RCM_GPMC_CLK_SRC_SEL Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-596. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 815Ch

Figure 2-296. MSS_RCM_GPMC_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				GPMC_CLK_SRC_SEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
GPMC_CLK_SRC_SEL							
RW							
0							

Access Types Legend

Table 2-597. GPMC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	GPMC_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for GPMC. Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.36 MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-598. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8160h

Figure 2-297. MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-599. CONTROLSS_PLL_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for CONTROLSS_PLL.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.37 MSS_RCM_I2C_CLK_SRC_SEL Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-600. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8164h

Figure 2-298. MSS_RCM_I2C_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-601. I2C_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for I2C.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.38 MSS_RCM_LIN0_UART0_CLK_SRC_SEL Register (Offset = 174h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-602. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8174h

Figure 2-299. MSS_RCM_LIN0_UART0_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-603. LIN0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.39 MSS_RCM_LIN1_UART1_CLK_SRC_SEL Register (Offset = 178h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-604. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8178h

Figure 2-300. MSS_RCM_LIN1_UART1_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-605. LIN1_UART1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.40 MSS_RCM_LIN2_UART2_CLK_SRC_SEL Register (Offset = 17Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-606. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 817Ch

Figure 2-301. MSS_RCM_LIN2_UART2_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-607. LIN2_UART2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.41 MSS_RCM_LIN3_UART3_CLK_SRC_SEL Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-608. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8180h

Figure 2-302. MSS_RCM_LIN3_UART3_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-609. LIN3_UART3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.42 MSS_RCM_LIN4_UART4_CLK_SRC_SEL Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-610. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8184h

Figure 2-303. MSS_RCM_LIN4_UART4_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-611. LIN4_UART4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.43 MSS_RCM_LIN5_UART5_CLK_SRC_SEL Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-612. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8188h

Figure 2-304. MSS_RCM_LIN5_UART5_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKSRCSEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKSRCSEL							
RW							
0							

Access Types Legend

Table 2-613. LIN5_UART5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.44 MSS_RCM_MCAN0_CLK_DIV_VAL Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-614. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8200h

Figure 2-305. MSS_RCM_MCAN0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-615. MCAN0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.Refer to AM602 clock planner for clock reference

2.5.45 MSS_RCM_MCAN1_CLK_DIV_VAL Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-616. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8204h

Figure 2-306. MSS_RCM_MCAN1_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-617. MCAN1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.Refer to AM602 clock planner for clock reference

2.5.46 MSS_RCM_MCAN2_CLK_DIV_VAL Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-618. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8208h

Figure 2-307. MSS_RCM_MCAN2_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-619. MCAN2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.Refer to AM602 clock planner for clock reference

2.5.47 MSS_RCM_MCAN3_CLK_DIV_VAL Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-620. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 820Ch

Figure 2-308. MSS_RCM_MCAN3_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-621. MCAN3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.Refer to AM602 clock planner for clock reference

2.5.48 MSS_RCM_QSPI0_CLK_DIV_VAL Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-622. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8210h

Figure 2-309. MSS_RCM_QSPI0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-623. QSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value QSPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.49 MSS_RCM_RTI0_CLK_DIV_VAL Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-624. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8214h

Figure 2-310. MSS_RCM_RTI0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-625. RTI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.50 MSS_RCM_RTI1_CLK_DIV_VAL Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-626. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8218h

Figure 2-311. MSS_RCM_RTI1_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-627. RTI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.51 MSS_RCM_RTI2_CLK_DIV_VAL Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-628. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 821Ch

Figure 2-312. MSS_RCM_RTI2_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-629. RTI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.52 MSS_RCM_RTI3_CLK_DIV_VAL Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-630. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8220h

Figure 2-313. MSS_RCM_RTI3_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-631. RTI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.53 MSS_RCM_WDT0_CLK_DIV_VAL Register (Offset = 228h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-632. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8228h

Figure 2-314. MSS_RCM_WDT0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-633. WDT0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.54 MSS_RCM_WDT1_CLK_DIV_VAL Register (Offset = 22Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-634. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 822Ch

Figure 2-315. MSS_RCM_WDT1_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-635. WDT1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.55 MSS_RCM_WDT2_CLK_DIV_VAL Register (Offset = 230h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-636. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8230h

Figure 2-316. MSS_RCM_WDT2_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-637. WDT2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.56 MSS_RCM_WDT3_CLK_DIV_VAL Register (Offset = 234h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-638. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8234h

Figure 2-317. MSS_RCM_WDT3_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-639. WDT3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.57 MSS_RCM_MCSPI0_CLK_DIV_VAL Register (Offset = 23Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-640. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 823Ch

Figure 2-318. MSS_RCM_MCSPI0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-641. MCSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.58 MSS_RCM_MCSPI1_CLK_DIV_VAL Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-642. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8240h

Figure 2-319. MSS_RCM_MCSPI1_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-643. MCSPI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.59 MSS_RCM_MCSPI2_CLK_DIV_VAL Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-644. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8244h

Figure 2-320. MSS_RCM_MCSPI2_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-645. MCSPI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.60 MSS_RCM_MCSPI3_CLK_DIV_VAL Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-646. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8248h

Figure 2-321. MSS_RCM_MCSPI3_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-647. MCSPI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.61 MSS_RCM_MCSPI4_CLK_DIV_VAL Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-648. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 824Ch

Figure 2-322. MSS_RCM_MCSPI4_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-649. MCSPI4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.62 MSS_RCM_MMC0_CLK_DIV_VAL Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-650. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8250h

Figure 2-323. MSS_RCM_MMC0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-651. MMC0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value MMCSD selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.63 MSS_RCM_ICSSM0_UART_CLK_DIV_VAL Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-652. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8254h

Figure 2-324. MSS_RCM_ICSSM0_UART_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-653. ICSSM0_UART_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value ICSSM_UCLK selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.64 MSS_RCM_CPTS_CLK_DIV_VAL Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-654. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8258h

Figure 2-325. MSS_RCM_CPTS_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-655. CPTS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value CPTS selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.65 MSS_RCM_GPMC_CLK_DIV_VAL Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-656. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 825Ch

Figure 2-326. MSS_RCM_GPMC_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-657. GPMC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value GPMC selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.66 MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-658. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8260h

Figure 2-327. MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-659. CONTROLSS_PLL_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value CONTROLSS_PLL selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.67 MSS_RCM_I2C_CLK_DIV_VAL Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-660. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8264h

Figure 2-328. MSS_RCM_I2C_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-661. I2C_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value I2C selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.68 MSS_RCM_LIN0_UART0_CLK_DIV_VAL Register (Offset = 274h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-662. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8274h

Figure 2-329. MSS_RCM_LIN0_UART0_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-663. LIN0_UART0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.69 MSS_RCM_LIN1_UART1_CLK_DIV_VAL Register (Offset = 278h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-664. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8278h

Figure 2-330. MSS_RCM_LIN1_UART1_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-665. LIN1_UART1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.70 MSS_RCM_LIN2_UART2_CLK_DIV_VAL Register (Offset = 27Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-666. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 827Ch

Figure 2-331. MSS_RCM_LIN2_UART2_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-667. LIN2_UART2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.71 MSS_RCM_LIN3_UART3_CLK_DIV_VAL Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-668. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8280h

Figure 2-332. MSS_RCM_LIN3_UART3_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-669. LIN3_UART3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.72 MSS_RCM_LIN4_UART4_CLK_DIV_VAL Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-670. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8284h

Figure 2-333. MSS_RCM_LIN4_UART4_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-671. LIN4_UART4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.73 MSS_RCM_LIN5_UART5_CLK_DIV_VAL Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-672. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8288h

Figure 2-334. MSS_RCM_LIN5_UART5_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-673. LIN5_UART5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.74 MSS_RCM_RGMII_250_CLK_DIV_VAL Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-674. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 828Ch

Figure 2-335. MSS_RCM_RGMII_250_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				100010001			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
100010001							

Access Types Legend

Table 2-675. RGMII_250_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	5F60811h	Divider value RGMII selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.75 MSS_RCM_RGMII_50_CLK_DIV_VAL Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-676. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8290h

Figure 2-336. MSS_RCM_RGMII_50_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				100110011001			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
100110011001							

Access Types Legend

Table 2-677. RGMII_50_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	174F058A79h	Divider value MII100 selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.76 MSS_RCM_RGMII_5_CLK_DIV_VAL Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-678. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8294h

Figure 2-337. MSS_RCM_RGMII_5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLKDIVR															
RW															
11000110110001101100011															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIVR															
RW															
11000110110001101100011															

Access Types Legend

Table 2-679. RGMII_5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	CLKDIVR	RW	2545131A7F6FEB953EBh	Divider value MII10 selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.77 MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-680. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8298h

Figure 2-338. MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKDIVR													
NONE		RW													
0		11000011001100001100110000 1100													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIVR															
RW															
11000011001100001100110000 1100															

Access Types Legend

Table 2-681. XTAL_MMC_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	CLKDIVR	RW	1636DF558 60E7A8EAE EB45F4Ch	Divider value for XTAL_32K clock.Data should be loaded as multibit. For example: if divider value of '0x30C' is required then '0x30CC330C' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.78 MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register (Offset = 29Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-682. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 829Ch

Figure 2-339. MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKDIVR													
NONE		RW													
0		11000011001100001100110000 1100													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIVR															
RW															
11000011001100001100110000 1100															

Access Types Legend

Table 2-683. XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	CLKDIVR	RW	1636DF558 60E7A8EAE EB45F4Ch	Divider value for XTAL_32K clock.Data should be loaded as multibit. For example: if divider value of '0x30C' is required then '0x30CC330C' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.79 MSS_RCM_MSS_ELM_CLK_DIV_VAL Register (Offset = 2A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-684. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82A0h

Figure 2-340. MSS_RCM_MSS_ELM_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				1100110011			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
1100110011							

Access Types Legend

Table 2-685. MSS_ELM_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	419258BBh	Divider value ELM clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.80 MSS_RCM_MCAN0_CLK_GATE Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-686. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8300h

Figure 2-341. MSS_RCM_MCAN0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-687. MCAN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding MCAN

2.5.81 MSS_RCM_MCAN1_CLK_GATE Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-688. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8304h

Figure 2-342. MSS_RCM_MCAN1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-689. MCAN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding MCAN

2.5.82 MSS_RCM_MCAN2_CLK_GATE Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-690. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8308h

Figure 2-343. MSS_RCM_MCAN2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-691. MCAN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding MCAN

2.5.83 MSS_RCM_MCAN3_CLK_GATE Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-692. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 830Ch

Figure 2-344. MSS_RCM_MCAN3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-693. MCAN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding MCAN

2.5.84 MSS_RCM_QSPI0_CLK_GATE Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-694. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8310h

Figure 2-345. MSS_RCM_QSPI0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-695. QSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for QSPI

2.5.85 MSS_RCM_RTI0_CLK_GATE Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-696. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8314h

Figure 2-346. MSS_RCM_RTI0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-697. RTI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding RTI

2.5.86 MSS_RCM_RTI1_CLK_GATE Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-698. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8318h

Figure 2-347. MSS_RCM_RTI1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-699. RTI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding RTI

2.5.87 MSS_RCM_RTI2_CLK_GATE Register (Offset = 31Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-700. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 831Ch

Figure 2-348. MSS_RCM_RTI2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-701. RTI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding RTI

2.5.88 MSS_RCM_RTI3_CLK_GATE Register (Offset = 320h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-702. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8320h

Figure 2-349. MSS_RCM_RTI3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-703. RTI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding RTI

2.5.89 MSS_RCM_WDT0_CLK_GATE Register (Offset = 328h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-704. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8328h

Figure 2-350. MSS_RCM_WDT0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-705. WDT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for WDT

2.5.90 MSS_RCM_WDT1_CLK_GATE Register (Offset = 32Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-706. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 832Ch

Figure 2-351. MSS_RCM_WDT1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-707. WDT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for WDT

2.5.91 MSS_RCM_WDT2_CLK_GATE Register (Offset = 330h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-708. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8330h

Figure 2-352. MSS_RCM_WDT2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-709. WDT2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for WDT

2.5.92 MSS_RCM_WDT3_CLK_GATE Register (Offset = 334h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-710. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8334h

Figure 2-353. MSS_RCM_WDT3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-711. WDT3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for WDT

2.5.93 MSS_RCM_MCSPI0_CLK_GATE Register (Offset = 33Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-712. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 833Ch

Figure 2-354. MSS_RCM_MCSPI0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-713. MCSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding SPI

2.5.94 MSS_RCM_MCSPI1_CLK_GATE Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-714. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8340h

Figure 2-355. MSS_RCM_MCSPI1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-715. MCSPI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding SPI

2.5.95 MSS_RCM_MCSPI2_CLK_GATE Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-716. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8344h

Figure 2-356. MSS_RCM_MCSPI2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-717. MCSPI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding SPI

2.5.96 MSS_RCM_MCSPI3_CLK_GATE Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-718. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8348h

Figure 2-357. MSS_RCM_MCSPI3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-719. MCSPI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding SPI

2.5.97 MSS_RCM_MCSPI4_CLK_GATE Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-720. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 834Ch

Figure 2-358. MSS_RCM_MCSPI4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-721. MCSPI4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for Corresponding SPI

2.5.98 MSS_RCM_MMC0_CLK_GATE Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-722. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8350h

Figure 2-359. MSS_RCM_MMC0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-723. MMC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for MMCSD

2.5.99 MSS_RCM_ICSSM0_UART_CLK_GATE Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-724. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8354h

Figure 2-360. MSS_RCM_ICSSM0_UART_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-725. ICSSM0_UART_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for ICSSM_UCLK

2.5.100 MSS_RCM_CPTS_CLK_GATE Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-726. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8358h

Figure 2-361. MSS_RCM_CPTS_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-727. CPTS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for CPTS

2.5.101 MSS_RCM_GPMC_CLK_GATE Register (Offset = 35Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-728. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 835Ch

Figure 2-362. MSS_RCM_GPMC_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-729. GPMC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for GPMC

2.5.102 MSS_RCM_CONTROLSS_PLL_CLK_GATE Register (Offset = 360h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-730. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8360h

Figure 2-363. MSS_RCM_CONTROLSS_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-731. CONTROLSS_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for CONTROLSS_PLL

2.5.103 MSS_RCM_I2C0_CLK_GATE Register (Offset = 364h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-732. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8364h

Figure 2-364. MSS_RCM_I2C0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-733. I2C0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for I2C

2.5.104 MSS_RCM_I2C1_CLK_GATE Register (Offset = 368h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-734. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8368h

Figure 2-365. MSS_RCM_I2C1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-735. I2C1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for I2C

2.5.105 MSS_RCM_I2C2_CLK_GATE Register (Offset = 36Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-736. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 836Ch

Figure 2-366. MSS_RCM_I2C2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-737. I2C2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for I2C

2.5.106 MSS_RCM_I2C3_CLK_GATE Register (Offset = 370h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-738. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8370h

Figure 2-367. MSS_RCM_I2C3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-739. I2C3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for I2C

2.5.107 MSS_RCM_LIN0_CLK_GATE Register (Offset = 374h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-740. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8374h

Figure 2-368. MSS_RCM_LIN0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-741. LIN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for SPIB

2.5.108 MSS_RCM_LIN1_CLK_GATE Register (Offset = 378h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-742. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8378h

Figure 2-369. MSS_RCM_LIN1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-743. LIN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for SPIB

2.5.109 MSS_RCM_LIN2_CLK_GATE Register (Offset = 37Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-744. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 837Ch

Figure 2-370. MSS_RCM_LIN2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-745. LIN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for SPIB

2.5.110 MSS_RCM_LIN3_CLK_GATE Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-746. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8380h

Figure 2-371. MSS_RCM_LIN3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-747. LIN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for SPIB

2.5.111 MSS_RCM_LIN4_CLK_GATE Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-748. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8384h

Figure 2-372. MSS_RCM_LIN4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-749. LIN4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for SPIB

2.5.112 MSS_RCM_UART0_CLK_GATE Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-750. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 838Ch

Figure 2-373. MSS_RCM_UART0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-751. UART0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.113 MSS_RCM_UART1_CLK_GATE Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-752. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8390h

Figure 2-374. MSS_RCM_UART1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-753. UART1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.114 MSS_RCM_UART2_CLK_GATE Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-754. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8394h

Figure 2-375. MSS_RCM_UART2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-755. UART2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.115 MSS_RCM_UART3_CLK_GATE Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-756. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8398h

Figure 2-376. MSS_RCM_UART3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-757. UART3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.116 MSS_RCM_UART4_CLK_GATE Register (Offset = 39Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-758. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 839Ch

Figure 2-377. MSS_RCM_UART4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-759. UART4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.117 MSS_RCM_UART5_CLK_GATE Register (Offset = 3A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-760. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A0h

Figure 2-378. MSS_RCM_UART5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-761. UART5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for corresponding UART

2.5.118 MSS_RCM_RGMII_250_CLK_GATE Register (Offset = 3A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-762. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A4h

Figure 2-379. MSS_RCM_RGMII_250_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-763. RGMII_250_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for RGMII

2.5.119 MSS_RCM_RGMII_50_CLK_GATE Register (Offset = 3A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-764. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A8h

Figure 2-380. MSS_RCM_RGMII_50_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-765. RGMII_50_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for MII100

2.5.120 MSS_RCM_RGMII_5_CLK_GATE Register (Offset = 3ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-766. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83ACh

Figure 2-381. MSS_RCM_RGMII_5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-767. RGMII_5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for MII10

2.5.121 MSS_RCM_MMC0_32K_CLK_GATE Register (Offset = 3B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-768. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B0h

Figure 2-382. MSS_RCM_MMC0_32K_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-769. MMC0_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for MMCSD_32K

2.5.122 MSS_RCM_TEMPSENSE_32K_CLK_GATE Register (Offset = 3B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-770. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B4h

Figure 2-383. MSS_RCM_TEMPSENSE_32K_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-771. TEMPSENSE_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for TEMPSENSE_32K

2.5.123 MSS_RCM_CPSW_CLK_GATE Register (Offset = 3B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-772. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B8h

Figure 2-384. MSS_RCM_CPSW_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-773. CPSW_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for CPSW CPPI

2.5.124 MSS_RCM_ICSSM0_IEP_CLK_GATE Register (Offset = 3BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-774. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83BCh

Figure 2-385. MSS_RCM_ICSSM0_IEP_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-775. ICSSM0_IEP_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for ICSSM_IEP

2.5.125 MSS_RCM_ICSSM0_CORE_CLK_GATE Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-776. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C0h

Figure 2-386. MSS_RCM_ICSSM0_CORE_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-777. ICSSM0_CORE_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for ICSSM_CORE

2.5.126 MSS_RCM_MSS_ICSSM_SYS_CLK_GATE Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-778. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C4h

Figure 2-387. MSS_RCM_MSS_ICSSM_SYS_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-779. MSS_ICSSM_SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for ICSSM_SYS

2.5.127 MSS_RCM_MSS_ELM_CLK_GATE Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-780. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C8h

Figure 2-388. MSS_RCM_MSS_ELM_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-781. MSS_ELM_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for ELM

2.5.128 MSS_RCM_R5SS0_CORE0_GATE Register (Offset = 3CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-782. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83CCh

Figure 2-389. MSS_RCM_R5SS0_CORE0_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKGATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-783. R5SS0_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	writing '111' will gate clock to CORE0 related peripherals inside Cortexr5ss

2.5.129 MSS_RCM_R5SS1_CORE0_GATE Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-784. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D0h

Figure 2-390. MSS_RCM_R5SS1_CORE0_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKGATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-785. R5SS1_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	writing '111' will gate clock to CORE0 related peripherals inside Cortexr5ss

2.5.130 MSS_RCM_R5SS0_CORE1_GATE Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-786. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D4h

Figure 2-391. MSS_RCM_R5SS0_CORE1_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKGATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-787. R5SS0_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	writing '111' will gate clock to CORE1 related peripherals inside Cortexr5ss

2.5.131 MSS_RCM_R5SS1_CORE1_GATE Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-788. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D8h

Figure 2-392. MSS_RCM_R5SS1_CORE1_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLKGATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-789. R5SS1_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	writing '111' will gate clock to CORE1 related peripherals inside Cortexr5ss

2.5.132 MSS_RCM_MCAN0_CLK_STATUS Register (Offset = 400h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-790. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8400h

Figure 2-393. MSS_RCM_MCAN0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-791. MCAN0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

2.5.133 MSS_RCM_MCAN1_CLK_STATUS Register (Offset = 404h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-792. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8404h

Figure 2-394. MSS_RCM_MCAN1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-793. MCAN1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

2.5.134 MSS_RCM_MCAN2_CLK_STATUS Register (Offset = 408h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-794. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8408h

Figure 2-395. MSS_RCM_MCAN2_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-795. MCAN2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

2.5.135 MSS_RCM_MCAN3_CLK_STATUS Register (Offset = 40Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-796. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 840Ch

Figure 2-396. MSS_RCM_MCAN3_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-797. MCAN3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

2.5.136 MSS_RCM_QSPI0_CLK_STATUS Register (Offset = 410h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-798. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8410h

Figure 2-397. MSS_RCM_QSPI0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-799. QSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for QSPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for QSPI

2.5.137 MSS_RCM_RTI0_CLK_STATUS Register (Offset = 414h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-800. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8414h

Figure 2-398. MSS_RCM_RTI0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-801. RTI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

2.5.138 MSS_RCM_RTI1_CLK_STATUS Register (Offset = 418h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-802. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8418h

Figure 2-399. MSS_RCM_RTI1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-803. RTI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

2.5.139 MSS_RCM_RTI2_CLK_STATUS Register (Offset = 41Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-804. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 841Ch

Figure 2-400. MSS_RCM_RTI2_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-805. RTI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

2.5.140 MSS_RCM_RTI3_CLK_STATUS Register (Offset = 420h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-806. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8420h

Figure 2-401. MSS_RCM_RTI3_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-807. RTI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

2.5.141 MSS_RCM_WDT0_CLK_STATUS Register (Offset = 428h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-808. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8428h

Figure 2-402. MSS_RCM_WDT0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-809. WDT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

2.5.142 MSS_RCM_WDT1_CLK_STATUS Register (Offset = 42Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-810. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 842Ch

Figure 2-403. MSS_RCM_WDT1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-811. WDT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

2.5.143 MSS_RCM_WDT2_CLK_STATUS Register (Offset = 430h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-812. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8430h

Figure 2-404. MSS_RCM_WDT2_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-813. WDT2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

2.5.144 MSS_RCM_WDT3_CLK_STATUS Register (Offset = 434h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-814. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8434h

Figure 2-405. MSS_RCM_WDT3_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-815. WDT3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

2.5.145 MSS_RCM_MCSPI0_CLK_STATUS Register (Offset = 43Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-816. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 843Ch

Figure 2-406. MSS_RCM_MCSPI0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-817. MCSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

2.5.146 MSS_RCM_MCSPI1_CLK_STATUS Register (Offset = 440h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-818. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8440h

Figure 2-407. MSS_RCM_MCSPI1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-819. MCSPI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

2.5.147 MSS_RCM_MCSPI2_CLK_STATUS Register (Offset = 444h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-820. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8444h

Figure 2-408. MSS_RCM_MCSPI2_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-821. MCSPI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

2.5.148 MSS_RCM_MCSPI3_CLK_STATUS Register (Offset = 448h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-822. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8448h

Figure 2-409. MSS_RCM_MCSPI3_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-823. MCSPI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

2.5.149 MSS_RCM_MCSPI4_CLK_STATUS Register (Offset = 44Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-824. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 844Ch

Figure 2-410. MSS_RCM_MCSPI4_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-825. MCSPI4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

2.5.150 MSS_RCM_MMC0_CLK_STATUS Register (Offset = 450h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-826. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8450h

Figure 2-411. MSS_RCM_MMC0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-827. MMC0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for MMCSD
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for MMCSD

2.5.151 MSS_RCM_ICSSM0_UART_CLK_STATUS Register (Offset = 454h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-828. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8454h

Figure 2-412. MSS_RCM_ICSSM0_UART_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-829. ICSSM0_UART_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for ICSSM_UCLK
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for ICSSM_UCLK

2.5.152 MSS_RCM_CPTS_CLK_STATUS Register (Offset = 458h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-830. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8458h

Figure 2-413. MSS_RCM_CPTS_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-831. CPTS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CPTS
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CPTS

2.5.153 MSS_RCM_GPMC_CLK_STATUS Register (Offset = 45Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-832. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 845Ch

Figure 2-414. MSS_RCM_GPMC_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-833. GPMC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for GPMC
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for GPMC

2.5.154 MSS_RCM_CONTROLSS_PLL_CLK_STATUS Register (Offset = 460h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-834. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8460h

Figure 2-415. MSS_RCM_CONTROLSS_PLL_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-835. CONTROLSS_PLL_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CONTROLSS_PLL
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CONTROLSS_PLL

2.5.155 MSS_RCM_I2C_CLK_STATUS Register (Offset = 464h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-836. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8464h

Figure 2-416. MSS_RCM_I2C_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-837. I2C_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for I2C
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for I2C

2.5.156 MSS_RCM_LIN0_UART0_CLK_STATUS Register (Offset = 474h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-838. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8474h

Figure 2-417. MSS_RCM_LIN0_UART0_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-839. LIN0_UART0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.157 MSS_RCM_LIN1_UART1_CLK_STATUS Register (Offset = 478h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-840. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8478h

Figure 2-418. MSS_RCM_LIN1_UART1_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-841. LIN1_UART1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.158 MSS_RCM_LIN2_UART2_CLK_STATUS Register (Offset = 47Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-842. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 847Ch

Figure 2-419. MSS_RCM_LIN2_UART2_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-843. LIN2_UART2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.159 MSS_RCM_LIN3_UART3_CLK_STATUS Register (Offset = 480h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-844. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8480h

Figure 2-420. MSS_RCM_LIN3_UART3_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-845. LIN3_UART3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.160 MSS_RCM_LIN4_UART4_CLK_STATUS Register (Offset = 484h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-846. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8484h

Figure 2-421. MSS_RCM_LIN4_UART4_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-847. LIN4_UART4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.161 MSS_RCM_LIN5_UART5_CLK_STATUS Register (Offset = 488h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-848. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8488h

Figure 2-422. MSS_RCM_LIN5_UART5_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-849. LIN5_UART5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

2.5.162 MSS_RCM_RGMII_250_CLK_STATUS Register (Offset = 48Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-850. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 848Ch

Figure 2-423. MSS_RCM_RGMII_250_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
1							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0							

Access Types Legend

Table 2-851. RGMII_250_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	1h	Status shows the current divider value choosen for RGMII
	RESERVED	NONE		Reserved

2.5.163 MSS_RCM_RGMII_50_CLK_STATUS Register (Offset = 490h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-852. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8490h

Figure 2-424. MSS_RCM_RGMII_50_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
1001							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0							

Access Types Legend

Table 2-853. RGMII_50_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	3E9h	Status shows the current divider value choosen for MII100
	RESERVED	NONE		Reserved

2.5.164 MSS_RCM_RGMII_5_CLK_STATUS Register (Offset = 494h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-854. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8494h

Figure 2-425. MSS_RCM_RGMII_5_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
1100011							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0							

Access Types Legend

Table 2-855. RGMII_5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	10C8EBh	Status shows the current divider value choosen for MII10
	RESERVED	NONE		Reserved

2.5.165 MSS_RCM_MMC0_32K_CLK_STATUS Register (Offset = 49Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-856. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 849Ch

Figure 2-426. MSS_RCM_MMC0_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						CURRDIVIDER									
NONE						RO									
0						1100001100									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRDIVIDER								RESERVED							
RO								NONE							
1100001100								0							

Access Types Legend

Table 2-857. MMC0_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17 - 8	CURRDIVIDER	RO	4190AF4Ch	Status shows the current divider value choosen for XTAL_32K
	RESERVED	NONE		Reserved

2.5.166 MSS_RCM_TEMPSENSE_32K_CLK_STATUS Register (Offset = 4A0h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-858. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A0h

Figure 2-427. MSS_RCM_TEMPSENSE_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						CURRDIVIDER									
NONE						RO									
0						1100001100									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRDIVIDER								RESERVED							
RO								NONE							
1100001100								0							

Access Types Legend

Table 2-859. TEMPSENSE_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17 - 8	CURRDIVIDER	RO	4190AF4Ch	Status shows the current divider value choosen for XTAL_32K
	RESERVED	NONE		Reserved

2.5.167 MSS_RCM_MSS_ELM_CLK_STATUS Register (Offset = 4A4h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-860. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A4h

Figure 2-428. MSS_RCM_MSS_ELM_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
11							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0							

Access Types Legend

Table 2-861. MSS_ELM_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	Bh	Status shows the current divider value choosen for ELM
	RESERVED	NONE		Reserved

2.5.168 MSS_RCM_R5SS0_POR_RST_CTRL Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-862. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8500h

Figure 2-429. MSS_RCM_R5SS0_POR_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-863. R5SS0_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will assert por reset to R5SS Read is always 000

2.5.169 MSS_RCM_R5SS1_POR_RST_CTRL Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-864. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8504h

Figure 2-430. MSS_RCM_R5SS1_POR_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-865. R5SS1_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will assert por reset to R5SS Read is always 000

2.5.170 MSS_RCM_R5SS0_CORE0_GRST_CTRL Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-866. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8508h

Figure 2-431. MSS_RCM_R5SS0_CORE0_GRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-867. R5SS0_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE0 and MSS_CORE0_VIM

2.5.171 MSS_RCM_R5SS1_CORE0_GRST_CTRL Register (Offset = 50Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-868. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 850Ch

Figure 2-432. MSS_RCM_R5SS1_CORE0_GRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-869. R5SS1_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE0 and MSS_CORE0_VIM

2.5.172 MSS_RCM_R5SS0_CORE1_GRST_CTRL Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-870. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8510h

Figure 2-433. MSS_RCM_R5SS0_CORE1_GRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-871. R5SS0_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE1 and MSS_CORE1_VIM

2.5.173 MSS_RCM_R5SS1_CORE1_GRST_CTRL Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-872. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8514h

Figure 2-434. MSS_RCM_R5SS1_CORE1_GRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-873. R5SS1_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE1 and MSS_CORE1_VIM

2.5.174 MSS_RCM_R5SS0_CORE0_LRST_CTRL Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-874. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8518h

Figure 2-435. MSS_RCM_R5SS0_CORE0_LRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-875. R5SS0_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE0 only

2.5.175 MSS_RCM_R5SS1_CORE0_LRST_CTRL Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-876. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 851Ch

Figure 2-436. MSS_RCM_R5SS1_CORE0_LRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-877. R5SS1_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE0 only

2.5.176 MSS_RCM_R5SS0_CORE1_LRST_CTRL Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-878. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8520h

Figure 2-437. MSS_RCM_R5SS0_CORE1_LRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-879. R5SS0_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE1 only

2.5.177 MSS_RCM_R5SS1_CORE1_LRST_CTRL Register (Offset = 524h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-880. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8524h

Figure 2-438. MSS_RCM_R5SS1_CORE1_LRST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-881. R5SS1_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:writing '111' will reset CORE1 only

2.5.178 MSS_RCM_R5SS0_VIM0_RST_CTRL Register (Offset = 528h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-882. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8528h

Figure 2-439. MSS_RCM_R5SS0_VIM0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-883. R5SS0_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_CORE0_VIM Writing 000 will deassert the reset

2.5.179 MSS_RCM_R5SS1_VIM0_RST_CTRL Register (Offset = 52Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-884. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 852Ch

Figure 2-440. MSS_RCM_R5SS1_VIM0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-885. R5SS1_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_CORE0_VIM Writing 000 will deassert the reset

2.5.180 MSS_RCM_R5SS0_VIM1_RST_CTRL Register (Offset = 530h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-886. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8530h

Figure 2-441. MSS_RCM_R5SS0_VIM1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-887. R5SS0_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_CORE1_VIM

2.5.181 MSS_RCM_R5SS1_VIM1_RST_CTRL Register (Offset = 534h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-888. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8534h

Figure 2-442. MSS_RCM_R5SS1_VIM1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-889. R5SS1_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_CORE1_VIM

2.5.182 MSS_RCM_MCRC0_RST_CTRL Register (Offset = 538h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-890. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8538h

Figure 2-443. MSS_RCM_MCRC0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-891. MCRC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MCRC

2.5.183 MSS_RCM_RTI0_RST_CTRL Register (Offset = 53Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-892. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 853Ch

Figure 2-444. MSS_RCM_RTI0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-893. RTI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding RTI

2.5.184 MSS_RCM_RTI1_RST_CTRL Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-894. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8540h

Figure 2-445. MSS_RCM_RTI1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-895. RTI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding RTI

2.5.185 MSS_RCM_RTI2_RST_CTRL Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-896. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8544h

Figure 2-446. MSS_RCM_RTI2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-897. RTI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding RTI

2.5.186 MSS_RCM_RTI3_RST_CTRL Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-898. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8548h

Figure 2-447. MSS_RCM_RTI3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-899. RTI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding RTI

2.5.187 MSS_RCM_WDT0_RST_CTRL Register (Offset = 54Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-900. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 854Ch

Figure 2-448. MSS_RCM_WDT0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-901. WDT0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset WDT

2.5.188 MSS_RCM_WDT1_RST_CTRL Register (Offset = 550h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-902. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8550h

Figure 2-449. MSS_RCM_WDT1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-903. WDT1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset WDT

2.5.189 MSS_RCM_WDT2_RST_CTRL Register (Offset = 554h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-904. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8554h

Figure 2-450. MSS_RCM_WDT2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-905. WDT2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset WDT

2.5.190 MSS_RCM_WDT3_RST_CTRL Register (Offset = 558h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-906. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8558h

Figure 2-451. MSS_RCM_WDT3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-907. WDT3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset WDT

2.5.191 MSS_RCM_TOP_ESM_RST_CTRL Register (Offset = 55Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-908. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 855Ch

Figure 2-452. MSS_RCM_TOP_ESM_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-909. TOP_ESM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset ESM

2.5.192 MSS_RCM_DCC0_RST_CTRL Register (Offset = 560h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-910. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8560h

Figure 2-453. MSS_RCM_DCC0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-911. DCC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset DCCA

2.5.193 MSS_RCM_DCC1_RST_CTRL Register (Offset = 564h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-912. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8564h

Figure 2-454. MSS_RCM_DCC1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-913. DCC1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset DCCB

2.5.194 MSS_RCM_DCC2_RST_CTRL Register (Offset = 568h) [reset = h]

Short Description: RW

Long Description:

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Table 2-914. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8568h

Figure 2-455. MSS_RCM_DCC2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-915. DCC2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset DCCC

2.5.195 MSS_RCM_DCC3_RST_CTRL Register (Offset = 56Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-916. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 856Ch

Figure 2-456. MSS_RCM_DCC3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-917. DCC3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset DCCD

2.5.196 MSS_RCM_MCSPI0_RST_CTRL Register (Offset = 570h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-918. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8570h

Figure 2-457. MSS_RCM_MCSPI0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-919. MCSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset Corresponding SPI

2.5.197 MSS_RCM_MCSPI1_RST_CTRL Register (Offset = 574h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-920. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8574h

Figure 2-458. MSS_RCM_MCSPI1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-921. MCSPI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset Corresponding SPI

2.5.198 MSS_RCM_MCSPI2_RST_CTRL Register (Offset = 578h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-922. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8578h

Figure 2-459. MSS_RCM_MCSPI2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-923. MCSPI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset Corresponding SPI

2.5.199 MSS_RCM_MCSPI3_RST_CTRL Register (Offset = 57Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-924. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 857Ch

Figure 2-460. MSS_RCM_MCSPI3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-925. MCSPI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset Corresponding SPI

2.5.200 MSS_RCM_MCSPI4_RST_CTRL Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-926. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8580h

Figure 2-461. MSS_RCM_MCSPI4_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-927. MCSPI4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset Corresponding SPI

2.5.201 MSS_RCM_QSPI0_RST_CTRL Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-928. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8584h

Figure 2-462. MSS_RCM_QSPI0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-929. QSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset QSPI

2.5.202 MSS_RCM_MCAN0_RST_CTRL Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-930. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8588h

Figure 2-463. MSS_RCM_MCAN0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-931. MCAN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding MCAN

2.5.203 MSS_RCM_MCAN1_RST_CTRL Register (Offset = 58Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-932. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 858Ch

Figure 2-464. MSS_RCM_MCAN1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-933. MCAN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding MCAN

2.5.204 MSS_RCM_MCAN2_RST_CTRL Register (Offset = 590h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-934. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8590h

Figure 2-465. MSS_RCM_MCAN2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-935. MCAN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding MCAN

2.5.205 MSS_RCM_MCAN3_RST_CTRL Register (Offset = 594h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-936. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8594h

Figure 2-466. MSS_RCM_MCAN3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-937. MCAN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding MCAN

2.5.206 MSS_RCM_I2C0_RST_CTRL Register (Offset = 598h) [reset = h]

Short Description: RW

Long Description:

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Table 2-938. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8598h

Figure 2-467. MSS_RCM_I2C0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-939. I2C0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding I2C

2.5.207 MSS_RCM_I2C1_RST_CTRL Register (Offset = 59Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-940. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 859Ch

Figure 2-468. MSS_RCM_I2C1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-941. I2C1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding I2C

2.5.208 MSS_RCM_I2C2_RST_CTRL Register (Offset = 5A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-942. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A0h

Figure 2-469. MSS_RCM_I2C2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-943. I2C2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding I2C

2.5.209 MSS_RCM_I2C3_RST_CTRL Register (Offset = 5A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-944. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A4h

Figure 2-470. MSS_RCM_I2C3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-945. I2C3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding I2C

2.5.210 MSS_RCM_UART0_RST_CTRL Register (Offset = 5A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-946. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A8h

Figure 2-471. MSS_RCM_UART0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-947. UART0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.211 MSS_RCM_UART1_RST_CTRL Register (Offset = 5ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-948. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ACh

Figure 2-472. MSS_RCM_UART1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-949. UART1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.212 MSS_RCM_UART2_RST_CTRL Register (Offset = 5B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-950. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B0h

Figure 2-473. MSS_RCM_UART2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-951. UART2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.213 MSS_RCM_UART3_RST_CTRL Register (Offset = 5B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-952. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B4h

Figure 2-474. MSS_RCM_UART3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-953. UART3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.214 MSS_RCM_UART4_RST_CTRL Register (Offset = 5B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-954. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B8h

Figure 2-475. MSS_RCM_UART4_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-955. UART4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.215 MSS_RCM_UART5_RST_CTRL Register (Offset = 5BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-956. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85BCh

Figure 2-476. MSS_RCM_UART5_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-957. UART5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding UART instance

2.5.216 MSS_RCM_LIN0_RST_CTRL Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-958. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C0h

Figure 2-477. MSS_RCM_LIN0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-959. LIN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset LIN

2.5.217 MSS_RCM_LIN1_RST_CTRL Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-960. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C4h

Figure 2-478. MSS_RCM_LIN1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-961. LIN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset LIN

2.5.218 MSS_RCM_LIN2_RST_CTRL Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-962. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C8h

Figure 2-479. MSS_RCM_LIN2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-963. LIN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset LIN

2.5.219 MSS_RCM_LIN3_RST_CTRL Register (Offset = 5CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-964. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85CCh

Figure 2-480. MSS_RCM_LIN3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-965. LIN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset LIN

2.5.220 MSS_RCM_LIN4_RST_CTRL Register (Offset = 5D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-966. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D0h

Figure 2-481. MSS_RCM_LIN4_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-967. LIN4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset LIN

2.5.221 MSS_RCM_EDMA_RST_CTRL Register (Offset = 5D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-968. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D8h

Figure 2-482. MSS_RCM_EDMA_RST_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED	TPTCA1_ASSERT			RESERVED	TPTCA0_ASSERT		
NONE	RW			NONE	RW		
0	0			0	0		
7	6	5	4	3	2	1	0
RESERVED	TPCCA_ASSERT			RESERVED	ASSERT		
NONE	RW			NONE	RW		
0	0			0	0		

Access Types Legend

Table 2-969. EDMA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
14 - 12	TPTCA1_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_TPTCA1
	RESERVED	NONE		Reserved
10 - 8	TPTCA0_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_TPTCA0
	RESERVED	NONE		Reserved
6 - 4	TPCCA_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS_TPCCA
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset EDMA

2.5.222 MSS_RCM_INFRA_RST_CTRL Register (Offset = 5DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-970. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85DCh

Figure 2-483. MSS_RCM_INFRA_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-971. INFRA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS INFRA

2.5.223 MSS_RCM_CPSW_RST_CTRL Register (Offset = 5E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-972. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E0h

Figure 2-484. MSS_RCM_CPSW_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-973. CPSW_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS CPSW

2.5.224 MSS_RCM_ICSSM0_RST_CTRL Register (Offset = 5E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-974. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E4h

Figure 2-485. MSS_RCM_ICSSM0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						ASSERT	
NONE						RW	
0						0	

Access Types Legend

Table 2-975. ICSSM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MSS ICSSM

2.5.225 MSS_RCM_MMC0_RST_CTRL Register (Offset = 5E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-976. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E8h

Figure 2-486. MSS_RCM_MMC0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-977. MMC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset MMCSD

2.5.226 MSS_RCM_GPIO0_RST_CTRL Register (Offset = 5ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-978. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ECh

Figure 2-487. MSS_RCM_GPIO0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-979. GPIO0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding GPIO

2.5.227 MSS_RCM_GPIO1_RST_CTRL Register (Offset = 5F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-980. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F0h

Figure 2-488. MSS_RCM_GPIO1_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-981. GPIO1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding GPIO

2.5.228 MSS_RCM_GPIO2_RST_CTRL Register (Offset = 5F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-982. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F4h

Figure 2-489. MSS_RCM_GPIO2_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-983. GPIO2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding GPIO

2.5.229 MSS_RCM_GPIO3_RST_CTRL Register (Offset = 5F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-984. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F8h

Figure 2-490. MSS_RCM_GPIO3_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-985. GPIO3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset corresponding GPIO

2.5.230 MSS_RCM_SPINLOCK0_RST_CTRL Register (Offset = 5FCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-986. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85FCh

Figure 2-491. MSS_RCM_SPINLOCK0_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-987. SPINLOCK0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset SPINLOCK

2.5.231 MSS_RCM_GPMC_RST_CTRL Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-988. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8600h

Figure 2-492. MSS_RCM_GPMC_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-989. GPMC_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset GPMC

2.5.232 MSS_RCM_TEMPSENSE_32K_RST_CTRL Register (Offset = 604h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-990. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8604h

Figure 2-493. MSS_RCM_TEMPSENSE_32K_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-991. TEMPSENSE_32K_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset TEMPSENSE

2.5.233 MSS_RCM_MSS_ELM_RST_CTRL Register (Offset = 608h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-992. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8608h

Figure 2-494. MSS_RCM_MSS_ELM_RST_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					ASSERT		
NONE					RW		
0					0		

Access Types Legend

Table 2-993. MSS_ELM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing '111' will reset ELM

2.5.234 MSS_RCM_L2OCRAM_BANK0_PD_CTRL Register (Offset = 700h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-994. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8700h

Figure 2-495. MSS_RCM_L2OCRAM_BANK0_PD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED						AGOODIN	
NONE						RW	
0						111	
7	6	5	4	3	2	1	0
RESERVED	AONIN			RESERVED		ISO	
NONE	RW			NONE		RW	
0	111			0		0	

Access Types Legend

Table 2-995. L2OCRAM_BANK0_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKA
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKA
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKA

2.5.235 MSS_RCM_L2OCRAM_BANK1_PD_CTRL Register (Offset = 704h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-996. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8704h

Figure 2-496. MSS_RCM_L2OCRAM_BANK1_PD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED					AGOODIN		
NONE					RW		
0					111		
7	6	5	4	3	2	1	0
RESERVED	AONIN			RESERVED	ISO		
NONE	RW			NONE	RW		
0	111			0	0		

Access Types Legend

Table 2-997. L2OCRAM_BANK1_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKB
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKB
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKB

2.5.236 MSS_RCM_L2OCRAM_BANK2_PD_CTRL Register (Offset = 708h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-998. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8708h

Figure 2-497. MSS_RCM_L2OCRAM_BANK2_PD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED						AGOODIN	
NONE						RW	
0						111	
7	6	5	4	3	2	1	0
RESERVED	AONIN			RESERVED		ISO	
NONE	RW			NONE		RW	
0	111			0		0	

Access Types Legend

Table 2-999. L2OCRAM_BANK2_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKC
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKC
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKC

2.5.237 MSS_RCM_L2OCRAM_BANK3_PD_CTRL Register (Offset = 70Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1000. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 870Ch

Figure 2-498. MSS_RCM_L2OCRAM_BANK3_PD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED						AGOODIN	
NONE						RW	
0						111	
7	6	5	4	3	2	1	0
RESERVED	AONIN			RESERVED		ISO	
NONE	RW			NONE		RW	
0	111			0		0	

Access Types Legend

Table 2-1001. L2OCRAM_BANK3_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKD
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKD
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKD

2.5.238 MSS_RCM_L2OCRAM_BANK0_PD_STATUS Register (Offset = 710h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1002. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8710h

Figure 2-499. MSS_RCM_L2OCRAM_BANK0_PD_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						AGOODOUT	AONOUT
NONE						RO	RO
0						1	1

Access Types Legend

Table 2-1003. L2OCRAM_BANK0_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKA
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKA

2.5.239 MSS_RCM_L2OCRAM_BANK1_PD_STATUS Register (Offset = 714h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1004. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8714h

Figure 2-500. MSS_RCM_L2OCRAM_BANK1_PD_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						AGOODOUT	AONOUT
NONE						RO	RO
0						1	1

Access Types Legend

Table 2-1005. L2OCRAM_BANK1_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKB
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKB

2.5.240 MSS_RCM_L2OCRAM_BANK2_PD_STATUS Register (Offset = 718h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1006. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8718h

Figure 2-501. MSS_RCM_L2OCRAM_BANK2_PD_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						AGOODOUT	AONOUT
NONE						RO	RO
0						1	1

Access Types Legend

Table 2-1007. L2OCRAM_BANK2_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKC
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKC

2.5.241 MSS_RCM_L2OCRAM_BANK3_PD_STATUS Register (Offset = 71Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1008. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 871Ch

Figure 2-502. MSS_RCM_L2OCRAM_BANK3_PD_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						AGOODOUT	AONOUT
NONE						RO	RO
0						1	1

Access Types Legend

Table 2-1009. L2OCRAM_BANK3_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKD
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKD

2.5.242 MSS_RCM_HW_REG0 Register (Offset = 720h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1010. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8720h

Figure 2-503. MSS_RCM_HW_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1011. HW_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

2.5.243 MSS_RCM_HW_REG1 Register (Offset = 724h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1012. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8724h

Figure 2-504. MSS_RCM_HW_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1013. HW_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

2.5.244 MSS_RCM_HW_REG2 Register (Offset = 728h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1014. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8728h

Figure 2-505. MSS_RCM_HW_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1015. HW_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

2.5.245 MSS_RCM_HW_REG3 Register (Offset = 72Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1016. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 872Ch

Figure 2-506. MSS_RCM_HW_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1017. HW_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

2.5.246 MSS_RCM_HSM_RTIA_CLK_SRC_SEL Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1018. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8800h

Figure 2-507. MSS_RCM_HSM_RTIA_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				HSM_RTI0_CLK_SRC_SEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
HSM_RTI0_CLK_SRC_SEL							
RW							
0							

Access Types Legend

Table 2-1019. HSM_RTIA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_RTI0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.247 MSS_RCM_HSM_WDT_CLK_SRC_SEL Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1020. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8804h

Figure 2-508. MSS_RCM_HSM_WDT_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				HSM_WDT0_CLK_SRC_SEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
HSM_WDT0_CLK_SRC_SEL							
RW							
0							

Access Types Legend

Table 2-1021. HSM_WDT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_WDT0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.248 MSS_RCM_HSM_RTC_CLK_SRC_SEL Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1022. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8808h

Figure 2-509. MSS_RCM_HSM_RTC_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				HSM_RTC0_CLK_SRC_SEL			
NONE				RW			
0				11101110111			
7	6	5	4	3	2	1	0
HSM_RTC0_CLK_SRC_SEL							
RW							
11101110111							

Access Types Legend

Table 2-1023. HSM_RTC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_RTC0_CLK_SRC_SEL	RW	295AD7F5Fh	Select line for selecting source clock for HSM_RTC.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.249 MSS_RCM_HSM_DMTA_CLK_SRC_SEL Register (Offset = 80Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1024. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 880Ch

Figure 2-510. MSS_RCM_HSM_DMTA_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				HSM_DTM0_CLK_SRC_SEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
HSM_DTM0_CLK_SRC_SEL							
RW							
0							

Access Types Legend

Table 2-1025. HSM_DMTA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_DTM0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_DMTA.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.250 MSS_RCM_HSM_DMTB_CLK_SRC_SEL Register (Offset = 810h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1026. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8810h

Figure 2-511. MSS_RCM_HSM_DMTB_CLK_SRC_SEL Name Register

15	14	13	12	11	10	9	8
RESERVED				HSM_DTM1_CLK_SRC_SEL			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
HSM_DTM1_CLK_SRC_SEL							
RW							
0							

Access Types Legend

Table 2-1027. HSM_DMTB_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_DTM1_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_DMTB.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Refer to AM602 clock spec for source clock reference

2.5.251 MSS_RCM_HSM_RTI_CLK_DIV_VAL Register (Offset = 814h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1028. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8814h

Figure 2-512. MSS_RCM_HSM_RTI_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-1029. HSM_RTI_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.252 MSS_RCM_HSM_WDT_CLK_DIV_VAL Register (Offset = 818h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1030. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8818h

Figure 2-513. MSS_RCM_HSM_WDT_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-1031. HSM_WDT_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.253 MSS_RCM_HSM_RTC_CLK_DIV_VAL Register (Offset = 81Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1032. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 881Ch

Figure 2-514. MSS_RCM_HSM_RTC_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-1033. HSM_RTC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM RTC selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.254 MSS_RCM_HSM_DMTA_CLK_DIV_VAL Register (Offset = 820h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1034. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8820h

Figure 2-515. MSS_RCM_HSM_DMTA_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-1035. HSM_DMTA_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM DMTA selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.255 MSS_RCM_HSM_DMTB_CLK_DIV_VAL Register (Offset = 824h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1036. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8824h

Figure 2-516. MSS_RCM_HSM_DMTB_CLK_DIV_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED				CLKDIVR			
NONE				RW			
0				0			
7	6	5	4	3	2	1	0
CLKDIVR							
RW							
0							

Access Types Legend

Table 2-1037. HSM_DMTB_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM DMTB selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

2.5.256 MSS_RCM_HSM_RTI_CLK_GATE Register (Offset = 828h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1038. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8828h

Figure 2-517. MSS_RCM_HSM_RTI_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-1039. HSM_RTI_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for HSM RTI

2.5.257 MSS_RCM_HSM_WDT_CLK_GATE Register (Offset = 82Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1040. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 882Ch

Figure 2-518. MSS_RCM_HSM_WDT_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-1041. HSM_WDT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for HSM WDT

2.5.258 MSS_RCM_HSM_RTC_CLK_GATE Register (Offset = 830h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1042. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8830h

Figure 2-519. MSS_RCM_HSM_RTC_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-1043. HSM_RTC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for HSM RTC

2.5.259 MSS_RCM_HSM_DMTA_CLK_GATE Register (Offset = 834h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1044. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8834h

Figure 2-520. MSS_RCM_HSM_DMTA_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						GATED	
NONE						RW	
0						0	

Access Types Legend

Table 2-1045. HSM_DMTA_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for HSM DMTA

2.5.260 MSS_RCM_HSM_DMTB_CLK_GATE Register (Offset = 838h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1046. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8838h

Figure 2-521. MSS_RCM_HSM_DMTB_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GATED		
NONE					RW		
0					0		

Access Types Legend

Table 2-1047. HSM_DMTB_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	writing '111' will gate clock for HSM DMTB

2.5.261 MSS_RCM_HSM_RTI_CLK_STATUS Register (Offset = 83Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1048. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 883Ch

Figure 2-522. MSS_RCM_HSM_RTI_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-1049. HSM_RTI_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_RTI

2.5.262 MSS_RCM_HSM_WDT_CLK_STATUS Register (Offset = 840h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1050. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8840h

Figure 2-523. MSS_RCM_HSM_WDT_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-1051. HSM_WDT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_WDT

2.5.263 MSS_RCM_HSM_RTC_CLK_STATUS Register (Offset = 844h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1052. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8844h

Figure 2-524. MSS_RCM_HSM_RTC_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
10000000							

Access Types Legend

Table 2-1053. HSM_RTC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_RTC
7 - 0	CLKINUSE	RO	989680h	Status shows the source clock slected for HSM_RTC

2.5.264 MSS_RCM_HSM_DMTA_CLK_STATUS Register (Offset = 848h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1054. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8848h

Figure 2-525. MSS_RCM_HSM_DMTA_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-1055. HSM_DMTA_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_DMTA
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_DMTA

2.5.265 MSS_RCM_HSM_DMTB_CLK_STATUS Register (Offset = 84Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1056. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 884Ch

Figure 2-526. MSS_RCM_HSM_DMTB_CLK_STATUS Name Register

15	14	13	12	11	10	9	8
CURRDIVIDER							
RO							
0							
7	6	5	4	3	2	1	0
CLKINUSE							
RO							
1							

Access Types Legend

Table 2-1057. HSM_DMTB_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_DMTB
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_DMTB

2.5.266 MSS_RCM_HW_SPARE_RW0 Register (Offset = FD0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1058. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD0h

Figure 2-527. MSS_RCM_HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW0															
RW															
0															

Access Types Legend

Table 2-1059. HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW0	RW	0h	Reserved for HW R&D

2.5.267 MSS_RCM_HW_SPARE_RW1 Register (Offset = FD4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1060. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD4h

Figure 2-528. MSS_RCM_HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW1															
RW															
0															

Access Types Legend

Table 2-1061. HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW1	RW	0h	Reserved for HW R&D

2.5.268 MSS_RCM_HW_SPARE_RW2 Register (Offset = FD8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1062. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD8h

Figure 2-529. MSS_RCM_HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW2															
RW															
0															

Access Types Legend

Table 2-1063. HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW2	RW	0h	Reserved for HW R&D

2.5.269 MSS_RCM_HW_SPARE_RW3 Register (Offset = FDCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1064. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FDCh

Figure 2-530. MSS_RCM_HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW3															
RW															
0															

Access Types Legend

Table 2-1065. HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW3	RW	0h	Reserved for HW R&D

2.5.270 MSS_RCM_HW_SPARE_RO0 Register (Offset = FE0h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1066. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE0h

Figure 2-531. MSS_RCM_HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO0															
RO															
0															

Access Types Legend

Table 2-1067. HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO0	RO	0h	Reserved for HW R&D

2.5.271 MSS_RCM_HW_SPARE_RO1 Register (Offset = FE4h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1068. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE4h

Figure 2-532. MSS_RCM_HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO1															
RO															
0															

Access Types Legend

Table 2-1069. HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO1	RO	0h	Reserved for HW R&D

2.5.272 MSS_RCM_HW_SPARE_RO2 Register (Offset = FE8h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1070. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE8h

Figure 2-533. MSS_RCM_HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO2															
RO															
0															

Access Types Legend

Table 2-1071. HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO2	RO	0h	Reserved for HW R&D

2.5.273 MSS_RCM_HW_SPARE_RO3 Register (Offset = FECh) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1072. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FECh

Figure 2-534. MSS_RCM_HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO3															
RO															
0															

Access Types Legend

Table 2-1073. HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO3	RO	0h	Reserved for HW R&D

2.5.274 MSS_RCM_HW_SPARE_WPH Register (Offset = FF0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1074. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FF0h

Figure 2-535. MSS_RCM_HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_WPH															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_WPH															
RW															
0															

Access Types Legend

Table 2-1075. HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_WPH	RW	0h	Reserved for HW R&D

2.5.275 MSS_RCM_HW_SPARE_REC Register (Offset = FF4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1076. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FF4h

Figure 2-536. MSS_RCM_HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_REC31	HW_SPARE_REC30	HW_SPARE_REC29	HW_SPARE_REC28	HW_SPARE_REC27	HW_SPARE_REC26	HW_SPARE_REC25	HW_SPARE_REC24	HW_SPARE_REC23	HW_SPARE_REC22	HW_SPARE_REC21	HW_SPARE_REC20	HW_SPARE_REC19	HW_SPARE_REC18	HW_SPARE_REC17	HW_SPARE_REC16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_REC15	HW_SPARE_REC14	HW_SPARE_REC13	HW_SPARE_REC12	HW_SPARE_REC11	HW_SPARE_REC10	HW_SPARE_REC9	HW_SPARE_REC8	HW_SPARE_REC7	HW_SPARE_REC6	HW_SPARE_REC5	HW_SPARE_REC4	HW_SPARE_REC3	HW_SPARE_REC2	HW_SPARE_REC1	HW_SPARE_REC0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 2-1077. HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC31	RW	0h	Reserved for HW R&D
30	HW_SPARE_REC30	RW	0h	Reserved for HW R&D
29	HW_SPARE_REC29	RW	0h	Reserved for HW R&D
28	HW_SPARE_REC28	RW	0h	Reserved for HW R&D
27	HW_SPARE_REC27	RW	0h	Reserved for HW R&D
26	HW_SPARE_REC26	RW	0h	Reserved for HW R&D
25	HW_SPARE_REC25	RW	0h	Reserved for HW R&D
24	HW_SPARE_REC24	RW	0h	Reserved for HW R&D
23	HW_SPARE_REC23	RW	0h	Reserved for HW R&D
22	HW_SPARE_REC22	RW	0h	Reserved for HW R&D
21	HW_SPARE_REC21	RW	0h	Reserved for HW R&D
20	HW_SPARE_REC20	RW	0h	Reserved for HW R&D
19	HW_SPARE_REC19	RW	0h	Reserved for HW R&D
18	HW_SPARE_REC18	RW	0h	Reserved for HW R&D
17	HW_SPARE_REC17	RW	0h	Reserved for HW R&D
16	HW_SPARE_REC16	RW	0h	Reserved for HW R&D
15	HW_SPARE_REC15	RW	0h	Reserved for HW R&D
14	HW_SPARE_REC14	RW	0h	Reserved for HW R&D
13	HW_SPARE_REC13	RW	0h	Reserved for HW R&D
12	HW_SPARE_REC12	RW	0h	Reserved for HW R&D
11	HW_SPARE_REC11	RW	0h	Reserved for HW R&D
10	HW_SPARE_REC10	RW	0h	Reserved for HW R&D
9	HW_SPARE_REC9	RW	0h	Reserved for HW R&D
8	HW_SPARE_REC8	RW	0h	Reserved for HW R&D

Table 2-1077. HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	HW_SPARE_REC7	RW	0h	Reserved for HW R&D
6	HW_SPARE_REC6	RW	0h	Reserved for HW R&D
5	HW_SPARE_REC5	RW	0h	Reserved for HW R&D
4	HW_SPARE_REC4	RW	0h	Reserved for HW R&D
3	HW_SPARE_REC3	RW	0h	Reserved for HW R&D
2	HW_SPARE_REC2	RW	0h	Reserved for HW R&D
1	HW_SPARE_REC1	RW	0h	Reserved for HW R&D
0	HW_SPARE_REC0	RW	0h	Reserved for HW R&D

2.5.276 MSS_RCM_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

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Table 2-1078. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9008h

Figure 2-537. MSS_RCM_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
RW															
0															

Access Types Legend

Table 2-1079. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

2.5.277 MSS_RCM_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-1080. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 900Ch

Figure 2-538. MSS_RCM_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
RW															
0															

Access Types Legend

Table 2-1081. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

2.5.278 MSS_RCM_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

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Table 2-1082. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9010h

Figure 2-539. MSS_RCM_INTR_RAW_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1083. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

2.5.279 MSS_RCM_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

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Table 2-1084. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9014h

Figure 2-540. MSS_RCM_INTR_ENABLED_STATUS_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1085. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

2.5.280 MSS_RCM_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

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Table 2-1086. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9018h

Figure 2-541. MSS_RCM_INTR_ENABLE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1087. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

2.5.281 MSS_RCM_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

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Table 2-1088. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 901Ch

Figure 2-542. MSS_RCM_INTR_ENABLE_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1089. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

2.5.282 MSS_RCM_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-1090. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9020h

Figure 2-543. MSS_RCM_EOI Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_VECTOR							
RW							
0							

Access Types Legend

Table 2-1091. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

2.5.283 MSS_RCM_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

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Table 2-1092. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9024h

Figure 2-544. MSS_RCM_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
RO															
0															

Access Types Legend

Table 2-1093. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

2.5.284 MSS_RCM_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

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Table 2-1094. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9028h

Figure 2-545. MSS_RCM_FAULT_TYPE_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	RO	RO					
0	0	0					

Access Types Legend

Table 2-1095. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

2.5.285 MSS_RCM_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

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Table 2-1096. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 902Ch

Figure 2-546. MSS_RCM_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
RO								RO							
0								0							

Access Types Legend

Table 2-1097. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

2.5.286 MSS_RCM_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 2-1098. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9030h

Figure 2-547. MSS_RCM_FAULT_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
FAULT_CLR							
WO							
0							

Access Types Legend

Table 2-1099. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

Table 2-1100. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

2.6 C2K_GLOBAL_CTRL Registers

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
0h	32	CONTROLSS_CTRL_PID	PID register	502F 0000h
4h	32	CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0	RW	502F 0004h
8h	32	CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1	RW	502F 0008h
10h	32	CONTROLSS_CTRL_EPWM_CLKSYNC	RW	502F 0010h
18h	0	CONTROLSS_CTRL_SDFM1_CLK0_SEL	RW	502F 0018h
20h	8	CONTROLSS_CTRL_EMUSTOPN_MASK	RW	502F 0020h
28h	32	CONTROLSS_CTRL_CLB_AQ_EN0	RW	502F 0028h
30h	32	CONTROLSS_CTRL_CLB_AQ_EN1	RW	502F 0030h
38h	32	CONTROLSS_CTRL_CLB_DB_EN0	RW	502F 0038h
40h	32	CONTROLSS_CTRL_CLB_DB_EN1	RW	502F 0040h
100h	8	CONTROLSS_CTRL_ETPWM0_CLK_GATE	RW	502F 0100h
104h	8	CONTROLSS_CTRL_ETPWM1_CLK_GATE	RW	502F 0104h
108h	8	CONTROLSS_CTRL_ETPWM2_CLK_GATE	RW	502F 0108h
10Ch	8	CONTROLSS_CTRL_ETPWM3_CLK_GATE	RW	502F 010Ch
110h	8	CONTROLSS_CTRL_ETPWM4_CLK_GATE	RW	502F 0110h
114h	8	CONTROLSS_CTRL_ETPWM5_CLK_GATE	RW	502F 0114h
118h	8	CONTROLSS_CTRL_ETPWM6_CLK_GATE	RW	502F 0118h
11Ch	8	CONTROLSS_CTRL_ETPWM7_CLK_GATE	RW	502F 011Ch
120h	8	CONTROLSS_CTRL_ETPWM8_CLK_GATE	RW	502F 0120h
124h	8	CONTROLSS_CTRL_ETPWM9_CLK_GATE	RW	502F 0124h
128h	8	CONTROLSS_CTRL_ETPWM10_CLK_GATE	RW	502F 0128h
12Ch	8	CONTROLSS_CTRL_ETPWM11_CLK_GATE	RW	502F 012Ch
130h	8	CONTROLSS_CTRL_ETPWM12_CLK_GATE	RW	502F 0130h
134h	8	CONTROLSS_CTRL_ETPWM13_CLK_GATE	RW	502F 0134h
138h	8	CONTROLSS_CTRL_ETPWM14_CLK_GATE	RW	502F 0138h
13Ch	8	CONTROLSS_CTRL_ETPWM15_CLK_GATE	RW	502F 013Ch
140h	8	CONTROLSS_CTRL_ETPWM16_CLK_GATE	RW	502F 0140h
144h	8	CONTROLSS_CTRL_ETPWM17_CLK_GATE	RW	502F 0144h
148h	8	CONTROLSS_CTRL_ETPWM18_CLK_GATE	RW	502F 0148h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
14Ch	8	CONTROLSS_CTRL_ETPWM19_CLK_GATE	RW	502F 014Ch
150h	8	CONTROLSS_CTRL_ETPWM20_CLK_GATE	RW	502F 0150h
154h	8	CONTROLSS_CTRL_ETPWM21_CLK_GATE	RW	502F 0154h
158h	8	CONTROLSS_CTRL_ETPWM22_CLK_GATE	RW	502F 0158h
15Ch	8	CONTROLSS_CTRL_ETPWM23_CLK_GATE	RW	502F 015Ch
160h	8	CONTROLSS_CTRL_ETPWM24_CLK_GATE	RW	502F 0160h
164h	8	CONTROLSS_CTRL_ETPWM25_CLK_GATE	RW	502F 0164h
168h	8	CONTROLSS_CTRL_ETPWM26_CLK_GATE	RW	502F 0168h
16Ch	8	CONTROLSS_CTRL_ETPWM27_CLK_GATE	RW	502F 016Ch
170h	8	CONTROLSS_CTRL_ETPWM28_CLK_GATE	RW	502F 0170h
174h	8	CONTROLSS_CTRL_ETPWM29_CLK_GATE	RW	502F 0174h
178h	8	CONTROLSS_CTRL_ETPWM30_CLK_GATE	RW	502F 0178h
17Ch	8	CONTROLSS_CTRL_ETPWM31_CLK_GATE	RW	502F 017Ch
180h	8	CONTROLSS_CTRL_FSI_TX0_CLK_GATE	RW	502F 0180h
184h	8	CONTROLSS_CTRL_FSI_TX1_CLK_GATE	RW	502F 0184h
188h	8	CONTROLSS_CTRL_FSI_TX2_CLK_GATE	RW	502F 0188h
18Ch	8	CONTROLSS_CTRL_FSI_TX3_CLK_GATE	RW	502F 018Ch
190h	8	CONTROLSS_CTRL_FSI_RX0_CLK_GATE	RW	502F 0190h
194h	8	CONTROLSS_CTRL_FSI_RX1_CLK_GATE	RW	502F 0194h
198h	8	CONTROLSS_CTRL_FSI_RX2_CLK_GATE	RW	502F 0198h
19Ch	8	CONTROLSS_CTRL_FSI_RX3_CLK_GATE	RW	502F 019Ch
1A0h	8	CONTROLSS_CTRL_CMPSSA0_CLK_GATE	RW	502F 01A0h
1A4h	8	CONTROLSS_CTRL_CMPSSA1_CLK_GATE	RW	502F 01A4h
1A8h	8	CONTROLSS_CTRL_CMPSSA2_CLK_GATE	RW	502F 01A8h
1ACh	8	CONTROLSS_CTRL_CMPSSA3_CLK_GATE	RW	502F 01ACh
1B0h	8	CONTROLSS_CTRL_CMPSSA4_CLK_GATE	RW	502F 01B0h
1B4h	8	CONTROLSS_CTRL_CMPSSA5_CLK_GATE	RW	502F 01B4h
1B8h	8	CONTROLSS_CTRL_CMPSSA6_CLK_GATE	RW	502F 01B8h
1BCh	8	CONTROLSS_CTRL_CMPSSA7_CLK_GATE	RW	502F 01BCh
1C0h	8	CONTROLSS_CTRL_CMPSSA8_CLK_GATE	RW	502F 01C0h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
1C4h	8	CONTROLSS_CTRL_CMPSSA9_CLK_GATE	RW	502F 01C4h
1D0h	8	CONTROLSS_CTRL_CMPSSB0_CLK_GATE	RW	502F 01D0h
1D4h	8	CONTROLSS_CTRL_CMPSSB1_CLK_GATE	RW	502F 01D4h
1D8h	8	CONTROLSS_CTRL_CMPSSB2_CLK_GATE	RW	502F 01D8h
1DCh	8	CONTROLSS_CTRL_CMPSSB3_CLK_GATE	RW	502F 01DCh
1E0h	8	CONTROLSS_CTRL_CMPSSB4_CLK_GATE	RW	502F 01E0h
1E4h	8	CONTROLSS_CTRL_CMPSSB5_CLK_GATE	RW	502F 01E4h
1E8h	8	CONTROLSS_CTRL_CMPSSB6_CLK_GATE	RW	502F 01E8h
1ECh	8	CONTROLSS_CTRL_CMPSSB7_CLK_GATE	RW	502F 01ECh
1F0h	8	CONTROLSS_CTRL_CMPSSB8_CLK_GATE	RW	502F 01F0h
1F4h	8	CONTROLSS_CTRL_CMPSSB9_CLK_GATE	RW	502F 01F4h
200h	8	CONTROLSS_CTRL_ECAP0_CLK_GATE	RW	502F 0200h
204h	8	CONTROLSS_CTRL_ECAP1_CLK_GATE	RW	502F 0204h
208h	8	CONTROLSS_CTRL_ECAP2_CLK_GATE	RW	502F 0208h
20Ch	8	CONTROLSS_CTRL_ECAP3_CLK_GATE	RW	502F 020Ch
210h	8	CONTROLSS_CTRL_ECAP4_CLK_GATE	RW	502F 0210h
214h	8	CONTROLSS_CTRL_ECAP5_CLK_GATE	RW	502F 0214h
218h	8	CONTROLSS_CTRL_ECAP6_CLK_GATE	RW	502F 0218h
21Ch	8	CONTROLSS_CTRL_ECAP7_CLK_GATE	RW	502F 021Ch
220h	8	CONTROLSS_CTRL_ECAP8_CLK_GATE	RW	502F 0220h
224h	8	CONTROLSS_CTRL_ECAP9_CLK_GATE	RW	502F 0224h
240h	8	CONTROLSS_CTRL_EQEP0_CLK_GATE	RW	502F 0240h
244h	8	CONTROLSS_CTRL_EQEP1_CLK_GATE	RW	502F 0244h
248h	8	CONTROLSS_CTRL_EQEP2_CLK_GATE	RW	502F 0248h
250h	8	CONTROLSS_CTRL_SDFM0_CLK_GATE	RW	502F 0250h
254h	8	CONTROLSS_CTRL_SDFM1_CLK_GATE	RW	502F 0254h
258h	8	CONTROLSS_CTRL_DAC_CLK_GATE	RW	502F 0258h
25Ch	8	CONTROLSS_CTRL_ADC0_CLK_GATE	RW	502F 025Ch
260h	8	CONTROLSS_CTRL_ADC1_CLK_GATE	RW	502F 0260h
264h	8	CONTROLSS_CTRL_ADC2_CLK_GATE	RW	502F 0264h
268h	8	CONTROLSS_CTRL_ADC3_CLK_GATE	RW	502F 0268h
26Ch	8	CONTROLSS_CTRL_ADC4_CLK_GATE	RW	502F 026Ch
270h	8	CONTROLSS_CTRL_OTTO0_CLK_GATE	RW	502F 0270h
274h	8	CONTROLSS_CTRL_OTTO1_CLK_GATE	RW	502F 0274h
278h	8	CONTROLSS_CTRL_OTTO2_CLK_GATE	RW	502F 0278h
27Ch	8	CONTROLSS_CTRL_OTTO3_CLK_GATE	RW	502F 027Ch
280h	8	CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE	RW	502F 0280h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
284h	8	CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE	RW	502F 0284h
288h	8	CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE	RW	502F 0288h
28Ch	8	CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE	RW	502F 028Ch
290h	8	CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE	RW	502F 0290h
294h	8	CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE	RW	502F 0294h
300h	8	CONTROLSS_CTRL_ETPWM0_RST	RW	502F 0300h
304h	8	CONTROLSS_CTRL_ETPWM1_RST	RW	502F 0304h
308h	8	CONTROLSS_CTRL_ETPWM2_RST	RW	502F 0308h
30Ch	8	CONTROLSS_CTRL_ETPWM3_RST	RW	502F 030Ch
310h	8	CONTROLSS_CTRL_ETPWM4_RST	RW	502F 0310h
314h	8	CONTROLSS_CTRL_ETPWM5_RST	RW	502F 0314h
318h	8	CONTROLSS_CTRL_ETPWM6_RST	RW	502F 0318h
31Ch	8	CONTROLSS_CTRL_ETPWM7_RST	RW	502F 031Ch
320h	8	CONTROLSS_CTRL_ETPWM8_RST	RW	502F 0320h
324h	8	CONTROLSS_CTRL_ETPWM9_RST	RW	502F 0324h
328h	8	CONTROLSS_CTRL_ETPWM10_RST	RW	502F 0328h
32Ch	8	CONTROLSS_CTRL_ETPWM11_RST	RW	502F 032Ch
330h	8	CONTROLSS_CTRL_ETPWM12_RST	RW	502F 0330h
334h	8	CONTROLSS_CTRL_ETPWM13_RST	RW	502F 0334h
338h	8	CONTROLSS_CTRL_ETPWM14_RST	RW	502F 0338h
33Ch	8	CONTROLSS_CTRL_ETPWM15_RST	RW	502F 033Ch
340h	8	CONTROLSS_CTRL_ETPWM16_RST	RW	502F 0340h
344h	8	CONTROLSS_CTRL_ETPWM17_RST	RW	502F 0344h
348h	8	CONTROLSS_CTRL_ETPWM18_RST	RW	502F 0348h
34Ch	8	CONTROLSS_CTRL_ETPWM19_RST	RW	502F 034Ch
350h	8	CONTROLSS_CTRL_ETPWM20_RST	RW	502F 0350h
354h	8	CONTROLSS_CTRL_ETPWM21_RST	RW	502F 0354h
358h	8	CONTROLSS_CTRL_ETPWM22_RST	RW	502F 0358h
35Ch	8	CONTROLSS_CTRL_ETPWM23_RST	RW	502F 035Ch
360h	8	CONTROLSS_CTRL_ETPWM24_RST	RW	502F 0360h
364h	8	CONTROLSS_CTRL_ETPWM25_RST	RW	502F 0364h
368h	8	CONTROLSS_CTRL_ETPWM26_RST	RW	502F 0368h
36Ch	8	CONTROLSS_CTRL_ETPWM27_RST	RW	502F 036Ch
370h	8	CONTROLSS_CTRL_ETPWM28_RST	RW	502F 0370h
374h	8	CONTROLSS_CTRL_ETPWM29_RST	RW	502F 0374h
378h	8	CONTROLSS_CTRL_ETPWM30_RST	RW	502F 0378h
37Ch	8	CONTROLSS_CTRL_ETPWM31_RST	RW	502F 037Ch
380h	8	CONTROLSS_CTRL_FSI_TX0_RST	RW	502F 0380h
384h	8	CONTROLSS_CTRL_FSI_TX1_RST	RW	502F 0384h
388h	8	CONTROLSS_CTRL_FSI_TX2_RST	RW	502F 0388h
38Ch	8	CONTROLSS_CTRL_FSI_TX3_RST	RW	502F 038Ch
390h	8	CONTROLSS_CTRL_FSI_RX0_RST	RW	502F 0390h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
394h	8	CONTROLSS_CTRL_FSI_RX1_RST	RW	502F 0394h
398h	8	CONTROLSS_CTRL_FSI_RX2_RST	RW	502F 0398h
39Ch	8	CONTROLSS_CTRL_FSI_RX3_RST	RW	502F 039Ch
3A0h	8	CONTROLSS_CTRL_CMPSSA0_RST	RW	502F 03A0h
3A4h	8	CONTROLSS_CTRL_CMPSSA1_RST	RW	502F 03A4h
3A8h	8	CONTROLSS_CTRL_CMPSSA2_RST	RW	502F 03A8h
3ACh	8	CONTROLSS_CTRL_CMPSSA3_RST	RW	502F 03ACh
3B0h	8	CONTROLSS_CTRL_CMPSSA4_RST	RW	502F 03B0h
3B4h	8	CONTROLSS_CTRL_CMPSSA5_RST	RW	502F 03B4h
3B8h	8	CONTROLSS_CTRL_CMPSSA6_RST	RW	502F 03B8h
3BCh	8	CONTROLSS_CTRL_CMPSSA7_RST	RW	502F 03BCh
3C0h	8	CONTROLSS_CTRL_CMPSSA8_RST	RW	502F 03C0h
3C4h	8	CONTROLSS_CTRL_CMPSSA9_RST	RW	502F 03C4h
3D0h	8	CONTROLSS_CTRL_CMPSSB0_RST	RW	502F 03D0h
3D4h	8	CONTROLSS_CTRL_CMPSSB1_RST	RW	502F 03D4h
3D8h	8	CONTROLSS_CTRL_CMPSSB2_RST	RW	502F 03D8h
3DCh	8	CONTROLSS_CTRL_CMPSSB3_RST	RW	502F 03DCh
3E0h	8	CONTROLSS_CTRL_CMPSSB4_RST	RW	502F 03E0h
3E4h	8	CONTROLSS_CTRL_CMPSSB5_RST	RW	502F 03E4h
3E8h	8	CONTROLSS_CTRL_CMPSSB6_RST	RW	502F 03E8h
3ECh	8	CONTROLSS_CTRL_CMPSSB7_RST	RW	502F 03ECh
3F0h	8	CONTROLSS_CTRL_CMPSSB8_RST	RW	502F 03F0h
3F4h	8	CONTROLSS_CTRL_CMPSSB9_RST	RW	502F 03F4h
400h	8	CONTROLSS_CTRL_ECAP0_RST	RW	502F 0400h
404h	8	CONTROLSS_CTRL_ECAP1_RST	RW	502F 0404h
408h	8	CONTROLSS_CTRL_ECAP2_RST	RW	502F 0408h
40Ch	8	CONTROLSS_CTRL_ECAP3_RST	RW	502F 040Ch
410h	8	CONTROLSS_CTRL_ECAP4_RST	RW	502F 0410h
414h	8	CONTROLSS_CTRL_ECAP5_RST	RW	502F 0414h
418h	8	CONTROLSS_CTRL_ECAP6_RST	RW	502F 0418h
41Ch	8	CONTROLSS_CTRL_ECAP7_RST	RW	502F 041Ch
420h	8	CONTROLSS_CTRL_ECAP8_RST	RW	502F 0420h
424h	8	CONTROLSS_CTRL_ECAP9_RST	RW	502F 0424h
440h	8	CONTROLSS_CTRL_EQEP0_RST	RW	502F 0440h
444h	8	CONTROLSS_CTRL_EQEP1_RST	RW	502F 0444h
448h	8	CONTROLSS_CTRL_EQEP2_RST	RW	502F 0448h
450h	8	CONTROLSS_CTRL_SDFM0_RST	RW	502F 0450h
454h	8	CONTROLSS_CTRL_SDFM1_RST	RW	502F 0454h
458h	8	CONTROLSS_CTRL_DAC_RST	RW	502F 0458h
45Ch	8	CONTROLSS_CTRL_ADC0_RST	RW	502F 045Ch
460h	8	CONTROLSS_CTRL_ADC1_RST	RW	502F 0460h
464h	8	CONTROLSS_CTRL_ADC2_RST	RW	502F 0464h
468h	8	CONTROLSS_CTRL_ADC3_RST	RW	502F 0468h
46Ch	8	CONTROLSS_CTRL_ADC4_RST	RW	502F 046Ch
470h	8	CONTROLSS_CTRL_OTTO0_RST	RW	502F 0470h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
474h	8	CONTROLSS_CTRL_OTTO1_RST	RW	502F 0474h
478h	8	CONTROLSS_CTRL_OTTO2_RST	RW	502F 0478h
47Ch	8	CONTROLSS_CTRL_OTTO3_RST	RW	502F 047Ch
500h	8	CONTROLSS_CTRL_EPWM0_HALTEN	RW	502F 0500h
504h	8	CONTROLSS_CTRL_EPWM1_HALTEN	RW	502F 0504h
508h	8	CONTROLSS_CTRL_EPWM2_HALTEN	RW	502F 0508h
50Ch	8	CONTROLSS_CTRL_EPWM3_HALTEN	RW	502F 050Ch
510h	8	CONTROLSS_CTRL_EPWM4_HALTEN	RW	502F 0510h
514h	8	CONTROLSS_CTRL_EPWM5_HALTEN	RW	502F 0514h
518h	8	CONTROLSS_CTRL_EPWM6_HALTEN	RW	502F 0518h
51Ch	8	CONTROLSS_CTRL_EPWM7_HALTEN	RW	502F 051Ch
520h	8	CONTROLSS_CTRL_EPWM8_HALTEN	RW	502F 0520h
524h	8	CONTROLSS_CTRL_EPWM9_HALTEN	RW	502F 0524h
528h	8	CONTROLSS_CTRL_EPWM10_HALTEN	RW	502F 0528h
52Ch	8	CONTROLSS_CTRL_EPWM11_HALTEN	RW	502F 052Ch
530h	8	CONTROLSS_CTRL_EPWM12_HALTEN	RW	502F 0530h
534h	8	CONTROLSS_CTRL_EPWM13_HALTEN	RW	502F 0534h
538h	8	CONTROLSS_CTRL_EPWM14_HALTEN	RW	502F 0538h
53Ch	8	CONTROLSS_CTRL_EPWM15_HALTEN	RW	502F 053Ch
540h	8	CONTROLSS_CTRL_EPWM16_HALTEN	RW	502F 0540h
544h	8	CONTROLSS_CTRL_EPWM17_HALTEN	RW	502F 0544h
548h	8	CONTROLSS_CTRL_EPWM18_HALTEN	RW	502F 0548h
54Ch	8	CONTROLSS_CTRL_EPWM19_HALTEN	RW	502F 054Ch
550h	8	CONTROLSS_CTRL_EPWM20_HALTEN	RW	502F 0550h
554h	8	CONTROLSS_CTRL_EPWM21_HALTEN	RW	502F 0554h
558h	8	CONTROLSS_CTRL_EPWM22_HALTEN	RW	502F 0558h
55Ch	8	CONTROLSS_CTRL_EPWM23_HALTEN	RW	502F 055Ch
560h	8	CONTROLSS_CTRL_EPWM24_HALTEN	RW	502F 0560h
564h	8	CONTROLSS_CTRL_EPWM25_HALTEN	RW	502F 0564h
568h	8	CONTROLSS_CTRL_EPWM26_HALTEN	RW	502F 0568h
56Ch	8	CONTROLSS_CTRL_EPWM27_HALTEN	RW	502F 056Ch
570h	8	CONTROLSS_CTRL_EPWM28_HALTEN	RW	502F 0570h
574h	8	CONTROLSS_CTRL_EPWM29_HALTEN	RW	502F 0574h
578h	8	CONTROLSS_CTRL_EPWM30_HALTEN	RW	502F 0578h
57Ch	8	CONTROLSS_CTRL_EPWM31_HALTEN	RW	502F 057Ch
580h	8	CONTROLSS_CTRL_CMPSSA0_HALTEN	RW	502F 0580h
584h	8	CONTROLSS_CTRL_CMPSSA1_HALTEN	RW	502F 0584h
588h	8	CONTROLSS_CTRL_CMPSSA2_HALTEN	RW	502F 0588h
58Ch	8	CONTROLSS_CTRL_CMPSSA3_HALTEN	RW	502F 058Ch
590h	8	CONTROLSS_CTRL_CMPSSA4_HALTEN	RW	502F 0590h
594h	8	CONTROLSS_CTRL_CMPSSA5_HALTEN	RW	502F 0594h
598h	8	CONTROLSS_CTRL_CMPSSA6_HALTEN	RW	502F 0598h
59Ch	8	CONTROLSS_CTRL_CMPSSA7_HALTEN	RW	502F 059Ch
5A0h	8	CONTROLSS_CTRL_CMPSSA8_HALTEN	RW	502F 05A0h
5A4h	8	CONTROLSS_CTRL_CMPSSA9_HALTEN	RW	502F 05A4h

Table 2-1101. CONTROLSS_CTRL, CONTROLSS_CTRL_CONTROLSS_CTRL Registers, Base Address=502F 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CTRL Physical Address
5A8h	8	CONTROLSS_CTRL_CMPSSB0_HALTEN	RW	502F 05A8h
5ACh	8	CONTROLSS_CTRL_CMPSSB1_HALTEN	RW	502F 05ACh
5B0h	8	CONTROLSS_CTRL_CMPSSB2_HALTEN	RW	502F 05B0h
5B4h	8	CONTROLSS_CTRL_CMPSSB3_HALTEN	RW	502F 05B4h
5B8h	8	CONTROLSS_CTRL_CMPSSB4_HALTEN	RW	502F 05B8h
5BCh	8	CONTROLSS_CTRL_CMPSSB5_HALTEN	RW	502F 05BCh
5C0h	8	CONTROLSS_CTRL_CMPSSB6_HALTEN	RW	502F 05C0h
5C4h	8	CONTROLSS_CTRL_CMPSSB7_HALTEN	RW	502F 05C4h
5C8h	8	CONTROLSS_CTRL_CMPSSB8_HALTEN	RW	502F 05C8h
5CCh	8	CONTROLSS_CTRL_CMPSSB9_HALTEN	RW	502F 05CCh
5D0h	8	CONTROLSS_CTRL_ECAP0_HALTEN	RW	502F 05D0h
5D4h	8	CONTROLSS_CTRL_ECAP1_HALTEN	RW	502F 05D4h
5D8h	8	CONTROLSS_CTRL_ECAP2_HALTEN	RW	502F 05D8h
5DCh	8	CONTROLSS_CTRL_ECAP3_HALTEN	RW	502F 05DCh
5E0h	8	CONTROLSS_CTRL_ECAP4_HALTEN	RW	502F 05E0h
5E4h	8	CONTROLSS_CTRL_ECAP5_HALTEN	RW	502F 05E4h
5E8h	8	CONTROLSS_CTRL_ECAP6_HALTEN	RW	502F 05E8h
5ECh	8	CONTROLSS_CTRL_ECAP7_HALTEN	RW	502F 05ECh
5F0h	8	CONTROLSS_CTRL_ECAP8_HALTEN	RW	502F 05F0h
5F4h	8	CONTROLSS_CTRL_ECAP9_HALTEN	RW	502F 05F4h
5F8h	8	CONTROLSS_CTRL_EQEP0_HALTEN	RW	502F 05F8h
5FCh	8	CONTROLSS_CTRL_EQEP1_HALTEN	RW	502F 05FCh
600h	8	CONTROLSS_CTRL_EQEP2_HALTEN	RW	502F 0600h
1008h	32	CONTROLSS_CTRL_LOCK0_KICK0	- KICK0 component	502F 1008h
100Ch	32	CONTROLSS_CTRL_LOCK0_KICK1	- KICK1 component	502F 100Ch
1010h	8	CONTROLSS_CTRL_INTR_RAW_STATUS	Interrupt Raw Status/Set Register	502F 1010h
1014h	8	CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR	Interrupt Enabled Status/Clear register	502F 1014h
1018h	8	CONTROLSS_CTRL_INTR_ENABLE	Interrupt Enable register	502F 1018h
101Ch	8	CONTROLSS_CTRL_INTR_ENABLE_CLEAR	Interrupt Enable Clear register	502F 101Ch
1020h	8	CONTROLSS_CTRL_EOI	EOI register	502F 1020h
1024h	32	CONTROLSS_CTRL_FAULT_ADDRESS	Fault Address register	502F 1024h
1028h	8	CONTROLSS_CTRL_FAULT_TYPE_STATUS	Fault Type Status register	502F 1028h
102Ch	32	CONTROLSS_CTRL_FAULT_ATTR_STATUS	Fault Attribute Status register	502F 102Ch
1030h	0	CONTROLSS_CTRL_FAULT_CLEAR	Fault Clear register	502F 1030h

2.6.1 CONTROLSS_CTRL_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 2-1102. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0000h

Figure 2-548. CONTROLSS_CTRL_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 2-1103. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

2.6.2 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Register (Offset = 4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1104. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0004h

Figure 2-549. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETPWM15		ETPWM14		ETPWM13		ETPWM12		ETPWM11		ETPWM10		ETPWM9		ETPWM8	
RW		RW		RW		RW		RW		RW		RW		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETPWM7		ETPWM6		ETPWM5		ETPWM4		ETPWM3		ETPWM2		ETPWM1		ETPWM0	
RW		RW		RW		RW		RW		RW		RW		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 2-1105. EPWM_STATICXBAR_SEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	ETPWM15	RW	0h	ETPWM15 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
29 - 28	ETPWM14	RW	0h	ETPWM14 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
27 - 26	ETPWM13	RW	0h	ETPWM13 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
25 - 24	ETPWM12	RW	0h	ETPWM12 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
23 - 22	ETPWM11	RW	0h	ETPWM11 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
21 - 20	ETPWM10	RW	0h	ETPWM10 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
19 - 18	ETPWM9	RW	0h	ETPWM9 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
17 - 16	ETPWM8	RW	0h	ETPWM8 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
15 - 14	ETPWM7	RW	0h	ETPWM7 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
13 - 12	ETPWM6	RW	0h	ETPWM6 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
11 - 10	ETPWM5	RW	0h	ETPWM5 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
9 - 8	ETPWM4	RW	0h	ETPWM4 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
7 - 6	ETPWM3	RW	0h	ETPWM3 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
5 - 4	ETPWM2	RW	0h	ETPWM2 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
3 - 2	ETPWM1	RW	0h	ETPWM1 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

Table 2-1105. EPWM_STATICXBAR_SEL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1 - 0	ETPWM0	RW	0h	ETPWM0 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

2.6.3 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Register (Offset = 8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1106. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0008h

Figure 2-550. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETPWM31		ETPWM30		ETPWM29		ETPWM28		ETPWM27		ETPWM26		ETPWM25		ETPWM24	
RW		RW		RW		RW		RW		RW		RW		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETPWM23		ETPWM22		ETPWM21		ETPWM20		ETPWM19		ETPWM18		ETPWM17		ETPWM16	
RW		RW		RW		RW		RW		RW		RW		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 2-1107. EPWM_STATICXBAR_SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	ETPWM31	RW	0h	ETPWM31 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
29 - 28	ETPWM30	RW	0h	ETPWM30 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
27 - 26	ETPWM29	RW	0h	ETPWM29 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
25 - 24	ETPWM28	RW	0h	ETPWM28 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
23 - 22	ETPWM27	RW	0h	ETPWM27 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
21 - 20	ETPWM26	RW	0h	ETPWM26 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
19 - 18	ETPWM25	RW	0h	ETPWM25 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
17 - 16	ETPWM24	RW	0h	ETPWM24 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
15 - 14	ETPWM23	RW	0h	ETPWM23 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
13 - 12	ETPWM22	RW	0h	ETPWM22 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
11 - 10	ETPWM21	RW	0h	ETPWM21 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
9 - 8	ETPWM20	RW	0h	ETPWM20 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
7 - 6	ETPWM19	RW	0h	ETPWM19 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
5 - 4	ETPWM18	RW	0h	ETPWM18 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
3 - 2	ETPWM17	RW	0h	ETPWM17 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

Table 2-1107. EPWM_STATICXBAR_SEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1 - 0	ETPWM16	RW	0h	ETPWM16 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

2.6.4 CONTROLSS_CTRL_EPWM_CLKSYNC Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1108. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0010h

Figure 2-551. CONTROLSS_CTRL_EPWM_CLKSYNC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT															
RW															
0															

Access Types Legend

Table 2-1109. EPWM_CLKSYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	BIT	RW	0h	ETPWM clock sync for each EPWM instance1: will allow CLK SYNC when GBCLKSYNC is written in0: No CLK SYNC when GBCLKSYNC is written in

2.6.5 CONTROLSS_CTRL_SDFM1_CLK0_SEL Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1110. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0018h

Figure 2-552. CONTROLSS_CTRL_SDFM1_CLK0_SEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 2-1111. SDFM1_CLK0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SEL	RW	0h	SDFM1 clock CK0 select0: source is SDFM1 CK0 from Pinmux1: source is SDFM0 CK0 from Pinmux

2.6.6 CONTROLSS_CTRL_EMUSTOPN_MASK Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1112. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0020h

Figure 2-553. CONTROLSS_CTRL_EMUSTOPN_MASK Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1113. EMUSTOPN_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5B1 enabled to control EMUSTOPn1: CR5B1 disabled to control EMUSTOPn
2	CR5A1	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5A1 enabled to control EMUSTOPn1: CR5A1 disabled to control EMUSTOPn
1	CR5B0	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5B0 enabled to control EMUSTOPn1: CR5B0 disabled to control EMUSTOPn
0	CR5A0	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5A0 enabled to control EMUSTOPn1: CR5A0 disabled to control EMUSTOPn

2.6.7 CONTROLSS_CTRL_CLB_AQ_EN0 Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1114. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0028h

Figure 2-554. CONTROLSS_CTRL_CLB_AQ_EN0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE															
RW															
0															

Access Types Legend

Table 2-1115. CLB_AQ_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_AQ signal of PWM[15:0]

2.6.8 CONTROLSS_CTRL_CLB_AQ_EN1 Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1116. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0030h

Figure 2-555. CONTROLSS_CTRL_CLB_AQ_EN1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE															
RW															
0															

Access Types Legend

Table 2-1117. CLB_AQ_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_AQ signal of PWM[31:16]

2.6.9 CONTROLSS_CTRL_CLB_DB_EN0 Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1118. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0038h

Figure 2-556. CONTROLSS_CTRL_CLB_DB_EN0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE															
RW															
0															

Access Types Legend

Table 2-1119. CLB_DB_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_DB signal of PWM[15:0]

2.6.10 CONTROLSS_CTRL_CLB_DB_EN1 Register (Offset = 40h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1120. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0040h

Figure 2-557. CONTROLSS_CTRL_CLB_DB_EN1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE															
RW															
0															

Access Types Legend

Table 2-1121. CLB_DB_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_DB signal of PWM[31:16]

2.6.11 CONTROLSS_CTRL_ETPWM0_CLK_GATE Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1122. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0100h

Figure 2-558. CONTROLSS_CTRL_ETPWM0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1123. ETPWM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.12 CONTROLSS_CTRL_ETPWM1_CLK_GATE Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1124. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0104h

Figure 2-559. CONTROLSS_CTRL_ETPWM1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1125. ETPWM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.13 CONTROLSS_CTRL_ETPWM2_CLK_GATE Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1126. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0108h

Figure 2-560. CONTROLSS_CTRL_ETPWM2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1127. ETPWM2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.14 CONTROLSS_CTRL_ETPWM3_CLK_GATE Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1128. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 010Ch

Figure 2-561. CONTROLSS_CTRL_ETPWM3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1129. ETPWM3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.15 CONTROLSS_CTRL_ETPWM4_CLK_GATE Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1130. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0110h

Figure 2-562. CONTROLSS_CTRL_ETPWM4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1131. ETPWM4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.16 CONTROLSS_CTRL_ETPWM5_CLK_GATE Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1132. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0114h

Figure 2-563. CONTROLSS_CTRL_ETPWM5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1133. ETPWM5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.17 CONTROLSS_CTRL_ETPWM6_CLK_GATE Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1134. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0118h

Figure 2-564. CONTROLSS_CTRL_ETPWM6_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1135. ETPWM6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.18 CONTROLSS_CTRL_ETPWM7_CLK_GATE Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1136. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 011Ch

Figure 2-565. CONTROLSS_CTRL_ETPWM7_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1137. ETPWM7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.19 CONTROLSS_CTRL_ETPWM8_CLK_GATE Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1138. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0120h

Figure 2-566. CONTROLSS_CTRL_ETPWM8_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1139. ETPWM8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.20 CONTROLSS_CTRL_ETPWM9_CLK_GATE Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1140. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0124h

Figure 2-567. CONTROLSS_CTRL_ETPWM9_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1141. ETPWM9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.21 CONTROLSS_CTRL_ETPWM10_CLK_GATE Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1142. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0128h

Figure 2-568. CONTROLSS_CTRL_ETPWM10_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1143. ETPWM10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.22 CONTROLSS_CTRL_ETPWM11_CLK_GATE Register (Offset = 12Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1144. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 012Ch

Figure 2-569. CONTROLSS_CTRL_ETPWM11_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1145. ETPWM11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.23 CONTROLSS_CTRL_ETPWM12_CLK_GATE Register (Offset = 130h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1146. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0130h

Figure 2-570. CONTROLSS_CTRL_ETPWM12_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1147. ETPWM12_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.24 CONTROLSS_CTRL_ETPWM13_CLK_GATE Register (Offset = 134h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1148. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0134h

Figure 2-571. CONTROLSS_CTRL_ETPWM13_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1149. ETPWM13_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.25 CONTROLSS_CTRL_ETPWM14_CLK_GATE Register (Offset = 138h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1150. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0138h

Figure 2-572. CONTROLSS_CTRL_ETPWM14_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1151. ETPWM14_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.26 CONTROLSS_CTRL_ETPWM15_CLK_GATE Register (Offset = 13Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1152. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 013Ch

Figure 2-573. CONTROLSS_CTRL_ETPWM15_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1153. ETPWM15_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.27 CONTROLSS_CTRL_ETPWM16_CLK_GATE Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1154. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0140h

Figure 2-574. CONTROLSS_CTRL_ETPWM16_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1155. ETPWM16_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.28 CONTROLSS_CTRL_ETPWM17_CLK_GATE Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1156. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0144h

Figure 2-575. CONTROLSS_CTRL_ETPWM17_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1157. ETPWM17_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.29 CONTROLSS_CTRL_ETPWM18_CLK_GATE Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1158. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0148h

Figure 2-576. CONTROLSS_CTRL_ETPWM18_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1159. ETPWM18_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.30 CONTROLSS_CTRL_ETPWM19_CLK_GATE Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1160. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 014Ch

Figure 2-577. CONTROLSS_CTRL_ETPWM19_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1161. ETPWM19_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.31 CONTROLSS_CTRL_ETPWM20_CLK_GATE Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1162. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0150h

Figure 2-578. CONTROLSS_CTRL_ETPWM20_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1163. ETPWM20_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.32 CONTROLSS_CTRL_ETPWM21_CLK_GATE Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1164. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0154h

Figure 2-579. CONTROLSS_CTRL_ETPWM21_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1165. ETPWM21_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.33 CONTROLSS_CTRL_ETPWM22_CLK_GATE Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1166. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0158h

Figure 2-580. CONTROLSS_CTRL_ETPWM22_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1167. ETPWM22_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.34 CONTROLSS_CTRL_ETPWM23_CLK_GATE Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1168. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 015Ch

Figure 2-581. CONTROLSS_CTRL_ETPWM23_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1169. ETPWM23_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.35 CONTROLSS_CTRL_ETPWM24_CLK_GATE Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1170. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0160h

Figure 2-582. CONTROLSS_CTRL_ETPWM24_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1171. ETPWM24_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.36 CONTROLSS_CTRL_ETPWM25_CLK_GATE Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1172. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0164h

Figure 2-583. CONTROLSS_CTRL_ETPWM25_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1173. ETPWM25_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.37 CONTROLSS_CTRL_ETPWM26_CLK_GATE Register (Offset = 168h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1174. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0168h

Figure 2-584. CONTROLSS_CTRL_ETPWM26_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1175. ETPWM26_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.38 CONTROLSS_CTRL_ETPWM27_CLK_GATE Register (Offset = 16Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1176. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 016Ch

Figure 2-585. CONTROLSS_CTRL_ETPWM27_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1177. ETPWM27_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.39 CONTROLSS_CTRL_ETPWM28_CLK_GATE Register (Offset = 170h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1178. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0170h

Figure 2-586. CONTROLSS_CTRL_ETPWM28_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1179. ETPWM28_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.40 CONTROLSS_CTRL_ETPWM29_CLK_GATE Register (Offset = 174h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1180. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0174h

Figure 2-587. CONTROLSS_CTRL_ETPWM29_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1181. ETPWM29_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.41 CONTROLSS_CTRL_ETPWM30_CLK_GATE Register (Offset = 178h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1182. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0178h

Figure 2-588. CONTROLSS_CTRL_ETPWM30_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1183. ETPWM30_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.42 CONTROLSS_CTRL_ETPWM31_CLK_GATE Register (Offset = 17Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1184. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 017Ch

Figure 2-589. CONTROLSS_CTRL_ETPWM31_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1185. ETPWM31_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

2.6.43 CONTROLSS_CTRL_FSI_TX0_CLK_GATE Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1186. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0180h

Figure 2-590. CONTROLSS_CTRL_FSI_TX0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1187. FSI_TX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

2.6.44 CONTROLSS_CTRL_FSI_TX1_CLK_GATE Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1188. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0184h

Figure 2-591. CONTROLSS_CTRL_FSI_TX1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1189. FSI_TX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

2.6.45 CONTROLSS_CTRL_FSI_TX2_CLK_GATE Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1190. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0188h

Figure 2-592. CONTROLSS_CTRL_FSI_TX2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1191. FSI_TX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

2.6.46 CONTROLSS_CTRL_FSI_TX3_CLK_GATE Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1192. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 018Ch

Figure 2-593. CONTROLSS_CTRL_FSI_TX3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1193. FSI_TX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

2.6.47 CONTROLSS_CTRL_FSI_RX0_CLK_GATE Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1194. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0190h

Figure 2-594. CONTROLSS_CTRL_FSI_RX0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1195. FSI_RX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

2.6.48 CONTROLSS_CTRL_FSI_RX1_CLK_GATE Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1196. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0194h

Figure 2-595. CONTROLSS_CTRL_FSI_RX1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1197. FSI_RX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

2.6.49 CONTROLSS_CTRL_FSI_RX2_CLK_GATE Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1198. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0198h

Figure 2-596. CONTROLSS_CTRL_FSI_RX2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1199. FSI_RX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

2.6.50 CONTROLSS_CTRL_FSI_RX3_CLK_GATE Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-1200. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 019Ch

Figure 2-597. CONTROLSS_CTRL_FSI_RX3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1201. FSI_RX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

2.6.51 CONTROLSS_CTRL_CMPSSA0_CLK_GATE Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1202. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A0h

Figure 2-598. CONTROLSS_CTRL_CMPSSA0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1203. CMPSSA0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.52 CONTROLSS_CTRL_CMPSSA1_CLK_GATE Register (Offset = 1A4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1204. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A4h

Figure 2-599. CONTROLSS_CTRL_CMPSSA1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1205. CMPSSA1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.53 CONTROLSS_CTRL_CMPSSA2_CLK_GATE Register (Offset = 1A8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1206. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A8h

Figure 2-600. CONTROLSS_CTRL_CMPSSA2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1207. CMPSSA2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.54 CONTROLSS_CTRL_CMPSSA3_CLK_GATE Register (Offset = 1ACh) [reset = h]

Short Description: RW

Long Description:

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Table 2-1208. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01ACh

Figure 2-601. CONTROLSS_CTRL_CMPSSA3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1209. CMPSSA3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.55 CONTROLSS_CTRL_CMPSSA4_CLK_GATE Register (Offset = 1B0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1210. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B0h

Figure 2-602. CONTROLSS_CTRL_CMPSSA4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1211. CMPSSA4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.56 CONTROLSS_CTRL_CMPSSA5_CLK_GATE Register (Offset = 1B4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1212. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B4h

Figure 2-603. CONTROLSS_CTRL_CMPSSA5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1213. CMPSSA5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.57 CONTROLSS_CTRL_CMPSSA6_CLK_GATE Register (Offset = 1B8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1214. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B8h

Figure 2-604. CONTROLSS_CTRL_CMPSSA6_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1215. CMPSSA6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.58 CONTROLSS_CTRL_CMPSSA7_CLK_GATE Register (Offset = 1BCh) [reset = h]

Short Description: RW

Long Description:

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Table 2-1216. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01BCh

Figure 2-605. CONTROLSS_CTRL_CMPSSA7_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1217. CMPSSA7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.59 CONTROLSS_CTRL_CMPSSA8_CLK_GATE Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1218. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01C0h

Figure 2-606. CONTROLSS_CTRL_CMPSSA8_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1219. CMPSSA8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.60 CONTROLSS_CTRL_CMPSSA9_CLK_GATE Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1220. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01C4h

Figure 2-607. CONTROLSS_CTRL_CMPSSA9_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1221. CMPSSA9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

2.6.61 CONTROLSS_CTRL_CMPSSB0_CLK_GATE Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1222. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D0h

Figure 2-608. CONTROLSS_CTRL_CMPSSB0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1223. CMPSSB0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.62 CONTROLSS_CTRL_CMPSSB1_CLK_GATE Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1224. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D4h

Figure 2-609. CONTROLSS_CTRL_CMPSSB1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1225. CMPSSB1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.63 CONTROLSS_CTRL_CMPSSB2_CLK_GATE Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1226. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D8h

Figure 2-610. CONTROLSS_CTRL_CMPSSB2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1227. CMPSSB2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.64 CONTROLSS_CTRL_CMPSSB3_CLK_GATE Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1228. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01DCh

Figure 2-611. CONTROLSS_CTRL_CMPSSB3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1229. CMPSSB3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.65 CONTROLSS_CTRL_CMPSSB4_CLK_GATE Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1230. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E0h

Figure 2-612. CONTROLSS_CTRL_CMPSSB4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1231. CMPSSB4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.66 CONTROLSS_CTRL_CMPSSB5_CLK_GATE Register (Offset = 1E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1232. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E4h

Figure 2-613. CONTROLSS_CTRL_CMPSSB5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1233. CMPSSB5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.67 CONTROLSS_CTRL_CMPSSB6_CLK_GATE Register (Offset = 1E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1234. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E8h

Figure 2-614. CONTROLSS_CTRL_CMPSSB6_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1235. CMPSSB6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.68 CONTROLSS_CTRL_CMPSSB7_CLK_GATE Register (Offset = 1ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1236. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01ECh

Figure 2-615. CONTROLSS_CTRL_CMPSSB7_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1237. CMPSSB7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.69 CONTROLSS_CTRL_CMPSSB8_CLK_GATE Register (Offset = 1F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1238. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01F0h

Figure 2-616. CONTROLSS_CTRL_CMPSSB8_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1239. CMPSSB8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.70 CONTROLSS_CTRL_CMPSSB9_CLK_GATE Register (Offset = 1F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1240. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01F4h

Figure 2-617. CONTROLSS_CTRL_CMPSSB9_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1241. CMPSSB9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

2.6.71 CONTROLSS_CTRL_ECAP0_CLK_GATE Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1242. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0200h

Figure 2-618. CONTROLSS_CTRL_ECAP0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1243. ECAP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.72 CONTROLSS_CTRL_ECAP1_CLK_GATE Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1244. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0204h

Figure 2-619. CONTROLSS_CTRL_ECAP1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1245. ECAP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.73 CONTROLSS_CTRL_ECAP2_CLK_GATE Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1246. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0208h

Figure 2-620. CONTROLSS_CTRL_ECAP2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1247. ECAP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.74 CONTROLSS_CTRL_ECAP3_CLK_GATE Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1248. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 020Ch

Figure 2-621. CONTROLSS_CTRL_ECAP3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1249. ECAP3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.75 CONTROLSS_CTRL_ECAP4_CLK_GATE Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1250. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0210h

Figure 2-622. CONTROLSS_CTRL_ECAP4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1251. ECAP4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.76 CONTROLSS_CTRL_ECAP5_CLK_GATE Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1252. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0214h

Figure 2-623. CONTROLSS_CTRL_ECAP5_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1253. ECAP5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.77 CONTROLSS_CTRL_ECAP6_CLK_GATE Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1254. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0218h

Figure 2-624. CONTROLSS_CTRL_ECAP6_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1255. ECAP6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.78 CONTROLSS_CTRL_ECAP7_CLK_GATE Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1256. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 021Ch

Figure 2-625. CONTROLSS_CTRL_ECAP7_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1257. ECAP7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.79 CONTROLSS_CTRL_ECAP8_CLK_GATE Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1258. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0220h

Figure 2-626. CONTROLSS_CTRL_ECAP8_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1259. ECAP8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.80 CONTROLSS_CTRL_ECAP9_CLK_GATE Register (Offset = 224h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1260. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0224h

Figure 2-627. CONTROLSS_CTRL_ECAP9_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1261. ECAP9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

2.6.81 CONTROLSS_CTRL_EQEP0_CLK_GATE Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1262. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0240h

Figure 2-628. CONTROLSS_CTRL_EQEP0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1263. EQEP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

2.6.82 CONTROLSS_CTRL_EQEP1_CLK_GATE Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1264. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0244h

Figure 2-629. CONTROLSS_CTRL_EQEP1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1265. EQEP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

2.6.83 CONTROLSS_CTRL_EQEP2_CLK_GATE Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1266. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0248h

Figure 2-630. CONTROLSS_CTRL_EQEP2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1267. EQEP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

2.6.84 CONTROLSS_CTRL_SDFM0_CLK_GATE Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1268. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0250h

Figure 2-631. CONTROLSS_CTRL_SDFM0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1269. SDFM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm

2.6.85 CONTROLSS_CTRL_SDFM1_CLK_GATE Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1270. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0254h

Figure 2-632. CONTROLSS_CTRL_SDFM1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1271. SDFM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm

2.6.86 CONTROLSS_CTRL_DAC_CLK_GATE Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1272. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0258h

Figure 2-633. CONTROLSS_CTRL_DAC_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1273. DAC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for dac

2.6.87 CONTROLSS_CTRL_ADC0_CLK_GATE Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1274. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 025Ch

Figure 2-634. CONTROLSS_CTRL_ADC0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1275. ADC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

2.6.88 CONTROLSS_CTRL_ADC1_CLK_GATE Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1276. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0260h

Figure 2-635. CONTROLSS_CTRL_ADC1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1277. ADC1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

2.6.89 CONTROLSS_CTRL_ADC2_CLK_GATE Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1278. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0264h

Figure 2-636. CONTROLSS_CTRL_ADC2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1279. ADC2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

2.6.90 CONTROLSS_CTRL_ADC3_CLK_GATE Register (Offset = 268h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1280. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0268h

Figure 2-637. CONTROLSS_CTRL_ADC3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1281. ADC3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

2.6.91 CONTROLSS_CTRL_ADC4_CLK_GATE Register (Offset = 26Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1282. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 026Ch

Figure 2-638. CONTROLSS_CTRL_ADC4_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1283. ADC4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

2.6.92 CONTROLSS_CTRL_OTTO0_CLK_GATE Register (Offset = 270h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1284. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0270h

Figure 2-639. CONTROLSS_CTRL_OTTO0_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1285. OTTO0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

2.6.93 CONTROLSS_CTRL_OTTO1_CLK_GATE Register (Offset = 274h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1286. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0274h

Figure 2-640. CONTROLSS_CTRL_OTTO1_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1287. OTTO1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

2.6.94 CONTROLSS_CTRL_OTTO2_CLK_GATE Register (Offset = 278h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1288. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0278h

Figure 2-641. CONTROLSS_CTRL_OTTO2_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1289. OTTO2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

2.6.95 CONTROLSS_CTRL_OTTO3_CLK_GATE Register (Offset = 27Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1290. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 027Ch

Figure 2-642. CONTROLSS_CTRL_OTTO3_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1291. OTTO3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

2.6.96 CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1292. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0280h

Figure 2-643. CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1293. SDFM0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm pll clock

2.6.97 CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1294. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0284h

Figure 2-644. CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1295. SDFM1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm pll clock

2.6.98 CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1296. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0288h

Figure 2-645. CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1297. FSI_TX0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

2.6.99 CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1298. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 028Ch

Figure 2-646. CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1299. FSI_TX1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

2.6.100 CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1300. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0290h

Figure 2-647. CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						CLK_GATE	
NONE						RW	
0						0	

Access Types Legend

Table 2-1301. FSI_TX2_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

2.6.101 CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1302. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0294h

Figure 2-648. CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					CLK_GATE		
NONE					RW		
0					0		

Access Types Legend

Table 2-1303. FSI_TX3_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

2.6.102 CONTROLSS_CTRL_ETPWM0_RST Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1304. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0300h

Figure 2-649. CONTROLSS_CTRL_ETPWM0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1305. ETPWM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.103 CONTROLSS_CTRL_ETPWM1_RST Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1306. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0304h

Figure 2-650. CONTROLSS_CTRL_ETPWM1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1307. ETPWM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.104 CONTROLSS_CTRL_ETPWM2_RST Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1308. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0308h

Figure 2-651. CONTROLSS_CTRL_ETPWM2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1309. ETPWM2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.105 CONTROLSS_CTRL_ETPWM3_RST Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1310. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 030Ch

Figure 2-652. CONTROLSS_CTRL_ETPWM3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1311. ETPWM3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.106 CONTROLSS_CTRL_ETPWM4_RST Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1312. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0310h

Figure 2-653. CONTROLSS_CTRL_ETPWM4_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1313. ETPWM4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.107 CONTROLSS_CTRL_ETPWM5_RST Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1314. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0314h

Figure 2-654. CONTROLSS_CTRL_ETPWM5_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1315. ETPWM5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.108 CONTROLSS_CTRL_ETPWM6_RST Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1316. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0318h

Figure 2-655. CONTROLSS_CTRL_ETPWM6_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1317. ETPWM6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.109 CONTROLSS_CTRL_ETPWM7_RST Register (Offset = 31Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1318. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 031Ch

Figure 2-656. CONTROLSS_CTRL_ETPWM7_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1319. ETPWM7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.110 CONTROLSS_CTRL_ETPWM8_RST Register (Offset = 320h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1320. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0320h

Figure 2-657. CONTROLSS_CTRL_ETPWM8_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1321. ETPWM8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.111 CONTROLSS_CTRL_ETPWM9_RST Register (Offset = 324h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1322. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0324h

Figure 2-658. CONTROLSS_CTRL_ETPWM9_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1323. ETPWM9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.112 CONTROLSS_CTRL_ETPWM10_RST Register (Offset = 328h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1324. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0328h

Figure 2-659. CONTROLSS_CTRL_ETPWM10_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1325. ETPWM10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.113 CONTROLSS_CTRL_ETPWM11_RST Register (Offset = 32Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1326. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 032Ch

Figure 2-660. CONTROLSS_CTRL_ETPWM11_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1327. ETPWM11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.114 CONTROLSS_CTRL_ETPWM12_RST Register (Offset = 330h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1328. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0330h

Figure 2-661. CONTROLSS_CTRL_ETPWM12_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1329. ETPWM12_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.115 CONTROLSS_CTRL_ETPWM13_RST Register (Offset = 334h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1330. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0334h

Figure 2-662. CONTROLSS_CTRL_ETPWM13_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1331. ETPWM13_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.116 CONTROLSS_CTRL_ETPWM14_RST Register (Offset = 338h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1332. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0338h

Figure 2-663. CONTROLSS_CTRL_ETPWM14_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1333. ETPWM14_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.117 CONTROLSS_CTRL_ETPWM15_RST Register (Offset = 33Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1334. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 033Ch

Figure 2-664. CONTROLSS_CTRL_ETPWM15_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1335. ETPWM15_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.118 CONTROLSS_CTRL_ETPWM16_RST Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1336. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0340h

Figure 2-665. CONTROLSS_CTRL_ETPWM16_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1337. ETPWM16_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.119 CONTROLSS_CTRL_ETPWM17_RST Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1338. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0344h

Figure 2-666. CONTROLSS_CTRL_ETPWM17_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1339. ETPWM17_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.120 CONTROLSS_CTRL_ETPWM18_RST Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1340. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0348h

Figure 2-667. CONTROLSS_CTRL_ETPWM18_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1341. ETPWM18_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.121 CONTROLSS_CTRL_ETPWM19_RST Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1342. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 034Ch

Figure 2-668. CONTROLSS_CTRL_ETPWM19_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RST		
NONE					RW		
0					0		

Access Types Legend

Table 2-1343. ETPWM19_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.122 CONTROLSS_CTRL_ETPWM20_RST Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1344. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0350h

Figure 2-669. CONTROLSS_CTRL_ETPWM20_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1345. ETPWM20_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.123 CONTROLSS_CTRL_ETPWM21_RST Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1346. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0354h

Figure 2-670. CONTROLSS_CTRL_ETPWM21_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1347. ETPWM21_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.124 CONTROLSS_CTRL_ETPWM22_RST Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1348. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0358h

Figure 2-671. CONTROLSS_CTRL_ETPWM22_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1349. ETPWM22_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.125 CONTROLSS_CTRL_ETPWM23_RST Register (Offset = 35Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1350. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 035Ch

Figure 2-672. CONTROLSS_CTRL_ETPWM23_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RST		
NONE					RW		
0					0		

Access Types Legend

Table 2-1351. ETPWM23_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.126 CONTROLSS_CTRL_ETPWM24_RST Register (Offset = 360h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1352. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0360h

Figure 2-673. CONTROLSS_CTRL_ETPWM24_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1353. ETPWM24_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.127 CONTROLSS_CTRL_ETPWM25_RST Register (Offset = 364h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1354. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0364h

Figure 2-674. CONTROLSS_CTRL_ETPWM25_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1355. ETPWM25_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.128 CONTROLSS_CTRL_ETPWM26_RST Register (Offset = 368h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1356. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0368h

Figure 2-675. CONTROLSS_CTRL_ETPWM26_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1357. ETPWM26_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.129 CONTROLSS_CTRL_ETPWM27_RST Register (Offset = 36Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1358. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 036Ch

Figure 2-676. CONTROLSS_CTRL_ETPWM27_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1359. ETPWM27_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.130 CONTROLSS_CTRL_ETPWM28_RST Register (Offset = 370h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1360. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0370h

Figure 2-677. CONTROLSS_CTRL_ETPWM28_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1361. ETPWM28_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.131 CONTROLSS_CTRL_ETPWM29_RST Register (Offset = 374h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1362. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0374h

Figure 2-678. CONTROLSS_CTRL_ETPWM29_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1363. ETPWM29_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.132 CONTROLSS_CTRL_ETPWM30_RST Register (Offset = 378h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1364. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0378h

Figure 2-679. CONTROLSS_CTRL_ETPWM30_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1365. ETPWM30_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.133 CONTROLSS_CTRL_ETPWM31_RST Register (Offset = 37Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1366. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 037Ch

Figure 2-680. CONTROLSS_CTRL_ETPWM31_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RST		
NONE					RW		
0					0		

Access Types Legend

Table 2-1367. ETPWM31_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

2.6.134 CONTROLSS_CTRL_FSI_TX0_RST Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1368. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0380h

Figure 2-681. CONTROLSS_CTRL_FSI_TX0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1369. FSI_TX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

2.6.135 CONTROLSS_CTRL_FSI_TX1_RST Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1370. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0384h

Figure 2-682. CONTROLSS_CTRL_FSI_TX1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1371. FSI_TX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

2.6.136 CONTROLSS_CTRL_FSI_TX2_RST Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1372. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0388h

Figure 2-683. CONTROLSS_CTRL_FSI_TX2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1373. FSI_TX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

2.6.137 CONTROLSS_CTRL_FSI_TX3_RST Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1374. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 038Ch

Figure 2-684. CONTROLSS_CTRL_FSI_TX3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1375. FSI_TX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

2.6.138 CONTROLSS_CTRL_FSI_RX0_RST Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1376. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0390h

Figure 2-685. CONTROLSS_CTRL_FSI_RX0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1377. FSI_RX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

2.6.139 CONTROLSS_CTRL_FSI_RX1_RST Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1378. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0394h

Figure 2-686. CONTROLSS_CTRL_FSI_RX1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1379. FSI_RX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

2.6.140 CONTROLSS_CTRL_FSI_RX2_RST Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1380. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0398h

Figure 2-687. CONTROLSS_CTRL_FSI_RX2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1381. FSI_RX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

2.6.141 CONTROLSS_CTRL_FSI_RX3_RST Register (Offset = 39Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1382. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 039Ch

Figure 2-688. CONTROLSS_CTRL_FSI_RX3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1383. FSI_RX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

2.6.142 CONTROLSS_CTRL_CMPSSA0_RST Register (Offset = 3A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1384. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A0h

Figure 2-689. CONTROLSS_CTRL_CMPSSA0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1385. CMPSSA0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.143 CONTROLSS_CTRL_CMPSSA1_RST Register (Offset = 3A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1386. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A4h

Figure 2-690. CONTROLSS_CTRL_CMPSSA1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1387. CMPSSA1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.144 CONTROLSS_CTRL_CMPSSA2_RST Register (Offset = 3A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1388. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A8h

Figure 2-691. CONTROLSS_CTRL_CMPSSA2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1389. CMPSSA2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.145 CONTROLSS_CTRL_CMPSSA3_RST Register (Offset = 3ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1390. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03ACh

Figure 2-692. CONTROLSS_CTRL_CMPSSA3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1391. CMPSSA3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.146 CONTROLSS_CTRL_CMPSSA4_RST Register (Offset = 3B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1392. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B0h

Figure 2-693. CONTROLSS_CTRL_CMPSSA4_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1393. CMPSSA4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.147 CONTROLSS_CTRL_CMPSSA5_RST Register (Offset = 3B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1394. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B4h

Figure 2-694. CONTROLSS_CTRL_CMPSSA5_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1395. CMPSSA5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.148 CONTROLSS_CTRL_CMPSSA6_RST Register (Offset = 3B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1396. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B8h

Figure 2-695. CONTROLSS_CTRL_CMPSSA6_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1397. CMPSSA6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.149 CONTROLSS_CTRL_CMPSSA7_RST Register (Offset = 3BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1398. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03BCh

Figure 2-696. CONTROLSS_CTRL_CMPSSA7_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1399. CMPSSA7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.150 CONTROLSS_CTRL_CMPSSA8_RST Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1400. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03C0h

Figure 2-697. CONTROLSS_CTRL_CMPSSA8_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1401. CMPSSA8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.151 CONTROLSS_CTRL_CMPSSA9_RST Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1402. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03C4h

Figure 2-698. CONTROLSS_CTRL_CMPSSA9_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1403. CMPSSA9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

2.6.152 CONTROLSS_CTRL_CMPSSB0_RST Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1404. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D0h

Figure 2-699. CONTROLSS_CTRL_CMPSSB0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1405. CMPSSB0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.153 CONTROLSS_CTRL_CMPSSB1_RST Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1406. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D4h

Figure 2-700. CONTROLSS_CTRL_CMPSSB1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1407. CMPSSB1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.154 CONTROLSS_CTRL_CMPSSB2_RST Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1408. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D8h

Figure 2-701. CONTROLSS_CTRL_CMPSSB2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1409. CMPSSB2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.155 CONTROLSS_CTRL_CMPSSB3_RST Register (Offset = 3DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1410. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03DCh

Figure 2-702. CONTROLSS_CTRL_CMPSSB3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RST		
NONE					RW		
0					0		

Access Types Legend

Table 2-1411. CMPSSB3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.156 CONTROLSS_CTRL_CMPSSB4_RST Register (Offset = 3E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1412. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E0h

Figure 2-703. CONTROLSS_CTRL_CMPSSB4_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1413. CMPSSB4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.157 CONTROLSS_CTRL_CMPSSB5_RST Register (Offset = 3E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1414. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E4h

Figure 2-704. CONTROLSS_CTRL_CMPSSB5_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1415. CMPSSB5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.158 CONTROLSS_CTRL_CMPSSB6_RST Register (Offset = 3E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1416. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E8h

Figure 2-705. CONTROLSS_CTRL_CMPSSB6_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1417. CMPSSB6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.159 CONTROLSS_CTRL_CMPSSB7_RST Register (Offset = 3ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1418. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03ECh

Figure 2-706. CONTROLSS_CTRL_CMPSSB7_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1419. CMPSSB7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.160 CONTROLSS_CTRL_CMPSSB8_RST Register (Offset = 3F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1420. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03F0h

Figure 2-707. CONTROLSS_CTRL_CMPSSB8_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1421. CMPSSB8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.161 CONTROLSS_CTRL_CMPSSB9_RST Register (Offset = 3F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1422. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03F4h

Figure 2-708. CONTROLSS_CTRL_CMPSSB9_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1423. CMPSSB9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

2.6.162 CONTROLSS_CTRL_ECAP0_RST Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1424. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0400h

Figure 2-709. CONTROLSS_CTRL_ECAP0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1425. ECAP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.163 CONTROLSS_CTRL_ECAP1_RST Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1426. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0404h

Figure 2-710. CONTROLSS_CTRL_ECAP1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1427. ECAP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.164 CONTROLSS_CTRL_ECAP2_RST Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1428. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0408h

Figure 2-711. CONTROLSS_CTRL_ECAP2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1429. ECAP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.165 CONTROLSS_CTRL_ECAP3_RST Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1430. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 040Ch

Figure 2-712. CONTROLSS_CTRL_ECAP3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1431. ECAP3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.166 CONTROLSS_CTRL_ECAP4_RST Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1432. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0410h

Figure 2-713. CONTROLSS_CTRL_ECAP4_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1433. ECAP4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.167 CONTROLSS_CTRL_ECAP5_RST Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1434. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0414h

Figure 2-714. CONTROLSS_CTRL_ECAP5_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1435. ECAP5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.168 CONTROLSS_CTRL_ECAP6_RST Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1436. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0418h

Figure 2-715. CONTROLSS_CTRL_ECAP6_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1437. ECAP6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.169 CONTROLSS_CTRL_ECAP7_RST Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1438. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 041Ch

Figure 2-716. CONTROLSS_CTRL_ECAP7_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1439. ECAP7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.170 CONTROLSS_CTRL_ECAP8_RST Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1440. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0420h

Figure 2-717. CONTROLSS_CTRL_ECAP8_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1441. ECAP8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.171 CONTROLSS_CTRL_ECAP9_RST Register (Offset = 424h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1442. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0424h

Figure 2-718. CONTROLSS_CTRL_ECAP9_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1443. ECAP9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

2.6.172 CONTROLSS_CTRL_EQEP0_RST Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1444. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0440h

Figure 2-719. CONTROLSS_CTRL_EQEP0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1445. EQEP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

2.6.173 CONTROLSS_CTRL_EQEP1_RST Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1446. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0444h

Figure 2-720. CONTROLSS_CTRL_EQEP1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1447. EQEP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

2.6.174 CONTROLSS_CTRL_EQEP2_RST Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1448. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0448h

Figure 2-721. CONTROLSS_CTRL_EQEP2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1449. EQEP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

2.6.175 CONTROLSS_CTRL_SDFM0_RST Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1450. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0450h

Figure 2-722. CONTROLSS_CTRL_SDFM0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1451. SDFM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding sdfm

2.6.176 CONTROLSS_CTRL_SDFM1_RST Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1452. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0454h

Figure 2-723. CONTROLSS_CTRL_SDFM1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1453. SDFM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding sdfm

2.6.177 CONTROLSS_CTRL_DAC_RST Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1454. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0458h

Figure 2-724. CONTROLSS_CTRL_DAC_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1455. DAC_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for dac

2.6.178 CONTROLSS_CTRL_ADC0_RST Register (Offset = 45Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1456. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 045Ch

Figure 2-725. CONTROLSS_CTRL_ADC0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1457. ADC0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

2.6.179 CONTROLSS_CTRL_ADC1_RST Register (Offset = 460h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1458. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0460h

Figure 2-726. CONTROLSS_CTRL_ADC1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1459. ADC1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

2.6.180 CONTROLSS_CTRL_ADC2_RST Register (Offset = 464h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1460. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0464h

Figure 2-727. CONTROLSS_CTRL_ADC2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1461. ADC2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

2.6.181 CONTROLSS_CTRL_ADC3_RST Register (Offset = 468h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1462. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0468h

Figure 2-728. CONTROLSS_CTRL_ADC3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1463. ADC3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

2.6.182 CONTROLSS_CTRL_ADC4_RST Register (Offset = 46Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1464. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 046Ch

Figure 2-729. CONTROLSS_CTRL_ADC4_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1465. ADC4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

2.6.183 CONTROLSS_CTRL_OTTO0_RST Register (Offset = 470h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1466. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0470h

Figure 2-730. CONTROLSS_CTRL_OTTO0_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1467. OTTO0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

2.6.184 CONTROLSS_CTRL_OTTO1_RST Register (Offset = 474h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1468. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0474h

Figure 2-731. CONTROLSS_CTRL_OTTO1_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1469. OTTO1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

2.6.185 CONTROLSS_CTRL_OTTO2_RST Register (Offset = 478h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1470. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0478h

Figure 2-732. CONTROLSS_CTRL_OTTO2_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1471. OTTO2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

2.6.186 CONTROLSS_CTRL_OTTO3_RST Register (Offset = 47Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1472. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 047Ch

Figure 2-733. CONTROLSS_CTRL_OTTO3_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						RST	
NONE						RW	
0						0	

Access Types Legend

Table 2-1473. OTTO3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

2.6.187 CONTROLSS_CTRL_EPWM0_HALTEN Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1474. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0500h

Figure 2-734. CONTROLSS_CTRL_EPWM0_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1475. EPWM0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.188 CONTROLSS_CTRL_EPWM1_HALTEN Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1476. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0504h

Figure 2-735. CONTROLSS_CTRL_EPWM1_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1477. EPWM1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.189 CONTROLSS_CTRL_EPWM2_HALTEN Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1478. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0508h

Figure 2-736. CONTROLSS_CTRL_EPWM2_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1479. EPWM2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.190 CONTROLSS_CTRL_EPWM3_HALTEN Register (Offset = 50Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1480. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 050Ch

Figure 2-737. CONTROLSS_CTRL_EPWM3_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1481. EPWM3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.191 CONTROLSS_CTRL_EPWM4_HALTEN Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1482. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0510h

Figure 2-738. CONTROLSS_CTRL_EPWM4_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1483. EPWM4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.192 CONTROLSS_CTRL_EPWM5_HALTEN Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1484. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0514h

Figure 2-739. CONTROLSS_CTRL_EPWM5_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1485. EPWM5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.193 CONTROLSS_CTRL_EPWM6_HALTEN Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1486. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0518h

Figure 2-740. CONTROLSS_CTRL_EPWM6_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1487. EPWM6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.194 CONTROLSS_CTRL_EPWM7_HALTEN Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1488. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 051Ch

Figure 2-741. CONTROLSS_CTRL_EPWM7_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1489. EPWM7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.195 CONTROLSS_CTRL_EPWM8_HALTEN Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1490. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0520h

Figure 2-742. CONTROLSS_CTRL_EPWM8_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1491. EPWM8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.196 CONTROLSS_CTRL_EPWM9_HALTEN Register (Offset = 524h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1492. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0524h

Figure 2-743. CONTROLSS_CTRL_EPWM9_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1493. EPWM9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.197 CONTROLSS_CTRL_EPWM10_HALTEN Register (Offset = 528h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1494. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0528h

Figure 2-744. CONTROLSS_CTRL_EPWM10_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1495. EPWM10_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.198 CONTROLSS_CTRL_EPWM11_HALTEN Register (Offset = 52Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1496. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 052Ch

Figure 2-745. CONTROLSS_CTRL_EPWM11_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1497. EPWM11_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.199 CONTROLSS_CTRL_EPWM12_HALTEN Register (Offset = 530h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1498. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0530h

Figure 2-746. CONTROLSS_CTRL_EPWM12_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1499. EPWM12_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.200 CONTROLSS_CTRL_EPWM13_HALTEN Register (Offset = 534h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1500. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0534h

Figure 2-747. CONTROLSS_CTRL_EPWM13_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1501. EPWM13_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.201 CONTROLSS_CTRL_EPWM14_HALTEN Register (Offset = 538h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1502. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0538h

Figure 2-748. CONTROLSS_CTRL_EPWM14_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1503. EPWM14_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.202 CONTROLSS_CTRL_EPWM15_HALTEN Register (Offset = 53Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-1504. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 053Ch

Figure 2-749. CONTROLSS_CTRL_EPWM15_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1505. EPWM15_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.203 CONTROLSS_CTRL_EPWM16_HALTEN Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1506. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0540h

Figure 2-750. CONTROLSS_CTRL_EPWM16_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1507. EPWM16_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.204 CONTROLSS_CTRL_EPWM17_HALTEN Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1508. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0544h

Figure 2-751. CONTROLSS_CTRL_EPWM17_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1509. EPWM17_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.205 CONTROLSS_CTRL_EPWM18_HALTEN Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1510. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0548h

Figure 2-752. CONTROLSS_CTRL_EPWM18_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1511. EPWM18_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.206 CONTROLSS_CTRL_EPWM19_HALTEN Register (Offset = 54Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1512. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 054Ch

Figure 2-753. CONTROLSS_CTRL_EPWM19_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1513. EPWM19_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.207 CONTROLSS_CTRL_EPWM20_HALTEN Register (Offset = 550h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1514. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0550h

Figure 2-754. CONTROLSS_CTRL_EPWM20_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1515. EPWM20_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.208 CONTROLSS_CTRL_EPWM21_HALTEN Register (Offset = 554h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1516. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0554h

Figure 2-755. CONTROLSS_CTRL_EPWM21_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1517. EPWM21_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.209 CONTROLSS_CTRL_EPWM22_HALTEN Register (Offset = 558h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1518. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0558h

Figure 2-756. CONTROLSS_CTRL_EPWM22_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1519. EPWM22_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.210 CONTROLSS_CTRL_EPWM23_HALTEN Register (Offset = 55Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1520. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 055Ch

Figure 2-757. CONTROLSS_CTRL_EPWM23_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1521. EPWM23_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.211 CONTROLSS_CTRL_EPWM24_HALTEN Register (Offset = 560h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1522. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0560h

Figure 2-758. CONTROLSS_CTRL_EPWM24_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1523. EPWM24_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.212 CONTROLSS_CTRL_EPWM25_HALTEN Register (Offset = 564h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1524. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0564h

Figure 2-759. CONTROLSS_CTRL_EPWM25_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1525. EPWM25_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.213 CONTROLSS_CTRL_EPWM26_HALTEN Register (Offset = 568h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1526. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0568h

Figure 2-760. CONTROLSS_CTRL_EPWM26_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1527. EPWM26_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.214 CONTROLSS_CTRL_EPWM27_HALTEN Register (Offset = 56Ch) [reset = h]

Short Description: RW

Long Description:

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Table 2-1528. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 056Ch

Figure 2-761. CONTROLSS_CTRL_EPWM27_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1529. EPWM27_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.215 CONTROLSS_CTRL_EPWM28_HALTEN Register (Offset = 570h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1530. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0570h

Figure 2-762. CONTROLSS_CTRL_EPWM28_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1531. EPWM28_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.216 CONTROLSS_CTRL_EPWM29_HALTEN Register (Offset = 574h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1532. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0574h

Figure 2-763. CONTROLSS_CTRL_EPWM29_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1533. EPWM29_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.217 CONTROLSS_CTRL_EPWM30_HALTEN Register (Offset = 578h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1534. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0578h

Figure 2-764. CONTROLSS_CTRL_EPWM30_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1535. EPWM30_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.218 CONTROLSS_CTRL_EPWM31_HALTEN Register (Offset = 57Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1536. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 057Ch

Figure 2-765. CONTROLSS_CTRL_EPWM31_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1537. EPWM31_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.219 CONTROLSS_CTRL_CMPSSA0_HALTEN Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1538. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0580h

Figure 2-766. CONTROLSS_CTRL_CMPSSA0_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1539. CMPSSA0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.220 CONTROLSS_CTRL_CMPSSA1_HALTEN Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1540. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0584h

Figure 2-767. CONTROLSS_CTRL_CMPSSA1_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1541. CMPSSA1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.221 CONTROLSS_CTRL_CMPSSA2_HALTEN Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1542. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0588h

Figure 2-768. CONTROLSS_CTRL_CMPSSA2_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1543. CMPSSA2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.222 CONTROLSS_CTRL_CMPSSA3_HALTEN Register (Offset = 58Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1544. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 058Ch

Figure 2-769. CONTROLSS_CTRL_CMPSSA3_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1545. CMPSSA3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.223 CONTROLSS_CTRL_CMPSSA4_HALTEN Register (Offset = 590h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1546. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0590h

Figure 2-770. CONTROLSS_CTRL_CMPSSA4_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1547. CMPSSA4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.224 CONTROLSS_CTRL_CMPSSA5_HALTEN Register (Offset = 594h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1548. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0594h

Figure 2-771. CONTROLSS_CTRL_CMPSSA5_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1549. CMPSSA5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.225 CONTROLSS_CTRL_CMPSSA6_HALTEN Register (Offset = 598h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1550. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0598h

Figure 2-772. CONTROLSS_CTRL_CMPSSA6_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1551. CMPSSA6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.226 CONTROLSS_CTRL_CMPSSA7_HALTEN Register (Offset = 59Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1552. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 059Ch

Figure 2-773. CONTROLSS_CTRL_CMPSSA7_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1553. CMPSSA7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.227 CONTROLSS_CTRL_CMPSSA8_HALTEN Register (Offset = 5A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1554. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A0h

Figure 2-774. CONTROLSS_CTRL_CMPSSA8_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1555. CMPSSA8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.228 CONTROLSS_CTRL_CMPSSA9_HALTEN Register (Offset = 5A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1556. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A4h

Figure 2-775. CONTROLSS_CTRL_CMPSSA9_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1557. CMPSSA9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.229 CONTROLSS_CTRL_CMPSSB0_HALTEN Register (Offset = 5A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1558. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A8h

Figure 2-776. CONTROLSS_CTRL_CMPSSB0_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1559. CMPSSB0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.230 CONTROLSS_CTRL_CMPSSB1_HALTEN Register (Offset = 5ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1560. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05ACh

Figure 2-777. CONTROLSS_CTRL_CMPSSB1_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1561. CMPSSB1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.231 CONTROLSS_CTRL_CMPSSB2_HALTEN Register (Offset = 5B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1562. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B0h

Figure 2-778. CONTROLSS_CTRL_CMPSSB2_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1563. CMPSSB2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.232 CONTROLSS_CTRL_CMPSSB3_HALTEN Register (Offset = 5B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1564. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B4h

Figure 2-779. CONTROLSS_CTRL_CMPSSB3_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1565. CMPSSB3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.233 CONTROLSS_CTRL_CMPSSB4_HALTEN Register (Offset = 5B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1566. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B8h

Figure 2-780. CONTROLSS_CTRL_CMPSSB4_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1567. CMPSSB4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.234 CONTROLSS_CTRL_CMPSSB5_HALTEN Register (Offset = 5BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1568. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05BCh

Figure 2-781. CONTROLSS_CTRL_CMPSSB5_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1569. CMPSSB5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.235 CONTROLSS_CTRL_CMPSSB6_HALTEN Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1570. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C0h

Figure 2-782. CONTROLSS_CTRL_CMPSSB6_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1571. CMPSSB6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.236 CONTROLSS_CTRL_CMPSSB7_HALTEN Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1572. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C4h

Figure 2-783. CONTROLSS_CTRL_CMPSSB7_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1573. CMPSSB7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.237 CONTROLSS_CTRL_CMPSSB8_HALTEN Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1574. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C8h

Figure 2-784. CONTROLSS_CTRL_CMPSSB8_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1575. CMPSSB8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.238 CONTROLSS_CTRL_CMPSSB9_HALTEN Register (Offset = 5CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1576. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05CCh

Figure 2-785. CONTROLSS_CTRL_CMPSSB9_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1577. CMPSSB9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.239 CONTROLSS_CTRL_ECAP0_HALTEN Register (Offset = 5D0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1578. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D0h

Figure 2-786. CONTROLSS_CTRL_ECAP0_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1579. ECAP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.240 CONTROLSS_CTRL_ECAP1_HALTEN Register (Offset = 5D4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1580. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D4h

Figure 2-787. CONTROLSS_CTRL_ECAP1_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1581. ECAP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.241 CONTROLSS_CTRL_ECAP2_HALTEN Register (Offset = 5D8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1582. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D8h

Figure 2-788. CONTROLSS_CTRL_ECAP2_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1583. ECAP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.242 CONTROLSS_CTRL_ECAP3_HALTEN Register (Offset = 5DCh) [reset = h]

Short Description: RW

Long Description:

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Table 2-1584. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05DCh

Figure 2-789. CONTROLSS_CTRL_ECAP3_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1585. ECAP3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.243 CONTROLSS_CTRL_ECAP4_HALTEN Register (Offset = 5E0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1586. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E0h

Figure 2-790. CONTROLSS_CTRL_ECAP4_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1587. ECAP4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.244 CONTROLSS_CTRL_ECAP5_HALTEN Register (Offset = 5E4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1588. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E4h

Figure 2-791. CONTROLSS_CTRL_ECAP5_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1589. ECAP5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.245 CONTROLSS_CTRL_ECAP6_HALTEN Register (Offset = 5E8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1590. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E8h

Figure 2-792. CONTROLSS_CTRL_ECAP6_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1591. ECAP6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.246 CONTROLSS_CTRL_ECAP7_HALTEN Register (Offset = 5ECh) [reset = h]

Short Description: RW

Long Description:

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Table 2-1592. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05ECh

Figure 2-793. CONTROLSS_CTRL_ECAP7_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1593. ECAP7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.247 CONTROLSS_CTRL_ECAP8_HALTEN Register (Offset = 5F0h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1594. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F0h

Figure 2-794. CONTROLSS_CTRL_ECAP8_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1595. ECAP8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.248 CONTROLSS_CTRL_ECAP9_HALTEN Register (Offset = 5F4h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1596. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F4h

Figure 2-795. CONTROLSS_CTRL_ECAP9_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1597. ECAP9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.249 CONTROLSS_CTRL_EQEP0_HALTEN Register (Offset = 5F8h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1598. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F8h

Figure 2-796. CONTROLSS_CTRL_EQEP0_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1599. EQEP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.250 CONTROLSS_CTRL_EQEP1_HALTEN Register (Offset = 5FCh) [reset = h]

Short Description: RW

Long Description:

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Table 2-1600. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05FCh

Figure 2-797. CONTROLSS_CTRL_EQEP1_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1601. EQEP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.251 CONTROLSS_CTRL_EQEP2_HALTEN Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

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Table 2-1602. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0600h

Figure 2-798. CONTROLSS_CTRL_EQEP2_HALTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				CR5B1	CR5A1	CR5B0	CR5A0
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1603. EQEP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

2.6.252 CONTROLSS_CTRL_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

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Table 2-1604. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1008h

Figure 2-799. CONTROLSS_CTRL_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK0															
RW															
0															

Access Types Legend

Table 2-1605. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

2.6.253 CONTROLSS_CTRL_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

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Table 2-1606. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 100Ch

Figure 2-800. CONTROLSS_CTRL_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK0_KICK1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK0_KICK1															
RW															
0															

Access Types Legend

Table 2-1607. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

2.6.254 CONTROLSS_CTRL_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

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Table 2-1608. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1010h

Figure 2-801. CONTROLSS_CTRL_INTR_RAW_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1609. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

2.6.255 CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

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Table 2-1610. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1014h

Figure 2-802. CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1611. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

2.6.256 CONTROLSS_CTRL_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

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Table 2-1612. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1018h

Figure 2-803. CONTROLSS_CTRL_INTR_ENABLE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1613. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

2.6.257 CONTROLSS_CTRL_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

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Table 2-1614. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 101Ch

Figure 2-804. CONTROLSS_CTRL_INTR_ENABLE_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 2-1615. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

2.6.258 CONTROLSS_CTRL_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

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Table 2-1616. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1020h

Figure 2-805. CONTROLSS_CTRL_EOI Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_VECTOR							
RW							
0							

Access Types Legend

Table 2-1617. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

2.6.259 CONTROLSS_CTRL_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

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Table 2-1618. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1024h

Figure 2-806. CONTROLSS_CTRL_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ADDR															
RO															
0															

Access Types Legend

Table 2-1619. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

2.6.260 CONTROLSS_CTRL_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

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Table 2-1620. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1028h

Figure 2-807. CONTROLSS_CTRL_FAULT_TYPE_STATUS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	RO	RO					
0	0	0					

Access Types Legend

Table 2-1621. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

2.6.261 CONTROLSS_CTRL_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

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Table 2-1622. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 102Ch

Figure 2-808. CONTROLSS_CTRL_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAULT_XID												FAULT_ROUTEID			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_ROUTEID								FAULT_PRIVID							
RO								RO							
0								0							

Access Types Legend

Table 2-1623. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

2.6.262 CONTROLSS_CTRL_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

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Table 2-1624. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1030h

Figure 2-809. CONTROLSS_CTRL_FAULT_CLEAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
FAULT_CLR							
WO							
0							

Access Types Legend

Table 2-1625. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

Table 2-1626. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

3 AM263x Real-time Control Subsystem Registers (CONTROLSS)

The AM263x Real-time Control Subsystem (CONTROLSS) registers are described below.

3.1 C2K_ADC Registers

Table 3-1. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
0h	16	CONTROLSS_ADC0_CFG_ADCCTL1	ADC Control 1 Register	502C 0000h	502C 1000h	502C 2000h
2h	16	CONTROLSS_ADC0_CFG_ADCCTL2	ADC Control 2 Register	502C 0002h	502C 1002h	502C 2002h
4h	16	CONTROLSS_ADC0_CFG_ADCBURSTCTL	ADC Burst Control Register	502C 0004h	502C 1004h	502C 2004h
6h	16	CONTROLSS_ADC0_CFG_ADCINTFLG	ADC Interrupt Flag Register	502C 0006h	502C 1006h	502C 2006h
8h	16	CONTROLSS_ADC0_CFG_ADCINTFLGCLR	ADC Interrupt Flag Clear Register	502C 0008h	502C 1008h	502C 2008h
Ah	16	CONTROLSS_ADC0_CFG_ADCINTOVF	ADC Interrupt Overflow Register	502C 000Ah	502C 100Ah	502C 200Ah
Ch	16	CONTROLSS_ADC0_CFG_ADCINTOVFCLR	ADC Interrupt Overflow Clear Register	502C 000Ch	502C 100Ch	502C 200Ch
Eh	16	CONTROLSS_ADC0_CFG_ADCINTSEL1N2	ADC Interrupt 1 and 2 Selection Register	502C 000Eh	502C 100Eh	502C 200Eh
10h	16	CONTROLSS_ADC0_CFG_ADCINTSEL3N4	ADC Interrupt 3 and 4 Selection Register	502C 0010h	502C 1010h	502C 2010h
12h	16	CONTROLSS_ADC0_CFG_ADCSOCPRICTL	ADC SOC Priority Control Register	502C 0012h	502C 1012h	502C 2012h
14h	16	CONTROLSS_ADC0_CFG_ADCINTSOCSEL1	ADC Interrupt SOC Selection 1 Register	502C 0014h	502C 1014h	502C 2014h
16h	16	CONTROLSS_ADC0_CFG_ADCINTSOCSEL2	ADC Interrupt SOC Selection 2 Register	502C 0016h	502C 1016h	502C 2016h
18h	16	CONTROLSS_ADC0_CFG_ADCSOCFLG1	ADC SOC Flag 1 Register	502C 0018h	502C 1018h	502C 2018h
1Ah	16	CONTROLSS_ADC0_CFG_ADCSOCFRC1	ADC SOC Force 1 Register	502C 001Ah	502C 101Ah	502C 201Ah
1Ch	16	CONTROLSS_ADC0_CFG_ADCSOCOVF1	ADC SOC Overflow 1 Register	502C 001Ch	502C 101Ch	502C 201Ch
1Eh	16	CONTROLSS_ADC0_CFG_ADCSOCOVFCLR1	ADC SOC Overflow Clear 1 Register	502C 001Eh	502C 101Eh	502C 201Eh
20h	32	CONTROLSS_ADC0_CFG_ADCSOC0CTL	ADC SOC0 Control Register	502C 0020h	502C 1020h	502C 2020h
24h	32	CONTROLSS_ADC0_CFG_ADCSOC1CTL	ADC SOC1 Control Register	502C 0024h	502C 1024h	502C 2024h
28h	32	CONTROLSS_ADC0_CFG_ADCSOC2CTL	ADC SOC2 Control Register	502C 0028h	502C 1028h	502C 2028h
2Ch	32	CONTROLSS_ADC0_CFG_ADCSOC3CTL	ADC SOC3 Control Register	502C 002Ch	502C 102Ch	502C 202Ch
30h	32	CONTROLSS_ADC0_CFG_ADCSOC4CTL	ADC SOC4 Control Register	502C 0030h	502C 1030h	502C 2030h
34h	32	CONTROLSS_ADC0_CFG_ADCSOC5CTL	ADC SOC5 Control Register	502C 0034h	502C 1034h	502C 2034h
38h	32	CONTROLSS_ADC0_CFG_ADCSOC6CTL	ADC SOC6 Control Register	502C 0038h	502C 1038h	502C 2038h

Table 3-1. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
3Ch	32	CONTROLSS_ADC0_CFG_ADCSOC7CTL	ADC SOC7 Control Register	502C 003Ch	502C 103Ch	502C 203Ch
40h	32	CONTROLSS_ADC0_CFG_ADCSOC8CTL	ADC SOC8 Control Register	502C 0040h	502C 1040h	502C 2040h
44h	32	CONTROLSS_ADC0_CFG_ADCSOC9CTL	ADC SOC9 Control Register	502C 0044h	502C 1044h	502C 2044h
48h	32	CONTROLSS_ADC0_CFG_ADCSOC10CTL	ADC SOC10 Control Register	502C 0048h	502C 1048h	502C 2048h
4Ch	32	CONTROLSS_ADC0_CFG_ADCSOC11CTL	ADC SOC11 Control Register	502C 004Ch	502C 104Ch	502C 204Ch
50h	32	CONTROLSS_ADC0_CFG_ADCSOC12CTL	ADC SOC12 Control Register	502C 0050h	502C 1050h	502C 2050h
54h	32	CONTROLSS_ADC0_CFG_ADCSOC13CTL	ADC SOC13 Control Register	502C 0054h	502C 1054h	502C 2054h
58h	32	CONTROLSS_ADC0_CFG_ADCSOC14CTL	ADC SOC14 Control Register	502C 0058h	502C 1058h	502C 2058h
5Ch	32	CONTROLSS_ADC0_CFG_ADCSOC15CTL	ADC SOC15 Control Register	502C 005Ch	502C 105Ch	502C 205Ch
60h	16	CONTROLSS_ADC0_CFG_ADCEVTSTAT	ADC Event Status Register	502C 0060h	502C 1060h	502C 2060h
64h	16	CONTROLSS_ADC0_CFG_ADCEVTCLR	ADC Event Clear Register	502C 0064h	502C 1064h	502C 2064h
68h	16	CONTROLSS_ADC0_CFG_ADCEVTSEL	ADC Event Selection Register	502C 0068h	502C 1068h	502C 2068h
6Ch	16	CONTROLSS_ADC0_CFG_ADCEVTINTSEL	ADC Event Interrupt Selection Register	502C 006Ch	502C 106Ch	502C 206Ch
70h	16	CONTROLSS_ADC0_CFG_ADCOSDETECT	ADC Open and Shorts Detect Register	502C 0070h	502C 1070h	502C 2070h
72h	16	CONTROLSS_ADC0_CFG_ADCCOUNTER	ADC Counter Register	502C 0072h	502C 1072h	502C 2072h
74h	16	CONTROLSS_ADC0_CFG_ADCREV	ADC Revision Register	502C 0074h	502C 1074h	502C 2074h
76h	16	CONTROLSS_ADC0_CFG_ADCOFFTRIM	ADC Offset Trim Register	502C 0076h	502C 1076h	502C 2076h
7Ch	32	CONTROLSS_ADC0_CFG_ADCCONFIG	ADC Config Register	502C 007Ch	502C 107Ch	502C 207Ch
80h	16	CONTROLSS_ADC0_CFG_ADCPPB1CONFIG	ADC PPB1 Config Register	502C 0080h	502C 1080h	502C 2080h
82h	16	CONTROLSS_ADC0_CFG_ADCPPB1STAMP	ADC PPB1 Sample Delay Time Stamp Register	502C 0082h	502C 1082h	502C 2082h
84h	16	CONTROLSS_ADC0_CFG_ADCPPB1OFFCAL	ADC PPB1 Offset Calibration Register	502C 0084h	502C 1084h	502C 2084h
86h	16	CONTROLSS_ADC0_CFG_ADCPPB1OFFREF	ADC PPB1 Offset Reference Register	502C 0086h	502C 1086h	502C 2086h
88h	32	CONTROLSS_ADC0_CFG_ADCPPB1TRIPHI	ADC PPB1 Trip High Register	502C 0088h	502C 1088h	502C 2088h
8Ch	32	CONTROLSS_ADC0_CFG_ADCPPB1TRIPLO	ADC PPB1 Trip Low/ Trigger Time Stamp Register	502C 008Ch	502C 108Ch	502C 208Ch
90h	16	CONTROLSS_ADC0_CFG_ADCPPB2CONFIG	ADC PPB2 Config Register	502C 0090h	502C 1090h	502C 2090h

Table 3-1. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
92h	16	CONTROLSS_ADC0_CFG_ADCPPB2STAMP	ADC PPB2 Sample Delay Time Stamp Register	502C 0092h	502C 1092h	502C 2092h
94h	16	CONTROLSS_ADC0_CFG_ADCPPB2OFFCAL	ADC PPB2 Offset Calibration Register	502C 0094h	502C 1094h	502C 2094h
96h	16	CONTROLSS_ADC0_CFG_ADCPPB2OFFREF	ADC PPB2 Offset Reference Register	502C 0096h	502C 1096h	502C 2096h
98h	32	CONTROLSS_ADC0_CFG_ADCPPB2TRIPHI	ADC PPB2 Trip High Register	502C 0098h	502C 1098h	502C 2098h
9Ch	32	CONTROLSS_ADC0_CFG_ADCPPB2TRIPLO	ADC PPB2 Trip Low/ Trigger Time Stamp Register	502C 009Ch	502C 109Ch	502C 209Ch
A0h	16	CONTROLSS_ADC0_CFG_ADCPPB3CONFIG	ADC PPB3 Config Register	502C 00A0h	502C 10A0h	502C 20A0h
A2h	16	CONTROLSS_ADC0_CFG_ADCPPB3STAMP	ADC PPB3 Sample Delay Time Stamp Register	502C 00A2h	502C 10A2h	502C 20A2h
A4h	16	CONTROLSS_ADC0_CFG_ADCPPB3OFFCAL	ADC PPB3 Offset Calibration Register	502C 00A4h	502C 10A4h	502C 20A4h
A6h	16	CONTROLSS_ADC0_CFG_ADCPPB3OFFREF	ADC PPB3 Offset Reference Register	502C 00A6h	502C 10A6h	502C 20A6h
A8h	32	CONTROLSS_ADC0_CFG_ADCPPB3TRIPHI	ADC PPB3 Trip High Register	502C 00A8h	502C 10A8h	502C 20A8h
ACh	32	CONTROLSS_ADC0_CFG_ADCPPB3TRIPLO	ADC PPB3 Trip Low/ Trigger Time Stamp Register	502C 00ACh	502C 10ACh	502C 20ACh
B0h	16	CONTROLSS_ADC0_CFG_ADCPPB4CONFIG	ADC PPB4 Config Register	502C 00B0h	502C 10B0h	502C 20B0h
B2h	16	CONTROLSS_ADC0_CFG_ADCPPB4STAMP	ADC PPB4 Sample Delay Time Stamp Register	502C 00B2h	502C 10B2h	502C 20B2h
B4h	16	CONTROLSS_ADC0_CFG_ADCPPB4OFFCAL	ADC PPB4 Offset Calibration Register	502C 00B4h	502C 10B4h	502C 20B4h
B6h	16	CONTROLSS_ADC0_CFG_ADCPPB4OFFREF	ADC PPB4 Offset Reference Register	502C 00B6h	502C 10B6h	502C 20B6h
B8h	32	CONTROLSS_ADC0_CFG_ADCPPB4TRIPHI	ADC PPB4 Trip High Register	502C 00B8h	502C 10B8h	502C 20B8h
BCh	32	CONTROLSS_ADC0_CFG_ADCPPB4TRIPLO	ADC PPB4 Trip Low/ Trigger Time Stamp Register	502C 00BCh	502C 10BCh	502C 20BCh
DEh	16	CONTROLSS_ADC0_CFG_ADCINTCYCLE	ADC Early Interrupt Generation Cycle	502C 00DEh	502C 10DEh	502C 20DEh
E0h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM1	ADC Linearity Trim 1 Register	502C 00E0h	502C 10E0h	502C 20E0h
E4h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM2	ADC Linearity Trim 2 Register	502C 00E4h	502C 10E4h	502C 20E4h
E8h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM3	ADC Linearity Trim 3 Register	502C 00E8h	502C 10E8h	502C 20E8h
ECh	32	CONTROLSS_ADC0_CFG_ADCINLTRIM4	ADC Linearity Trim 4 Register	502C 00ECh	502C 10ECh	502C 20ECh
F0h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM5	ADC Linearity Trim 5 Register	502C 00F0h	502C 10F0h	502C 20F0h
F4h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM6	ADC Linearity Trim 6 Register	502C 00F4h	502C 10F4h	502C 20F4h

Table 3-1. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
FCh	32	CONTROLSS_ADC0_CFG_ADCINLTRIMCTL	ADC Linearity Trim Control Register	502C 00FCh	502C 10FCh	502C 20FCh

Table 3-2. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
0h	16	CONTROLSS_ADC0_CFG_ADCCTL1	ADC Control 1 Register	502C 3000h	502C 4000h
2h	16	CONTROLSS_ADC0_CFG_ADCCTL2	ADC Control 2 Register	502C 3002h	502C 4002h
4h	16	CONTROLSS_ADC0_CFG_ADCBURSTCTL	ADC Burst Control Register	502C 3004h	502C 4004h
6h	16	CONTROLSS_ADC0_CFG_ADCINTFLG	ADC Interrupt Flag Register	502C 3006h	502C 4006h
8h	16	CONTROLSS_ADC0_CFG_ADCINTFLGCLR	ADC Interrupt Flag Clear Register	502C 3008h	502C 4008h
Ah	16	CONTROLSS_ADC0_CFG_ADCINTOVF	ADC Interrupt Overflow Register	502C 300Ah	502C 400Ah
Ch	16	CONTROLSS_ADC0_CFG_ADCINTOVFCLR	ADC Interrupt Overflow Clear Register	502C 300Ch	502C 400Ch
Eh	16	CONTROLSS_ADC0_CFG_ADCINTSEL1N2	ADC Interrupt 1 and 2 Selection Register	502C 300Eh	502C 400Eh
10h	16	CONTROLSS_ADC0_CFG_ADCINTSEL3N4	ADC Interrupt 3 and 4 Selection Register	502C 3010h	502C 4010h
12h	16	CONTROLSS_ADC0_CFG_ADCSOCPRICTL	ADC SOC Priority Control Register	502C 3012h	502C 4012h
14h	16	CONTROLSS_ADC0_CFG_ADCINTSOCSEL1	ADC Interrupt SOC Selection 1 Register	502C 3014h	502C 4014h
16h	16	CONTROLSS_ADC0_CFG_ADCINTSOCSEL2	ADC Interrupt SOC Selection 2 Register	502C 3016h	502C 4016h
18h	16	CONTROLSS_ADC0_CFG_ADCSOCFLG1	ADC SOC Flag 1 Register	502C 3018h	502C 4018h
1Ah	16	CONTROLSS_ADC0_CFG_ADCSOCFRC1	ADC SOC Force 1 Register	502C 301Ah	502C 401Ah
1Ch	16	CONTROLSS_ADC0_CFG_ADCSOCOVF1	ADC SOC Overflow 1 Register	502C 301Ch	502C 401Ch
1Eh	16	CONTROLSS_ADC0_CFG_ADCSOCOVFCLR1	ADC SOC Overflow Clear 1 Register	502C 301Eh	502C 401Eh
20h	32	CONTROLSS_ADC0_CFG_ADCSOC0CTL	ADC SOC0 Control Register	502C 3020h	502C 4020h
24h	32	CONTROLSS_ADC0_CFG_ADCSOC1CTL	ADC SOC1 Control Register	502C 3024h	502C 4024h
28h	32	CONTROLSS_ADC0_CFG_ADCSOC2CTL	ADC SOC2 Control Register	502C 3028h	502C 4028h
2Ch	32	CONTROLSS_ADC0_CFG_ADCSOC3CTL	ADC SOC3 Control Register	502C 302Ch	502C 402Ch
30h	32	CONTROLSS_ADC0_CFG_ADCSOC4CTL	ADC SOC4 Control Register	502C 3030h	502C 4030h
34h	32	CONTROLSS_ADC0_CFG_ADCSOC5CTL	ADC SOC5 Control Register	502C 3034h	502C 4034h

Table 3-2. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
38h	32	CONTROLSS_ADC0_CFG_ADCSOC6CTL	ADC SOC6 Control Register	502C 3038h	502C 4038h
3Ch	32	CONTROLSS_ADC0_CFG_ADCSOC7CTL	ADC SOC7 Control Register	502C 303Ch	502C 403Ch
40h	32	CONTROLSS_ADC0_CFG_ADCSOC8CTL	ADC SOC8 Control Register	502C 3040h	502C 4040h
44h	32	CONTROLSS_ADC0_CFG_ADCSOC9CTL	ADC SOC9 Control Register	502C 3044h	502C 4044h
48h	32	CONTROLSS_ADC0_CFG_ADCSOC10CTL	ADC SOC10 Control Register	502C 3048h	502C 4048h
4Ch	32	CONTROLSS_ADC0_CFG_ADCSOC11CTL	ADC SOC11 Control Register	502C 304Ch	502C 404Ch
50h	32	CONTROLSS_ADC0_CFG_ADCSOC12CTL	ADC SOC12 Control Register	502C 3050h	502C 4050h
54h	32	CONTROLSS_ADC0_CFG_ADCSOC13CTL	ADC SOC13 Control Register	502C 3054h	502C 4054h
58h	32	CONTROLSS_ADC0_CFG_ADCSOC14CTL	ADC SOC14 Control Register	502C 3058h	502C 4058h
5Ch	32	CONTROLSS_ADC0_CFG_ADCSOC15CTL	ADC SOC15 Control Register	502C 305Ch	502C 405Ch
60h	16	CONTROLSS_ADC0_CFG_ADCEVTSTAT	ADC Event Status Register	502C 3060h	502C 4060h
64h	16	CONTROLSS_ADC0_CFG_ADCEVTCLR	ADC Event Clear Register	502C 3064h	502C 4064h
68h	16	CONTROLSS_ADC0_CFG_ADCEVTSEL	ADC Event Selection Register	502C 3068h	502C 4068h
6Ch	16	CONTROLSS_ADC0_CFG_ADCEVTINTSEL	ADC Event Interrupt Selection Register	502C 306Ch	502C 406Ch
70h	16	CONTROLSS_ADC0_CFG_ADCOSDETECT	ADC Open and Shorts Detect Register	502C 3070h	502C 4070h
72h	16	CONTROLSS_ADC0_CFG_ADCCOUNTER	ADC Counter Register	502C 3072h	502C 4072h
74h	16	CONTROLSS_ADC0_CFG_ADCREV	ADC Revision Register	502C 3074h	502C 4074h
76h	16	CONTROLSS_ADC0_CFG_ADCOFFTRIM	ADC Offset Trim Register	502C 3076h	502C 4076h
7Ch	32	CONTROLSS_ADC0_CFG_ADCCONFIG	ADC Config Register	502C 307Ch	502C 407Ch
80h	16	CONTROLSS_ADC0_CFG_ADCPPB1CONFIG	ADC PPB1 Config Register	502C 3080h	502C 4080h
82h	16	CONTROLSS_ADC0_CFG_ADCPPB1STAMP	ADC PPB1 Sample Delay Time Stamp Register	502C 3082h	502C 4082h
84h	16	CONTROLSS_ADC0_CFG_ADCPPB1OFFCAL	ADC PPB1 Offset Calibration Register	502C 3084h	502C 4084h
86h	16	CONTROLSS_ADC0_CFG_ADCPPB1OFFREF	ADC PPB1 Offset Reference Register	502C 3086h	502C 4086h
88h	32	CONTROLSS_ADC0_CFG_ADCPPB1TRIPHI	ADC PPB1 Trip High Register	502C 3088h	502C 4088h
8Ch	32	CONTROLSS_ADC0_CFG_ADCPPB1TRIPLO	ADC PPB1 Trip Low/ Trigger Time Stamp Register	502C 308Ch	502C 408Ch
90h	16	CONTROLSS_ADC0_CFG_ADCPPB2CONFIG	ADC PPB2 Config Register	502C 3090h	502C 4090h

Table 3-2. CONTROLSS_ADC0_CFG, CONTROLSS_ADC0_CFG_CONTROLSS_ADC_CFG Registers, Base Address=502C 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
92h	16	CONTROLSS_ADC0_CFG_ADCPPB2STAMP	ADC PPB2 Sample Delay Time Stamp Register	502C 3092h	502C 4092h
94h	16	CONTROLSS_ADC0_CFG_ADCPPB2OFFCAL	ADC PPB2 Offset Calibration Register	502C 3094h	502C 4094h
96h	16	CONTROLSS_ADC0_CFG_ADCPPB2OFFREF	ADC PPB2 Offset Reference Register	502C 3096h	502C 4096h
98h	32	CONTROLSS_ADC0_CFG_ADCPPB2TRIPHI	ADC PPB2 Trip High Register	502C 3098h	502C 4098h
9Ch	32	CONTROLSS_ADC0_CFG_ADCPPB2TRIPLO	ADC PPB2 Trip Low/ Trigger Time Stamp Register	502C 309Ch	502C 409Ch
A0h	16	CONTROLSS_ADC0_CFG_ADCPPB3CONFIG	ADC PPB3 Config Register	502C 30A0h	502C 40A0h
A2h	16	CONTROLSS_ADC0_CFG_ADCPPB3STAMP	ADC PPB3 Sample Delay Time Stamp Register	502C 30A2h	502C 40A2h
A4h	16	CONTROLSS_ADC0_CFG_ADCPPB3OFFCAL	ADC PPB3 Offset Calibration Register	502C 30A4h	502C 40A4h
A6h	16	CONTROLSS_ADC0_CFG_ADCPPB3OFFREF	ADC PPB3 Offset Reference Register	502C 30A6h	502C 40A6h
A8h	32	CONTROLSS_ADC0_CFG_ADCPPB3TRIPHI	ADC PPB3 Trip High Register	502C 30A8h	502C 40A8h
ACh	32	CONTROLSS_ADC0_CFG_ADCPPB3TRIPLO	ADC PPB3 Trip Low/ Trigger Time Stamp Register	502C 30ACh	502C 40ACh
B0h	16	CONTROLSS_ADC0_CFG_ADCPPB4CONFIG	ADC PPB4 Config Register	502C 30B0h	502C 40B0h
B2h	16	CONTROLSS_ADC0_CFG_ADCPPB4STAMP	ADC PPB4 Sample Delay Time Stamp Register	502C 30B2h	502C 40B2h
B4h	16	CONTROLSS_ADC0_CFG_ADCPPB4OFFCAL	ADC PPB4 Offset Calibration Register	502C 30B4h	502C 40B4h
B6h	16	CONTROLSS_ADC0_CFG_ADCPPB4OFFREF	ADC PPB4 Offset Reference Register	502C 30B6h	502C 40B6h
B8h	32	CONTROLSS_ADC0_CFG_ADCPPB4TRIPHI	ADC PPB4 Trip High Register	502C 30B8h	502C 40B8h
BCh	32	CONTROLSS_ADC0_CFG_ADCPPB4TRIPLO	ADC PPB4 Trip Low/ Trigger Time Stamp Register	502C 30BCh	502C 40BCh
DEh	16	CONTROLSS_ADC0_CFG_ADCINTCYCLE	ADC Early Interrupt Generation Cycle	502C 30DEh	502C 40DEh
E0h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM1	ADC Linearity Trim 1 Register	502C 30E0h	502C 40E0h
E4h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM2	ADC Linearity Trim 2 Register	502C 30E4h	502C 40E4h
E8h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM3	ADC Linearity Trim 3 Register	502C 30E8h	502C 40E8h
ECh	32	CONTROLSS_ADC0_CFG_ADCINLTRIM4	ADC Linearity Trim 4 Register	502C 30ECh	502C 40ECh
F0h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM5	ADC Linearity Trim 5 Register	502C 30F0h	502C 40F0h
F4h	32	CONTROLSS_ADC0_CFG_ADCINLTRIM6	ADC Linearity Trim 6 Register	502C 30F4h	502C 40F4h
FCh	32	CONTROLSS_ADC0_CFG_ADCINLTRIMCTL	ADC Linearity Trim Control Register	502C 30FCh	502C 40FCh

3.1.1 CONTROLSS_ADC0_CFG_ADCCTL1 Register (Offset = 0h) [reset = h]

Short Description: ADC Control 1 Register

Long Description:

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Table 3-3. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0000h
CONTROLSS_ADC1_CFG	502C 1000h
CONTROLSS_ADC2_CFG	502C 2000h
CONTROLSS_ADC3_CFG	502C 3000h
CONTROLSS_ADC4_CFG	502C 4000h

Figure 3-1. CONTROLSS_ADC0_CFG_ADCCTL1 Name Register

15	14	13	12	11	10	9	8
RESERVED		ADCBSY	RESERVED	ADCBSYCHN			
RO		RO	RO	RO			
0		0	0	0			
7	6	5	4	3	2	1	0
ADCPWDNZ	RESERVED				INTPULSEPOS	RESERVED	
RW	RO				RW	RO	
0	0				0	0	

Access Types Legend

Table 3-4. ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	RO		Reserved
13	ADCBSY	RO	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel 1 ADC is busy and cannot sample another channel
12	RESERVED	RO		Reserved
11 - 8	ADCBSYCHN	RO	0h	ADC Busy Channel. Set when an ADC Start of Conversion (SOC) is generated. When ADCBSY=0: holds the value of the last converted SOC When ADCBSY=1: reflects the SOC currently being processed 0h SOC0 is currently processing or was last SOC converted 1h SOC1 is currently processing or was last SOC converted 2h SOC2 is currently processing or was last SOC converted 3h SOC3 is currently processing or was last SOC converted 4h SOC4 is currently processing or was last SOC converted 5h SOC5 is currently processing or was last SOC converted 6h SOC6 is currently processing or was last SOC converted 7h SOC7 is currently processing or was last SOC converted 8h SOC8 is currently processing or was last SOC converted 9h SOC9 is currently processing or was last SOC converted Ah SOC10 is currently processing or was last SOC converted Bh SOC11 is currently processing or was last SOC converted Ch SOC12 is currently processing or was last SOC converted Dh SOC13 is currently processing or was last SOC converted Eh SOC14 is currently processing or was last SOC converted Fh SOC15 is currently processing or was last SOC converted
7	ADCPWDNZ	RW	0h	ADC Power Down (active low). This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6 - 3	RESERVED	RO		Reserved

Table 3-4. ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INTPULSEPOS	RW	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion (at the end of the acquisition window) plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1 - 0	RESERVED	RO		Reserved

3.1.2 CONTROLSS_ADC0_CFG_ADCCTL2 Register (Offset = 2h) [reset = h]

Short Description: ADC Control 2 Register

Long Description:

Return to Summary Table

Table 3-5. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0002h
CONTROLSS_ADC1_CFG	502C 1002h
CONTROLSS_ADC2_CFG	502C 2002h
CONTROLSS_ADC3_CFG	502C 3002h
CONTROLSS_ADC4_CFG	502C 4002h

Figure 3-2. CONTROLSS_ADC0_CFG_ADCCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
SIGNALMODE	RESOLUTION	RESERVED		PRESCALE			
RW	RW	RO		RW			
0	0	0		0			

Access Types Legend

Table 3-6. ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 8	RESERVED	RO		Reserved
7	SIGNALMODE	RW	0h	SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode. 0 Single-ended 1 Differential
6	RESOLUTION	RW	0h	SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution. 0 12-bit resolution 1 16-bit resolution
5 - 4	RESERVED	RO		Reserved
3 - 0	PRESCALE	RW	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

3.1.3 CONTROLSS_ADC0_CFG_ADCBURSTCTL Register (Offset = 4h) [reset = h]

Short Description: ADC Burst Control Register

Long Description:

Return to Summary Table

Table 3-7. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0004h
CONTROLSS_ADC1_CFG	502C 1004h
CONTROLSS_ADC2_CFG	502C 2004h
CONTROLSS_ADC3_CFG	502C 3004h
CONTROLSS_ADC4_CFG	502C 4004h

Figure 3-3. CONTROLSS_ADC0_CFG_ADCBURSTCTL Name Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED			BURSTSIZE			
RW	RO			RW			
0	0			0			
7	6	5	4	3	2	1	0
RESERVED	BURSTTRIGSEL						
RO	RW						
0	0						

Access Types Legend

Table 3-8. ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	RW	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14 - 12	RESERVED	RO		Reserved
11 - 8	BURSTSIZE	RW	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted
7	RESERVED	RO		Reserved
6 - 0	BURSTTRIGSEL	RW	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. 00h - 7Fh: See AM602 spec. for trigger defintion

3.1.4 CONTROLSS_ADC0_CFG_ADCINTFLG Register (Offset = 6h) [reset = h]

Short Description: ADC Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-9. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0006h
CONTROLSS_ADC1_CFG	502C 1006h
CONTROLSS_ADC2_CFG	502C 2006h
CONTROLSS_ADC3_CFG	502C 3006h
CONTROLSS_ADC4_CFG	502C 4006h

Figure 3-4. CONTROLSS_ADC0_CFG_ADCINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
RO				RO	RO	RO	RO
0				0	0	0	0

Access Types Legend

Table 3-10. ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	ADCINT4	RO	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	RO	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
1	ADCINT2	RO	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

Table 3-10. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	RO	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

3.1.5 CONTROLSS_ADC0_CFG_ADCINTFLGCLR Register (Offset = 8h) [reset = h]

Short Description: ADC Interrupt Flag Clear Register

Long Description:

Return to Summary Table

Table 3-11. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0008h
CONTROLSS_ADC1_CFG	502C 1008h
CONTROLSS_ADC2_CFG	502C 2008h
CONTROLSS_ADC3_CFG	502C 3008h
CONTROLSS_ADC4_CFG	502C 4008h

Figure 3-5. CONTROLSS_ADC0_CFG_ADCINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
RO				RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0				0	0	0	0

Access Types Legend

Table 3-12. ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	ADCINT4	RW RRETURNS 0S	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT4 and ADCINT4RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
2	ADCINT3	RW RRETURNS 0S	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT3 and ADCINT3RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
1	ADCINT2	RW RRETURNS 0S	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT2 and ADCINT2RESULT flags in the ADCINTFLG register. . If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
0	ADCINT1	RW RRETURNS 0S	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT1 and ADCINT1RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set

3.1.6 CONTROLSS_ADC0_CFG_ADCINTOVF Register (Offset = Ah) [reset = h]

Short Description: ADC Interrupt Overflow Register

Long Description:

Return to Summary Table

Table 3-13. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ah
CONTROLSS_ADC1_CFG	502C 100Ah
CONTROLSS_ADC2_CFG	502C 200Ah
CONTROLSS_ADC3_CFG	502C 300Ah
CONTROLSS_ADC4_CFG	502C 400Ah

Figure 3-6. CONTROLSS_ADC0_CFG_ADCINTOVF Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
RO				RO	RO	RO	RO
0				0	0	0	0

Access Types Legend

Table 3-14. ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	ADCINT4	RO	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
2	ADCINT3	RO	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
1	ADCINT2	RO	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
0	ADCINT1	RO	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

3.1.7 CONTROLSS_ADC0_CFG_ADCINTOVFCLR Register (Offset = Ch) [reset = h]

Short Description: ADC Interrupt Overflow Clear Register

Long Description:

Return to Summary Table

Table 3-15. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ch
CONTROLSS_ADC1_CFG	502C 100Ch
CONTROLSS_ADC2_CFG	502C 200Ch
CONTROLSS_ADC3_CFG	502C 300Ch
CONTROLSS_ADC4_CFG	502C 400Ch

Figure 3-7. CONTROLSS_ADC0_CFG_ADCINTOVFCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
RO				RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0				0	0	0	0

Access Types Legend

Table 3-16. ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	ADCINT4	RW RRETURNS 0S	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	RW RRETURNS 0S	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	RW RRETURNS 0S	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	RW RRETURNS 0S	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

3.1.8 CONTROLSS_ADC0_CFG_ADCINTSEL1N2 Register (Offset = Eh) [reset = h]

Short Description: ADC Interrupt 1 and 2 Selection Register

Long Description:

Return to Summary Table

Table 3-17. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Eh
CONTROLSS_ADC1_CFG	502C 100Eh
CONTROLSS_ADC2_CFG	502C 200Eh
CONTROLSS_ADC3_CFG	502C 300Eh
CONTROLSS_ADC4_CFG	502C 400Eh

Figure 3-8. CONTROLSS_ADC0_CFG_ADCINTSEL1N2 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT2CONT	INT2E	RESERVED	INT2SEL			
RO	RW	RW	RO	RW			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT1CONT	INT1E	RESERVED	INT1SEL			
RO	RW	RW	RO	RW			
0	0	0	0	0			

Access Types Legend

Table 3-18. ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT2CONT	RW	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	RW	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12	RESERVED	RO		Reserved
11 - 8	INT2SEL	RW	0h	ADCINT2 EOC Source Select 0h EOC0 is trigger for ADCINT2 1h EOC1 is trigger for ADCINT2 2h EOC2 is trigger for ADCINT2 3h EOC3 is trigger for ADCINT2 4h EOC4 is trigger for ADCINT2 5h EOC5 is trigger for ADCINT2 6h EOC6 is trigger for ADCINT2 7h EOC7 is trigger for ADCINT2 8h EOC8 is trigger for ADCINT2 9h EOC9 is trigger for ADCINT2 Ah EOC10 is trigger for ADCINT2 Bh EOC11 is trigger for ADCINT2 Ch EOC12 is trigger for ADCINT2 Dh EOC13 is trigger for ADCINT2 Eh EOC14 is trigger for ADCINT2 Fh EOC15 is trigger for ADCINT2
7	RESERVED	RO		Reserved
6	INT1CONT	RW	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT1E	RW	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4	RESERVED	RO		Reserved

Table 3-18. ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT1SEL	RW	0h	ADCINT1 EOC Source Select 0h EOC0 is trigger for ADCINT1 1h EOC1 is trigger for ADCINT1 2h EOC2 is trigger for ADCINT1 3h EOC3 is trigger for ADCINT1 4h EOC4 is trigger for ADCINT1 5h EOC5 is trigger for ADCINT1 6h EOC6 is trigger for ADCINT1 7h EOC7 is trigger for ADCINT1 8h EOC8 is trigger for ADCINT1 9h EOC9 is trigger for ADCINT1 Ah EOC10 is trigger for ADCINT1 Bh EOC11 is trigger for ADCINT1 Ch EOC12 is trigger for ADCINT1 Dh EOC13 is trigger for ADCINT1 Eh EOC14 is trigger for ADCINT1 Fh EOC15 is trigger for ADCINT1

3.1.9 CONTROLSS_ADC0_CFG_ADCINTSEL3N4 Register (Offset = 10h) [reset = h]

Short Description: ADC Interrupt 3 and 4 Selection Register

Long Description:

Return to Summary Table

Table 3-19. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0010h
CONTROLSS_ADC1_CFG	502C 1010h
CONTROLSS_ADC2_CFG	502C 2010h
CONTROLSS_ADC3_CFG	502C 3010h
CONTROLSS_ADC4_CFG	502C 4010h

Figure 3-9. CONTROLSS_ADC0_CFG_ADCINTSEL3N4 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT4CONT	INT4E	RESERVED	INT4SEL			
RO	RW	RW	RO	RW			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT3CONT	INT3E	RESERVED	INT3SEL			
RO	RW	RW	RO	RW			
0	0	0	0	0			

Access Types Legend

Table 3-20. ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT4CONT	RW	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	RW	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12	RESERVED	RO		Reserved
11 - 8	INT4SEL	RW	0h	ADCINT4 EOC Source Select 0h EOC0 is trigger for ADCINT4 1h EOC1 is trigger for ADCINT4 2h EOC2 is trigger for ADCINT4 3h EOC3 is trigger for ADCINT4 4h EOC4 is trigger for ADCINT4 5h EOC5 is trigger for ADCINT4 6h EOC6 is trigger for ADCINT4 7h EOC7 is trigger for ADCINT4 8h EOC8 is trigger for ADCINT4 9h EOC9 is trigger for ADCINT4 Ah EOC10 is trigger for ADCINT4 Bh EOC11 is trigger for ADCINT4 Ch EOC12 is trigger for ADCINT4 Dh EOC13 is trigger for ADCINT4 Eh EOC14 is trigger for ADCINT4 Fh EOC15 is trigger for ADCINT4
7	RESERVED	RO		Reserved
6	INT3CONT	RW	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT3E	RW	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4	RESERVED	RO		Reserved

Table 3-20. ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT3SEL	RW	0h	ADCINT3 EOC Source Select 0h EOC0 is trigger for ADCINT3 1h EOC1 is trigger for ADCINT3 2h EOC2 is trigger for ADCINT3 3h EOC3 is trigger for ADCINT3 4h EOC4 is trigger for ADCINT3 5h EOC5 is trigger for ADCINT3 6h EOC6 is trigger for ADCINT3 7h EOC7 is trigger for ADCINT3 8h EOC8 is trigger for ADCINT3 9h EOC9 is trigger for ADCINT3 Ah EOC10 is trigger for ADCINT3 Bh EOC11 is trigger for ADCINT3 Ch EOC12 is trigger for ADCINT3 Dh EOC13 is trigger for ADCINT3 Eh EOC14 is trigger for ADCINT3 Fh EOC15 is trigger for ADCINT3

3.1.10 CONTROLSS_ADC0_CFG_ADCSOCPRICTL Register (Offset = 12h) [reset = h]

Short Description: ADC SOC Priority Control Register

Long Description:

Return to Summary Table

Table 3-21. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0012h
CONTROLSS_ADC1_CFG	502C 1012h
CONTROLSS_ADC2_CFG	502C 2012h
CONTROLSS_ADC3_CFG	502C 3012h
CONTROLSS_ADC4_CFG	502C 4012h

Figure 3-10. CONTROLSS_ADC0_CFG_ADCSOCPRICTL Name Register

15	14	13	12	11	10	9	8
RESERVED						RRPOINTER	
RO						RO	
0						10000	
7	6	5	4	3	2	1	0
RRPOINTER			SOCPRIORITY				
RO			RW				
10000			0				

Access Types Legend

Table 3-22. ADCSOCPRICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 5	RRPOINTER	RO	2710h	Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions. 00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority. 01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority. 02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority. 03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority. 04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority. 05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority. 06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority. 07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority. 08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority. 09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority. 0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority. 0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority. 0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority. 0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority. 0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority. 0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority. 10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the device is reset, when the ADCCTL1.RESET bit is set, or when the ADCSOCPRICTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect. Others Invalid value.

Table 3-22. ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4 - 0	SOCPRIORITY	RW	0h	SOC Priority Determines the cutoff point for priority mode and round robin arbitration for SOCx 00h SOC priority is handled in round robin mode for all channels. 01h SOC0 is high priority, rest of channels are in round robin mode. 02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode. 03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode. 04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode. 05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode. 06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode. 07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode. 08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode. 09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode. 0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode. 0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode. 0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode. 0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode. 0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode. 0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode. 10h All SOCs are in high priority mode, arbitrated by SOC number. Others Invalid selection.

3.1.11 CONTROLSS_ADC0_CFG_ADCINTSOCSEL1 Register (Offset = 14h) [reset = h]

Short Description: ADC Interrupt SOC Selection 1 Register

Long Description:

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Table 3-23. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0014h
CONTROLSS_ADC1_CFG	502C 1014h
CONTROLSS_ADC2_CFG	502C 2014h
CONTROLSS_ADC3_CFG	502C 3014h
CONTROLSS_ADC4_CFG	502C 4014h

Figure 3-11. CONTROLSS_ADC0_CFG_ADCINTSOCSEL1 Name Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
RW		RW		RW		RW	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC3		SOC2		SOC1		SOC0	
RW		RW		RW		RW	
0		0		0		0	

Access Types Legend

Table 3-24. ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC7	RW	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC7. 10 ADCINT2 will trigger SOC7. 11 Invalid selection.
13 - 12	SOC6	RW	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC6. 10 ADCINT2 will trigger SOC6. 11 Invalid selection.
11 - 10	SOC5	RW	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC5. 10 ADCINT2 will trigger SOC5. 11 Invalid selection.
9 - 8	SOC4	RW	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC4. 10 ADCINT2 will trigger SOC4. 11 Invalid selection.
7 - 6	SOC3	RW	0h	SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC3. 10 ADCINT2 will trigger SOC3. 11 Invalid selection.

Table 3-24. ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 4	SOC2	RW	0h	SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC2. 10 ADCINT2 will trigger SOC2. 11 Invalid selection.
3 - 2	SOC1	RW	0h	SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC1. 10 ADCINT2 will trigger SOC1. 11 Invalid selection.
1 - 0	SOC0	RW	0h	SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC0. 10 ADCINT2 will trigger SOC0. 11 Invalid selection.

3.1.12 CONTROLSS_ADC0_CFG_ADCINTSOCSEL2 Register (Offset = 16h) [reset = h]

Short Description: ADC Interrupt SOC Selection 2 Register

Long Description:

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Table 3-25. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0016h
CONTROLSS_ADC1_CFG	502C 1016h
CONTROLSS_ADC2_CFG	502C 2016h
CONTROLSS_ADC3_CFG	502C 3016h
CONTROLSS_ADC4_CFG	502C 4016h

Figure 3-12. CONTROLSS_ADC0_CFG_ADCINTSOCSEL2 Name Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
RW		RW		RW		RW	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
RW		RW		RW		RW	
0		0		0		0	

Access Types Legend

Table 3-26. ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC15	RW	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC15. 10 ADCINT2 will trigger SOC15. 11 Invalid selection.
13 - 12	SOC14	RW	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC14. 10 ADCINT2 will trigger SOC14. 11 Invalid selection.
11 - 10	SOC13	RW	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC13. 10 ADCINT2 will trigger SOC13. 11 Invalid selection.
9 - 8	SOC12	RW	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC12. 10 ADCINT2 will trigger SOC12. 11 Invalid selection.
7 - 6	SOC11	RW	0h	SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC11. 10 ADCINT2 will trigger SOC11. 11 Invalid selection.

Table 3-26. ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 4	SOC10	RW	0h	SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC10. 10 ADCINT2 will trigger SOC10. 11 Invalid selection.
3 - 2	SOC9	RW	0h	SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC9. 10 ADCINT2 will trigger SOC9. 11 Invalid selection.
1 - 0	SOC8	RW	0h	SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC8. 10 ADCINT2 will trigger SOC8. 11 Invalid selection.

3.1.13 CONTROLSS_ADC0_CFG_ADCSOCFLG1 Register (Offset = 18h) [reset = h]

Short Description: ADC SOC Flag 1 Register

Long Description:

Return to Summary Table

Table 3-27. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0018h
CONTROLSS_ADC1_CFG	502C 1018h
CONTROLSS_ADC2_CFG	502C 2018h
CONTROLSS_ADC3_CFG	502C 3018h
CONTROLSS_ADC4_CFG	502C 4018h

Figure 3-13. CONTROLSS_ADC0_CFG_ADCSOCFLG1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-28. ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	RO	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	RO	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	RO	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	RO	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
11	SOC11	RO	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	RO	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	RO	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	RO	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
7	SOC7	RO	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
6	SOC6	RO	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOC5	RO	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	RO	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	RO	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
2	SOC2	RO	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
1	SOC1	RO	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	RO	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

3.1.14 CONTROLSS_ADC0_CFG_ADCSOCFRC1 Register (Offset = 1Ah) [reset = h]

Short Description: ADC SOC Force 1 Register

Long Description:

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Table 3-29. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ah
CONTROLSS_ADC1_CFG	502C 101Ah
CONTROLSS_ADC2_CFG	502C 201Ah
CONTROLSS_ADC3_CFG	502C 301Ah
CONTROLSS_ADC4_CFG	502C 401Ah

Figure 3-14. CONTROLSS_ADC0_CFG_ADCSOCFRC1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-30. ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	RW RRETURNS0S	0h	SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
14	SOC14	RW RRETURNS0S	0h	SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	RW RRETURNS 0S	0h	SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
12	SOC12	RW RRETURNS 0S	0h	SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
11	SOC11	RW RRETURNS 0S	0h	SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
10	SOC10	RW RRETURNS 0S	0h	SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
9	SOC9	RW RRETURNS 0S	0h	SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	RW RRETURNS 0S	0h	SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
7	SOC7	RW RRETURNS 0S	0h	SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
6	SOC6	RW RRETURNS 0S	0h	SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
5	SOC5	RW RRETURNS 0S	0h	SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
4	SOC4	RW RRETURNS 0S	0h	SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	RW RRETURNS 0S	0h	SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
2	SOC2	RW RRETURNS 0S	0h	SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
1	SOC1	RW RRETURNS 0S	0h	SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
0	SOC0	RW RRETURNS 0S	0h	SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

3.1.15 CONTROLSS_ADC0_CFG_ADCSOCOVF1 Register (Offset = 1Ch) [reset = h]

Short Description: ADC SOC Overflow 1 Register

Long Description:

Return to Summary Table

Table 3-31. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ch
CONTROLSS_ADC1_CFG	502C 101Ch
CONTROLSS_ADC2_CFG	502C 201Ch
CONTROLSS_ADC3_CFG	502C 301Ch
CONTROLSS_ADC4_CFG	502C 401Ch

Figure 3-15. CONTROLSS_ADC0_CFG_ADCSOCOVF1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-32. ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	RO	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
14	SOC14	RO	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
13	SOC13	RO	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
12	SOC12	RO	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	RO	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
10	SOC10	RO	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
9	SOC9	RO	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
8	SOC8	RO	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
7	SOC7	RO	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
6	SOC6	RO	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
5	SOC5	RO	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
4	SOC4	RO	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
3	SOC3	RO	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
2	SOC2	RO	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOC1	RO	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
0	SOC0	RO	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

3.1.16 CONTROLSS_ADC0_CFG_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = h]

Short Description: ADC SOC Overflow Clear 1 Register

Long Description:

Return to Summary Table

Table 3-33. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Eh
CONTROLSS_ADC1_CFG	502C 101Eh
CONTROLSS_ADC2_CFG	502C 201Eh
CONTROLSS_ADC3_CFG	502C 301Eh
CONTROLSS_ADC4_CFG	502C 401Eh

Figure 3-16. CONTROLSS_ADC0_CFG_ADCSOCOVFCLR1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	RW RRETURNS 0S	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	RW RRETURNS 0S	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	RW RRETURNS 0S	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	RW RRETURNS 0S	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	RW RRETURNS 0S	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
10	SOC10	RW RRETURNS 0S	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
9	SOC9	RW RRETURNS 0S	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
8	SOC8	RW RRETURNS 0S	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
7	SOC7	RW RRETURNS 0S	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
6	SOC6	RW RRETURNS 0S	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
5	SOC5	RW RRETURNS 0S	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
4	SOC4	RW RRETURNS 0S	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
3	SOC3	RW RRETURNS 0S	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SOC2	RW RRETURNS 0S	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
1	SOC1	RW RRETURNS 0S	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
0	SOC0	RW RRETURNS 0S	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

3.1.17 CONTROLSS_ADC0_CFG_ADCSOC0CTL Register (Offset = 20h) [reset = h]

Short Description: ADC SOC0 Control Register

Long Description:

Return to Summary Table

Table 3-35. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0020h
CONTROLSS_ADC1_CFG	502C 1020h
CONTROLSS_ADC2_CFG	502C 2020h
CONTROLSS_ADC3_CFG	502C 3020h
CONTROLSS_ADC4_CFG	502C 4020h

Figure 3-17. CONTROLSS_ADC0_CFG_ADCSOC0CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-36. ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.18 CONTROLSS_ADC0_CFG_ADCSOC1CTL Register (Offset = 24h) [reset = h]

Short Description: ADC SOC1 Control Register

Long Description:

Return to Summary Table

Table 3-37. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0024h
CONTROLSS_ADC1_CFG	502C 1024h
CONTROLSS_ADC2_CFG	502C 2024h
CONTROLSS_ADC3_CFG	502C 3024h
CONTROLSS_ADC4_CFG	502C 4024h

Figure 3-18. CONTROLSS_ADC0_CFG_ADCSOC1CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-38. ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.19 CONTROLSS_ADC0_CFG_ADCSOC2CTL Register (Offset = 28h) [reset = h]

Short Description: ADC SOC2 Control Register

Long Description:

Return to Summary Table

Table 3-39. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0028h
CONTROLSS_ADC1_CFG	502C 1028h
CONTROLSS_ADC2_CFG	502C 2028h
CONTROLSS_ADC3_CFG	502C 3028h
CONTROLSS_ADC4_CFG	502C 4028h

Figure 3-19. CONTROLSS_ADC0_CFG_ADCSOC2CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-40. ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.20 CONTROLSS_ADC0_CFG_ADCSOC3CTL Register (Offset = 2Ch) [reset = h]

Short Description: ADC SOC3 Control Register

Long Description:

Return to Summary Table

Table 3-41. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 002Ch
CONTROLSS_ADC1_CFG	502C 102Ch
CONTROLSS_ADC2_CFG	502C 202Ch
CONTROLSS_ADC3_CFG	502C 302Ch
CONTROLSS_ADC4_CFG	502C 402Ch

Figure 3-20. CONTROLSS_ADC0_CFG_ADCSOC3CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-42. ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.21 CONTROLSS_ADC0_CFG_ADCSOC4CTL Register (Offset = 30h) [reset = h]

Short Description: ADC SOC4 Control Register

Long Description:

Return to Summary Table

Table 3-43. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0030h
CONTROLSS_ADC1_CFG	502C 1030h
CONTROLSS_ADC2_CFG	502C 2030h
CONTROLSS_ADC3_CFG	502C 3030h
CONTROLSS_ADC4_CFG	502C 4030h

Figure 3-21. CONTROLSS_ADC0_CFG_ADCSOC4CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-44. ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.22 CONTROLSS_ADC0_CFG_ADCSOC5CTL Register (Offset = 34h) [reset = h]

Short Description: ADC SOC5 Control Register

Long Description:

Return to Summary Table

Table 3-45. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0034h
CONTROLSS_ADC1_CFG	502C 1034h
CONTROLSS_ADC2_CFG	502C 2034h
CONTROLSS_ADC3_CFG	502C 3034h
CONTROLSS_ADC4_CFG	502C 4034h

Figure 3-22. CONTROLSS_ADC0_CFG_ADCSOC5CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-46. ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.23 CONTROLSS_ADC0_CFG_ADCSOC6CTL Register (Offset = 38h) [reset = h]

Short Description: ADC SOC6 Control Register

Long Description:

Return to Summary Table

Table 3-47. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0038h
CONTROLSS_ADC1_CFG	502C 1038h
CONTROLSS_ADC2_CFG	502C 2038h
CONTROLSS_ADC3_CFG	502C 3038h
CONTROLSS_ADC4_CFG	502C 4038h

Figure 3-23. CONTROLSS_ADC0_CFG_ADCSOC6CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-48. ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.24 CONTROLSS_ADC0_CFG_ADCSOC7CTL Register (Offset = 3Ch) [reset = h]

Short Description: ADC SOC7 Control Register

Long Description:

Return to Summary Table

Table 3-49. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 003Ch
CONTROLSS_ADC1_CFG	502C 103Ch
CONTROLSS_ADC2_CFG	502C 203Ch
CONTROLSS_ADC3_CFG	502C 303Ch
CONTROLSS_ADC4_CFG	502C 403Ch

Figure 3-24. CONTROLSS_ADC0_CFG_ADCSOC7CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-50. ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.25 CONTROLSS_ADC0_CFG_ADCSOC8CTL Register (Offset = 40h) [reset = h]

Short Description: ADC SOC8 Control Register

Long Description:

Return to Summary Table

Table 3-51. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0040h
CONTROLSS_ADC1_CFG	502C 1040h
CONTROLSS_ADC2_CFG	502C 2040h
CONTROLSS_ADC3_CFG	502C 3040h
CONTROLSS_ADC4_CFG	502C 4040h

Figure 3-25. CONTROLSS_ADC0_CFG_ADCSOC8CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-52. ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.26 CONTROLSS_ADC0_CFG_ADCSOC9CTL Register (Offset = 44h) [reset = h]

Short Description: ADC SOC9 Control Register

Long Description:

Return to Summary Table

Table 3-53. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0044h
CONTROLSS_ADC1_CFG	502C 1044h
CONTROLSS_ADC2_CFG	502C 2044h
CONTROLSS_ADC3_CFG	502C 3044h
CONTROLSS_ADC4_CFG	502C 4044h

Figure 3-26. CONTROLSS_ADC0_CFG_ADCSOC9CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-54. ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.27 CONTROLSS_ADC0_CFG_ADCSOC10CTL Register (Offset = 48h) [reset = h]

Short Description: ADC SOC10 Control Register

Long Description:

Return to Summary Table

Table 3-55. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0048h
CONTROLSS_ADC1_CFG	502C 1048h
CONTROLSS_ADC2_CFG	502C 2048h
CONTROLSS_ADC3_CFG	502C 3048h
CONTROLSS_ADC4_CFG	502C 4048h

Figure 3-27. CONTROLSS_ADC0_CFG_ADCSOC10CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-56. ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.28 CONTROLSS_ADC0_CFG_ADCSOC11CTL Register (Offset = 4Ch) [reset = h]

Short Description: ADC SOC11 Control Register

Long Description:

Return to Summary Table

Table 3-57. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 004Ch
CONTROLSS_ADC1_CFG	502C 104Ch
CONTROLSS_ADC2_CFG	502C 204Ch
CONTROLSS_ADC3_CFG	502C 304Ch
CONTROLSS_ADC4_CFG	502C 404Ch

Figure 3-28. CONTROLSS_ADC0_CFG_ADCSOC11CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-58. ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.29 CONTROLSS_ADC0_CFG_ADCSOC12CTL Register (Offset = 50h) [reset = h]

Short Description: ADC SOC12 Control Register

Long Description:

Return to Summary Table

Table 3-59. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0050h
CONTROLSS_ADC1_CFG	502C 1050h
CONTROLSS_ADC2_CFG	502C 2050h
CONTROLSS_ADC3_CFG	502C 3050h
CONTROLSS_ADC4_CFG	502C 4050h

Figure 3-29. CONTROLSS_ADC0_CFG_ADCSOC12CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-60. ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.30 CONTROLSS_ADC0_CFG_ADCSOC13CTL Register (Offset = 54h) [reset = h]

Short Description: ADC SOC13 Control Register

Long Description:

Return to Summary Table

Table 3-61. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0054h
CONTROLSS_ADC1_CFG	502C 1054h
CONTROLSS_ADC2_CFG	502C 2054h
CONTROLSS_ADC3_CFG	502C 3054h
CONTROLSS_ADC4_CFG	502C 4054h

Figure 3-30. CONTROLSS_ADC0_CFG_ADCSOC13CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-62. ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.31 CONTROLSS_ADC0_CFG_ADCSOC14CTL Register (Offset = 58h) [reset = h]

Short Description: ADC SOC14 Control Register

Long Description:

Return to Summary Table

Table 3-63. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0058h
CONTROLSS_ADC1_CFG	502C 1058h
CONTROLSS_ADC2_CFG	502C 2058h
CONTROLSS_ADC3_CFG	502C 3058h
CONTROLSS_ADC4_CFG	502C 4058h

Figure 3-31. CONTROLSS_ADC0_CFG_ADCSOC14CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-64. ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.32 CONTROLSS_ADC0_CFG_ADCSOC15CTL Register (Offset = 5Ch) [reset = h]

Short Description: ADC SOC15 Control Register

Long Description:

Return to Summary Table

Table 3-65. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 005Ch
CONTROLSS_ADC1_CFG	502C 105Ch
CONTROLSS_ADC2_CFG	502C 205Ch
CONTROLSS_ADC3_CFG	502C 305Ch
CONTROLSS_ADC4_CFG	502C 405Ch

Figure 3-32. CONTROLSS_ADC0_CFG_ADCSOC15CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
RO					RW							RW			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
RW	RO							RW							
0	0							0							

Access Types Legend

Table 3-66. ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	RO		Reserved
26 - 20	TRIGSEL	RW	0h	SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	RW	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	RO		Reserved
8 - 0	ACQPS	RW	0h	SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

3.1.33 CONTROLSS_ADC0_CFG_ADCEVTSTAT Register (Offset = 60h) [reset = h]

Short Description: ADC Event Status Register

Long Description:

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Table 3-67. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0060h
CONTROLSS_ADC1_CFG	502C 1060h
CONTROLSS_ADC2_CFG	502C 2060h
CONTROLSS_ADC3_CFG	502C 3060h
CONTROLSS_ADC4_CFG	502C 4060h

Figure 3-33. CONTROLSS_ADC0_CFG_ADCEVTSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-68. ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	PPB4ZERO	RO	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal.
13	PPB4TRIPLO	RO	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
12	PPB4TRIPHI	RO	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred.
11	RESERVED	RO		Reserved
10	PPB3ZERO	RO	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal.
9	PPB3TRIPLO	RO	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
8	PPB3TRIPHI	RO	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred.
7	RESERVED	RO		Reserved
6	PPB2ZERO	RO	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal.
5	PPB2TRIPLO	RO	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
4	PPB2TRIPHI	RO	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred.
3	RESERVED	RO		Reserved

Table 3-68. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PPB1ZERO	RO	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal.
1	PPB1TRIPLO	RO	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
0	PPB1TRIPHI	RO	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred.

3.1.34 CONTROLSS_ADC0_CFG_ADCEVTCLR Register (Offset = 64h) [reset = h]

Short Description: ADC Event Clear Register

Long Description:

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Table 3-69. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0064h
CONTROLSS_ADC1_CFG	502C 1064h
CONTROLSS_ADC2_CFG	502C 2064h
CONTROLSS_ADC3_CFG	502C 3064h
CONTROLSS_ADC4_CFG	502C 4064h

Figure 3-34. CONTROLSS_ADC0_CFG_ADCEVTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
RO	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RO	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
RO	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RO	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-70. ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	PPB4ZERO	RW RRETURNS 0S	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
13	PPB4TRIPLO	RW RRETURNS 0S	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
12	PPB4TRIPHI	RW RRETURNS 0S	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
11	RESERVED	RO		Reserved
10	PPB3ZERO	RW RRETURNS 0S	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
9	PPB3TRIPLO	RW RRETURNS 0S	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
8	PPB3TRIPHI	RW RRETURNS 0S	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
7	RESERVED	RO		Reserved
6	PPB2ZERO	RW RRETURNS 0S	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.

Table 3-70. ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PPB2TRIPLO	RW RRETURNS 0S	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
4	PPB2TRIPHI	RW RRETURNS 0S	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
3	RESERVED	RO		Reserved
2	PPB1ZERO	RW RRETURNS 0S	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
1	PPB1TRIPLO	RW RRETURNS 0S	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
0	PPB1TRIPHI	RW RRETURNS 0S	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.

3.1.35 CONTROLSS_ADC0_CFG_ADCEVTSEL Register (Offset = 68h) [reset = h]

Short Description: ADC Event Selection Register

Long Description:

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Table 3-71. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0068h
CONTROLSS_ADC1_CFG	502C 1068h
CONTROLSS_ADC2_CFG	502C 2068h
CONTROLSS_ADC3_CFG	502C 3068h
CONTROLSS_ADC4_CFG	502C 4068h

Figure 3-35. CONTROLSS_ADC0_CFG_ADCEVTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
RO	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
RO	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-72. ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	PPB4ZERO	RW	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	RW	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	RW	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED	RO		Reserved
10	PPB3ZERO	RW	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	RW	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	RW	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
7	RESERVED	RO		Reserved

Table 3-72. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PPB2ZERO	RW	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
5	PPB2TRIPLO	RW	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	RW	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED	RO		Reserved
2	PPB1ZERO	RW	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	RW	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	RW	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

3.1.36 CONTROLSS_ADC0_CFG_ADCEVTINTSEL Register (Offset = 6Ch) [reset = h]

Short Description: ADC Event Interrupt Selection Register

Long Description:

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Table 3-73. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 006Ch
CONTROLSS_ADC1_CFG	502C 106Ch
CONTROLSS_ADC2_CFG	502C 206Ch
CONTROLSS_ADC3_CFG	502C 306Ch
CONTROLSS_ADC4_CFG	502C 406Ch

Figure 3-36. CONTROLSS_ADC0_CFG_ADCEVTINTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
RO	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
RO	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-74. ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	PPB4ZERO	RW	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	RW	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	RW	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED	RO		Reserved
10	PPB3ZERO	RW	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	RW	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	RW	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
7	RESERVED	RO		Reserved

Table 3-74. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PPB2ZERO	RW	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
5	PPB2TRIPLO	RW	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	RW	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED	RO		Reserved
2	PPB1ZERO	RW	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	RW	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	RW	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

3.1.37 CONTROLSS_ADC0_CFG_ADCOSDETECT Register (Offset = 70h) [reset = h]

Short Description: ADC Open and Shorts Detect Register

Long Description:

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Table 3-75. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0070h
CONTROLSS_ADC1_CFG	502C 1070h
CONTROLSS_ADC2_CFG	502C 2070h
CONTROLSS_ADC3_CFG	502C 3070h
CONTROLSS_ADC4_CFG	502C 4070h

Figure 3-37. CONTROLSS_ADC0_CFG_ADCOSDETECT Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED						DETECTCFG	
RO						RW	
0						0	

Access Types Legend

Table 3-76. ADCOSDETECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	RO		Reserved
2 - 0	DETECTCFG	RW	0h	ADC Opens and Shorts Detect Configuration. This bit field defines the open/shorts detection circuit state. 0h Open/Shorts detection circuit is disabled. 1h Open/Shorts detection circuit is enabled at zero scale. 2h Open/Shorts detection circuit is enabled at full scale. 3h Open/Shorts detection circuit is enabled at (nominal) 5/12 scale. 4h Open/Shorts detection circuit is enabled at (nominal) 7/12 scale. 5h Open/Shorts detection circuit is enabled with a (nominal) 5K pulldown to VSSA. 6h Open/Shorts detection circuit is enabled with a (nominal) 5K pullup to VDDA. 7h Open/Shorts detection circuit is enabled with a (nominal) 7K pulldown to VSSA.

3.1.38 CONTROLSS_ADC0_CFG_ADCCOUNTER Register (Offset = 72h) [reset = h]

Short Description: ADC Counter Register

Long Description:

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Table 3-77. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0072h
CONTROLSS_ADC1_CFG	502C 1072h
CONTROLSS_ADC2_CFG	502C 2072h
CONTROLSS_ADC3_CFG	502C 3072h
CONTROLSS_ADC4_CFG	502C 4072h

Figure 3-38. CONTROLSS_ADC0_CFG_ADCCOUNTER Name Register

15	14	13	12	11	10	9	8
RESERVED				FREECOUNT			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
FREECOUNT							
RO							
0							

Access Types Legend

Table 3-78. ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	FREECOUNT	RO	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

3.1.39 CONTROLSS_ADC0_CFG_ADCREV Register (Offset = 74h) [reset = h]

Short Description: ADC Revision Register

Long Description:

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Table 3-79. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0074h
CONTROLSS_ADC1_CFG	502C 1074h
CONTROLSS_ADC2_CFG	502C 2074h
CONTROLSS_ADC3_CFG	502C 3074h
CONTROLSS_ADC4_CFG	502C 4074h

Figure 3-39. CONTROLSS_ADC0_CFG_ADCREV Name Register

15	14	13	12	11	10	9	8
REV							
RO							
1							
7	6	5	4	3	2	1	0
TYPE							
RO							
101							

Access Types Legend

Table 3-80. ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	REV	RO	1h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h.
7 - 0	TYPE	RO	65h	ADC Type. Always set to 5 for this ADC.

3.1.40 CONTROLSS_ADC0_CFG_ADCOFFTRIM Register (Offset = 76h) [reset = h]

Short Description: ADC Offset Trim Register

Long Description:

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Table 3-81. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0076h
CONTROLSS_ADC1_CFG	502C 1076h
CONTROLSS_ADC2_CFG	502C 2076h
CONTROLSS_ADC3_CFG	502C 3076h
CONTROLSS_ADC4_CFG	502C 4076h

Figure 3-40. CONTROLSS_ADC0_CFG_ADCOFFTRIM Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
OFFTRIM							
RW							
0							

Access Types Legend

Table 3-82. ADCOFFTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7 - 0	OFFTRIM	RW	0h	ADC Offset Trim Adjusts the conversion results of the converter up or down to account for offset error in the ADC. A factory trim setting will be loaded during device boot. Offset can be corrected in the range of +7 to -8 LSBs. Value is 16*Offset in 8-bit 2's complement: 7 LSB (16*7) = 112 6 LSB (16*6) = 96 5 LSB (16*5) = 80 4 LSB (16*4) = 64 3 LSB (16*3) = 48 2 LSB (16*2) = 32 1 LSB (16*1) = 16 0 LSB (16*0) = 0 -1 LSB (16*(-1)) = 240 : : -7LSB(16*(-7)) = 144

3.1.41 CONTROLSS_ADC0_CFG_ADCCONFIG Register (Offset = 7Ch) [reset = h]

Short Description: ADC Config Register

Long Description:

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Table 3-83. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 007Ch
CONTROLSS_ADC1_CFG	502C 107Ch
CONTROLSS_ADC2_CFG	502C 207Ch
CONTROLSS_ADC3_CFG	502C 307Ch
CONTROLSS_ADC4_CFG	502C 407Ch

Figure 3-41. CONTROLSS_ADC0_CFG_ADCCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CONFIG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG															
RW															
0															

Access Types Legend

Table 3-84. ADCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CONFIG	RW	0h	ADC Configuration. This bit field is used for TI internal testing/ debugging.

3.1.42 CONTROLSS_ADC0_CFG_ADCPPB1CONFIG Register (Offset = 80h) [reset = h]

Short Description: ADC PPB1 Config Register

Long Description:

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Table 3-85. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0080h
CONTROLSS_ADC1_CFG	502C 1080h
CONTROLSS_ADC2_CFG	502C 2080h
CONTROLSS_ADC3_CFG	502C 3080h
CONTROLSS_ADC4_CFG	502C 4080h

Figure 3-42. CONTROLSS_ADC0_CFG_ADCPPB1CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
RO		RW	RW	RW			
0		0	0	0			

Access Types Legend

Table 3-86. ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	RO		Reserved
5	CBCEN	RW	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	RW	0h	ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register. 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx

Table 3-86. ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	RW	0h	ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 1 0001 SOC1/EOC1/RESULT1 is associated with post processing block 1 0010 SOC2/EOC2/RESULT2 is associated with post processing block 1 0011 SOC3/EOC3/RESULT3 is associated with post processing block 1 0100 SOC4/EOC4/RESULT4 is associated with post processing block 1 0101 SOC5/EOC5/RESULT5 is associated with post processing block 1 0110 SOC6/EOC6/RESULT6 is associated with post processing block 1 0111 SOC7/EOC7/RESULT7 is associated with post processing block 1 1000 SOC8/EOC8/RESULT8 is associated with post processing block 1 1001 SOC9/EOC9/RESULT9 is associated with post processing block 1 1010 SOC10/EOC10/RESULT10 is associated with post processing block 1 1011 SOC11/EOC11/RESULT11 is associated with post processing block 1 1100 SOC12/EOC12/RESULT12 is associated with post processing block 1 1101 SOC13/EOC13/RESULT13 is associated with post processing block 1 1110 SOC14/EOC14/RESULT14 is associated with post processing block 1 1111 SOC15/EOC15/RESULT15 is associated with post processing block 1

3.1.43 CONTROLSS_ADC0_CFG_ADCPPB1STAMP Register (Offset = 82h) [reset = h]

Short Description: ADC PPB1 Sample Delay Time Stamp Register

Long Description:

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Table 3-87. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0082h
CONTROLSS_ADC1_CFG	502C 1082h
CONTROLSS_ADC2_CFG	502C 2082h
CONTROLSS_ADC3_CFG	502C 3082h
CONTROLSS_ADC4_CFG	502C 4082h

Figure 3-43. CONTROLSS_ADC0_CFG_ADCPPB1STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
RO							
0							

Access Types Legend

Table 3-88. ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DLYSTAMP	RO	0h	ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.1.44 CONTROLSS_ADC0_CFG_ADCPPB1OFFCAL Register (Offset = 84h) [reset = h]

Short Description: ADC PPB1 Offset Calibration Register

Long Description:

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Table 3-89. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0084h
CONTROLSS_ADC1_CFG	502C 1084h
CONTROLSS_ADC2_CFG	502C 2084h
CONTROLSS_ADC3_CFG	502C 3084h
CONTROLSS_ADC4_CFG	502C 4084h

Figure 3-44. CONTROLSS_ADC0_CFG_ADCPPB1OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
RW							
0							

Access Types Legend

Table 3-90. ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	OFFCAL	RW	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.1.45 CONTROLSS_ADC0_CFG_ADCPPB1OFFREF Register (Offset = 86h) [reset = h]

Short Description: ADC PPB1 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-91. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0086h
CONTROLSS_ADC1_CFG	502C 1086h
CONTROLSS_ADC2_CFG	502C 2086h
CONTROLSS_ADC3_CFG	502C 3086h
CONTROLSS_ADC4_CFG	502C 4086h

Figure 3-45. CONTROLSS_ADC0_CFG_ADCPPB1OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
RW							
0							
7	6	5	4	3	2	1	0
OFFREF							
RW							
0							

Access Types Legend

Table 3-92. ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	RW	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.1.46 CONTROLSS_ADC0_CFG_ADCPPB1TRIPHI Register (Offset = 88h) [reset = h]

Short Description: ADC PPB1 Trip High Register

Long Description:

Return to Summary Table

Table 3-93. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0088h
CONTROLSS_ADC1_CFG	502C 1088h
CONTROLSS_ADC2_CFG	502C 2088h
CONTROLSS_ADC3_CFG	502C 3088h
CONTROLSS_ADC4_CFG	502C 4088h

Figure 3-46. CONTROLSS_ADC0_CFG_ADCPPB1TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
RO															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
RW															
0															

Access Types Legend

Table 3-94. ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	RO		Reserved
16	HSIGN	RW	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	RW	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB1RESULT register.

3.1.47 CONTROLSS_ADC0_CFG_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = h]

Short Description: ADC PPB1 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-95. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 008Ch
CONTROLSS_ADC1_CFG	502C 108Ch
CONTROLSS_ADC2_CFG	502C 208Ch
CONTROLSS_ADC3_CFG	502C 308Ch
CONTROLSS_ADC4_CFG	502C 408Ch

Figure 3-47. CONTROLSS_ADC0_CFG_ADCPPB1TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
RO												RO			RW
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
RW															
0															

Access Types Legend

Table 3-96. ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	RO	0h	ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	RO		Reserved
16	LSIGN	RW	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	RW	0h	ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB1RESULT register.

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3.1.48 CONTROLSS_ADC0_CFG_ADCPPB2CONFIG Register (Offset = 90h) [reset = h]

Short Description: ADC PPB2 Config Register

Long Description:

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Table 3-97. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0090h
CONTROLSS_ADC1_CFG	502C 1090h
CONTROLSS_ADC2_CFG	502C 2090h
CONTROLSS_ADC3_CFG	502C 3090h
CONTROLSS_ADC4_CFG	502C 4090h

Figure 3-48. CONTROLSS_ADC0_CFG_ADCPPB2CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
RO		RW	RW	RW			
0		0	0	0			

Access Types Legend

Table 3-98. ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	RO		Reserved
5	CBCEN	RW	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	RW	0h	ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register. 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx

Table 3-98. ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	RW	0h	ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 2 0001 SOC1/EOC1/RESULT1 is associated with post processing block 2 0010 SOC2/EOC2/RESULT2 is associated with post processing block 2 0011 SOC3/EOC3/RESULT3 is associated with post processing block 2 0100 SOC4/EOC4/RESULT4 is associated with post processing block 2 0101 SOC5/EOC5/RESULT5 is associated with post processing block 2 0110 SOC6/EOC6/RESULT6 is associated with post processing block 2 0111 SOC7/EOC7/RESULT7 is associated with post processing block 2 1000 SOC8/EOC8/RESULT8 is associated with post processing block 2 1001 SOC9/EOC9/RESULT9 is associated with post processing block 2 1010 SOC10/EOC10/RESULT10 is associated with post processing block 2 1011 SOC11/EOC11/RESULT11 is associated with post processing block 2 1100 SOC12/EOC12/RESULT12 is associated with post processing block 2 1101 SOC13/EOC13/RESULT13 is associated with post processing block 2 1110 SOC14/EOC14/RESULT14 is associated with post processing block 2 1111 SOC15/EOC15/RESULT15 is associated with post processing block 2

3.1.49 CONTROLSS_ADC0_CFG_ADCPPB2STAMP Register (Offset = 92h) [reset = h]

Short Description: ADC PPB2 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-99. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0092h
CONTROLSS_ADC1_CFG	502C 1092h
CONTROLSS_ADC2_CFG	502C 2092h
CONTROLSS_ADC3_CFG	502C 3092h
CONTROLSS_ADC4_CFG	502C 4092h

Figure 3-49. CONTROLSS_ADC0_CFG_ADCPPB2STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
RO							
0							

Access Types Legend

Table 3-100. ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DLYSTAMP	RO	0h	ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.1.50 CONTROLSS_ADC0_CFG_ADCPPB2OFFCAL Register (Offset = 94h) [reset = h]

Short Description: ADC PPB2 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-101. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0094h
CONTROLSS_ADC1_CFG	502C 1094h
CONTROLSS_ADC2_CFG	502C 2094h
CONTROLSS_ADC3_CFG	502C 3094h
CONTROLSS_ADC4_CFG	502C 4094h

Figure 3-50. CONTROLSS_ADC0_CFG_ADCPPB2OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
RW							
0							

Access Types Legend

Table 3-102. ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	OFFCAL	RW	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.1.51 CONTROLSS_ADC0_CFG_ADCPPB2OFFREF Register (Offset = 96h) [reset = h]

Short Description: ADC PPB2 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-103. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0096h
CONTROLSS_ADC1_CFG	502C 1096h
CONTROLSS_ADC2_CFG	502C 2096h
CONTROLSS_ADC3_CFG	502C 3096h
CONTROLSS_ADC4_CFG	502C 4096h

Figure 3-51. CONTROLSS_ADC0_CFG_ADCPPB2OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
RW							
0							
7	6	5	4	3	2	1	0
OFFREF							
RW							
0							

Access Types Legend

Table 3-104. ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	RW	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.1.52 CONTROLSS_ADC0_CFG_ADCPPB2TRIPHI Register (Offset = 98h) [reset = h]

Short Description: ADC PPB2 Trip High Register

Long Description:

Return to Summary Table

Table 3-105. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0098h
CONTROLSS_ADC1_CFG	502C 1098h
CONTROLSS_ADC2_CFG	502C 2098h
CONTROLSS_ADC3_CFG	502C 3098h
CONTROLSS_ADC4_CFG	502C 4098h

Figure 3-52. CONTROLSS_ADC0_CFG_ADCPPB2TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
RO															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
RW															
0															

Access Types Legend

Table 3-106. ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	RO		Reserved
16	HSIGN	RW	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	RW	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB2RESULT register.

3.1.53 CONTROLSS_ADC0_CFG_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = h]

Short Description: ADC PPB2 Trip Low/Trigger Time Stamp Register

Long Description:

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Table 3-107. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 009Ch
CONTROLSS_ADC1_CFG	502C 109Ch
CONTROLSS_ADC2_CFG	502C 209Ch
CONTROLSS_ADC3_CFG	502C 309Ch
CONTROLSS_ADC4_CFG	502C 409Ch

Figure 3-53. CONTROLSS_ADC0_CFG_ADCPPB2TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
RO												RO			RW
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
RW															
0															

Access Types Legend

Table 3-108. ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	RO	0h	ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	RO		Reserved
16	LSIGN	RW	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	RW	0h	ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB2RESULT register.

3.1.54 CONTROLSS_ADC0_CFG_ADCPPB3CONFIG Register (Offset = A0h) [reset = h]

Short Description: ADC PPB3 Config Register

Long Description:

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Table 3-109. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A0h
CONTROLSS_ADC1_CFG	502C 10A0h
CONTROLSS_ADC2_CFG	502C 20A0h
CONTROLSS_ADC3_CFG	502C 30A0h
CONTROLSS_ADC4_CFG	502C 40A0h

Figure 3-54. CONTROLSS_ADC0_CFG_ADCPPB3CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
RO		RW	RW	RW			
0		0	0	0			

Access Types Legend

Table 3-110. ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	RO		Reserved
5	CBCEN	RW	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	RW	0h	ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register. 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx

Table 3-110. ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	RW	0h	ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 3 0001 SOC1/EOC1/RESULT1 is associated with post processing block 3 0010 SOC2/EOC2/RESULT2 is associated with post processing block 3 0011 SOC3/EOC3/RESULT3 is associated with post processing block 3 0100 SOC4/EOC4/RESULT4 is associated with post processing block 3 0101 SOC5/EOC5/RESULT5 is associated with post processing block 3 0110 SOC6/EOC6/RESULT6 is associated with post processing block 3 0111 SOC7/EOC7/RESULT7 is associated with post processing block 3 1000 SOC8/EOC8/RESULT8 is associated with post processing block 3 1001 SOC9/EOC9/RESULT9 is associated with post processing block 3 1010 SOC10/EOC10/RESULT10 is associated with post processing block 3 1011 SOC11/EOC11/RESULT11 is associated with post processing block 3 1100 SOC12/EOC12/RESULT12 is associated with post processing block 3 1101 SOC13/EOC13/RESULT13 is associated with post processing block 3 1110 SOC14/EOC14/RESULT14 is associated with post processing block 3 1111 SOC15/EOC15/RESULT15 is associated with post processing block 3

3.1.55 CONTROLSS_ADC0_CFG_ADCPPB3STAMP Register (Offset = A2h) [reset = h]

Short Description: ADC PPB3 Sample Delay Time Stamp Register

Long Description:

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Table 3-111. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A2h
CONTROLSS_ADC1_CFG	502C 10A2h
CONTROLSS_ADC2_CFG	502C 20A2h
CONTROLSS_ADC3_CFG	502C 30A2h
CONTROLSS_ADC4_CFG	502C 40A2h

Figure 3-55. CONTROLSS_ADC0_CFG_ADCPPB3STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
RO							
0							

Access Types Legend

Table 3-112. ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DLYSTAMP	RO	0h	ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.1.56 CONTROLSS_ADC0_CFG_ADCPPB3OFFCAL Register (Offset = A4h) [reset = h]

Short Description: ADC PPB3 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-113. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A4h
CONTROLSS_ADC1_CFG	502C 10A4h
CONTROLSS_ADC2_CFG	502C 20A4h
CONTROLSS_ADC3_CFG	502C 30A4h
CONTROLSS_ADC4_CFG	502C 40A4h

Figure 3-56. CONTROLSS_ADC0_CFG_ADCPPB3OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
RW							
0							

Access Types Legend

Table 3-114. ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	OFFCAL	RW	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.1.57 CONTROLSS_ADC0_CFG_ADCPPB3OFFREF Register (Offset = A6h) [reset = h]

Short Description: ADC PPB3 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-115. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A6h
CONTROLSS_ADC1_CFG	502C 10A6h
CONTROLSS_ADC2_CFG	502C 20A6h
CONTROLSS_ADC3_CFG	502C 30A6h
CONTROLSS_ADC4_CFG	502C 40A6h

Figure 3-57. CONTROLSS_ADC0_CFG_ADCPPB3OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
RW							
0							
7	6	5	4	3	2	1	0
OFFREF							
RW							
0							

Access Types Legend

Table 3-116. ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	RW	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.1.58 CONTROLSS_ADC0_CFG_ADCPPB3TRIPHI Register (Offset = A8h) [reset = h]

Short Description: ADC PPB3 Trip High Register

Long Description:

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Table 3-117. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A8h
CONTROLSS_ADC1_CFG	502C 10A8h
CONTROLSS_ADC2_CFG	502C 20A8h
CONTROLSS_ADC3_CFG	502C 30A8h
CONTROLSS_ADC4_CFG	502C 40A8h

Figure 3-58. CONTROLSS_ADC0_CFG_ADCPPB3TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
RO															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
RW															
0															

Access Types Legend

Table 3-118. ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	RO		Reserved
16	HSIGN	RW	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	RW	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB3RESULT register.

3.1.59 CONTROLSS_ADC0_CFG_ADCPPB3TRIPLO Register (Offset = ACh) [reset = h]

Short Description: ADC PPB3 Trip Low/Trigger Time Stamp Register

Long Description:

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Table 3-119. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ACh
CONTROLSS_ADC1_CFG	502C 10ACh
CONTROLSS_ADC2_CFG	502C 20ACh
CONTROLSS_ADC3_CFG	502C 30ACh
CONTROLSS_ADC4_CFG	502C 40ACh

Figure 3-59. CONTROLSS_ADC0_CFG_ADCPPB3TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
RO												RO			RW
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
RW															
0															

Access Types Legend

Table 3-120. ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	RO	0h	ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	RO		Reserved
16	LSIGN	RW	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	RW	0h	ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB3RESULT register.

3.1.60 CONTROLSS_ADC0_CFG_ADCPPB4CONFIG Register (Offset = B0h) [reset = h]

Short Description: ADC PPB4 Config Register

Long Description:

Return to Summary Table

Table 3-121. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B0h
CONTROLSS_ADC1_CFG	502C 10B0h
CONTROLSS_ADC2_CFG	502C 20B0h
CONTROLSS_ADC3_CFG	502C 30B0h
CONTROLSS_ADC4_CFG	502C 40B0h

Figure 3-60. CONTROLSS_ADC0_CFG_ADCPPB4CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
RO		RW	RW	RW			
0		0	0	0			

Access Types Legend

Table 3-122. ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	RO		Reserved
5	CBCEN	RW	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	RW	0h	ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register. 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx

Table 3-122. ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	RW	0h	ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 4 0001 SOC1/EOC1/RESULT1 is associated with post processing block 4 0010 SOC2/EOC2/RESULT2 is associated with post processing block 4 0011 SOC3/EOC3/RESULT3 is associated with post processing block 4 0100 SOC4/EOC4/RESULT4 is associated with post processing block 4 0101 SOC5/EOC5/RESULT5 is associated with post processing block 4 0110 SOC6/EOC6/RESULT6 is associated with post processing block 4 0111 SOC7/EOC7/RESULT7 is associated with post processing block 4 1000 SOC8/EOC8/RESULT8 is associated with post processing block 4 1001 SOC9/EOC9/RESULT9 is associated with post processing block 4 1010 SOC10/EOC10/RESULT10 is associated with post processing block 4 1011 SOC11/EOC11/RESULT11 is associated with post processing block 4 1100 SOC12/EOC12/RESULT12 is associated with post processing block 4 1101 SOC13/EOC13/RESULT13 is associated with post processing block 4 1110 SOC14/EOC14/RESULT14 is associated with post processing block 4 1111 SOC15/EOC15/RESULT15 is associated with post processing block 4

3.1.61 CONTROLSS_ADC0_CFG_ADCPPB4STAMP Register (Offset = B2h) [reset = h]

Short Description: ADC PPB4 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-123. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B2h
CONTROLSS_ADC1_CFG	502C 10B2h
CONTROLSS_ADC2_CFG	502C 20B2h
CONTROLSS_ADC3_CFG	502C 30B2h
CONTROLSS_ADC4_CFG	502C 40B2h

Figure 3-61. CONTROLSS_ADC0_CFG_ADCPPB4STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
RO							
0							

Access Types Legend

Table 3-124. ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DLYSTAMP	RO	0h	ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

3.1.62 CONTROLSS_ADC0_CFG_ADCPPB4OFFCAL Register (Offset = B4h) [reset = h]

Short Description: ADC PPB4 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-125. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B4h
CONTROLSS_ADC1_CFG	502C 10B4h
CONTROLSS_ADC2_CFG	502C 20B4h
CONTROLSS_ADC3_CFG	502C 30B4h
CONTROLSS_ADC4_CFG	502C 40B4h

Figure 3-62. CONTROLSS_ADC0_CFG_ADCPPB4OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
RW							
0							

Access Types Legend

Table 3-126. ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	OFFCAL	RW	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

3.1.63 CONTROLSS_ADC0_CFG_ADCPPB4OFFREF Register (Offset = B6h) [reset = h]

Short Description: ADC PPB4 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-127. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B6h
CONTROLSS_ADC1_CFG	502C 10B6h
CONTROLSS_ADC2_CFG	502C 20B6h
CONTROLSS_ADC3_CFG	502C 30B6h
CONTROLSS_ADC4_CFG	502C 40B6h

Figure 3-63. CONTROLSS_ADC0_CFG_ADCPPB4OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
RW							
0							
7	6	5	4	3	2	1	0
OFFREF							
RW							
0							

Access Types Legend

Table 3-128. ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	RW	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

3.1.64 CONTROLSS_ADC0_CFG_ADCPPB4TRIPHI Register (Offset = B8h) [reset = h]

Short Description: ADC PPB4 Trip High Register

Long Description:

Return to Summary Table

Table 3-129. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B8h
CONTROLSS_ADC1_CFG	502C 10B8h
CONTROLSS_ADC2_CFG	502C 20B8h
CONTROLSS_ADC3_CFG	502C 30B8h
CONTROLSS_ADC4_CFG	502C 40B8h

Figure 3-64. CONTROLSS_ADC0_CFG_ADCPPB4TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
RO															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
RW															
0															

Access Types Legend

Table 3-130. ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	RO		Reserved
16	HSIGN	RW	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	RW	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB4RESULT register.

3.1.65 CONTROLSS_ADC0_CFG_ADCPPB4TRIPLO Register (Offset = BCh) [reset = h]

Short Description: ADC PPB4 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-131. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00BCh
CONTROLSS_ADC1_CFG	502C 10BCh
CONTROLSS_ADC2_CFG	502C 20BCh
CONTROLSS_ADC3_CFG	502C 30BCh
CONTROLSS_ADC4_CFG	502C 40BCh

Figure 3-65. CONTROLSS_ADC0_CFG_ADCPPB4TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
RO												RO			RW
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
RW															
0															

Access Types Legend

Table 3-132. ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	RO	0h	ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	RO		Reserved
16	LSIGN	RW	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	RW	0h	ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register.

3.1.66 CONTROLSS_ADC0_CFG_ADCINTCYCLE Register (Offset = DEh) [reset = h]

Short Description: ADC Early Interrupt Generation Cycle

Long Description:

Return to Summary Table

Table 3-133. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00DEh
CONTROLSS_ADC1_CFG	502C 10DEh
CONTROLSS_ADC2_CFG	502C 20DEh
CONTROLSS_ADC3_CFG	502C 30DEh
CONTROLSS_ADC4_CFG	502C 40DEh

Figure 3-66. CONTROLSS_ADC0_CFG_ADCINTCYCLE Name Register

15	14	13	12	11	10	9	8
DELAY							
RW							
0							
7	6	5	4	3	2	1	0
DELAY							
RW							
0							

Access Types Legend

Table 3-134. ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DELAY	RW	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated.

3.1.67 CONTROLSS_ADC0_CFG_ADCINLTRIM1 Register (Offset = E0h) [reset = h]

Short Description: ADC Linearity Trim 1 Register

Long Description:

Return to Summary Table

Table 3-135. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E0h
CONTROLSS_ADC1_CFG	502C 10E0h
CONTROLSS_ADC2_CFG	502C 20E0h
CONTROLSS_ADC3_CFG	502C 30E0h
CONTROLSS_ADC4_CFG	502C 40E0h

Figure 3-67. CONTROLSS_ADC0_CFG_ADCINLTRIM1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM31TO0															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM31TO0															
RW															
11000000111111111101110															

Access Types Legend

Table 3-136. ADCINLTRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM31TO0	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 31-0. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.68 CONTROLSS_ADC0_CFG_ADCINLTRIM2 Register (Offset = E4h) [reset = h]

Short Description: ADC Linearity Trim 2 Register

Long Description:

Return to Summary Table

Table 3-137. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E4h
CONTROLSS_ADC1_CFG	502C 10E4h
CONTROLSS_ADC2_CFG	502C 20E4h
CONTROLSS_ADC3_CFG	502C 30E4h
CONTROLSS_ADC4_CFG	502C 40E4h

Figure 3-68. CONTROLSS_ADC0_CFG_ADCINLTRIM2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM63TO32															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM63TO32															
RW															
11000000111111111101110															

Access Types Legend

Table 3-138. ADCINLTRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM63TO32	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 63-32. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.69 CONTROLSS_ADC0_CFG_ADCINLTRIM3 Register (Offset = E8h) [reset = h]

Short Description: ADC Linearity Trim 3 Register

Long Description:

Return to Summary Table

Table 3-139. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E8h
CONTROLSS_ADC1_CFG	502C 10E8h
CONTROLSS_ADC2_CFG	502C 20E8h
CONTROLSS_ADC3_CFG	502C 30E8h
CONTROLSS_ADC4_CFG	502C 40E8h

Figure 3-69. CONTROLSS_ADC0_CFG_ADCINLTRIM3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM95TO64															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM95TO64															
RW															
11000000111111111101110															

Access Types Legend

Table 3-140. ADCINLTRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM95TO64	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 95-64. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.70 CONTROLSS_ADC0_CFG_ADCINLTRIM4 Register (Offset = ECh) [reset = h]

Short Description: ADC Linearity Trim 4 Register

Long Description:

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Table 3-141. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ECh
CONTROLSS_ADC1_CFG	502C 10ECh
CONTROLSS_ADC2_CFG	502C 20ECh
CONTROLSS_ADC3_CFG	502C 30ECh
CONTROLSS_ADC4_CFG	502C 40ECh

Figure 3-70. CONTROLSS_ADC0_CFG_ADCINLTRIM4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM127TO96															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM127TO96															
RW															
11000000111111111101110															

Access Types Legend

Table 3-142. ADCINLTRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM127TO96	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 127-96. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.71 CONTROLSS_ADC0_CFG_ADCINLTRIM5 Register (Offset = F0h) [reset = h]

Short Description: ADC Linearity Trim 5 Register

Long Description:

Return to Summary Table

Table 3-143. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F0h
CONTROLSS_ADC1_CFG	502C 10F0h
CONTROLSS_ADC2_CFG	502C 20F0h
CONTROLSS_ADC3_CFG	502C 30F0h
CONTROLSS_ADC4_CFG	502C 40F0h

Figure 3-71. CONTROLSS_ADC0_CFG_ADCINLTRIM5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM159TO128															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM159TO128															
RW															
11000000111111111101110															

Access Types Legend

Table 3-144. ADCINLTRIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM159TO128	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 159-128. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.72 CONTROLSS_ADC0_CFG_ADCINLTRIM6 Register (Offset = F4h) [reset = h]

Short Description: ADC Linearity Trim 6 Register

Long Description:

Return to Summary Table

Table 3-145. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F4h
CONTROLSS_ADC1_CFG	502C 10F4h
CONTROLSS_ADC2_CFG	502C 20F4h
CONTROLSS_ADC3_CFG	502C 30F4h
CONTROLSS_ADC4_CFG	502C 40F4h

Figure 3-72. CONTROLSS_ADC0_CFG_ADCINLTRIM6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM191TO160															
RW															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM191TO160															
RW															
11000000111111111101110															

Access Types Legend

Table 3-146. ADCINLTRIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM191TO160	RW	174B1CAC9D925FD54AB6h	ADC Linearity Trim Bits 191-160. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.1.73 CONTROLSS_ADC0_CFG_ADCINLTRIMCTL Register (Offset = FCh) [reset = h]

Short Description: ADC Linearity Trim Control Register

Long Description:

Return to Summary Table

Table 3-147. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00FCh
CONTROLSS_ADC1_CFG	502C 10FCh
CONTROLSS_ADC2_CFG	502C 20FCh
CONTROLSS_ADC3_CFG	502C 30FCh
CONTROLSS_ADC4_CFG	502C 40FCh

Figure 3-73. CONTROLSS_ADC0_CFG_ADCINLTRIMCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CALIBSTEP					CALIB MODE
RO										RW					RW
0										0					0

Access Types Legend

Table 3-148. ADCINLTRIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	KEY	RW	0h	ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero.
15 - 6	RESERVED	RO		Reserved
5 - 1	CALIBSTEP	RW	0h	ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.
0	CALIBMODE	RW	0h	ADC Linearity Calibration Mode.

3.2 C2K_ADC_RESULT_REGS Registers

Table 3-149. CONTROLSS_ADC0_RESULT, CONTROLSS_ADC0_RESULT_CONTROLSS_ADC0_RESULT Registers, Base Address=5010 0000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_RESULT Physical Address
0h	16	CONTROLSS_ADC0_RESULT_ADCRESULT0	ADC Result 0 Register	5010 0000h
2h	16	CONTROLSS_ADC0_RESULT_ADCRESULT1	ADC Result 1 Register	5010 0002h
4h	16	CONTROLSS_ADC0_RESULT_ADCRESULT2	ADC Result 2 Register	5010 0004h
6h	16	CONTROLSS_ADC0_RESULT_ADCRESULT3	ADC Result 3 Register	5010 0006h

Table 3-149. CONTROLSS_ADC0_RESULT, CONTROLSS_ADC0_RESULT_CONTROLSS_ADC0_RESULT Registers, Base Address=5010 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC0_RESULT Physical Address
8h	16	CONTROLSS_ADC0_RESULT_ADCRESULT4	ADC Result 4 Register	5010 0008h
Ah	16	CONTROLSS_ADC0_RESULT_ADCRESULT5	ADC Result 5 Register	5010 000Ah
Ch	16	CONTROLSS_ADC0_RESULT_ADCRESULT6	ADC Result 6 Register	5010 000Ch
Eh	16	CONTROLSS_ADC0_RESULT_ADCRESULT7	ADC Result 7 Register	5010 000Eh
10h	16	CONTROLSS_ADC0_RESULT_ADCRESULT8	ADC Result 8 Register	5010 0010h
12h	16	CONTROLSS_ADC0_RESULT_ADCRESULT9	ADC Result 9 Register	5010 0012h
14h	16	CONTROLSS_ADC0_RESULT_ADCRESULT10	ADC Result 10 Register	5010 0014h
16h	16	CONTROLSS_ADC0_RESULT_ADCRESULT11	ADC Result 11 Register	5010 0016h
18h	16	CONTROLSS_ADC0_RESULT_ADCRESULT12	ADC Result 12 Register	5010 0018h
1Ah	16	CONTROLSS_ADC0_RESULT_ADCRESULT13	ADC Result 13 Register	5010 001Ah
1Ch	16	CONTROLSS_ADC0_RESULT_ADCRESULT14	ADC Result 14 Register	5010 001Ch
1Eh	16	CONTROLSS_ADC0_RESULT_ADCRESULT15	ADC Result 15 Register	5010 001Eh
20h	32	CONTROLSS_ADC0_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	5010 0020h
24h	32	CONTROLSS_ADC0_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	5010 0024h
28h	32	CONTROLSS_ADC0_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	5010 0028h
2Ch	32	CONTROLSS_ADC0_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	5010 002Ch

Table 3-150. CONTROLSS_ADC0_RESULT, CONTROLSS_ADC0_RESULT_CONTROLSS_ADC0_RESULT Registers, Base Address=5010 0000H, Length=4

Offset	Length	Acronym	Register Name
0h	16	CONTROLSS_ADC0_RESULT_ADCRESULT0	ADC Result 0 Register
2h	16	CONTROLSS_ADC0_RESULT_ADCRESULT1	ADC Result 1 Register
4h	16	CONTROLSS_ADC0_RESULT_ADCRESULT2	ADC Result 2 Register
6h	16	CONTROLSS_ADC0_RESULT_ADCRESULT3	ADC Result 3 Register
8h	16	CONTROLSS_ADC0_RESULT_ADCRESULT4	ADC Result 4 Register
Ah	16	CONTROLSS_ADC0_RESULT_ADCRESULT5	ADC Result 5 Register
Ch	16	CONTROLSS_ADC0_RESULT_ADCRESULT6	ADC Result 6 Register
Eh	16	CONTROLSS_ADC0_RESULT_ADCRESULT7	ADC Result 7 Register

Table 3-150. CONTROLSS_ADC0_RESULT, CONTROLSS_ADC0_RESULT_CONTROLSS_ADC0_RESULT Registers, Base Address=5010 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
10h	16	CONTROLSS_ADC0_RESULT_ADCRESULT8	ADC Result 8 Register
12h	16	CONTROLSS_ADC0_RESULT_ADCRESULT9	ADC Result 9 Register
14h	16	CONTROLSS_ADC0_RESULT_ADCRESULT10	ADC Result 10 Register
16h	16	CONTROLSS_ADC0_RESULT_ADCRESULT11	ADC Result 11 Register
18h	16	CONTROLSS_ADC0_RESULT_ADCRESULT12	ADC Result 12 Register
1Ah	16	CONTROLSS_ADC0_RESULT_ADCRESULT13	ADC Result 13 Register
1Ch	16	CONTROLSS_ADC0_RESULT_ADCRESULT14	ADC Result 14 Register
1Eh	16	CONTROLSS_ADC0_RESULT_ADCRESULT15	ADC Result 15 Register
20h	32	CONTROLSS_ADC0_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register
24h	32	CONTROLSS_ADC0_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register
28h	32	CONTROLSS_ADC0_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register
2Ch	32	CONTROLSS_ADC0_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register

Table 3-151. CONTROLSS_ADC1_RESULT, CONTROLSS_ADC1_RESULT_CONTROLSS_ADC1_RESULT Registers, Base Address=5010 1000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_ADC1_RESULT Physical Address
0h	16	CONTROLSS_ADC1_RESULT_ADCRESULT0	ADC Result 0 Register	5010 1000h
2h	16	CONTROLSS_ADC1_RESULT_ADCRESULT1	ADC Result 1 Register	5010 1002h
4h	16	CONTROLSS_ADC1_RESULT_ADCRESULT2	ADC Result 2 Register	5010 1004h
6h	16	CONTROLSS_ADC1_RESULT_ADCRESULT3	ADC Result 3 Register	5010 1006h
8h	16	CONTROLSS_ADC1_RESULT_ADCRESULT4	ADC Result 4 Register	5010 1008h
Ah	16	CONTROLSS_ADC1_RESULT_ADCRESULT5	ADC Result 5 Register	5010 100Ah
Ch	16	CONTROLSS_ADC1_RESULT_ADCRESULT6	ADC Result 6 Register	5010 100Ch
Eh	16	CONTROLSS_ADC1_RESULT_ADCRESULT7	ADC Result 7 Register	5010 100Eh
10h	16	CONTROLSS_ADC1_RESULT_ADCRESULT8	ADC Result 8 Register	5010 1010h
12h	16	CONTROLSS_ADC1_RESULT_ADCRESULT9	ADC Result 9 Register	5010 1012h
14h	16	CONTROLSS_ADC1_RESULT_ADCRESULT10	ADC Result 10 Register	5010 1014h
16h	16	CONTROLSS_ADC1_RESULT_ADCRESULT11	ADC Result 11 Register	5010 1016h

Table 3-151. CONTROLSS_ADC1_RESULT, CONTROLSS_ADC1_RESULT_CONTROLSS_ADC1_RESULT Registers, Base Address=5010 1000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC1_RESULT Physical Address
18h	16	CONTROLSS_ADC1_RESULT_ADCRESULT12	ADC Result 12 Register	5010 1018h
1Ah	16	CONTROLSS_ADC1_RESULT_ADCRESULT13	ADC Result 13 Register	5010 101Ah
1Ch	16	CONTROLSS_ADC1_RESULT_ADCRESULT14	ADC Result 14 Register	5010 101Ch
1Eh	16	CONTROLSS_ADC1_RESULT_ADCRESULT15	ADC Result 15 Register	5010 101Eh
20h	32	CONTROLSS_ADC1_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	5010 1020h
24h	32	CONTROLSS_ADC1_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	5010 1024h
28h	32	CONTROLSS_ADC1_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	5010 1028h
2Ch	32	CONTROLSS_ADC1_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	5010 102Ch

Table 3-152. CONTROLSS_ADC1_RESULT, CONTROLSS_ADC1_RESULT_CONTROLSS_ADC1_RESULT Registers, Base Address=5010 1000H, Length=4

Offset	Length	Acronym	Register Name
0h	16	CONTROLSS_ADC1_RESULT_ADCRESULT0	ADC Result 0 Register
2h	16	CONTROLSS_ADC1_RESULT_ADCRESULT1	ADC Result 1 Register
4h	16	CONTROLSS_ADC1_RESULT_ADCRESULT2	ADC Result 2 Register
6h	16	CONTROLSS_ADC1_RESULT_ADCRESULT3	ADC Result 3 Register
8h	16	CONTROLSS_ADC1_RESULT_ADCRESULT4	ADC Result 4 Register
Ah	16	CONTROLSS_ADC1_RESULT_ADCRESULT5	ADC Result 5 Register
Ch	16	CONTROLSS_ADC1_RESULT_ADCRESULT6	ADC Result 6 Register
Eh	16	CONTROLSS_ADC1_RESULT_ADCRESULT7	ADC Result 7 Register
10h	16	CONTROLSS_ADC1_RESULT_ADCRESULT8	ADC Result 8 Register
12h	16	CONTROLSS_ADC1_RESULT_ADCRESULT9	ADC Result 9 Register
14h	16	CONTROLSS_ADC1_RESULT_ADCRESULT10	ADC Result 10 Register
16h	16	CONTROLSS_ADC1_RESULT_ADCRESULT11	ADC Result 11 Register
18h	16	CONTROLSS_ADC1_RESULT_ADCRESULT12	ADC Result 12 Register
1Ah	16	CONTROLSS_ADC1_RESULT_ADCRESULT13	ADC Result 13 Register
1Ch	16	CONTROLSS_ADC1_RESULT_ADCRESULT14	ADC Result 14 Register
1Eh	16	CONTROLSS_ADC1_RESULT_ADCRESULT15	ADC Result 15 Register

Table 3-152. CONTROLSS_ADC1_RESULT, CONTROLSS_ADC1_RESULT_CONTROLSS_ADC1_RESULT Registers, Base Address=5010 1000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
20h	32	CONTROLSS_ADC1_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register
24h	32	CONTROLSS_ADC1_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register
28h	32	CONTROLSS_ADC1_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register
2Ch	32	CONTROLSS_ADC1_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register

Table 3-153. CONTROLSS_ADC2_RESULT, CONTROLSS_ADC2_RESULT_CONTROLSS_ADC2_RESULT Registers, Base Address=5010 2000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_ADC2_RESULT Physical Address
0h	16	CONTROLSS_ADC2_RESULT_ADCRESULT0	ADC Result 0 Register	5010 2000h
2h	16	CONTROLSS_ADC2_RESULT_ADCRESULT1	ADC Result 1 Register	5010 2002h
4h	16	CONTROLSS_ADC2_RESULT_ADCRESULT2	ADC Result 2 Register	5010 2004h
6h	16	CONTROLSS_ADC2_RESULT_ADCRESULT3	ADC Result 3 Register	5010 2006h
8h	16	CONTROLSS_ADC2_RESULT_ADCRESULT4	ADC Result 4 Register	5010 2008h
Ah	16	CONTROLSS_ADC2_RESULT_ADCRESULT5	ADC Result 5 Register	5010 200Ah
Ch	16	CONTROLSS_ADC2_RESULT_ADCRESULT6	ADC Result 6 Register	5010 200Ch
Eh	16	CONTROLSS_ADC2_RESULT_ADCRESULT7	ADC Result 7 Register	5010 200Eh
10h	16	CONTROLSS_ADC2_RESULT_ADCRESULT8	ADC Result 8 Register	5010 2010h
12h	16	CONTROLSS_ADC2_RESULT_ADCRESULT9	ADC Result 9 Register	5010 2012h
14h	16	CONTROLSS_ADC2_RESULT_ADCRESULT10	ADC Result 10 Register	5010 2014h
16h	16	CONTROLSS_ADC2_RESULT_ADCRESULT11	ADC Result 11 Register	5010 2016h
18h	16	CONTROLSS_ADC2_RESULT_ADCRESULT12	ADC Result 12 Register	5010 2018h
1Ah	16	CONTROLSS_ADC2_RESULT_ADCRESULT13	ADC Result 13 Register	5010 201Ah
1Ch	16	CONTROLSS_ADC2_RESULT_ADCRESULT14	ADC Result 14 Register	5010 201Ch
1Eh	16	CONTROLSS_ADC2_RESULT_ADCRESULT15	ADC Result 15 Register	5010 201Eh
20h	32	CONTROLSS_ADC2_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	5010 2020h
24h	32	CONTROLSS_ADC2_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	5010 2024h
28h	32	CONTROLSS_ADC2_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	5010 2028h

Table 3-153. CONTROLSS_ADC2_RESULT, CONTROLSS_ADC2_RESULT_CONTROLSS_ADC2_RESULT Registers, Base Address=5010 2000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC2_RESULT Physical Address
2Ch	32	CONTROLSS_ADC2_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	5010 202Ch

Table 3-154. CONTROLSS_ADC2_RESULT, CONTROLSS_ADC2_RESULT_CONTROLSS_ADC2_RESULT Registers, Base Address=5010 2000H, Length=4

Offset	Length	Acronym	Register Name
0h	16	CONTROLSS_ADC2_RESULT_ADCRESULT0	ADC Result 0 Register
2h	16	CONTROLSS_ADC2_RESULT_ADCRESULT1	ADC Result 1 Register
4h	16	CONTROLSS_ADC2_RESULT_ADCRESULT2	ADC Result 2 Register
6h	16	CONTROLSS_ADC2_RESULT_ADCRESULT3	ADC Result 3 Register
8h	16	CONTROLSS_ADC2_RESULT_ADCRESULT4	ADC Result 4 Register
Ah	16	CONTROLSS_ADC2_RESULT_ADCRESULT5	ADC Result 5 Register
Ch	16	CONTROLSS_ADC2_RESULT_ADCRESULT6	ADC Result 6 Register
Eh	16	CONTROLSS_ADC2_RESULT_ADCRESULT7	ADC Result 7 Register
10h	16	CONTROLSS_ADC2_RESULT_ADCRESULT8	ADC Result 8 Register
12h	16	CONTROLSS_ADC2_RESULT_ADCRESULT9	ADC Result 9 Register
14h	16	CONTROLSS_ADC2_RESULT_ADCRESULT10	ADC Result 10 Register
16h	16	CONTROLSS_ADC2_RESULT_ADCRESULT11	ADC Result 11 Register
18h	16	CONTROLSS_ADC2_RESULT_ADCRESULT12	ADC Result 12 Register
1Ah	16	CONTROLSS_ADC2_RESULT_ADCRESULT13	ADC Result 13 Register
1Ch	16	CONTROLSS_ADC2_RESULT_ADCRESULT14	ADC Result 14 Register
1Eh	16	CONTROLSS_ADC2_RESULT_ADCRESULT15	ADC Result 15 Register
20h	32	CONTROLSS_ADC2_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register
24h	32	CONTROLSS_ADC2_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register
28h	32	CONTROLSS_ADC2_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register
2Ch	32	CONTROLSS_ADC2_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register

Table 3-155. CONTROLSS_ADC3_RESULT, CONTROLSS_ADC3_RESULT_CONTROLSS_ADC3_RESULT Registers, Base Address=5010 3000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_ADC3_RESULT Physical Address
0h	16	CONTROLSS_ADC3_RESULT_ADCRESULT0	ADC Result 0 Register	5010 3000h
2h	16	CONTROLSS_ADC3_RESULT_ADCRESULT1	ADC Result 1 Register	5010 3002h
4h	16	CONTROLSS_ADC3_RESULT_ADCRESULT2	ADC Result 2 Register	5010 3004h
6h	16	CONTROLSS_ADC3_RESULT_ADCRESULT3	ADC Result 3 Register	5010 3006h
8h	16	CONTROLSS_ADC3_RESULT_ADCRESULT4	ADC Result 4 Register	5010 3008h
Ah	16	CONTROLSS_ADC3_RESULT_ADCRESULT5	ADC Result 5 Register	5010 300Ah
Ch	16	CONTROLSS_ADC3_RESULT_ADCRESULT6	ADC Result 6 Register	5010 300Ch
Eh	16	CONTROLSS_ADC3_RESULT_ADCRESULT7	ADC Result 7 Register	5010 300Eh
10h	16	CONTROLSS_ADC3_RESULT_ADCRESULT8	ADC Result 8 Register	5010 3010h
12h	16	CONTROLSS_ADC3_RESULT_ADCRESULT9	ADC Result 9 Register	5010 3012h
14h	16	CONTROLSS_ADC3_RESULT_ADCRESULT10	ADC Result 10 Register	5010 3014h
16h	16	CONTROLSS_ADC3_RESULT_ADCRESULT11	ADC Result 11 Register	5010 3016h
18h	16	CONTROLSS_ADC3_RESULT_ADCRESULT12	ADC Result 12 Register	5010 3018h
1Ah	16	CONTROLSS_ADC3_RESULT_ADCRESULT13	ADC Result 13 Register	5010 301Ah
1Ch	16	CONTROLSS_ADC3_RESULT_ADCRESULT14	ADC Result 14 Register	5010 301Ch
1Eh	16	CONTROLSS_ADC3_RESULT_ADCRESULT15	ADC Result 15 Register	5010 301Eh
20h	32	CONTROLSS_ADC3_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	5010 3020h
24h	32	CONTROLSS_ADC3_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	5010 3024h
28h	32	CONTROLSS_ADC3_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	5010 3028h
2Ch	32	CONTROLSS_ADC3_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	5010 302Ch

Table 3-156. CONTROLSS_ADC3_RESULT, CONTROLSS_ADC3_RESULT_CONTROLSS_ADC3_RESULT Registers, Base Address=5010 3000H, Length=4

Offset	Length	Acronym	Register Name
0h	16	CONTROLSS_ADC3_RESULT_ADCRESULT0	ADC Result 0 Register
2h	16	CONTROLSS_ADC3_RESULT_ADCRESULT1	ADC Result 1 Register
4h	16	CONTROLSS_ADC3_RESULT_ADCRESULT2	ADC Result 2 Register
6h	16	CONTROLSS_ADC3_RESULT_ADCRESULT3	ADC Result 3 Register

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Table 3-156. CONTROLSS_ADC3_RESULT, CONTROLSS_ADC3_RESULT_CONTROLSS_ADC3_RESULT Registers, Base Address=5010 3000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
8h	16	CONTROLSS_ADC3_RESULT_ADCRESULT4	ADC Result 4 Register
Ah	16	CONTROLSS_ADC3_RESULT_ADCRESULT5	ADC Result 5 Register
Ch	16	CONTROLSS_ADC3_RESULT_ADCRESULT6	ADC Result 6 Register
Eh	16	CONTROLSS_ADC3_RESULT_ADCRESULT7	ADC Result 7 Register
10h	16	CONTROLSS_ADC3_RESULT_ADCRESULT8	ADC Result 8 Register
12h	16	CONTROLSS_ADC3_RESULT_ADCRESULT9	ADC Result 9 Register
14h	16	CONTROLSS_ADC3_RESULT_ADCRESULT10	ADC Result 10 Register
16h	16	CONTROLSS_ADC3_RESULT_ADCRESULT11	ADC Result 11 Register
18h	16	CONTROLSS_ADC3_RESULT_ADCRESULT12	ADC Result 12 Register
1Ah	16	CONTROLSS_ADC3_RESULT_ADCRESULT13	ADC Result 13 Register
1Ch	16	CONTROLSS_ADC3_RESULT_ADCRESULT14	ADC Result 14 Register
1Eh	16	CONTROLSS_ADC3_RESULT_ADCRESULT15	ADC Result 15 Register
20h	32	CONTROLSS_ADC3_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register
24h	32	CONTROLSS_ADC3_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register
28h	32	CONTROLSS_ADC3_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register
2Ch	32	CONTROLSS_ADC3_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register

Table 3-157. CONTROLSS_ADC4_RESULT, CONTROLSS_ADC4_RESULT_CONTROLSS_ADC4_RESULT Registers, Base Address=5010 4000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_ADC4_RESULT Physical Address
0h	16	CONTROLSS_ADC4_RESULT_ADCRESULT0	ADC Result 0 Register	5010 4000h
2h	16	CONTROLSS_ADC4_RESULT_ADCRESULT1	ADC Result 1 Register	5010 4002h
4h	16	CONTROLSS_ADC4_RESULT_ADCRESULT2	ADC Result 2 Register	5010 4004h
6h	16	CONTROLSS_ADC4_RESULT_ADCRESULT3	ADC Result 3 Register	5010 4006h
8h	16	CONTROLSS_ADC4_RESULT_ADCRESULT4	ADC Result 4 Register	5010 4008h
Ah	16	CONTROLSS_ADC4_RESULT_ADCRESULT5	ADC Result 5 Register	5010 400Ah
Ch	16	CONTROLSS_ADC4_RESULT_ADCRESULT6	ADC Result 6 Register	5010 400Ch
Eh	16	CONTROLSS_ADC4_RESULT_ADCRESULT7	ADC Result 7 Register	5010 400Eh

Table 3-157. CONTROLSS_ADC4_RESULT, CONTROLSS_ADC4_RESULT_CONTROLSS_ADC4_RESULT Registers, Base Address=5010 4000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ADC4_RESULT Physical Address
10h	16	CONTROLSS_ADC4_RESULT_ADCRESULT8	ADC Result 8 Register	5010 4010h
12h	16	CONTROLSS_ADC4_RESULT_ADCRESULT9	ADC Result 9 Register	5010 4012h
14h	16	CONTROLSS_ADC4_RESULT_ADCRESULT10	ADC Result 10 Register	5010 4014h
16h	16	CONTROLSS_ADC4_RESULT_ADCRESULT11	ADC Result 11 Register	5010 4016h
18h	16	CONTROLSS_ADC4_RESULT_ADCRESULT12	ADC Result 12 Register	5010 4018h
1Ah	16	CONTROLSS_ADC4_RESULT_ADCRESULT13	ADC Result 13 Register	5010 401Ah
1Ch	16	CONTROLSS_ADC4_RESULT_ADCRESULT14	ADC Result 14 Register	5010 401Ch
1Eh	16	CONTROLSS_ADC4_RESULT_ADCRESULT15	ADC Result 15 Register	5010 401Eh
20h	32	CONTROLSS_ADC4_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register	5010 4020h
24h	32	CONTROLSS_ADC4_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register	5010 4024h
28h	32	CONTROLSS_ADC4_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register	5010 4028h
2Ch	32	CONTROLSS_ADC4_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register	5010 402Ch

Table 3-158. CONTROLSS_ADC4_RESULT, CONTROLSS_ADC4_RESULT_CONTROLSS_ADC4_RESULT Registers, Base Address=5010 4000H, Length=4

Offset	Length	Acronym	Register Name
0h	16	CONTROLSS_ADC4_RESULT_ADCRESULT0	ADC Result 0 Register
2h	16	CONTROLSS_ADC4_RESULT_ADCRESULT1	ADC Result 1 Register
4h	16	CONTROLSS_ADC4_RESULT_ADCRESULT2	ADC Result 2 Register
6h	16	CONTROLSS_ADC4_RESULT_ADCRESULT3	ADC Result 3 Register
8h	16	CONTROLSS_ADC4_RESULT_ADCRESULT4	ADC Result 4 Register
Ah	16	CONTROLSS_ADC4_RESULT_ADCRESULT5	ADC Result 5 Register
Ch	16	CONTROLSS_ADC4_RESULT_ADCRESULT6	ADC Result 6 Register
Eh	16	CONTROLSS_ADC4_RESULT_ADCRESULT7	ADC Result 7 Register
10h	16	CONTROLSS_ADC4_RESULT_ADCRESULT8	ADC Result 8 Register
12h	16	CONTROLSS_ADC4_RESULT_ADCRESULT9	ADC Result 9 Register
14h	16	CONTROLSS_ADC4_RESULT_ADCRESULT10	ADC Result 10 Register
16h	16	CONTROLSS_ADC4_RESULT_ADCRESULT11	ADC Result 11 Register

Table 3-158. CONTROLSS_ADC4_RESULT, CONTROLSS_ADC4_RESULT_CONTROLSS_ADC4_RESULT Registers, Base Address=5010 4000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
18h	16	CONTROLSS_ADC4_RESULT_ADCRESULT12	ADC Result 12 Register
1Ah	16	CONTROLSS_ADC4_RESULT_ADCRESULT13	ADC Result 13 Register
1Ch	16	CONTROLSS_ADC4_RESULT_ADCRESULT14	ADC Result 14 Register
1Eh	16	CONTROLSS_ADC4_RESULT_ADCRESULT15	ADC Result 15 Register
20h	32	CONTROLSS_ADC4_RESULT_ADCPPB1RESULT	ADC Post Processing Block 1 Result Register
24h	32	CONTROLSS_ADC4_RESULT_ADCPPB2RESULT	ADC Post Processing Block 2 Result Register
28h	32	CONTROLSS_ADC4_RESULT_ADCPPB3RESULT	ADC Post Processing Block 3 Result Register
2Ch	32	CONTROLSS_ADC4_RESULT_ADCPPB4RESULT	ADC Post Processing Block 4 Result Register

3.2.1 CONTROLSS_ADC0_RESULT_ADCRESULT0 Register (Offset = 0h) [reset = h]

Short Description: ADC Result 0 Register

Long Description:

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Table 3-159. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0000h

Figure 3-74. CONTROLSS_ADC0_RESULT_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-160. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 0[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.2.2 CONTROLSS_ADC0_RESULT_ADCRESULT1 Register (Offset = 2h) [reset = h]

Short Description: ADC Result 1 Register

Long Description:

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Table 3-161. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0002h

Figure 3-75. CONTROLSS_ADC0_RESULT_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-162. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 1[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.2.3 CONTROLSS_ADC0_RESULT_ADCRESULT2 Register (Offset = 4h) [reset = h]

Short Description: ADC Result 2 Register

Long Description:

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Table 3-163. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0004h

Figure 3-76. CONTROLSS_ADC0_RESULT_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-164. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 2[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.2.4 CONTROLSS_ADC0_RESULT_ADCRESULT3 Register (Offset = 6h) [reset = h]

Short Description: ADC Result 3 Register

Long Description:

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Table 3-165. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0006h

Figure 3-77. CONTROLSS_ADC0_RESULT_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-166. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 3[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.2.5 CONTROLSS_ADC0_RESULT_ADCRESULT4 Register (Offset = 8h) [reset = h]

Short Description: ADC Result 4 Register

Long Description:

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Table 3-167. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0008h

Figure 3-78. CONTROLSS_ADC0_RESULT_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-168. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 4[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.2.6 CONTROLSS_ADC0_RESULT_ADCRESULT5 Register (Offset = Ah) [reset = h]

Short Description: ADC Result 5 Register

Long Description:

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Table 3-169. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ah

Figure 3-79. CONTROLSS_ADC0_RESULT_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-170. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 5[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.2.7 CONTROLSS_ADC0_RESULT_ADCRESULT6 Register (Offset = Ch) [reset = h]

Short Description: ADC Result 6 Register

Long Description:

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Table 3-171. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ch

Figure 3-80. CONTROLSS_ADC0_RESULT_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-172. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 6[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.2.8 CONTROLSS_ADC0_RESULT_ADCRESULT7 Register (Offset = Eh) [reset = h]

Short Description: ADC Result 7 Register

Long Description:

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Table 3-173. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Eh

Figure 3-81. CONTROLSS_ADC0_RESULT_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-174. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 7[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.2.9 CONTROLSS_ADC0_RESULT_ADCRESULT8 Register (Offset = 10h) [reset = h]

Short Description: ADC Result 8 Register

Long Description:

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Table 3-175. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0010h

Figure 3-82. CONTROLSS_ADC0_RESULT_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-176. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 8[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.2.10 CONTROLSS_ADC0_RESULT_ADCRESULT9 Register (Offset = 12h) [reset = h]

Short Description: ADC Result 9 Register

Long Description:

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Table 3-177. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0012h

Figure 3-83. CONTROLSS_ADC0_RESULT_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-178. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 9[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.2.11 CONTROLSS_ADC0_RESULT_ADCRESULT10 Register (Offset = 14h) [reset = h]

Short Description: ADC Result 10 Register

Long Description:

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Table 3-179. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0014h

Figure 3-84. CONTROLSS_ADC0_RESULT_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-180. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 10[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.2.12 CONTROLSS_ADC0_RESULT_ADCRESULT11 Register (Offset = 16h) [reset = h]

Short Description: ADC Result 11 Register

Long Description:

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Table 3-181. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0016h

Figure 3-85. CONTROLSS_ADC0_RESULT_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-182. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 11[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.2.13 CONTROLSS_ADC0_RESULT_ADCRESULT12 Register (Offset = 18h) [reset = h]

Short Description: ADC Result 12 Register

Long Description:

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Table 3-183. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0018h

Figure 3-86. CONTROLSS_ADC0_RESULT_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-184. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 12[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.2.14 CONTROLSS_ADC0_RESULT_ADCRESULT13 Register (Offset = 1Ah) [reset = h]

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-185. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ah

Figure 3-87. CONTROLSS_ADC0_RESULT_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-186. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 13[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.2.15 CONTROLSS_ADC0_RESULT_ADCRESULT14 Register (Offset = 1Ch) [reset = h]

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-187. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ch

Figure 3-88. CONTROLSS_ADC0_RESULT_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-188. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 14[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.2.16 CONTROLSS_ADC0_RESULT_ADCRESULT15 Register (Offset = 1Eh) [reset = h]

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-189. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Eh

Figure 3-89. CONTROLSS_ADC0_RESULT_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-190. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 15[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.2.17 CONTROLSS_ADC0_RESULT_ADCPPB1RESULT Register (Offset = 20h) [reset = h]

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-191. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0020h

Figure 3-90. CONTROLSS_ADC0_RESULT_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-192. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 1[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.18 CONTROLSS_ADC0_RESULT_ADCPPB2RESULT Register (Offset = 24h) [reset = h]

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-193. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0024h

Figure 3-91. CONTROLSS_ADC0_RESULT_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-194. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 2[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.19 CONTROLSS_ADC0_RESULT_ADCPPB3RESULT Register (Offset = 28h) [reset = h]

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-195. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0028h

Figure 3-92. CONTROLSS_ADC0_RESULT_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-196. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 3[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.20 CONTROLSS_ADC0_RESULT_ADCPPB4RESULT Register (Offset = 2Ch) [reset = h]

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-197. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 002Ch

Figure 3-93. CONTROLSS_ADC0_RESULT_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-198. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 4[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.21 CONTROLSS_ADC1_RESULT_ADCRESULT0 Register (Offset = 0h) [reset = h]

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-199. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1000h

Figure 3-94. CONTROLSS_ADC1_RESULT_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-200. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 0[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.2.22 CONTROLSS_ADC1_RESULT_ADCRESULT1 Register (Offset = 2h) [reset = h]

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-201. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1002h

Figure 3-95. CONTROLSS_ADC1_RESULT_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-202. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 1[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.2.23 CONTROLSS_ADC1_RESULT_ADCRESULT2 Register (Offset = 4h) [reset = h]

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-203. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1004h

Figure 3-96. CONTROLSS_ADC1_RESULT_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-204. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 2[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.2.24 CONTROLSS_ADC1_RESULT_ADCRESULT3 Register (Offset = 6h) [reset = h]

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-205. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1006h

Figure 3-97. CONTROLSS_ADC1_RESULT_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-206. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 3[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.2.25 CONTROLSS_ADC1_RESULT_ADCRESULT4 Register (Offset = 8h) [reset = h]

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-207. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1008h

Figure 3-98. CONTROLSS_ADC1_RESULT_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-208. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 4[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.2.26 CONTROLSS_ADC1_RESULT_ADCRESULT5 Register (Offset = Ah) [reset = h]

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-209. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 100Ah

Figure 3-99. CONTROLSS_ADC1_RESULT_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-210. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 5[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.2.27 CONTROLSS_ADC1_RESULT_ADCRESULT6 Register (Offset = Ch) [reset = h]

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-211. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 100Ch

Figure 3-100. CONTROLSS_ADC1_RESULT_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-212. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 6[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.2.28 CONTROLSS_ADC1_RESULT_ADCRESULT7 Register (Offset = Eh) [reset = h]

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-213. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 100Eh

Figure 3-101. CONTROLSS_ADC1_RESULT_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-214. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 7[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.2.29 CONTROLSS_ADC1_RESULT_ADCRESULT8 Register (Offset = 10h) [reset = h]

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-215. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1010h

Figure 3-102. CONTROLSS_ADC1_RESULT_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-216. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 8[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.2.30 CONTROLSS_ADC1_RESULT_ADCRESULT9 Register (Offset = 12h) [reset = h]

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-217. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1012h

Figure 3-103. CONTROLSS_ADC1_RESULT_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-218. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 9[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.2.31 CONTROLSS_ADC1_RESULT_ADCRESULT10 Register (Offset = 14h) [reset = h]

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-219. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1014h

Figure 3-104. CONTROLSS_ADC1_RESULT_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-220. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 10[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.2.32 CONTROLSS_ADC1_RESULT_ADCRESULT11 Register (Offset = 16h) [reset = h]

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-221. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1016h

Figure 3-105. CONTROLSS_ADC1_RESULT_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-222. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 11[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.2.33 CONTROLSS_ADC1_RESULT_ADCRESULT12 Register (Offset = 18h) [reset = h]

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-223. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1018h

Figure 3-106. CONTROLSS_ADC1_RESULT_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-224. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 12[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.2.34 CONTROLSS_ADC1_RESULT_ADCRESULT13 Register (Offset = 1Ah) [reset = h]

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-225. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 101Ah

Figure 3-107. CONTROLSS_ADC1_RESULT_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-226. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 13[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.2.35 CONTROLSS_ADC1_RESULT_ADCRESULT14 Register (Offset = 1Ch) [reset = h]

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-227. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 101Ch

Figure 3-108. CONTROLSS_ADC1_RESULT_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-228. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 14[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.2.36 CONTROLSS_ADC1_RESULT_ADCRESULT15 Register (Offset = 1Eh) [reset = h]

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-229. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 101Eh

Figure 3-109. CONTROLSS_ADC1_RESULT_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-230. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 15[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.2.37 CONTROLSS_ADC1_RESULT_ADCPPB1RESULT Register (Offset = 20h) [reset = h]

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-231. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1020h

Figure 3-110. CONTROLSS_ADC1_RESULT_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-232. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 1[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.38 CONTROLSS_ADC1_RESULT_ADCPPB2RESULT Register (Offset = 24h) [reset = h]

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-233. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1024h

Figure 3-111. CONTROLSS_ADC1_RESULT_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-234. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 2[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.39 CONTROLSS_ADC1_RESULT_ADCPPB3RESULT Register (Offset = 28h) [reset = h]

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-235. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 1028h

Figure 3-112. CONTROLSS_ADC1_RESULT_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-236. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 3[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.40 CONTROLSS_ADC1_RESULT_ADCPPB4RESULT Register (Offset = 2Ch) [reset = h]

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-237. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC1_RESULT	5010 102Ch

Figure 3-113. CONTROLSS_ADC1_RESULT_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-238. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 4[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.41 CONTROLSS_ADC2_RESULT_ADCRESULT0 Register (Offset = 0h) [reset = h]

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-239. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2000h

Figure 3-114. CONTROLSS_ADC2_RESULT_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-240. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 0[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.2.42 CONTROLSS_ADC2_RESULT_ADCRESULT1 Register (Offset = 2h) [reset = h]

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-241. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2002h

Figure 3-115. CONTROLSS_ADC2_RESULT_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-242. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 1[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.2.43 CONTROLSS_ADC2_RESULT_ADCRESULT2 Register (Offset = 4h) [reset = h]

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-243. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2004h

Figure 3-116. CONTROLSS_ADC2_RESULT_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-244. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 2[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.2.44 CONTROLSS_ADC2_RESULT_ADCRESULT3 Register (Offset = 6h) [reset = h]

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-245. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2006h

Figure 3-117. CONTROLSS_ADC2_RESULT_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-246. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 3[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.2.45 CONTROLSS_ADC2_RESULT_ADCRESULT4 Register (Offset = 8h) [reset = h]

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-247. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2008h

Figure 3-118. CONTROLSS_ADC2_RESULT_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-248. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 4[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.2.46 CONTROLSS_ADC2_RESULT_ADCRESULT5 Register (Offset = Ah) [reset = h]

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-249. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 200Ah

Figure 3-119. CONTROLSS_ADC2_RESULT_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-250. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 5[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.2.47 CONTROLSS_ADC2_RESULT_ADCRESULT6 Register (Offset = Ch) [reset = h]

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-251. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 200Ch

Figure 3-120. CONTROLSS_ADC2_RESULT_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-252. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 6[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.2.48 CONTROLSS_ADC2_RESULT_ADCRESULT7 Register (Offset = Eh) [reset = h]

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-253. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 200Eh

Figure 3-121. CONTROLSS_ADC2_RESULT_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-254. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 7[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.2.49 CONTROLSS_ADC2_RESULT_ADCRESULT8 Register (Offset = 10h) [reset = h]

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-255. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2010h

Figure 3-122. CONTROLSS_ADC2_RESULT_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-256. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 8[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.2.50 CONTROLSS_ADC2_RESULT_ADCRESULT9 Register (Offset = 12h) [reset = h]

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-257. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2012h

Figure 3-123. CONTROLSS_ADC2_RESULT_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-258. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 9[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.2.51 CONTROLSS_ADC2_RESULT_ADCRESULT10 Register (Offset = 14h) [reset = h]

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-259. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2014h

Figure 3-124. CONTROLSS_ADC2_RESULT_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-260. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 10[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.2.52 CONTROLSS_ADC2_RESULT_ADCRESULT11 Register (Offset = 16h) [reset = h]

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-261. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2016h

Figure 3-125. CONTROLSS_ADC2_RESULT_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-262. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 11[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.2.53 CONTROLSS_ADC2_RESULT_ADCRESULT12 Register (Offset = 18h) [reset = h]

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-263. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2018h

Figure 3-126. CONTROLSS_ADC2_RESULT_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-264. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 12[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.2.54 CONTROLSS_ADC2_RESULT_ADCRESULT13 Register (Offset = 1Ah) [reset = h]

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-265. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 201Ah

Figure 3-127. CONTROLSS_ADC2_RESULT_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-266. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 13[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.2.55 CONTROLSS_ADC2_RESULT_ADCRESULT14 Register (Offset = 1Ch) [reset = h]

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-267. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 201Ch

Figure 3-128. CONTROLSS_ADC2_RESULT_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-268. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 14[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.2.56 CONTROLSS_ADC2_RESULT_ADCRESULT15 Register (Offset = 1Eh) [reset = h]

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-269. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 201Eh

Figure 3-129. CONTROLSS_ADC2_RESULT_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-270. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 15[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.2.57 CONTROLSS_ADC2_RESULT_ADCPPB1RESULT Register (Offset = 20h) [reset = h]

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-271. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2020h

Figure 3-130. CONTROLSS_ADC2_RESULT_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-272. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 1[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.58 CONTROLSS_ADC2_RESULT_ADCPPB2RESULT Register (Offset = 24h) [reset = h]

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-273. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2024h

Figure 3-131. CONTROLSS_ADC2_RESULT_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-274. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 2[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.59 CONTROLSS_ADC2_RESULT_ADCPPB3RESULT Register (Offset = 28h) [reset = h]

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-275. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 2028h

Figure 3-132. CONTROLSS_ADC2_RESULT_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-276. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 3[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.60 CONTROLSS_ADC2_RESULT_ADCPPB4RESULT Register (Offset = 2Ch) [reset = h]

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-277. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC2_RESULT	5010 202Ch

Figure 3-133. CONTROLSS_ADC2_RESULT_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-278. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 4[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.61 CONTROLSS_ADC3_RESULT_ADCRESULT0 Register (Offset = 0h) [reset = h]

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-279. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3000h

Figure 3-134. CONTROLSS_ADC3_RESULT_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-280. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 0[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.2.62 CONTROLSS_ADC3_RESULT_ADCRESULT1 Register (Offset = 2h) [reset = h]

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-281. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3002h

Figure 3-135. CONTROLSS_ADC3_RESULT_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-282. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 1[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.2.63 CONTROLSS_ADC3_RESULT_ADCRESULT2 Register (Offset = 4h) [reset = h]

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-283. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3004h

Figure 3-136. CONTROLSS_ADC3_RESULT_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-284. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 2[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.2.64 CONTROLSS_ADC3_RESULT_ADCRESULT3 Register (Offset = 6h) [reset = h]

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-285. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3006h

Figure 3-137. CONTROLSS_ADC3_RESULT_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-286. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 3[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.2.65 CONTROLSS_ADC3_RESULT_ADCRESULT4 Register (Offset = 8h) [reset = h]

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-287. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3008h

Figure 3-138. CONTROLSS_ADC3_RESULT_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-288. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 4[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.2.66 CONTROLSS_ADC3_RESULT_ADCRESULT5 Register (Offset = Ah) [reset = h]

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-289. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 300Ah

Figure 3-139. CONTROLSS_ADC3_RESULT_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-290. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 5[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.2.67 CONTROLSS_ADC3_RESULT_ADCRESULT6 Register (Offset = Ch) [reset = h]

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-291. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 300Ch

Figure 3-140. CONTROLSS_ADC3_RESULT_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-292. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 6[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.2.68 CONTROLSS_ADC3_RESULT_ADCRESULT7 Register (Offset = Eh) [reset = h]

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-293. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 300Eh

Figure 3-141. CONTROLSS_ADC3_RESULT_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-294. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 7[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.2.69 CONTROLSS_ADC3_RESULT_ADCRESULT8 Register (Offset = 10h) [reset = h]

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-295. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3010h

Figure 3-142. CONTROLSS_ADC3_RESULT_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-296. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 8[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.2.70 CONTROLSS_ADC3_RESULT_ADCRESULT9 Register (Offset = 12h) [reset = h]

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-297. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3012h

Figure 3-143. CONTROLSS_ADC3_RESULT_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-298. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 9[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.2.71 CONTROLSS_ADC3_RESULT_ADCRESULT10 Register (Offset = 14h) [reset = h]

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-299. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3014h

Figure 3-144. CONTROLSS_ADC3_RESULT_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-300. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 10[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.2.72 CONTROLSS_ADC3_RESULT_ADCRESULT11 Register (Offset = 16h) [reset = h]

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-301. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3016h

Figure 3-145. CONTROLSS_ADC3_RESULT_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-302. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 11[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.2.73 CONTROLSS_ADC3_RESULT_ADCRESULT12 Register (Offset = 18h) [reset = h]

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-303. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3018h

Figure 3-146. CONTROLSS_ADC3_RESULT_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-304. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 12[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.2.74 CONTROLSS_ADC3_RESULT_ADCRESULT13 Register (Offset = 1Ah) [reset = h]

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-305. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 301Ah

Figure 3-147. CONTROLSS_ADC3_RESULT_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-306. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 13[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.2.75 CONTROLSS_ADC3_RESULT_ADCRESULT14 Register (Offset = 1Ch) [reset = h]

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-307. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 301Ch

Figure 3-148. CONTROLSS_ADC3_RESULT_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-308. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 14[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.2.76 CONTROLSS_ADC3_RESULT_ADCRESULT15 Register (Offset = 1Eh) [reset = h]

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-309. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 301Eh

Figure 3-149. CONTROLSS_ADC3_RESULT_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-310. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 15[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.2.77 CONTROLSS_ADC3_RESULT_ADCPPB1RESULT Register (Offset = 20h) [reset = h]

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-311. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3020h

Figure 3-150. CONTROLSS_ADC3_RESULT_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-312. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 1[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.78 CONTROLSS_ADC3_RESULT_ADCPPB2RESULT Register (Offset = 24h) [reset = h]

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-313. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3024h

Figure 3-151. CONTROLSS_ADC3_RESULT_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-314. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 2[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.79 CONTROLSS_ADC3_RESULT_ADCPPB3RESULT Register (Offset = 28h) [reset = h]

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-315. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 3028h

Figure 3-152. CONTROLSS_ADC3_RESULT_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-316. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 3[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.80 CONTROLSS_ADC3_RESULT_ADCPPB4RESULT Register (Offset = 2Ch) [reset = h]

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-317. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC3_RESULT	5010 302Ch

Figure 3-153. CONTROLSS_ADC3_RESULT_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-318. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 4[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.81 CONTROLSS_ADC4_RESULT_ADCRESULT0 Register (Offset = 0h) [reset = h]

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-319. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4000h

Figure 3-154. CONTROLSS_ADC4_RESULT_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-320. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 0[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

3.2.82 CONTROLSS_ADC4_RESULT_ADCRESULT1 Register (Offset = 2h) [reset = h]

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-321. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4002h

Figure 3-155. CONTROLSS_ADC4_RESULT_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-322. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 1[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

3.2.83 CONTROLSS_ADC4_RESULT_ADCRESULT2 Register (Offset = 4h) [reset = h]

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-323. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4004h

Figure 3-156. CONTROLSS_ADC4_RESULT_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-324. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 2[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

3.2.84 CONTROLSS_ADC4_RESULT_ADCRESULT3 Register (Offset = 6h) [reset = h]

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-325. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4006h

Figure 3-157. CONTROLSS_ADC4_RESULT_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-326. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 3[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

3.2.85 CONTROLSS_ADC4_RESULT_ADCRESULT4 Register (Offset = 8h) [reset = h]

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-327. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4008h

Figure 3-158. CONTROLSS_ADC4_RESULT_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-328. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 4[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

3.2.86 CONTROLSS_ADC4_RESULT_ADCRESULT5 Register (Offset = Ah) [reset = h]

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-329. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 400Ah

Figure 3-159. CONTROLSS_ADC4_RESULT_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-330. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 5[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

3.2.87 CONTROLSS_ADC4_RESULT_ADCRESULT6 Register (Offset = Ch) [reset = h]

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-331. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 400Ch

Figure 3-160. CONTROLSS_ADC4_RESULT_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-332. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 6[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

3.2.88 CONTROLSS_ADC4_RESULT_ADCRESULT7 Register (Offset = Eh) [reset = h]

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-333. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 400Eh

Figure 3-161. CONTROLSS_ADC4_RESULT_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-334. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 7[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

3.2.89 CONTROLSS_ADC4_RESULT_ADCRESULT8 Register (Offset = 10h) [reset = h]

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-335. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4010h

Figure 3-162. CONTROLSS_ADC4_RESULT_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-336. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 8[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

3.2.90 CONTROLSS_ADC4_RESULT_ADCRESULT9 Register (Offset = 12h) [reset = h]

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-337. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4012h

Figure 3-163. CONTROLSS_ADC4_RESULT_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-338. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 9[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

3.2.91 CONTROLSS_ADC4_RESULT_ADCRESULT10 Register (Offset = 14h) [reset = h]

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-339. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4014h

Figure 3-164. CONTROLSS_ADC4_RESULT_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-340. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 10[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

3.2.92 CONTROLSS_ADC4_RESULT_ADCRESULT11 Register (Offset = 16h) [reset = h]

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-341. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4016h

Figure 3-165. CONTROLSS_ADC4_RESULT_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-342. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 11[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

3.2.93 CONTROLSS_ADC4_RESULT_ADCRESULT12 Register (Offset = 18h) [reset = h]

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-343. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4018h

Figure 3-166. CONTROLSS_ADC4_RESULT_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-344. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 12[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

3.2.94 CONTROLSS_ADC4_RESULT_ADCRESULT13 Register (Offset = 1Ah) [reset = h]

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-345. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 401Ah

Figure 3-167. CONTROLSS_ADC4_RESULT_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-346. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 13[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

3.2.95 CONTROLSS_ADC4_RESULT_ADCRESULT14 Register (Offset = 1Ch) [reset = h]

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-347. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 401Ch

Figure 3-168. CONTROLSS_ADC4_RESULT_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-348. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 14[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

3.2.96 CONTROLSS_ADC4_RESULT_ADCRESULT15 Register (Offset = 1Eh) [reset = h]

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-349. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 401Eh

Figure 3-169. CONTROLSS_ADC4_RESULT_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
RO							
0							
7	6	5	4	3	2	1	0
RESULT							
RO							
0							

Access Types Legend

Table 3-350. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	RO	0h	ADC Result 15[[br]] [[br]]16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

3.2.97 CONTROLSS_ADC4_RESULT_ADCPPB1RESULT Register (Offset = 20h) [reset = h]

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-351. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4020h

Figure 3-170. CONTROLSS_ADC4_RESULT_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-352. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 1[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.98 CONTROLSS_ADC4_RESULT_ADCPPB2RESULT Register (Offset = 24h) [reset = h]

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-353. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4024h

Figure 3-171. CONTROLSS_ADC4_RESULT_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-354. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 2[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.99 CONTROLSS_ADC4_RESULT_ADCPPB3RESULT Register (Offset = 28h) [reset = h]

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

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Table 3-355. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 4028h

Figure 3-172. CONTROLSS_ADC4_RESULT_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-356. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 3[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.2.100 CONTROLSS_ADC4_RESULT_ADCPPB4RESULT Register (Offset = 2Ch) [reset = h]

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-357. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC4_RESULT	5010 402Ch

Figure 3-173. CONTROLSS_ADC4_RESULT_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIGN															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPBRESULT															
RO															
0															

Access Types Legend

Table 3-358. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	RO	0h	Sign Extended Bits. These bits reflect the same value as bit 16.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	RO	0h	ADC Post Processing Block Result 4[[br]] [[br]]The result of the offset/reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to ensure that post conversion processing is populated in this register.[[br]] [[br]]NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

Table 3-359. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined

3.3 C2K_CMPSSA Registers

Table 3-360. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
0h	16	CONTROLSS_CMPSSA0_COMPCTL	CMPSS Comparator Control Register	5020 0000h	5020 1000h	5020 2000h
2h	16	CONTROLSS_CMPSSA0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 0002h	5020 1002h	5020 2002h
4h	16	CONTROLSS_CMPSSA0_COMPSTS	CMPSS Comparator Status Register	5020 0004h	5020 1004h	5020 2004h
6h	16	CONTROLSS_CMPSSA0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 0006h	5020 1006h	5020 2006h
8h	16	CONTROLSS_CMPSSA0_COMPDACCTL	CMPSS DAC Control Register	5020 0008h	5020 1008h	5020 2008h
Ah	16	CONTROLSS_CMPSSA0_COMPDACCTL2	CMPSS DAC Control Register 2	5020 000Ah	5020 100Ah	5020 200Ah
Ch	16	CONTROLSS_CMPSSA0_DACHVALS	CMPSS High DAC Value Shadow Register	5020 000Ch	5020 100Ch	5020 200Ch
Eh	16	CONTROLSS_CMPSSA0_DACHVALA	CMPSS High DAC Value Active Register	5020 000Eh	5020 100Eh	5020 200Eh
10h	16	CONTROLSS_CMPSSA0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 0010h	5020 1010h	5020 2010h
14h	16	CONTROLSS_CMPSSA0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 0014h	5020 1014h	5020 2014h
18h	16	CONTROLSS_CMPSSA0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 0018h	5020 1018h	5020 2018h
1Ch	16	CONTROLSS_CMPSSA0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 001Ch	5020 101Ch	5020 201Ch
20h	16	CONTROLSS_CMPSSA0_RAMPSTS	CMPSS Ramp Status Register	5020 0020h	5020 1020h	5020 2020h
24h	16	CONTROLSS_CMPSSA0_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 0024h	5020 1024h	5020 2024h
26h	16	CONTROLSS_CMPSSA0_DACLVALA	CMPSS Low DAC Value Active Register	5020 0026h	5020 1026h	5020 2026h
28h	16	CONTROLSS_CMPSSA0_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 0028h	5020 1028h	5020 2028h
2Ah	16	CONTROLSS_CMPSSA0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 002Ah	5020 102Ah	5020 202Ah
2Ch	16	CONTROLSS_CMPSSA0_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 002Ch	5020 102Ch	5020 202Ch
2Eh	16	CONTROLSS_CMPSSA0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 002Eh	5020 102Eh	5020 202Eh
30h	16	CONTROLSS_CMPSSA0_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 0030h	5020 1030h	5020 2030h

Table 3-360. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
32h	16	CONTROLSS_CMPSSA0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 0032h	5020 1032h	5020 2032h
34h	16	CONTROLSS_CMPSSA0_COMPLOCK	CMPSS Lock Register	5020 0034h	5020 1034h	5020 2034h
38h	16	CONTROLSS_CMPSSA0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 0038h	5020 1038h	5020 2038h
3Ah	16	CONTROLSS_CMPSSA0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 003Ah	5020 103Ah	5020 203Ah
3Ch	16	CONTROLSS_CMPSSA0_CONFIG1	CMPSS Config1 Register	5020 003Ch	5020 103Ch	5020 203Ch

Table 3-361. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
0h	16	CONTROLSS_CMPSSA0_COMPCTL	CMPSS Comparator Control Register	5020 3000h	5020 4000h	5020 5000h
2h	16	CONTROLSS_CMPSSA0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 3002h	5020 4002h	5020 5002h
4h	16	CONTROLSS_CMPSSA0_COMPSTS	CMPSS Comparator Status Register	5020 3004h	5020 4004h	5020 5004h
6h	16	CONTROLSS_CMPSSA0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 3006h	5020 4006h	5020 5006h
8h	16	CONTROLSS_CMPSSA0_COMPDACCTL	CMPSS DAC Control Register	5020 3008h	5020 4008h	5020 5008h
Ah	16	CONTROLSS_CMPSSA0_COMPDACCTL2	CMPSS DAC Control Register 2	5020 300Ah	5020 400Ah	5020 500Ah
Ch	16	CONTROLSS_CMPSSA0_DACHVALS	CMPSS High DAC Value Shadow Register	5020 300Ch	5020 400Ch	5020 500Ch
Eh	16	CONTROLSS_CMPSSA0_DACHVALA	CMPSS High DAC Value Active Register	5020 300Eh	5020 400Eh	5020 500Eh
10h	16	CONTROLSS_CMPSSA0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 3010h	5020 4010h	5020 5010h
14h	16	CONTROLSS_CMPSSA0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 3014h	5020 4014h	5020 5014h
18h	16	CONTROLSS_CMPSSA0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 3018h	5020 4018h	5020 5018h
1Ch	16	CONTROLSS_CMPSSA0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 301Ch	5020 401Ch	5020 501Ch
20h	16	CONTROLSS_CMPSSA0_RAMPSTS	CMPSS Ramp Status Register	5020 3020h	5020 4020h	5020 5020h
24h	16	CONTROLSS_CMPSSA0_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 3024h	5020 4024h	5020 5024h

Table 3-361. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
26h	16	CONTROLSS_CMPSSA0_DACLVALA	CMPSS Low DAC Value Active Register	5020 3026h	5020 4026h	5020 5026h
28h	16	CONTROLSS_CMPSSA0_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 3028h	5020 4028h	5020 5028h
2Ah	16	CONTROLSS_CMPSSA0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 302Ah	5020 402Ah	5020 502Ah
2Ch	16	CONTROLSS_CMPSSA0_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 302Ch	5020 402Ch	5020 502Ch
2Eh	16	CONTROLSS_CMPSSA0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 302Eh	5020 402Eh	5020 502Eh
30h	16	CONTROLSS_CMPSSA0_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 3030h	5020 4030h	5020 5030h
32h	16	CONTROLSS_CMPSSA0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 3032h	5020 4032h	5020 5032h
34h	16	CONTROLSS_CMPSSA0_COMPLOCK	CMPSS Lock Register	5020 3034h	5020 4034h	5020 5034h
38h	16	CONTROLSS_CMPSSA0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 3038h	5020 4038h	5020 5038h
3Ah	16	CONTROLSS_CMPSSA0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 303Ah	5020 403Ah	5020 503Ah
3Ch	16	CONTROLSS_CMPSSA0_CONFIG1	CMPSS Config1 Register	5020 303Ch	5020 403Ch	5020 503Ch

Table 3-362. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
0h	16	CONTROLSS_CMPSSA0_COMPCTL	CMPSS Comparator Control Register	5020 6000h	5020 7000h	5020 8000h
2h	16	CONTROLSS_CMPSSA0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 6002h	5020 7002h	5020 8002h
4h	16	CONTROLSS_CMPSSA0_COMPSTS	CMPSS Comparator Status Register	5020 6004h	5020 7004h	5020 8004h
6h	16	CONTROLSS_CMPSSA0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 6006h	5020 7006h	5020 8006h
8h	16	CONTROLSS_CMPSSA0_COMPDACCTL	CMPSS DAC Control Register	5020 6008h	5020 7008h	5020 8008h
Ah	16	CONTROLSS_CMPSSA0_COMPDACCTL2	CMPSS DAC Control Register 2	5020 600Ah	5020 700Ah	5020 800Ah
Ch	16	CONTROLSS_CMPSSA0_DACHVALS	CMPSS High DAC Value Shadow Register	5020 600Ch	5020 700Ch	5020 800Ch
Eh	16	CONTROLSS_CMPSSA0_DACHVALA	CMPSS High DAC Value Active Register	5020 600Eh	5020 700Eh	5020 800Eh
10h	16	CONTROLSS_CMPSSA0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 6010h	5020 7010h	5020 8010h

Table 3-362. CONTROLSS_CMPSSA0, CONTROLSS_CMPSSA0_CONTROLSS_CMPSSA Registers, Base Address=5020 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
14h	16	CONTROLSS_CMPSSA0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 6014h	5020 7014h	5020 8014h
18h	16	CONTROLSS_CMPSSA0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 6018h	5020 7018h	5020 8018h
1Ch	16	CONTROLSS_CMPSSA0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 601Ch	5020 701Ch	5020 801Ch
20h	16	CONTROLSS_CMPSSA0_RAMPSTS	CMPSS Ramp Status Register	5020 6020h	5020 7020h	5020 8020h
24h	16	CONTROLSS_CMPSSA0_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 6024h	5020 7024h	5020 8024h
26h	16	CONTROLSS_CMPSSA0_DACLVALA	CMPSS Low DAC Value Active Register	5020 6026h	5020 7026h	5020 8026h
28h	16	CONTROLSS_CMPSSA0_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 6028h	5020 7028h	5020 8028h
2Ah	16	CONTROLSS_CMPSSA0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 602Ah	5020 702Ah	5020 802Ah
2Ch	16	CONTROLSS_CMPSSA0_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 602Ch	5020 702Ch	5020 802Ch
2Eh	16	CONTROLSS_CMPSSA0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 602Eh	5020 702Eh	5020 802Eh
30h	16	CONTROLSS_CMPSSA0_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 6030h	5020 7030h	5020 8030h
32h	16	CONTROLSS_CMPSSA0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 6032h	5020 7032h	5020 8032h
34h	16	CONTROLSS_CMPSSA0_COMPLOCK	CMPSS Lock Register	5020 6034h	5020 7034h	5020 8034h
38h	16	CONTROLSS_CMPSSA0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 6038h	5020 7038h	5020 8038h
3Ah	16	CONTROLSS_CMPSSA0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 603Ah	5020 703Ah	5020 803Ah
3Ch	16	CONTROLSS_CMPSSA0_CONFIG1	CMPSS Config1 Register	5020 603Ch	5020 703Ch	5020 803Ch

Table 3-363. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
0h	16	CONTROLSS_CMPSSA1_COMPCTL	CMPSS Comparator Control Register	5020 0000h	5020 1000h	5020 2000h
2h	16	CONTROLSS_CMPSSA1_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 0002h	5020 1002h	5020 2002h
4h	16	CONTROLSS_CMPSSA1_COMPSTS	CMPSS Comparator Status Register	5020 0004h	5020 1004h	5020 2004h
6h	16	CONTROLSS_CMPSSA1_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 0006h	5020 1006h	5020 2006h

Table 3-363. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
8h	16	CONTROLSS_CMPSSA1_COMPDACCTL	CMPSS DAC Control Register	5020 0008h	5020 1008h	5020 2008h
Ah	16	CONTROLSS_CMPSSA1_COMPDACCTL2	CMPSS DAC Control Register 2	5020 000Ah	5020 100Ah	5020 200Ah
Ch	16	CONTROLSS_CMPSSA1_DACHVALS	CMPSS High DAC Value Shadow Register	5020 000Ch	5020 100Ch	5020 200Ch
Eh	16	CONTROLSS_CMPSSA1_DACHVALA	CMPSS High DAC Value Active Register	5020 000Eh	5020 100Eh	5020 200Eh
10h	16	CONTROLSS_CMPSSA1_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 0010h	5020 1010h	5020 2010h
14h	16	CONTROLSS_CMPSSA1_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 0014h	5020 1014h	5020 2014h
18h	16	CONTROLSS_CMPSSA1_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 0018h	5020 1018h	5020 2018h
1Ch	16	CONTROLSS_CMPSSA1_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 001Ch	5020 101Ch	5020 201Ch
20h	16	CONTROLSS_CMPSSA1_RAMPSTS	CMPSS Ramp Status Register	5020 0020h	5020 1020h	5020 2020h
24h	16	CONTROLSS_CMPSSA1_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 0024h	5020 1024h	5020 2024h
26h	16	CONTROLSS_CMPSSA1_DACLVALA	CMPSS Low DAC Value Active Register	5020 0026h	5020 1026h	5020 2026h
28h	16	CONTROLSS_CMPSSA1_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 0028h	5020 1028h	5020 2028h
2Ah	16	CONTROLSS_CMPSSA1_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 002Ah	5020 102Ah	5020 202Ah
2Ch	16	CONTROLSS_CMPSSA1_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 002Ch	5020 102Ch	5020 202Ch
2Eh	16	CONTROLSS_CMPSSA1_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 002Eh	5020 102Eh	5020 202Eh
30h	16	CONTROLSS_CMPSSA1_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 0030h	5020 1030h	5020 2030h
32h	16	CONTROLSS_CMPSSA1_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 0032h	5020 1032h	5020 2032h
34h	16	CONTROLSS_CMPSSA1_COMPLOCK	CMPSS Lock Register	5020 0034h	5020 1034h	5020 2034h
38h	16	CONTROLSS_CMPSSA1_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 0038h	5020 1038h	5020 2038h
3Ah	16	CONTROLSS_CMPSSA1_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 003Ah	5020 103Ah	5020 203Ah
3Ch	16	CONTROLSS_CMPSSA1_CONFIG1	CMPSS Config1 Register	5020 003Ch	5020 103Ch	5020 203Ch

Table 3-364. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
0h	16	CONTROLSS_CMPSSA1_COMPCTL	CMPSS Comparator Control Register	5020 3000h	5020 4000h	5020 5000h
2h	16	CONTROLSS_CMPSSA1_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 3002h	5020 4002h	5020 5002h
4h	16	CONTROLSS_CMPSSA1_COMPSTS	CMPSS Comparator Status Register	5020 3004h	5020 4004h	5020 5004h
6h	16	CONTROLSS_CMPSSA1_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 3006h	5020 4006h	5020 5006h
8h	16	CONTROLSS_CMPSSA1_COMPDACCTL	CMPSS DAC Control Register	5020 3008h	5020 4008h	5020 5008h
Ah	16	CONTROLSS_CMPSSA1_COMPDACCTL2	CMPSS DAC Control Register 2	5020 300Ah	5020 400Ah	5020 500Ah
Ch	16	CONTROLSS_CMPSSA1_DACHVALS	CMPSS High DAC Value Shadow Register	5020 300Ch	5020 400Ch	5020 500Ch
Eh	16	CONTROLSS_CMPSSA1_DACHVALA	CMPSS High DAC Value Active Register	5020 300Eh	5020 400Eh	5020 500Eh
10h	16	CONTROLSS_CMPSSA1_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 3010h	5020 4010h	5020 5010h
14h	16	CONTROLSS_CMPSSA1_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 3014h	5020 4014h	5020 5014h
18h	16	CONTROLSS_CMPSSA1_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 3018h	5020 4018h	5020 5018h
1Ch	16	CONTROLSS_CMPSSA1_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 301Ch	5020 401Ch	5020 501Ch
20h	16	CONTROLSS_CMPSSA1_RAMPSTS	CMPSS Ramp Status Register	5020 3020h	5020 4020h	5020 5020h
24h	16	CONTROLSS_CMPSSA1_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 3024h	5020 4024h	5020 5024h
26h	16	CONTROLSS_CMPSSA1_DACLVALA	CMPSS Low DAC Value Active Register	5020 3026h	5020 4026h	5020 5026h
28h	16	CONTROLSS_CMPSSA1_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 3028h	5020 4028h	5020 5028h
2Ah	16	CONTROLSS_CMPSSA1_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 302Ah	5020 402Ah	5020 502Ah
2Ch	16	CONTROLSS_CMPSSA1_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 302Ch	5020 402Ch	5020 502Ch
2Eh	16	CONTROLSS_CMPSSA1_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 302Eh	5020 402Eh	5020 502Eh
30h	16	CONTROLSS_CMPSSA1_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 3030h	5020 4030h	5020 5030h
32h	16	CONTROLSS_CMPSSA1_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 3032h	5020 4032h	5020 5032h
34h	16	CONTROLSS_CMPSSA1_COMPLOCK	CMPSS Lock Register	5020 3034h	5020 4034h	5020 5034h
38h	16	CONTROLSS_CMPSSA1_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 3038h	5020 4038h	5020 5038h

Table 3-364. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
3Ah	16	CONTROLSS_CMPSSA1_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 303Ah	5020 403Ah	5020 503Ah
3Ch	16	CONTROLSS_CMPSSA1_CONFIG1	CMPSS Config1 Register	5020 303Ch	5020 403Ch	5020 503Ch

Table 3-365. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
0h	16	CONTROLSS_CMPSSA1_COMPCTL	CMPSS Comparator Control Register	5020 6000h	5020 7000h	5020 8000h
2h	16	CONTROLSS_CMPSSA1_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5020 6002h	5020 7002h	5020 8002h
4h	16	CONTROLSS_CMPSSA1_COMPSTS	CMPSS Comparator Status Register	5020 6004h	5020 7004h	5020 8004h
6h	16	CONTROLSS_CMPSSA1_COMPSTSCLR	CMPSS Comparator Status Clear Register	5020 6006h	5020 7006h	5020 8006h
8h	16	CONTROLSS_CMPSSA1_COMPDACCTL	CMPSS DAC Control Register	5020 6008h	5020 7008h	5020 8008h
Ah	16	CONTROLSS_CMPSSA1_COMPDACCTL2	CMPSS DAC Control Register 2	5020 600Ah	5020 700Ah	5020 800Ah
Ch	16	CONTROLSS_CMPSSA1_DACHVALS	CMPSS High DAC Value Shadow Register	5020 600Ch	5020 700Ch	5020 800Ch
Eh	16	CONTROLSS_CMPSSA1_DACHVALA	CMPSS High DAC Value Active Register	5020 600Eh	5020 700Eh	5020 800Eh
10h	16	CONTROLSS_CMPSSA1_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5020 6010h	5020 7010h	5020 8010h
14h	16	CONTROLSS_CMPSSA1_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5020 6014h	5020 7014h	5020 8014h
18h	16	CONTROLSS_CMPSSA1_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5020 6018h	5020 7018h	5020 8018h
1Ch	16	CONTROLSS_CMPSSA1_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5020 601Ch	5020 701Ch	5020 801Ch
20h	16	CONTROLSS_CMPSSA1_RAMPSTS	CMPSS Ramp Status Register	5020 6020h	5020 7020h	5020 8020h
24h	16	CONTROLSS_CMPSSA1_DACLVALS	CMPSS Low DAC Value Shadow Register	5020 6024h	5020 7024h	5020 8024h
26h	16	CONTROLSS_CMPSSA1_DACLVALA	CMPSS Low DAC Value Active Register	5020 6026h	5020 7026h	5020 8026h
28h	16	CONTROLSS_CMPSSA1_RAMPDLYA	CMPSS Ramp Delay Active Register	5020 6028h	5020 7028h	5020 8028h
2Ah	16	CONTROLSS_CMPSSA1_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5020 602Ah	5020 702Ah	5020 802Ah
2Ch	16	CONTROLSS_CMPSSA1_CTRIPLFILCTL	CTRIPL Filter Control Register	5020 602Ch	5020 702Ch	5020 802Ch

Table 3-365. CONTROLSS_CMPSSA1, CONTROLSS_CMPSSA1_CONTROLSS_CMPSSA Registers, Base Address=5020 1000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
2Eh	16	CONTROLSS_CMPSSA1_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5020 602Eh	5020 702Eh	5020 802Eh
30h	16	CONTROLSS_CMPSSA1_CTRIPHFILCTL	CTRIPH Filter Control Register	5020 6030h	5020 7030h	5020 8030h
32h	16	CONTROLSS_CMPSSA1_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5020 6032h	5020 7032h	5020 8032h
34h	16	CONTROLSS_CMPSSA1_COMPLOCK	CMPSS Lock Register	5020 6034h	5020 7034h	5020 8034h
38h	16	CONTROLSS_CMPSSA1_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5020 6038h	5020 7038h	5020 8038h
3Ah	16	CONTROLSS_CMPSSA1_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5020 603Ah	5020 703Ah	5020 803Ah
3Ch	16	CONTROLSS_CMPSSA1_CONFIG1	CMPSS Config1 Register	5020 603Ch	5020 703Ch	5020 803Ch

3.3.1 CONTROLSS_CMPSSA0_COMPCTL Register (Offset = 0h) [reset = h]

Short Description: CMPSS Comparator Control Register

Long Description:

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Table 3-366. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0000h
CONTROLSS_CMPSSA1	5020 1000h
CONTROLSS_CMPSSA2	5020 2000h
CONTROLSS_CMPSSA3	5020 3000h
CONTROLSS_CMPSSA4	5020 4000h
CONTROLSS_CMPSSA5	5020 5000h
CONTROLSS_CMPSSA6	5020 6000h
CONTROLSS_CMPSSA7	5020 7000h
CONTROLSS_CMPSSA8	5020 8000h
CONTROLSS_CMPSSA9	5020 9000h

Figure 3-174. CONTROLSS_CMPSSA0_COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	COMPLSOURCE
RW	RW	RW		RW		RW	RW
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	COMPHSOURCE
RO	RW	RW		RW		RW	RW
0	0	0		0		0	0

Access Types Legend

Table 3-367. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	RW	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	RW	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13 - 12	CTRIPOUTLSEL	RW	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11 - 10	CTRIPLSEL	RW	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	RW	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	COMPLSOURCE	RW	0h	CompL Pos Mux Select0 positive mux selects INL_3p3v voltage (default)1 postive mux selects INH_3p3v
7	RESERVED	RO		Reserved

Table 3-367. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ASYNCHEN	RW	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5 - 4	CTRIPOUTHSEL	RW	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH
3 - 2	CTRIPHSEL	RW	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	RW	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	COMPHSOURCE	RW	0h	CompH neg Mux slect0 negative mux selects DAC voltage (default)1 negative mux selects INL_3p3v

3.3.2 CONTROLSS_CMPSSA0_COMPHYSCTL Register (Offset = 2h) [reset = h]

Short Description: CMPSS Comparator Hysteresis Control Register

Long Description:

Return to Summary Table

Table 3-368. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0002h
CONTROLSS_CMPSSA1	5020 1002h
CONTROLSS_CMPSSA2	5020 2002h
CONTROLSS_CMPSSA3	5020 3002h
CONTROLSS_CMPSSA4	5020 4002h
CONTROLSS_CMPSSA5	5020 5002h
CONTROLSS_CMPSSA6	5020 6002h
CONTROLSS_CMPSSA7	5020 7002h
CONTROLSS_CMPSSA8	5020 8002h
CONTROLSS_CMPSSA9	5020 9002h

Figure 3-175. CONTROLSS_CMPSSA0_COMPHYSCTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				COMPHYS			
RO				RW			
0				0			

Access Types Legend

Table 3-369. COMPHYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	COMPHYS	RW	0h	Comparator hysteresis. Sets the amount of hysteresis on the comparator inputs. 0 None 1 Set to typical hysteresis 2 Set to 2x of typical hysteresis 3 Set to 3x of typical hysteresis 4 Set to 4x of typical hysteresis others : undefined

3.3.3 CONTROLSS_CMPSSA0_COMPSTS Register (Offset = 4h) [reset = h]

Short Description: CMPSS Comparator Status Register

Long Description:

Return to Summary Table

Table 3-370. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0004h
CONTROLSS_CMPSSA1	5020 1004h
CONTROLSS_CMPSSA2	5020 2004h
CONTROLSS_CMPSSA3	5020 3004h
CONTROLSS_CMPSSA4	5020 4004h
CONTROLSS_CMPSSA5	5020 5004h
CONTROLSS_CMPSSA6	5020 6004h
CONTROLSS_CMPSSA7	5020 7004h
CONTROLSS_CMPSSA8	5020 8004h
CONTROLSS_CMPSSA9	5020 9004h

Figure 3-176. CONTROLSS_CMPSSA0_COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED						COMPLLATCH	COMPLSTS
RO						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED						COMPHLATCH	COMPHSTS
RO						RO	RO
0						0	0

Access Types Legend

Table 3-371. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	COMPLLATCH	RO	0h	Latched value of low comparator digital filter output
8	COMPLSTS	RO	0h	Low comparator digital filter output
7 - 2	RESERVED	RO		Reserved
1	COMPHLATCH	RO	0h	Latched value of high comparator digital filter output
0	COMPHSTS	RO	0h	High comparator digital filter output

3.3.4 CONTROLSS_CMPSSA0_COMPSTSCLR Register (Offset = 6h) [reset = h]

Short Description: CMPSS Comparator Status Clear Register

Long Description:

Return to Summary Table

Table 3-372. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0006h
CONTROLSS_CMPSSA1	5020 1006h
CONTROLSS_CMPSSA2	5020 2006h
CONTROLSS_CMPSSA3	5020 3006h
CONTROLSS_CMPSSA4	5020 4006h
CONTROLSS_CMPSSA5	5020 5006h
CONTROLSS_CMPSSA6	5020 6006h
CONTROLSS_CMPSSA7	5020 7006h
CONTROLSS_CMPSSA8	5020 8006h
CONTROLSS_CMPSSA9	5020 9006h

Figure 3-177. CONTROLSS_CMPSSA0_COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED					LSYNCCLREN	LLATCHCLR	RESERVED
RO					RW	RW RRETURNS0S	RO
0					0	0	0
7	6	5	4	3	2	1	0
RESERVED					HSYNCCLREN	HLATCHCLR	RESERVED
RO					RW	RW RRETURNS0S	RO
0					0	0	0

Access Types Legend

Table 3-373. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	LSYNCCLREN	RW	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	RW RRETURNS 0S	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8 - 3	RESERVED	RO		Reserved
2	HSYNCCLREN	RW	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	RW RRETURNS 0S	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]
0	RESERVED	RO		Reserved

3.3.5 CONTROLSS_CMPSSA0_COMPDACCTL Register (Offset = 8h) [reset = h]

Short Description: CMPSS DAC Control Register

Long Description:

Return to Summary Table

Table 3-374. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0008h
CONTROLSS_CMPSSA1	5020 1008h
CONTROLSS_CMPSSA2	5020 2008h
CONTROLSS_CMPSSA3	5020 3008h
CONTROLSS_CMPSSA4	5020 4008h
CONTROLSS_CMPSSA5	5020 5008h
CONTROLSS_CMPSSA6	5020 6008h
CONTROLSS_CMPSSA7	5020 7008h
CONTROLSS_CMPSSA8	5020 8008h
CONTROLSS_CMPSSA9	5020 9008h

Figure 3-178. CONTROLSS_CMPSSA0_COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED	BLANKEN	BLANKSOURCE			
RW		RO	RW	RW			
0		0	0	0			
7	6	5	4	3	2	1	0
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
RW	RW	RW	RW				RW
0	0	0	0				0

Access Types Legend

Table 3-375. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREESOFT	RW	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED	RO		Reserved
12	BLANKEN	RW	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11 - 8	BLANKSOURCE	RW	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK
7	SWLOADSEL	RW	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER
6	RAMPLOADSEL	RW	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS

Table 3-375. COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SELREF	RW	0h	CMPSS reference select0 vref_1p8v as reference voltage (default)1 vdd_1p8v as reference voltage
4 - 1	RAMPSOURCE	RW	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	RW	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

3.3.6 CONTROLSS_CMPSSA0_COMPDACCTL2 Register (Offset = Ah) [reset = h]

Short Description: CMPSS DAC Control Register 2

Long Description:

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Table 3-376. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ah
CONTROLSS_CMPSSA1	5020 100Ah
CONTROLSS_CMPSSA2	5020 200Ah
CONTROLSS_CMPSSA3	5020 300Ah
CONTROLSS_CMPSSA4	5020 400Ah
CONTROLSS_CMPSSA5	5020 500Ah
CONTROLSS_CMPSSA6	5020 600Ah
CONTROLSS_CMPSSA7	5020 700Ah
CONTROLSS_CMPSSA8	5020 800Ah
CONTROLSS_CMPSSA9	5020 900Ah

Figure 3-179. CONTROLSS_CMPSSA0_COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED					RAMPSOURCEUSEL	RESERVED	BLANKSOURCEUSEL
RO					RW	RO	RW
0					0	0	0
7	6	5	4	3	2	1	0
RESERVED		DEACTIVESEL					DEENABLE
RO		RW					RW
0		0					0

Access Types Legend

Table 3-377. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	RAMPSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source
9	RESERVED	RO		Reserved
8	BLANKSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source
7 - 6	RESERVED	RO		Reserved
5 - 1	DEACTIVESEL	RW	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE
0	DEENABLE	RW	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

3.3.7 CONTROLSS_CMPSSA0_DACHVALS Register (Offset = Ch) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-378. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ch
CONTROLSS_CMPSSA1	5020 100Ch
CONTROLSS_CMPSSA2	5020 200Ch
CONTROLSS_CMPSSA3	5020 300Ch
CONTROLSS_CMPSSA4	5020 400Ch
CONTROLSS_CMPSSA5	5020 500Ch
CONTROLSS_CMPSSA6	5020 600Ch
CONTROLSS_CMPSSA7	5020 700Ch
CONTROLSS_CMPSSA8	5020 800Ch
CONTROLSS_CMPSSA9	5020 900Ch

Figure 3-180. CONTROLSS_CMPSSA0_DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-379. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

3.3.8 CONTROLSS_CMPSSA0_DACHVALA Register (Offset = Eh) [reset = h]

Short Description: CMPSS High DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-380. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Eh
CONTROLSS_CMPSSA1	5020 100Eh
CONTROLSS_CMPSSA2	5020 200Eh
CONTROLSS_CMPSSA3	5020 300Eh
CONTROLSS_CMPSSA4	5020 400Eh
CONTROLSS_CMPSSA5	5020 500Eh
CONTROLSS_CMPSSA6	5020 600Eh
CONTROLSS_CMPSSA7	5020 700Eh
CONTROLSS_CMPSSA8	5020 800Eh
CONTROLSS_CMPSSA9	5020 900Eh

Figure 3-181. CONTROLSS_CMPSSA0_DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RO							
0							

Access Types Legend

Table 3-381. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	High DAC active value. Value that is actively driven by the high DAC.

3.3.9 CONTROLSS_CMPSSA0_RAMPMAXREFA Register (Offset = 10h) [reset = h]

Short Description: CMPSS Ramp Max Reference Active Register

Long Description:

Return to Summary Table

Table 3-382. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0010h
CONTROLSS_CMPSSA1	5020 1010h
CONTROLSS_CMPSSA2	5020 2010h
CONTROLSS_CMPSSA3	5020 3010h
CONTROLSS_CMPSSA4	5020 4010h
CONTROLSS_CMPSSA5	5020 5010h
CONTROLSS_CMPSSA6	5020 6010h
CONTROLSS_CMPSSA7	5020 7010h
CONTROLSS_CMPSSA8	5020 8010h
CONTROLSS_CMPSSA9	5020 9010h

Figure 3-182. CONTROLSS_CMPSSA0_RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
RO							
0							
7	6	5	4	3	2	1	0
RAMPMAXREF							
RO							
0							

Access Types Legend

Table 3-383. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RO	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

3.3.10 CONTROLSS_CMPSSA0_RAMPMAXREFS Register (Offset = 14h) [reset = h]

Short Description: CMPSS Ramp Max Reference Shadow Register

Long Description:

Return to Summary Table

Table 3-384. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0014h
CONTROLSS_CMPSSA1	5020 1014h
CONTROLSS_CMPSSA2	5020 2014h
CONTROLSS_CMPSSA3	5020 3014h
CONTROLSS_CMPSSA4	5020 4014h
CONTROLSS_CMPSSA5	5020 5014h
CONTROLSS_CMPSSA6	5020 6014h
CONTROLSS_CMPSSA7	5020 7014h
CONTROLSS_CMPSSA8	5020 8014h
CONTROLSS_CMPSSA9	5020 9014h

Figure 3-183. CONTROLSS_CMPSSA0_RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
RW							
0							
7	6	5	4	3	2	1	0
RAMPMAXREF							
RW							
0							

Access Types Legend

Table 3-385. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RW	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

3.3.11 CONTROLSS_CMPSSA0_RAMPDECVALA Register (Offset = 18h) [reset = h]

Short Description: CMPSS Ramp Decrement Value Active Register

Long Description:

Return to Summary Table

Table 3-386. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0018h
CONTROLSS_CMPSSA1	5020 1018h
CONTROLSS_CMPSSA2	5020 2018h
CONTROLSS_CMPSSA3	5020 3018h
CONTROLSS_CMPSSA4	5020 4018h
CONTROLSS_CMPSSA5	5020 5018h
CONTROLSS_CMPSSA6	5020 6018h
CONTROLSS_CMPSSA7	5020 7018h
CONTROLSS_CMPSSA8	5020 8018h
CONTROLSS_CMPSSA9	5020 9018h

Figure 3-184. CONTROLSS_CMPSSA0_RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
RO							
0							
7	6	5	4	3	2	1	0
RAMPDECVAL							
RO							
0							

Access Types Legend

Table 3-387. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RO	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

3.3.12 CONTROLSS_CMPSSA0_RAMPDECVALS Register (Offset = 1Ch) [reset = h]

Short Description: CMPSS Ramp Decrement Value Shadow Register

Long Description:

Return to Summary Table

Table 3-388. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 001Ch
CONTROLSS_CMPSSA1	5020 101Ch
CONTROLSS_CMPSSA2	5020 201Ch
CONTROLSS_CMPSSA3	5020 301Ch
CONTROLSS_CMPSSA4	5020 401Ch
CONTROLSS_CMPSSA5	5020 501Ch
CONTROLSS_CMPSSA6	5020 601Ch
CONTROLSS_CMPSSA7	5020 701Ch
CONTROLSS_CMPSSA8	5020 801Ch
CONTROLSS_CMPSSA9	5020 901Ch

Figure 3-185. CONTROLSS_CMPSSA0_RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
RW							
0							
7	6	5	4	3	2	1	0
RAMPDECVAL							
RW							
0							

Access Types Legend

Table 3-389. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RW	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

3.3.13 CONTROLSS_CMPSSA0_RAMPSTS Register (Offset = 20h) [reset = h]

Short Description: CMPSS Ramp Status Register

Long Description:

Return to Summary Table

Table 3-390. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0020h
CONTROLSS_CMPSSA1	5020 1020h
CONTROLSS_CMPSSA2	5020 2020h
CONTROLSS_CMPSSA3	5020 3020h
CONTROLSS_CMPSSA4	5020 4020h
CONTROLSS_CMPSSA5	5020 5020h
CONTROLSS_CMPSSA6	5020 6020h
CONTROLSS_CMPSSA7	5020 7020h
CONTROLSS_CMPSSA8	5020 8020h
CONTROLSS_CMPSSA9	5020 9020h

Figure 3-186. CONTROLSS_CMPSSA0_RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
RO							
0							
7	6	5	4	3	2	1	0
RAMPVALUE							
RO							
0							

Access Types Legend

Table 3-391. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPVALUE	RO	0h	Ramp value. Present value of ramp generator.

3.3.14 CONTROLSS_CMPSSA0_DACLVALS Register (Offset = 24h) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-392. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0024h
CONTROLSS_CMPSSA1	5020 1024h
CONTROLSS_CMPSSA2	5020 2024h
CONTROLSS_CMPSSA3	5020 3024h
CONTROLSS_CMPSSA4	5020 4024h
CONTROLSS_CMPSSA5	5020 5024h
CONTROLSS_CMPSSA6	5020 6024h
CONTROLSS_CMPSSA7	5020 7024h
CONTROLSS_CMPSSA8	5020 8024h
CONTROLSS_CMPSSA9	5020 9024h

Figure 3-187. CONTROLSS_CMPSSA0_DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-393. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

3.3.15 CONTROLSS_CMPSSA0_DACLVALA Register (Offset = 26h) [reset = h]

Short Description: CMPSS Low DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-394. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0026h
CONTROLSS_CMPSSA1	5020 1026h
CONTROLSS_CMPSSA2	5020 2026h
CONTROLSS_CMPSSA3	5020 3026h
CONTROLSS_CMPSSA4	5020 4026h
CONTROLSS_CMPSSA5	5020 5026h
CONTROLSS_CMPSSA6	5020 6026h
CONTROLSS_CMPSSA7	5020 7026h
CONTROLSS_CMPSSA8	5020 8026h
CONTROLSS_CMPSSA9	5020 9026h

Figure 3-188. CONTROLSS_CMPSSA0_DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RO							
0							

Access Types Legend

Table 3-395. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	Low DAC active value. Value that is actively driven by the low DAC.

3.3.16 CONTROLSS_CMPSSA0_RAMPDLYA Register (Offset = 28h) [reset = h]

Short Description: CMPSS Ramp Delay Active Register

Long Description:

Return to Summary Table

Table 3-396. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0028h
CONTROLSS_CMPSSA1	5020 1028h
CONTROLSS_CMPSSA2	5020 2028h
CONTROLSS_CMPSSA3	5020 3028h
CONTROLSS_CMPSSA4	5020 4028h
CONTROLSS_CMPSSA5	5020 5028h
CONTROLSS_CMPSSA6	5020 6028h
CONTROLSS_CMPSSA7	5020 7028h
CONTROLSS_CMPSSA8	5020 8028h
CONTROLSS_CMPSSA9	5020 9028h

Figure 3-189. CONTROLSS_CMPSSA0_RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED			DELAY				
RO			RO				
0			0				
7	6	5	4	3	2	1	0
DELAY							
RO							
0							

Access Types Legend

Table 3-397. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RO	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

3.3.17 CONTROLSS_CMPSSA0_RAMPDLYS Register (Offset = 2Ah) [reset = h]

Short Description: CMPSS Ramp Delay Shadow Register

Long Description:

Return to Summary Table

Table 3-398. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ah
CONTROLSS_CMPSSA1	5020 102Ah
CONTROLSS_CMPSSA2	5020 202Ah
CONTROLSS_CMPSSA3	5020 302Ah
CONTROLSS_CMPSSA4	5020 402Ah
CONTROLSS_CMPSSA5	5020 502Ah
CONTROLSS_CMPSSA6	5020 602Ah
CONTROLSS_CMPSSA7	5020 702Ah
CONTROLSS_CMPSSA8	5020 802Ah
CONTROLSS_CMPSSA9	5020 902Ah

Figure 3-190. CONTROLSS_CMPSSA0_RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED			DELAY				
RO			RW				
0			0				
7	6	5	4	3	2	1	0
DELAY							
RW							
0							

Access Types Legend

Table 3-399. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RW	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

3.3.18 CONTROLSS_CMPSSA0_CTRIPLFILCTL Register (Offset = 2Ch) [reset = h]

Short Description: CTRIPL Filter Control Register

Long Description:

Return to Summary Table

Table 3-400. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ch
CONTROLSS_CMPSSA1	5020 102Ch
CONTROLSS_CMPSSA2	5020 202Ch
CONTROLSS_CMPSSA3	5020 302Ch
CONTROLSS_CMPSSA4	5020 402Ch
CONTROLSS_CMPSSA5	5020 502Ch
CONTROLSS_CMPSSA6	5020 602Ch
CONTROLSS_CMPSSA7	5020 702Ch
CONTROLSS_CMPSSA8	5020 802Ch
CONTROLSS_CMPSSA9	5020 902Ch

Figure 3-191. CONTROLSS_CMPSSA0_CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-401. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.3.19 CONTROLSS_CMPSSA0_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = h]

Short Description: CTRIPL Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-402. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Eh
CONTROLSS_CMPSSA1	5020 102Eh
CONTROLSS_CMPSSA2	5020 202Eh
CONTROLSS_CMPSSA3	5020 302Eh
CONTROLSS_CMPSSA4	5020 402Eh
CONTROLSS_CMPSSA5	5020 502Eh
CONTROLSS_CMPSSA6	5020 602Eh
CONTROLSS_CMPSSA7	5020 702Eh
CONTROLSS_CMPSSA8	5020 802Eh
CONTROLSS_CMPSSA9	5020 902Eh

Figure 3-192. CONTROLSS_CMPSSA0_CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
RW							
0							
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-403. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

3.3.20 CONTROLSS_CMPSSA0_CTRIPHFILCTL Register (Offset = 30h) [reset = h]

Short Description: CTRIPH Filter Control Register

Long Description:

Return to Summary Table

Table 3-404. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0030h
CONTROLSS_CMPSSA1	5020 1030h
CONTROLSS_CMPSSA2	5020 2030h
CONTROLSS_CMPSSA3	5020 3030h
CONTROLSS_CMPSSA4	5020 4030h
CONTROLSS_CMPSSA5	5020 5030h
CONTROLSS_CMPSSA6	5020 6030h
CONTROLSS_CMPSSA7	5020 7030h
CONTROLSS_CMPSSA8	5020 8030h
CONTROLSS_CMPSSA9	5020 9030h

Figure 3-193. CONTROLSS_CMPSSA0_CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-405. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.3.21 CONTROLSS_CMPSSA0_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = h]

Short Description: CTRIPH Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-406. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0032h
CONTROLSS_CMPSSA1	5020 1032h
CONTROLSS_CMPSSA2	5020 2032h
CONTROLSS_CMPSSA3	5020 3032h
CONTROLSS_CMPSSA4	5020 4032h
CONTROLSS_CMPSSA5	5020 5032h
CONTROLSS_CMPSSA6	5020 6032h
CONTROLSS_CMPSSA7	5020 7032h
CONTROLSS_CMPSSA8	5020 8032h
CONTROLSS_CMPSSA9	5020 9032h

Figure 3-194. CONTROLSS_CMPSSA0_CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
RW							
0							
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-407. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

3.3.22 CONTROLSS_CMPSSA0_COMPLOCK Register (Offset = 34h) [reset = h]

Short Description: CMPSS Lock Register

Long Description:

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Table 3-408. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0034h
CONTROLSS_CMPSSA1	5020 1034h
CONTROLSS_CMPSSA2	5020 2034h
CONTROLSS_CMPSSA3	5020 3034h
CONTROLSS_CMPSSA4	5020 4034h
CONTROLSS_CMPSSA5	5020 5034h
CONTROLSS_CMPSSA6	5020 6034h
CONTROLSS_CMPSSA7	5020 7034h
CONTROLSS_CMPSSA8	5020 8034h
CONTROLSS_CMPSSA9	5020 9034h

Figure 3-195. CONTROLSS_CMPSSA0_COMPLOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			TEST	CTRIP	DACCTL	COMPHYSCTL	COMPCTL
RO			RW SONCE	RW SONCE	RW SONCE	RW SONCE	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-409. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	TEST	RW SONCE	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	RW SONCE	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	RW SONCE	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	RW SONCE	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

3.3.23 CONTROLSS_CMPSSA0_DACHVALS2 Register (Offset = 38h) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register 2

Long Description:

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Table 3-410. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0038h
CONTROLSS_CMPSSA1	5020 1038h
CONTROLSS_CMPSSA2	5020 2038h
CONTROLSS_CMPSSA3	5020 3038h
CONTROLSS_CMPSSA4	5020 4038h
CONTROLSS_CMPSSA5	5020 5038h
CONTROLSS_CMPSSA6	5020 6038h
CONTROLSS_CMPSSA7	5020 7038h
CONTROLSS_CMPSSA8	5020 8038h
CONTROLSS_CMPSSA9	5020 9038h

Figure 3-196. CONTROLSS_CMPSSA0_DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-411. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

3.3.24 CONTROLSS_CMPSSA0_DACLVALS2 Register (Offset = 3Ah) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register 2

Long Description:

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Table 3-412. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ah
CONTROLSS_CMPSSA1	5020 103Ah
CONTROLSS_CMPSSA2	5020 203Ah
CONTROLSS_CMPSSA3	5020 303Ah
CONTROLSS_CMPSSA4	5020 403Ah
CONTROLSS_CMPSSA5	5020 503Ah
CONTROLSS_CMPSSA6	5020 603Ah
CONTROLSS_CMPSSA7	5020 703Ah
CONTROLSS_CMPSSA8	5020 803Ah
CONTROLSS_CMPSSA9	5020 903Ah

Figure 3-197. CONTROLSS_CMPSSA0_DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-413. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

3.3.25 CONTROLSS_CMPSSA0_CONFIG1 Register (Offset = 3Ch) [reset = h]

Short Description: CMPSS Config1 Register

Long Description:

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Table 3-414. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ch
CONTROLSS_CMPSSA1	5020 103Ch
CONTROLSS_CMPSSA2	5020 203Ch
CONTROLSS_CMPSSA3	5020 303Ch
CONTROLSS_CMPSSA4	5020 403Ch
CONTROLSS_CMPSSA5	5020 503Ch
CONTROLSS_CMPSSA6	5020 603Ch
CONTROLSS_CMPSSA7	5020 703Ch
CONTROLSS_CMPSSA8	5020 803Ch
CONTROLSS_CMPSSA9	5020 903Ch

Figure 3-198. CONTROLSS_CMPSSA0_CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
RW							
0							
7	6	5	4	3	2	1	0
COMPLHYS				COMPHHYS			
RW				RW			
0				0			

Access Types Legend

Table 3-415. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	SPARE	RW	0h	SPARE
7 - 4	COMPLHYS	RW	0h	compL Hysterisishystl_1p1v[3] = reservedhystl_1p1v[2] = control which comparator output value the hysteresis is applied tohystl_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB
3 - 0	COMPHHYS	RW	0h	CompH Hysteresishysth_1p1v[3] = reservedhysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b11 comparator hysteresis is applied when the comparator output is 1'b0hysth_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB

Table 3-416. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RW SONCE	RW SONCE	Undefined

3.4 C2K_CMPSSB Registers

Table 3-417. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB0 Physical Address	CONTROLSS_CMPSSB1 Physical Address	CONTROLSS_CMPSSB2 Physical Address
0h	16	CONTROLSS_CMPSSB0_COMPCTL	CMPSS Comparator Control Register	5022 0000h	5022 1000h	5022 2000h
2h	16	CONTROLSS_CMPSSB0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5022 0002h	5022 1002h	5022 2002h
4h	16	CONTROLSS_CMPSSB0_COMPSTS	CMPSS Comparator Status Register	5022 0004h	5022 1004h	5022 2004h
6h	16	CONTROLSS_CMPSSB0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5022 0006h	5022 1006h	5022 2006h
8h	16	CONTROLSS_CMPSSB0_COMPDACCTL	CMPSS DAC Control Register	5022 0008h	5022 1008h	5022 2008h
Ah	16	CONTROLSS_CMPSSB0_COMPDACCTL2	CMPSS DAC Control Register 2	5022 000Ah	5022 100Ah	5022 200Ah
Ch	16	CONTROLSS_CMPSSB0_DACHVALS	CMPSS High DAC Value Shadow Register	5022 000Ch	5022 100Ch	5022 200Ch
Eh	16	CONTROLSS_CMPSSB0_DACHVALA	CMPSS High DAC Value Active Register	5022 000Eh	5022 100Eh	5022 200Eh
10h	16	CONTROLSS_CMPSSB0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5022 0010h	5022 1010h	5022 2010h
14h	16	CONTROLSS_CMPSSB0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5022 0014h	5022 1014h	5022 2014h
18h	16	CONTROLSS_CMPSSB0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5022 0018h	5022 1018h	5022 2018h
1Ch	16	CONTROLSS_CMPSSB0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5022 001Ch	5022 101Ch	5022 201Ch
20h	16	CONTROLSS_CMPSSB0_RAMPSTS	CMPSS Ramp Status Register	5022 0020h	5022 1020h	5022 2020h
24h	16	CONTROLSS_CMPSSB0_DACLVALS	CMPSS Low DAC Value Shadow Register	5022 0024h	5022 1024h	5022 2024h
26h	16	CONTROLSS_CMPSSB0_DACLVALA	CMPSS Low DAC Value Active Register	5022 0026h	5022 1026h	5022 2026h
28h	16	CONTROLSS_CMPSSB0_RAMPDLYA	CMPSS Ramp Delay Active Register	5022 0028h	5022 1028h	5022 2028h
2Ah	16	CONTROLSS_CMPSSB0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5022 002Ah	5022 102Ah	5022 202Ah
2Ch	16	CONTROLSS_CMPSSB0_CTRIPLFILCTL	CTRIPL Filter Control Register	5022 002Ch	5022 102Ch	5022 202Ch

Table 3-417. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB0 Physical Address	CONTROLSS_CMPSSB1 Physical Address	CONTROLSS_CMPSSB2 Physical Address
2Eh	16	CONTROLSS_CMPSSB0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5022 002Eh	5022 102Eh	5022 202Eh
30h	16	CONTROLSS_CMPSSB0_CTRIPHFILCTL	CTRIPH Filter Control Register	5022 0030h	5022 1030h	5022 2030h
32h	16	CONTROLSS_CMPSSB0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5022 0032h	5022 1032h	5022 2032h
34h	16	CONTROLSS_CMPSSB0_COMPLOCK	CMPSS Lock Register	5022 0034h	5022 1034h	5022 2034h
38h	16	CONTROLSS_CMPSSB0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5022 0038h	5022 1038h	5022 2038h
3Ah	16	CONTROLSS_CMPSSB0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5022 003Ah	5022 103Ah	5022 203Ah
3Ch	16	CONTROLSS_CMPSSB0_CONFIG1	CMPSS Config1 Register	5022 003Ch	5022 103Ch	5022 203Ch

Table 3-418. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB3 Physical Address	CONTROLSS_CMPSSB4 Physical Address	CONTROLSS_CMPSSB5 Physical Address
0h	16	CONTROLSS_CMPSSB0_COMPCTL	CMPSS Comparator Control Register	5022 3000h	5022 4000h	5022 5000h
2h	16	CONTROLSS_CMPSSB0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5022 3002h	5022 4002h	5022 5002h
4h	16	CONTROLSS_CMPSSB0_COMPSTS	CMPSS Comparator Status Register	5022 3004h	5022 4004h	5022 5004h
6h	16	CONTROLSS_CMPSSB0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5022 3006h	5022 4006h	5022 5006h
8h	16	CONTROLSS_CMPSSB0_COMPDACCTL	CMPSS DAC Control Register	5022 3008h	5022 4008h	5022 5008h
Ah	16	CONTROLSS_CMPSSB0_COMPDACCTL2	CMPSS DAC Control Register 2	5022 300Ah	5022 400Ah	5022 500Ah
Ch	16	CONTROLSS_CMPSSB0_DACHVALS	CMPSS High DAC Value Shadow Register	5022 300Ch	5022 400Ch	5022 500Ch
Eh	16	CONTROLSS_CMPSSB0_DACHVALA	CMPSS High DAC Value Active Register	5022 300Eh	5022 400Eh	5022 500Eh
10h	16	CONTROLSS_CMPSSB0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5022 3010h	5022 4010h	5022 5010h
14h	16	CONTROLSS_CMPSSB0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5022 3014h	5022 4014h	5022 5014h
18h	16	CONTROLSS_CMPSSB0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5022 3018h	5022 4018h	5022 5018h
1Ch	16	CONTROLSS_CMPSSB0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5022 301Ch	5022 401Ch	5022 501Ch
20h	16	CONTROLSS_CMPSSB0_RAMPSTS	CMPSS Ramp Status Register	5022 3020h	5022 4020h	5022 5020h

Table 3-418. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB3 Physical Address	CONTROLSS_CMPSSB4 Physical Address	CONTROLSS_CMPSSB5 Physical Address
24h	16	CONTROLSS_CMPSSB0_DACLVALS	CMPSS Low DAC Value Shadow Register	5022 3024h	5022 4024h	5022 5024h
26h	16	CONTROLSS_CMPSSB0_DACLVALA	CMPSS Low DAC Value Active Register	5022 3026h	5022 4026h	5022 5026h
28h	16	CONTROLSS_CMPSSB0_RAMPDLYA	CMPSS Ramp Delay Active Register	5022 3028h	5022 4028h	5022 5028h
2Ah	16	CONTROLSS_CMPSSB0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5022 302Ah	5022 402Ah	5022 502Ah
2Ch	16	CONTROLSS_CMPSSB0_CTRIPLFILCTL	CTRIPL Filter Control Register	5022 302Ch	5022 402Ch	5022 502Ch
2Eh	16	CONTROLSS_CMPSSB0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5022 302Eh	5022 402Eh	5022 502Eh
30h	16	CONTROLSS_CMPSSB0_CTRIPHFILCTL	CTRIPH Filter Control Register	5022 3030h	5022 4030h	5022 5030h
32h	16	CONTROLSS_CMPSSB0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5022 3032h	5022 4032h	5022 5032h
34h	16	CONTROLSS_CMPSSB0_COMPLOCK	CMPSS Lock Register	5022 3034h	5022 4034h	5022 5034h
38h	16	CONTROLSS_CMPSSB0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5022 3038h	5022 4038h	5022 5038h
3Ah	16	CONTROLSS_CMPSSB0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5022 303Ah	5022 403Ah	5022 503Ah
3Ch	16	CONTROLSS_CMPSSB0_CONFIG1	CMPSS Config1 Register	5022 303Ch	5022 403Ch	5022 503Ch

Table 3-419. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB6 Physical Address	CONTROLSS_CMPSSB7 Physical Address	CONTROLSS_CMPSSB8 Physical Address
0h	16	CONTROLSS_CMPSSB0_COMPCTL	CMPSS Comparator Control Register	5022 6000h	5022 7000h	5022 8000h
2h	16	CONTROLSS_CMPSSB0_COMPHYSCTL	CMPSS Comparator Hysteresis Control Register	5022 6002h	5022 7002h	5022 8002h
4h	16	CONTROLSS_CMPSSB0_COMPSTS	CMPSS Comparator Status Register	5022 6004h	5022 7004h	5022 8004h
6h	16	CONTROLSS_CMPSSB0_COMPSTSCLR	CMPSS Comparator Status Clear Register	5022 6006h	5022 7006h	5022 8006h
8h	16	CONTROLSS_CMPSSB0_COMPDACCTL	CMPSS DAC Control Register	5022 6008h	5022 7008h	5022 8008h
Ah	16	CONTROLSS_CMPSSB0_COMPDACCTL2	CMPSS DAC Control Register 2	5022 600Ah	5022 700Ah	5022 800Ah
Ch	16	CONTROLSS_CMPSSB0_DACHVALS	CMPSS High DAC Value Shadow Register	5022 600Ch	5022 700Ch	5022 800Ch
Eh	16	CONTROLSS_CMPSSB0_DACHVALA	CMPSS High DAC Value Active Register	5022 600Eh	5022 700Eh	5022 800Eh

Table 3-419. CONTROLSS_CMPSSB0, CONTROLSS_CMPSSB0_CONTROLSS_CMPSSB Registers, Base Address=5022 0000H, Length=6 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_CMPSSB6 Physical Address	CONTROLSS_CMPSSB7 Physical Address	CONTROLSS_CMPSSB8 Physical Address
10h	16	CONTROLSS_CMPSSB0_RAMPMAXREFA	CMPSS Ramp Max Reference Active Register	5022 6010h	5022 7010h	5022 8010h
14h	16	CONTROLSS_CMPSSB0_RAMPMAXREFS	CMPSS Ramp Max Reference Shadow Register	5022 6014h	5022 7014h	5022 8014h
18h	16	CONTROLSS_CMPSSB0_RAMPDECVALA	CMPSS Ramp Decrement Value Active Register	5022 6018h	5022 7018h	5022 8018h
1Ch	16	CONTROLSS_CMPSSB0_RAMPDECVALS	CMPSS Ramp Decrement Value Shadow Register	5022 601Ch	5022 701Ch	5022 801Ch
20h	16	CONTROLSS_CMPSSB0_RAMPSTS	CMPSS Ramp Status Register	5022 6020h	5022 7020h	5022 8020h
24h	16	CONTROLSS_CMPSSB0_DACLVALS	CMPSS Low DAC Value Shadow Register	5022 6024h	5022 7024h	5022 8024h
26h	16	CONTROLSS_CMPSSB0_DACLVALA	CMPSS Low DAC Value Active Register	5022 6026h	5022 7026h	5022 8026h
28h	16	CONTROLSS_CMPSSB0_RAMPDLYA	CMPSS Ramp Delay Active Register	5022 6028h	5022 7028h	5022 8028h
2Ah	16	CONTROLSS_CMPSSB0_RAMPDLYS	CMPSS Ramp Delay Shadow Register	5022 602Ah	5022 702Ah	5022 802Ah
2Ch	16	CONTROLSS_CMPSSB0_CTRIPLFILCTL	CTRIPL Filter Control Register	5022 602Ch	5022 702Ch	5022 802Ch
2Eh	16	CONTROLSS_CMPSSB0_CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register	5022 602Eh	5022 702Eh	5022 802Eh
30h	16	CONTROLSS_CMPSSB0_CTRIPHFILCTL	CTRIPH Filter Control Register	5022 6030h	5022 7030h	5022 8030h
32h	16	CONTROLSS_CMPSSB0_CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register	5022 6032h	5022 7032h	5022 8032h
34h	16	CONTROLSS_CMPSSB0_COMPLOCK	CMPSS Lock Register	5022 6034h	5022 7034h	5022 8034h
38h	16	CONTROLSS_CMPSSB0_DACHVALS2	CMPSS High DAC Value Shadow Register 2	5022 6038h	5022 7038h	5022 8038h
3Ah	16	CONTROLSS_CMPSSB0_DACLVALS2	CMPSS Low DAC Value Shadow Register 2	5022 603Ah	5022 703Ah	5022 803Ah
3Ch	16	CONTROLSS_CMPSSB0_CONFIG1	CMPSS Config1 Register	5022 603Ch	5022 703Ch	5022 803Ch

3.4.1 CONTROLSS_CMPSSB0_COMPCTL Register (Offset = 0h) [reset = h]

Short Description: CMPSS Comparator Control Register

Long Description:

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Table 3-420. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0000h
CONTROLSS_CMPSSB1	5022 1000h
CONTROLSS_CMPSSB2	5022 2000h
CONTROLSS_CMPSSB3	5022 3000h
CONTROLSS_CMPSSB4	5022 4000h
CONTROLSS_CMPSSB5	5022 5000h
CONTROLSS_CMPSSB6	5022 6000h
CONTROLSS_CMPSSB7	5022 7000h
CONTROLSS_CMPSSB8	5022 8000h
CONTROLSS_CMPSSB9	5022 9000h

Figure 3-199. CONTROLSS_CMPSSB0_COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	RESERVED_3
RW	RW	RW		RW		RW	RW
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	RESERVED_1
RO	RW	RW		RW		RW	RW
0	0	0		0		0	0

Access Types Legend

Table 3-421. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	RW	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	RW	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13 - 12	CTRIPOUTLSEL	RW	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11 - 10	CTRIPLSEL	RW	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	RW	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	RESERVED_3	RW	0h	Reserved for CMPSSB
7	RESERVED	RO		Reserved

Table 3-421. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ASYNCHEN	RW	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5 - 4	CTRIPOUTHSEL	RW	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH
3 - 2	CTRIPHSEL	RW	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	RW	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	RESERVED_1	RW	0h	Reserved for CMPSSB

3.4.2 CONTROLSS_CMPSSB0_COMPHYSCTL Register (Offset = 2h) [reset = h]

Short Description: CMPSS Comparator Hysteresis Control Register

Long Description:

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Table 3-422. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0002h
CONTROLSS_CMPSSB1	5022 1002h
CONTROLSS_CMPSSB2	5022 2002h
CONTROLSS_CMPSSB3	5022 3002h
CONTROLSS_CMPSSB4	5022 4002h
CONTROLSS_CMPSSB5	5022 5002h
CONTROLSS_CMPSSB6	5022 6002h
CONTROLSS_CMPSSB7	5022 7002h
CONTROLSS_CMPSSB8	5022 8002h
CONTROLSS_CMPSSB9	5022 9002h

Figure 3-200. CONTROLSS_CMPSSB0_COMPHYSCTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				COMPHYS			
RO				RW			
0				0			

Access Types Legend

Table 3-423. COMPHYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	COMPHYS	RW	0h	Comparator hysteresis. Sets the amount of hysteresis on the comparator inputs. 0 None 1 Set to typical hysteresis 2 Set to 2x of typical hysteresis 3 Set to 3x of typical hysteresis 4 Set to 4x of typical hysteresis others : undefined

3.4.3 CONTROLSS_CMPSSB0_COMPSTS Register (Offset = 4h) [reset = h]

Short Description: CMPSS Comparator Status Register

Long Description:

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Table 3-424. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0004h
CONTROLSS_CMPSSB1	5022 1004h
CONTROLSS_CMPSSB2	5022 2004h
CONTROLSS_CMPSSB3	5022 3004h
CONTROLSS_CMPSSB4	5022 4004h
CONTROLSS_CMPSSB5	5022 5004h
CONTROLSS_CMPSSB6	5022 6004h
CONTROLSS_CMPSSB7	5022 7004h
CONTROLSS_CMPSSB8	5022 8004h
CONTROLSS_CMPSSB9	5022 9004h

Figure 3-201. CONTROLSS_CMPSSB0_COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED						COMPLLATCH	COMPLSTS
RO						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED						COMPHLATCH	COMPHSTS
RO						RO	RO
0						0	0

Access Types Legend

Table 3-425. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	COMPLLATCH	RO	0h	Latched value of low comparator digital filter output
8	COMPLSTS	RO	0h	Low comparator digital filter output
7 - 2	RESERVED	RO		Reserved
1	COMPHLATCH	RO	0h	Latched value of high comparator digital filter output
0	COMPHSTS	RO	0h	High comparator digital filter output

3.4.4 CONTROLSS_CMPSSB0_COMPSTSCLR Register (Offset = 6h) [reset = h]

Short Description: CMPSS Comparator Status Clear Register

Long Description:

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Table 3-426. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0006h
CONTROLSS_CMPSSB1	5022 1006h
CONTROLSS_CMPSSB2	5022 2006h
CONTROLSS_CMPSSB3	5022 3006h
CONTROLSS_CMPSSB4	5022 4006h
CONTROLSS_CMPSSB5	5022 5006h
CONTROLSS_CMPSSB6	5022 6006h
CONTROLSS_CMPSSB7	5022 7006h
CONTROLSS_CMPSSB8	5022 8006h
CONTROLSS_CMPSSB9	5022 9006h

Figure 3-202. CONTROLSS_CMPSSB0_COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED					LSYNCCLREN	LLATCHCLR	RESERVED
RO					RW	RW RRETURNS0S	RO
0					0	0	0
7	6	5	4	3	2	1	0
RESERVED					HSYNCCLREN	HLATCHCLR	RESERVED
RO					RW	RW RRETURNS0S	RO
0					0	0	0

Access Types Legend

Table 3-427. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	LSYNCCLREN	RW	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	RW RRETURNS 0S	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8 - 3	RESERVED	RO		Reserved
2	HSYNCCLREN	RW	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	RW RRETURNS 0S	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]
0	RESERVED	RO		Reserved

3.4.5 CONTROLSS_CMPSSB0_COMPDACCTL Register (Offset = 8h) [reset = h]

Short Description: CMPSS DAC Control Register

Long Description:

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Table 3-428. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0008h
CONTROLSS_CMPSSB1	5022 1008h
CONTROLSS_CMPSSB2	5022 2008h
CONTROLSS_CMPSSB3	5022 3008h
CONTROLSS_CMPSSB4	5022 4008h
CONTROLSS_CMPSSB5	5022 5008h
CONTROLSS_CMPSSB6	5022 6008h
CONTROLSS_CMPSSB7	5022 7008h
CONTROLSS_CMPSSB8	5022 8008h
CONTROLSS_CMPSSB9	5022 9008h

Figure 3-203. CONTROLSS_CMPSSB0_COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED	BLANKEN	BLANKSOURCE			
RW		RO	RW	RW			
0		0	0	0			
7	6	5	4	3	2	1	0
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
RW	RW	RW	RW				RW
0	0	0	0				0

Access Types Legend

Table 3-429. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREESOFT	RW	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED	RO		Reserved
12	BLANKEN	RW	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11 - 8	BLANKSOURCE	RW	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK
7	SWLOADSEL	RW	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER
6	RAMPLOADSEL	RW	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS

ADVANCE INFORMATION

Table 3-429. COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SELREF	RW	0h	CMPSS reference select0 vref_1p8v as reference voltage (default)1 vdd_1p8v as reference voltage
4 - 1	RAMPSOURCE	RW	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	RW	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

3.4.6 CONTROLSS_CMPSSB0_COMPDACCTL2 Register (Offset = Ah) [reset = h]

Short Description: CMPSS DAC Control Register 2

Long Description:

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Table 3-430. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Ah
CONTROLSS_CMPSSB1	5022 100Ah
CONTROLSS_CMPSSB2	5022 200Ah
CONTROLSS_CMPSSB3	5022 300Ah
CONTROLSS_CMPSSB4	5022 400Ah
CONTROLSS_CMPSSB5	5022 500Ah
CONTROLSS_CMPSSB6	5022 600Ah
CONTROLSS_CMPSSB7	5022 700Ah
CONTROLSS_CMPSSB8	5022 800Ah
CONTROLSS_CMPSSB9	5022 900Ah

Figure 3-204. CONTROLSS_CMPSSB0_COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED					RAMPSOURCEUSEL	RESERVED	BLANKSOURCEUSEL
RO					RW	RO	RW
0					0	0	0
7	6	5	4	3	2	1	0
RESERVED		DEACTIVESEL					DEENABLE
RO		RW					RW
0		0					0

Access Types Legend

Table 3-431. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	RAMPSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source
9	RESERVED	RO		Reserved
8	BLANKSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source
7 - 6	RESERVED	RO		Reserved
5 - 1	DEACTIVESEL	RW	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE
0	DEENABLE	RW	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

ADVANCE INFORMATION

3.4.7 CONTROLSS_CMPSSB0_DACHVALS Register (Offset = Ch) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register

Long Description:

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Table 3-432. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Ch
CONTROLSS_CMPSSB1	5022 100Ch
CONTROLSS_CMPSSB2	5022 200Ch
CONTROLSS_CMPSSB3	5022 300Ch
CONTROLSS_CMPSSB4	5022 400Ch
CONTROLSS_CMPSSB5	5022 500Ch
CONTROLSS_CMPSSB6	5022 600Ch
CONTROLSS_CMPSSB7	5022 700Ch
CONTROLSS_CMPSSB8	5022 800Ch
CONTROLSS_CMPSSB9	5022 900Ch

Figure 3-205. CONTROLSS_CMPSSB0_DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-433. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

3.4.8 CONTROLSS_CMPSSB0_DACHVALA Register (Offset = Eh) [reset = h]

Short Description: CMPSS High DAC Value Active Register

Long Description:

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Table 3-434. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Eh
CONTROLSS_CMPSSB1	5022 100Eh
CONTROLSS_CMPSSB2	5022 200Eh
CONTROLSS_CMPSSB3	5022 300Eh
CONTROLSS_CMPSSB4	5022 400Eh
CONTROLSS_CMPSSB5	5022 500Eh
CONTROLSS_CMPSSB6	5022 600Eh
CONTROLSS_CMPSSB7	5022 700Eh
CONTROLSS_CMPSSB8	5022 800Eh
CONTROLSS_CMPSSB9	5022 900Eh

Figure 3-206. CONTROLSS_CMPSSB0_DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RO							
0							

Access Types Legend

Table 3-435. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	High DAC active value. Value that is actively driven by the high DAC.

3.4.9 CONTROLSS_CMPSSB0_RAMPMAXREFA Register (Offset = 10h) [reset = h]

Short Description: CMPSS Ramp Max Reference Active Register

Long Description:

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Table 3-436. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0010h
CONTROLSS_CMPSSB1	5022 1010h
CONTROLSS_CMPSSB2	5022 2010h
CONTROLSS_CMPSSB3	5022 3010h
CONTROLSS_CMPSSB4	5022 4010h
CONTROLSS_CMPSSB5	5022 5010h
CONTROLSS_CMPSSB6	5022 6010h
CONTROLSS_CMPSSB7	5022 7010h
CONTROLSS_CMPSSB8	5022 8010h
CONTROLSS_CMPSSB9	5022 9010h

Figure 3-207. CONTROLSS_CMPSSB0_RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
RO							
0							
7	6	5	4	3	2	1	0
RAMPMAXREF							
RO							
0							

Access Types Legend

Table 3-437. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RO	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

3.4.10 CONTROLSS_CMPSSB0_RAMPMAXREFS Register (Offset = 14h) [reset = h]

Short Description: CMPSS Ramp Max Reference Shadow Register

Long Description:

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Table 3-438. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0014h
CONTROLSS_CMPSSB1	5022 1014h
CONTROLSS_CMPSSB2	5022 2014h
CONTROLSS_CMPSSB3	5022 3014h
CONTROLSS_CMPSSB4	5022 4014h
CONTROLSS_CMPSSB5	5022 5014h
CONTROLSS_CMPSSB6	5022 6014h
CONTROLSS_CMPSSB7	5022 7014h
CONTROLSS_CMPSSB8	5022 8014h
CONTROLSS_CMPSSB9	5022 9014h

Figure 3-208. CONTROLSS_CMPSSB0_RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
RW							
0							
7	6	5	4	3	2	1	0
RAMPMAXREF							
RW							
0							

Access Types Legend

Table 3-439. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RW	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

3.4.11 CONTROLSS_CMPSSB0_RAMPDECVALA Register (Offset = 18h) [reset = h]

Short Description: CMPSS Ramp Decrement Value Active Register

Long Description:

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Table 3-440. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0018h
CONTROLSS_CMPSSB1	5022 1018h
CONTROLSS_CMPSSB2	5022 2018h
CONTROLSS_CMPSSB3	5022 3018h
CONTROLSS_CMPSSB4	5022 4018h
CONTROLSS_CMPSSB5	5022 5018h
CONTROLSS_CMPSSB6	5022 6018h
CONTROLSS_CMPSSB7	5022 7018h
CONTROLSS_CMPSSB8	5022 8018h
CONTROLSS_CMPSSB9	5022 9018h

Figure 3-209. CONTROLSS_CMPSSB0_RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
RO							
0							
7	6	5	4	3	2	1	0
RAMPDECVAL							
RO							
0							

Access Types Legend

Table 3-441. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RO	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

3.4.12 CONTROLSS_CMPSSB0_RAMPDECVALS Register (Offset = 1Ch) [reset = h]

Short Description: CMPSS Ramp Decrement Value Shadow Register

Long Description:

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Table 3-442. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 001Ch
CONTROLSS_CMPSSB1	5022 101Ch
CONTROLSS_CMPSSB2	5022 201Ch
CONTROLSS_CMPSSB3	5022 301Ch
CONTROLSS_CMPSSB4	5022 401Ch
CONTROLSS_CMPSSB5	5022 501Ch
CONTROLSS_CMPSSB6	5022 601Ch
CONTROLSS_CMPSSB7	5022 701Ch
CONTROLSS_CMPSSB8	5022 801Ch
CONTROLSS_CMPSSB9	5022 901Ch

Figure 3-210. CONTROLSS_CMPSSB0_RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
RW							
0							
7	6	5	4	3	2	1	0
RAMPDECVAL							
RW							
0							

Access Types Legend

Table 3-443. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RW	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

3.4.13 CONTROLSS_CMPSSB0_RAMPSTS Register (Offset = 20h) [reset = h]

Short Description: CMPSS Ramp Status Register

Long Description:

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Table 3-444. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0020h
CONTROLSS_CMPSSB1	5022 1020h
CONTROLSS_CMPSSB2	5022 2020h
CONTROLSS_CMPSSB3	5022 3020h
CONTROLSS_CMPSSB4	5022 4020h
CONTROLSS_CMPSSB5	5022 5020h
CONTROLSS_CMPSSB6	5022 6020h
CONTROLSS_CMPSSB7	5022 7020h
CONTROLSS_CMPSSB8	5022 8020h
CONTROLSS_CMPSSB9	5022 9020h

Figure 3-211. CONTROLSS_CMPSSB0_RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
RO							
0							
7	6	5	4	3	2	1	0
RAMPVALUE							
RO							
0							

Access Types Legend

Table 3-445. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPVALUE	RO	0h	Ramp value. Present value of ramp generator.

3.4.14 CONTROLSS_CMPSSB0_DACLVALS Register (Offset = 24h) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register

Long Description:

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Table 3-446. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0024h
CONTROLSS_CMPSSB1	5022 1024h
CONTROLSS_CMPSSB2	5022 2024h
CONTROLSS_CMPSSB3	5022 3024h
CONTROLSS_CMPSSB4	5022 4024h
CONTROLSS_CMPSSB5	5022 5024h
CONTROLSS_CMPSSB6	5022 6024h
CONTROLSS_CMPSSB7	5022 7024h
CONTROLSS_CMPSSB8	5022 8024h
CONTROLSS_CMPSSB9	5022 9024h

Figure 3-212. CONTROLSS_CMPSSB0_DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-447. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

3.4.15 CONTROLSS_CMPSSB0_DACLVALA Register (Offset = 26h) [reset = h]

Short Description: CMPSS Low DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-448. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0026h
CONTROLSS_CMPSSB1	5022 1026h
CONTROLSS_CMPSSB2	5022 2026h
CONTROLSS_CMPSSB3	5022 3026h
CONTROLSS_CMPSSB4	5022 4026h
CONTROLSS_CMPSSB5	5022 5026h
CONTROLSS_CMPSSB6	5022 6026h
CONTROLSS_CMPSSB7	5022 7026h
CONTROLSS_CMPSSB8	5022 8026h
CONTROLSS_CMPSSB9	5022 9026h

Figure 3-213. CONTROLSS_CMPSSB0_DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RO							
0							

Access Types Legend

Table 3-449. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	Low DAC active value. Value that is actively driven by the low DAC.

3.4.16 CONTROLSS_CMPSSB0_RAMPDLYA Register (Offset = 28h) [reset = h]

Short Description: CMPSS Ramp Delay Active Register

Long Description:

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Table 3-450. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0028h
CONTROLSS_CMPSSB1	5022 1028h
CONTROLSS_CMPSSB2	5022 2028h
CONTROLSS_CMPSSB3	5022 3028h
CONTROLSS_CMPSSB4	5022 4028h
CONTROLSS_CMPSSB5	5022 5028h
CONTROLSS_CMPSSB6	5022 6028h
CONTROLSS_CMPSSB7	5022 7028h
CONTROLSS_CMPSSB8	5022 8028h
CONTROLSS_CMPSSB9	5022 9028h

Figure 3-214. CONTROLSS_CMPSSB0_RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED			DELAY				
RO			RO				
0			0				
7	6	5	4	3	2	1	0
DELAY							
RO							
0							

Access Types Legend

Table 3-451. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RO	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

3.4.17 CONTROLSS_CMPSSB0_RAMPDLYS Register (Offset = 2Ah) [reset = h]

Short Description: CMPSS Ramp Delay Shadow Register

Long Description:

Return to Summary Table

Table 3-452. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Ah
CONTROLSS_CMPSSB1	5022 102Ah
CONTROLSS_CMPSSB2	5022 202Ah
CONTROLSS_CMPSSB3	5022 302Ah
CONTROLSS_CMPSSB4	5022 402Ah
CONTROLSS_CMPSSB5	5022 502Ah
CONTROLSS_CMPSSB6	5022 602Ah
CONTROLSS_CMPSSB7	5022 702Ah
CONTROLSS_CMPSSB8	5022 802Ah
CONTROLSS_CMPSSB9	5022 902Ah

Figure 3-215. CONTROLSS_CMPSSB0_RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED			DELAY				
RO			RW				
0			0				
7	6	5	4	3	2	1	0
DELAY							
RW							
0							

Access Types Legend

Table 3-453. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RW	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

3.4.18 CONTROLSS_CMPSSB0_CTRIPLFILCTL Register (Offset = 2Ch) [reset = h]

Short Description: CTRIPL Filter Control Register

Long Description:

Return to Summary Table

Table 3-454. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Ch
CONTROLSS_CMPSSB1	5022 102Ch
CONTROLSS_CMPSSB2	5022 202Ch
CONTROLSS_CMPSSB3	5022 302Ch
CONTROLSS_CMPSSB4	5022 402Ch
CONTROLSS_CMPSSB5	5022 502Ch
CONTROLSS_CMPSSB6	5022 602Ch
CONTROLSS_CMPSSB7	5022 702Ch
CONTROLSS_CMPSSB8	5022 802Ch
CONTROLSS_CMPSSB9	5022 902Ch

Figure 3-216. CONTROLSS_CMPSSB0_CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-455. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.4.19 CONTROLSS_CMPSSB0_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = h]

Short Description: CTRIPL Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-456. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Eh
CONTROLSS_CMPSSB1	5022 102Eh
CONTROLSS_CMPSSB2	5022 202Eh
CONTROLSS_CMPSSB3	5022 302Eh
CONTROLSS_CMPSSB4	5022 402Eh
CONTROLSS_CMPSSB5	5022 502Eh
CONTROLSS_CMPSSB6	5022 602Eh
CONTROLSS_CMPSSB7	5022 702Eh
CONTROLSS_CMPSSB8	5022 802Eh
CONTROLSS_CMPSSB9	5022 902Eh

Figure 3-217. CONTROLSS_CMPSSB0_CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
RW							
0							
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-457. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

3.4.20 CONTROLSS_CMPSSB0_CTRIPHFILCTL Register (Offset = 30h) [reset = h]

Short Description: CTRIPH Filter Control Register

Long Description:

Return to Summary Table

Table 3-458. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0030h
CONTROLSS_CMPSSB1	5022 1030h
CONTROLSS_CMPSSB2	5022 2030h
CONTROLSS_CMPSSB3	5022 3030h
CONTROLSS_CMPSSB4	5022 4030h
CONTROLSS_CMPSSB5	5022 5030h
CONTROLSS_CMPSSB6	5022 6030h
CONTROLSS_CMPSSB7	5022 7030h
CONTROLSS_CMPSSB8	5022 8030h
CONTROLSS_CMPSSB9	5022 9030h

Figure 3-218. CONTROLSS_CMPSSB0_CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-459. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.4.21 CONTROLSS_CMPSSB0_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = h]

Short Description: CTRIPH Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-460. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0032h
CONTROLSS_CMPSSB1	5022 1032h
CONTROLSS_CMPSSB2	5022 2032h
CONTROLSS_CMPSSB3	5022 3032h
CONTROLSS_CMPSSB4	5022 4032h
CONTROLSS_CMPSSB5	5022 5032h
CONTROLSS_CMPSSB6	5022 6032h
CONTROLSS_CMPSSB7	5022 7032h
CONTROLSS_CMPSSB8	5022 8032h
CONTROLSS_CMPSSB9	5022 9032h

Figure 3-219. CONTROLSS_CMPSSB0_CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
RW							
0							
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-461. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

3.4.22 CONTROLSS_CMPSSB0_COMPLOCK Register (Offset = 34h) [reset = h]

Short Description: CMPSS Lock Register

Long Description:

Return to Summary Table

Table 3-462. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0034h
CONTROLSS_CMPSSB1	5022 1034h
CONTROLSS_CMPSSB2	5022 2034h
CONTROLSS_CMPSSB3	5022 3034h
CONTROLSS_CMPSSB4	5022 4034h
CONTROLSS_CMPSSB5	5022 5034h
CONTROLSS_CMPSSB6	5022 6034h
CONTROLSS_CMPSSB7	5022 7034h
CONTROLSS_CMPSSB8	5022 8034h
CONTROLSS_CMPSSB9	5022 9034h

Figure 3-220. CONTROLSS_CMPSSB0_COMPLOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			TEST	CTRIP	DACCTL	COMPHYSCTL	COMPCTL
RO			RW SONCE	RW SONCE	RW SONCE	RW SONCE	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-463. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	TEST	RW SONCE	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	RW SONCE	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	RW SONCE	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	RW SONCE	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

3.4.23 CONTROLSS_CMPSSB0_DACHVALS2 Register (Offset = 38h) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-464. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0038h
CONTROLSS_CMPSSB1	5022 1038h
CONTROLSS_CMPSSB2	5022 2038h
CONTROLSS_CMPSSB3	5022 3038h
CONTROLSS_CMPSSB4	5022 4038h
CONTROLSS_CMPSSB5	5022 5038h
CONTROLSS_CMPSSB6	5022 6038h
CONTROLSS_CMPSSB7	5022 7038h
CONTROLSS_CMPSSB8	5022 8038h
CONTROLSS_CMPSSB9	5022 9038h

Figure 3-221. CONTROLSS_CMPSSB0_DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-465. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

3.4.24 CONTROLSS_CMPSSB0_DACLVALS2 Register (Offset = 3Ah) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-466. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 003Ah
CONTROLSS_CMPSSB1	5022 103Ah
CONTROLSS_CMPSSB2	5022 203Ah
CONTROLSS_CMPSSB3	5022 303Ah
CONTROLSS_CMPSSB4	5022 403Ah
CONTROLSS_CMPSSB5	5022 503Ah
CONTROLSS_CMPSSB6	5022 603Ah
CONTROLSS_CMPSSB7	5022 703Ah
CONTROLSS_CMPSSB8	5022 803Ah
CONTROLSS_CMPSSB9	5022 903Ah

Figure 3-222. CONTROLSS_CMPSSB0_DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVAL							
RW							
0							

Access Types Legend

Table 3-467. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

3.4.25 CONTROLSS_CMPSSB0_CONFIG1 Register (Offset = 3Ch) [reset = h]

Short Description: CMPSS Config1 Register

Long Description:

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Table 3-468. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 003Ch
CONTROLSS_CMPSSB1	5022 103Ch
CONTROLSS_CMPSSB2	5022 203Ch
CONTROLSS_CMPSSB3	5022 303Ch
CONTROLSS_CMPSSB4	5022 403Ch
CONTROLSS_CMPSSB5	5022 503Ch
CONTROLSS_CMPSSB6	5022 603Ch
CONTROLSS_CMPSSB7	5022 703Ch
CONTROLSS_CMPSSB8	5022 803Ch
CONTROLSS_CMPSSB9	5022 903Ch

Figure 3-223. CONTROLSS_CMPSSB0_CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
RW							
0							
7	6	5	4	3	2	1	0
COMPLHYS				COMPHHYS			
RW				RW			
0				0			

Access Types Legend

Table 3-469. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	SPARE	RW	0h	SPARE
7 - 4	COMPLHYS	RW	0h	compL Hysterisishystl_1p1v[3] = reservedhystl_1p1v[2] = control which comparator output value the hysteresis is applied tohystl_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB
3 - 0	COMPHHYS	RW	0h	CompH Hysteresishysth_1p1v[3] = reservedhysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b11 comparator hysteresis is applied when the comparator output is 1'b0hysth_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB

Table 3-470. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RW SONCE	RW SONCE	Undefined

3.5 C2K_DAC Registers

Table 3-471. CONTROLSS_DAC0, CONTROLSS_DAC0_CONTROLSS_DAC Registers, Base Address=5026 0000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_DAC0 Physical Address
0h	16	CONTROLSS_DAC0_DACREV	DAC Revision Register	5026 0000h
2h	16	CONTROLSS_DAC0_DACCTL_ALT2_	DAC Control Register	5026 0002h
4h	16	CONTROLSS_DAC0_DACVALA	DAC Value Register - Active	5026 0004h
6h	16	CONTROLSS_DAC0_DACVALS	DAC Value Register - Shadow	5026 0006h
8h	16	CONTROLSS_DAC0_DACOUTEN	DAC Output Enable Register	5026 0008h
Ah	16	CONTROLSS_DAC0_DACLOCK	DAC Lock Register	5026 000Ah
Ch	16	CONTROLSS_DAC0_DACTRIM	DAC Trim Register	5026 000Ch

3.5.1 CONTROLSS_DAC0_DACREV Register (Offset = 0h) [reset = h]

Short Description: DAC Revision Register

Long Description:

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Table 3-472. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0000h

Figure 3-224. CONTROLSS_DAC0_DACREV Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
REV							
RO							
0							

Access Types Legend

Table 3-473. DACREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7 - 0	REV	RO	0h	DAC Revision

3.5.2 CONTROLSS_DAC0_DACCTL_ALT2_ Register (Offset = 2h) [reset = h]

Short Description: DAC Control Register

Long Description:

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Table 3-474. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0002h

Figure 3-225. CONTROLSS_DAC0_DACCTL_ALT2_ Name Register

15	14	13	12	11	10	9	8
RESERVED							SYNCSEL
RO							RW
0							0
7	6	5	4	3	2	1	0
SYNCSEL				RESERVED	LOADMODE	MODE	DACREFSEL
RW				RO	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 3-475. DACCTL_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8 - 4	SYNCSEL	RW	0h	DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register.[[br]] [[br]]Where n represents the maximum number of EPWMSYNCPER signals available on the device:[[br]] [[br]] 0 EPWM1SYNCPER[[br]] 1 EPWM2SYNCPER[[br]] 2 EPWM3SYNCPER[[br]] ...[[br]] n-1 EPWMnSYNCPER
3	RESERVED	RO		Reserved
2	LOADMODE	RW	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS.[[br]] [[br]] 0 Load on next SYSCLK[[br]] 1 Load on next EPWMSYNCPER specified by SYNCSEL
1	MODE	RW	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected.[[br]] [[br]] 0 Gain is 1[[br]] 1 Gain is 2
0	DACREFSEL	RW	0h	DAC reference select. Selects which voltage references are used by the DAC.[[br]] [[br]] 0 VDAC/VSSA are the reference voltages[[br]] 1 ADC VREFHI/VSSA are the reference voltages

3.5.3 CONTROLSS_DAC0_DACVALA Register (Offset = 4h) [reset = h]

Short Description: DAC Value Register - Active

Long Description:

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Table 3-476. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0004h

Figure 3-226. CONTROLSS_DAC0_DACVALA Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVALA			
RO				RO			
0				0			
7	6	5	4	3	2	1	0
DACVALA							
RO							
0							

Access Types Legend

Table 3-477. DACVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVALA	RO	0h	Active output code currently driven by the DAC

3.5.4 CONTROLSS_DAC0_DACVALS Register (Offset = 6h) [reset = h]

Short Description: DAC Value Register - Shadow

Long Description:

Return to Summary Table

Table 3-478. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0006h

Figure 3-227. CONTROLSS_DAC0_DACVALS Name Register

15	14	13	12	11	10	9	8
RESERVED				DACVALS			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
DACVALS							
RW							
0							

Access Types Legend

Table 3-479. DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVALS	RW	0h	Shadow output code to be loaded into DACVALA

3.5.5 CONTROLSS_DAC0_DACOUTEN Register (Offset = 8h) [reset = h]

Short Description: DAC Output Enable Register

Long Description:

Return to Summary Table

Table 3-480. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0008h

Figure 3-228. CONTROLSS_DAC0_DACOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED							DACOUTEN
RO							RW
0							0

Access Types Legend

Table 3-481. DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DACOUTEN	RW	0h	DAC output enable[[br]] [[br]] 0 DAC output is disabled[[br]] 1 DAC output is enabled

3.5.6 CONTROLSS_DAC0_DACLOCK Register (Offset = Ah) [reset = h]

Short Description: DAC Lock Register

Long Description:

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Table 3-482. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 000Ah

Figure 3-229. CONTROLSS_DAC0_DACLOCK Name Register

15	14	13	12	11	10	9	8
KEY				RESERVED			
RW RRETURNS0S				RO			
0				0			
7	6	5	4	3	2	1	0
RESERVED					DACOUTEN	DACVAL	DACCTL
RO					RW SONCE	RW SONCE	RW SONCE
0					0	0	0

Access Types Legend

Table 3-483. DACLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	KEY	RW RRETURNS 0S	0h	Writes to this register succeed only if this field is written with a value of 0xA.[[br]] [[br]]Only 16-bit writes will succeed (provided the KEY matches). Read-modify-writes to individual bits in this register will be ignored.
11 - 3	RESERVED	RO		Reserved
2	DACOUTEN	RW SONCE	0h	Lock write-access to the DACOUTEN register.[[br]] [[br]] 0 DACOUTEN register is not locked. Write 0 to this bit has no effect. [[br]] 1 DACOUTEN register is locked. Only a system reset can clear this bit.
1	DACVAL	RW SONCE	0h	Lock write-access to the DACVALS register.[[br]] [[br]] 0 DACVALS register is not locked. Write 0 to this bit has no effect.[[br]] 1 DACVALS register is locked. Only a system reset can clear this bit.
0	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register.[[br]] [[br]] 0 DACCTL register is not locked. Write 0 to this bit has no effect.[[br]] 1 DACCTL register is locked. Only a system reset can clear this bit.

3.5.7 CONTROLSS_DAC0_DACTRIM Register (Offset = Ch) [reset = h]

Short Description: DAC Trim Register

Long Description:

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Table 3-484. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 000Ch

Figure 3-230. CONTROLSS_DAC0_DACTRIM Name Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
RO				RW			
0				0			
7	6	5	4	3	2	1	0
OFFSET_TRIM							
RW							
0							

Access Types Legend

Table 3-485. DACTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 8	RESERVED	RW		DAC Gain Trim. This signed (two's complement) bit field is used to adjust the gain of the DAC. This register will be written with a factory set value during the device boot procedure.[[br]] [[br]] 1000 Gain is increased by the equivalent of 0.8%[[br]] ...[[br]] 1110 Gain is increased by the equivalent of 0.2% LSB[[br]] 1111 Gain is increased by the equivalent of 0.1% LSB[[br]] 0000 Gain is not adjusted[[br]] 0001 Gain is decreased by the equivalent of 0.1% LSB[[br]] 0010 Gain is decreased by the equivalent of 0.2% LSB[[br]] ...[[br]] 0111 Gain is decreased by the equivalent of 0.7% LSB
7 - 0	OFFSET_TRIM	RW	0h	DAC Offset Trim.[[br]] [[br]]This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

Table 3-486. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RW SONCE	RW SONCE	Undefined

3.6 C2K_DMAXBAR Registers

Table 3-487. CONTROLSS_DMAXBAR, CONTROLSS_DMAXBAR_CONTROLSS_DMAXBAR Registers, Base Address=502D 6000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_DMAXBAR Physical Address
0h	32	CONTROLSS_DMAXBAR_PID	PID register	502D 6000h
100h	8	CONTROLSS_DMAXBAR_DMAXBAR0_GSEL	RW	502D 6100h
104h	8	CONTROLSS_DMAXBAR_DMAXBAR0_G0	RW	502D 6104h
108h	8	CONTROLSS_DMAXBAR_DMAXBAR0_G1	RW	502D 6108h
10Ch	8	CONTROLSS_DMAXBAR_DMAXBAR0_G2	RW	502D 610Ch
110h	8	CONTROLSS_DMAXBAR_DMAXBAR0_G3	RW	502D 6110h
114h	8	CONTROLSS_DMAXBAR_DMAXBAR0_G4	RW	502D 6114h
118h	8	CONTROLSS_DMAXBAR_DMAXBAR0_G5	RW	502D 6118h
140h	8	CONTROLSS_DMAXBAR_DMAXBAR1_GSEL	RW	502D 6140h
144h	8	CONTROLSS_DMAXBAR_DMAXBAR1_G0	RW	502D 6144h
148h	8	CONTROLSS_DMAXBAR_DMAXBAR1_G1	RW	502D 6148h
14Ch	8	CONTROLSS_DMAXBAR_DMAXBAR1_G2	RW	502D 614Ch
150h	8	CONTROLSS_DMAXBAR_DMAXBAR1_G3	RW	502D 6150h
154h	8	CONTROLSS_DMAXBAR_DMAXBAR1_G4	RW	502D 6154h
158h	8	CONTROLSS_DMAXBAR_DMAXBAR1_G5	RW	502D 6158h
180h	8	CONTROLSS_DMAXBAR_DMAXBAR2_GSEL	RW	502D 6180h
184h	8	CONTROLSS_DMAXBAR_DMAXBAR2_G0	RW	502D 6184h
188h	8	CONTROLSS_DMAXBAR_DMAXBAR2_G1	RW	502D 6188h
18Ch	8	CONTROLSS_DMAXBAR_DMAXBAR2_G2	RW	502D 618Ch
190h	8	CONTROLSS_DMAXBAR_DMAXBAR2_G3	RW	502D 6190h
194h	8	CONTROLSS_DMAXBAR_DMAXBAR2_G4	RW	502D 6194h
198h	8	CONTROLSS_DMAXBAR_DMAXBAR2_G5	RW	502D 6198h
1C0h	8	CONTROLSS_DMAXBAR_DMAXBAR3_GSEL	RW	502D 61C0h
1C4h	8	CONTROLSS_DMAXBAR_DMAXBAR3_G0	RW	502D 61C4h
1C8h	8	CONTROLSS_DMAXBAR_DMAXBAR3_G1	RW	502D 61C8h
1CCh	8	CONTROLSS_DMAXBAR_DMAXBAR3_G2	RW	502D 61CCh
1D0h	8	CONTROLSS_DMAXBAR_DMAXBAR3_G3	RW	502D 61D0h
1D4h	8	CONTROLSS_DMAXBAR_DMAXBAR3_G4	RW	502D 61D4h
1D8h	8	CONTROLSS_DMAXBAR_DMAXBAR3_G5	RW	502D 61D8h
200h	8	CONTROLSS_DMAXBAR_DMAXBAR4_GSEL	RW	502D 6200h
204h	8	CONTROLSS_DMAXBAR_DMAXBAR4_G0	RW	502D 6204h
208h	8	CONTROLSS_DMAXBAR_DMAXBAR4_G1	RW	502D 6208h

Table 3-487. CONTROLSS_DMAXBAR, CONTROLSS_DMAXBAR_CONTROLSS_DMAXBAR Registers, Base Address=502D 6000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_DMAXBAR Physical Address
20Ch	8	CONTROLSS_DMAXBAR_DMAXBAR4_G2	RW	502D 620Ch
210h	8	CONTROLSS_DMAXBAR_DMAXBAR4_G3	RW	502D 6210h
214h	8	CONTROLSS_DMAXBAR_DMAXBAR4_G4	RW	502D 6214h
218h	8	CONTROLSS_DMAXBAR_DMAXBAR4_G5	RW	502D 6218h
240h	8	CONTROLSS_DMAXBAR_DMAXBAR5_GSEL	RW	502D 6240h
244h	8	CONTROLSS_DMAXBAR_DMAXBAR5_G0	RW	502D 6244h
248h	8	CONTROLSS_DMAXBAR_DMAXBAR5_G1	RW	502D 6248h
24Ch	8	CONTROLSS_DMAXBAR_DMAXBAR5_G2	RW	502D 624Ch
250h	8	CONTROLSS_DMAXBAR_DMAXBAR5_G3	RW	502D 6250h
254h	8	CONTROLSS_DMAXBAR_DMAXBAR5_G4	RW	502D 6254h
258h	8	CONTROLSS_DMAXBAR_DMAXBAR5_G5	RW	502D 6258h
280h	8	CONTROLSS_DMAXBAR_DMAXBAR6_GSEL	RW	502D 6280h
284h	8	CONTROLSS_DMAXBAR_DMAXBAR6_G0	RW	502D 6284h
288h	8	CONTROLSS_DMAXBAR_DMAXBAR6_G1	RW	502D 6288h
28Ch	8	CONTROLSS_DMAXBAR_DMAXBAR6_G2	RW	502D 628Ch
290h	8	CONTROLSS_DMAXBAR_DMAXBAR6_G3	RW	502D 6290h
294h	8	CONTROLSS_DMAXBAR_DMAXBAR6_G4	RW	502D 6294h
298h	8	CONTROLSS_DMAXBAR_DMAXBAR6_G5	RW	502D 6298h
2C0h	8	CONTROLSS_DMAXBAR_DMAXBAR7_GSEL	RW	502D 62C0h
2C4h	8	CONTROLSS_DMAXBAR_DMAXBAR7_G0	RW	502D 62C4h
2C8h	8	CONTROLSS_DMAXBAR_DMAXBAR7_G1	RW	502D 62C8h
2CCh	8	CONTROLSS_DMAXBAR_DMAXBAR7_G2	RW	502D 62CCh
2D0h	8	CONTROLSS_DMAXBAR_DMAXBAR7_G3	RW	502D 62D0h
2D4h	8	CONTROLSS_DMAXBAR_DMAXBAR7_G4	RW	502D 62D4h
2D8h	8	CONTROLSS_DMAXBAR_DMAXBAR7_G5	RW	502D 62D8h
300h	8	CONTROLSS_DMAXBAR_DMAXBAR8_GSEL	RW	502D 6300h
304h	8	CONTROLSS_DMAXBAR_DMAXBAR8_G0	RW	502D 6304h
308h	8	CONTROLSS_DMAXBAR_DMAXBAR8_G1	RW	502D 6308h
30Ch	8	CONTROLSS_DMAXBAR_DMAXBAR8_G2	RW	502D 630Ch
310h	8	CONTROLSS_DMAXBAR_DMAXBAR8_G3	RW	502D 6310h
314h	8	CONTROLSS_DMAXBAR_DMAXBAR8_G4	RW	502D 6314h
318h	8	CONTROLSS_DMAXBAR_DMAXBAR8_G5	RW	502D 6318h
340h	8	CONTROLSS_DMAXBAR_DMAXBAR9_GSEL	RW	502D 6340h
344h	8	CONTROLSS_DMAXBAR_DMAXBAR9_G0	RW	502D 6344h
348h	8	CONTROLSS_DMAXBAR_DMAXBAR9_G1	RW	502D 6348h
34Ch	8	CONTROLSS_DMAXBAR_DMAXBAR9_G2	RW	502D 634Ch
350h	8	CONTROLSS_DMAXBAR_DMAXBAR9_G3	RW	502D 6350h
354h	8	CONTROLSS_DMAXBAR_DMAXBAR9_G4	RW	502D 6354h
358h	8	CONTROLSS_DMAXBAR_DMAXBAR9_G5	RW	502D 6358h
380h	8	CONTROLSS_DMAXBAR_DMAXBAR10_GSEL	RW	502D 6380h
384h	8	CONTROLSS_DMAXBAR_DMAXBAR10_G0	RW	502D 6384h

Table 3-487. CONTROLSS_DMAXBAR, CONTROLSS_DMAXBAR_CONTROLSS_DMAXBAR Registers, Base Address=502D 6000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_DMAXBAR Physical Address
388h	8	CONTROLSS_DMAXBAR_DMAXBAR10_G1	RW	502D 6388h
38Ch	8	CONTROLSS_DMAXBAR_DMAXBAR10_G2	RW	502D 638Ch
390h	8	CONTROLSS_DMAXBAR_DMAXBAR10_G3	RW	502D 6390h
394h	8	CONTROLSS_DMAXBAR_DMAXBAR10_G4	RW	502D 6394h
398h	8	CONTROLSS_DMAXBAR_DMAXBAR10_G5	RW	502D 6398h
3C0h	8	CONTROLSS_DMAXBAR_DMAXBAR11_GSEL	RW	502D 63C0h
3C4h	8	CONTROLSS_DMAXBAR_DMAXBAR11_G0	RW	502D 63C4h
3C8h	8	CONTROLSS_DMAXBAR_DMAXBAR11_G1	RW	502D 63C8h
3CCh	8	CONTROLSS_DMAXBAR_DMAXBAR11_G2	RW	502D 63CCh
3D0h	8	CONTROLSS_DMAXBAR_DMAXBAR11_G3	RW	502D 63D0h
3D4h	8	CONTROLSS_DMAXBAR_DMAXBAR11_G4	RW	502D 63D4h
3D8h	8	CONTROLSS_DMAXBAR_DMAXBAR11_G5	RW	502D 63D8h
400h	8	CONTROLSS_DMAXBAR_DMAXBAR12_GSEL	RW	502D 6400h
404h	8	CONTROLSS_DMAXBAR_DMAXBAR12_G0	RW	502D 6404h
408h	8	CONTROLSS_DMAXBAR_DMAXBAR12_G1	RW	502D 6408h
40Ch	8	CONTROLSS_DMAXBAR_DMAXBAR12_G2	RW	502D 640Ch
410h	8	CONTROLSS_DMAXBAR_DMAXBAR12_G3	RW	502D 6410h
414h	8	CONTROLSS_DMAXBAR_DMAXBAR12_G4	RW	502D 6414h
418h	8	CONTROLSS_DMAXBAR_DMAXBAR12_G5	RW	502D 6418h
440h	8	CONTROLSS_DMAXBAR_DMAXBAR13_GSEL	RW	502D 6440h
444h	8	CONTROLSS_DMAXBAR_DMAXBAR13_G0	RW	502D 6444h
448h	8	CONTROLSS_DMAXBAR_DMAXBAR13_G1	RW	502D 6448h
44Ch	8	CONTROLSS_DMAXBAR_DMAXBAR13_G2	RW	502D 644Ch
450h	8	CONTROLSS_DMAXBAR_DMAXBAR13_G3	RW	502D 6450h
454h	8	CONTROLSS_DMAXBAR_DMAXBAR13_G4	RW	502D 6454h
458h	8	CONTROLSS_DMAXBAR_DMAXBAR13_G5	RW	502D 6458h
480h	8	CONTROLSS_DMAXBAR_DMAXBAR14_GSEL	RW	502D 6480h
484h	8	CONTROLSS_DMAXBAR_DMAXBAR14_G0	RW	502D 6484h
488h	8	CONTROLSS_DMAXBAR_DMAXBAR14_G1	RW	502D 6488h
48Ch	8	CONTROLSS_DMAXBAR_DMAXBAR14_G2	RW	502D 648Ch
490h	8	CONTROLSS_DMAXBAR_DMAXBAR14_G3	RW	502D 6490h
494h	8	CONTROLSS_DMAXBAR_DMAXBAR14_G4	RW	502D 6494h
498h	8	CONTROLSS_DMAXBAR_DMAXBAR14_G5	RW	502D 6498h
4C0h	8	CONTROLSS_DMAXBAR_DMAXBAR15_GSEL	RW	502D 64C0h
4C4h	8	CONTROLSS_DMAXBAR_DMAXBAR15_G0	RW	502D 64C4h
4C8h	8	CONTROLSS_DMAXBAR_DMAXBAR15_G1	RW	502D 64C8h
4CCh	8	CONTROLSS_DMAXBAR_DMAXBAR15_G2	RW	502D 64CCh
4D0h	8	CONTROLSS_DMAXBAR_DMAXBAR15_G3	RW	502D 64D0h
4D4h	8	CONTROLSS_DMAXBAR_DMAXBAR15_G4	RW	502D 64D4h
4D8h	8	CONTROLSS_DMAXBAR_DMAXBAR15_G5	RW	502D 64D8h

3.6.1 CONTROLSS_DMAXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-488. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6000h

Figure 3-231. CONTROLSS_DMAXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-489. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.6.2 CONTROLSS_DMAXBAR_DMAXBAR0_GSEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-490. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6100h

Figure 3-232. CONTROLSS_DMAXBAR_DMAXBAR0_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-491. DMAXBAR0_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.3 CONTROLSS_DMAXBAR_DMAXBAR0_G0 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-492. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6104h

Figure 3-233. CONTROLSS_DMAXBAR_DMAXBAR0_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-493. DMAXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.4 CONTROLSS_DMAXBAR_DMAXBAR0_G1 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-494. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6108h

Figure 3-234. CONTROLSS_DMAXBAR_DMAXBAR0_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-495. DMAXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.5 CONTROLSS_DMAXBAR_DMAXBAR0_G2 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-496. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 610Ch

Figure 3-235. CONTROLSS_DMAXBAR_DMAXBAR0_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-497. DMAXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.6 CONTROLSS_DMAXBAR_DMAXBAR0_G3 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-498. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6110h

Figure 3-236. CONTROLSS_DMAXBAR_DMAXBAR0_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-499. DMAXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.7 CONTROLSS_DMAXBAR_DMAXBAR0_G4 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-500. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6114h

Figure 3-237. CONTROLSS_DMAXBAR_DMAXBAR0_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-501. DMAXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.8 CONTROLSS_DMAXBAR_DMAXBAR0_G5 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-502. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6118h

Figure 3-238. CONTROLSS_DMAXBAR_DMAXBAR0_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-503. DMAXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.9 CONTROLSS_DMAXBAR_DMAXBAR1_GSEL Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-504. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6140h

Figure 3-239. CONTROLSS_DMAXBAR_DMAXBAR1_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-505. DMAXBAR1_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.10 CONTROLSS_DMAXBAR_DMAXBAR1_G0 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-506. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6144h

Figure 3-240. CONTROLSS_DMAXBAR_DMAXBAR1_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-507. DMAXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.11 CONTROLSS_DMAXBAR_DMAXBAR1_G1 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-508. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6148h

Figure 3-241. CONTROLSS_DMAXBAR_DMAXBAR1_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-509. DMAXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.12 CONTROLSS_DMAXBAR_DMAXBAR1_G2 Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-510. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 614Ch

Figure 3-242. CONTROLSS_DMAXBAR_DMAXBAR1_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-511. DMAXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.13 CONTROLSS_DMAXBAR_DMAXBAR1_G3 Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-512. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6150h

Figure 3-243. CONTROLSS_DMAXBAR_DMAXBAR1_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-513. DMAXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.14 CONTROLSS_DMAXBAR_DMAXBAR1_G4 Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-514. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6154h

Figure 3-244. CONTROLSS_DMAXBAR_DMAXBAR1_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-515. DMAXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.15 CONTROLSS_DMAXBAR_DMAXBAR1_G5 Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-516. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6158h

Figure 3-245. CONTROLSS_DMAXBAR_DMAXBAR1_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-517. DMAXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.16 CONTROLSS_DMAXBAR_DMAXBAR2_GSEL Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-518. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6180h

Figure 3-246. CONTROLSS_DMAXBAR_DMAXBAR2_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-519. DMAXBAR2_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.17 CONTROLSS_DMAXBAR_DMAXBAR2_G0 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-520. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6184h

Figure 3-247. CONTROLSS_DMAXBAR_DMAXBAR2_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-521. DMAXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.18 CONTROLSS_DMAXBAR_DMAXBAR2_G1 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-522. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6188h

Figure 3-248. CONTROLSS_DMAXBAR_DMAXBAR2_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-523. DMAXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.19 CONTROLSS_DMAXBAR_DMAXBAR2_G2 Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-524. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 618Ch

Figure 3-249. CONTROLSS_DMAXBAR_DMAXBAR2_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-525. DMAXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.20 CONTROLSS_DMAXBAR_DMAXBAR2_G3 Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-526. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6190h

Figure 3-250. CONTROLSS_DMAXBAR_DMAXBAR2_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-527. DMAXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.21 CONTROLSS_DMAXBAR_DMAXBAR2_G4 Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-528. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6194h

Figure 3-251. CONTROLSS_DMAXBAR_DMAXBAR2_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-529. DMAXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.22 CONTROLSS_DMAXBAR_DMAXBAR2_G5 Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-530. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6198h

Figure 3-252. CONTROLSS_DMAXBAR_DMAXBAR2_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-531. DMAXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.23 CONTROLSS_DMAXBAR_DMAXBAR3_GSEL Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-532. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C0h

Figure 3-253. CONTROLSS_DMAXBAR_DMAXBAR3_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-533. DMAXBAR3_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.24 CONTROLSS_DMAXBAR_DMAXBAR3_G0 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-534. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C4h

Figure 3-254. CONTROLSS_DMAXBAR_DMAXBAR3_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-535. DMAXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.25 CONTROLSS_DMAXBAR_DMAXBAR3_G1 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-536. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C8h

Figure 3-255. CONTROLSS_DMAXBAR_DMAXBAR3_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-537. DMAXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.26 CONTROLSS_DMAXBAR_DMAXBAR3_G2 Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-538. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61CCh

Figure 3-256. CONTROLSS_DMAXBAR_DMAXBAR3_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-539. DMAXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.27 CONTROLSS_DMAXBAR_DMAXBAR3_G3 Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-540. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D0h

Figure 3-257. CONTROLSS_DMAXBAR_DMAXBAR3_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-541. DMAXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.28 CONTROLSS_DMAXBAR_DMAXBAR3_G4 Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-542. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D4h

Figure 3-258. CONTROLSS_DMAXBAR_DMAXBAR3_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-543. DMAXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.29 CONTROLSS_DMAXBAR_DMAXBAR3_G5 Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-544. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D8h

Figure 3-259. CONTROLSS_DMAXBAR_DMAXBAR3_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-545. DMAXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.30 CONTROLSS_DMAXBAR_DMAXBAR4_GSEL Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-546. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6200h

Figure 3-260. CONTROLSS_DMAXBAR_DMAXBAR4_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-547. DMAXBAR4_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.31 CONTROLSS_DMAXBAR_DMAXBAR4_G0 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-548. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6204h

Figure 3-261. CONTROLSS_DMAXBAR_DMAXBAR4_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-549. DMAXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.32 CONTROLSS_DMAXBAR_DMAXBAR4_G1 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-550. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6208h

Figure 3-262. CONTROLSS_DMAXBAR_DMAXBAR4_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-551. DMAXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.33 CONTROLSS_DMAXBAR_DMAXBAR4_G2 Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-552. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 620Ch

Figure 3-263. CONTROLSS_DMAXBAR_DMAXBAR4_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-553. DMAXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.34 CONTROLSS_DMAXBAR_DMAXBAR4_G3 Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-554. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6210h

Figure 3-264. CONTROLSS_DMAXBAR_DMAXBAR4_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-555. DMAXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.35 CONTROLSS_DMAXBAR_DMAXBAR4_G4 Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-556. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6214h

Figure 3-265. CONTROLSS_DMAXBAR_DMAXBAR4_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-557. DMAXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.36 CONTROLSS_DMAXBAR_DMAXBAR4_G5 Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-558. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6218h

Figure 3-266. CONTROLSS_DMAXBAR_DMAXBAR4_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-559. DMAXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.37 CONTROLSS_DMAXBAR_DMAXBAR5_GSEL Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-560. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6240h

Figure 3-267. CONTROLSS_DMAXBAR_DMAXBAR5_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-561. DMAXBAR5_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.38 CONTROLSS_DMAXBAR_DMAXBAR5_G0 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-562. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6244h

Figure 3-268. CONTROLSS_DMAXBAR_DMAXBAR5_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-563. DMAXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.39 CONTROLSS_DMAXBAR_DMAXBAR5_G1 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-564. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6248h

Figure 3-269. CONTROLSS_DMAXBAR_DMAXBAR5_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-565. DMAXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.40 CONTROLSS_DMAXBAR_DMAXBAR5_G2 Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-566. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 624Ch

Figure 3-270. CONTROLSS_DMAXBAR_DMAXBAR5_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-567. DMAXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.41 CONTROLSS_DMAXBAR_DMAXBAR5_G3 Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-568. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6250h

Figure 3-271. CONTROLSS_DMAXBAR_DMAXBAR5_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-569. DMAXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.42 CONTROLSS_DMAXBAR_DMAXBAR5_G4 Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-570. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6254h

Figure 3-272. CONTROLSS_DMAXBAR_DMAXBAR5_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-571. DMAXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.43 CONTROLSS_DMAXBAR_DMAXBAR5_G5 Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-572. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6258h

Figure 3-273. CONTROLSS_DMAXBAR_DMAXBAR5_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-573. DMAXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.44 CONTROLSS_DMAXBAR_DMAXBAR6_GSEL Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-574. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6280h

Figure 3-274. CONTROLSS_DMAXBAR_DMAXBAR6_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-575. DMAXBAR6_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.45 CONTROLSS_DMAXBAR_DMAXBAR6_G0 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-576. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6284h

Figure 3-275. CONTROLSS_DMAXBAR_DMAXBAR6_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-577. DMAXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.46 CONTROLSS_DMAXBAR_DMAXBAR6_G1 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-578. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6288h

Figure 3-276. CONTROLSS_DMAXBAR_DMAXBAR6_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-579. DMAXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.47 CONTROLSS_DMAXBAR_DMAXBAR6_G2 Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-580. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 628Ch

Figure 3-277. CONTROLSS_DMAXBAR_DMAXBAR6_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-581. DMAXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.48 CONTROLSS_DMAXBAR_DMAXBAR6_G3 Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-582. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6290h

Figure 3-278. CONTROLSS_DMAXBAR_DMAXBAR6_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-583. DMAXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.49 CONTROLSS_DMAXBAR_DMAXBAR6_G4 Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-584. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6294h

Figure 3-279. CONTROLSS_DMAXBAR_DMAXBAR6_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-585. DMAXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.50 CONTROLSS_DMAXBAR_DMAXBAR6_G5 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-586. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6298h

Figure 3-280. CONTROLSS_DMAXBAR_DMAXBAR6_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-587. DMAXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.51 CONTROLSS_DMAXBAR_DMAXBAR7_GSEL Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-588. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C0h

Figure 3-281. CONTROLSS_DMAXBAR_DMAXBAR7_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-589. DMAXBAR7_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.52 CONTROLSS_DMAXBAR_DMAXBAR7_G0 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-590. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C4h

Figure 3-282. CONTROLSS_DMAXBAR_DMAXBAR7_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-591. DMAXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.53 CONTROLSS_DMAXBAR_DMAXBAR7_G1 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-592. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C8h

Figure 3-283. CONTROLSS_DMAXBAR_DMAXBAR7_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-593. DMAXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.54 CONTROLSS_DMAXBAR_DMAXBAR7_G2 Register (Offset = 2CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-594. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62CCh

Figure 3-284. CONTROLSS_DMAXBAR_DMAXBAR7_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-595. DMAXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.55 CONTROLSS_DMAXBAR_DMAXBAR7_G3 Register (Offset = 2D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-596. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D0h

Figure 3-285. CONTROLSS_DMAXBAR_DMAXBAR7_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-597. DMAXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.56 CONTROLSS_DMAXBAR_DMAXBAR7_G4 Register (Offset = 2D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-598. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D4h

Figure 3-286. CONTROLSS_DMAXBAR_DMAXBAR7_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-599. DMAXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.57 CONTROLSS_DMAXBAR_DMAXBAR7_G5 Register (Offset = 2D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-600. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D8h

Figure 3-287. CONTROLSS_DMAXBAR_DMAXBAR7_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-601. DMAXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.58 CONTROLSS_DMAXBAR_DMAXBAR8_GSEL Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-602. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6300h

Figure 3-288. CONTROLSS_DMAXBAR_DMAXBAR8_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-603. DMAXBAR8_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.59 CONTROLSS_DMAXBAR_DMAXBAR8_G0 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-604. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6304h

Figure 3-289. CONTROLSS_DMAXBAR_DMAXBAR8_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-605. DMAXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.60 CONTROLSS_DMAXBAR_DMAXBAR8_G1 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-606. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6308h

Figure 3-290. CONTROLSS_DMAXBAR_DMAXBAR8_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-607. DMAXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.61 CONTROLSS_DMAXBAR_DMAXBAR8_G2 Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-608. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 630Ch

Figure 3-291. CONTROLSS_DMAXBAR_DMAXBAR8_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-609. DMAXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.62 CONTROLSS_DMAXBAR_DMAXBAR8_G3 Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-610. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6310h

Figure 3-292. CONTROLSS_DMAXBAR_DMAXBAR8_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-611. DMAXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.63 CONTROLSS_DMAXBAR_DMAXBAR8_G4 Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-612. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6314h

Figure 3-293. CONTROLSS_DMAXBAR_DMAXBAR8_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-613. DMAXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.64 CONTROLSS_DMAXBAR_DMAXBAR8_G5 Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-614. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6318h

Figure 3-294. CONTROLSS_DMAXBAR_DMAXBAR8_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-615. DMAXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.65 CONTROLSS_DMAXBAR_DMAXBAR9_GSEL Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-616. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6340h

Figure 3-295. CONTROLSS_DMAXBAR_DMAXBAR9_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-617. DMAXBAR9_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.66 CONTROLSS_DMAXBAR_DMAXBAR9_G0 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-618. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6344h

Figure 3-296. CONTROLSS_DMAXBAR_DMAXBAR9_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-619. DMAXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.67 CONTROLSS_DMAXBAR_DMAXBAR9_G1 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-620. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6348h

Figure 3-297. CONTROLSS_DMAXBAR_DMAXBAR9_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-621. DMAXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.68 CONTROLSS_DMAXBAR_DMAXBAR9_G2 Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-622. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 634Ch

Figure 3-298. CONTROLSS_DMAXBAR_DMAXBAR9_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-623. DMAXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.69 CONTROLSS_DMAXBAR_DMAXBAR9_G3 Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-624. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6350h

Figure 3-299. CONTROLSS_DMAXBAR_DMAXBAR9_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-625. DMAXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.70 CONTROLSS_DMAXBAR_DMAXBAR9_G4 Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-626. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6354h

Figure 3-300. CONTROLSS_DMAXBAR_DMAXBAR9_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-627. DMAXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.71 CONTROLSS_DMAXBAR_DMAXBAR9_G5 Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-628. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6358h

Figure 3-301. CONTROLSS_DMAXBAR_DMAXBAR9_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-629. DMAXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.72 CONTROLSS_DMAXBAR_DMAXBAR10_GSEL Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-630. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6380h

Figure 3-302. CONTROLSS_DMAXBAR_DMAXBAR10_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-631. DMAXBAR10_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.73 CONTROLSS_DMAXBAR_DMAXBAR10_G0 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-632. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6384h

Figure 3-303. CONTROLSS_DMAXBAR_DMAXBAR10_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-633. DMAXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.74 CONTROLSS_DMAXBAR_DMAXBAR10_G1 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-634. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6388h

Figure 3-304. CONTROLSS_DMAXBAR_DMAXBAR10_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-635. DMAXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.75 CONTROLSS_DMAXBAR_DMAXBAR10_G2 Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-636. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 638Ch

Figure 3-305. CONTROLSS_DMAXBAR_DMAXBAR10_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-637. DMAXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.76 CONTROLSS_DMAXBAR_DMAXBAR10_G3 Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-638. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6390h

Figure 3-306. CONTROLSS_DMAXBAR_DMAXBAR10_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-639. DMAXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.77 CONTROLSS_DMAXBAR_DMAXBAR10_G4 Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-640. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6394h

Figure 3-307. CONTROLSS_DMAXBAR_DMAXBAR10_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-641. DMAXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.78 CONTROLSS_DMAXBAR_DMAXBAR10_G5 Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-642. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6398h

Figure 3-308. CONTROLSS_DMAXBAR_DMAXBAR10_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-643. DMAXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.79 CONTROLSS_DMAXBAR_DMAXBAR11_GSEL Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-644. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C0h

Figure 3-309. CONTROLSS_DMAXBAR_DMAXBAR11_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-645. DMAXBAR11_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.80 CONTROLSS_DMAXBAR_DMAXBAR11_G0 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-646. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C4h

Figure 3-310. CONTROLSS_DMAXBAR_DMAXBAR11_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-647. DMAXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.81 CONTROLSS_DMAXBAR_DMAXBAR11_G1 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-648. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C8h

Figure 3-311. CONTROLSS_DMAXBAR_DMAXBAR11_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-649. DMAXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.82 CONTROLSS_DMAXBAR_DMAXBAR11_G2 Register (Offset = 3CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-650. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63CCh

Figure 3-312. CONTROLSS_DMAXBAR_DMAXBAR11_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-651. DMAXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.83 CONTROLSS_DMAXBAR_DMAXBAR11_G3 Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-652. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D0h

Figure 3-313. CONTROLSS_DMAXBAR_DMAXBAR11_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-653. DMAXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.84 CONTROLSS_DMAXBAR_DMAXBAR11_G4 Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-654. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D4h

Figure 3-314. CONTROLSS_DMAXBAR_DMAXBAR11_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-655. DMAXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.85 CONTROLSS_DMAXBAR_DMAXBAR11_G5 Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-656. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D8h

Figure 3-315. CONTROLSS_DMAXBAR_DMAXBAR11_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-657. DMAXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.86 CONTROLSS_DMAXBAR_DMAXBAR12_GSEL Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-658. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6400h

Figure 3-316. CONTROLSS_DMAXBAR_DMAXBAR12_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-659. DMAXBAR12_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.87 CONTROLSS_DMAXBAR_DMAXBAR12_G0 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-660. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6404h

Figure 3-317. CONTROLSS_DMAXBAR_DMAXBAR12_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-661. DMAXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.88 CONTROLSS_DMAXBAR_DMAXBAR12_G1 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-662. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6408h

Figure 3-318. CONTROLSS_DMAXBAR_DMAXBAR12_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-663. DMAXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.89 CONTROLSS_DMAXBAR_DMAXBAR12_G2 Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-664. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 640Ch

Figure 3-319. CONTROLSS_DMAXBAR_DMAXBAR12_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-665. DMAXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.90 CONTROLSS_DMAXBAR_DMAXBAR12_G3 Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-666. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6410h

Figure 3-320. CONTROLSS_DMAXBAR_DMAXBAR12_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-667. DMAXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.91 CONTROLSS_DMAXBAR_DMAXBAR12_G4 Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-668. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6414h

Figure 3-321. CONTROLSS_DMAXBAR_DMAXBAR12_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-669. DMAXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.92 CONTROLSS_DMAXBAR_DMAXBAR12_G5 Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-670. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6418h

Figure 3-322. CONTROLSS_DMAXBAR_DMAXBAR12_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-671. DMAXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.93 CONTROLSS_DMAXBAR_DMAXBAR13_GSEL Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-672. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6440h

Figure 3-323. CONTROLSS_DMAXBAR_DMAXBAR13_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-673. DMAXBAR13_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.94 CONTROLSS_DMAXBAR_DMAXBAR13_G0 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-674. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6444h

Figure 3-324. CONTROLSS_DMAXBAR_DMAXBAR13_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-675. DMAXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.95 CONTROLSS_DMAXBAR_DMAXBAR13_G1 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-676. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6448h

Figure 3-325. CONTROLSS_DMAXBAR_DMAXBAR13_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-677. DMAXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.96 CONTROLSS_DMAXBAR_DMAXBAR13_G2 Register (Offset = 44Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-678. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 644Ch

Figure 3-326. CONTROLSS_DMAXBAR_DMAXBAR13_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-679. DMAXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.97 CONTROLSS_DMAXBAR_DMAXBAR13_G3 Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

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Table 3-680. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6450h

Figure 3-327. CONTROLSS_DMAXBAR_DMAXBAR13_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-681. DMAXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.98 CONTROLSS_DMAXBAR_DMAXBAR13_G4 Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-682. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6454h

Figure 3-328. CONTROLSS_DMAXBAR_DMAXBAR13_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-683. DMAXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.99 CONTROLSS_DMAXBAR_DMAXBAR13_G5 Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-684. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6458h

Figure 3-329. CONTROLSS_DMAXBAR_DMAXBAR13_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-685. DMAXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.100 CONTROLSS_DMAXBAR_DMAXBAR14_GSEL Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-686. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6480h

Figure 3-330. CONTROLSS_DMAXBAR_DMAXBAR14_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-687. DMAXBAR14_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.101 CONTROLSS_DMAXBAR_DMAXBAR14_G0 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-688. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6484h

Figure 3-331. CONTROLSS_DMAXBAR_DMAXBAR14_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-689. DMAXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.102 CONTROLSS_DMAXBAR_DMAXBAR14_G1 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-690. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6488h

Figure 3-332. CONTROLSS_DMAXBAR_DMAXBAR14_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-691. DMAXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.103 CONTROLSS_DMAXBAR_DMAXBAR14_G2 Register (Offset = 48Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-692. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 648Ch

Figure 3-333. CONTROLSS_DMAXBAR_DMAXBAR14_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-693. DMAXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.104 CONTROLSS_DMAXBAR_DMAXBAR14_G3 Register (Offset = 490h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-694. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6490h

Figure 3-334. CONTROLSS_DMAXBAR_DMAXBAR14_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-695. DMAXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.105 CONTROLSS_DMAXBAR_DMAXBAR14_G4 Register (Offset = 494h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-696. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6494h

Figure 3-335. CONTROLSS_DMAXBAR_DMAXBAR14_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-697. DMAXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.106 CONTROLSS_DMAXBAR_DMAXBAR14_G5 Register (Offset = 498h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-698. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6498h

Figure 3-336. CONTROLSS_DMAXBAR_DMAXBAR14_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-699. DMAXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.6.107 CONTROLSS_DMAXBAR_DMAXBAR15_GSEL Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-700. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C0h

Figure 3-337. CONTROLSS_DMAXBAR_DMAXBAR15_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					GSEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-701. DMAXBAR15_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

3.6.108 CONTROLSS_DMAXBAR_DMAXBAR15_G0 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-702. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C4h

Figure 3-338. CONTROLSS_DMAXBAR_DMAXBAR15_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-703. DMAXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

3.6.109 CONTROLSS_DMAXBAR_DMAXBAR15_G1 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-704. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C8h

Figure 3-339. CONTROLSS_DMAXBAR_DMAXBAR15_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-705. DMAXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

3.6.110 CONTROLSS_DMAXBAR_DMAXBAR15_G2 Register (Offset = 4CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-706. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64CCh

Figure 3-340. CONTROLSS_DMAXBAR_DMAXBAR15_G2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-707. DMAXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.6.111 CONTROLSS_DMAXBAR_DMAXBAR15_G3 Register (Offset = 4D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-708. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D0h

Figure 3-341. CONTROLSS_DMAXBAR_DMAXBAR15_G3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-709. DMAXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

3.6.112 CONTROLSS_DMAXBAR_DMAXBAR15_G4 Register (Offset = 4D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-710. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D4h

Figure 3-342. CONTROLSS_DMAXBAR_DMAXBAR15_G4 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-711. DMAXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

3.6.113 CONTROLSS_DMAXBAR_DMAXBAR15_G5 Register (Offset = 4D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-712. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D8h

Figure 3-343. CONTROLSS_DMAXBAR_DMAXBAR15_G5 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-713. DMAXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

Table 3-714. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.7 C2K_ECAP Registers

Table 3-715. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP0 Physical Address	CONTROLSS_ECAP1 Physical Address	CONTROLSS_ECAP2 Physical Address
0h	32	CONTROLSS_ECAP0_TSCTR	Time-Stamp Counter	5024 0000h	5024 1000h	5024 2000h
4h	32	CONTROLSS_ECAP0_CTRPHS	Counter Phase Offset Value Register	5024 0004h	5024 1004h	5024 2004h
8h	32	CONTROLSS_ECAP0_CAP1	Capture 1 Register	5024 0008h	5024 1008h	5024 2008h
Ch	32	CONTROLSS_ECAP0_CAP2	Capture 2 Register	5024 000Ch	5024 100Ch	5024 200Ch
10h	32	CONTROLSS_ECAP0_CAP3	Capture 3 Register	5024 0010h	5024 1010h	5024 2010h
14h	32	CONTROLSS_ECAP0_CAP4	Capture 4 Register	5024 0014h	5024 1014h	5024 2014h
24h	32	CONTROLSS_ECAP0_ECCTL0	Capture Control Register 0	5024 0024h	5024 1024h	5024 2024h
28h	16	CONTROLSS_ECAP0_ECCTL1	Capture Control Register 1	5024 0028h	5024 1028h	5024 2028h
2Ah	16	CONTROLSS_ECAP0_ECCTL2	Capture Control Register 2	5024 002Ah	5024 102Ah	5024 202Ah
2Ch	16	CONTROLSS_ECAP0_ECEINT	The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts	5024 002Ch	5024 102Ch	5024 202Ch
2Eh	16	CONTROLSS_ECAP0_ECFLG	Capture Interrupt Flag Register	5024 002Eh	5024 102Eh	5024 202Eh
30h	16	CONTROLSS_ECAP0_ECCLR	Capture Interrupt Clear Register	5024 0030h	5024 1030h	5024 2030h
32h	16	CONTROLSS_ECAP0_ECFRC	Capture Interrupt Force Register	5024 0032h	5024 1032h	5024 2032h

Table 3-715. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP0 Physical Address	CONTROLSS_ECAP1 Physical Address	CONTROLSS_ECAP2 Physical Address
3Ch	32	CONTROLSS_ECAP0_ECAPSYNCINSEL	SYNC source select register	5024 003Ch	5024 103Ch	5024 203Ch
40h	32	CONTROLSS_ECAP0_HRCTL	High-Res Control Register	5024 0040h	5024 1040h	5024 2040h
48h	32	CONTROLSS_ECAP0_HRINTEN	High-Res Calibration Interrupt Enable Register	5024 0048h	5024 1048h	5024 2048h
4Ch	32	CONTROLSS_ECAP0_HRFLG	High-Res Calibration Interrupt Flag Register	5024 004Ch	5024 104Ch	5024 204Ch
50h	32	CONTROLSS_ECAP0_HRCLR	High-Res Calibration Interrupt Clear Register	5024 0050h	5024 1050h	5024 2050h
54h	32	CONTROLSS_ECAP0_HRFRC	High-Res Calibration Interrupt Force Register	5024 0054h	5024 1054h	5024 2054h
58h	32	CONTROLSS_ECAP0_HRCALPRD	High-Res Calibration Period Register	5024 0058h	5024 1058h	5024 2058h
5Ch	32	CONTROLSS_ECAP0_HRSYSCLKCTR	High-Res Calibration SYSCLK Counter Register	5024 005Ch	5024 105Ch	5024 205Ch
60h	32	CONTROLSS_ECAP0_HRSYSCLKCAP	High-Res Calibration SYSCLK Capture Register	5024 0060h	5024 1060h	5024 2060h
64h	32	CONTROLSS_ECAP0_HRCLKCTR	High-Res Calibration HRCLK Counter Register	5024 0064h	5024 1064h	5024 2064h
68h	32	CONTROLSS_ECAP0_HRCLKCAP	High-Res Calibration HRCLK Capture Register	5024 0068h	5024 1068h	5024 2068h
74h	32	CONTROLSS_ECAP0_HRDEBUGCTL	High-Res Debug control register	5024 0074h	5024 1074h	5024 2074h
78h	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE1	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 0078h	5024 1078h	5024 2078h
7Ch	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE2	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 007Ch	5024 107Ch	5024 207Ch
80h	32	CONTROLSS_ECAP0_MUNIT_COMMON_CTL	Control registers for monitoring unit {#}	5024 0080h	5024 1080h	5024 2080h
C0h	32	CONTROLSS_ECAP0_MUNIT_1_CTL	Control registers for monitoring unit 1	5024 00C0h	5024 10C0h	5024 20C0h
C4h	32	CONTROLSS_ECAP0_MUNIT_1_SHADOW_CTL	Shadow control registers for monitoring unit 1	5024 00C4h	5024 10C4h	5024 20C4h
D0h	32	CONTROLSS_ECAP0_MUNIT_1_MIN	Min value for monitoring unit 1	5024 00D0h	5024 10D0h	5024 20D0h
D4h	32	CONTROLSS_ECAP0_MUNIT_1_MAX	Max value for monitoring unit 1	5024 00D4h	5024 10D4h	5024 20D4h
D8h	32	CONTROLSS_ECAP0_MUNIT_1_MIN_SHADOW	Shadow register for Min value of monitoring unit 1	5024 00D8h	5024 10D8h	5024 20D8h

Table 3-715. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP0 Physical Address	CONTROLSS_ECAP1 Physical Address	CONTROLSS_ECAP2 Physical Address
DCh	32	CONTROLSS_ECAP0_MUNIT_1_MAX_SHADOW	Shadow register for Max value of monitoring unit 1	5024 00DCh	5024 10DCh	5024 20DCh
E0h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 1	5024 00E0h	5024 10E0h	5024 20E0h
E4h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 1	5024 00E4h	5024 10E4h	5024 20E4h
100h	32	CONTROLSS_ECAP0_MUNIT_2_CTL	Control registers for monitoring unit 2	5024 0100h	5024 1100h	5024 2100h
104h	32	CONTROLSS_ECAP0_MUNIT_2_SHADOW_CTL	Shadow control registers for monitoring unit 2	5024 0104h	5024 1104h	5024 2104h
110h	32	CONTROLSS_ECAP0_MUNIT_2_MIN	Min value for monitoring unit 2	5024 0110h	5024 1110h	5024 2110h
114h	32	CONTROLSS_ECAP0_MUNIT_2_MAX	Max value for monitoring unit 2	5024 0114h	5024 1114h	5024 2114h
118h	32	CONTROLSS_ECAP0_MUNIT_2_MIN_SHADOW	Shadow register for Min value of monitoring unit 2	5024 0118h	5024 1118h	5024 2118h
11Ch	32	CONTROLSS_ECAP0_MUNIT_2_MAX_SHADOW	Shadow register for Max value of monitoring unit 2	5024 011Ch	5024 111Ch	5024 211Ch
120h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 2	5024 0120h	5024 1120h	5024 2120h
124h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 2	5024 0124h	5024 1124h	5024 2124h

Table 3-716. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
0h	32	CONTROLSS_ECAP0_TSCTR	Time-Stamp Counter	5024 3000h	5024 4000h	5024 5000h
4h	32	CONTROLSS_ECAP0_CTRPHS	Counter Phase Offset Value Register	5024 3004h	5024 4004h	5024 5004h
8h	32	CONTROLSS_ECAP0_CAP1	Capture 1 Register	5024 3008h	5024 4008h	5024 5008h
Ch	32	CONTROLSS_ECAP0_CAP2	Capture 2 Register	5024 300Ch	5024 400Ch	5024 500Ch
10h	32	CONTROLSS_ECAP0_CAP3	Capture 3 Register	5024 3010h	5024 4010h	5024 5010h
14h	32	CONTROLSS_ECAP0_CAP4	Capture 4 Register	5024 3014h	5024 4014h	5024 5014h
24h	32	CONTROLSS_ECAP0_ECCTL0	Capture Control Register 0	5024 3024h	5024 4024h	5024 5024h
28h	16	CONTROLSS_ECAP0_ECCTL1	Capture Control Register 1	5024 3028h	5024 4028h	5024 5028h
2Ah	16	CONTROLSS_ECAP0_ECCTL2	Capture Control Register 2	5024 302Ah	5024 402Ah	5024 502Ah

Table 3-716. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
2Ch	16	CONTROLSS_ECAP0_ECEINT	The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts	5024 302Ch	5024 402Ch	5024 502Ch
2Eh	16	CONTROLSS_ECAP0_ECFLG	Capture Interrupt Flag Register	5024 302Eh	5024 402Eh	5024 502Eh
30h	16	CONTROLSS_ECAP0_ECCLR	Capture Interrupt Clear Register	5024 3030h	5024 4030h	5024 5030h
32h	16	CONTROLSS_ECAP0_ECFRC	Capture Interrupt Force Register	5024 3032h	5024 4032h	5024 5032h
3Ch	32	CONTROLSS_ECAP0_ECAPSYNCINSEL	SYNC source select register	5024 303Ch	5024 403Ch	5024 503Ch
40h	32	CONTROLSS_ECAP0_HRCTL	High-Res Control Register	5024 3040h	5024 4040h	5024 5040h
48h	32	CONTROLSS_ECAP0_HRINTEN	High-Res Calibration Interrupt Enable Register	5024 3048h	5024 4048h	5024 5048h
4Ch	32	CONTROLSS_ECAP0_HRFLG	High-Res Calibration Interrupt Flag Register	5024 304Ch	5024 404Ch	5024 504Ch
50h	32	CONTROLSS_ECAP0_HRCLR	High-Res Calibration Interrupt Clear Register	5024 3050h	5024 4050h	5024 5050h
54h	32	CONTROLSS_ECAP0_HRFRC	High-Res Calibration Interrupt Force Register	5024 3054h	5024 4054h	5024 5054h
58h	32	CONTROLSS_ECAP0_HRCALPRD	High-Res Calibration Period Register	5024 3058h	5024 4058h	5024 5058h
5Ch	32	CONTROLSS_ECAP0_HRSYSCLKCTR	High-Res Calibration SYSCLK Counter Register	5024 305Ch	5024 405Ch	5024 505Ch
60h	32	CONTROLSS_ECAP0_HRSYSCLKCAP	High-Res Calibration SYSCLK Capture Register	5024 3060h	5024 4060h	5024 5060h

Table 3-716. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
64h	32	CONTROLSS_ECAP0_HRCLKCTR	High-Res Calibration HRCLK Counter Register	5024 3064h	5024 4064h	5024 5064h
68h	32	CONTROLSS_ECAP0_HRCLKCAP	High-Res Calibration HRCLK Capture Register	5024 3068h	5024 4068h	5024 5068h
74h	32	CONTROLSS_ECAP0_HRDEBUGCTL	High-Res Debug control register	5024 3074h	5024 4074h	5024 5074h
78h	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE1	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 3078h	5024 4078h	5024 5078h
7Ch	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE2	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 307Ch	5024 407Ch	5024 507Ch
80h	32	CONTROLSS_ECAP0_MUNIT_COMMON_CTL	Control registers for monitoring unit {#}	5024 3080h	5024 4080h	5024 5080h
C0h	32	CONTROLSS_ECAP0_MUNIT_1_CTL	Control registers for monitoring unit 1	5024 30C0h	5024 40C0h	5024 50C0h
C4h	32	CONTROLSS_ECAP0_MUNIT_1_SHADOW_CTL	Shadow control registers for monitoring unit 1	5024 30C4h	5024 40C4h	5024 50C4h
D0h	32	CONTROLSS_ECAP0_MUNIT_1_MIN	Min value for monitoring unit 1	5024 30D0h	5024 40D0h	5024 50D0h
D4h	32	CONTROLSS_ECAP0_MUNIT_1_MAX	Max value for monitoring unit 1	5024 30D4h	5024 40D4h	5024 50D4h
D8h	32	CONTROLSS_ECAP0_MUNIT_1_MIN_SHADOW	Shadow register for Min value of monitoring unit 1	5024 30D8h	5024 40D8h	5024 50D8h
DCh	32	CONTROLSS_ECAP0_MUNIT_1_MAX_SHADOW	Shadow register for Max value of monitoring unit 1	5024 30DCh	5024 40DCh	5024 50DCh
E0h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 1	5024 30E0h	5024 40E0h	5024 50E0h
E4h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 1	5024 30E4h	5024 40E4h	5024 50E4h
100h	32	CONTROLSS_ECAP0_MUNIT_2_CTL	Control registers for monitoring unit 2	5024 3100h	5024 4100h	5024 5100h
104h	32	CONTROLSS_ECAP0_MUNIT_2_SHADOW_CTL	Shadow control registers for monitoring unit 2	5024 3104h	5024 4104h	5024 5104h
110h	32	CONTROLSS_ECAP0_MUNIT_2_MIN	Min value for monitoring unit 2	5024 3110h	5024 4110h	5024 5110h
114h	32	CONTROLSS_ECAP0_MUNIT_2_MAX	Max value for monitoring unit 2	5024 3114h	5024 4114h	5024 5114h
118h	32	CONTROLSS_ECAP0_MUNIT_2_MIN_SHADOW	Shadow register for Min value of monitoring unit 2	5024 3118h	5024 4118h	5024 5118h
11Ch	32	CONTROLSS_ECAP0_MUNIT_2_MAX_SHADOW	Shadow register for Max value of monitoring unit 2	5024 311Ch	5024 411Ch	5024 511Ch

Table 3-716. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
120h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 2	5024 3120h	5024 4120h	5024 5120h
124h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 2	5024 3124h	5024 4124h	5024 5124h

Table 3-717. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP6 Physical Address	CONTROLSS_ECAP7 Physical Address	CONTROLSS_ECAP8 Physical Address
0h	32	CONTROLSS_ECAP0_TSCTR	Time-Stamp Counter	5024 6000h	5024 7000h	5024 8000h
4h	32	CONTROLSS_ECAP0_CTRPHS	Counter Phase Offset Value Register	5024 6004h	5024 7004h	5024 8004h
8h	32	CONTROLSS_ECAP0_CAP1	Capture 1 Register	5024 6008h	5024 7008h	5024 8008h
Ch	32	CONTROLSS_ECAP0_CAP2	Capture 2 Register	5024 600Ch	5024 700Ch	5024 800Ch
10h	32	CONTROLSS_ECAP0_CAP3	Capture 3 Register	5024 6010h	5024 7010h	5024 8010h
14h	32	CONTROLSS_ECAP0_CAP4	Capture 4 Register	5024 6014h	5024 7014h	5024 8014h
24h	32	CONTROLSS_ECAP0_ECCTL0	Capture Control Register 0	5024 6024h	5024 7024h	5024 8024h
28h	16	CONTROLSS_ECAP0_ECCTL1	Capture Control Register 1	5024 6028h	5024 7028h	5024 8028h
2Ah	16	CONTROLSS_ECAP0_ECCTL2	Capture Control Register 2	5024 602Ah	5024 702Ah	5024 802Ah
2Ch	16	CONTROLSS_ECAP0_ECEINT	The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts	5024 602Ch	5024 702Ch	5024 802Ch
2Eh	16	CONTROLSS_ECAP0_ECFLG	Capture Interrupt Flag Register	5024 602Eh	5024 702Eh	5024 802Eh

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Table 3-717. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP6 Physical Address	CONTROLSS_ECAP7 Physical Address	CONTROLSS_ECAP8 Physical Address
30h	16	CONTROLSS_ECAP0_ECCLR	Capture Interrupt Clear Register	5024 6030h	5024 7030h	5024 8030h
32h	16	CONTROLSS_ECAP0_ECFRC	Capture Interrupt Force Register	5024 6032h	5024 7032h	5024 8032h
3Ch	32	CONTROLSS_ECAP0_ECAPSYNCINSEL	SYNC source select register	5024 603Ch	5024 703Ch	5024 803Ch
40h	32	CONTROLSS_ECAP0_HRCTL	High-Res Control Register	5024 6040h	5024 7040h	5024 8040h
48h	32	CONTROLSS_ECAP0_HRINTEN	High-Res Calibration Interrupt Enable Register	5024 6048h	5024 7048h	5024 8048h
4Ch	32	CONTROLSS_ECAP0_HRFLG	High-Res Calibration Interrupt Flag Register	5024 604Ch	5024 704Ch	5024 804Ch
50h	32	CONTROLSS_ECAP0_HRCLR	High-Res Calibration Interrupt Clear Register	5024 6050h	5024 7050h	5024 8050h
54h	32	CONTROLSS_ECAP0_HRFRC	High-Res Calibration Interrupt Force Register	5024 6054h	5024 7054h	5024 8054h
58h	32	CONTROLSS_ECAP0_HRCALPRD	High-Res Calibration Period Register	5024 6058h	5024 7058h	5024 8058h
5Ch	32	CONTROLSS_ECAP0_HRSYSCLKCTR	High-Res Calibration SYSCLK Counter Register	5024 605Ch	5024 705Ch	5024 805Ch
60h	32	CONTROLSS_ECAP0_HRSYSCLKCAP	High-Res Calibration SYSCLK Capture Register	5024 6060h	5024 7060h	5024 8060h
64h	32	CONTROLSS_ECAP0_HRCLKCTR	High-Res Calibration HRCLK Counter Register	5024 6064h	5024 7064h	5024 8064h
68h	32	CONTROLSS_ECAP0_HRCLKCAP	High-Res Calibration HRCLK Capture Register	5024 6068h	5024 7068h	5024 8068h
74h	32	CONTROLSS_ECAP0_HRDEBUGCTL	High-Res Debug control register	5024 6074h	5024 7074h	5024 8074h
78h	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE1	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 6078h	5024 7078h	5024 8078h
7Ch	32	CONTROLSS_ECAP0_HRDEBUGOBSERVE2	High-Res Raw output & internal nodes of HRCLK capture delay line	5024 607Ch	5024 707Ch	5024 807Ch
80h	32	CONTROLSS_ECAP0_MUNIT_COMMON_CTL	Control registers for monitoring unit {#}	5024 6080h	5024 7080h	5024 8080h
C0h	32	CONTROLSS_ECAP0_MUNIT_1_CTL	Control registers for monitoring unit 1	5024 60C0h	5024 70C0h	5024 80C0h
C4h	32	CONTROLSS_ECAP0_MUNIT_1_SHADOW_CTL	Shadow control registers for monitoring unit 1	5024 60C4h	5024 70C4h	5024 80C4h
D0h	32	CONTROLSS_ECAP0_MUNIT_1_MIN	Min value for monitoring unit 1	5024 60D0h	5024 70D0h	5024 80D0h
D4h	32	CONTROLSS_ECAP0_MUNIT_1_MAX	Max value for monitoring unit 1	5024 60D4h	5024 70D4h	5024 80D4h

Table 3-717. CONTROLSS_ECAP0, CONTROLSS_ECAP0_CONTROLSS_ECAP Registers, Base Address=5024 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ECAP6 Physical Address	CONTROLSS_ECAP7 Physical Address	CONTROLSS_ECAP8 Physical Address
D8h	32	CONTROLSS_ECAP0_MUNIT_1_MIN_SHADOW	Shadow register for Min value of monitoring unit 1	5024 60D8h	5024 70D8h	5024 80D8h
DCh	32	CONTROLSS_ECAP0_MUNIT_1_MAX_SHADOW	Shadow register for Max value of monitoring unit 1	5024 60DCh	5024 70DCh	5024 80DCh
E0h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 1	5024 60E0h	5024 70E0h	5024 80E0h
E4h	32	CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 1	5024 60E4h	5024 70E4h	5024 80E4h
100h	32	CONTROLSS_ECAP0_MUNIT_2_CTL	Control registers for monitoring unit 2	5024 6100h	5024 7100h	5024 8100h
104h	32	CONTROLSS_ECAP0_MUNIT_2_SHADOW_CTL	Shadow control registers for monitoring unit 2	5024 6104h	5024 7104h	5024 8104h
110h	32	CONTROLSS_ECAP0_MUNIT_2_MIN	Min value for monitoring unit 2	5024 6110h	5024 7110h	5024 8110h
114h	32	CONTROLSS_ECAP0_MUNIT_2_MAX	Max value for monitoring unit 2	5024 6114h	5024 7114h	5024 8114h
118h	32	CONTROLSS_ECAP0_MUNIT_2_MIN_SHADOW	Shadow register for Min value of monitoring unit 2	5024 6118h	5024 7118h	5024 8118h
11Ch	32	CONTROLSS_ECAP0_MUNIT_2_MAX_SHADOW	Shadow register for Max value of monitoring unit 2	5024 611Ch	5024 711Ch	5024 811Ch
120h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MIN	Observed Min value of check being enabled on minotoring unit 2	5024 6120h	5024 7120h	5024 8120h
124h	32	CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MAX	Observed Max value of check being enabled on minotoring unit 2	5024 6124h	5024 7124h	5024 8124h

3.7.1 CONTROLSS_ECAP0_TSCTR Register (Offset = 0h) [reset = h]

Short Description: Time-Stamp Counter

Long Description:

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Table 3-718. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0000h
CONTROLSS_ECAP1	5024 1000h
CONTROLSS_ECAP2	5024 2000h
CONTROLSS_ECAP3	5024 3000h
CONTROLSS_ECAP4	5024 4000h
CONTROLSS_ECAP5	5024 5000h
CONTROLSS_ECAP6	5024 6000h
CONTROLSS_ECAP7	5024 7000h
CONTROLSS_ECAP8	5024 8000h
CONTROLSS_ECAP9	5024 9000h

Figure 3-344. CONTROLSS_ECAP0_TSCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSCTR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCTR															
RW															
0															

Access Types Legend

Table 3-719. TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TSCTR	RW	0h	Active 32-bit counter register that is used as the capture time-base HR mode : 1) This register reads HRCOUNTER value and is not writable 2) can be reset using CTRFILTRESET 3) Its not synchronized to SYSCLK domain so reads may not be accurate

3.7.2 CONTROLSS_ECAP0_CTRPHS Register (Offset = 4h) [reset = h]

Short Description: Counter Phase Offset Value Register

Long Description:

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Table 3-720. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0004h
CONTROLSS_ECAP1	5024 1004h
CONTROLSS_ECAP2	5024 2004h
CONTROLSS_ECAP3	5024 3004h
CONTROLSS_ECAP4	5024 4004h
CONTROLSS_ECAP5	5024 5004h
CONTROLSS_ECAP6	5024 6004h
CONTROLSS_ECAP7	5024 7004h
CONTROLSS_ECAP8	5024 8004h
CONTROLSS_ECAP9	5024 9004h

Figure 3-345. CONTROLSS_ECAP0_CTRPHS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTRPHS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRPHS															
RW															
0															

Access Types Legend

Table 3-721. CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CTRPHS	RW	0h	Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases. This register is not applicable in HR mode.

3.7.3 CONTROLSS_ECAP0_CAP1 Register (Offset = 8h) [reset = h]

Short Description: Capture 1 Register

Long Description:

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Table 3-722. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0008h
CONTROLSS_ECAP1	5024 1008h
CONTROLSS_ECAP2	5024 2008h
CONTROLSS_ECAP3	5024 3008h
CONTROLSS_ECAP4	5024 4008h
CONTROLSS_ECAP5	5024 5008h
CONTROLSS_ECAP6	5024 6008h
CONTROLSS_ECAP7	5024 7008h
CONTROLSS_ECAP8	5024 8008h
CONTROLSS_ECAP9	5024 9008h

Figure 3-346. CONTROLSS_ECAP0_CAP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1															
RW															
0															

Access Types Legend

Table 3-723. CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP1	RW	0h	This register can be loaded (written) by: - Time-Stamp counter value (TSCTR) during a capture event - Software - may be useful for test purposes or initialization - ARPD shadow register (CAP3) when used in APWM mode

3.7.4 CONTROLSS_ECAP0_CAP2 Register (Offset = Ch) [reset = h]

Short Description: Capture 2 Register

Long Description:

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Table 3-724. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 000Ch
CONTROLSS_ECAP1	5024 100Ch
CONTROLSS_ECAP2	5024 200Ch
CONTROLSS_ECAP3	5024 300Ch
CONTROLSS_ECAP4	5024 400Ch
CONTROLSS_ECAP5	5024 500Ch
CONTROLSS_ECAP6	5024 600Ch
CONTROLSS_ECAP7	5024 700Ch
CONTROLSS_ECAP8	5024 800Ch
CONTROLSS_ECAP9	5024 900Ch

Figure 3-347. CONTROLSS_ECAP0_CAP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2															
RW															
0															

Access Types Legend

Table 3-725. CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP2	RW	0h	This register can be loaded (written) by: - Time-Stamp (counter value) during a capture event - Software - may be useful for test purposes - ACMP shadow register (CAP4) when used in APWM mode

3.7.5 CONTROLSS_ECAP0_CAP3 Register (Offset = 10h) [reset = h]

Short Description: Capture 3 Register

Long Description:

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Table 3-726. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0010h
CONTROLSS_ECAP1	5024 1010h
CONTROLSS_ECAP2	5024 2010h
CONTROLSS_ECAP3	5024 3010h
CONTROLSS_ECAP4	5024 4010h
CONTROLSS_ECAP5	5024 5010h
CONTROLSS_ECAP6	5024 6010h
CONTROLSS_ECAP7	5024 7010h
CONTROLSS_ECAP8	5024 8010h
CONTROLSS_ECAP9	5024 9010h

Figure 3-348. CONTROLSS_ECAP0_CAP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3															
RW															
0															

Access Types Legend

Table 3-727. CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP3	RW	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. You can update the PWM period value through this register. CAP3 (APRD) shadows CAP1 in this mode.

3.7.6 CONTROLSS_ECAP0_CAP4 Register (Offset = 14h) [reset = h]

Short Description: Capture 4 Register

Long Description:

Return to Summary Table

Table 3-728. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0014h
CONTROLSS_ECAP1	5024 1014h
CONTROLSS_ECAP2	5024 2014h
CONTROLSS_ECAP3	5024 3014h
CONTROLSS_ECAP4	5024 4014h
CONTROLSS_ECAP5	5024 5014h
CONTROLSS_ECAP6	5024 6014h
CONTROLSS_ECAP7	5024 7014h
CONTROLSS_ECAP8	5024 8014h
CONTROLSS_ECAP9	5024 9014h

Figure 3-349. CONTROLSS_ECAP0_CAP4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAP4															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4															
RW															
0															

Access Types Legend

Table 3-729. CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP4	RW	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. You can update the PWM compare value via this register. CAP4 (ACMP) shadows CAP2 in this mode.

3.7.7 CONTROLSS_ECAP0_ECCTL0 Register (Offset = 24h) [reset = h]

Short Description: Capture Control Register 0

Long Description:

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Table 3-730. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0024h
CONTROLSS_ECAP1	5024 1024h
CONTROLSS_ECAP2	5024 2024h
CONTROLSS_ECAP3	5024 3024h
CONTROLSS_ECAP4	5024 4024h
CONTROLSS_ECAP5	5024 5024h
CONTROLSS_ECAP6	5024 6024h
CONTROLSS_ECAP7	5024 7024h
CONTROLSS_ECAP8	5024 8024h
CONTROLSS_ECAP9	5024 9024h

Figure 3-350. CONTROLSS_ECAP0_ECCTL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														SOCEVTSEL	
RO RRETURNS0S														RW	
0														0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUALPRD				RESERVED				INPUTSEL							
RW				RO RRETURNS0S				RW							
0				0				11111111							

Access Types Legend

Table 3-731. ECCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED	RO RRETURNS 0S		Reserved
17 - 16	SOCEVTSEL	RW	0h	ADC SOC event select Capture Mode: 00b (R/W) = SOC trigger source is CEVT1 01b (R/W) = SOC trigger source is CEVT2 10b (R/W) = SOC trigger source is CEVT3 11b (R/W) = SOC trigger source is CEVT4 APWM Mode: 00b (R/W) = SOC trigger interrupt source is period match 01b (R/W) = SOC trigger interrupt source is compare match 10b (R/W) = SOC trigger interrupt source is period match or compare match 11b (R/W) = Disabled
15 - 12	QUALPRD	RW	0h	Qual period to filter out noise on input signals being monitored, Not applicable for HR mode. 0x0 : Bypass 0x1 : pulses of with 1 cycle or less will be filtered out 0x2 : pulses of with 2 cycles or less will be filtered out .... 0xF : pulses of with 15 cycles or less will be filtered out
11 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	INPUTSEL	RW	A98AC7h	Capture input source select bits 0x0 capture input is ECAPxINPUT[0] 0x1 capture input is ECAPxINPUT[1] 0x2 capture input is ECAPxINPUT[2] ... 0xFF capture input is ECAPxINPUT[256]

3.7.8 CONTROLSS_ECAP0_ECCTL1 Register (Offset = 28h) [reset = h]

Short Description: Capture Control Register 1

Long Description:

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Table 3-732. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0028h
CONTROLSS_ECAP1	5024 1028h
CONTROLSS_ECAP2	5024 2028h
CONTROLSS_ECAP3	5024 3028h
CONTROLSS_ECAP4	5024 4028h
CONTROLSS_ECAP5	5024 5028h
CONTROLSS_ECAP6	5024 6028h
CONTROLSS_ECAP7	5024 7028h
CONTROLSS_ECAP8	5024 8028h
CONTROLSS_ECAP9	5024 9028h

Figure 3-351. CONTROLSS_ECAP0_ECCTL1 Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PRESCALE					CAPLDEN
RW		RW					RW
0		0					0
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-733. ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREE_SOFT	RW	0h	Emulation Control 0x0 | ECAP_STOP_EMUTSCTR counter stops immediately on emulation suspend 0x1 | ECAP_RUNS_UNTILTSCTR counter runs until = 0 0x2 | ECAP_UNAF_EMU_SUSTSCTR counter is unaffected by emulation suspend (Run Free) 0x3 | ECAP_UNAF_EMU_SUS2TSCTR counter is unaffected by emulation suspend (Run Free)
13 - 9	PRESCALE	RW	0h	Event Filter prescale select 0x00 | ECAP_DIV1Divide by 1 (i.e,. no prescale, by-pass the prescaler) 0x01 | ECAP_DIV2Divide by 2 0x02 | ECAP_DIV4Divide by 4 0x03 | ECAP_DIV6Divide by 6 0x04 | ECAP_DIV8Divide by 8 0x05 | ECAP_DIV10Divide by 10 0x1E | ECAP_DIV60Divide by 60 0x1F | ECAP_DIV62Divide by 62
8	CAPLDEN	RW	0h	Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated. 0 | ECAP_DISABLEDisable CAP1-4 register loads at capture event time. 1 | ECAP_ENABLEEnable CAP1-4 register loads at capture event time.
7	CTRRST4	RW	0h	Counter Reset on Capture Event 4 0 | ECAP_DO_NOT_RESET_EVENT4Do not reset counter on Capture Event 4 (absolute time stamp operation) 1 | ECAP_RESET_EVENT4Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)

Table 3-733. ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CAP4POL	RW	0h	Capture Event 4 Polarity select 0 | ECAP_CAP_EVENT4_RISECapture Event 4 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT4_FALLCapture Event 4 triggered on a falling edge (FE)
5	CTRRST3	RW	0h	Counter Reset on Capture Event 3 0 | ECAP_DO_NOT_RESET_EVENT3Do not reset counter on Capture Event 3 (absolute time stamp) 1 | ECAP_RESET_EVENT3Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	RW	0h	Capture Event 3 Polarity select 0 | ECAP_CAP_EVENT3_RISECapture Event 3 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT3_FALLCapture Event 3 triggered on a falling edge (FE)
3	CTRRST2	RW	0h	Counter Reset on Capture Event 2 0 | ECAP_DO_NOT_RESET_EVENT2Do not reset counter on Capture Event 2 (absolute time stamp) 1 | ECAP_RESET_EVENT2Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	RW	0h	Capture Event 2 Polarity select 0 | ECAP_CAP_EVENT2_RISECapture Event 2 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT2_FALLCapture Event 2 triggered on a falling edge (FE)
1	CTRRST1	RW	0h	Counter Reset on Capture Event 1 0 | ECAP_DO_NOT_RESET_EVENT1Do not reset counter on Capture Event 1 (absolute time stamp) 1 | ECAP_RESET_EVENT1Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	RW	0h	Capture Event 1 Polarity select 0 | ECAP_CAP_EVENT1_RISECapture Event 1 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT1_FALLCapture Event 1 triggered on a falling edge (FE)

3.7.9 CONTROLSS_ECAP0_ECCTL2 Register (Offset = 2Ah) [reset = h]

Short Description: Capture Control Register 2

Long Description:

Return to Summary Table

Table 3-734. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Ah
CONTROLSS_ECAP1	5024 102Ah
CONTROLSS_ECAP2	5024 202Ah
CONTROLSS_ECAP3	5024 302Ah
CONTROLSS_ECAP4	5024 402Ah
CONTROLSS_ECAP5	5024 502Ah
CONTROLSS_ECAP6	5024 602Ah
CONTROLSS_ECAP7	5024 702Ah
CONTROLSS_ECAP8	5024 802Ah
CONTROLSS_ECAP9	5024 902Ah

Figure 3-352. CONTROLSS_ECAP0_ECCTL2 Name Register

15	14	13	12	11	10	9	8
MODCNTRSTS		DMAEVTSEL		CTRFILTRESET	APWMPOL	CAP_APWM	SWSYNC
RW		RW		RW RRETURNS0S	RW	RW	RW RRETURNS0S
0		0		0	0	0	0
7	6	5	4	3	2	1	0
SYNCO_SEL		SYNCI_EN	TSCTRSTOP	REARM	STOP_WRAP		CONT_ONESHT
RW		RW	RW	RW RRETURNS0S	RW		RW
0		0	0	0	11		0

Access Types Legend

Table 3-735. ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	MODCNTRSTS	RW	0h	This bit field reads current status on modulo counter 00b (R) = CAP1 register gets loaded on next capture event. 01b (R) = CAP2 register gets loaded on next capture event. 10b (R) = CAP3 register gets loaded on next capture event. 11b (R) = CAP4 register gets loaded on next capture event.
13 - 12	DMAEVTSEL	RW	0h	DMA event select Capture Mode: 00b (R/W) = DMA interrupt source is CEVT1 01b (R/W) = DMA interrupt source is CEVT2 10b (R/W) = DMA interrupt source is CEVT3 11b (R/W) = DMA interrupt source is CEVT4 APWM Mode: 00b (R/W) = DMA interrupt source is period match 01b (R/W) = DMA interrupt source is compare match 10b (R/W) = DMA interrupt source is period match or compare match 11b (R/W) = Disabled
11	CTRFILTRESET	RW RRETURNS0S	0h	Reset Bit 0h (R) = No effect 1h (W) = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured.

Table 3-735. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	APWMPOL	RW	0h	APWM output polarity select. This is applicable only in APWM operating mode. 0 | ECAP_OUTPUT_ACTIVE_HIGHOutput is active high (Compare value defines high time) 1 | ECAP_OUTPUT_ACTIVE_LOWOutput is active low (Compare value defines low time)
9	CAP_APWM	RW	0h	CAP/APWM operating mode select 0 | ECAP_MODULEECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input 1 | ECAP_MODULE_APWMECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output
8	SWSYNC	RW RRETURNS 0S	0h	Software-forced Counter (TSCTR) Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event. 0 | ECAP_ZERO_NOEFFECTWriting a zero has no effect. Reading always returns a zero 1 | ECAP_WRITE_TSCTRWriting a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful.
7 - 6	SYNCO_SEL	RW	0h	Sync-Out Select 0x0 | SWSYNCsync out signal is SWSYNC 0x1 | ECAP_CTR_PRD_TO_SYNCOUTSelect CTR = PRD event to be the sync-out signal 0x2 | ECAP_DISABLE_SYNC_OUTDisable sync out signal 0x3 | ECAP_DISABLE_SYNC_OUTDisable sync out signal
5	SYNCI_EN	RW	0h	Counter (TSCTR) Sync-In select mode 0 | ECAP_DISABLE_SYNC_INDisable sync-in option 1 | ECAP_ENABLE_COUNTER_REGISTEREnable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	RW	0h	Time Stamp (TSCTR) Counter Stop (freeze) Control 0 | ECAP_TSCTR_STOPPEDTSCTR stopped 1 | ECAP_TSCTR_FREE_RUNNINGTSCTR free-running
3	REARM	RW RRETURNS 0S	0h	Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode 0 | ECAP_NO_EFFECT_RETURNS_0Has no effect (reading always returns a 0) 1 | ECAP_ARMS_ONESHOTArms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads
2 - 1	STOP_WRAP	RW	Bh	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1-4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped (frozen) - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. 0x0 | ECAP_STOPEVENT1_WRAPEVENT2Stop after Capture Event 1 in one-shot mode Wrap after Capture Event 1 in continuous mode. 0x1 | ECAP_STOPEVENT2_WRAPEVENT2Stop after Capture Event 2 in one-shot mode Wrap after Capture Event 2 in continuous mode. 0x2 | ECAP_STOPEVENT3_WRAPEVENT2Stop after Capture Event 3 in one-shot mode Wrap after Capture Event 3 in continuous mode. 0x3 | ECAP_STOPEVENT4_WRAPEVENT2Stop after Capture Event 4 in one-shot mode Wrap after Capture Event 4 in continuous mode.

Table 3-735. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CONT_ONESHT	RW	0h	Continuous or one-shot mode control (applicable only in capture mode) 0 | ECAP_OPP_CONTOperate in continuous mode 1 | ECAP_OPP_ONEOperate in one-Shot mode

3.7.10 CONTROLSS_ECAP0_ECEINT Register (Offset = 2Ch) [reset = h]

Short Description: The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts

Long Description:

Return to Summary Table

Table 3-736. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Ch
CONTROLSS_ECAP1	5024 102Ch
CONTROLSS_ECAP2	5024 202Ch
CONTROLSS_ECAP3	5024 302Ch
CONTROLSS_ECAP4	5024 402Ch
CONTROLSS_ECAP5	5024 502Ch
CONTROLSS_ECAP6	5024 602Ch
CONTROLSS_ECAP7	5024 702Ch
CONTROLSS_ECAP8	5024 802Ch
CONTROLSS_ECAP9	5024 902Ch

Figure 3-353. CONTROLSS_ECAP0_ECEINT Name Register

15	14	13	12	11	10	9	8
RESERVED			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
RO			RW	RW	RW	RW	RW
0			0	0	0	0	0
7	6	5	4	3	2	1	0
CTR_EQ_CMP	CTR_EQ_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
RW	RW	RW	RW	RW	RW	RW	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-737. ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 2 interrupt 1 : Enable Monitoring unit 2 error event 2 interrupt
11	MUNIT_2_ERROR_EVT1	RW	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 1 interrupt 1 : Enable Monitoring unit 2 error event 1 interrupt
10	MUNIT_1_ERROR_EVT2	RW	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 2 interrupt 1 : Enable Monitoring unit 1 error event 2 interrupt
9	MUNIT_1_ERROR_EVT1	RW	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 1 interrupt 1 : Enable Monitoring unit 1 error event 1 interrupt

Table 3-737. ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HRERROR	RW	0h	High resolution error interrupt enable 0 | ECAP_DISAB_HRERROR_INTERRUPTDisable High Resolution Error as an Interrupt source 1 | ECAP_ENAB_HRERROR_INTERRUPTEnable High Resolution Error as an Interrupt source
7	CTR_EQ_CMP	RW	0h	Counter Equal Compare Interrupt Enable 0 | ECAP_DISAB_CE_INTERRUPTDisable Compare Equal as an Interrupt source 1 | ECAP_ENAB_CE_INTERRUPTEnable Compare Equal as an Interrupt source
6	CTR_EQ_PRD	RW	0h	Counter Equal Period Interrupt Enable 0 | ECAP_DISAB_PE_INTERRUPTDisable Period Equal as an Interrupt source 1 | ECAP_ENAB_PE_INTERRUPTEnable Period Equal as an Interrupt source
5	CTROVF	RW	0h	Counter Overflow Interrupt Enable 0 | ECAP_DISAB_CO_INTERRUPTDisabled counter Overflow as an Interrupt source 1 | ECAP_ENAB_CO_INTERRUPTEnable counter Overflow as an Interrupt source
4	CEVT4	RW	0h	Capture Event 4 Interrupt Enable 0 | ECAP_DISAB_CAP4_INTERRUPTDisable Capture Event 4 as an Interrupt source 1 | ECAP_ENAB_CAP4_INTERRUPTCapture Event 4 Interrupt Enable
3	CEVT3	RW	0h	Capture Event 3 Interrupt Enable 0 | ECAP_DISAB_CAP3_INTERRUPTDisable Capture Event 3 as an Interrupt source 1 | ECAP_ENAB_CAP3_INTERRUPTEnable Capture Event 3 as an Interrupt source
2	CEVT2	RW	0h	Capture Event 2 Interrupt Enable 0 | ECAP_DISAB_CAP2_INTERRUPTDisable Capture Event 2 as an Interrupt source 1 | ECAP_ENAB_CAP2_INTERRUPTEnable Capture Event 2 as an Interrupt source
1	CEVT1	RW	0h	Capture Event 1 Interrupt Enable 0 | ECAP_DISAB_CAP1_INTERRUPTDisable Capture Event 1 as an Interrupt source 1 | ECAP_ENAB_CAP1_INTERRUPTEnable Capture Event 1 as an Interrupt source
0	RESERVED	RO		Reserved

3.7.11 CONTROLSS_ECAP0_ECFLG Register (Offset = 2Eh) [reset = h]

Short Description: Capture Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-738. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Eh
CONTROLSS_ECAP1	5024 102Eh
CONTROLSS_ECAP2	5024 202Eh
CONTROLSS_ECAP3	5024 302Eh
CONTROLSS_ECAP4	5024 402Eh
CONTROLSS_ECAP5	5024 502Eh
CONTROLSS_ECAP6	5024 602Eh
CONTROLSS_ECAP7	5024 702Eh
CONTROLSS_ECAP8	5024 802Eh
CONTROLSS_ECAP9	5024 902Eh

Figure 3-354. CONTROLSS_ECAP0_ECFLG Name Register

15	14	13	12	11	10	9	8
RESERVED			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
RO			RO	RO	RO	RO	RO
0			0	0	0	0	0
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-739. ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RO	0h	Error event 2 Interrupt Flag from monitoring unit 2
11	MUNIT_2_ERROR_EVT1	RO	0h	Error event 2 Interrupt Flag from monitoring unit 2
10	MUNIT_1_ERROR_EVT2	RO	0h	Error event 2 Interrupt Flag from monitoring unit 1
9	MUNIT_1_ERROR_EVT1	RO	0h	Error event 2 Interrupt Flag from monitoring unit 1
8	HRERROR	RO	0h	High resolution error status flag Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_HIGH_RESOLUTION_ERRORIndicates the High resolution Error occurred
7	CTR_CMP	RO	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_COUNTER_COMPARE_REGIndicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR_PRD	RO	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_PERIOD_VALUE_RESETIndicates the counter (TSCTR) reached the period register value (APRD) and was reset.

Table 3-739. ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTROVF	RO	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_COUNTER_TRANSIndicates the counter (TSCTR) has made the transition from FFFFFFFF to 00000000
4	CEVT4	RO	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_4TH_EVENT_ECAPXIndicates the fourth event occurred at ECAPx pin
3	CEVT3	RO	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_3RD_EVENT_ECAPXIndicates the third event occurred at ECAPx pin.
2	CEVT2	RO	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_2ND_EVENT_ECAPXIndicates the second event occurred at ECAPx pin.
1	CEVT1	RO	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_1ST_EVENT_ECAPXIndicates the first event occurred at ECAPx pin.
0	INT	RO	0h	Global Interrupt Status Flag Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_INTERRUPTIndicates that an interrupt was generated.

3.7.12 CONTROLSS_ECAP0_ECCLR Register (Offset = 30h) [reset = h]

Short Description: Capture Interrupt Clear Register

Long Description:

Return to Summary Table

Table 3-740. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0030h
CONTROLSS_ECAP1	5024 1030h
CONTROLSS_ECAP2	5024 2030h
CONTROLSS_ECAP3	5024 3030h
CONTROLSS_ECAP4	5024 4030h
CONTROLSS_ECAP5	5024 5030h
CONTROLSS_ECAP6	5024 6030h
CONTROLSS_ECAP7	5024 7030h
CONTROLSS_ECAP8	5024 8030h
CONTROLSS_ECAP9	5024 9030h

Figure 3-355. CONTROLSS_ECAP0_ECCLR Name Register

15	14	13	12	11	10	9	8
RESERVED			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
RO			RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0			0	0	0	0	0
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-741. ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW RRETURNS0S	0h	Writing '1' clears MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	RW RRETURNS0S	0h	Writing '1' clears MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	RW RRETURNS0S	0h	Writing '1' clears MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	RW RRETURNS0S	0h	Writing '1' clears MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	RW RRETURNS0S	0h	High resolution error status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_HRERRORWriting a 1 clears the HRERROR flag.

Table 3-741. ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CTR_CMP	RW RRETURNS 0S	0h	Counter Equal Compare Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTR_CMPWriting a 1 clears the CTR=CMP flag.
6	CTR_PRD	RW RRETURNS 0S	0h	Counter Equal Period Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTR_PRDWriting a 1 clears the CTR=PRD flag.
5	CTROVF	RW RRETURNS 0S	0h	Counter Overflow Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTROVFWriting a 1 clears the CTROVF flag.
4	CEVT4	RW RRETURNS 0S	0h	Capture Event 4 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT4Writing a 1 clears the CEVT4 flag.
3	CEVT3	RW RRETURNS 0S	0h	Capture Event 3 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT3Writing a 1 clears the CEVT3 flag.
2	CEVT2	RW RRETURNS 0S	0h	Capture Event 2 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT2Writing a 1 clears the CEVT2 flag.
1	CEVT1	RW RRETURNS 0S	0h	Capture Event 1 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT1Writing a 1 clears the CEVT1 flag.
0	INT	RW RRETURNS 0S	0h	ECAP Global Interrupt Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_INTWriting a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1

3.7.13 CONTROLSS_ECAP0_ECFRC Register (Offset = 32h) [reset = h]

Short Description: Capture Interrupt Force Register

Long Description:

Return to Summary Table

Table 3-742. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0032h
CONTROLSS_ECAP1	5024 1032h
CONTROLSS_ECAP2	5024 2032h
CONTROLSS_ECAP3	5024 3032h
CONTROLSS_ECAP4	5024 4032h
CONTROLSS_ECAP5	5024 5032h
CONTROLSS_ECAP6	5024 6032h
CONTROLSS_ECAP7	5024 7032h
CONTROLSS_ECAP8	5024 8032h
CONTROLSS_ECAP9	5024 9032h

Figure 3-356. CONTROLSS_ECAP0_ECFRC Name Register

15	14	13	12	11	10	9	8
RESERVED			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
RO			RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0			0	0	0	0	0
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-743. ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW RRETURNS0S	0h	Writing '1' sets MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	RW RRETURNS0S	0h	Writing '1' sets MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	RW RRETURNS0S	0h	Writing '1' sets MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	RW RRETURNS0S	0h	Writing '1' sets MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	RW RRETURNS0S	0h	High resolution error Force interrupt 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTR_CMPWriting a 1 sets the CTR_CMP flag.
7	CTR_CMP	RW RRETURNS0S	0h	Force Counter Equal Compare Interrupt. This event is only active in APWM mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTR_CMPWriting a 1 sets the CTR_CMP flag.

Table 3-743. ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CTR_PRD	RW RRETURNS 0S	0h	Force Counter Equal Period Interrupt. This event is only active in APWM mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_CLEARS_CTR_PRDWriting a 1 sets the CTR_PRD flag.
5	CTROVF	RW RRETURNS 0S	0h	Force Counter Overflow 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTROVFWriting a 1 to this bit sets the CTROVF flag.
4	CEVT4	RW RRETURNS 0S	0h	Force Capture Event 4. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT4Writing a 1 sets the CEVT4 flag.
3	CEVT3	RW RRETURNS 0S	0h	Force Capture Event 3. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT3Writing a 1 sets the CEVT3 flag.
2	CEVT2	RW RRETURNS 0S	0h	Force Capture Event 2. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT2Writing a 1 sets the CEVT2 flag.
1	CEVT1	RW RRETURNS 0S	0h	Force Capture Event 1. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT1Sets the CEVT1 flag.
0	RESERVED	RO		Reserved

3.7.14 CONTROLSS_ECAP0_ECAPSYNCINSEL Register (Offset = 3Ch) [reset = h]

Short Description: SYNC source select register

Long Description:

Return to Summary Table

Table 3-744. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 003Ch
CONTROLSS_ECAP1	5024 103Ch
CONTROLSS_ECAP2	5024 203Ch
CONTROLSS_ECAP3	5024 303Ch
CONTROLSS_ECAP4	5024 403Ch
CONTROLSS_ECAP5	5024 503Ch
CONTROLSS_ECAP6	5024 603Ch
CONTROLSS_ECAP7	5024 703Ch
CONTROLSS_ECAP8	5024 803Ch
CONTROLSS_ECAP9	5024 903Ch

Figure 3-357. CONTROLSS_ECAP0_ECAPSYNCINSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									SEL						
RO									RW						
0									1						

Access Types Legend

Table 3-745. ECAPSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	RO		Reserved
6 - 0	SEL	RW	1h	These bits determines the source of SYNCIN signal. 0x0 : Disabled using SOC tieoff. 0x7F : Refer to SOC spec for details.

3.7.15 CONTROLSS_ECAP0_HRCTL Register (Offset = 40h) [reset = h]

Short Description: High-Res Control Register

Long Description:

Return to Summary Table

Table 3-746. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0040h
CONTROLSS_ECAP1	5024 1040h
CONTROLSS_ECAP2	5024 2040h
CONTROLSS_ECAP3	5024 3040h
CONTROLSS_ECAP4	5024 4040h
CONTROLSS_ECAP5	5024 5040h
CONTROLSS_ECAP6	5024 6040h
CONTROLSS_ECAP7	5024 7040h
CONTROLSS_ECAP8	5024 8040h
CONTROLSS_ECAP9	5024 9040h

Figure 3-358. CONTROLSS_ECAP0_HRCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CALIB CONT	CALIB STS	CALIB START	PRDS EL	HRCL KE	HRE
RW										RW	RO	RW RRET URNS 0S	RW	RW	RW
0										0	0	0	0	0	0

Access Types Legend

Table 3-747. HRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED	RW		Reserved
5	CALIBCONT	RW	0h	Continuous mode Calibration Select Bit: 0 Continuous mode disabled. 1 Continuous mode enabled. Calibration automatically restarts at end of current calibration cycle.
4	CALIBSTS	RO	0h	Calibration status Bit: 0 No active calibration cycle 1 Calibration cycle in progress
3	CALIBSTART	RW RRETURNS 0S	0h	Calibration start Bit: 0 No effect 1 Starts the calibration cycle
2	PRDSEL	RW	0h	Calibration Period Match Select Bit: 0 Use SYSCLK Counter For Period Match (default at reset) 1 Reserved
1	HRCLKE	RW	0h	High Resolution Clock Enable Bit: 0 High resolution clock disabled (default at reset) 1 High resolution clock enabled. The clock should be enabled before enabling the high res function via the HRE bit.

Table 3-747. HRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HRE	RW	0h	High Resolution Enable Bit: 0 High resolution mode disabled (default at reset) 1 High resolution mode enabled. Enabling this mode will connect the capture registers and edge event modes of the ECAP to be accessed by the High Res function. Note: The High Res clock needs to be enabled (using the HRCLKE bit) first before enabling the module. Allow a certain start up stabilization period before enabling the module.

3.7.16 CONTROLSS_ECAP0_HRINTEN Register (Offset = 48h) [reset = h]

Short Description: High-Res Calibration Interrupt Enable Register

Long Description:

Return to Summary Table

Table 3-748. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0048h
CONTROLSS_ECAP1	5024 1048h
CONTROLSS_ECAP2	5024 2048h
CONTROLSS_ECAP3	5024 3048h
CONTROLSS_ECAP4	5024 4048h
CONTROLSS_ECAP5	5024 5048h
CONTROLSS_ECAP6	5024 6048h
CONTROLSS_ECAP7	5024 7048h
CONTROLSS_ECAP8	5024 8048h
CONTROLSS_ECAP9	5024 9048h

Figure 3-359. CONTROLSS_ECAP0_HRINTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CALPRDCHKSTS	CALIBDONE	RESERVED
RO RRETURNS0S													RW	RW	RO RRETURNS0S
0													0	0	0

Access Types Legend

Table 3-749. HRINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS0S		Reserved
2	CALPRDCHKSTS	RW	0h	Calibration Period Check status Interrupt Enable: 0 Disable Calibration Period Check interrupt status 1 Enable Calibration Period Check interrupt status
1	CALIBDONE	RW	0h	Calibration done Interrupt Enable: 0 Disable Calibration done Interrupt 1 Enable Calibration done Interrupt
0	RESERVED	RO RRETURNS0S		Reserved

3.7.17 CONTROLSS_ECAP0_HRFLG Register (Offset = 4Ch) [reset = h]

Short Description: High-Res Calibration Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-750. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 004Ch
CONTROLSS_ECAP1	5024 104Ch
CONTROLSS_ECAP2	5024 204Ch
CONTROLSS_ECAP3	5024 304Ch
CONTROLSS_ECAP4	5024 404Ch
CONTROLSS_ECAP5	5024 504Ch
CONTROLSS_ECAP6	5024 604Ch
CONTROLSS_ECAP7	5024 704Ch
CONTROLSS_ECAP8	5024 804Ch
CONTROLSS_ECAP9	5024 904Ch

Figure 3-360. CONTROLSS_ECAP0_HRFLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CALPRDCHKSTS	CALIBDONE	CALIBINT
RO RRETURNS0S													RO	RO	RO
0													0	0	0

Access Types Legend

Table 3-751. HRFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS0S		Reserved
2	CALPRDCHKSTS	RO	0h	Calibration period check status Flag Bit: 1 Indicates that calibration ended before PRDCHK due to overflow on one of the counters. 0 Indicates no event occurred. Note: This bit remains latched until cleared by the user using the HRCLR [CALPRDCHKSTS] bit.
1	CALIBDONE	RO	0h	Calibration Done Interrupt Flag Bit: 1 Indicates calibration cycle is completed 0 Indicates calibration cycle has not completed. Note: This bit remains latched until cleared by the user using the HRCLR [CALIBDONE] bit.
0	CALIBINT	RO	0h	Global calibration Interrupt Status Flag: 1 Indicates that an interrupt was generated from CALIBDONE or CALPRDCHKSTS. 0 Indicates no interrupt generated.

3.7.18 CONTROLSS_ECAP0_HRCLR Register (Offset = 50h) [reset = h]

Short Description: High-Res Calibration Interrupt Clear Register

Long Description:

Return to Summary Table

Table 3-752. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0050h
CONTROLSS_ECAP1	5024 1050h
CONTROLSS_ECAP2	5024 2050h
CONTROLSS_ECAP3	5024 3050h
CONTROLSS_ECAP4	5024 4050h
CONTROLSS_ECAP5	5024 5050h
CONTROLSS_ECAP6	5024 6050h
CONTROLSS_ECAP7	5024 7050h
CONTROLSS_ECAP8	5024 8050h
CONTROLSS_ECAP9	5024 9050h

Figure 3-361. CONTROLSS_ECAP0_HRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CALPRDCHKSTS	CALIBDONE	CALIBINT
RO RRETURNS0S													RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0													0	0	0

Access Types Legend

Table 3-753. HRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS0S		Reserved
2	CALPRDCHKSTS	RW RRETURNS0S	0h	Clear Calibration period check status Flag Bit: 1 Clears the CALPRDCHKSTS flag register bit. 0 No effect. Note: H/W has priority over CPU writes if the user tries to clear a flag bit and an event occurs on the same cycle that tries to set the flag for the selected bit.
1	CALIBDONE	RW RRETURNS0S	0h	Clear Calibration Done Interrupt Flag Bit: 1 Clears the CALIBDONE interrupt flag register bit. 0 No effect. Note: H/W has priority over CPU writes if the user tries to clear a flag bit and an event occurs on the same cycle that tries to set the flag for the selected bit.
0	CALIBINT	RW RRETURNS0S	0h	Clear Global calibration Interrupt Flag 1 Clears the Global interrupt flag and enables further interrupts to be generated if any of the event flags are set. 0 No effect.

3.7.19 CONTROLSS_ECAP0_HRFRC Register (Offset = 54h) [reset = h]

Short Description: High-Res Calibration Interrupt Force Register

Long Description:

Return to Summary Table

Table 3-754. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0054h
CONTROLSS_ECAP1	5024 1054h
CONTROLSS_ECAP2	5024 2054h
CONTROLSS_ECAP3	5024 3054h
CONTROLSS_ECAP4	5024 4054h
CONTROLSS_ECAP5	5024 5054h
CONTROLSS_ECAP6	5024 6054h
CONTROLSS_ECAP7	5024 7054h
CONTROLSS_ECAP8	5024 8054h
CONTROLSS_ECAP9	5024 9054h

Figure 3-362. CONTROLSS_ECAP0_HRFRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CALPRDCHKSTS	CALIBDONE	RESERVED
RO RRETURNS0S													RW RRETURNS0S	RW RRETURNS0S	RO RRETURNS0S
0													0	0	0

Access Types Legend

Table 3-755. HRFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS0S		Reserved
2	CALPRDCHKSTS	RW RRETURNS0S	0h	Force CALPRDCHKSTS flag: 0 No effect 1 Sets the CALPRDCHKSTS flag.
1	CALIBDONE	RW RRETURNS0S	0h	Force CALIBDONE flag: 0 No effect 1 Sets the CALIBDONE flag.
0	RESERVED	RO RRETURNS0S		Reserved

3.7.20 CONTROLSS_ECAP0_HRCALPRD Register (Offset = 58h) [reset = h]

Short Description: High-Res Calibration Period Register

Long Description:

Return to Summary Table

Table 3-756. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0058h
CONTROLSS_ECAP1	5024 1058h
CONTROLSS_ECAP2	5024 2058h
CONTROLSS_ECAP3	5024 3058h
CONTROLSS_ECAP4	5024 4058h
CONTROLSS_ECAP5	5024 5058h
CONTROLSS_ECAP6	5024 6058h
CONTROLSS_ECAP7	5024 7058h
CONTROLSS_ECAP8	5024 8058h
CONTROLSS_ECAP9	5024 9058h

Figure 3-363. CONTROLSS_ECAP0_HRCALPRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRD															
RW															
11111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRD															
RW															
11111111111111111111															

Access Types Legend

Table 3-757. HRCALPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PRD	RW	3C3BC3A4A2F75C71C7h	Register to program calibration period. The period value is matched against HRSYSCLKCTR. On a match an interrupt is generated and the counter registers values are captured.

3.7.21 CONTROLSS_ECAP0_HRSYSCLKCTR Register (Offset = 5Ch) [reset = h]

Short Description: High-Res Calibration SYSCLK Counter Register

Long Description:

Return to Summary Table

Table 3-758. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 005Ch
CONTROLSS_ECAP1	5024 105Ch
CONTROLSS_ECAP2	5024 205Ch
CONTROLSS_ECAP3	5024 305Ch
CONTROLSS_ECAP4	5024 405Ch
CONTROLSS_ECAP5	5024 505Ch
CONTROLSS_ECAP6	5024 605Ch
CONTROLSS_ECAP7	5024 705Ch
CONTROLSS_ECAP8	5024 805Ch
CONTROLSS_ECAP9	5024 905Ch

Figure 3-364. CONTROLSS_ECAP0_HRSYSCLKCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRSYSCLKCTR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRSYSCLKCTR															
RO															
0															

Access Types Legend

Table 3-759. HRSYSCLKCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HRSYSCLKCTR	RO	0h	Current SYSCLK counter value

3.7.22 CONTROLSS_ECAP0_HRSYSCLKCAP Register (Offset = 60h) [reset = h]

Short Description: High-Res Calibration SYSCLK Capture Register

Long Description:

Return to Summary Table

Table 3-760. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0060h
CONTROLSS_ECAP1	5024 1060h
CONTROLSS_ECAP2	5024 2060h
CONTROLSS_ECAP3	5024 3060h
CONTROLSS_ECAP4	5024 4060h
CONTROLSS_ECAP5	5024 5060h
CONTROLSS_ECAP6	5024 6060h
CONTROLSS_ECAP7	5024 7060h
CONTROLSS_ECAP8	5024 8060h
CONTROLSS_ECAP9	5024 9060h

Figure 3-365. CONTROLSS_ECAP0_HRSYSCLKCAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRSYSCLKCAP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRSYSCLKCAP															
RO															
0															

Access Types Legend

Table 3-761. HRSYSCLKCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HRSYSCLKCAP	RO	0h	HRSYSCLKCTR is captures into this register at end of calibration cycle.

3.7.23 CONTROLSS_ECAP0_HRCLKCTR Register (Offset = 64h) [reset = h]

Short Description: High-Res Calibration HRCLK Counter Register

Long Description:

Return to Summary Table

Table 3-762. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0064h
CONTROLSS_ECAP1	5024 1064h
CONTROLSS_ECAP2	5024 2064h
CONTROLSS_ECAP3	5024 3064h
CONTROLSS_ECAP4	5024 4064h
CONTROLSS_ECAP5	5024 5064h
CONTROLSS_ECAP6	5024 6064h
CONTROLSS_ECAP7	5024 7064h
CONTROLSS_ECAP8	5024 8064h
CONTROLSS_ECAP9	5024 9064h

Figure 3-366. CONTROLSS_ECAP0_HRCLKCTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRCLKCTR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRCLKCTR															
RO															
0															

Access Types Legend

Table 3-763. HRCLKCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HRCLKCTR	RO	0h	Current HRCLK counter value Note: HRCLK is not synchronized to SYSCLK domain so reads may not be accurate

3.7.24 CONTROLSS_ECAP0_HRCLKCAP Register (Offset = 68h) [reset = h]

Short Description: High-Res Calibration HRCLK Capture Register

Long Description:

Return to Summary Table

Table 3-764. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0068h
CONTROLSS_ECAP1	5024 1068h
CONTROLSS_ECAP2	5024 2068h
CONTROLSS_ECAP3	5024 3068h
CONTROLSS_ECAP4	5024 4068h
CONTROLSS_ECAP5	5024 5068h
CONTROLSS_ECAP6	5024 6068h
CONTROLSS_ECAP7	5024 7068h
CONTROLSS_ECAP8	5024 8068h
CONTROLSS_ECAP9	5024 9068h

Figure 3-367. CONTROLSS_ECAP0_HRCLKCAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRCLKCAP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HRCLKCAP															
RO															
0															

Access Types Legend

Table 3-765. HRCLKCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HRCLKCAP	RO	0h	HRCLKCTR is captures into this register at end of calibration cycle. Note: HRCLK is not synchronized to SYSCLK domain so reads may not be accurate

3.7.25 CONTROLSS_ECAP0_HRDEBUGCTL Register (Offset = 74h) [reset = h]

Short Description: High-Res Debug control register

Long Description:

Return to Summary Table

Table 3-766. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0074h
CONTROLSS_ECAP1	5024 1074h
CONTROLSS_ECAP2	5024 2074h
CONTROLSS_ECAP3	5024 3074h
CONTROLSS_ECAP4	5024 4074h
CONTROLSS_ECAP5	5024 5074h
CONTROLSS_ECAP6	5024 6074h
CONTROLSS_ECAP7	5024 7074h
CONTROLSS_ECAP8	5024 8074h
CONTROLSS_ECAP9	5024 9074h

Figure 3-368. CONTROLSS_ECAP0_HRDEBUGCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				OBSERVE_SRC_SEL				RESERVED		CALIB_INPUT_SEL		RESERVED	CAPIN_MMAP_SOURCE	DELAYRESETDLINE	DISABLEINVSEL
RO RRETURNS0S				RW				RO RRETURNS0S		RW		RO RRETURNS0S	RW	RW	RW
0				0				0		0		0	0	0	0

Access Types Legend

Table 3-767. HRDEBUGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED	RO RRETURNS0S		Reserved
11 - 8	OBSERVE_SRC_SEL	RW	0h	Select bits for selecting source for OBSERVE1 and OBSERVE2 registers 1000 HROUTH and HROUTL will read HR1OUT 1001 HROUTH and HROUTL will read HR2OUT 1010 HROUTH and HROUTL will read Capture Delayline 1 OBS1 1011 HROUTH and HROUTL will read Capture Delayline 2 OBS1 1100 HROUTH and HROUTL will read Capture Delayline 1 OBS2 1101 HROUTH and HROUTL will read Capture Delayline 2 OBS2
7 - 6	RESERVED	RO RRETURNS0S		Reserved

Table 3-767. HRDEBUGCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 4	CALIB_INPUT_SEL	RW	0h	Select bit for calibration input, can be used to get fault coverage using these inputs 00 CAPIN is one of 128 inputs selected by INPUTSEL 01 CAPIN is connected to CAPIN_MEMMAP_SOURCE 10 CAPIN is internally generated signal waveform with 8*HRCLK cycle high and 8*HRCLK cycle low, used for linearity check of capture delay line 1 11 CAPIN is internally generated signal waveform with 8*HRCLK cycle high and 8*HRCLK cycle low, delayed by half HRCLK, used for linearity check of capture delay line 2
3	RESERVED	RO RRETURNS 0S		Reserved
2	CAPIN_MMAP_SOURCE	RW	0h	Memory mapped CAPIN source Note : select CALIN source first, it may happen that you may see interrupt if MMAP source is different from current value of CAPIN. This is debug feature hence no additional HW is necessary to prevent this.
1	DELAYRESETDLINE	RW	0h	Controls the reset delayline timing 0 reset is forced on next falling edge of HRCLK (1/2 cycle after capture) 1 reset is applied a cycle later (1 1/2 cycles after capture)
0	DISABLEINVSEL	RW	0h	Disable INVSEL Logic: 0 State machine controls inversion on input signal 1 CAPIN signal propagated into delay line without inversion, this means only rising edges can be measured

3.7.26 CONTROLSS_ECAP0_HRDEBUGOBSERVE1 Register (Offset = 78h) [reset = h]

Short Description: High-Res Raw output & internal nodes of HRCLK capture delay line

Long Description:

Return to Summary Table

Table 3-768. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0078h
CONTROLSS_ECAP1	5024 1078h
CONTROLSS_ECAP2	5024 2078h
CONTROLSS_ECAP3	5024 3078h
CONTROLSS_ECAP4	5024 4078h
CONTROLSS_ECAP5	5024 5078h
CONTROLSS_ECAP6	5024 6078h
CONTROLSS_ECAP7	5024 7078h
CONTROLSS_ECAP8	5024 8078h
CONTROLSS_ECAP9	5024 9078h

Figure 3-369. CONTROLSS_ECAP0_HRDEBUGOBSERVE1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HROUTH															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HROUTH															
RO															
0															

Access Types Legend

Table 3-769. HRDEBUGOBSERVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HROUTH	RO	0h	Reads raw output of HROUT capture delay line 1

3.7.27 CONTROLSS_ECAP0_HRDEBUGOBSERVE2 Register (Offset = 7Ch) [reset = h]

Short Description: High-Res Raw output & internal nodes of HRCLK capture delay line

Long Description:

Return to Summary Table

Table 3-770. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 007Ch
CONTROLSS_ECAP1	5024 107Ch
CONTROLSS_ECAP2	5024 207Ch
CONTROLSS_ECAP3	5024 307Ch
CONTROLSS_ECAP4	5024 407Ch
CONTROLSS_ECAP5	5024 507Ch
CONTROLSS_ECAP6	5024 607Ch
CONTROLSS_ECAP7	5024 707Ch
CONTROLSS_ECAP8	5024 807Ch
CONTROLSS_ECAP9	5024 907Ch

Figure 3-370. CONTROLSS_ECAP0_HRDEBUGOBSERVE2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HROUTL															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HROUTL															
RO															
0															

Access Types Legend

Table 3-771. HRDEBUGOBSERVE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HROUTL	RO	0h	Reads raw output of HROUT capture delay line 2

3.7.28 CONTROLSS_ECAP0_MUNIT_COMMON_CTL Register (Offset = 80h) [reset = h]

Short Description: Control registers for monitoring unit {#}

Long Description:

Return to Summary Table

Table 3-772. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0080h
CONTROLSS_ECAP1	5024 1080h
CONTROLSS_ECAP2	5024 2080h
CONTROLSS_ECAP3	5024 3080h
CONTROLSS_ECAP4	5024 4080h
CONTROLSS_ECAP5	5024 5080h
CONTROLSS_ECAP6	5024 6080h
CONTROLSS_ECAP7	5024 7080h
CONTROLSS_ECAP8	5024 8080h
CONTROLSS_ECAP9	5024 9080h

Figure 3-371. CONTROLSS_ECAP0_MUNIT_COMMON_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	GLDSTRBSEL							RESERVED	TRIPSEL						
RO RRETURNS0S	RW							RO RRETURNS0S	RW						
0	0							0	0						

Access Types Legend

Table 3-773. MUNIT_COMMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS0S		Reserved
15	RESERVED	RO RRETURNS0S		Reserved
14 - 8	GLDSTRBSEL	RW	0h	Global load strobe select to enable shadow to active loading 0x0 : Disabled with SOC level tieoff. 0x1 to 0x7F : Global load strobe from SOC level including ETPWM global load strobes.
7	RESERVED	RO RRETURNS0S		Reserved
6 - 0	TRIPSEL	RW	0h	Trip signal select to disable and enable signal monitoring automatically 0x0 : Disabled, Trip signals does not affect signal monitoring, achieved with SOC level tieoff. 0x1 to 0x7F : Signal monioring is disabled when selected signal is high and enabled when it is low

3.7.29 CONTROLSS_ECAP0_MUNIT_1_CTL Register (Offset = C0h) [reset = h]

Short Description: Control registers for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-774. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00C0h
CONTROLSS_ECAP1	5024 10C0h
CONTROLSS_ECAP2	5024 20C0h
CONTROLSS_ECAP3	5024 30C0h
CONTROLSS_ECAP4	5024 40C0h
CONTROLSS_ECAP5	5024 50C0h
CONTROLSS_ECAP6	5024 60C0h
CONTROLSS_ECAP7	5024 70C0h
CONTROLSS_ECAP8	5024 80C0h
CONTROLSS_ECAP9	5024 90C0h

Figure 3-372. CONTROLSS_ECAP0_MUNIT_1_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MON_SEL				RESERVED						DEBUG_RANGE_EN	EN
RO RRETURNS0S				RW				RO RRETURNS0S						RW	RW
0				0				0						0	0

Access Types Legend

Table 3-775. MUNIT_1_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS 0S		Reserved
15 - 12	RESERVED	RO RRETURNS 0S		Reserved
11 - 8	MON_SEL	RW	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved (High Pulse width)
7 - 2	RESERVED	RO RRETURNS 0S		Reserved
1	DEBUG_RANGE_EN	RW	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 1 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers.

Table 3-775. MUNIT_1_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN	RW	0h	0 : Monitoring unit 1 is disabled 1 : Monitoring unit 1 is enabled

3.7.30 CONTROLSS_ECAP0_MUNIT_1_SHADOW_CTL Register (Offset = C4h) [reset = h]

Short Description: Shadow control registers for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-776. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00C4h
CONTROLSS_ECAP1	5024 10C4h
CONTROLSS_ECAP2	5024 20C4h
CONTROLSS_ECAP3	5024 30C4h
CONTROLSS_ECAP4	5024 40C4h
CONTROLSS_ECAP5	5024 50C4h
CONTROLSS_ECAP6	5024 60C4h
CONTROLSS_ECAP7	5024 70C4h
CONTROLSS_ECAP8	5024 80C4h
CONTROLSS_ECAP9	5024 90C4h

Figure 3-373. CONTROLSS_ECAP0_MUNIT_1_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													LOAD MODE	SWSYNC	SYNCI_EN
RO RRETURNS0S													RW	RW RRETURNS 0S	RW
0													0	0	0

Access Types Legend

Table 3-777. MUNIT_1_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2	LOADMODE	RW	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event
1	SWSYNC	RW RRETURNS 0S	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_1_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	RW	0h	Shadow Enable 0 : Disabled 1 : Enabled

3.7.31 CONTROLSS_ECAP0_MUNIT_1_MIN Register (Offset = D0h) [reset = h]

Short Description: Min value for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-778. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D0h
CONTROLSS_ECAP1	5024 10D0h
CONTROLSS_ECAP2	5024 20D0h
CONTROLSS_ECAP3	5024 30D0h
CONTROLSS_ECAP4	5024 40D0h
CONTROLSS_ECAP5	5024 50D0h
CONTROLSS_ECAP6	5024 60D0h
CONTROLSS_ECAP7	5024 70D0h
CONTROLSS_ECAP8	5024 80D0h
CONTROLSS_ECAP9	5024 90D0h

Figure 3-374. CONTROLSS_ECAP0_MUNIT_1_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
RW															
0															

Access Types Legend

Table 3-779. MUNIT_1_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RW	0h	Minimum value for monitoring

3.7.32 CONTROLSS_ECAP0_MUNIT_1_MAX Register (Offset = D4h) [reset = h]

Short Description: Max value for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-780. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D4h
CONTROLSS_ECAP1	5024 10D4h
CONTROLSS_ECAP2	5024 20D4h
CONTROLSS_ECAP3	5024 30D4h
CONTROLSS_ECAP4	5024 40D4h
CONTROLSS_ECAP5	5024 50D4h
CONTROLSS_ECAP6	5024 60D4h
CONTROLSS_ECAP7	5024 70D4h
CONTROLSS_ECAP8	5024 80D4h
CONTROLSS_ECAP9	5024 90D4h

Figure 3-375. CONTROLSS_ECAP0_MUNIT_1_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
RW															
0															

Access Types Legend

Table 3-781. MUNIT_1_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RW	0h	Maximum value for monitoring

3.7.33 CONTROLSS_ECAP0_MUNIT_1_MIN_SHADOW Register (Offset = D8h) [reset = h]

Short Description: Shadow register for Min value of monitoring unit 1

Long Description:

Return to Summary Table

Table 3-782. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D8h
CONTROLSS_ECAP1	5024 10D8h
CONTROLSS_ECAP2	5024 20D8h
CONTROLSS_ECAP3	5024 30D8h
CONTROLSS_ECAP4	5024 40D8h
CONTROLSS_ECAP5	5024 50D8h
CONTROLSS_ECAP6	5024 60D8h
CONTROLSS_ECAP7	5024 70D8h
CONTROLSS_ECAP8	5024 80D8h
CONTROLSS_ECAP9	5024 90D8h

Figure 3-376. CONTROLSS_ECAP0_MUNIT_1_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW															
RW															
0															

Access Types Legend

Table 3-783. MUNIT_1_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE_SHADOW	RW	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

3.7.34 CONTROLSS_ECAP0_MUNIT_1_MAX_SHADOW Register (Offset = DCh) [reset = h]

Short Description: Shadow register for Max value of monitoring unit 1

Long Description:

Return to Summary Table

Table 3-784. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00DCh
CONTROLSS_ECAP1	5024 10DCh
CONTROLSS_ECAP2	5024 20DCh
CONTROLSS_ECAP3	5024 30DCh
CONTROLSS_ECAP4	5024 40DCh
CONTROLSS_ECAP5	5024 50DCh
CONTROLSS_ECAP6	5024 60DCh
CONTROLSS_ECAP7	5024 70DCh
CONTROLSS_ECAP8	5024 80DCh
CONTROLSS_ECAP9	5024 90DCh

Figure 3-377. CONTROLSS_ECAP0_MUNIT_1_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE_SHADOW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE_SHADOW															
RW															
0															

Access Types Legend

Table 3-785. MUNIT_1_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE_SHADOW	RW	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

3.7.35 CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MIN Register (Offset = E0h) [reset = h]

Short Description: Observed Min value of check being enabled on minotoring unit 1

Long Description:

Return to Summary Table

Table 3-786. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00E0h
CONTROLSS_ECAP1	5024 10E0h
CONTROLSS_ECAP2	5024 20E0h
CONTROLSS_ECAP3	5024 30E0h
CONTROLSS_ECAP4	5024 40E0h
CONTROLSS_ECAP5	5024 50E0h
CONTROLSS_ECAP6	5024 60E0h
CONTROLSS_ECAP7	5024 70E0h
CONTROLSS_ECAP8	5024 80E0h
CONTROLSS_ECAP9	5024 90E0h

Figure 3-378. CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
RO															
11111111111111111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
RO															
11111111111111111111111111111111															

Access Types Legend

Table 3-787. MUNIT_1_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RO	8C3DEFB1EDB984FE2AC71C71C7h	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

3.7.36 CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MAX Register (Offset = E4h) [reset = h]

Short Description: Observed Max value of check being enabled on minotoring unit 1

Long Description:

Return to Summary Table

Table 3-788. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00E4h
CONTROLSS_ECAP1	5024 10E4h
CONTROLSS_ECAP2	5024 20E4h
CONTROLSS_ECAP3	5024 30E4h
CONTROLSS_ECAP4	5024 40E4h
CONTROLSS_ECAP5	5024 50E4h
CONTROLSS_ECAP6	5024 60E4h
CONTROLSS_ECAP7	5024 70E4h
CONTROLSS_ECAP8	5024 80E4h
CONTROLSS_ECAP9	5024 90E4h

Figure 3-379. CONTROLSS_ECAP0_MUNIT_1_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
RO															
0															

Access Types Legend

Table 3-789. MUNIT_1_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RO	0h	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

3.7.37 CONTROLSS_ECAP0_MUNIT_2_CTL Register (Offset = 100h) [reset = h]

Short Description: Control registers for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-790. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0100h
CONTROLSS_ECAP1	5024 1100h
CONTROLSS_ECAP2	5024 2100h
CONTROLSS_ECAP3	5024 3100h
CONTROLSS_ECAP4	5024 4100h
CONTROLSS_ECAP5	5024 5100h
CONTROLSS_ECAP6	5024 6100h
CONTROLSS_ECAP7	5024 7100h
CONTROLSS_ECAP8	5024 8100h
CONTROLSS_ECAP9	5024 9100h

Figure 3-380. CONTROLSS_ECAP0_MUNIT_2_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MON_SEL				RESERVED						DEBUG_RANGE_EN	EN
RO RRETURNS0S				RW				RO RRETURNS0S						RW	RW
0				0				0						0	0

Access Types Legend

Table 3-791. MUNIT_2_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS0S		Reserved
15 - 12	RESERVED	RO RRETURNS0S		Reserved
11 - 8	MON_SEL	RW	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved (High Pulse width)
7 - 2	RESERVED	RO RRETURNS0S		Reserved
1	DEBUG_RANGE_EN	RW	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 2 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers.

Table 3-791. MUNIT_2_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN	RW	0h	0 : Monitoring unit 2 is disabled 1 : Monitoring unit 2 is enabled

3.7.38 CONTROLSS_ECAP0_MUNIT_2_SHADOW_CTL Register (Offset = 104h) [reset = h]

Short Description: Shadow control registers for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-792. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0104h
CONTROLSS_ECAP1	5024 1104h
CONTROLSS_ECAP2	5024 2104h
CONTROLSS_ECAP3	5024 3104h
CONTROLSS_ECAP4	5024 4104h
CONTROLSS_ECAP5	5024 5104h
CONTROLSS_ECAP6	5024 6104h
CONTROLSS_ECAP7	5024 7104h
CONTROLSS_ECAP8	5024 8104h
CONTROLSS_ECAP9	5024 9104h

Figure 3-381. CONTROLSS_ECAP0_MUNIT_2_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													LOAD MODE	SWSYNC	SYNCI_EN
RO RRETURNS0S													RW	RW RRETURNS 0S	RW
0													0	0	0

Access Types Legend

Table 3-793. MUNIT_2_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2	LOADMODE	RW	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event
1	SWSYNC	RW RRETURNS 0S	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_2_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	RW	0h	Shadow Enable 0 : Disabled 1 : Enabled

3.7.39 CONTROLSS_ECAP0_MUNIT_2_MIN Register (Offset = 110h) [reset = h]

Short Description: Min value for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-794. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0110h
CONTROLSS_ECAP1	5024 1110h
CONTROLSS_ECAP2	5024 2110h
CONTROLSS_ECAP3	5024 3110h
CONTROLSS_ECAP4	5024 4110h
CONTROLSS_ECAP5	5024 5110h
CONTROLSS_ECAP6	5024 6110h
CONTROLSS_ECAP7	5024 7110h
CONTROLSS_ECAP8	5024 8110h
CONTROLSS_ECAP9	5024 9110h

Figure 3-382. CONTROLSS_ECAP0_MUNIT_2_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
RW															
0															

Access Types Legend

Table 3-795. MUNIT_2_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RW	0h	Minimum value for monitoring

3.7.40 CONTROLSS_ECAP0_MUNIT_2_MAX Register (Offset = 114h) [reset = h]

Short Description: Max value for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-796. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0114h
CONTROLSS_ECAP1	5024 1114h
CONTROLSS_ECAP2	5024 2114h
CONTROLSS_ECAP3	5024 3114h
CONTROLSS_ECAP4	5024 4114h
CONTROLSS_ECAP5	5024 5114h
CONTROLSS_ECAP6	5024 6114h
CONTROLSS_ECAP7	5024 7114h
CONTROLSS_ECAP8	5024 8114h
CONTROLSS_ECAP9	5024 9114h

Figure 3-383. CONTROLSS_ECAP0_MUNIT_2_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
RW															
0															

Access Types Legend

Table 3-797. MUNIT_2_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RW	0h	Maximum value for monitoring

3.7.41 CONTROLSS_ECAP0_MUNIT_2_MIN_SHADOW Register (Offset = 118h) [reset = h]

Short Description: Shadow register for Min value of monitoring unit 2

Long Description:

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Table 3-798. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0118h
CONTROLSS_ECAP1	5024 1118h
CONTROLSS_ECAP2	5024 2118h
CONTROLSS_ECAP3	5024 3118h
CONTROLSS_ECAP4	5024 4118h
CONTROLSS_ECAP5	5024 5118h
CONTROLSS_ECAP6	5024 6118h
CONTROLSS_ECAP7	5024 7118h
CONTROLSS_ECAP8	5024 8118h
CONTROLSS_ECAP9	5024 9118h

Figure 3-384. CONTROLSS_ECAP0_MUNIT_2_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW															
RW															
0															

Access Types Legend

Table 3-799. MUNIT_2_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE_SHADOW	RW	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

3.7.42 CONTROLSS_ECAP0_MUNIT_2_MAX_SHADOW Register (Offset = 11Ch) [reset = h]

Short Description: Shadow register for Max value of monitoring unit 2

Long Description:

Return to Summary Table

Table 3-800. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 011Ch
CONTROLSS_ECAP1	5024 111Ch
CONTROLSS_ECAP2	5024 211Ch
CONTROLSS_ECAP3	5024 311Ch
CONTROLSS_ECAP4	5024 411Ch
CONTROLSS_ECAP5	5024 511Ch
CONTROLSS_ECAP6	5024 611Ch
CONTROLSS_ECAP7	5024 711Ch
CONTROLSS_ECAP8	5024 811Ch
CONTROLSS_ECAP9	5024 911Ch

Figure 3-385. CONTROLSS_ECAP0_MUNIT_2_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE_SHADOW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE_SHADOW															
RW															
0															

Access Types Legend

Table 3-801. MUNIT_2_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE_SHADOW	RW	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

3.7.43 CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MIN Register (Offset = 120h) [reset = h]

Short Description: Observed Min value of check being enabled on minotoring unit 2

Long Description:

Return to Summary Table

Table 3-802. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0120h
CONTROLSS_ECAP1	5024 1120h
CONTROLSS_ECAP2	5024 2120h
CONTROLSS_ECAP3	5024 3120h
CONTROLSS_ECAP4	5024 4120h
CONTROLSS_ECAP5	5024 5120h
CONTROLSS_ECAP6	5024 6120h
CONTROLSS_ECAP7	5024 7120h
CONTROLSS_ECAP8	5024 8120h
CONTROLSS_ECAP9	5024 9120h

Figure 3-386. CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIN_VALUE															
RO															
11111111111111111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIN_VALUE															
RO															
11111111111111111111111111111111															

Access Types Legend

Table 3-803. MUNIT_2_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RO	8C3DEFB1EDB984FE2AC71C71C7h	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

3.7.44 CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MAX Register (Offset = 124h) [reset = h]

Short Description: Observed Max value of check being enabled on minotoring unit 2

Long Description:

Return to Summary Table

Table 3-804. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0124h
CONTROLSS_ECAP1	5024 1124h
CONTROLSS_ECAP2	5024 2124h
CONTROLSS_ECAP3	5024 3124h
CONTROLSS_ECAP4	5024 4124h
CONTROLSS_ECAP5	5024 5124h
CONTROLSS_ECAP6	5024 6124h
CONTROLSS_ECAP7	5024 7124h
CONTROLSS_ECAP8	5024 8124h
CONTROLSS_ECAP9	5024 9124h

Figure 3-387. CONTROLSS_ECAP0_MUNIT_2_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_VALUE															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX_VALUE															
RO															
0															

Access Types Legend

Table 3-805. MUNIT_2_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RO	0h	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

Table 3-806. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO RRETURNS0S	RO RRETURNS0S	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RO	RO	Undefined

3.8 C2K_EQEP Registers

Table 3-807. CONTROLSS_EQEP0, CONTROLSS_EQEP0_CONTROLSS_EQEP Registers, Base Address=5027 0000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_EQEP 0 Physical Address	CONTROLSS_EQEP 1 Physical Address	CONTROLSS_EQEP 2 Physical Address
0h	32	CONTROLSS_EQEP0_QPOSCNT	Position Counter	5027 0000h	5027 1000h	5027 2000h
4h	32	CONTROLSS_EQEP0_QPOSINIT	Position Counter Init	5027 0004h	5027 1004h	5027 2004h
8h	32	CONTROLSS_EQEP0_QPOSMAX	Maximum Position Count	5027 0008h	5027 1008h	5027 2008h
Ch	32	CONTROLSS_EQEP0_QPOSCMP	Position Compare	5027 000Ch	5027 100Ch	5027 200Ch
10h	32	CONTROLSS_EQEP0_QPOSILAT	Index Position Latch	5027 0010h	5027 1010h	5027 2010h
14h	32	CONTROLSS_EQEP0_QPOSSLAT	Strobe Position Latch	5027 0014h	5027 1014h	5027 2014h
18h	32	CONTROLSS_EQEP0_QPOSLAT	Position Latch	5027 0018h	5027 1018h	5027 2018h
1Ch	32	CONTROLSS_EQEP0_QUTMR	QEP Unit Timer	5027 001Ch	5027 101Ch	5027 201Ch
20h	32	CONTROLSS_EQEP0_QUPRD	QEP Unit Period	5027 0020h	5027 1020h	5027 2020h
24h	16	CONTROLSS_EQEP0_QWDTMR	QEP Watchdog Timer	5027 0024h	5027 1024h	5027 2024h
26h	16	CONTROLSS_EQEP0_QWDPRD	QEP Watchdog Period	5027 0026h	5027 1026h	5027 2026h
28h	16	CONTROLSS_EQEP0_QDECCTL	Quadrature Decoder Control	5027 0028h	5027 1028h	5027 2028h
2Ah	16	CONTROLSS_EQEP0_QEPCTL	QEP Control	5027 002Ah	5027 102Ah	5027 202Ah
2Ch	16	CONTROLSS_EQEP0_QCAPCTL	Qaudrature Capture Control	5027 002Ch	5027 102Ch	5027 202Ch
2Eh	16	CONTROLSS_EQEP0_QPOSCTL	Position Compare Control	5027 002Eh	5027 102Eh	5027 202Eh
30h	16	CONTROLSS_EQEP0_QEINT	QEP Interrupt Control	5027 0030h	5027 1030h	5027 2030h
32h	16	CONTROLSS_EQEP0_QFLG	QEP Interrupt Flag	5027 0032h	5027 1032h	5027 2032h
34h	16	CONTROLSS_EQEP0_QCLR	QEP Interrupt Clear	5027 0034h	5027 1034h	5027 2034h
36h	16	CONTROLSS_EQEP0_QFRC	QEP Interrupt Force	5027 0036h	5027 1036h	5027 2036h
38h	16	CONTROLSS_EQEP0_QEPSTS	QEP Status	5027 0038h	5027 1038h	5027 2038h

Table 3-807. CONTROLSS_EQEP0, CONTROLSS_EQEP0_CONTROLSS_EQEP Registers, Base Address=5027 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_EQEP0 Physical Address	CONTROLSS_EQEP1 Physical Address	CONTROLSS_EQEP2 Physical Address
3Ah	16	CONTROLSS_EQEP0_QCTMR	QEP Capture Timer	5027 003Ah	5027 103Ah	5027 203Ah
3Ch	16	CONTROLSS_EQEP0_QCPRD	QEP Capture Period	5027 003Ch	5027 103Ch	5027 203Ch
3Eh	16	CONTROLSS_EQEP0_QCTMRLAT	QEP Capture Latch	5027 003Eh	5027 103Eh	5027 203Eh
40h	16	CONTROLSS_EQEP0_QCPRDLAT	QEP Capture Period Latch	5027 0040h	5027 1040h	5027 2040h
60h	32	CONTROLSS_EQEP0_REV	QEP Revision Number	5027 0060h	5027 1060h	5027 2060h
64h	32	CONTROLSS_EQEP0_QEPSTROBESEL	QEP Strobe select register	5027 0064h	5027 1064h	5027 2064h
68h	32	CONTROLSS_EQEP0_QMACTRL	QMA Control register	5027 0068h	5027 1068h	5027 2068h
6Ch	32	CONTROLSS_EQEP0_QEPSRCSEL	QEP Source Select Register	5027 006Ch	5027 106Ch	5027 206Ch

3.8.1 CONTROLSS_EQEP0_QPOSCNT Register (Offset = 0h) [reset = h]

Short Description: Position Counter

Long Description:

Return to Summary Table

Table 3-808. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0000h
CONTROLSS_EQEP1	5027 1000h
CONTROLSS_EQEP2	5027 2000h

Figure 3-388. CONTROLSS_EQEP0_QPOSCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCNT															
RW															
0															

Access Types Legend

Table 3-809. QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSCNT	RW	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Note: It is recommended to only write to the position counter register (QPOSCNT) during initialization, i.e. when the eQEP position counter is disabled (QPEN bit of QEPCTL is zero). Once the position counter is enabled (QPEN bit is one), writing to the eQEP position counter register (QPOSCNT) may cause unexpected results.

3.8.2 CONTROLSS_EQEP0_QPOSINIT Register (Offset = 4h) [reset = h]

Short Description: Position Counter Init

Long Description:

Return to Summary Table

Table 3-810. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0004h
CONTROLSS_EQEP1	5027 1004h
CONTROLSS_EQEP2	5027 2004h

Figure 3-389. CONTROLSS_EQEP0_QPOSINIT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSINIT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSINIT															
RW															
0															

Access Types Legend

Table 3-811. QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSINIT	RW	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes.

3.8.3 CONTROLSS_EQEP0_QPOSMAX Register (Offset = 8h) [reset = h]

Short Description: Maximum Position Count

Long Description:

Return to Summary Table

Table 3-812. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0008h
CONTROLSS_EQEP1	5027 1008h
CONTROLSS_EQEP2	5027 2008h

Figure 3-390. CONTROLSS_EQEP0_QPOSMAX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSMAX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSMAX															
RW															
0															

Access Types Legend

Table 3-813. QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSMAX	RW	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes.

3.8.4 CONTROLSS_EQEP0_QPOSCMP Register (Offset = Ch) [reset = h]

Short Description: Position Compare

Long Description:

Return to Summary Table

Table 3-814. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 000Ch
CONTROLSS_EQEP1	5027 100Ch
CONTROLSS_EQEP2	5027 200Ch

Figure 3-391. CONTROLSS_EQEP0_QPOSCMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSCMP															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCMP															
RW															
0															

Access Types Legend

Table 3-815. QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSCMP	RW	0h	Position Compare The position-compare value in this register is compared with the position counter (QPOSCNT) to generate sync output and/or interrupt on compare match.

3.8.5 CONTROLSS_EQEP0_QPOSILAT Register (Offset = 10h) [reset = h]

Short Description: Index Position Latch

Long Description:

Return to Summary Table

Table 3-816. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0010h
CONTROLSS_EQEP1	5027 1010h
CONTROLSS_EQEP2	5027 2010h

Figure 3-392. CONTROLSS_EQEP0_QPOSILAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSILAT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSILAT															
RO															
0															

Access Types Legend

Table 3-817. QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSILAT	RO	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits.

3.8.6 CONTROLSS_EQEP0_QPOSSLAT Register (Offset = 14h) [reset = h]

Short Description: Strobe Position Latch

Long Description:

Return to Summary Table

Table 3-818. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0014h
CONTROLSS_EQEP1	5027 1014h
CONTROLSS_EQEP2	5027 2014h

Figure 3-393. CONTROLSS_EQEP0_QPOSSLAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSSLAT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSSLAT															
RO															
0															

Access Types Legend

Table 3-819. QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSSLAT	RO	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits.

3.8.7 CONTROLSS_EQEP0_QPOSLAT Register (Offset = 18h) [reset = h]

Short Description: Position Latch

Long Description:

Return to Summary Table

Table 3-820. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0018h
CONTROLSS_EQEP1	5027 1018h
CONTROLSS_EQEP2	5027 2018h

Figure 3-394. CONTROLSS_EQEP0_QPOSLAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QPOSLAT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSLAT															
RO															
0															

Access Types Legend

Table 3-821. QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSLAT	RO	0h	Position Latch The position-counter value is latched into this register on a unit time out event.

3.8.8 CONTROLSS_EQEP0_QUTMR Register (Offset = 1Ch) [reset = h]

Short Description: QEP Unit Timer

Long Description:

Return to Summary Table

Table 3-822. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 001Ch
CONTROLSS_EQEP1	5027 101Ch
CONTROLSS_EQEP2	5027 201Ch

Figure 3-395. CONTROLSS_EQEP0_QUTMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QUTMR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUTMR															
RW															
0															

Access Types Legend

Table 3-823. QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QUTMR	RW	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated.

3.8.9 CONTROLSS_EQEP0_QUPRD Register (Offset = 20h) [reset = h]

Short Description: QEP Unit Period

Long Description:

Return to Summary Table

Table 3-824. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0020h
CONTROLSS_EQEP1	5027 1020h
CONTROLSS_EQEP2	5027 2020h

Figure 3-396. CONTROLSS_EQEP0_QUPRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QUPRD															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUPRD															
RW															
0															

Access Types Legend

Table 3-825. QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QUPRD	RW	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes.

3.8.10 CONTROLSS_EQEP0_QWDTMR Register (Offset = 24h) [reset = h]

Short Description: QEP Watchdog Timer

Long Description:

Return to Summary Table

Table 3-826. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0024h
CONTROLSS_EQEP1	5027 1024h
CONTROLSS_EQEP2	5027 2024h

Figure 3-397. CONTROLSS_EQEP0_QWDTMR Name Register

15	14	13	12	11	10	9	8
QWDTMR							
RW							
0							
7	6	5	4	3	2	1	0
QWDTMR							
RW							
0							

Access Types Legend

Table 3-827. QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QWDTMR	RW	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion.

3.8.11 CONTROLSS_EQEP0_QWDPRD Register (Offset = 26h) [reset = h]

Short Description: QEP Watchdog Period

Long Description:

Return to Summary Table

Table 3-828. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0026h
CONTROLSS_EQEP1	5027 1026h
CONTROLSS_EQEP2	5027 2026h

Figure 3-398. CONTROLSS_EQEP0_QWDPRD Name Register

15	14	13	12	11	10	9	8
QWDPRD							
RW							
0							
7	6	5	4	3	2	1	0
QWDPRD							
RW							
0							

Access Types Legend

Table 3-829. QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QWDPRD	RW	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated.

3.8.12 CONTROLSS_EQEP0_QDECCTL Register (Offset = 28h) [reset = h]

Short Description: Quadrature Decoder Control

Long Description:

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Table 3-830. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0028h
CONTROLSS_EQEP1	5027 1028h
CONTROLSS_EQEP2	5027 2028h

Figure 3-399. CONTROLSS_EQEP0_QDECCTL Name Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
RW		RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0
7	6	5	4	3	2	1	0
QBP	QIP	QSP	RESERVED				QIDIRE
RW	RW	RW	RO				RW
0	0	0	0				0

Access Types Legend

Table 3-831. QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	QSRC	RW	0h	Position-counter source selection
13	SOEN	RW	0h	Sync output-enable 0 | SYNC_DISABLEDisable position-compare sync output 1 | SYNC_ENABLEEnable position-compare sync output
12	SPSEL	RW	0h	Sync output pin selection 0 | INDEX_PINIndex pin is used for sync output 1 | STROBE_PINStrobe pin is used for sync output
11	XCR	RW	0h	External Clock Rate 0 | XCR_2XRESOL2x resolution: Count the rising/falling edge 1 | XCR_1XRESOL1x resolution: Count the rising edge only
10	SWAP	RW	0h	CLK/DIR Signal Source for Position Counter 0 | SWAP_DISABLEQuadrature-clock inputs are not swapped 1 | SWAP_ENABLEQuadrature-clock inputs are swapped
9	IGATE	RW	0h	Index pulse gating option 0 | IGATE_DISABLEDisable gating of Index pulse 1 | IGATE_ENABLEGate the index pin with strobe
8	QAP	RW	0h	QEPA input polarity 0 | QAP_NOPOLARNo effect 1 | QAP_POLARNegates QEPA input
7	QBP	RW	0h	QEPB input polarity 0 | QBP_NOPOLARNo effect 1 | QBP_POLARNegates QEPB input
6	QIP	RW	0h	QEPI input polarity 0 | QIP_NOPOLARNo effect 1 | QIP_POLARNegates QEPI input
5	QSP	RW	0h	QEPS input polarity 0 | QSP_NOPOLARNo effect 1 | QSP_POLARNegates QEPS input
4 - 1	RESERVED	RO		Reserved
0	QIDIRE	RW	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled

3.8.13 CONTROLSS_EQEP0_QEPCTL Register (Offset = 2Ah) [reset = h]

Short Description: QEP Control

Long Description:

Return to Summary Table

Table 3-832. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Ah
CONTROLSS_EQEP1	5027 102Ah
CONTROLSS_EQEP2	5027 202Ah

Figure 3-400. CONTROLSS_EQEP0_QEPCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
RW		RW		RW		RW	
0		0		0		0	
7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
RW	RW	RW		RW	RW	RW	RW
0	0	0		0	0	0	0

Access Types Legend

Table 3-833. QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREE_SOFT	RW	0h	Emulation mode 0x0 | FREE_SOFT_0QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 0x1 | FREE_SOFT_1QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 0x2 | FREE_SOFT_2QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 0x3 | FREE_SOFT_3Same as FREE_SOFT_2
13 - 12	PCRM	RW	0h	Postion counter reset 0x0 | PCRM_INDEXPosition counter reset on an index event 0x1 | PCRM_MAXPOSPosition counter reset on the maximum position 0x2 | PCRM_FIRSTINDEXPosition counter reset on the first index event 0x3 | PCRM_TIMEEVENTPosition counter reset on a unit time event
11 - 10	SEI	RW	0h	Strobe event initialization of position counter 0x0 | SEI_NOTHING0Does nothing (action disabled) 0x1 | SEI_NOTHING1Does nothing (action disabled) 0x2 | SEI_INITQEPSRISINGInitializes the position counter on rising edge of the QEPS signal 0x3 | SEI_INITQEPSCLOCKClockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9 - 8	IEI	RW	0h	Index event init of position count 0x0 | IEI_NOTHING0Do nothing (action disabled) 0x1 | IEI_NOTHING1Do nothing (action disabled) 0x2 | IEI_INITRISINGInitializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 0x3 | IEI_INITFALLINGInitializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)

Table 3-833. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SWI	RW	0h	Software init position counter 0 | SWI_NOTHINGDo nothing (action disabled) 1 | SWI_INITPOSInitialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	RW	0h	Strobe event latch of position counter 0 | SEL_QEPSRISINGThe position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1 | SEL_QEPSCLOCKClockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5 - 4	IEL	RW	0h	Index event latch of position counter (software index marker) 0x0 | IEL_RSVDReserved 0x1 | IEL_POSRISINGLatches position counter on rising edge of the index signal 0x2 | IEL_POSFALLINGLatches position counter on falling edge of the index signal 0x3 | IEL_SIMSoftware index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.
3	QPEN	RW	0h	Quadrature position counter enable/software reset 0 | QPEN_RESETReset the eQEP peripheral internal operating flags/ read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLG register do not get reset or cleared and show the actual state of that flag. 1 | QPEN_ENABLEeQEP position counter is enabled
2	QCLM	RW	0h	QEP capture latch mode 0 | QCLM_CPULatch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1 | QCLM_TIMEOUTLatch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	RW	0h	QEP unit timer enable 0 | UTE_DISABLEDisable eQEP unit timer 1 | UTE_ENABLEEnable unit timer
0	WDE	RW	0h	QEP watchdog enable 0 | WDE_DISABLEDisable the eQEP watchdog timer 1 | WDE_ENABLEEnable the eQEP watchdog timer

3.8.14 CONTROLSS_EQEP0_QCAPCTL Register (Offset = 2Ch) [reset = h]

Short Description: Qaudrature Capture Control

Long Description:

Return to Summary Table

Table 3-834. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Ch
CONTROLSS_EQEP1	5027 102Ch
CONTROLSS_EQEP2	5027 202Ch

Figure 3-401. CONTROLSS_EQEP0_QCAPCTL Name Register

15	14	13	12	11	10	9	8
CEN	RESERVED						
RW	RO						
0	0						
7	6	5	4	3	2	1	0
RESERVED	CCPS			UPPS			
RO	RW			RW			
0	0			0			

Access Types Legend

Table 3-835. QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	RW	0h	Enable eQEP capture 0 | CEN_DISABLEeQEP capture unit is disabled 1 | CEN_ENABLEeQEP capture unit is enabled
14 - 7	RESERVED	RO		Reserved
6 - 4	CCPS	RW	0h	eQEP capture timer clock prescaler 0x0 | SYSCLKOUT1CAPCLK = SYSCLKOUT/1 0x1 | SYSCLKOUT2CAPCLK = SYSCLKOUT/2 0x2 | SYSCLKOUT4CAPCLK = SYSCLKOUT/4 0x3 | SYSCLKOUT8CAPCLK = SYSCLKOUT/8 0x4 | SYSCLKOUT16CAPCLK = SYSCLKOUT/16 0x5 | SYSCLKOUT32CAPCLK = SYSCLKOUT/32 0x6 | SYSCLKOUT64CAPCLK = SYSCLKOUT/64 0x7 | SYSCLKOUT128CAPCLK = SYSCLKOUT/128
3 - 0	UPPS	RW	0h	Unit position event prescaler 0x0 | QCLK1UPEVNT = QCLK/1 0x1 | QCLK2UPEVNT = QCLK/2 0x2 | QCLK4UPEVNT = QCLK/4 0x3 | QCLK8UPEVNT = QCLK/8 0x4 | QCLK16UPEVNT = QCLK/16 0x5 | QCLK32UPEVNT = QCLK/32 0x6 | QCLK64UPEVNT = QCLK/64 0x7 | QCLK128UPEVNT = QCLK/128 0x8 | QCLK256UPEVNT = QCLK/256 0x9 | QCLK512UPEVNT = QCLK/512 0xA | QCLK1024UPEVNT = QCLK/1024 0xB | QCLK2048UPEVNT = QCLK/2048 0xC | QCLK_RSVD0Reserved 0xD | QCLK_RSVD1Reserved 0xE | QCLK_RSVD2Reserved 0xF | QCLK_RSVD3Reserved

3.8.15 CONTROLSS_EQEP0_QPOSCTL Register (Offset = 2Eh) [reset = h]

Short Description: Position Compare Control

Long Description:

Return to Summary Table

Table 3-836. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Eh
CONTROLSS_EQEP1	5027 102Eh
CONTROLSS_EQEP2	5027 202Eh

Figure 3-402. CONTROLSS_EQEP0_QPOSCTL Name Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
RW	RW	RW	RW	RW			
0	0	0	0	0			
7	6	5	4	3	2	1	0
PCSPW							
RW							
0							

Access Types Legend

Table 3-837. QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	RW	0h	Position compare of shadow enable 0 | PCSHDW_DISABLEShadow disabled, load Immediate 1 | PCSHDW_ENABLEShadow enabled
14	PCLOAD	RW	0h	Position compare of shadow load 0 | PCLOAD_0Load on QPOSCNT = 0 1 | PCLOAD_QPOSCMPLoad when QPOSCNT = QPOSCMP
13	PCPOL	RW	0h	Polarity of sync output 0 | PCPOL_HIGHActive HIGH pulse output 1 | PCPOL_LOWActive LOW pulse output
12	PCE	RW	0h	Position compare enable/disable 0 | PCE_DISABLEDisable position compare unit 1 | PCE_ENABLEEnable position compare unit
11 - 0	PCSPW	RW	0h	Select-position-compare sync output pulse width 0x000 | SYSCLKOUT41 * 4 * SYSCLKOUT cycles 0x001 | SYSCLKOUT82 * 4 * SYSCLKOUT cycles 0xFFF | SYSCLKOUT163844096 * 4 * SYSCLKOUT cycles

3.8.16 CONTROLSS_EQEP0_QEINT Register (Offset = 30h) [reset = h]

Short Description: QEP Interrupt Control

Long Description:

Return to Summary Table

Table 3-838. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0030h
CONTROLSS_EQEP1	5027 1030h
CONTROLSS_EQEP2	5027 2030h

Figure 3-403. CONTROLSS_EQEP0_QEINT Name Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
RO			RW	RW	RW	RW	RW
0			0	0	0	0	0
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED
RW	RW	RW	RW	RW	RW	RW	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-839. QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW	0h	QMA Error Interrupt enable 0 | QMAE_DISABLEInterrupt is disabled 1 | QMAE_ENABLEInterrupt is enabled
11	UTO	RW	0h	Unit time out interrupt enable 0 | UTO_DISABLEInterrupt is disabled 1 | UTO_ENABLEInterrupt is enabled
10	IEL	RW	0h	Index event latch interrupt enable 0 | IEL_DISABLEInterrupt is disabled 1 | IEL_ENABLEInterrupt is enabled
9	SEL	RW	0h	Strobe event latch interrupt enable 0 | SEL_DISABLEInterrupt is disabled 1 | SEL_ENABLEInterrupt is enabled
8	PCM	RW	0h	Position-compare match interrupt enable 0 | PCM_DISABLEInterrupt is disabled 1 | PCM_ENABLEInterrupt is enabled
7	PCR	RW	0h	Position-compare ready interrupt enable 0 | PCR_DISABLEInterrupt is disabled 1 | PCR_ENABLEInterrupt is enabled
6	PCO	RW	0h	Position counter overflow interrupt enable 0 | PCO_DISABLEInterrupt is disabled 1 | PCO_ENABLEInterrupt is enabled
5	PCU	RW	0h	Position counter underflow interrupt enable 0 | PCU_DISABLEInterrupt is disabled 1 | PCU_ENABLEInterrupt is enabled
4	WTO	RW	0h	Watchdog time out interrupt enable 0 | WTO_DISABLEInterrupt is disabled 1 | WTO_ENABLEInterrupt is enabled
3	QDC	RW	0h	Quadrature direction change interrupt enable 0 | QDC_DISABLEInterrupt is disabled 1 | QDC_ENABLEInterrupt is enabled
2	QPE	RW	0h	Quadrature phase error interrupt enable 0 | QPE_DISABLEInterrupt is disabled 1 | QPE_ENABLEInterrupt is enabled
1	PCE	RW	0h	Position counter error interrupt enable 0 | PCE_DISABLEInterrupt is disabled 1 | PCE_ENABLEInterrupt is enabled
0	RESERVED	RO		Reserved

3.8.17 CONTROLSS_EQEP0_QFLG Register (Offset = 32h) [reset = h]

Short Description: QEP Interrupt Flag

Long Description:

Return to Summary Table

Table 3-840. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0032h
CONTROLSS_EQEP1	5027 1032h
CONTROLSS_EQEP2	5027 2032h

Figure 3-404. CONTROLSS_EQEP0_QFLG Name Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
RO			RO	RO	RO	RO	RO
0			0	0	0	0	0
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-841. QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RO	0h	QMA Error interrupt flag Read0 | QMAE_NOFLAGNo interrupt generated Read1 | QMAE_FLAGInterrupt was generated
11	UTO	RO	0h	Unit time out interrupt flag Read0 | UTO_NOFLAGNo interrupt generated Read1 | UTO_FLAGSet by eQEP unit timer period match
10	IEL	RO	0h	Index event latch interrupt flag Read0 | IEL_NOFLAGNo interrupt generated Read1 | IEL_FLAGThis bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	RO	0h	Strobe event latch interrupt flag Read0 | SEL_NOFLAGNo interrupt generated Read1 | SEL_FLAGThis bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	RO	0h	eQEP compare match event interrupt flag Read0 | PCM_NOFLAGNo interrupt generated Read1 | PCM_FLAGThis bit is set on position-compare match
7	PCR	RO	0h	Position-compare ready interrupt flag Read0 | PCR_NOFLAGNo interrupt generated Read1 | PCR_FLAGThis bit is set after transferring the shadow register value to the active position compare register
6	PCO	RO	0h	Position counter overflow interrupt flag Read0 | PCO_NOFLAGNo interrupt generated Read1 | PCO_FLAGThis bit is set on position counter overflow.
5	PCU	RO	0h	Position counter underflow interrupt flag Read0 | PCU_NOFLAGNo interrupt generated Read1 | PCU_FLAGThis bit is set on position counter underflow.
4	WTO	RO	0h	Watchdog timeout interrupt flag Read0 | WTO_NOFLAGNo interrupt generated Read1 | WTO_FLAGSet by watchdog timeout
3	QDC	RO	0h	Quadrature direction change interrupt flag Read0 | QDC_NOFLAGNo interrupt generated Read1 | QDC_FLAGInterrupt was generated

Table 3-841. QFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PHE	RO	0h	Quadrature phase error interrupt flag Read0 | PHE_NOFLAGNo interrupt generated Read1 | PHE_FLAGSet on simultaneous transition of QEPA and QEPB
1	PCE	RO	0h	Position counter error interrupt flag Read0 | PCE_NOFLAGNo interrupt generated Read1 | PCE_FLAGPosition counter error
0	INT	RO	0h	Global interrupt status flag Read0 | INT_NOFLAGNo interrupt generated Read1 | INT_FLAGInterrupt was generated

3.8.18 CONTROLSS_EQEP0_QCLR Register (Offset = 34h) [reset = h]

Short Description: QEP Interrupt Clear

Long Description:

Return to Summary Table

Table 3-842. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0034h
CONTROLSS_EQEP1	5027 1034h
CONTROLSS_EQEP2	5027 2034h

Figure 3-405. CONTROLSS_EQEP0_QCLR Name Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
RO			RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0			0	0	0	0	0
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-843. QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW RRETURNS 0S	0h	Clear QMA Error interrupt flag 0 | QMAE_NOEFFECTNo effect 1 | QMAE_CLRClears the interrupt flag
11	UTO	RW RRETURNS 0S	0h	Clear unit time out interrupt flag 0 | UTO_NOEFFECTNo effect 1 | UTO_CLRClears the interrupt flag
10	IEL	RW RRETURNS 0S	0h	Clear index event latch interrupt flag 0 | IEL_NOEFFECTNo effect 1 | IEL_CLRClears the interrupt flag
9	SEL	RW RRETURNS 0S	0h	Clear strobe event latch interrupt flag 0 | SEL_NOEFFECTNo effect 1 | SEL_CLRClears the interrupt flag
8	PCM	RW RRETURNS 0S	0h	Clear eQEP compare match event interrupt flag 0 | PCM_NOEFFECTNo effect 1 | PCM_CLRClears the interrupt flag
7	PCR	RW RRETURNS 0S	0h	Clear position-compare ready interrupt flag 0 | PCR_NOEFFECTNo effect 1 | PCR_CLRClears the interrupt flag
6	PCO	RW RRETURNS 0S	0h	Clear position counter overflow interrupt flag 0 | PCO_NOEFFECTNo effect 1 | PCO_CLRClears the interrupt flag
5	PCU	RW RRETURNS 0S	0h	Clear position counter underflow interrupt flag 0 | PCU_NOEFFECTNo effect 1 | PCU_CLRClears the interrupt flag
4	WTO	RW RRETURNS 0S	0h	Clear watchdog timeout interrupt flag 0 | WTO_NOEFFECTNo effect 1 | WTO_CLRClears the interrupt flag

Table 3-843. QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QDC	RW RRETURNS 0S	0h	Clear quadrature direction change interrupt flag 0 | QDC_NOEFFECTNo effect 1 | QDC_CLRClears the interrupt flag
2	PHE	RW RRETURNS 0S	0h	Clear quadrature phase error interrupt flag 0 | PHE_NOEFFECTNo effect 1 | PHE_CLRClears the interrupt flag
1	PCE	RW RRETURNS 0S	0h	Clear position counter error interrupt flag 0 | PCE_NOEFFECTNo effect 1 | PCE_CLRClears the interrupt flag
0	INT	RW RRETURNS 0S	0h	Global interrupt clear flag 0 | INT_NOEFFECTNo effect 1 | INT_CLRClears the interrupt flag

3.8.19 CONTROLSS_EQEP0_QFRC Register (Offset = 36h) [reset = h]

Short Description: QEP Interrupt Force

Long Description:

Return to Summary Table

Table 3-844. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0036h
CONTROLSS_EQEP1	5027 1036h
CONTROLSS_EQEP2	5027 2036h

Figure 3-406. CONTROLSS_EQEP0_QFRC Name Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
RO			RW	RW	RW	RW	RW
0			0	0	0	0	0
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED
RW	RW	RW	RW	RW	RW	RW	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-845. QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW	0h	Force QMA error interrupt 0 | QMAE_NOEFFECTNo effect 1 | QMAE_FORCEForce the interrupt
11	UTO	RW	0h	Force unit time out interrupt 0 | UTO_NOEFFECTNo effect 1 | UTO_FORCEForce the interrupt
10	IEL	RW	0h	Force index event latch interrupt 0 | IEL_NOEFFECTNo effect 1 | IEL_FORCEForce the interrupt
9	SEL	RW	0h	Force strobe event latch interrupt 0 | SEL_NOEFFECTNo effect 1 | SEL_FORCEForce the interrupt
8	PCM	RW	0h	Force position-compare match interrupt 0 | PCM_NOEFFECTNo effect 1 | PCM_FORCEForce the interrupt
7	PCR	RW	0h	Force position-compare ready interrupt 0 | PCR_NOEFFECTNo effect 1 | PCR_FORCEForce the interrupt
6	PCO	RW	0h	Force position counter overflow interrupt 0 | PCO_NOEFFECTNo effect 1 | PCO_FORCEForce the interrupt
5	PCU	RW	0h	Force position counter underflow interrupt 0 | PCU_NOEFFECTNo effect 1 | PCU_FORCEForce the interrupt
4	WTO	RW	0h	Force watchdog time out interrupt 0 | WTO_NOEFFECTNo effect 1 | WTO_FORCEForce the interrupt
3	QDC	RW	0h	Force quadrature direction change interrupt 0 | QDC_NOEFFECTNo effect 1 | QDC_FORCEForce the interrupt
2	PHE	RW	0h	Force quadrature phase error interrupt 0 | PHE_NOEFFECTNo effect 1 | PHE_FORCEForce the interrupt
1	PCE	RW	0h	Force position counter error interrupt 0 | PCE_NOEFFECTNo effect 1 | PCE_FORCEForce the interrupt
0	RESERVED	RO		Reserved

3.8.20 CONTROLSS_EQEP0_QEPSTS Register (Offset = 38h) [reset = h]

Short Description: QEP Status

Long Description:

Return to Summary Table

Table 3-846. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0038h
CONTROLSS_EQEP1	5027 1038h
CONTROLSS_EQEP2	5027 2038h

Figure 3-407. CONTROLSS_EQEP0_QEPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
RW	RO	RO	RO	RW	RW	RW	RO
1	0	0	0	0	0	0	0

Access Types Legend

Table 3-847. QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	UPEVNT	RW	1h	Unit position event flag 0 | UPEVNT_NODETCTNo unit position event detected 1 | UPEVNT_DETCTUnit position event detected. Write 1 to clear
6	FIDF	RO	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Read0 | FIDF_COUNTERCLKCounter-clockwise rotation (or reverse movement) on the first index event Read1 | FIDF_CLKClockwise rotation (or forward movement) on the first index event
5	QDF	RO	0h	Quadrature direction flag Read0 | QDF_COUNTERCLKCounter-clockwise rotation (or reverse movement) Read1 | QDF_CLKClockwise rotation (or forward movement)
4	QDLF	RO	0h	eQEP direction latch flag Read0 | QDLF_COUNTERCLKCounter-clockwise rotation (or reverse movement) on index event marker Read1 | QDLF_CLKClockwise rotation (or forward movement) on index event marker
3	COEF	RW	0h	Capture overflow error flag 0 | COEF_WRT1Overflow has not occurred. 1 | COEF_OVFOverflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	RW	0h	Capture direction error flag 0 | CDEF_WRT1Capture direction error has not occurred. 1 | CDEF_DIRECTDirection change occurred between the capture position event. This bit is cleared by writing a '1'.
1	FIMF	RW	0h	First index marker flag 0 | FIMF_WRT1First index pulse has not occurred. 1 | FIMF_SETINDEXSet by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	RO	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Read0 | PCEF_NOERRORNo error occurred during the last index transition Read1 | PCEF_ERRORPosition counter error

3.8.21 CONTROLSS_EQEP0_QCTMR Register (Offset = 3Ah) [reset = h]

Short Description: QEP Capture Timer

Long Description:

Return to Summary Table

Table 3-848. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Ah
CONTROLSS_EQEP1	5027 103Ah
CONTROLSS_EQEP2	5027 203Ah

Figure 3-408. CONTROLSS_EQEP0_QCTMR Name Register

15	14	13	12	11	10	9	8
QCTMR							
RW							
0							
7	6	5	4	3	2	1	0
QCTMR							
RW							
0							

Access Types Legend

Table 3-849. QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCTMR	RW	0h	This register provides time base for edge capture unit.

3.8.22 CONTROLSS_EQEP0_QCPRD Register (Offset = 3Ch) [reset = h]

Short Description: QEP Capture Period

Long Description:

Return to Summary Table

Table 3-850. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Ch
CONTROLSS_EQEP1	5027 103Ch
CONTROLSS_EQEP2	5027 203Ch

Figure 3-409. CONTROLSS_EQEP0_QCPRD Name Register

15	14	13	12	11	10	9	8
QCPRD							
RW							
0							
7	6	5	4	3	2	1	0
QCPRD							
RW							
0							

Access Types Legend

Table 3-851. QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCPRD	RW	0h	This register holds the period count value between the last successive eQEP position events

3.8.23 CONTROLSS_EQEP0_QCTMRLAT Register (Offset = 3Eh) [reset = h]

Short Description: QEP Capture Latch

Long Description:

Return to Summary Table

Table 3-852. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Eh
CONTROLSS_EQEP1	5027 103Eh
CONTROLSS_EQEP2	5027 203Eh

Figure 3-410. CONTROLSS_EQEP0_QCTMRLAT Name Register

15	14	13	12	11	10	9	8
QCTMRLAT							
RO							
0							
7	6	5	4	3	2	1	0
QCTMRLAT							
RO							
0							

Access Types Legend

Table 3-853. QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCTMRLAT	RO	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

3.8.24 CONTROLSS_EQEP0_QCPRDLAT Register (Offset = 40h) [reset = h]

Short Description: QEP Capture Period Latch

Long Description:

Return to Summary Table

Table 3-854. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0040h
CONTROLSS_EQEP1	5027 1040h
CONTROLSS_EQEP2	5027 2040h

Figure 3-411. CONTROLSS_EQEP0_QCPRDLAT Name Register

15	14	13	12	11	10	9	8
QCPRDLAT							
RO							
0							
7	6	5	4	3	2	1	0
QCPRDLAT							
RO							
0							

Access Types Legend

Table 3-855. QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCPRDLAT	RO	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

3.8.25 CONTROLSS_EQEP0_REV Register (Offset = 60h) [reset = h]

Short Description: QEP Revision Number

Long Description:

Return to Summary Table

Table 3-856. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0060h
CONTROLSS_EQEP1	5027 1060h
CONTROLSS_EQEP2	5027 2060h

Figure 3-412. CONTROLSS_EQEP0_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MINOR			MAJOR		
RO RRETURNS0S										RO			RO		
0										10			1		

Access Types Legend

Table 3-857. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED	RO RRETURNS 0S		Reserved
5 - 3	MINOR	RO	Ah	This field specifies the Minor Revision number for the eQEP IP.
2 - 0	MAJOR	RO	1h	This field specifies the Major Revision number for the eQEP IP.

3.8.26 CONTROLSS_EQEP0_QEPSTROBESEL Register (Offset = 64h) [reset = h]

Short Description: QEP Strobe select register

Long Description:

Return to Summary Table

Table 3-858. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0064h
CONTROLSS_EQEP1	5027 1064h
CONTROLSS_EQEP2	5027 2064h

Figure 3-413. CONTROLSS_EQEP0_QEPSTROBESEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														STROBESEL	
RO RRETURNS0S														RW	
0														0	

Access Types Legend

Table 3-859. QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO RRETURNS 0S		Reserved
1 - 0	STROBESEL	RW	0h	Strobe source select: 0x0 | QS_AFTER_POL_MUXQEP Strobe after polarity mux 0x1 | QS_AFTER_POL_MUXQEP Strobe after polarity mux 0x2 | ADCSOCA_AS_QSQEP Strobe after polarity mux ORed with ADCSOCA 0x3 | ADCSOCB_AS_QSQEP Strobe after polarity mux ORed with ADCSOCB

3.8.27 CONTROLSS_EQEP0_QMACTRL Register (Offset = 68h) [reset = h]

Short Description: QMA Control register

Long Description:

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Table 3-860. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0068h
CONTROLSS_EQEP1	5027 1068h
CONTROLSS_EQEP2	5027 2068h

Figure 3-414. CONTROLSS_EQEP0_QMACTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO RRETURNS0S															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MODE		
RO RRETURNS0S													RW		
0													0		

Access Types Legend

Table 3-861. QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2 - 0	MODE	RW	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed (reserved) 1xx : QMA Module is bypassed (reserved)

3.8.28 CONTROLSS_EQEP0_QEPSRCSEL Register (Offset = 6Ch) [reset = h]

Short Description: QEP Source Select Register

Long Description:

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Table 3-862. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 006Ch
CONTROLSS_EQEP1	5027 106Ch
CONTROLSS_EQEP2	5027 206Ch

Figure 3-415. CONTROLSS_EQEP0_QEPSRCSEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			QEPSSEL					RESERVED			QEPISEL				
RO RRETURNS0S			RW					RO RRETURNS0S			RW				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			QEPBSEL					RESERVED			QEPASEL				
RO RRETURNS0S			RW					RO RRETURNS0S			RW				
0			0					0			0				

Access Types Legend

Table 3-863. QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED	RO RRETURNS 0S		Reserved
28 - 24	QEPSSEL	RW	0h	QEP Strobe source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
23 - 21	RESERVED	RO RRETURNS 0S		Reserved
20 - 16	QEPISEL	RW	0h	QEP Index source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
15 - 13	RESERVED	RO RRETURNS 0S		Reserved
12 - 8	QEPBSEL	RW	0h	QEPB source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
7 - 5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	QEPASEL	RW	0h	QEPA source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.

Table 3-864. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RO RRETURNS0S	RO RRETURNS0S	Undefined

3.9 C2K_FSI_RX Registers

Table 3-865. CONTROLSS_FSI0_RX0, CONTROLSS_FSI_RX0_CONTROLSS_FSI_RX Registers, Base Address=5029 0000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_FSI_RX0 Physical Address	CONTROLSS_FSI_RX1 Physical Address	CONTROLSS_FSI_RX2 Physical Address
0h	16	CONTROLSS_FSI_RX0_RX_MASTER_CTRL_ALTC_	Receive master control register	5029 0000h	5029 1000h	502B 0000h
8h	16	CONTROLSS_FSI_RX0_RX_OPER_CTRL	Receive operation control register	5029 0008h	5029 1008h	502B 0008h
Ch	16	CONTROLSS_FSI_RX0_RX_FRAME_INFO	Receive frame control register	5029 000Ch	5029 100Ch	502B 000Ch
Eh	16	CONTROLSS_FSI_RX0_RX_FRAME_TAG_UDATA	Receive frame tag and user data register	5029 000Eh	5029 100Eh	502B 000Eh
10h	16	CONTROLSS_FSI_RX0_RX_DMA_CTRL	Receive DMA event control register	5029 0010h	5029 1010h	502B 0010h
14h	16	CONTROLSS_FSI_RX0_RX_EVT_STS_ALT1_	Receive event and error status flag register	5029 0014h	5029 1014h	502B 0014h
16h	16	CONTROLSS_FSI_RX0_RX_CRC_INFO	Receive CRC info of received and computed CRC	5029 0016h	5029 1016h	502B 0016h
18h	16	CONTROLSS_FSI_RX0_RX_EVT_CLR_ALT1_	Receive event and error clear register	5029 0018h	5029 1018h	502B 0018h
1Ah	16	CONTROLSS_FSI_RX0_RX_EVT_FRC_ALT1_	Receive event and error flag force register	5029 001Ah	5029 101Ah	502B 001Ah
1Ch	16	CONTROLSS_FSI_RX0_RX_BUF_PTR_LOAD	Receive buffer pointer load register	5029 001Ch	5029 101Ch	502B 001Ch
1Eh	16	CONTROLSS_FSI_RX0_RX_BUF_PTR_STS	Receive buffer pointer status register	5029 001Eh	5029 101Eh	502B 001Eh
20h	16	CONTROLSS_FSI_RX0_RX_FRAME_WD_CTRL	Receive frame watchdog control register	5029 0020h	5029 1020h	502B 0020h
24h	32	CONTROLSS_FSI_RX0_RX_FRAME_WD_REF	Receive frame watchdog counter reference	5029 0024h	5029 1024h	502B 0024h
28h	32	CONTROLSS_FSI_RX0_RX_FRAME_WD_CNT	Receive frame watchdog current count	5029 0028h	5029 1028h	502B 0028h
2Ch	16	CONTROLSS_FSI_RX0_RX_PING_WD_CTRL	Receive ping watchdog control register	5029 002Ch	5029 102Ch	502B 002Ch
2Eh	16	CONTROLSS_FSI_RX0_RX_PING_TAG	Receive ping tag register	5029 002Eh	5029 102Eh	502B 002Eh
30h	32	CONTROLSS_FSI_RX0_RX_PING_WD_REF	Receive ping watchdog counter reference	5029 0030h	5029 1030h	502B 0030h

Table 3-865. CONTROLSS_FSI0_RX0, CONTROLSS_FSI_RX0_CONTROLSS_FSI_RX Registers, Base Address=5029 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_FSI_RX0 Physical Address	CONTROLSS_FSI_RX1 Physical Address	CONTROLSS_FSI_RX2 Physical Address
34h	32	CONTROLSS_FSI_RX0_RX_PING_WD_CNT	Receive pingwatchdog current count	5029 0034h	5029 1034h	502B 0034h
38h	16	CONTROLSS_FSI_RX0_RX_INT1_CTRL_ALT1_	Receive interrupt control register for RX_INT1	5029 0038h	5029 1038h	502B 0038h
3Ah	16	CONTROLSS_FSI_RX0_RX_INT2_CTRL_ALT1_	Receive interrupt control register for RX_INT2	5029 003Ah	5029 103Ah	502B 003Ah
3Ch	16	CONTROLSS_FSI_RX0_RX_LOCK_CTRL	Receive lock control register	5029 003Ch	5029 103Ch	502B 003Ch
40h	32	CONTROLSS_FSI_RX0_RX_ECC_DATA	Receive ECC data register	5029 0040h	5029 1040h	502B 0040h
44h	16	CONTROLSS_FSI_RX0_RX_ECC_VAL	Receive ECC value register	5029 0044h	5029 1044h	502B 0044h
48h	32	CONTROLSS_FSI_RX0_RX_ECC_SEC_DATA	Receive ECC corrected data register	5029 0048h	5029 1048h	502B 0048h
4Ch	16	CONTROLSS_FSI_RX0_RX_ECC_LOG	Receive ECC log and status register	5029 004Ch	5029 104Ch	502B 004Ch
50h	16	CONTROLSS_FSI_RX0_RX_FRAME_TAG_CMP	Receive frame tag compare register	5029 0050h	5029 1050h	502B 0050h
52h	16	CONTROLSS_FSI_RX0_RX_PING_TAG_CMP	Receive ping tag compare register	5029 0052h	5029 1052h	502B 0052h
58h	32	CONTROLSS_FSI_RX0_RX_TRIG_CTRL_0	Receive Trigger Control register 0	5029 0058h	5029 1058h	502B 0058h
5Ch	32	CONTROLSS_FSI_RX0_RX_TRIG_WIDTH_0	Receive Trigger Wdith register 0	5029 005Ch	5029 105Ch	502B 005Ch
60h	16	CONTROLSS_FSI_RX0_RX_DLYLINE_CTRL	Receive delay line control register	5029 0060h	5029 1060h	502B 0060h
64h	32	CONTROLSS_FSI_RX0_RX_TRIG_CTRL_1	Receive Trigger Control register 1	5029 0064h	5029 1064h	502B 0064h
68h	32	CONTROLSS_FSI_RX0_RX_TRIG_CTRL_2	Receive Trigger Control register 2	5029 0068h	5029 1068h	502B 0068h
6Ch	32	CONTROLSS_FSI_RX0_RX_TRIG_CTRL_3	Receive Trigger Control register 3	5029 006Ch	5029 106Ch	502B 006Ch
70h	32	CONTROLSS_FSI_RX0_RX_VIS_1	Receive debug visibility register 1	5029 0070h	5029 1070h	502B 0070h
74h	16	CONTROLSS_FSI_RX0_RX_UDATA_FILTER	Receive User Data Filter Control register	5029 0074h	5029 1074h	502B 0074h
80h	16	CONTROLSS_FSI_RX0_RX_BUF_BASE	Base address for receive data buffer	5029 0080h	5029 1080h	502B 0080h

3.9.1 CONTROLSS_FSI_RX0_RX_MASTER_CTRL_ALTC_ Register (Offset = 0h) [reset = h]

Short Description: Receive master control register

Long Description:

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Table 3-866. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0000h
CONTROLSS_FSI_RX1	5029 1000h
CONTROLSS_FSI_RX2	502B 0000h
CONTROLSS_FSI_RX3	502B 1000h

Figure 3-416. CONTROLSS_FSI_RX0_RX_MASTER_CTRL_ALTC_ Name Register

15	14	13	12	11	10	9	8
KEY							
WO							
0							
7	6	5	4	3	2	1	0
RESERVED			DATA_FILTER_EN	INPUT_ISOLATE	SPI_PAIRING	INT_LOOPBACK	CORE_RST
RO			RW	RW	RW	RW	RW
0			0	0	0	0	0

Access Types Legend

Table 3-867. RX_MASTER_CTRL_ALTC_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 5	RESERVED	RO		Reserved
4	DATA_FILTER_EN	RW	0h	Data Filter Enable Bit. 0h (R/W) = Data filtering is disabled. 1h (R/W) = Data filtering is enabled.
3	INPUT_ISOLATE	RW	0h	When set to 1, the FSI RX inputs (RXCLK, RXD0 and RXD1) will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not affect the RX module itself.
2	SPI_PAIRING	RW	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only (RX_OPER_CTRL.SPI_MODE = 1) 0h (R/W) = SPI clock pairing is not enabled. 1h (R/W) = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

Table 3-867. RX_MASTER_CTRL_ALTC_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_LOOPBACK	RW	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h (R/W) = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h (R/W) = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.
0	CORE_RST	RW	0h	Receiver Master Core Reset bit This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h (R/W) = Receiver core is not in reset and can receive frames. 1h (R/W) = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

3.9.2 CONTROLSS_FSI_RX0_RX_OPER_CTRL Register (Offset = 8h) [reset = h]

Short Description: Receive operation control register

Long Description:

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Table 3-868. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0008h
CONTROLSS_FSI_RX1	5029 1008h
CONTROLSS_FSI_RX2	502B 0008h
CONTROLSS_FSI_RX3	502B 1008h

Figure 3-417. CONTROLSS_FSI_RX0_RX_OPER_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED							PING_WD_RST_MODE
RO							RW
0							0
7	6	5	4	3	2	1	0
ECC_SEL	N_WORDS				SPI_MODE	DATA_WIDTH	
RW	RW				RW	RW	
0	0				0	0	

Access Types Legend

Table 3-869. RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8	PING_WD_RST_MODE	RW	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h (R/W) = The ping watchdog counter will reset and restart only by ping frames. 1h (R/W) = The ping watchdog counter will reset and restart by any received frame.
7	ECC_SEL	RW	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used.
6 - 3	N_WORDS	RW	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data).
2	SPI_MODE	RW	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode.
1 - 0	DATA_WIDTH	RW	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h (R/W) = Data will be received on one data line, RXD0. 1h (R/W) = Data will be received on two data lines, RXD0 and RXD1. 2h, 3h (R/W) = Reserved

3.9.3 CONTROLSS_FSI_RX0_RX_FRAME_INFO Register (Offset = Ch) [reset = h]

Short Description: Receive frame control register

Long Description:

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Table 3-870. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 000Ch
CONTROLSS_FSI_RX1	5029 100Ch
CONTROLSS_FSI_RX2	502B 000Ch
CONTROLSS_FSI_RX3	502B 100Ch

Figure 3-418. CONTROLSS_FSI_RX0_RX_FRAME_INFO Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				FRAME_TYPE			
RO				RO			
0				0			

Access Types Legend

Table 3-871. RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	FRAME_TYPE	RO	0h	Received Frame Type This field indicates the type of frame that was successfully received last. 0000b (R/W) = A ping frame was received 0100b (R/W) = A DATA_1_WORD frame was received (16-bit data). 0101b (R/W) = A DATA_2_WORD frame was received (32-bit data). 0110b (R/W) = A DATA_4_WORD frame was received (64-bit data). 0111b (R/W) = A DATA_6_WORD frame was received (96-bit data). 0011b (R/W) = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words (1 to 16) to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b (R/W) = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used.

3.9.4 CONTROLSS_FSI_RX0_RX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = h]

Short Description: Receive frame tag and user data register

Long Description:

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Table 3-872. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 000Eh
CONTROLSS_FSI_RX1	5029 100Eh
CONTROLSS_FSI_RX2	502B 000Eh
CONTROLSS_FSI_RX3	502B 100Eh

Figure 3-419. CONTROLSS_FSI_RX0_RX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			FRAME_TAG				RESERVED
RO			RO				RO
0			0				0

Access Types Legend

Table 3-873. RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	USER_DATA	RO	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame.
7 - 5	RESERVED	RO		Reserved
4 - 1	FRAME_TAG	RO	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	RESERVED	RO		Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register (bits 4:0), application software can directly index into an array of 32-bit data.

3.9.5 CONTROLSS_FSI_RX0_RX_DMA_CTRL Register (Offset = 10h) [reset = h]

Short Description: Receive DMA event control register

Long Description:

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Table 3-874. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0010h
CONTROLSS_FSI_RX1	5029 1010h
CONTROLSS_FSI_RX2	502B 0010h
CONTROLSS_FSI_RX3	502B 1010h

Figure 3-420. CONTROLSS_FSI_RX0_RX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED							DMA_EVT_EN
RO							RW
0							0

Access Types Legend

Table 3-875. RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DMA_EVT_EN	RW	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames.

3.9.6 CONTROLSS_FSI_RX0_RX_EVT_STS_ALT1_ Register (Offset = 14h) [reset = h]

Short Description: Receive event and error status flag register

Long Description:

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Table 3-876. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0014h
CONTROLSS_FSI_RX1	5029 1014h
CONTROLSS_FSI_RX2	502B 0014h
CONTROLSS_FSI_RX3	502B 1014h

Figure 3-421. CONTROLSS_FSI_RX0_RX_EVT_STS_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-877. RX_EVT_STS_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	RO	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched error frame received. 1h (R) = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
13	DATA_TAG_MATCH	RO	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched data frame received. 1h (R) = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
12	PING_TAG_MATCH	RO	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched ping frame received. 1h (R) = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
11	DATA_FRAME	RO	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No data frame has been received. 1h (R) = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

Table 3-877. RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	FRAME_OVERRUN	RO	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame overrun has not ocurred. 1h (R) = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
9	PING_FRAME	RO	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No ping frame has been received. 1h (R) = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
8	ERR_FRAME	RO	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No error frame has been received. 1h (R) = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
7	BUF_UNDERRUN	RO	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive Buffer Underrun has not ocurred. 1h (R) = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
6	FRAME_DONE	RO	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No frame has been successfully received. 1h (R) = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
5	BUF_OVERRUN	RO	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive buffer overrun has not ocurred. 1h (R) = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
4	EOF_ERR	RO	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid end-of-frame has not been received. 1h (R) = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
3	TYPE_ERR	RO	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid frame type has not been received. 1h (R) = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
2	CRC_ERR	RO	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = CRC error has not occured. 1h (R) = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
1	FRAME_WD_TO	RO	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame watchdog timeout has not occured. 1h (R) = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

Table 3-877. RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PING_WD_TO	RO	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Ping watchdog timeout has not occured. 1h (R) = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

3.9.7 CONTROLSS_FSI_RX0_RX_CRC_INFO Register (Offset = 16h) [reset = h]

Short Description: Receive CRC info of received and computed CRC

Long Description:

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Table 3-878. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0016h
CONTROLSS_FSI_RX1	5029 1016h
CONTROLSS_FSI_RX2	502B 0016h
CONTROLSS_FSI_RX3	502B 1016h

Figure 3-422. CONTROLSS_FSI_RX0_RX_CRC_INFO Name Register

15	14	13	12	11	10	9	8
CALC_CRC							
RO							
0							
7	6	5	4	3	2	1	0
RX_CRC							
RO							
0							

Access Types Legend

Table 3-879. RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CALC_CRC	RO	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.
7 - 0	RX_CRC	RO	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.

3.9.8 CONTROLSS_FSI_RX0_RX_EVT_CLR_ALT1_ Register (Offset = 18h) [reset = h]

Short Description: Receive event and error clear register

Long Description:

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Table 3-880. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0018h
CONTROLSS_FSI_RX1	5029 1018h
CONTROLSS_FSI_RX2	502B 0018h
CONTROLSS_FSI_RX3	502B 1018h

Figure 3-423. CONTROLSS_FSI_RX0_RX_EVT_CLR_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
RO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-881. RX_EVT_CLR_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	WO	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
13	DATA_TAG_MATCH	WO	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
12	PING_TAG_MATCH	WO	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
11	DATA_FRAME	WO	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
10	FRAME_OVERRUN	WO	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
9	PING_FRAME	WO	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
8	ERR_FRAME	WO	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

Table 3-881. RX_EVT_CLR_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	BUF_UNDERRUN	WO	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
6	FRAME_DONE	WO	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
5	BUF_OVERRUN	WO	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
4	EOF_ERR	WO	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
3	TYPE_ERR	WO	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
2	CRC_ERR	WO	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
1	FRAME_WD_TO	WO	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
0	PING_WD_TO	WO	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

3.9.9 CONTROLSS_FSI_RX0_RX_EVT_FRC_ALT1_ Register (Offset = 1Ah) [reset = h]

Short Description: Receive event and error flag force register

Long Description:

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Table 3-882. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Ah
CONTROLSS_FSI_RX1	5029 101Ah
CONTROLSS_FSI_RX2	502B 001Ah
CONTROLSS_FSI_RX3	502B 101Ah

Figure 3-424. CONTROLSS_FSI_RX0_RX_EVT_FRC_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
RO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-883. RX_EVT_FRC_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	WO	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
13	DATA_TAG_MATCH	WO	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
12	PING_TAG_MATCH	WO	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
11	DATA_FRAME	WO	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.

Table 3-883. RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	FRAME_OVERRUN	WO	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
9	PING_FRAME	WO	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
8	ERR_FRAME	WO	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
7	BUF_UNDERRUN	WO	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
6	FRAME_DONE	WO	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
5	BUF_OVERRUN	WO	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
4	EOF_ERR	WO	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
3	TYPE_ERR	WO	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
2	CRC_ERR	WO	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
1	FRAME_WD_TO	WO	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.

Table 3-883. RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PING_WD_TO	WO	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.

3.9.10 CONTROLSS_FSI_RX0_RX_BUF_PTR_LOAD Register (Offset = 1Ch) [reset = h]

Short Description: Receive buffer pointer load register

Long Description:

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Table 3-884. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Ch
CONTROLSS_FSI_RX1	5029 101Ch
CONTROLSS_FSI_RX2	502B 001Ch
CONTROLSS_FSI_RX3	502B 101Ch

Figure 3-425. CONTROLSS_FSI_RX0_RX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				BUF_PTR_LOAD			
RO				RW			
0				0			

Access Types Legend

Table 3-885. RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	BUF_PTR_LOAD	RW	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after (3 RXCLK + 3 SYCLK) cycles.

3.9.11 CONTROLSS_FSI_RX0_RX_BUF_PTR_STS Register (Offset = 1Eh) [reset = h]

Short Description: Receive buffer pointer status register

Long Description:

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Table 3-886. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Eh
CONTROLSS_FSI_RX1	5029 101Eh
CONTROLSS_FSI_RX2	502B 001Eh
CONTROLSS_FSI_RX3	502B 101Eh

Figure 3-426. CONTROLSS_FSI_RX0_RX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			CURR_WORD_CNT				
RO			RO				
0			0				
7	6	5	4	3	2	1	0
RESERVED				CURR_BUF_PTR			
RO				RO			
0				0			

Access Types Legend

Table 3-887. RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 8	CURR_WORD_CNT	RO	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition.
7 - 4	RESERVED	RO		Reserved
3 - 0	CURR_BUF_PTR	RO	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

3.9.12 CONTROLSS_FSI_RX0_RX_FRAME_WD_CTRL Register (Offset = 20h) [reset = h]

Short Description: Receive frame watchdog control register

Long Description:

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Table 3-888. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0020h
CONTROLSS_FSI_RX1	5029 1020h
CONTROLSS_FSI_RX2	502B 0020h
CONTROLSS_FSI_RX3	502B 1020h

Figure 3-427. CONTROLSS_FSI_RX0_RX_FRAME_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED						FRAME_WD_EN	FRAME_WD_CNT_RST
RO						RW	RW
0						0	0

Access Types Legend

Table 3-889. RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	FRAME_WD_EN	RW	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter (RX_FRAME_WD_CNT) will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value (RX_FRAME_WD_REF) is reached, it will generate a frame watchdog timeout event (RX_EVT_STS.FRAME_WD_TO) and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h (R/W) = The frame watchdog counter is disabled and not running. 1h (R/W) = The frame watchdog counter logic is enabled and running.
0	FRAME_WD_CNT_RST	RW	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the FRAME_WD_CNT_RST. 1h (W) = The frame watchdog counter will be reset to 0.

3.9.13 CONTROLSS_FSI_RX0_RX_FRAME_WD_REF Register (Offset = 24h) [reset = h]

Short Description: Receive frame watchdog counter reference

Long Description:

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Table 3-890. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0024h
CONTROLSS_FSI_RX1	5029 1024h
CONTROLSS_FSI_RX2	502B 0024h
CONTROLSS_FSI_RX3	502B 1024h

Figure 3-428. CONTROLSS_FSI_RX0_RX_FRAME_WD_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAME_WD_REF															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_REF															
RW															
0															

Access Types Legend

Table 3-891. RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRAME_WD_REF	RW	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached.

3.9.14 CONTROLSS_FSI_RX0_RX_FRAME_WD_CNT Register (Offset = 28h) [reset = h]

Short Description: Receive frame watchdog current count

Long Description:

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Table 3-892. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0028h
CONTROLSS_FSI_RX1	5029 1028h
CONTROLSS_FSI_RX2	502B 0028h
CONTROLSS_FSI_RX3	502B 1028h

Figure 3-429. CONTROLSS_FSI_RX0_RX_FRAME_WD_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAME_WD_CNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_CNT															
RO															
0															

Access Types Legend

Table 3-893. RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRAME_WD_CNT	RO	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame.

3.9.15 CONTROLSS_FSI_RX0_RX_PING_WD_CTRL Register (Offset = 2Ch) [reset = h]

Short Description: Receive ping watchdog control register

Long Description:

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Table 3-894. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 002Ch
CONTROLSS_FSI_RX1	5029 102Ch
CONTROLSS_FSI_RX2	502B 002Ch
CONTROLSS_FSI_RX3	502B 102Ch

Figure 3-430. CONTROLSS_FSI_RX0_RX_PING_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED						PING_WD_EN	PING_WD_RST
RO						RW	RW
0						0	0

Access Types Legend

Table 3-895. RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	PING_WD_EN	RW	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter (RX_PING_WD_CNT) will begin counting from 0 when it is enabled. When the reference value (RX_PING_WD_REF) is reached, it will generate a ping watchdog timeout event (RX_EVT_STS.PING_WD_TO) and the counter value will reset to 0, and resume counting 0h (R/W) = The ping watchdog counter is disabled and not running. 1h (R/W) = The ping watchdog counter logic is enabled and running.
0	PING_WD_RST	RW	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the PING_WD_RST. 1h (W) = The ping watchdog counter will be reset to 0.

3.9.16 CONTROLSS_FSI_RX0_RX_PING_TAG Register (Offset = 2Eh) [reset = h]

Short Description: Receive ping tag register

Long Description:

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Table 3-896. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 002Eh
CONTROLSS_FSI_RX1	5029 102Eh
CONTROLSS_FSI_RX2	502B 002Eh
CONTROLSS_FSI_RX3	502B 102Eh

Figure 3-431. CONTROLSS_FSI_RX0_RX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			PING_TAG				RESERVED
RO			RO				RO
0			0				0

Access Types Legend

Table 3-897. RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4 - 1	PING_TAG	RO	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	RESERVED	RO		Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register (bits 4:0), application software can directly index into an array of 32-bit data.

3.9.17 CONTROLSS_FSI_RX0_RX_PING_WD_REF Register (Offset = 30h) [reset = h]

Short Description: Receive ping watchdog counter reference

Long Description:

Return to Summary Table

Table 3-898. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0030h
CONTROLSS_FSI_RX1	5029 1030h
CONTROLSS_FSI_RX2	502B 0030h
CONTROLSS_FSI_RX3	502B 1030h

Figure 3-432. CONTROLSS_FSI_RX0_RX_PING_WD_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PING_WD_REF															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_REF															
RW															
0															

Access Types Legend

Table 3-899. RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PING_WD_REF	RW	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached.

3.9.18 CONTROLSS_FSI_RX0_RX_PING_WD_CNT Register (Offset = 34h) [reset = h]

Short Description: Receive pingwatchdog current count

Long Description:

Return to Summary Table

Table 3-900. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0034h
CONTROLSS_FSI_RX1	5029 1034h
CONTROLSS_FSI_RX2	502B 0034h
CONTROLSS_FSI_RX3	502B 1034h

Figure 3-433. CONTROLSS_FSI_RX0_RX_PING_WD_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PING_WD_CNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_CNT															
RO															
0															

Access Types Legend

Table 3-901. RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PING_WD_CNT	RO	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame.

3.9.19 CONTROLSS_FSI_RX0_RX_INT1_CTRL_ALT1_ Register (Offset = 38h) [reset = h]

Short Description: Receive interrupt control register for RX_INT1

Long Description:

Return to Summary Table

Table 3-902. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0038h
CONTROLSS_FSI_RX1	5029 1038h
CONTROLSS_FSI_RX2	502B 0038h
CONTROLSS_FSI_RX3	502B 1038h

Figure 3-434. CONTROLSS_FSI_RX0_RX_INT1_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED	INT1_EN_ERROR_TAG_MATCH	INT1_EN_DATA_TAG_MATCH	INT1_EN_PING_TAG_MATCH	INT1_EN_DATA_FRAME	INT1_EN_FRAME_OVERRUN	INT1_EN_PING_FRAME	INT1_EN_ERR_FRAME
RO	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
INT1_EN_UNDERRUN	INT1_EN_FRAME_DONE	INT1_EN_OVERRUN	INT1_EN_EOF_ERR	INT1_EN_TYPE_ERR	INT1_EN_CRC_ERR	INT1_EN_FRAME_WD_TO	INT1_EN_PING_WD_TO
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-903. RX_INT1_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT1_EN_ERROR_TAG_MATCH	RW	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT1_EN_DATA_TAG_MATCH	RW	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT1_EN_PING_TAG_MATCH	RW	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT1_EN_DATA_FRAME	RW	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

Table 3-903. RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT1_EN_FRAME_OVERRUN	RW	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT1_EN_PING_FRAME	RW	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
8	INT1_EN_ERR_FRAME	RW	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT1_EN_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT1_EN_FRAME_DONE	RW	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT1_EN_OVERRUN	RW	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT1_EN_EOF_ERR	RW	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT1_EN_TYPE_ERR	RW	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT1_EN_CRC_ERR	RW	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
1	INT1_EN_FRAME_WD_TO	RW	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

Table 3-903. RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT1_EN_PING_WD_TO	RW	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

3.9.20 CONTROLSS_FSI_RX0_RX_INT2_CTRL_ALT1_ Register (Offset = 3Ah) [reset = h]

Short Description: Receive interrupt control register for RX_INT2

Long Description:

Return to Summary Table

Table 3-904. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 003Ah
CONTROLSS_FSI_RX1	5029 103Ah
CONTROLSS_FSI_RX2	502B 003Ah
CONTROLSS_FSI_RX3	502B 103Ah

Figure 3-435. CONTROLSS_FSI_RX0_RX_INT2_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED	INT2_EN_ERROR_TAG_MATCH	INT2_EN_DATA_TAG_MATCH	INT2_EN_PING_TAG_MATCH	INT2_EN_DATA_FRAME	INT2_EN_FRAME_OVERRUN	INT2_EN_PING_FRAME	INT2_EN_ERR_FRAME
RO	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
INT2_EN_UNDERRUN	INT2_EN_FRAME_DONE	INT2_EN_OVERRUN	INT2_EN_EOF_ERR	INT2_EN_TYPE_ERR	INT2_EN_CRC_ERR	INT2_EN_FRAME_WD_TO	INT2_EN_PING_WD_TO
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-905. RX_INT2_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT2_EN_ERROR_TAG_MATCH	RW	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT2_EN_DATA_TAG_MATCH	RW	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT2_EN_PING_TAG_MATCH	RW	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT2_EN_DATA_FRAME	RW	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

Table 3-905. RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT2_EN_FRAME_OVERRUN	RW	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT2_EN_PING_FRAME	RW	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
8	INT2_EN_ERR_FRAME	RW	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT2_EN_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT2_EN_FRAME_DONE	RW	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT2_EN_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT2_EN_EOF_ERR	RW	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT2_EN_TYPE_ERR	RW	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT2_EN_CRC_ERR	RW	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
1	INT2_EN_FRAME_WD_TO	RW	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

Table 3-905. RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT2_EN_PING_WD_TO	RW	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

3.9.21 CONTROLSS_FSI_RX0_RX_LOCK_CTRL Register (Offset = 3Ch) [reset = h]

Short Description: Receive lock control register

Long Description:

Return to Summary Table

Table 3-906. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 003Ch
CONTROLSS_FSI_RX1	5029 103Ch
CONTROLSS_FSI_RX2	502B 003Ch
CONTROLSS_FSI_RX3	502B 103Ch

Figure 3-436. CONTROLSS_FSI_RX0_RX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
WO							
0							
7	6	5	4	3	2	1	0
RESERVED							LOCK
RO							RW
0							0

Access Types Legend

Table 3-907. RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 1	RESERVED	RO		Reserved
0	LOCK	RW	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h (R/W) = Receive control registers can be modified and are not locked. 1h (R/W) = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

3.9.22 CONTROLSS_FSI_RX0_RX_ECC_DATA Register (Offset = 40h) [reset = h]

Short Description: Receive ECC data register

Long Description:

Return to Summary Table

Table 3-908. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0040h
CONTROLSS_FSI_RX1	5029 1040h
CONTROLSS_FSI_RX2	502B 0040h
CONTROLSS_FSI_RX3	502B 1040h

Figure 3-437. CONTROLSS_FSI_RX0_RX_ECC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA_HIGH															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_LOW															
RW															
0															

Access Types Legend

Table 3-909. RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA_HIGH	RW	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15 - 0	DATA_LOW	RW	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

3.9.23 CONTROLSS_FSI_RX0_RX_ECC_VAL Register (Offset = 44h) [reset = h]

Short Description: Receive ECC value register

Long Description:

Return to Summary Table

Table 3-910. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0044h
CONTROLSS_FSI_RX1	5029 1044h
CONTROLSS_FSI_RX2	502B 0044h
CONTROLSS_FSI_RX3	502B 1044h

Figure 3-438. CONTROLSS_FSI_RX0_RX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	ECC_VAL						
RO	RW						
0	0						

Access Types Legend

Table 3-911. RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	RO		Reserved
6 - 0	ECC_VAL	RW	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register.

3.9.24 CONTROLSS_FSI_RX0_RX_ECC_SEC_DATA Register (Offset = 48h) [reset = h]

Short Description: Receive ECC corrected data register

Long Description:

Return to Summary Table

Table 3-912. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0048h
CONTROLSS_FSI_RX1	5029 1048h
CONTROLSS_FSI_RX2	502B 0048h
CONTROLSS_FSI_RX3	502B 1048h

Figure 3-439. CONTROLSS_FSI_RX0_RX_ECC_SEC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEC_DATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEC_DATA															
RO															
0															

Access Types Legend

Table 3-913. RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEC_DATA	RO	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used.

3.9.25 CONTROLSS_FSI_RX0_RX_ECC_LOG Register (Offset = 4Ch) [reset = h]

Short Description: Receive ECC log and status register

Long Description:

Return to Summary Table

Table 3-914. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 004Ch
CONTROLSS_FSI_RX1	5029 104Ch
CONTROLSS_FSI_RX2	502B 004Ch
CONTROLSS_FSI_RX3	502B 104Ch

Figure 3-440. CONTROLSS_FSI_RX0_RX_ECC_LOG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED						MBE	SBE
RO						RO	RO
0						1	1

Access Types Legend

Table 3-915. RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	MBE	RO	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h (R) Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h (R) Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used.
0	SBE	RO	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h (R) No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h (R) A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA.

3.9.26 CONTROLSS_FSI_RX0_RX_FRAME_TAG_CMP Register (Offset = 50h) [reset = h]

Short Description: Receive frame tag compare register

Long Description:

Return to Summary Table

Table 3-916. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0050h
CONTROLSS_FSI_RX1	5029 1050h
CONTROLSS_FSI_RX2	502B 0050h
CONTROLSS_FSI_RX3	502B 1050h

Figure 3-441. CONTROLSS_FSI_RX0_RX_FRAME_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED						BROADCAST_EN	CMP_EN
RO						RW	RW
0						0	0
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
RW				RW			
0				0			

Access Types Legend

Table 3-917. RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	BROADCAST_EN	RW	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled.
8	CMP_EN	RW	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h (R/W) Frame tag comparison is disabled. 1h (R/W) Frame tag comparison is enabled.
7 - 4	TAG_MASK	RW	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames.
3 - 0	TAG_REF	RW	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames.

3.9.27 CONTROLSS_FSI_RX0_RX_PING_TAG_CMP Register (Offset = 52h) [reset = h]

Short Description: Receive ping tag compare register

Long Description:

Return to Summary Table

Table 3-918. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0052h
CONTROLSS_FSI_RX1	5029 1052h
CONTROLSS_FSI_RX2	502B 0052h
CONTROLSS_FSI_RX3	502B 1052h

Figure 3-442. CONTROLSS_FSI_RX0_RX_PING_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED						BROADCAST_EN	CMP_EN
RO						RW	RW
0						0	0
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
RW				RW			
0				0			

Access Types Legend

Table 3-919. RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	BROADCAST_EN	RW	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled.
8	CMP_EN	RW	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h (R/W) Ping tag comparison is disabled. 1h (R/W) Ping tag comparison is enabled.
7 - 4	TAG_MASK	RW	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames.
3 - 0	TAG_REF	RW	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames.

3.9.28 CONTROLSS_FSI_RX0_RX_TRIG_CTRL_0 Register (Offset = 58h) [reset = h]

Short Description: Receive Trigger Control register 0

Long Description:

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Table 3-920. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0058h
CONTROLSS_FSI_RX1	5029 1058h
CONTROLSS_FSI_RX2	502B 0058h
CONTROLSS_FSI_RX3	502B 1058h

Figure 3-443. CONTROLSS_FSI_RX0_RX_TRIG_CTRL_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED			TRIG_SEL				TRIG_EN
RW								RO			RW				RW
0								0			0				0

Access Types Legend

Table 3-921. RX_TRIG_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

3.9.29 CONTROLSS_FSI_RX0_RX_TRIG_WIDTH_0 Register (Offset = 5Ch) [reset = h]

Short Description: Receive Trigger Wdith register 0

Long Description:

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Table 3-922. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 005Ch
CONTROLSS_FSI_RX1	5029 105Ch
CONTROLSS_FSI_RX2	502B 005Ch
CONTROLSS_FSI_RX3	502B 105Ch

Figure 3-444. CONTROLSS_FSI_RX0_RX_TRIG_WIDTH_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_WIDTH															
RW															
0															

Access Types Legend

Table 3-923. RX_TRIG_WIDTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		Reserved
15 - 0	RX_TRIG_WIDTH	RW	0h	This register decides the width(in SYSCLK cycles) of wide pulse output of the RX trigger module.

3.9.30 CONTROLSS_FSI_RX0_RX_DLYLINE_CTRL Register (Offset = 60h) [reset = h]

Short Description: Receive delay line control register

Long Description:

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Table 3-924. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0060h
CONTROLSS_FSI_RX1	5029 1060h
CONTROLSS_FSI_RX2	502B 0060h
CONTROLSS_FSI_RX3	502B 1060h

Figure 3-445. CONTROLSS_FSI_RX0_RX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED	RXD1_DLY					RXD0_DLY	
RO	RW					RW	
0	0					0	
7	6	5	4	3	2	1	0
RXD0_DLY			RXCLK_DLY				
RW			RW				
0			0				

Access Types Legend

Table 3-925. RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14 - 10	RXD1_DLY	RW	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD1 path. 2h (R/W) Two delay elements are included in the RXD1 path. ... 1Fh (R/W) 31 delay elements are included in the RXD1 path, the maximum.
9 - 5	RXD0_DLY	RW	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD0 path. 2h (R/W) Two delay elements are included in the RXD0 path. ... 1Fh (R/W) 31 delay elements are included in the RXD0 path, the maximum.
4 - 0	RXCLK_DLY	RW	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the RXCLK path. 2h (R/W) Two delay elements are included in the RXCLK path. ... 1Fh (R/W) 31 delay elements are included in the RXCLK path, the maximum.

3.9.31 CONTROLSS_FSI_RX0_RX_TRIG_CTRL_1 Register (Offset = 64h) [reset = h]

Short Description: Receive Trigger Control register 1

Long Description:

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Table 3-926. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0064h
CONTROLSS_FSI_RX1	5029 1064h
CONTROLSS_FSI_RX2	502B 0064h
CONTROLSS_FSI_RX3	502B 1064h

Figure 3-446. CONTROLSS_FSI_RX0_RX_TRIG_CTRL_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED			TRIG_SEL				TRIG_EN
RW								RO			RW				RW
0								0			0				0

Access Types Legend

Table 3-927. RX_TRIG_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

3.9.32 CONTROLSS_FSI_RX0_RX_TRIG_CTRL_2 Register (Offset = 68h) [reset = h]

Short Description: Receive Trigger Control register 2

Long Description:

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Table 3-928. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0068h
CONTROLSS_FSI_RX1	5029 1068h
CONTROLSS_FSI_RX2	502B 0068h
CONTROLSS_FSI_RX3	502B 1068h

Figure 3-447. CONTROLSS_FSI_RX0_RX_TRIG_CTRL_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED			TRIG_SEL				TRIG_EN
RW								RO			RW				RW
0								0			0				0

Access Types Legend

Table 3-929. RX_TRIG_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

3.9.33 CONTROLSS_FSI_RX0_RX_TRIG_CTRL_3 Register (Offset = 6Ch) [reset = h]

Short Description: Receive Trigger Control register 3

Long Description:

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Table 3-930. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 006Ch
CONTROLSS_FSI_RX1	5029 106Ch
CONTROLSS_FSI_RX2	502B 006Ch
CONTROLSS_FSI_RX3	502B 106Ch

Figure 3-448. CONTROLSS_FSI_RX0_RX_TRIG_CTRL_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_TRIG_DLY															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_TRIG_DLY								RESERVED			TRIG_SEL				TRIG_EN
RW								RO			RW				RW
0								0			0				0

Access Types Legend

Table 3-931. RX_TRIG_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

3.9.34 CONTROLSS_FSI_RX0_RX_VIS_1 Register (Offset = 70h) [reset = h]

Short Description: Receive debug visibility register 1

Long Description:

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Table 3-932. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0070h
CONTROLSS_FSI_RX1	5029 1070h
CONTROLSS_FSI_RX2	502B 0070h
CONTROLSS_FSI_RX3	502B 1070h

Figure 3-449. CONTROLSS_FSI_RX0_RX_VIS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RX_CORE_STS	RESERVED		
RO												RO	RO		
0												0	0		

Access Types Legend

Table 3-933. RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RESERVED	RO		Reserved
3	RX_CORE_STS	RO	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h (R) The receiver core is operating normally. 1h (R) The receiver core has entered into an error state and should be reset.
2 - 0	RESERVED	RO		Reserved

3.9.35 CONTROLSS_FSI_RX0_RX_UDATA_FILTER Register (Offset = 74h) [reset = h]

Short Description: Receive User Data Filter Control register

Long Description:

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Table 3-934. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0074h
CONTROLSS_FSI_RX1	5029 1074h
CONTROLSS_FSI_RX2	502B 0074h
CONTROLSS_FSI_RX3	502B 1074h

Figure 3-450. CONTROLSS_FSI_RX0_RX_UDATA_FILTER Name Register

15	14	13	12	11	10	9	8
UDATA_MASK							
RW							
0							
7	6	5	4	3	2	1	0
UDATA_REG							
RW							
0							

Access Types Legend

Table 3-935. RX_UDATA_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	UDATA_MASK	RW	0h	Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position.
7 - 0	UDATA_REG	RW	0h	Reference to be used for comparing the USERDATA field when filtering is enabled.

3.9.36 CONTROLSS_FSI_RX0_RX_BUF_BASE Register (Offset = 80h) [reset = h]

Short Description: Base address for receive data buffer

Long Description:

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Table 3-936. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0080h
CONTROLSS_FSI_RX1	5029 1080h
CONTROLSS_FSI_RX2	502B 0080h
CONTROLSS_FSI_RX3	502B 1080h

Figure 3-451. CONTROLSS_FSI_RX0_RX_BUF_BASE Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
RO							
0							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
RO							
0							

Access Types Legend

Table 3-937. RX_BUF_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BASE_ADDRESS	RO	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver.

Table 3-938. Access Type Codes

Access Type	Code	Description
WO	WO	Undefined
RO	RO	Undefined
RW	RW	Undefined

3.10 C2K_FSI_TX Registers

Table 3-939. CONTROLSS_FSI0_TX0, CONTROLSS_FSI_TX0_CONTROLSS_FSI_TX Registers, Base Address=5028 0000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_FSI_TX0 Physical Address	CONTROLSS_FSI_TX1 Physical Address	CONTROLSS_FSI_TX2 Physical Address
0h	16	CONTROLSS_FSI_TX0_TX_MASTER_CTRL	Transmit master control register	5028 0000h	5028 1000h	502A 0000h
4h	16	CONTROLSS_FSI_TX0_TX_CLK_CTRL	Transmit clock control register	5028 0004h	5028 1004h	502A 0004h
8h	16	CONTROLSS_FSI_TX0_TX_OPER_CTRL_LO_ALT2_	Transmit operation control register low	5028 0008h	5028 1008h	502A 0008h
Ah	16	CONTROLSS_FSI_TX0_TX_OPER_CTRL_HI_ALT1_	Transmit operation control register high	5028 000Ah	5028 100Ah	502A 000Ah
Ch	16	CONTROLSS_FSI_TX0_TX_FRAME_CTRL	Transmit frame control register	5028 000Ch	5028 100Ch	502A 000Ch
Eh	16	CONTROLSS_FSI_TX0_TX_FRAME_TAG_UDATA	Transmit frame tag and user data register	5028 000Eh	5028 100Eh	502A 000Eh
10h	16	CONTROLSS_FSI_TX0_TX_BUF_PTR_LOAD	Transmit buffer pointer control load register	5028 0010h	5028 1010h	502A 0010h
12h	16	CONTROLSS_FSI_TX0_TX_BUF_PTR_STS	Transmit buffer pointer control status register	5028 0012h	5028 1012h	502A 0012h
14h	16	CONTROLSS_FSI_TX0_TX_PING_CTRL_ALT1_	Transmit ping control register	5028 0014h	5028 1014h	502A 0014h
16h	16	CONTROLSS_FSI_TX0_TX_PING_TAG	Transmit ping tag register	5028 0016h	5028 1016h	502A 0016h
18h	32	CONTROLSS_FSI_TX0_TX_PING_TO_REF	Transmit ping timeout counter reference	5028 0018h	5028 1018h	502A 0018h
1Ch	32	CONTROLSS_FSI_TX0_TX_PING_TO_CNT	Transmit ping timeout current count	5028 001Ch	5028 101Ch	502A 001Ch
20h	16	CONTROLSS_FSI_TX0_TX_INT_CTRL	Transmit interrupt event control register	5028 0020h	5028 1020h	502A 0020h
22h	16	CONTROLSS_FSI_TX0_TX_DMA_CTRL	Transmit DMA event control register	5028 0022h	5028 1022h	502A 0022h
24h	16	CONTROLSS_FSI_TX0_TX_LOCK_CTRL	Transmit lock control register	5028 0024h	5028 1024h	502A 0024h
28h	16	CONTROLSS_FSI_TX0_TX_EVT_STS	Transmit event and error status flag register	5028 0028h	5028 1028h	502A 0028h
2Ch	16	CONTROLSS_FSI_TX0_TX_EVT_CLR	Transmit event and error clear register	5028 002Ch	5028 102Ch	502A 002Ch
2Eh	16	CONTROLSS_FSI_TX0_TX_EVT_FRC	Transmit event and error flag force register	5028 002Eh	5028 102Eh	502A 002Eh
30h	16	CONTROLSS_FSI_TX0_TX_USER_CRC	Transmit user-defined CRC register	5028 0030h	5028 1030h	502A 0030h
40h	32	CONTROLSS_FSI_TX0_TX_ECC_DATA	Transmit ECC data register	5028 0040h	5028 1040h	502A 0040h

Table 3-939. CONTROLSS_FSI0_TX0, CONTROLSS_FSI_TX0_CONTROLSS_FSI_TX Registers, Base Address=5028 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_FSI_TX0 Physical Address	CONTROLSS_FSI_TX1 Physical Address	CONTROLSS_FSI_TX2 Physical Address
44h	16	CONTROLSS_FSI_TX0_TX_ECC_VAL	Transmit ECC value register	5028 0044h	5028 1044h	502A 0044h
48h	16	CONTROLSS_FSI_TX0_TX_DLYLINE_CTRL	Transmit delay Line control register	5028 0048h	5028 1048h	502A 0048h
80h	16	CONTROLSS_FSI_TX0_TX_BUF_BASE	Base address for transmit buffer	5028 0080h	5028 1080h	502A 0080h

3.10.1 CONTROLSS_FSI_TX0_TX_MASTER_CTRL Register (Offset = 0h) [reset = h]

Short Description: Transmit master control register

Long Description:

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Table 3-940. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0000h
CONTROLSS_FSI_TX1	5028 1000h
CONTROLSS_FSI_TX2	502A 0000h
CONTROLSS_FSI_TX3	502A 1000h

Figure 3-452. CONTROLSS_FSI_TX0_TX_MASTER_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
WO							
0							
7	6	5	4	3	2	1	0
RESERVED						FLUSH	CORE_RST
RO						RW	RW
0						0	0

Access Types Legend

Table 3-941. TX_MASTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 2	RESERVED	RO		Reserved
1	FLUSH	RW	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h (R/W) = Clear this bit. 1h (R/W) = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0.
0	CORE_RST	RW	0h	Transmitter Master Core Reset bit This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared. 0h (R/W) = Transmitter core is not in reset and can transmit frames. 1h (R/W) = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

3.10.2 CONTROLSS_FSI_TX0_TX_CLK_CTRL Register (Offset = 4h) [reset = h]

Short Description: Transmit clock control register

Long Description:

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Table 3-942. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0004h
CONTROLSS_FSI_TX1	5028 1004h
CONTROLSS_FSI_TX2	502A 0004h
CONTROLSS_FSI_TX3	502A 1004h

Figure 3-453. CONTROLSS_FSI_TX0_TX_CLK_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED						PRESCALE_VAL	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
PRESCALE_VAL						CLK_EN	CLK_RST
RW						RW	RW
0						0	0

Access Types Legend

Table 3-943. TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 2	PRESCALE_VAL	RW	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h (R/W) = Reserved 1h (R/W) = Input clock /1 2h (R/W) = Input clock /2 3h (R/W) = Input clock /3 4h (R/W) = Input clock /4 ... FFh (R/W) = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN
1	CLK_EN	RW	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h (R/W) = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h (R/W) = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled.
0	CLK_RST	RW	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h (R/W) = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h (R/W) = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit.

3.10.3 CONTROLSS_FSI_TX0_TX_OPER_CTRL_LO_ALT2_ Register (Offset = 8h) [reset = h]

Short Description: Transmit operation control register low

Long Description:

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Table 3-944. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0008h
CONTROLSS_FSI_TX1	5028 1008h
CONTROLSS_FSI_TX2	502A 0008h
CONTROLSS_FSI_TX3	502A 1008h

Figure 3-454. CONTROLSS_FSI_TX0_TX_OPER_CTRL_LO_ALT2_ Name Register

15	14	13	12	11	10	9	8
RESERVED					SEL_TDM_IN	TDM_ENABLE	SEL_PLLCLK
RO					RW	RW	RW
0					0	0	0
7	6	5	4	3	2	1	0
PING_TO_MODE	SW_CRC	START_MODE			SPI_MODE	DATA_WIDTH	
RW	RW	RW			RW	RW	
0	0	0			0	0	

Access Types Legend

Table 3-945. TX_OPER_CTRL_LO_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	SEL_TDM_IN	RW	0h	Input TDM port Select bit This bit selects the input port for the transmitter core between the TDM input pins or the RX module. When this bit is '0', the inputs selected for TDM are from the TDM input pins. When this bit is '1', then inputs selected for TDM are from the RX module.
9	TDM_ENABLE	RW	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-slave TDM operation. 0h (R/W) Transmit TDM Mode is not enabled. 1h (R/W) Transmit TDM Mode is enabled.
8	SEL_PLLCLK	RW	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h (R/W) = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h (R/W) = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler.
7	PING_TO_MODE	RW	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h (R/W) = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h (R/W) = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout
6	SW_CRC	RW	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h (R/W) = The transmitted CRC value is computed by hardware. 1h (R/W) = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register.
5 - 3	START_MODE	RW	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h (R/W) = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h (R/W) = The configured external trigger will initiate a new transmission. 2h (R/W) = Either writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use.

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Table 3-945. TX_OPER_CTRL_LO_ALT2_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SPI_MODE	RW	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode.
1 - 0	DATA_WIDTH	RW	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h (R/W) = Data will be transmitted on one data line (TXD0) 1h (R/W) = Data will be transmitted on two data lines (TXD0 and TXD1). The format of the data is described in the preceeding chapter. 2h, 3h (R/W) = Reserved

3.10.4 CONTROLSS_FSI_TX0_TX_OPER_CTRL_HI_ALT1_ Register (Offset = Ah) [reset = h]

Short Description: Transmit operation control register high

Long Description:

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Table 3-946. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Ah
CONTROLSS_FSI_TX1	5028 100Ah
CONTROLSS_FSI_TX2	502A 000Ah
CONTROLSS_FSI_TX3	502A 100Ah

Figure 3-455. CONTROLSS_FSI_TX0_TX_OPER_CTRL_HI_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED			EXT_TRIG_SEL				
RO			RW				
0			0				
7	6	5	4	3	2	1	0
EXT_TRIG_SEL	ECC_SEL	FORCE_ERR	RESERVED				
RW	RW	RW	RO				
0	0	0	0				

Access Types Legend

Table 3-947. TX_OPER_CTRL_HI_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 7	EXT_TRIG_SEL	RW	0h	External Trigger Select bit These bits define which of the 64 external inputs will be used as the source for the external input trigger. 00h (R/W) = Trigger 1 is the source. 01h (R/W) = Trigger 2 is the source. 02h (R/W) = Trigger 3 is the source. ... 3Fh (R/W) = Trigger 64 is the source.
6	ECC_SEL	RW	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used.
5	FORCE_ERR	RW	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode (FSI Transmit). 0h (R/W) = The CRC will not be forced to 0. 1h (R/W) = The CRC will be forced to 0 in a buffer overrun or underrun condition.
4 - 0	RESERVED	RO		Reserved

3.10.5 CONTROLSS_FSI_TX0_TX_FRAME_CTRL Register (Offset = Ch) [reset = h]

Short Description: Transmit frame control register

Long Description:

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Table 3-948. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Ch
CONTROLSS_FSI_TX1	5028 100Ch
CONTROLSS_FSI_TX2	502A 000Ch
CONTROLSS_FSI_TX3	502A 100Ch

Figure 3-456. CONTROLSS_FSI_TX0_TX_FRAME_CTRL Name Register

15	14	13	12	11	10	9	8
START	RESERVED						
RW	RO						
0	0						
7	6	5	4	3	2	1	0
N_WORDS				FRAME_TYPE			
RW				RW			
0				0			

Access Types Legend

Table 3-949. TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	RW	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Start the next transmission. This bit will be cleared by hardware.
14 - 8	RESERVED	RO		Reserved
7 - 4	N_WORDS	RW	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data).
3 - 0	FRAME_TYPE	RW	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b (R/W) = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b (R/W) = DATA_1_WORD Frame. One word data frame (16-bit data). 0101b (R/W) = DATA_2_WORD Frame. Two word data frame (32-bit data). 0110b (R/W) = DATA_4_WORD Frame. Four word data frame (64-bit data). 0111b (R/W) = DATA_6_WORD Frame. Six word data frame (96-bit data). 0011b (R/W) = DATA_N_WORD Frame. The N_WORDS field will determine the number of words (1 to 16) to be sent. Both the transmitter and receiver must have the same value programmed. 1111b (R/W) = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used.

3.10.6 CONTROLSS_FSI_TX0_TX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = h]

Short Description: Transmit frame tag and user data register

Long Description:

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Table 3-950. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Eh
CONTROLSS_FSI_TX1	5028 100Eh
CONTROLSS_FSI_TX2	502A 000Eh
CONTROLSS_FSI_TX3	502A 100Eh

Figure 3-457. CONTROLSS_FSI_TX0_TX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
RW							
0							
7	6	5	4	3	2	1	0
RESERVED				FRAME_TAG			
RO				RW			
0				0			

Access Types Legend

Table 3-951. TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	USER_DATA	RW	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior.
7 - 4	RESERVED	RO		Reserved
3 - 0	FRAME_TAG	RW	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead.

3.10.7 CONTROLSS_FSI_TX0_TX_BUF_PTR_LOAD Register (Offset = 10h) [reset = h]

Short Description: Transmit buffer pointer control load register

Long Description:

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Table 3-952. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0010h
CONTROLSS_FSI_TX1	5028 1010h
CONTROLSS_FSI_TX2	502A 0010h
CONTROLSS_FSI_TX3	502A 1010h

Figure 3-458. CONTROLSS_FSI_TX0_TX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				BUF_PTR_LOAD			
RO				RW			
0				0			

Access Types Legend

Table 3-953. TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	BUF_PTR_LOAD	RW	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior.

3.10.8 CONTROLSS_FSI_TX0_TX_BUF_PTR_STS Register (Offset = 12h) [reset = h]

Short Description: Transmit buffer pointer control status register

Long Description:

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Table 3-954. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0012h
CONTROLSS_FSI_TX1	5028 1012h
CONTROLSS_FSI_TX2	502A 0012h
CONTROLSS_FSI_TX3	502A 1012h

Figure 3-459. CONTROLSS_FSI_TX0_TX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED			CURR_WORD_CNT				
RO			RO				
0			0				
7	6	5	4	3	2	1	0
RESERVED				CURR_BUF_PTR			
RO				RO			
0				0			

Access Types Legend

Table 3-955. TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 8	CURR_WORD_CNT	RO	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition.
7 - 4	RESERVED	RO		Reserved
3 - 0	CURR_BUF_PTR	RO	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

3.10.9 CONTROLSS_FSI_TX0_TX_PING_CTRL_ALT1_ Register (Offset = 14h) [reset = h]

Short Description: Transmit ping control register

Long Description:

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Table 3-956. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0014h
CONTROLSS_FSI_TX1	5028 1014h
CONTROLSS_FSI_TX2	502A 0014h
CONTROLSS_FSI_TX3	502A 1014h

Figure 3-460. CONTROLSS_FSI_TX0_TX_PING_CTRL_ALT1_ Name Register

15	14	13	12	11	10	9	8
RESERVED							EXT_TRIG_SEL
RO							RW
0							0
7	6	5	4	3	2	1	0
EXT_TRIG_SEL					EXT_TRIG_EN	TIMER_EN	CNT_RST
RW					RW	RW	RW
0					0	0	0

Access Types Legend

Table 3-957. TX_PING_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8 - 3	EXT_TRIG_SEL	RW	0h	External Trigger Select bits This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h (R/W) = Trigger 1 will be used to generate a ping frame. 1h (R/W) = Trigger 2 will be used to generate a ping frame. .. 3Fh (R/W) = Trigger 64 will be used to generate a ping frame.
2	EXT_TRIG_EN	RW	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h (R/W) = External triggers will not be used to generate ping frames. 1h (R/W) = The selected external trigger (selected by EXT_TRIG_SEL bits) will be able to generate a ping frame. The ping timer will be ignored if this bit is set.
1	TIMER_EN	RW	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h (R/W) = The ping timer is disabled and will not generate ping frames. 1h (R/W) = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function.
0	CNT_RST	RW	0h	Ping Counter Reset bit Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter. 0h (R/W) = Clear the CNT_RST. 1h (R/W) = The ping counter will be reset to 0.

3.10.10 CONTROLSS_FSI_TX0_TX_PING_TAG Register (Offset = 16h) [reset = h]

Short Description: Transmit ping tag register

Long Description:

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Table 3-958. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0016h
CONTROLSS_FSI_TX1	5028 1016h
CONTROLSS_FSI_TX2	502A 0016h
CONTROLSS_FSI_TX3	502A 1016h

Figure 3-461. CONTROLSS_FSI_TX0_TX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				TAG			
RO				RW			
0				0			

Access Types Legend

Table 3-959. TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	TAG	RW	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value.

3.10.11 CONTROLSS_FSI_TX0_TX_PING_TO_REF Register (Offset = 18h) [reset = h]

Short Description: Transmit ping timeout counter reference

Long Description:

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Table 3-960. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0018h
CONTROLSS_FSI_TX1	5028 1018h
CONTROLSS_FSI_TX2	502A 0018h
CONTROLSS_FSI_TX3	502A 1018h

Figure 3-462. CONTROLSS_FSI_TX0_TX_PING_TO_REF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_REF															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_REF															
RW															
0															

Access Types Legend

Table 3-961. TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_REF	RW	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting.

3.10.12 CONTROLSS_FSI_TX0_TX_PING_TO_CNT Register (Offset = 1Ch) [reset = h]

Short Description: Transmit ping timeout current count

Long Description:

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Table 3-962. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 001Ch
CONTROLSS_FSI_TX1	5028 101Ch
CONTROLSS_FSI_TX2	502A 001Ch
CONTROLSS_FSI_TX3	502A 101Ch

Figure 3-463. CONTROLSS_FSI_TX0_TX_PING_TO_CNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_CNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_CNT															
RO															
0															

Access Types Legend

Table 3-963. TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_CNT	RO	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value (TX_PING_TO_REF), at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter

3.10.13 CONTROLSS_FSI_TX0_TX_INT_CTRL Register (Offset = 20h) [reset = h]

Short Description: Transmit interrupt event control register

Long Description:

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Table 3-964. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0020h
CONTROLSS_FSI_TX1	5028 1020h
CONTROLSS_FSI_TX2	502A 0020h
CONTROLSS_FSI_TX3	502A 1020h

Figure 3-464. CONTROLSS_FSI_TX0_TX_INT_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED				INT2_EN_PING_TO	INT2_EN_BUF_OVERRUN	INT2_EN_BUF_UNDERRUN	INT2_EN_FRAME_DONE
RO				RW	RW	RW	RW
0				0	0	0	0
7	6	5	4	3	2	1	0
RESERVED				INT1_EN_PING_TO	INT1_EN_BUF_OVERRUN	INT1_EN_BUF_UNDERRUN	INT1_EN_FRAME_DONE
RO				RW	RW	RW	RW
0				0	0	0	0

Access Types Legend

Table 3-965. TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11	INT2_EN_PING_TO	RW	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT2.
10	INT2_EN_BUF_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT2.
9	INT2_EN_BUF_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT2.
8	INT2_EN_FRAME_DONE	RW	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT2.
7 - 4	RESERVED	RO		Reserved
3	INT1_EN_PING_TO	RW	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT1.
2	INT1_EN_BUF_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT1.

Table 3-965. TX_INT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT1_EN_BUF_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT1.
0	INT1_EN_FRAME_DONE	RW	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT1.

3.10.14 CONTROLSS_FSI_TX0_TX_DMA_CTRL Register (Offset = 22h) [reset = h]

Short Description: Transmit DMA event control register

Long Description:

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Table 3-966. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0022h
CONTROLSS_FSI_TX1	5028 1022h
CONTROLSS_FSI_TX2	502A 0022h
CONTROLSS_FSI_TX3	502A 1022h

Figure 3-465. CONTROLSS_FSI_TX0_TX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED							DMA_EVT_EN
RO							RW
0							0

Access Types Legend

Table 3-967. TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DMA_EVT_EN	RW	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames.

3.10.15 CONTROLSS_FSI_TX0_TX_LOCK_CTRL Register (Offset = 24h) [reset = h]

Short Description: Transmit lock control register

Long Description:

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Table 3-968. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0024h
CONTROLSS_FSI_TX1	5028 1024h
CONTROLSS_FSI_TX2	502A 0024h
CONTROLSS_FSI_TX3	502A 1024h

Figure 3-466. CONTROLSS_FSI_TX0_TX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
WO							
0							
7	6	5	4	3	2	1	0
RESERVED							LOCK
RO							RW
0							0

Access Types Legend

Table 3-969. TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 1	RESERVED	RO		Reserved
0	LOCK	RW	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h (R/W) = Transmit control registers can be modified and are not locked. 1h (R/W) = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

3.10.16 CONTROLSS_FSI_TX0_TX_EVT_STS Register (Offset = 28h) [reset = h]

Short Description: Transmit event and error status flag register

Long Description:

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Table 3-970. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0028h
CONTROLSS_FSI_TX1	5028 1028h
CONTROLSS_FSI_TX2	502A 0028h
CONTROLSS_FSI_TX3	502A 1028h

Figure 3-467. CONTROLSS_FSI_TX0_TX_EVT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
RO				RO	RO	RO	RO
0				0	0	0	0

Access Types Legend

Table 3-971. TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	RO	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = A ping frame has not been triggered. 1h (R) = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
2	BUF_OVERRUN	RO	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Overrun has not occured. 1h (R) = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
1	BUF_UNDERRUN	RO	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Underrun has not occured. 1h (R) = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
0	FRAME_DONE	RO	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Frame Done condition has not occured. 1h (R) = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.

3.10.17 CONTROLSS_FSI_TX0_TX_EVT_CLR Register (Offset = 2Ch) [reset = h]

Short Description: Transmit event and error clear register

Long Description:

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Table 3-972. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 002Ch
CONTROLSS_FSI_TX1	5028 102Ch
CONTROLSS_FSI_TX2	502A 002Ch
CONTROLSS_FSI_TX3	502A 102Ch

Figure 3-468. CONTROLSS_FSI_TX0_TX_EVT_CLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
RO				WO	WO	WO	WO
0				0	0	0	0

Access Types Legend

Table 3-973. TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	WO	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event.
2	BUF_OVERRUN	WO	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
1	BUF_UNDERRUN	WO	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
0	FRAME_DONE	WO	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.

3.10.18 CONTROLSS_FSI_TX0_TX_EVT_FRC Register (Offset = 2Eh) [reset = h]

Short Description: Transmit event and error flag force register

Long Description:

Return to Summary Table

Table 3-974. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 002Eh
CONTROLSS_FSI_TX1	5028 102Eh
CONTROLSS_FSI_TX2	502A 002Eh
CONTROLSS_FSI_TX3	502A 102Eh

Figure 3-469. CONTROLSS_FSI_TX0_TX_EVT_FRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
RO				WO	WO	WO	WO
0				0	0	0	0

Access Types Legend

Table 3-975. TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	WO	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.
2	BUF_OVERRUN	WO	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Force the corresponding flag bit in the TX_EVT_STS Register.
1	BUF_UNDERRUN	WO	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.
0	FRAME_DONE	WO	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.

3.10.19 CONTROLSS_FSI_TX0_TX_USER_CRC Register (Offset = 30h) [reset = h]

Short Description: Transmit user-defined CRC register

Long Description:

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Table 3-976. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0030h
CONTROLSS_FSI_TX1	5028 1030h
CONTROLSS_FSI_TX2	502A 0030h
CONTROLSS_FSI_TX3	502A 1030h

Figure 3-470. CONTROLSS_FSI_TX0_TX_USER_CRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
USER_CRC							
RW							
0							

Access Types Legend

Table 3-977. TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7 - 0	USER_CRC	RW	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option (TX_OPER_CTRL_LO.SW_CRC = 1). This register is ignored if the hardware CRC generation is enabled.

3.10.20 CONTROLSS_FSI_TX0_TX_ECC_DATA Register (Offset = 40h) [reset = h]

Short Description: Transmit ECC data register

Long Description:

Return to Summary Table

Table 3-978. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0040h
CONTROLSS_FSI_TX1	5028 1040h
CONTROLSS_FSI_TX2	502A 0040h
CONTROLSS_FSI_TX3	502A 1040h

Figure 3-471. CONTROLSS_FSI_TX0_TX_ECC_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA_HIGH															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_LOW															
RW															
0															

Access Types Legend

Table 3-979. TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA_HIGH	RW	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15 - 0	DATA_LOW	RW	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

3.10.21 CONTROLSS_FSI_TX0_TX_ECC_VAL Register (Offset = 44h) [reset = h]

Short Description: Transmit ECC value register

Long Description:

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Table 3-980. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0044h
CONTROLSS_FSI_TX1	5028 1044h
CONTROLSS_FSI_TX2	502A 0044h
CONTROLSS_FSI_TX3	502A 1044h

Figure 3-472. CONTROLSS_FSI_TX0_TX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	ECC_VAL						
RO	RO						
0	1100						

Access Types Legend

Table 3-981. TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	RO		Reserved
6 - 0	ECC_VAL	RO	44Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register.

3.10.22 CONTROLSS_FSI_TX0_TX_DLYLINE_CTRL Register (Offset = 48h) [reset = h]

Short Description: Transmit delay Line control register

Long Description:

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Table 3-982. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0048h
CONTROLSS_FSI_TX1	5028 1048h
CONTROLSS_FSI_TX2	502A 0048h
CONTROLSS_FSI_TX3	502A 1048h

Figure 3-473. CONTROLSS_FSI_TX0_TX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED	TXD1_DLY					TXD0_DLY	
RO	RW					RW	
0	0					0	
7	6	5	4	3	2	1	0
TXD0_DLY			TXCLK_DLY				
RW			RW				
0			0				

Access Types Legend

Table 3-983. TX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14 - 10	TXD1_DLY	RW	0h	Delay Line Tap Select for TXD1 This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD1 path. 2h (R/W) Two delay elements are included in the TXD1 path. ... 1Fh (R/W) 31 delay elements are included in the TXD1 path, the maximum.
9 - 5	TXD0_DLY	RW	0h	Delay Line Tap Select for TXD0 This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD0 path. 2h (R/W) Two delay elements are included in the TXD0 path. ... 1Fh (R/W) 31 delay elements are included in the TXD0 path, the maximum.
4 - 0	TXCLK_DLY	RW	0h	Delay Line Tap Select for TXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the TXCLK path. 2h (R/W) Two delay elements are included in the TXCLK path. ... 1Fh (R/W) 31 delay elements are included in the TXCLK path, the maximum.

3.10.23 CONTROLSS_FSI_TX0_TX_BUF_BASE Register (Offset = 80h) [reset = h]

Short Description: Base address for transmit buffer

Long Description:

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Table 3-984. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0080h
CONTROLSS_FSI_TX1	5028 1080h
CONTROLSS_FSI_TX2	502A 0080h
CONTROLSS_FSI_TX3	502A 1080h

Figure 3-474. CONTROLSS_FSI_TX0_TX_BUF_BASE Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
RW							
0							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
RW							
0							

Access Types Legend

Table 3-985. TX_BUF_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BASE_ADDRESS	RW	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter.

Table 3-986. Access Type Codes

Access Type	Code	Description
WO	WO	Undefined
RO	RO	Undefined
RW	RW	Undefined

3.11 C2K_ICLXBAR Registers

Table 3-987. CONTROLSS_ICLXBAR, CONTROLSS_ICLXBAR_CONTROLSS_ICLXBAR Registers, Base Address=502D 4000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_ICLXBAR Physical Address
0h	32	CONTROLSS_ICLXBAR_PID	PID register	502D 4000h
100h	32	CONTROLSS_ICLXBAR_ICLXBAR0_G0	RW	502D 4100h
104h	32	CONTROLSS_ICLXBAR_ICLXBAR0_G1	RW	502D 4104h
108h	32	CONTROLSS_ICLXBAR_ICLXBAR0_G2	RW	502D 4108h
140h	32	CONTROLSS_ICLXBAR_ICLXBAR1_G0	RW	502D 4140h
144h	32	CONTROLSS_ICLXBAR_ICLXBAR1_G1	RW	502D 4144h
148h	32	CONTROLSS_ICLXBAR_ICLXBAR1_G2	RW	502D 4148h
180h	32	CONTROLSS_ICLXBAR_ICLXBAR2_G0	RW	502D 4180h
184h	32	CONTROLSS_ICLXBAR_ICLXBAR2_G1	RW	502D 4184h
188h	32	CONTROLSS_ICLXBAR_ICLXBAR2_G2	RW	502D 4188h
1C0h	32	CONTROLSS_ICLXBAR_ICLXBAR3_G0	RW	502D 41C0h
1C4h	32	CONTROLSS_ICLXBAR_ICLXBAR3_G1	RW	502D 41C4h
1C8h	32	CONTROLSS_ICLXBAR_ICLXBAR3_G2	RW	502D 41C8h
200h	32	CONTROLSS_ICLXBAR_ICLXBAR4_G0	RW	502D 4200h
204h	32	CONTROLSS_ICLXBAR_ICLXBAR4_G1	RW	502D 4204h
208h	32	CONTROLSS_ICLXBAR_ICLXBAR4_G2	RW	502D 4208h
240h	32	CONTROLSS_ICLXBAR_ICLXBAR5_G0	RW	502D 4240h
244h	32	CONTROLSS_ICLXBAR_ICLXBAR5_G1	RW	502D 4244h
248h	32	CONTROLSS_ICLXBAR_ICLXBAR5_G2	RW	502D 4248h
280h	32	CONTROLSS_ICLXBAR_ICLXBAR6_G0	RW	502D 4280h
284h	32	CONTROLSS_ICLXBAR_ICLXBAR6_G1	RW	502D 4284h
288h	32	CONTROLSS_ICLXBAR_ICLXBAR6_G2	RW	502D 4288h
2C0h	32	CONTROLSS_ICLXBAR_ICLXBAR7_G0	RW	502D 42C0h
2C4h	32	CONTROLSS_ICLXBAR_ICLXBAR7_G1	RW	502D 42C4h
2C8h	32	CONTROLSS_ICLXBAR_ICLXBAR7_G2	RW	502D 42C8h
300h	32	CONTROLSS_ICLXBAR_ICLXBAR8_G0	RW	502D 4300h
304h	32	CONTROLSS_ICLXBAR_ICLXBAR8_G1	RW	502D 4304h
308h	32	CONTROLSS_ICLXBAR_ICLXBAR8_G2	RW	502D 4308h
340h	32	CONTROLSS_ICLXBAR_ICLXBAR9_G0	RW	502D 4340h
344h	32	CONTROLSS_ICLXBAR_ICLXBAR9_G1	RW	502D 4344h
348h	32	CONTROLSS_ICLXBAR_ICLXBAR9_G2	RW	502D 4348h
380h	32	CONTROLSS_ICLXBAR_ICLXBAR10_G0	RW	502D 4380h
384h	32	CONTROLSS_ICLXBAR_ICLXBAR10_G1	RW	502D 4384h
388h	32	CONTROLSS_ICLXBAR_ICLXBAR10_G2	RW	502D 4388h
3C0h	32	CONTROLSS_ICLXBAR_ICLXBAR11_G0	RW	502D 43C0h
3C4h	32	CONTROLSS_ICLXBAR_ICLXBAR11_G1	RW	502D 43C4h
3C8h	32	CONTROLSS_ICLXBAR_ICLXBAR11_G2	RW	502D 43C8h

Table 3-987. CONTROLSS_ICLXBAR, CONTROLSS_ICLXBAR_CONTROLSS_ICLXBAR Registers, Base Address=502D 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_ICLXBAR Physical Address
400h	32	CONTROLSS_ICLXBAR_ICLXBAR12_G0	RW	502D 4400h
404h	32	CONTROLSS_ICLXBAR_ICLXBAR12_G1	RW	502D 4404h
408h	32	CONTROLSS_ICLXBAR_ICLXBAR12_G2	RW	502D 4408h
440h	32	CONTROLSS_ICLXBAR_ICLXBAR13_G0	RW	502D 4440h
444h	32	CONTROLSS_ICLXBAR_ICLXBAR13_G1	RW	502D 4444h
448h	32	CONTROLSS_ICLXBAR_ICLXBAR13_G2	RW	502D 4448h
480h	32	CONTROLSS_ICLXBAR_ICLXBAR14_G0	RW	502D 4480h
484h	32	CONTROLSS_ICLXBAR_ICLXBAR14_G1	RW	502D 4484h
488h	32	CONTROLSS_ICLXBAR_ICLXBAR14_G2	RW	502D 4488h
4C0h	32	CONTROLSS_ICLXBAR_ICLXBAR15_G0	RW	502D 44C0h
4C4h	32	CONTROLSS_ICLXBAR_ICLXBAR15_G1	RW	502D 44C4h
4C8h	32	CONTROLSS_ICLXBAR_ICLXBAR15_G2	RW	502D 44C8h

3.11.1 CONTROLSS_ICLXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-988. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4000h

Figure 3-475. CONTROLSS_ICLXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-989. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.11.2 CONTROLSS_ICLXBAR_ICLXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-990. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4100h

Figure 3-476. CONTROLSS_ICLXBAR_ICLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-991. ICLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.3 CONTROLSS_ICLXBAR_ICLXBAR0_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-992. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4104h

Figure 3-477. CONTROLSS_ICLXBAR_ICLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-993. ICLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.4 CONTROLSS_ICLXBAR_ICLXBAR0_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-994. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4108h

Figure 3-478. CONTROLSS_ICLXBAR_ICLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-995. ICLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.5 CONTROLSS_ICLXBAR_ICLXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-996. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4140h

Figure 3-479. CONTROLSS_ICLXBAR_ICLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-997. ICLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar1 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.6 CONTROLSS_ICLXBAR_ICLXBAR1_G1 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-998. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4144h

Figure 3-480. CONTROLSS_ICLXBAR_ICLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-999. ICLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar1 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.7 CONTROLSS_ICLXBAR_ICLXBAR1_G2 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1000. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4148h

Figure 3-481. CONTROLSS_ICLXBAR_ICLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1001. ICLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar1 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.8 CONTROLSS_ICLXBAR_ICLXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1002. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4180h

Figure 3-482. CONTROLSS_ICLXBAR_ICLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1003. ICLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar2 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.9 CONTROLSS_ICLXBAR_ICLXBAR2_G1 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1004. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4184h

Figure 3-483. CONTROLSS_ICLXBAR_ICLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1005. ICLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar2 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.10 CONTROLSS_ICLXBAR_ICLXBAR2_G2 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1006. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4188h

Figure 3-484. CONTROLSS_ICLXBAR_ICLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1007. ICLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar2 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.11 CONTROLSS_ICLXBAR_ICLXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1008. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C0h

Figure 3-485. CONTROLSS_ICLXBAR_ICLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1009. ICLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar3 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.12 CONTROLSS_ICLXBAR_ICLXBAR3_G1 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1010. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C4h

Figure 3-486. CONTROLSS_ICLXBAR_ICLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1011. ICLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar3 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.13 CONTROLSS_ICLXBAR_ICLXBAR3_G2 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1012. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C8h

Figure 3-487. CONTROLSS_ICLXBAR_ICLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1013. ICLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar3 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.14 CONTROLSS_ICLXBAR_ICLXBAR4_G0 Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1014. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4200h

Figure 3-488. CONTROLSS_ICLXBAR_ICLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1015. ICLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar4 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.15 CONTROLSS_ICLXBAR_ICLXBAR4_G1 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1016. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4204h

Figure 3-489. CONTROLSS_ICLXBAR_ICLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1017. ICLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar4 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.16 CONTROLSS_ICLXBAR_ICLXBAR4_G2 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1018. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4208h

Figure 3-490. CONTROLSS_ICLXBAR_ICLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1019. ICLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar4 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.17 CONTROLSS_ICLXBAR_ICLXBAR5_G0 Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1020. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4240h

Figure 3-491. CONTROLSS_ICLXBAR_ICLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1021. ICLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar5 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.18 CONTROLSS_ICLXBAR_ICLXBAR5_G1 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1022. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4244h

Figure 3-492. CONTROLSS_ICLXBAR_ICLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1023. ICLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar5 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.19 CONTROLSS_ICLXBAR_ICLXBAR5_G2 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1024. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4248h

Figure 3-493. CONTROLSS_ICLXBAR_ICLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1025. ICLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar5 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.20 CONTROLSS_ICLXBAR_ICLXBAR6_G0 Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1026. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4280h

Figure 3-494. CONTROLSS_ICLXBAR_ICLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1027. ICLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar6 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.21 CONTROLSS_ICLXBAR_ICLXBAR6_G1 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1028. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4284h

Figure 3-495. CONTROLSS_ICLXBAR_ICLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1029. ICLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar6 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.22 CONTROLSS_ICLXBAR_ICLXBAR6_G2 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1030. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4288h

Figure 3-496. CONTROLSS_ICLXBAR_ICLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1031. ICLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar6 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.23 CONTROLSS_ICLXBAR_ICLXBAR7_G0 Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1032. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C0h

Figure 3-497. CONTROLSS_ICLXBAR_ICLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1033. ICLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar7 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.24 CONTROLSS_ICLXBAR_ICLXBAR7_G1 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1034. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C4h

Figure 3-498. CONTROLSS_ICLXBAR_ICLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1035. ICLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar7 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.25 CONTROLSS_ICLXBAR_ICLXBAR7_G2 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1036. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C8h

Figure 3-499. CONTROLSS_ICLXBAR_ICLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1037. ICLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar7 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.26 CONTROLSS_ICLXBAR_ICLXBAR8_G0 Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1038. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4300h

Figure 3-500. CONTROLSS_ICLXBAR_ICLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1039. ICLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar8 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.27 CONTROLSS_ICLXBAR_ICLXBAR8_G1 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1040. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4304h

Figure 3-501. CONTROLSS_ICLXBAR_ICLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1041. ICLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar8 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.28 CONTROLSS_ICLXBAR_ICLXBAR8_G2 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1042. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4308h

Figure 3-502. CONTROLSS_ICLXBAR_ICLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1043. ICLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar8 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.29 CONTROLSS_ICLXBAR_ICLXBAR9_G0 Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1044. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4340h

Figure 3-503. CONTROLSS_ICLXBAR_ICLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1045. ICLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar9 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.30 CONTROLSS_ICLXBAR_ICLXBAR9_G1 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1046. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4344h

Figure 3-504. CONTROLSS_ICLXBAR_ICLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1047. ICLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar9 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.31 CONTROLSS_ICLXBAR_ICLXBAR9_G2 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1048. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4348h

Figure 3-505. CONTROLSS_ICLXBAR_ICLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1049. ICLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar9 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.32 CONTROLSS_ICLXBAR_ICLXBAR10_G0 Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1050. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4380h

Figure 3-506. CONTROLSS_ICLXBAR_ICLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1051. ICLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar10 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.33 CONTROLSS_ICLXBAR_ICLXBAR10_G1 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1052. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4384h

Figure 3-507. CONTROLSS_ICLXBAR_ICLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1053. ICLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar10 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

ADVANCE INFORMATION

3.11.34 CONTROLSS_ICLXBAR_ICLXBAR10_G2 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1054. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4388h

Figure 3-508. CONTROLSS_ICLXBAR_ICLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1055. ICLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar10 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.35 CONTROLSS_ICLXBAR_ICLXBAR11_G0 Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1056. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C0h

Figure 3-509. CONTROLSS_ICLXBAR_ICLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1057. ICLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar11 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.36 CONTROLSS_ICLXBAR_ICLXBAR11_G1 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1058. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C4h

Figure 3-510. CONTROLSS_ICLXBAR_ICLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1059. ICLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar11 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.37 CONTROLSS_ICLXBAR_ICLXBAR11_G2 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1060. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C8h

Figure 3-511. CONTROLSS_ICLXBAR_ICLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1061. ICLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar11 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.38 CONTROLSS_ICLXBAR_ICLXBAR12_G0 Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1062. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4400h

Figure 3-512. CONTROLSS_ICLXBAR_ICLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1063. ICLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar12 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.39 CONTROLSS_ICLXBAR_ICLXBAR12_G1 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1064. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4404h

Figure 3-513. CONTROLSS_ICLXBAR_ICLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1065. ICLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar12 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.40 CONTROLSS_ICLXBAR_ICLXBAR12_G2 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1066. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4408h

Figure 3-514. CONTROLSS_ICLXBAR_ICLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1067. ICLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar12 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.41 CONTROLSS_ICLXBAR_ICLXBAR13_G0 Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1068. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4440h

Figure 3-515. CONTROLSS_ICLXBAR_ICLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1069. ICLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar13 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.42 CONTROLSS_ICLXBAR_ICLXBAR13_G1 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1070. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4444h

Figure 3-516. CONTROLSS_ICLXBAR_ICLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1071. ICLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar13 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.43 CONTROLSS_ICLXBAR_ICLXBAR13_G2 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1072. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4448h

Figure 3-517. CONTROLSS_ICLXBAR_ICLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1073. ICLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar13 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.44 CONTROLSS_ICLXBAR_ICLXBAR14_G0 Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1074. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4480h

Figure 3-518. CONTROLSS_ICLXBAR_ICLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1075. ICLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar14 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.45 CONTROLSS_ICLXBAR_ICLXBAR14_G1 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1076. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4484h

Figure 3-519. CONTROLSS_ICLXBAR_ICLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1077. ICLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar14 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.46 CONTROLSS_ICLXBAR_ICLXBAR14_G2 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1078. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4488h

Figure 3-520. CONTROLSS_ICLXBAR_ICLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1079. ICLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar14 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.11.47 CONTROLSS_ICLXBAR_ICLXBAR15_G0 Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1080. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C0h

Figure 3-521. CONTROLSS_ICLXBAR_ICLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1081. ICLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar15 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

3.11.48 CONTROLSS_ICLXBAR_ICLXBAR15_G1 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1082. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C4h

Figure 3-522. CONTROLSS_ICLXBAR_ICLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1083. ICLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar15 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

3.11.49 CONTROLSS_ICLXBAR_ICLXBAR15_G2 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1084. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C8h

Figure 3-523. CONTROLSS_ICLXBAR_ICLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1085. ICLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar15 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

Table 3-1086. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.12 C2K_INPUTXBAR Registers

Table 3-1087. CONTROLSS_INPUTXBAR, CONTROLSS_INPUTXBAR_CONTROLSS_INPUTXBAR Registers, Base Address=502D 0000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_INPUTXBAR Physical Address
0h	32	CONTROLSS_INPUTXBAR_PID	PID register	502D 0000h
100h	0	CONTROLSS_INPUTXBAR_INPUTXBAR0_GSEL	RW	502D 0100h
104h	8	CONTROLSS_INPUTXBAR_INPUTXBAR0_G0	RW	502D 0104h
108h	8	CONTROLSS_INPUTXBAR_INPUTXBAR0_G1	RW	502D 0108h
140h	0	CONTROLSS_INPUTXBAR_INPUTXBAR1_GSEL	RW	502D 0140h
144h	8	CONTROLSS_INPUTXBAR_INPUTXBAR1_G0	RW	502D 0144h
148h	8	CONTROLSS_INPUTXBAR_INPUTXBAR1_G1	RW	502D 0148h
180h	0	CONTROLSS_INPUTXBAR_INPUTXBAR2_GSEL	RW	502D 0180h
184h	8	CONTROLSS_INPUTXBAR_INPUTXBAR2_G0	RW	502D 0184h
188h	8	CONTROLSS_INPUTXBAR_INPUTXBAR2_G1	RW	502D 0188h
1C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR3_GSEL	RW	502D 01C0h
1C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR3_G0	RW	502D 01C4h
1C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR3_G1	RW	502D 01C8h
200h	0	CONTROLSS_INPUTXBAR_INPUTXBAR4_GSEL	RW	502D 0200h
204h	8	CONTROLSS_INPUTXBAR_INPUTXBAR4_G0	RW	502D 0204h
208h	8	CONTROLSS_INPUTXBAR_INPUTXBAR4_G1	RW	502D 0208h
240h	0	CONTROLSS_INPUTXBAR_INPUTXBAR5_GSEL	RW	502D 0240h
244h	8	CONTROLSS_INPUTXBAR_INPUTXBAR5_G0	RW	502D 0244h
248h	8	CONTROLSS_INPUTXBAR_INPUTXBAR5_G1	RW	502D 0248h
280h	0	CONTROLSS_INPUTXBAR_INPUTXBAR6_GSEL	RW	502D 0280h
284h	8	CONTROLSS_INPUTXBAR_INPUTXBAR6_G0	RW	502D 0284h
288h	8	CONTROLSS_INPUTXBAR_INPUTXBAR6_G1	RW	502D 0288h
2C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR7_GSEL	RW	502D 02C0h

Table 3-1087. CONTROLSS_INPUTXBAR, CONTROLSS_INPUTXBAR_CONTROLSS_INPUTXBAR Registers, Base Address=502D 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INPUTXBAR Physical Address
2C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR7_G0	RW	502D 02C4h
2C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR7_G1	RW	502D 02C8h
300h	0	CONTROLSS_INPUTXBAR_INPUTXBAR8_GSEL	RW	502D 0300h
304h	8	CONTROLSS_INPUTXBAR_INPUTXBAR8_G0	RW	502D 0304h
308h	8	CONTROLSS_INPUTXBAR_INPUTXBAR8_G1	RW	502D 0308h
340h	0	CONTROLSS_INPUTXBAR_INPUTXBAR9_GSEL	RW	502D 0340h
344h	8	CONTROLSS_INPUTXBAR_INPUTXBAR9_G0	RW	502D 0344h
348h	8	CONTROLSS_INPUTXBAR_INPUTXBAR9_G1	RW	502D 0348h
380h	0	CONTROLSS_INPUTXBAR_INPUTXBAR10_GSEL	RW	502D 0380h
384h	8	CONTROLSS_INPUTXBAR_INPUTXBAR10_G0	RW	502D 0384h
388h	8	CONTROLSS_INPUTXBAR_INPUTXBAR10_G1	RW	502D 0388h
3C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR11_GSEL	RW	502D 03C0h
3C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR11_G0	RW	502D 03C4h
3C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR11_G1	RW	502D 03C8h
400h	0	CONTROLSS_INPUTXBAR_INPUTXBAR12_GSEL	RW	502D 0400h
404h	8	CONTROLSS_INPUTXBAR_INPUTXBAR12_G0	RW	502D 0404h
408h	8	CONTROLSS_INPUTXBAR_INPUTXBAR12_G1	RW	502D 0408h
440h	0	CONTROLSS_INPUTXBAR_INPUTXBAR13_GSEL	RW	502D 0440h
444h	8	CONTROLSS_INPUTXBAR_INPUTXBAR13_G0	RW	502D 0444h
448h	8	CONTROLSS_INPUTXBAR_INPUTXBAR13_G1	RW	502D 0448h
480h	0	CONTROLSS_INPUTXBAR_INPUTXBAR14_GSEL	RW	502D 0480h
484h	8	CONTROLSS_INPUTXBAR_INPUTXBAR14_G0	RW	502D 0484h
488h	8	CONTROLSS_INPUTXBAR_INPUTXBAR14_G1	RW	502D 0488h
4C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR15_GSEL	RW	502D 04C0h
4C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR15_G0	RW	502D 04C4h
4C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR15_G1	RW	502D 04C8h
500h	0	CONTROLSS_INPUTXBAR_INPUTXBAR16_GSEL	RW	502D 0500h

Table 3-1087. CONTROLSS_INPUTXBAR, CONTROLSS_INPUTXBAR_CONTROLSS_INPUTXBAR Registers, Base Address=502D 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INPUTXBAR Physical Address
504h	8	CONTROLSS_INPUTXBAR_INPUTXBAR16_G0	RW	502D 0504h
508h	8	CONTROLSS_INPUTXBAR_INPUTXBAR16_G1	RW	502D 0508h
540h	0	CONTROLSS_INPUTXBAR_INPUTXBAR17_GSEL	RW	502D 0540h
544h	8	CONTROLSS_INPUTXBAR_INPUTXBAR17_G0	RW	502D 0544h
548h	8	CONTROLSS_INPUTXBAR_INPUTXBAR17_G1	RW	502D 0548h
580h	0	CONTROLSS_INPUTXBAR_INPUTXBAR18_GSEL	RW	502D 0580h
584h	8	CONTROLSS_INPUTXBAR_INPUTXBAR18_G0	RW	502D 0584h
588h	8	CONTROLSS_INPUTXBAR_INPUTXBAR18_G1	RW	502D 0588h
5C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR19_GSEL	RW	502D 05C0h
5C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR19_G0	RW	502D 05C4h
5C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR19_G1	RW	502D 05C8h
600h	0	CONTROLSS_INPUTXBAR_INPUTXBAR20_GSEL	RW	502D 0600h
604h	8	CONTROLSS_INPUTXBAR_INPUTXBAR20_G0	RW	502D 0604h
608h	8	CONTROLSS_INPUTXBAR_INPUTXBAR20_G1	RW	502D 0608h
640h	0	CONTROLSS_INPUTXBAR_INPUTXBAR21_GSEL	RW	502D 0640h
644h	8	CONTROLSS_INPUTXBAR_INPUTXBAR21_G0	RW	502D 0644h
648h	8	CONTROLSS_INPUTXBAR_INPUTXBAR21_G1	RW	502D 0648h
680h	0	CONTROLSS_INPUTXBAR_INPUTXBAR22_GSEL	RW	502D 0680h
684h	8	CONTROLSS_INPUTXBAR_INPUTXBAR22_G0	RW	502D 0684h
688h	8	CONTROLSS_INPUTXBAR_INPUTXBAR22_G1	RW	502D 0688h
6C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR23_GSEL	RW	502D 06C0h
6C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR23_G0	RW	502D 06C4h
6C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR23_G1	RW	502D 06C8h
700h	0	CONTROLSS_INPUTXBAR_INPUTXBAR24_GSEL	RW	502D 0700h
704h	8	CONTROLSS_INPUTXBAR_INPUTXBAR24_G0	RW	502D 0704h
708h	8	CONTROLSS_INPUTXBAR_INPUTXBAR24_G1	RW	502D 0708h
740h	0	CONTROLSS_INPUTXBAR_INPUTXBAR25_GSEL	RW	502D 0740h

Table 3-1087. CONTROLSS_INPUTXBAR, CONTROLSS_INPUTXBAR_CONTROLSS_INPUTXBAR Registers, Base Address=502D 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INPUTXBAR Physical Address
744h	8	CONTROLSS_INPUTXBAR_INPUTXBAR25_G0	RW	502D 0744h
748h	8	CONTROLSS_INPUTXBAR_INPUTXBAR25_G1	RW	502D 0748h
780h	0	CONTROLSS_INPUTXBAR_INPUTXBAR26_GSEL	RW	502D 0780h
784h	8	CONTROLSS_INPUTXBAR_INPUTXBAR26_G0	RW	502D 0784h
788h	8	CONTROLSS_INPUTXBAR_INPUTXBAR26_G1	RW	502D 0788h
7C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR27_GSEL	RW	502D 07C0h
7C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR27_G0	RW	502D 07C4h
7C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR27_G1	RW	502D 07C8h
800h	0	CONTROLSS_INPUTXBAR_INPUTXBAR28_GSEL	RW	502D 0800h
804h	8	CONTROLSS_INPUTXBAR_INPUTXBAR28_G0	RW	502D 0804h
808h	8	CONTROLSS_INPUTXBAR_INPUTXBAR28_G1	RW	502D 0808h
840h	0	CONTROLSS_INPUTXBAR_INPUTXBAR29_GSEL	RW	502D 0840h
844h	8	CONTROLSS_INPUTXBAR_INPUTXBAR29_G0	RW	502D 0844h
848h	8	CONTROLSS_INPUTXBAR_INPUTXBAR29_G1	RW	502D 0848h
880h	0	CONTROLSS_INPUTXBAR_INPUTXBAR30_GSEL	RW	502D 0880h
884h	8	CONTROLSS_INPUTXBAR_INPUTXBAR30_G0	RW	502D 0884h
888h	8	CONTROLSS_INPUTXBAR_INPUTXBAR30_G1	RW	502D 0888h
8C0h	0	CONTROLSS_INPUTXBAR_INPUTXBAR31_GSEL	RW	502D 08C0h
8C4h	8	CONTROLSS_INPUTXBAR_INPUTXBAR31_G0	RW	502D 08C4h
8C8h	8	CONTROLSS_INPUTXBAR_INPUTXBAR31_G1	RW	502D 08C8h

3.12.1 CONTROLSS_INPUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1088. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0000h

Figure 3-524. CONTROLSS_INPUTXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-1089. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.12.2 CONTROLSS_INPUTXBAR_INPUTXBAR0_GSEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1090. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0100h

Figure 3-525. CONTROLSS_INPUTXBAR_INPUTXBAR0_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1091. INPUTXBAR0_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.3 CONTROLSS_INPUTXBAR_INPUTXBAR0_G0 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1092. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0104h

Figure 3-526. CONTROLSS_INPUTXBAR_INPUTXBAR0_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1093. INPUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.4 CONTROLSS_INPUTXBAR_INPUTXBAR0_G1 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1094. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0108h

Figure 3-527. CONTROLSS_INPUTXBAR_INPUTXBAR0_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1095. INPUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.5 CONTROLSS_INPUTXBAR_INPUTXBAR1_GSEL Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1096. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0140h

Figure 3-528. CONTROLSS_INPUTXBAR_INPUTXBAR1_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1097. INPUTXBAR1_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.6 CONTROLSS_INPUTXBAR_INPUTXBAR1_G0 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1098. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0144h

Figure 3-529. CONTROLSS_INPUTXBAR_INPUTXBAR1_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1099. INPUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.7 CONTROLSS_INPUTXBAR_INPUTXBAR1_G1 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1100. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0148h

Figure 3-530. CONTROLSS_INPUTXBAR_INPUTXBAR1_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1101. INPUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.8 CONTROLSS_INPUTXBAR_INPUTXBAR2_GSEL Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1102. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0180h

Figure 3-531. CONTROLSS_INPUTXBAR_INPUTXBAR2_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1103. INPUTXBAR2_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.9 CONTROLSS_INPUTXBAR_INPUTXBAR2_G0 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1104. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0184h

Figure 3-532. CONTROLSS_INPUTXBAR_INPUTXBAR2_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1105. INPUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.10 CONTROLSS_INPUTXBAR_INPUTXBAR2_G1 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1106. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0188h

Figure 3-533. CONTROLSS_INPUTXBAR_INPUTXBAR2_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1107. INPUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.11 CONTROLSS_INPUTXBAR_INPUTXBAR3_GSEL Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1108. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C0h

Figure 3-534. CONTROLSS_INPUTXBAR_INPUTXBAR3_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1109. INPUTXBAR3_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.12 CONTROLSS_INPUTXBAR_INPUTXBAR3_G0 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1110. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C4h

Figure 3-535. CONTROLSS_INPUTXBAR_INPUTXBAR3_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1111. INPUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.13 CONTROLSS_INPUTXBAR_INPUTXBAR3_G1 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1112. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C8h

Figure 3-536. CONTROLSS_INPUTXBAR_INPUTXBAR3_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1113. INPUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.14 CONTROLSS_INPUTXBAR_INPUTXBAR4_GSEL Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1114. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0200h

Figure 3-537. CONTROLSS_INPUTXBAR_INPUTXBAR4_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1115. INPUTXBAR4_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.15 CONTROLSS_INPUTXBAR_INPUTXBAR4_G0 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1116. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0204h

Figure 3-538. CONTROLSS_INPUTXBAR_INPUTXBAR4_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1117. INPUTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.16 CONTROLSS_INPUTXBAR_INPUTXBAR4_G1 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1118. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0208h

Figure 3-539. CONTROLSS_INPUTXBAR_INPUTXBAR4_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1119. INPUTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.17 CONTROLSS_INPUTXBAR_INPUTXBAR5_GSEL Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1120. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0240h

Figure 3-540. CONTROLSS_INPUTXBAR_INPUTXBAR5_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1121. INPUTXBAR5_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.18 CONTROLSS_INPUTXBAR_INPUTXBAR5_G0 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1122. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0244h

Figure 3-541. CONTROLSS_INPUTXBAR_INPUTXBAR5_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1123. INPUTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.19 CONTROLSS_INPUTXBAR_INPUTXBAR5_G1 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1124. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0248h

Figure 3-542. CONTROLSS_INPUTXBAR_INPUTXBAR5_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1125. INPUTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.20 CONTROLSS_INPUTXBAR_INPUTXBAR6_GSEL Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1126. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0280h

Figure 3-543. CONTROLSS_INPUTXBAR_INPUTXBAR6_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1127. INPUTXBAR6_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.21 CONTROLSS_INPUTXBAR_INPUTXBAR6_G0 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1128. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0284h

Figure 3-544. CONTROLSS_INPUTXBAR_INPUTXBAR6_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1129. INPUTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.22 CONTROLSS_INPUTXBAR_INPUTXBAR6_G1 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1130. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0288h

Figure 3-545. CONTROLSS_INPUTXBAR_INPUTXBAR6_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1131. INPUTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.23 CONTROLSS_INPUTXBAR_INPUTXBAR7_GSEL Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1132. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C0h

Figure 3-546. CONTROLSS_INPUTXBAR_INPUTXBAR7_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1133. INPUTXBAR7_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.24 CONTROLSS_INPUTXBAR_INPUTXBAR7_G0 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1134. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C4h

Figure 3-547. CONTROLSS_INPUTXBAR_INPUTXBAR7_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1135. INPUTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.25 CONTROLSS_INPUTXBAR_INPUTXBAR7_G1 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1136. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C8h

Figure 3-548. CONTROLSS_INPUTXBAR_INPUTXBAR7_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1137. INPUTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.26 CONTROLSS_INPUTXBAR_INPUTXBAR8_GSEL Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1138. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0300h

Figure 3-549. CONTROLSS_INPUTXBAR_INPUTXBAR8_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1139. INPUTXBAR8_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.27 CONTROLSS_INPUTXBAR_INPUTXBAR8_G0 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1140. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0304h

Figure 3-550. CONTROLSS_INPUTXBAR_INPUTXBAR8_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1141. INPUTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.28 CONTROLSS_INPUTXBAR_INPUTXBAR8_G1 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1142. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0308h

Figure 3-551. CONTROLSS_INPUTXBAR_INPUTXBAR8_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1143. INPUTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.29 CONTROLSS_INPUTXBAR_INPUTXBAR9_GSEL Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1144. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0340h

Figure 3-552. CONTROLSS_INPUTXBAR_INPUTXBAR9_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1145. INPUTXBAR9_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.30 CONTROLSS_INPUTXBAR_INPUTXBAR9_G0 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1146. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0344h

Figure 3-553. CONTROLSS_INPUTXBAR_INPUTXBAR9_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1147. INPUTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.31 CONTROLSS_INPUTXBAR_INPUTXBAR9_G1 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1148. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0348h

Figure 3-554. CONTROLSS_INPUTXBAR_INPUTXBAR9_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1149. INPUTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.32 CONTROLSS_INPUTXBAR_INPUTXBAR10_GSEL Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1150. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0380h

Figure 3-555. CONTROLSS_INPUTXBAR_INPUTXBAR10_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1151. INPUTXBAR10_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.33 CONTROLSS_INPUTXBAR_INPUTXBAR10_G0 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1152. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0384h

Figure 3-556. CONTROLSS_INPUTXBAR_INPUTXBAR10_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1153. INPUTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.34 CONTROLSS_INPUTXBAR_INPUTXBAR10_G1 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1154. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0388h

Figure 3-557. CONTROLSS_INPUTXBAR_INPUTXBAR10_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1155. INPUTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.35 CONTROLSS_INPUTXBAR_INPUTXBAR11_GSEL Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1156. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C0h

Figure 3-558. CONTROLSS_INPUTXBAR_INPUTXBAR11_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1157. INPUTXBAR11_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.36 CONTROLSS_INPUTXBAR_INPUTXBAR11_G0 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1158. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C4h

Figure 3-559. CONTROLSS_INPUTXBAR_INPUTXBAR11_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1159. INPUTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.37 CONTROLSS_INPUTXBAR_INPUTXBAR11_G1 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1160. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C8h

Figure 3-560. CONTROLSS_INPUTXBAR_INPUTXBAR11_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1161. INPUTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.38 CONTROLSS_INPUTXBAR_INPUTXBAR12_GSEL Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1162. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0400h

Figure 3-561. CONTROLSS_INPUTXBAR_INPUTXBAR12_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1163. INPUTXBAR12_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.39 CONTROLSS_INPUTXBAR_INPUTXBAR12_G0 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1164. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0404h

Figure 3-562. CONTROLSS_INPUTXBAR_INPUTXBAR12_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1165. INPUTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.40 CONTROLSS_INPUTXBAR_INPUTXBAR12_G1 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1166. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0408h

Figure 3-563. CONTROLSS_INPUTXBAR_INPUTXBAR12_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1167. INPUTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.41 CONTROLSS_INPUTXBAR_INPUTXBAR13_GSEL Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1168. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0440h

Figure 3-564. CONTROLSS_INPUTXBAR_INPUTXBAR13_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1169. INPUTXBAR13_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.42 CONTROLSS_INPUTXBAR_INPUTXBAR13_G0 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1170. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0444h

Figure 3-565. CONTROLSS_INPUTXBAR_INPUTXBAR13_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1171. INPUTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.43 CONTROLSS_INPUTXBAR_INPUTXBAR13_G1 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1172. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0448h

Figure 3-566. CONTROLSS_INPUTXBAR_INPUTXBAR13_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				SEL			
NONE				RW			
0				0			

Access Types Legend

Table 3-1173. INPUTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.44 CONTROLSS_INPUTXBAR_INPUTXBAR14_GSEL Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1174. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0480h

Figure 3-567. CONTROLSS_INPUTXBAR_INPUTXBAR14_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1175. INPUTXBAR14_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.45 CONTROLSS_INPUTXBAR_INPUTXBAR14_G0 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1176. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0484h

Figure 3-568. CONTROLSS_INPUTXBAR_INPUTXBAR14_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1177. INPUTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.46 CONTROLSS_INPUTXBAR_INPUTXBAR14_G1 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1178. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0488h

Figure 3-569. CONTROLSS_INPUTXBAR_INPUTXBAR14_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1179. INPUTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.47 CONTROLSS_INPUTXBAR_INPUTXBAR15_GSEL Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1180. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C0h

Figure 3-570. CONTROLSS_INPUTXBAR_INPUTXBAR15_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1181. INPUTXBAR15_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.48 CONTROLSS_INPUTXBAR_INPUTXBAR15_G0 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1182. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C4h

Figure 3-571. CONTROLSS_INPUTXBAR_INPUTXBAR15_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1183. INPUTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.49 CONTROLSS_INPUTXBAR_INPUTXBAR15_G1 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1184. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C8h

Figure 3-572. CONTROLSS_INPUTXBAR_INPUTXBAR15_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1185. INPUTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.50 CONTROLSS_INPUTXBAR_INPUTXBAR16_GSEL Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1186. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0500h

Figure 3-573. CONTROLSS_INPUTXBAR_INPUTXBAR16_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1187. INPUTXBAR16_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.51 CONTROLSS_INPUTXBAR_INPUTXBAR16_G0 Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1188. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0504h

Figure 3-574. CONTROLSS_INPUTXBAR_INPUTXBAR16_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1189. INPUTXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.52 CONTROLSS_INPUTXBAR_INPUTXBAR16_G1 Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1190. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0508h

Figure 3-575. CONTROLSS_INPUTXBAR_INPUTXBAR16_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1191. INPUTXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.53 CONTROLSS_INPUTXBAR_INPUTXBAR17_GSEL Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1192. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0540h

Figure 3-576. CONTROLSS_INPUTXBAR_INPUTXBAR17_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1193. INPUTXBAR17_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.54 CONTROLSS_INPUTXBAR_INPUTXBAR17_G0 Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1194. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0544h

Figure 3-577. CONTROLSS_INPUTXBAR_INPUTXBAR17_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1195. INPUTXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.55 CONTROLSS_INPUTXBAR_INPUTXBAR17_G1 Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1196. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0548h

Figure 3-578. CONTROLSS_INPUTXBAR_INPUTXBAR17_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1197. INPUTXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.56 CONTROLSS_INPUTXBAR_INPUTXBAR18_GSEL Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1198. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0580h

Figure 3-579. CONTROLSS_INPUTXBAR_INPUTXBAR18_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1199. INPUTXBAR18_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.57 CONTROLSS_INPUTXBAR_INPUTXBAR18_G0 Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1200. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0584h

Figure 3-580. CONTROLSS_INPUTXBAR_INPUTXBAR18_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1201. INPUTXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.58 CONTROLSS_INPUTXBAR_INPUTXBAR18_G1 Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1202. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0588h

Figure 3-581. CONTROLSS_INPUTXBAR_INPUTXBAR18_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1203. INPUTXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.59 CONTROLSS_INPUTXBAR_INPUTXBAR19_GSEL Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1204. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C0h

Figure 3-582. CONTROLSS_INPUTXBAR_INPUTXBAR19_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1205. INPUTXBAR19_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.60 CONTROLSS_INPUTXBAR_INPUTXBAR19_G0 Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1206. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C4h

Figure 3-583. CONTROLSS_INPUTXBAR_INPUTXBAR19_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1207. INPUTXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.61 CONTROLSS_INPUTXBAR_INPUTXBAR19_G1 Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1208. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C8h

Figure 3-584. CONTROLSS_INPUTXBAR_INPUTXBAR19_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1209. INPUTXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.62 CONTROLSS_INPUTXBAR_INPUTXBAR20_GSEL Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1210. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0600h

Figure 3-585. CONTROLSS_INPUTXBAR_INPUTXBAR20_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1211. INPUTXBAR20_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.63 CONTROLSS_INPUTXBAR_INPUTXBAR20_G0 Register (Offset = 604h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1212. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0604h

Figure 3-586. CONTROLSS_INPUTXBAR_INPUTXBAR20_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1213. INPUTXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.64 CONTROLSS_INPUTXBAR_INPUTXBAR20_G1 Register (Offset = 608h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1214. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0608h

Figure 3-587. CONTROLSS_INPUTXBAR_INPUTXBAR20_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1215. INPUTXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.65 CONTROLSS_INPUTXBAR_INPUTXBAR21_GSEL Register (Offset = 640h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1216. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0640h

Figure 3-588. CONTROLSS_INPUTXBAR_INPUTXBAR21_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1217. INPUTXBAR21_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.66 CONTROLSS_INPUTXBAR_INPUTXBAR21_G0 Register (Offset = 644h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1218. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0644h

Figure 3-589. CONTROLSS_INPUTXBAR_INPUTXBAR21_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1219. INPUTXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.67 CONTROLSS_INPUTXBAR_INPUTXBAR21_G1 Register (Offset = 648h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1220. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0648h

Figure 3-590. CONTROLSS_INPUTXBAR_INPUTXBAR21_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1221. INPUTXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.68 CONTROLSS_INPUTXBAR_INPUTXBAR22_GSEL Register (Offset = 680h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1222. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0680h

Figure 3-591. CONTROLSS_INPUTXBAR_INPUTXBAR22_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1223. INPUTXBAR22_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.69 CONTROLSS_INPUTXBAR_INPUTXBAR22_G0 Register (Offset = 684h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1224. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0684h

Figure 3-592. CONTROLSS_INPUTXBAR_INPUTXBAR22_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1225. INPUTXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.70 CONTROLSS_INPUTXBAR_INPUTXBAR22_G1 Register (Offset = 688h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1226. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0688h

Figure 3-593. CONTROLSS_INPUTXBAR_INPUTXBAR22_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1227. INPUTXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.71 CONTROLSS_INPUTXBAR_INPUTXBAR23_GSEL Register (Offset = 6C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1228. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C0h

Figure 3-594. CONTROLSS_INPUTXBAR_INPUTXBAR23_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1229. INPUTXBAR23_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.72 CONTROLSS_INPUTXBAR_INPUTXBAR23_G0 Register (Offset = 6C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1230. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C4h

Figure 3-595. CONTROLSS_INPUTXBAR_INPUTXBAR23_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1231. INPUTXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.73 CONTROLSS_INPUTXBAR_INPUTXBAR23_G1 Register (Offset = 6C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1232. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C8h

Figure 3-596. CONTROLSS_INPUTXBAR_INPUTXBAR23_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1233. INPUTXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.74 CONTROLSS_INPUTXBAR_INPUTXBAR24_GSEL Register (Offset = 700h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1234. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0700h

Figure 3-597. CONTROLSS_INPUTXBAR_INPUTXBAR24_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1235. INPUTXBAR24_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.75 CONTROLSS_INPUTXBAR_INPUTXBAR24_G0 Register (Offset = 704h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1236. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0704h

Figure 3-598. CONTROLSS_INPUTXBAR_INPUTXBAR24_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1237. INPUTXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.76 CONTROLSS_INPUTXBAR_INPUTXBAR24_G1 Register (Offset = 708h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1238. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0708h

Figure 3-599. CONTROLSS_INPUTXBAR_INPUTXBAR24_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1239. INPUTXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.77 CONTROLSS_INPUTXBAR_INPUTXBAR25_GSEL Register (Offset = 740h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1240. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0740h

Figure 3-600. CONTROLSS_INPUTXBAR_INPUTXBAR25_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1241. INPUTXBAR25_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.78 CONTROLSS_INPUTXBAR_INPUTXBAR25_G0 Register (Offset = 744h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1242. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0744h

Figure 3-601. CONTROLSS_INPUTXBAR_INPUTXBAR25_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1243. INPUTXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.79 CONTROLSS_INPUTXBAR_INPUTXBAR25_G1 Register (Offset = 748h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1244. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0748h

Figure 3-602. CONTROLSS_INPUTXBAR_INPUTXBAR25_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1245. INPUTXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.80 CONTROLSS_INPUTXBAR_INPUTXBAR26_GSEL Register (Offset = 780h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1246. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0780h

Figure 3-603. CONTROLSS_INPUTXBAR_INPUTXBAR26_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1247. INPUTXBAR26_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.81 CONTROLSS_INPUTXBAR_INPUTXBAR26_G0 Register (Offset = 784h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1248. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0784h

Figure 3-604. CONTROLSS_INPUTXBAR_INPUTXBAR26_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1249. INPUTXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.82 CONTROLSS_INPUTXBAR_INPUTXBAR26_G1 Register (Offset = 788h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1250. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0788h

Figure 3-605. CONTROLSS_INPUTXBAR_INPUTXBAR26_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1251. INPUTXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.83 CONTROLSS_INPUTXBAR_INPUTXBAR27_GSEL Register (Offset = 7C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1252. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C0h

Figure 3-606. CONTROLSS_INPUTXBAR_INPUTXBAR27_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1253. INPUTXBAR27_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.84 CONTROLSS_INPUTXBAR_INPUTXBAR27_G0 Register (Offset = 7C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1254. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C4h

Figure 3-607. CONTROLSS_INPUTXBAR_INPUTXBAR27_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1255. INPUTXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.85 CONTROLSS_INPUTXBAR_INPUTXBAR27_G1 Register (Offset = 7C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1256. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C8h

Figure 3-608. CONTROLSS_INPUTXBAR_INPUTXBAR27_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1257. INPUTXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.86 CONTROLSS_INPUTXBAR_INPUTXBAR28_GSEL Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1258. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0800h

Figure 3-609. CONTROLSS_INPUTXBAR_INPUTXBAR28_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1259. INPUTXBAR28_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.87 CONTROLSS_INPUTXBAR_INPUTXBAR28_G0 Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1260. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0804h

Figure 3-610. CONTROLSS_INPUTXBAR_INPUTXBAR28_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1261. INPUTXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.88 CONTROLSS_INPUTXBAR_INPUTXBAR28_G1 Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1262. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0808h

Figure 3-611. CONTROLSS_INPUTXBAR_INPUTXBAR28_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1263. INPUTXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.89 CONTROLSS_INPUTXBAR_INPUTXBAR29_GSEL Register (Offset = 840h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1264. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0840h

Figure 3-612. CONTROLSS_INPUTXBAR_INPUTXBAR29_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1265. INPUTXBAR29_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.90 CONTROLSS_INPUTXBAR_INPUTXBAR29_G0 Register (Offset = 844h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1266. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0844h

Figure 3-613. CONTROLSS_INPUTXBAR_INPUTXBAR29_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1267. INPUTXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.91 CONTROLSS_INPUTXBAR_INPUTXBAR29_G1 Register (Offset = 848h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1268. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0848h

Figure 3-614. CONTROLSS_INPUTXBAR_INPUTXBAR29_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1269. INPUTXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.92 CONTROLSS_INPUTXBAR_INPUTXBAR30_GSEL Register (Offset = 880h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1270. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0880h

Figure 3-615. CONTROLSS_INPUTXBAR_INPUTXBAR30_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1271. INPUTXBAR30_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.93 CONTROLSS_INPUTXBAR_INPUTXBAR30_G0 Register (Offset = 884h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1272. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0884h

Figure 3-616. CONTROLSS_INPUTXBAR_INPUTXBAR30_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1273. INPUTXBAR30_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.94 CONTROLSS_INPUTXBAR_INPUTXBAR30_G1 Register (Offset = 888h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1274. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0888h

Figure 3-617. CONTROLSS_INPUTXBAR_INPUTXBAR30_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1275. INPUTXBAR30_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.12.95 CONTROLSS_INPUTXBAR_INPUTXBAR31_GSEL Register (Offset = 8C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1276. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C0h

Figure 3-618. CONTROLSS_INPUTXBAR_INPUTXBAR31_GSEL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
GSEL							
RW							
0							

Access Types Legend

Table 3-1277. INPUTXBAR31_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

3.12.96 CONTROLSS_INPUTXBAR_INPUTXBAR31_G0 Register (Offset = 8C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1278. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C4h

Figure 3-619. CONTROLSS_INPUTXBAR_INPUTXBAR31_G0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1279. INPUTXBAR31_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

3.12.97 CONTROLSS_INPUTXBAR_INPUTXBAR31_G1 Register (Offset = 8C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1280. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C8h

Figure 3-620. CONTROLSS_INPUTXBAR_INPUTXBAR31_G1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			SEL				
NONE			RW				
0			0				

Access Types Legend

Table 3-1281. INPUTXBAR31_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

Table 3-1282. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.13 C2K_INTXBAR Registers

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
0h	32	CONTROLSS_INTXBAR_PID	PID register	502D 5000h
100h	32	CONTROLSS_INTXBAR_INTXBAR0_G0	RW	502D 5100h
104h	32	CONTROLSS_INTXBAR_INTXBAR0_G1	RW	502D 5104h
108h	24	CONTROLSS_INTXBAR_INTXBAR0_G2	RW	502D 5108h
10Ch	16	CONTROLSS_INTXBAR_INTXBAR0_G3	RW	502D 510Ch
110h	16	CONTROLSS_INTXBAR_INTXBAR0_G4	RW	502D 5110h
114h	16	CONTROLSS_INTXBAR_INTXBAR0_G5	RW	502D 5114h
118h	8	CONTROLSS_INTXBAR_INTXBAR0_G6	RW	502D 5118h
140h	32	CONTROLSS_INTXBAR_INTXBAR1_G0	RW	502D 5140h
144h	32	CONTROLSS_INTXBAR_INTXBAR1_G1	RW	502D 5144h
148h	24	CONTROLSS_INTXBAR_INTXBAR1_G2	RW	502D 5148h
14Ch	16	CONTROLSS_INTXBAR_INTXBAR1_G3	RW	502D 514Ch
150h	16	CONTROLSS_INTXBAR_INTXBAR1_G4	RW	502D 5150h
154h	16	CONTROLSS_INTXBAR_INTXBAR1_G5	RW	502D 5154h
158h	8	CONTROLSS_INTXBAR_INTXBAR1_G6	RW	502D 5158h
180h	32	CONTROLSS_INTXBAR_INTXBAR2_G0	RW	502D 5180h
184h	32	CONTROLSS_INTXBAR_INTXBAR2_G1	RW	502D 5184h
188h	24	CONTROLSS_INTXBAR_INTXBAR2_G2	RW	502D 5188h
18Ch	16	CONTROLSS_INTXBAR_INTXBAR2_G3	RW	502D 518Ch
190h	16	CONTROLSS_INTXBAR_INTXBAR2_G4	RW	502D 5190h
194h	16	CONTROLSS_INTXBAR_INTXBAR2_G5	RW	502D 5194h
198h	8	CONTROLSS_INTXBAR_INTXBAR2_G6	RW	502D 5198h
1C0h	32	CONTROLSS_INTXBAR_INTXBAR3_G0	RW	502D 51C0h
1C4h	32	CONTROLSS_INTXBAR_INTXBAR3_G1	RW	502D 51C4h
1C8h	24	CONTROLSS_INTXBAR_INTXBAR3_G2	RW	502D 51C8h
1CCh	16	CONTROLSS_INTXBAR_INTXBAR3_G3	RW	502D 51CCh
1D0h	16	CONTROLSS_INTXBAR_INTXBAR3_G4	RW	502D 51D0h
1D4h	16	CONTROLSS_INTXBAR_INTXBAR3_G5	RW	502D 51D4h
1D8h	8	CONTROLSS_INTXBAR_INTXBAR3_G6	RW	502D 51D8h
200h	32	CONTROLSS_INTXBAR_INTXBAR4_G0	RW	502D 5200h
204h	32	CONTROLSS_INTXBAR_INTXBAR4_G1	RW	502D 5204h
208h	24	CONTROLSS_INTXBAR_INTXBAR4_G2	RW	502D 5208h
20Ch	16	CONTROLSS_INTXBAR_INTXBAR4_G3	RW	502D 520Ch
210h	16	CONTROLSS_INTXBAR_INTXBAR4_G4	RW	502D 5210h
214h	16	CONTROLSS_INTXBAR_INTXBAR4_G5	RW	502D 5214h
218h	8	CONTROLSS_INTXBAR_INTXBAR4_G6	RW	502D 5218h
240h	32	CONTROLSS_INTXBAR_INTXBAR5_G0	RW	502D 5240h
244h	32	CONTROLSS_INTXBAR_INTXBAR5_G1	RW	502D 5244h

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
248h	24	CONTROLSS_INTXBAR_INTXBAR5_G2	RW	502D 5248h
24Ch	16	CONTROLSS_INTXBAR_INTXBAR5_G3	RW	502D 524Ch
250h	16	CONTROLSS_INTXBAR_INTXBAR5_G4	RW	502D 5250h
254h	16	CONTROLSS_INTXBAR_INTXBAR5_G5	RW	502D 5254h
258h	8	CONTROLSS_INTXBAR_INTXBAR5_G6	RW	502D 5258h
280h	32	CONTROLSS_INTXBAR_INTXBAR6_G0	RW	502D 5280h
284h	32	CONTROLSS_INTXBAR_INTXBAR6_G1	RW	502D 5284h
288h	24	CONTROLSS_INTXBAR_INTXBAR6_G2	RW	502D 5288h
28Ch	16	CONTROLSS_INTXBAR_INTXBAR6_G3	RW	502D 528Ch
290h	16	CONTROLSS_INTXBAR_INTXBAR6_G4	RW	502D 5290h
294h	16	CONTROLSS_INTXBAR_INTXBAR6_G5	RW	502D 5294h
298h	8	CONTROLSS_INTXBAR_INTXBAR6_G6	RW	502D 5298h
2C0h	32	CONTROLSS_INTXBAR_INTXBAR7_G0	RW	502D 52C0h
2C4h	32	CONTROLSS_INTXBAR_INTXBAR7_G1	RW	502D 52C4h
2C8h	24	CONTROLSS_INTXBAR_INTXBAR7_G2	RW	502D 52C8h
2CCh	16	CONTROLSS_INTXBAR_INTXBAR7_G3	RW	502D 52CCh
2D0h	16	CONTROLSS_INTXBAR_INTXBAR7_G4	RW	502D 52D0h
2D4h	16	CONTROLSS_INTXBAR_INTXBAR7_G5	RW	502D 52D4h
2D8h	8	CONTROLSS_INTXBAR_INTXBAR7_G6	RW	502D 52D8h
300h	32	CONTROLSS_INTXBAR_INTXBAR8_G0	RW	502D 5300h
304h	32	CONTROLSS_INTXBAR_INTXBAR8_G1	RW	502D 5304h
308h	24	CONTROLSS_INTXBAR_INTXBAR8_G2	RW	502D 5308h
30Ch	16	CONTROLSS_INTXBAR_INTXBAR8_G3	RW	502D 530Ch
310h	16	CONTROLSS_INTXBAR_INTXBAR8_G4	RW	502D 5310h
314h	16	CONTROLSS_INTXBAR_INTXBAR8_G5	RW	502D 5314h
318h	8	CONTROLSS_INTXBAR_INTXBAR8_G6	RW	502D 5318h
340h	32	CONTROLSS_INTXBAR_INTXBAR9_G0	RW	502D 5340h
344h	32	CONTROLSS_INTXBAR_INTXBAR9_G1	RW	502D 5344h
348h	24	CONTROLSS_INTXBAR_INTXBAR9_G2	RW	502D 5348h
34Ch	16	CONTROLSS_INTXBAR_INTXBAR9_G3	RW	502D 534Ch
350h	16	CONTROLSS_INTXBAR_INTXBAR9_G4	RW	502D 5350h
354h	16	CONTROLSS_INTXBAR_INTXBAR9_G5	RW	502D 5354h
358h	8	CONTROLSS_INTXBAR_INTXBAR9_G6	RW	502D 5358h
380h	32	CONTROLSS_INTXBAR_INTXBAR10_G0	RW	502D 5380h
384h	32	CONTROLSS_INTXBAR_INTXBAR10_G1	RW	502D 5384h
388h	24	CONTROLSS_INTXBAR_INTXBAR10_G2	RW	502D 5388h
38Ch	16	CONTROLSS_INTXBAR_INTXBAR10_G3	RW	502D 538Ch
390h	16	CONTROLSS_INTXBAR_INTXBAR10_G4	RW	502D 5390h
394h	16	CONTROLSS_INTXBAR_INTXBAR10_G5	RW	502D 5394h
398h	8	CONTROLSS_INTXBAR_INTXBAR10_G6	RW	502D 5398h
3C0h	32	CONTROLSS_INTXBAR_INTXBAR11_G0	RW	502D 53C0h
3C4h	32	CONTROLSS_INTXBAR_INTXBAR11_G1	RW	502D 53C4h
3C8h	24	CONTROLSS_INTXBAR_INTXBAR11_G2	RW	502D 53C8h
3CCh	16	CONTROLSS_INTXBAR_INTXBAR11_G3	RW	502D 53CCh
3D0h	16	CONTROLSS_INTXBAR_INTXBAR11_G4	RW	502D 53D0h

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
3D4h	16	CONTROLSS_INTXBAR_INTXBAR11_G5	RW	502D 53D4h
3D8h	8	CONTROLSS_INTXBAR_INTXBAR11_G6	RW	502D 53D8h
400h	32	CONTROLSS_INTXBAR_INTXBAR12_G0	RW	502D 5400h
404h	32	CONTROLSS_INTXBAR_INTXBAR12_G1	RW	502D 5404h
408h	24	CONTROLSS_INTXBAR_INTXBAR12_G2	RW	502D 5408h
40Ch	16	CONTROLSS_INTXBAR_INTXBAR12_G3	RW	502D 540Ch
410h	16	CONTROLSS_INTXBAR_INTXBAR12_G4	RW	502D 5410h
414h	16	CONTROLSS_INTXBAR_INTXBAR12_G5	RW	502D 5414h
418h	8	CONTROLSS_INTXBAR_INTXBAR12_G6	RW	502D 5418h
440h	32	CONTROLSS_INTXBAR_INTXBAR13_G0	RW	502D 5440h
444h	32	CONTROLSS_INTXBAR_INTXBAR13_G1	RW	502D 5444h
448h	24	CONTROLSS_INTXBAR_INTXBAR13_G2	RW	502D 5448h
44Ch	16	CONTROLSS_INTXBAR_INTXBAR13_G3	RW	502D 544Ch
450h	16	CONTROLSS_INTXBAR_INTXBAR13_G4	RW	502D 5450h
454h	16	CONTROLSS_INTXBAR_INTXBAR13_G5	RW	502D 5454h
458h	8	CONTROLSS_INTXBAR_INTXBAR13_G6	RW	502D 5458h
480h	32	CONTROLSS_INTXBAR_INTXBAR14_G0	RW	502D 5480h
484h	32	CONTROLSS_INTXBAR_INTXBAR14_G1	RW	502D 5484h
488h	24	CONTROLSS_INTXBAR_INTXBAR14_G2	RW	502D 5488h
48Ch	16	CONTROLSS_INTXBAR_INTXBAR14_G3	RW	502D 548Ch
490h	16	CONTROLSS_INTXBAR_INTXBAR14_G4	RW	502D 5490h
494h	16	CONTROLSS_INTXBAR_INTXBAR14_G5	RW	502D 5494h
498h	8	CONTROLSS_INTXBAR_INTXBAR14_G6	RW	502D 5498h
4C0h	32	CONTROLSS_INTXBAR_INTXBAR15_G0	RW	502D 54C0h
4C4h	32	CONTROLSS_INTXBAR_INTXBAR15_G1	RW	502D 54C4h
4C8h	24	CONTROLSS_INTXBAR_INTXBAR15_G2	RW	502D 54C8h
4CCh	16	CONTROLSS_INTXBAR_INTXBAR15_G3	RW	502D 54CCh
4D0h	16	CONTROLSS_INTXBAR_INTXBAR15_G4	RW	502D 54D0h
4D4h	16	CONTROLSS_INTXBAR_INTXBAR15_G5	RW	502D 54D4h
4D8h	8	CONTROLSS_INTXBAR_INTXBAR15_G6	RW	502D 54D8h
500h	32	CONTROLSS_INTXBAR_INTXBAR16_G0	RW	502D 5500h
504h	32	CONTROLSS_INTXBAR_INTXBAR16_G1	RW	502D 5504h
508h	24	CONTROLSS_INTXBAR_INTXBAR16_G2	RW	502D 5508h
50Ch	16	CONTROLSS_INTXBAR_INTXBAR16_G3	RW	502D 550Ch
510h	16	CONTROLSS_INTXBAR_INTXBAR16_G4	RW	502D 5510h
514h	16	CONTROLSS_INTXBAR_INTXBAR16_G5	RW	502D 5514h
518h	8	CONTROLSS_INTXBAR_INTXBAR16_G6	RW	502D 5518h
540h	32	CONTROLSS_INTXBAR_INTXBAR17_G0	RW	502D 5540h
544h	32	CONTROLSS_INTXBAR_INTXBAR17_G1	RW	502D 5544h
548h	24	CONTROLSS_INTXBAR_INTXBAR17_G2	RW	502D 5548h
54Ch	16	CONTROLSS_INTXBAR_INTXBAR17_G3	RW	502D 554Ch
550h	16	CONTROLSS_INTXBAR_INTXBAR17_G4	RW	502D 5550h
554h	16	CONTROLSS_INTXBAR_INTXBAR17_G5	RW	502D 5554h
558h	8	CONTROLSS_INTXBAR_INTXBAR17_G6	RW	502D 5558h
580h	32	CONTROLSS_INTXBAR_INTXBAR18_G0	RW	502D 5580h

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
584h	32	CONTROLSS_INTXBAR_INTXBAR18_G1	RW	502D 5584h
588h	24	CONTROLSS_INTXBAR_INTXBAR18_G2	RW	502D 5588h
58Ch	16	CONTROLSS_INTXBAR_INTXBAR18_G3	RW	502D 558Ch
590h	16	CONTROLSS_INTXBAR_INTXBAR18_G4	RW	502D 5590h
594h	16	CONTROLSS_INTXBAR_INTXBAR18_G5	RW	502D 5594h
598h	8	CONTROLSS_INTXBAR_INTXBAR18_G6	RW	502D 5598h
5C0h	32	CONTROLSS_INTXBAR_INTXBAR19_G0	RW	502D 55C0h
5C4h	32	CONTROLSS_INTXBAR_INTXBAR19_G1	RW	502D 55C4h
5C8h	24	CONTROLSS_INTXBAR_INTXBAR19_G2	RW	502D 55C8h
5CCh	16	CONTROLSS_INTXBAR_INTXBAR19_G3	RW	502D 55CCh
5D0h	16	CONTROLSS_INTXBAR_INTXBAR19_G4	RW	502D 55D0h
5D4h	16	CONTROLSS_INTXBAR_INTXBAR19_G5	RW	502D 55D4h
5D8h	8	CONTROLSS_INTXBAR_INTXBAR19_G6	RW	502D 55D8h
600h	32	CONTROLSS_INTXBAR_INTXBAR20_G0	RW	502D 5600h
604h	32	CONTROLSS_INTXBAR_INTXBAR20_G1	RW	502D 5604h
608h	24	CONTROLSS_INTXBAR_INTXBAR20_G2	RW	502D 5608h
60Ch	16	CONTROLSS_INTXBAR_INTXBAR20_G3	RW	502D 560Ch
610h	16	CONTROLSS_INTXBAR_INTXBAR20_G4	RW	502D 5610h
614h	16	CONTROLSS_INTXBAR_INTXBAR20_G5	RW	502D 5614h
618h	8	CONTROLSS_INTXBAR_INTXBAR20_G6	RW	502D 5618h
640h	32	CONTROLSS_INTXBAR_INTXBAR21_G0	RW	502D 5640h
644h	32	CONTROLSS_INTXBAR_INTXBAR21_G1	RW	502D 5644h
648h	24	CONTROLSS_INTXBAR_INTXBAR21_G2	RW	502D 5648h
64Ch	16	CONTROLSS_INTXBAR_INTXBAR21_G3	RW	502D 564Ch
650h	16	CONTROLSS_INTXBAR_INTXBAR21_G4	RW	502D 5650h
654h	16	CONTROLSS_INTXBAR_INTXBAR21_G5	RW	502D 5654h
658h	8	CONTROLSS_INTXBAR_INTXBAR21_G6	RW	502D 5658h
680h	32	CONTROLSS_INTXBAR_INTXBAR22_G0	RW	502D 5680h
684h	32	CONTROLSS_INTXBAR_INTXBAR22_G1	RW	502D 5684h
688h	24	CONTROLSS_INTXBAR_INTXBAR22_G2	RW	502D 5688h
68Ch	16	CONTROLSS_INTXBAR_INTXBAR22_G3	RW	502D 568Ch
690h	16	CONTROLSS_INTXBAR_INTXBAR22_G4	RW	502D 5690h
694h	16	CONTROLSS_INTXBAR_INTXBAR22_G5	RW	502D 5694h
698h	8	CONTROLSS_INTXBAR_INTXBAR22_G6	RW	502D 5698h
6C0h	32	CONTROLSS_INTXBAR_INTXBAR23_G0	RW	502D 56C0h
6C4h	32	CONTROLSS_INTXBAR_INTXBAR23_G1	RW	502D 56C4h
6C8h	24	CONTROLSS_INTXBAR_INTXBAR23_G2	RW	502D 56C8h
6CCh	16	CONTROLSS_INTXBAR_INTXBAR23_G3	RW	502D 56CCh
6D0h	16	CONTROLSS_INTXBAR_INTXBAR23_G4	RW	502D 56D0h
6D4h	16	CONTROLSS_INTXBAR_INTXBAR23_G5	RW	502D 56D4h
6D8h	8	CONTROLSS_INTXBAR_INTXBAR23_G6	RW	502D 56D8h
700h	32	CONTROLSS_INTXBAR_INTXBAR24_G0	RW	502D 5700h
704h	32	CONTROLSS_INTXBAR_INTXBAR24_G1	RW	502D 5704h
708h	24	CONTROLSS_INTXBAR_INTXBAR24_G2	RW	502D 5708h
70Ch	16	CONTROLSS_INTXBAR_INTXBAR24_G3	RW	502D 570Ch

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
710h	16	CONTROLSS_INTXBAR_INTXBAR24_G4	RW	502D 5710h
714h	16	CONTROLSS_INTXBAR_INTXBAR24_G5	RW	502D 5714h
718h	8	CONTROLSS_INTXBAR_INTXBAR24_G6	RW	502D 5718h
740h	32	CONTROLSS_INTXBAR_INTXBAR25_G0	RW	502D 5740h
744h	32	CONTROLSS_INTXBAR_INTXBAR25_G1	RW	502D 5744h
748h	24	CONTROLSS_INTXBAR_INTXBAR25_G2	RW	502D 5748h
74Ch	16	CONTROLSS_INTXBAR_INTXBAR25_G3	RW	502D 574Ch
750h	16	CONTROLSS_INTXBAR_INTXBAR25_G4	RW	502D 5750h
754h	16	CONTROLSS_INTXBAR_INTXBAR25_G5	RW	502D 5754h
758h	8	CONTROLSS_INTXBAR_INTXBAR25_G6	RW	502D 5758h
780h	32	CONTROLSS_INTXBAR_INTXBAR26_G0	RW	502D 5780h
784h	32	CONTROLSS_INTXBAR_INTXBAR26_G1	RW	502D 5784h
788h	24	CONTROLSS_INTXBAR_INTXBAR26_G2	RW	502D 5788h
78Ch	16	CONTROLSS_INTXBAR_INTXBAR26_G3	RW	502D 578Ch
790h	16	CONTROLSS_INTXBAR_INTXBAR26_G4	RW	502D 5790h
794h	16	CONTROLSS_INTXBAR_INTXBAR26_G5	RW	502D 5794h
798h	8	CONTROLSS_INTXBAR_INTXBAR26_G6	RW	502D 5798h
7C0h	32	CONTROLSS_INTXBAR_INTXBAR27_G0	RW	502D 57C0h
7C4h	32	CONTROLSS_INTXBAR_INTXBAR27_G1	RW	502D 57C4h
7C8h	24	CONTROLSS_INTXBAR_INTXBAR27_G2	RW	502D 57C8h
7CCh	16	CONTROLSS_INTXBAR_INTXBAR27_G3	RW	502D 57CCh
7D0h	16	CONTROLSS_INTXBAR_INTXBAR27_G4	RW	502D 57D0h
7D4h	16	CONTROLSS_INTXBAR_INTXBAR27_G5	RW	502D 57D4h
7D8h	8	CONTROLSS_INTXBAR_INTXBAR27_G6	RW	502D 57D8h
800h	32	CONTROLSS_INTXBAR_INTXBAR28_G0	RW	502D 5800h
804h	32	CONTROLSS_INTXBAR_INTXBAR28_G1	RW	502D 5804h
808h	24	CONTROLSS_INTXBAR_INTXBAR28_G2	RW	502D 5808h
80Ch	16	CONTROLSS_INTXBAR_INTXBAR28_G3	RW	502D 580Ch
810h	16	CONTROLSS_INTXBAR_INTXBAR28_G4	RW	502D 5810h
814h	16	CONTROLSS_INTXBAR_INTXBAR28_G5	RW	502D 5814h
818h	8	CONTROLSS_INTXBAR_INTXBAR28_G6	RW	502D 5818h
840h	32	CONTROLSS_INTXBAR_INTXBAR29_G0	RW	502D 5840h
844h	32	CONTROLSS_INTXBAR_INTXBAR29_G1	RW	502D 5844h
848h	24	CONTROLSS_INTXBAR_INTXBAR29_G2	RW	502D 5848h
84Ch	16	CONTROLSS_INTXBAR_INTXBAR29_G3	RW	502D 584Ch
850h	16	CONTROLSS_INTXBAR_INTXBAR29_G4	RW	502D 5850h
854h	16	CONTROLSS_INTXBAR_INTXBAR29_G5	RW	502D 5854h
858h	8	CONTROLSS_INTXBAR_INTXBAR29_G6	RW	502D 5858h
880h	32	CONTROLSS_INTXBAR_INTXBAR30_G0	RW	502D 5880h
884h	32	CONTROLSS_INTXBAR_INTXBAR30_G1	RW	502D 5884h
888h	24	CONTROLSS_INTXBAR_INTXBAR30_G2	RW	502D 5888h
88Ch	16	CONTROLSS_INTXBAR_INTXBAR30_G3	RW	502D 588Ch
890h	16	CONTROLSS_INTXBAR_INTXBAR30_G4	RW	502D 5890h
894h	16	CONTROLSS_INTXBAR_INTXBAR30_G5	RW	502D 5894h
898h	8	CONTROLSS_INTXBAR_INTXBAR30_G6	RW	502D 5898h

Table 3-1283. CONTROLSS_INTXBAR, CONTROLSS_INTXBAR_CONTROLSS_INTXBAR Registers, Base Address=502D 5000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_INTXBAR Physical Address
8C0h	32	CONTROLSS_INTXBAR_INTXBAR31_G0	RW	502D 58C0h
8C4h	32	CONTROLSS_INTXBAR_INTXBAR31_G1	RW	502D 58C4h
8C8h	24	CONTROLSS_INTXBAR_INTXBAR31_G2	RW	502D 58C8h
8CCh	16	CONTROLSS_INTXBAR_INTXBAR31_G3	RW	502D 58CCh
8D0h	16	CONTROLSS_INTXBAR_INTXBAR31_G4	RW	502D 58D0h
8D4h	16	CONTROLSS_INTXBAR_INTXBAR31_G5	RW	502D 58D4h
8D8h	8	CONTROLSS_INTXBAR_INTXBAR31_G6	RW	502D 58D8h

3.13.1 CONTROLSS_INTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-1284. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5000h

Figure 3-621. CONTROLSS_INTXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-1285. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.13.2 CONTROLSS_INTXBAR_INTXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1286. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5100h

Figure 3-622. CONTROLSS_INTXBAR_INTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1287. INTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.3 CONTROLSS_INTXBAR_INTXBAR0_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1288. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5104h

Figure 3-623. CONTROLSS_INTXBAR_INTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1289. INTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.4 CONTROLSS_INTXBAR_INTXBAR0_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1290. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5108h

Figure 3-624. CONTROLSS_INTXBAR_INTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1291. INTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.5 CONTROLSS_INTXBAR_INTXBAR0_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1292. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 510Ch

Figure 3-625. CONTROLSS_INTXBAR_INTXBAR0_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1293. INTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.6 CONTROLSS_INTXBAR_INTXBAR0_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1294. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5110h

Figure 3-626. CONTROLSS_INTXBAR_INTXBAR0_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1295. INTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.7 CONTROLSS_INTXBAR_INTXBAR0_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1296. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5114h

Figure 3-627. CONTROLSS_INTXBAR_INTXBAR0_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1297. INTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.8 CONTROLSS_INTXBAR_INTXBAR0_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1298. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5118h

Figure 3-628. CONTROLSS_INTXBAR_INTXBAR0_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1299. INTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.9 CONTROLSS_INTXBAR_INTXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1300. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5140h

Figure 3-629. CONTROLSS_INTXBAR_INTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1301. INTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.10 CONTROLSS_INTXBAR_INTXBAR1_G1 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1302. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5144h

Figure 3-630. CONTROLSS_INTXBAR_INTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1303. INTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.11 CONTROLSS_INTXBAR_INTXBAR1_G2 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1304. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5148h

Figure 3-631. CONTROLSS_INTXBAR_INTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1305. INTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.12 CONTROLSS_INTXBAR_INTXBAR1_G3 Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1306. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 514Ch

Figure 3-632. CONTROLSS_INTXBAR_INTXBAR1_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1307. INTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.13 CONTROLSS_INTXBAR_INTXBAR1_G4 Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1308. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5150h

Figure 3-633. CONTROLSS_INTXBAR_INTXBAR1_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1309. INTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.14 CONTROLSS_INTXBAR_INTXBAR1_G5 Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1310. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5154h

Figure 3-634. CONTROLSS_INTXBAR_INTXBAR1_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1311. INTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.15 CONTROLSS_INTXBAR_INTXBAR1_G6 Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1312. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5158h

Figure 3-635. CONTROLSS_INTXBAR_INTXBAR1_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					SEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-1313. INTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.16 CONTROLSS_INTXBAR_INTXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1314. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5180h

Figure 3-636. CONTROLSS_INTXBAR_INTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1315. INTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.17 CONTROLSS_INTXBAR_INTXBAR2_G1 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1316. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5184h

Figure 3-637. CONTROLSS_INTXBAR_INTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1317. INTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.18 CONTROLSS_INTXBAR_INTXBAR2_G2 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1318. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5188h

Figure 3-638. CONTROLSS_INTXBAR_INTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1319. INTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.19 CONTROLSS_INTXBAR_INTXBAR2_G3 Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1320. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 518Ch

Figure 3-639. CONTROLSS_INTXBAR_INTXBAR2_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1321. INTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.20 CONTROLSS_INTXBAR_INTXBAR2_G4 Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1322. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5190h

Figure 3-640. CONTROLSS_INTXBAR_INTXBAR2_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1323. INTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.21 CONTROLSS_INTXBAR_INTXBAR2_G5 Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1324. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5194h

Figure 3-641. CONTROLSS_INTXBAR_INTXBAR2_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1325. INTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.22 CONTROLSS_INTXBAR_INTXBAR2_G6 Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1326. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5198h

Figure 3-642. CONTROLSS_INTXBAR_INTXBAR2_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1327. INTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.23 CONTROLSS_INTXBAR_INTXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1328. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C0h

Figure 3-643. CONTROLSS_INTXBAR_INTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1329. INTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.24 CONTROLSS_INTXBAR_INTXBAR3_G1 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1330. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C4h

Figure 3-644. CONTROLSS_INTXBAR_INTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1331. INTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.25 CONTROLSS_INTXBAR_INTXBAR3_G2 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1332. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C8h

Figure 3-645. CONTROLSS_INTXBAR_INTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1333. INTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.26 CONTROLSS_INTXBAR_INTXBAR3_G3 Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1334. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51CCh

Figure 3-646. CONTROLSS_INTXBAR_INTXBAR3_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1335. INTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.27 CONTROLSS_INTXBAR_INTXBAR3_G4 Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1336. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D0h

Figure 3-647. CONTROLSS_INTXBAR_INTXBAR3_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1337. INTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.28 CONTROLSS_INTXBAR_INTXBAR3_G5 Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1338. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D4h

Figure 3-648. CONTROLSS_INTXBAR_INTXBAR3_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1339. INTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.29 CONTROLSS_INTXBAR_INTXBAR3_G6 Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1340. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D8h

Figure 3-649. CONTROLSS_INTXBAR_INTXBAR3_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1341. INTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.30 CONTROLSS_INTXBAR_INTXBAR4_G0 Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1342. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5200h

Figure 3-650. CONTROLSS_INTXBAR_INTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1343. INTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.31 CONTROLSS_INTXBAR_INTXBAR4_G1 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1344. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5204h

Figure 3-651. CONTROLSS_INTXBAR_INTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1345. INTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.32 CONTROLSS_INTXBAR_INTXBAR4_G2 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1346. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5208h

Figure 3-652. CONTROLSS_INTXBAR_INTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1347. INTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.33 CONTROLSS_INTXBAR_INTXBAR4_G3 Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1348. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 520Ch

Figure 3-653. CONTROLSS_INTXBAR_INTXBAR4_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1349. INTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.34 CONTROLSS_INTXBAR_INTXBAR4_G4 Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1350. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5210h

Figure 3-654. CONTROLSS_INTXBAR_INTXBAR4_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1351. INTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.35 CONTROLSS_INTXBAR_INTXBAR4_G5 Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1352. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5214h

Figure 3-655. CONTROLSS_INTXBAR_INTXBAR4_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1353. INTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.36 CONTROLSS_INTXBAR_INTXBAR4_G6 Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1354. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5218h

Figure 3-656. CONTROLSS_INTXBAR_INTXBAR4_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1355. INTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.37 CONTROLSS_INTXBAR_INTXBAR5_G0 Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1356. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5240h

Figure 3-657. CONTROLSS_INTXBAR_INTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1357. INTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.38 CONTROLSS_INTXBAR_INTXBAR5_G1 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1358. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5244h

Figure 3-658. CONTROLSS_INTXBAR_INTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1359. INTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.39 CONTROLSS_INTXBAR_INTXBAR5_G2 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1360. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5248h

Figure 3-659. CONTROLSS_INTXBAR_INTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1361. INTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.40 CONTROLSS_INTXBAR_INTXBAR5_G3 Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1362. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 524Ch

Figure 3-660. CONTROLSS_INTXBAR_INTXBAR5_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1363. INTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.41 CONTROLSS_INTXBAR_INTXBAR5_G4 Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1364. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5250h

Figure 3-661. CONTROLSS_INTXBAR_INTXBAR5_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1365. INTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.42 CONTROLSS_INTXBAR_INTXBAR5_G5 Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1366. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5254h

Figure 3-662. CONTROLSS_INTXBAR_INTXBAR5_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1367. INTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.43 CONTROLSS_INTXBAR_INTXBAR5_G6 Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1368. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5258h

Figure 3-663. CONTROLSS_INTXBAR_INTXBAR5_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1369. INTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.44 CONTROLSS_INTXBAR_INTXBAR6_G0 Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1370. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5280h

Figure 3-664. CONTROLSS_INTXBAR_INTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1371. INTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.45 CONTROLSS_INTXBAR_INTXBAR6_G1 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1372. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5284h

Figure 3-665. CONTROLSS_INTXBAR_INTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1373. INTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.46 CONTROLSS_INTXBAR_INTXBAR6_G2 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1374. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5288h

Figure 3-666. CONTROLSS_INTXBAR_INTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1375. INTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.47 CONTROLSS_INTXBAR_INTXBAR6_G3 Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1376. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 528Ch

Figure 3-667. CONTROLSS_INTXBAR_INTXBAR6_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1377. INTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.48 CONTROLSS_INTXBAR_INTXBAR6_G4 Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1378. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5290h

Figure 3-668. CONTROLSS_INTXBAR_INTXBAR6_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1379. INTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.49 CONTROLSS_INTXBAR_INTXBAR6_G5 Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1380. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5294h

Figure 3-669. CONTROLSS_INTXBAR_INTXBAR6_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1381. INTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.50 CONTROLSS_INTXBAR_INTXBAR6_G6 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1382. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5298h

Figure 3-670. CONTROLSS_INTXBAR_INTXBAR6_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1383. INTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.51 CONTROLSS_INTXBAR_INTXBAR7_G0 Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1384. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C0h

Figure 3-671. CONTROLSS_INTXBAR_INTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1385. INTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.52 CONTROLSS_INTXBAR_INTXBAR7_G1 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1386. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C4h

Figure 3-672. CONTROLSS_INTXBAR_INTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1387. INTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.53 CONTROLSS_INTXBAR_INTXBAR7_G2 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1388. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C8h

Figure 3-673. CONTROLSS_INTXBAR_INTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1389. INTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.54 CONTROLSS_INTXBAR_INTXBAR7_G3 Register (Offset = 2CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1390. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52CCh

Figure 3-674. CONTROLSS_INTXBAR_INTXBAR7_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1391. INTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.55 CONTROLSS_INTXBAR_INTXBAR7_G4 Register (Offset = 2D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1392. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D0h

Figure 3-675. CONTROLSS_INTXBAR_INTXBAR7_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1393. INTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.56 CONTROLSS_INTXBAR_INTXBAR7_G5 Register (Offset = 2D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1394. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D4h

Figure 3-676. CONTROLSS_INTXBAR_INTXBAR7_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1395. INTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.57 CONTROLSS_INTXBAR_INTXBAR7_G6 Register (Offset = 2D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1396. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D8h

Figure 3-677. CONTROLSS_INTXBAR_INTXBAR7_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1397. INTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.58 CONTROLSS_INTXBAR_INTXBAR8_G0 Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1398. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5300h

Figure 3-678. CONTROLSS_INTXBAR_INTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1399. INTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.59 CONTROLSS_INTXBAR_INTXBAR8_G1 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1400. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5304h

Figure 3-679. CONTROLSS_INTXBAR_INTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1401. INTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.60 CONTROLSS_INTXBAR_INTXBAR8_G2 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1402. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5308h

Figure 3-680. CONTROLSS_INTXBAR_INTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1403. INTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.61 CONTROLSS_INTXBAR_INTXBAR8_G3 Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1404. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 530Ch

Figure 3-681. CONTROLSS_INTXBAR_INTXBAR8_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1405. INTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.62 CONTROLSS_INTXBAR_INTXBAR8_G4 Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1406. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5310h

Figure 3-682. CONTROLSS_INTXBAR_INTXBAR8_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1407. INTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.63 CONTROLSS_INTXBAR_INTXBAR8_G5 Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1408. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5314h

Figure 3-683. CONTROLSS_INTXBAR_INTXBAR8_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1409. INTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.64 CONTROLSS_INTXBAR_INTXBAR8_G6 Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1410. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5318h

Figure 3-684. CONTROLSS_INTXBAR_INTXBAR8_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1411. INTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.65 CONTROLSS_INTXBAR_INTXBAR9_G0 Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1412. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5340h

Figure 3-685. CONTROLSS_INTXBAR_INTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1413. INTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.66 CONTROLSS_INTXBAR_INTXBAR9_G1 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1414. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5344h

Figure 3-686. CONTROLSS_INTXBAR_INTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1415. INTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.67 CONTROLSS_INTXBAR_INTXBAR9_G2 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1416. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5348h

Figure 3-687. CONTROLSS_INTXBAR_INTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1417. INTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.68 CONTROLSS_INTXBAR_INTXBAR9_G3 Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1418. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 534Ch

Figure 3-688. CONTROLSS_INTXBAR_INTXBAR9_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1419. INTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.69 CONTROLSS_INTXBAR_INTXBAR9_G4 Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1420. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5350h

Figure 3-689. CONTROLSS_INTXBAR_INTXBAR9_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1421. INTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.70 CONTROLSS_INTXBAR_INTXBAR9_G5 Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1422. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5354h

Figure 3-690. CONTROLSS_INTXBAR_INTXBAR9_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1423. INTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.71 CONTROLSS_INTXBAR_INTXBAR9_G6 Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1424. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5358h

Figure 3-691. CONTROLSS_INTXBAR_INTXBAR9_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1425. INTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.72 CONTROLSS_INTXBAR_INTXBAR10_G0 Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1426. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5380h

Figure 3-692. CONTROLSS_INTXBAR_INTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1427. INTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.73 CONTROLSS_INTXBAR_INTXBAR10_G1 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1428. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5384h

Figure 3-693. CONTROLSS_INTXBAR_INTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1429. INTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.74 CONTROLSS_INTXBAR_INTXBAR10_G2 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1430. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5388h

Figure 3-694. CONTROLSS_INTXBAR_INTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1431. INTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.75 CONTROLSS_INTXBAR_INTXBAR10_G3 Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1432. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 538Ch

Figure 3-695. CONTROLSS_INTXBAR_INTXBAR10_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1433. INTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.76 CONTROLSS_INTXBAR_INTXBAR10_G4 Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1434. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5390h

Figure 3-696. CONTROLSS_INTXBAR_INTXBAR10_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1435. INTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.77 CONTROLSS_INTXBAR_INTXBAR10_G5 Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1436. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5394h

Figure 3-697. CONTROLSS_INTXBAR_INTXBAR10_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1437. INTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.78 CONTROLSS_INTXBAR_INTXBAR10_G6 Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1438. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5398h

Figure 3-698. CONTROLSS_INTXBAR_INTXBAR10_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1439. INTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.79 CONTROLSS_INTXBAR_INTXBAR11_G0 Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1440. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C0h

Figure 3-699. CONTROLSS_INTXBAR_INTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1441. INTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.80 CONTROLSS_INTXBAR_INTXBAR11_G1 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1442. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C4h

Figure 3-700. CONTROLSS_INTXBAR_INTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1443. INTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.81 CONTROLSS_INTXBAR_INTXBAR11_G2 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1444. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C8h

Figure 3-701. CONTROLSS_INTXBAR_INTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1445. INTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.82 CONTROLSS_INTXBAR_INTXBAR11_G3 Register (Offset = 3CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1446. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53CCh

Figure 3-702. CONTROLSS_INTXBAR_INTXBAR11_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1447. INTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.83 CONTROLSS_INTXBAR_INTXBAR11_G4 Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1448. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D0h

Figure 3-703. CONTROLSS_INTXBAR_INTXBAR11_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1449. INTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.84 CONTROLSS_INTXBAR_INTXBAR11_G5 Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1450. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D4h

Figure 3-704. CONTROLSS_INTXBAR_INTXBAR11_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1451. INTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.85 CONTROLSS_INTXBAR_INTXBAR11_G6 Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1452. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D8h

Figure 3-705. CONTROLSS_INTXBAR_INTXBAR11_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1453. INTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.86 CONTROLSS_INTXBAR_INTXBAR12_G0 Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1454. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5400h

Figure 3-706. CONTROLSS_INTXBAR_INTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1455. INTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.87 CONTROLSS_INTXBAR_INTXBAR12_G1 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1456. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5404h

Figure 3-707. CONTROLSS_INTXBAR_INTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1457. INTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.88 CONTROLSS_INTXBAR_INTXBAR12_G2 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1458. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5408h

Figure 3-708. CONTROLSS_INTXBAR_INTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1459. INTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.89 CONTROLSS_INTXBAR_INTXBAR12_G3 Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1460. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 540Ch

Figure 3-709. CONTROLSS_INTXBAR_INTXBAR12_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1461. INTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.90 CONTROLSS_INTXBAR_INTXBAR12_G4 Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1462. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5410h

Figure 3-710. CONTROLSS_INTXBAR_INTXBAR12_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1463. INTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.91 CONTROLSS_INTXBAR_INTXBAR12_G5 Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1464. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5414h

Figure 3-711. CONTROLSS_INTXBAR_INTXBAR12_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1465. INTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.92 CONTROLSS_INTXBAR_INTXBAR12_G6 Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1466. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5418h

Figure 3-712. CONTROLSS_INTXBAR_INTXBAR12_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1467. INTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.93 CONTROLSS_INTXBAR_INTXBAR13_G0 Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1468. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5440h

Figure 3-713. CONTROLSS_INTXBAR_INTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1469. INTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.94 CONTROLSS_INTXBAR_INTXBAR13_G1 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1470. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5444h

Figure 3-714. CONTROLSS_INTXBAR_INTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1471. INTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.95 CONTROLSS_INTXBAR_INTXBAR13_G2 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1472. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5448h

Figure 3-715. CONTROLSS_INTXBAR_INTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1473. INTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.96 CONTROLSS_INTXBAR_INTXBAR13_G3 Register (Offset = 44Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1474. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 544Ch

Figure 3-716. CONTROLSS_INTXBAR_INTXBAR13_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1475. INTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.97 CONTROLSS_INTXBAR_INTXBAR13_G4 Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1476. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5450h

Figure 3-717. CONTROLSS_INTXBAR_INTXBAR13_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1477. INTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.98 CONTROLSS_INTXBAR_INTXBAR13_G5 Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1478. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5454h

Figure 3-718. CONTROLSS_INTXBAR_INTXBAR13_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1479. INTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.99 CONTROLSS_INTXBAR_INTXBAR13_G6 Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1480. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5458h

Figure 3-719. CONTROLSS_INTXBAR_INTXBAR13_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1481. INTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.100 CONTROLSS_INTXBAR_INTXBAR14_G0 Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1482. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5480h

Figure 3-720. CONTROLSS_INTXBAR_INTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1483. INTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.101 CONTROLSS_INTXBAR_INTXBAR14_G1 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1484. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5484h

Figure 3-721. CONTROLSS_INTXBAR_INTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1485. INTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.102 CONTROLSS_INTXBAR_INTXBAR14_G2 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1486. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5488h

Figure 3-722. CONTROLSS_INTXBAR_INTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1487. INTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.103 CONTROLSS_INTXBAR_INTXBAR14_G3 Register (Offset = 48Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1488. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 548Ch

Figure 3-723. CONTROLSS_INTXBAR_INTXBAR14_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1489. INTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.104 CONTROLSS_INTXBAR_INTXBAR14_G4 Register (Offset = 490h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1490. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5490h

Figure 3-724. CONTROLSS_INTXBAR_INTXBAR14_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1491. INTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.105 CONTROLSS_INTXBAR_INTXBAR14_G5 Register (Offset = 494h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1492. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5494h

Figure 3-725. CONTROLSS_INTXBAR_INTXBAR14_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1493. INTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.106 CONTROLSS_INTXBAR_INTXBAR14_G6 Register (Offset = 498h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1494. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5498h

Figure 3-726. CONTROLSS_INTXBAR_INTXBAR14_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1495. INTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.107 CONTROLSS_INTXBAR_INTXBAR15_G0 Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1496. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C0h

Figure 3-727. CONTROLSS_INTXBAR_INTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1497. INTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.108 CONTROLSS_INTXBAR_INTXBAR15_G1 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1498. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C4h

Figure 3-728. CONTROLSS_INTXBAR_INTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1499. INTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.109 CONTROLSS_INTXBAR_INTXBAR15_G2 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1500. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C8h

Figure 3-729. CONTROLSS_INTXBAR_INTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1501. INTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.110 CONTROLSS_INTXBAR_INTXBAR15_G3 Register (Offset = 4CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1502. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54CCh

Figure 3-730. CONTROLSS_INTXBAR_INTXBAR15_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1503. INTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.111 CONTROLSS_INTXBAR_INTXBAR15_G4 Register (Offset = 4D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1504. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D0h

Figure 3-731. CONTROLSS_INTXBAR_INTXBAR15_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1505. INTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.112 CONTROLSS_INTXBAR_INTXBAR15_G5 Register (Offset = 4D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1506. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D4h

Figure 3-732. CONTROLSS_INTXBAR_INTXBAR15_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1507. INTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.113 CONTROLSS_INTXBAR_INTXBAR15_G6 Register (Offset = 4D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1508. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D8h

Figure 3-733. CONTROLSS_INTXBAR_INTXBAR15_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1509. INTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.114 CONTROLSS_INTXBAR_INTXBAR16_G0 Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1510. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5500h

Figure 3-734. CONTROLSS_INTXBAR_INTXBAR16_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1511. INTXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.115 CONTROLSS_INTXBAR_INTXBAR16_G1 Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1512. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5504h

Figure 3-735. CONTROLSS_INTXBAR_INTXBAR16_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1513. INTXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.116 CONTROLSS_INTXBAR_INTXBAR16_G2 Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1514. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5508h

Figure 3-736. CONTROLSS_INTXBAR_INTXBAR16_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1515. INTXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.117 CONTROLSS_INTXBAR_INTXBAR16_G3 Register (Offset = 50Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1516. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 550Ch

Figure 3-737. CONTROLSS_INTXBAR_INTXBAR16_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1517. INTXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.118 CONTROLSS_INTXBAR_INTXBAR16_G4 Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1518. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5510h

Figure 3-738. CONTROLSS_INTXBAR_INTXBAR16_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1519. INTXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.119 CONTROLSS_INTXBAR_INTXBAR16_G5 Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1520. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5514h

Figure 3-739. CONTROLSS_INTXBAR_INTXBAR16_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1521. INTXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.120 CONTROLSS_INTXBAR_INTXBAR16_G6 Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1522. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5518h

Figure 3-740. CONTROLSS_INTXBAR_INTXBAR16_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1523. INTXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.121 CONTROLSS_INTXBAR_INTXBAR17_G0 Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1524. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5540h

Figure 3-741. CONTROLSS_INTXBAR_INTXBAR17_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1525. INTXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.122 CONTROLSS_INTXBAR_INTXBAR17_G1 Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1526. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5544h

Figure 3-742. CONTROLSS_INTXBAR_INTXBAR17_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1527. INTXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.123 CONTROLSS_INTXBAR_INTXBAR17_G2 Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1528. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5548h

Figure 3-743. CONTROLSS_INTXBAR_INTXBAR17_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1529. INTXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.124 CONTROLSS_INTXBAR_INTXBAR17_G3 Register (Offset = 54Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1530. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 554Ch

Figure 3-744. CONTROLSS_INTXBAR_INTXBAR17_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1531. INTXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.125 CONTROLSS_INTXBAR_INTXBAR17_G4 Register (Offset = 550h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1532. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5550h

Figure 3-745. CONTROLSS_INTXBAR_INTXBAR17_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1533. INTXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.126 CONTROLSS_INTXBAR_INTXBAR17_G5 Register (Offset = 554h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1534. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5554h

Figure 3-746. CONTROLSS_INTXBAR_INTXBAR17_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1535. INTXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.127 CONTROLSS_INTXBAR_INTXBAR17_G6 Register (Offset = 558h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1536. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5558h

Figure 3-747. CONTROLSS_INTXBAR_INTXBAR17_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1537. INTXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.128 CONTROLSS_INTXBAR_INTXBAR18_G0 Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1538. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5580h

Figure 3-748. CONTROLSS_INTXBAR_INTXBAR18_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1539. INTXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.129 CONTROLSS_INTXBAR_INTXBAR18_G1 Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1540. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5584h

Figure 3-749. CONTROLSS_INTXBAR_INTXBAR18_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1541. INTXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.130 CONTROLSS_INTXBAR_INTXBAR18_G2 Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1542. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5588h

Figure 3-750. CONTROLSS_INTXBAR_INTXBAR18_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1543. INTXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.131 CONTROLSS_INTXBAR_INTXBAR18_G3 Register (Offset = 58Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1544. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 558Ch

Figure 3-751. CONTROLSS_INTXBAR_INTXBAR18_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1545. INTXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.132 CONTROLSS_INTXBAR_INTXBAR18_G4 Register (Offset = 590h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1546. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5590h

Figure 3-752. CONTROLSS_INTXBAR_INTXBAR18_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1547. INTXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.133 CONTROLSS_INTXBAR_INTXBAR18_G5 Register (Offset = 594h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1548. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5594h

Figure 3-753. CONTROLSS_INTXBAR_INTXBAR18_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1549. INTXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.134 CONTROLSS_INTXBAR_INTXBAR18_G6 Register (Offset = 598h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1550. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5598h

Figure 3-754. CONTROLSS_INTXBAR_INTXBAR18_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1551. INTXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.135 CONTROLSS_INTXBAR_INTXBAR19_G0 Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1552. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C0h

Figure 3-755. CONTROLSS_INTXBAR_INTXBAR19_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1553. INTXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.136 CONTROLSS_INTXBAR_INTXBAR19_G1 Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1554. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C4h

Figure 3-756. CONTROLSS_INTXBAR_INTXBAR19_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1555. INTXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.137 CONTROLSS_INTXBAR_INTXBAR19_G2 Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1556. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C8h

Figure 3-757. CONTROLSS_INTXBAR_INTXBAR19_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1557. INTXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.138 CONTROLSS_INTXBAR_INTXBAR19_G3 Register (Offset = 5CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1558. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55CCh

Figure 3-758. CONTROLSS_INTXBAR_INTXBAR19_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1559. INTXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.139 CONTROLSS_INTXBAR_INTXBAR19_G4 Register (Offset = 5D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1560. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D0h

Figure 3-759. CONTROLSS_INTXBAR_INTXBAR19_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1561. INTXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.140 CONTROLSS_INTXBAR_INTXBAR19_G5 Register (Offset = 5D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1562. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D4h

Figure 3-760. CONTROLSS_INTXBAR_INTXBAR19_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1563. INTXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.141 CONTROLSS_INTXBAR_INTXBAR19_G6 Register (Offset = 5D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1564. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D8h

Figure 3-761. CONTROLSS_INTXBAR_INTXBAR19_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1565. INTXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.142 CONTROLSS_INTXBAR_INTXBAR20_G0 Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1566. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5600h

Figure 3-762. CONTROLSS_INTXBAR_INTXBAR20_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1567. INTXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.143 CONTROLSS_INTXBAR_INTXBAR20_G1 Register (Offset = 604h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1568. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5604h

Figure 3-763. CONTROLSS_INTXBAR_INTXBAR20_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1569. INTXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.144 CONTROLSS_INTXBAR_INTXBAR20_G2 Register (Offset = 608h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1570. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5608h

Figure 3-764. CONTROLSS_INTXBAR_INTXBAR20_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1571. INTXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.145 CONTROLSS_INTXBAR_INTXBAR20_G3 Register (Offset = 60Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1572. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 560Ch

Figure 3-765. CONTROLSS_INTXBAR_INTXBAR20_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1573. INTXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.146 CONTROLSS_INTXBAR_INTXBAR20_G4 Register (Offset = 610h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1574. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5610h

Figure 3-766. CONTROLSS_INTXBAR_INTXBAR20_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1575. INTXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.147 CONTROLSS_INTXBAR_INTXBAR20_G5 Register (Offset = 614h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1576. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5614h

Figure 3-767. CONTROLSS_INTXBAR_INTXBAR20_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1577. INTXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.148 CONTROLSS_INTXBAR_INTXBAR20_G6 Register (Offset = 618h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1578. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5618h

Figure 3-768. CONTROLSS_INTXBAR_INTXBAR20_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1579. INTXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.149 CONTROLSS_INTXBAR_INTXBAR21_G0 Register (Offset = 640h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1580. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5640h

Figure 3-769. CONTROLSS_INTXBAR_INTXBAR21_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1581. INTXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.150 CONTROLSS_INTXBAR_INTXBAR21_G1 Register (Offset = 644h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1582. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5644h

Figure 3-770. CONTROLSS_INTXBAR_INTXBAR21_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1583. INTXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.151 CONTROLSS_INTXBAR_INTXBAR21_G2 Register (Offset = 648h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1584. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5648h

Figure 3-771. CONTROLSS_INTXBAR_INTXBAR21_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1585. INTXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.152 CONTROLSS_INTXBAR_INTXBAR21_G3 Register (Offset = 64Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1586. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 564Ch

Figure 3-772. CONTROLSS_INTXBAR_INTXBAR21_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1587. INTXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.153 CONTROLSS_INTXBAR_INTXBAR21_G4 Register (Offset = 650h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1588. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5650h

Figure 3-773. CONTROLSS_INTXBAR_INTXBAR21_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1589. INTXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.154 CONTROLSS_INTXBAR_INTXBAR21_G5 Register (Offset = 654h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1590. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5654h

Figure 3-774. CONTROLSS_INTXBAR_INTXBAR21_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1591. INTXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.155 CONTROLSS_INTXBAR_INTXBAR21_G6 Register (Offset = 658h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1592. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5658h

Figure 3-775. CONTROLSS_INTXBAR_INTXBAR21_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1593. INTXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.156 CONTROLSS_INTXBAR_INTXBAR22_G0 Register (Offset = 680h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1594. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5680h

Figure 3-776. CONTROLSS_INTXBAR_INTXBAR22_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1595. INTXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.157 CONTROLSS_INTXBAR_INTXBAR22_G1 Register (Offset = 684h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1596. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5684h

Figure 3-777. CONTROLSS_INTXBAR_INTXBAR22_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1597. INTXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.158 CONTROLSS_INTXBAR_INTXBAR22_G2 Register (Offset = 688h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1598. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5688h

Figure 3-778. CONTROLSS_INTXBAR_INTXBAR22_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1599. INTXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.159 CONTROLSS_INTXBAR_INTXBAR22_G3 Register (Offset = 68Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1600. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 568Ch

Figure 3-779. CONTROLSS_INTXBAR_INTXBAR22_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1601. INTXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.160 CONTROLSS_INTXBAR_INTXBAR22_G4 Register (Offset = 690h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1602. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5690h

Figure 3-780. CONTROLSS_INTXBAR_INTXBAR22_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1603. INTXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.161 CONTROLSS_INTXBAR_INTXBAR22_G5 Register (Offset = 694h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1604. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5694h

Figure 3-781. CONTROLSS_INTXBAR_INTXBAR22_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1605. INTXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.162 CONTROLSS_INTXBAR_INTXBAR22_G6 Register (Offset = 698h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1606. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5698h

Figure 3-782. CONTROLSS_INTXBAR_INTXBAR22_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1607. INTXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.163 CONTROLSS_INTXBAR_INTXBAR23_G0 Register (Offset = 6C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1608. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C0h

Figure 3-783. CONTROLSS_INTXBAR_INTXBAR23_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1609. INTXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.164 CONTROLSS_INTXBAR_INTXBAR23_G1 Register (Offset = 6C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1610. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C4h

Figure 3-784. CONTROLSS_INTXBAR_INTXBAR23_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1611. INTXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.165 CONTROLSS_INTXBAR_INTXBAR23_G2 Register (Offset = 6C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1612. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C8h

Figure 3-785. CONTROLSS_INTXBAR_INTXBAR23_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1613. INTXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.166 CONTROLSS_INTXBAR_INTXBAR23_G3 Register (Offset = 6CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1614. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56CCh

Figure 3-786. CONTROLSS_INTXBAR_INTXBAR23_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1615. INTXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.167 CONTROLSS_INTXBAR_INTXBAR23_G4 Register (Offset = 6D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1616. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D0h

Figure 3-787. CONTROLSS_INTXBAR_INTXBAR23_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1617. INTXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.168 CONTROLSS_INTXBAR_INTXBAR23_G5 Register (Offset = 6D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1618. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D4h

Figure 3-788. CONTROLSS_INTXBAR_INTXBAR23_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1619. INTXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.169 CONTROLSS_INTXBAR_INTXBAR23_G6 Register (Offset = 6D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1620. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D8h

Figure 3-789. CONTROLSS_INTXBAR_INTXBAR23_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1621. INTXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.170 CONTROLSS_INTXBAR_INTXBAR24_G0 Register (Offset = 700h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1622. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5700h

Figure 3-790. CONTROLSS_INTXBAR_INTXBAR24_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1623. INTXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.171 CONTROLSS_INTXBAR_INTXBAR24_G1 Register (Offset = 704h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1624. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5704h

Figure 3-791. CONTROLSS_INTXBAR_INTXBAR24_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1625. INTXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.172 CONTROLSS_INTXBAR_INTXBAR24_G2 Register (Offset = 708h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1626. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5708h

Figure 3-792. CONTROLSS_INTXBAR_INTXBAR24_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1627. INTXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.173 CONTROLSS_INTXBAR_INTXBAR24_G3 Register (Offset = 70Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1628. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 570Ch

Figure 3-793. CONTROLSS_INTXBAR_INTXBAR24_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1629. INTXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.174 CONTROLSS_INTXBAR_INTXBAR24_G4 Register (Offset = 710h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1630. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5710h

Figure 3-794. CONTROLSS_INTXBAR_INTXBAR24_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1631. INTXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.175 CONTROLSS_INTXBAR_INTXBAR24_G5 Register (Offset = 714h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1632. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5714h

Figure 3-795. CONTROLSS_INTXBAR_INTXBAR24_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1633. INTXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.176 CONTROLSS_INTXBAR_INTXBAR24_G6 Register (Offset = 718h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1634. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5718h

Figure 3-796. CONTROLSS_INTXBAR_INTXBAR24_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1635. INTXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.177 CONTROLSS_INTXBAR_INTXBAR25_G0 Register (Offset = 740h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1636. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5740h

Figure 3-797. CONTROLSS_INTXBAR_INTXBAR25_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1637. INTXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.178 CONTROLSS_INTXBAR_INTXBAR25_G1 Register (Offset = 744h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1638. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5744h

Figure 3-798. CONTROLSS_INTXBAR_INTXBAR25_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1639. INTXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.179 CONTROLSS_INTXBAR_INTXBAR25_G2 Register (Offset = 748h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1640. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5748h

Figure 3-799. CONTROLSS_INTXBAR_INTXBAR25_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1641. INTXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.180 CONTROLSS_INTXBAR_INTXBAR25_G3 Register (Offset = 74Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1642. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 574Ch

Figure 3-800. CONTROLSS_INTXBAR_INTXBAR25_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1643. INTXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.181 CONTROLSS_INTXBAR_INTXBAR25_G4 Register (Offset = 750h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1644. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5750h

Figure 3-801. CONTROLSS_INTXBAR_INTXBAR25_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1645. INTXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.182 CONTROLSS_INTXBAR_INTXBAR25_G5 Register (Offset = 754h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1646. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5754h

Figure 3-802. CONTROLSS_INTXBAR_INTXBAR25_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1647. INTXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.183 CONTROLSS_INTXBAR_INTXBAR25_G6 Register (Offset = 758h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1648. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5758h

Figure 3-803. CONTROLSS_INTXBAR_INTXBAR25_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					SEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-1649. INTXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.184 CONTROLSS_INTXBAR_INTXBAR26_G0 Register (Offset = 780h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1650. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5780h

Figure 3-804. CONTROLSS_INTXBAR_INTXBAR26_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1651. INTXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.185 CONTROLSS_INTXBAR_INTXBAR26_G1 Register (Offset = 784h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1652. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5784h

Figure 3-805. CONTROLSS_INTXBAR_INTXBAR26_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1653. INTXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.186 CONTROLSS_INTXBAR_INTXBAR26_G2 Register (Offset = 788h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1654. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5788h

Figure 3-806. CONTROLSS_INTXBAR_INTXBAR26_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1655. INTXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.187 CONTROLSS_INTXBAR_INTXBAR26_G3 Register (Offset = 78Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1656. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 578Ch

Figure 3-807. CONTROLSS_INTXBAR_INTXBAR26_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1657. INTXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.188 CONTROLSS_INTXBAR_INTXBAR26_G4 Register (Offset = 790h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1658. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5790h

Figure 3-808. CONTROLSS_INTXBAR_INTXBAR26_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1659. INTXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.189 CONTROLSS_INTXBAR_INTXBAR26_G5 Register (Offset = 794h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1660. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5794h

Figure 3-809. CONTROLSS_INTXBAR_INTXBAR26_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1661. INTXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.190 CONTROLSS_INTXBAR_INTXBAR26_G6 Register (Offset = 798h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1662. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5798h

Figure 3-810. CONTROLSS_INTXBAR_INTXBAR26_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1663. INTXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.191 CONTROLSS_INTXBAR_INTXBAR27_G0 Register (Offset = 7C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1664. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C0h

Figure 3-811. CONTROLSS_INTXBAR_INTXBAR27_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1665. INTXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.192 CONTROLSS_INTXBAR_INTXBAR27_G1 Register (Offset = 7C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1666. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C4h

Figure 3-812. CONTROLSS_INTXBAR_INTXBAR27_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1667. INTXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.193 CONTROLSS_INTXBAR_INTXBAR27_G2 Register (Offset = 7C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1668. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C8h

Figure 3-813. CONTROLSS_INTXBAR_INTXBAR27_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1669. INTXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.194 CONTROLSS_INTXBAR_INTXBAR27_G3 Register (Offset = 7CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1670. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57CCh

Figure 3-814. CONTROLSS_INTXBAR_INTXBAR27_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1671. INTXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.195 CONTROLSS_INTXBAR_INTXBAR27_G4 Register (Offset = 7D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1672. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D0h

Figure 3-815. CONTROLSS_INTXBAR_INTXBAR27_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1673. INTXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.196 CONTROLSS_INTXBAR_INTXBAR27_G5 Register (Offset = 7D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1674. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D4h

Figure 3-816. CONTROLSS_INTXBAR_INTXBAR27_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1675. INTXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.197 CONTROLSS_INTXBAR_INTXBAR27_G6 Register (Offset = 7D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1676. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D8h

Figure 3-817. CONTROLSS_INTXBAR_INTXBAR27_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					SEL		
NONE					RW		
0					0		

Access Types Legend

Table 3-1677. INTXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.198 CONTROLSS_INTXBAR_INTXBAR28_G0 Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1678. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5800h

Figure 3-818. CONTROLSS_INTXBAR_INTXBAR28_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1679. INTXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.199 CONTROLSS_INTXBAR_INTXBAR28_G1 Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1680. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5804h

Figure 3-819. CONTROLSS_INTXBAR_INTXBAR28_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1681. INTXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.200 CONTROLSS_INTXBAR_INTXBAR28_G2 Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1682. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5808h

Figure 3-820. CONTROLSS_INTXBAR_INTXBAR28_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1683. INTXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.201 CONTROLSS_INTXBAR_INTXBAR28_G3 Register (Offset = 80Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1684. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 580Ch

Figure 3-821. CONTROLSS_INTXBAR_INTXBAR28_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1685. INTXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.202 CONTROLSS_INTXBAR_INTXBAR28_G4 Register (Offset = 810h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1686. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5810h

Figure 3-822. CONTROLSS_INTXBAR_INTXBAR28_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1687. INTXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.203 CONTROLSS_INTXBAR_INTXBAR28_G5 Register (Offset = 814h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1688. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5814h

Figure 3-823. CONTROLSS_INTXBAR_INTXBAR28_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1689. INTXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.204 CONTROLSS_INTXBAR_INTXBAR28_G6 Register (Offset = 818h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1690. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5818h

Figure 3-824. CONTROLSS_INTXBAR_INTXBAR28_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1691. INTXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.205 CONTROLSS_INTXBAR_INTXBAR29_G0 Register (Offset = 840h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1692. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5840h

Figure 3-825. CONTROLSS_INTXBAR_INTXBAR29_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1693. INTXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.206 CONTROLSS_INTXBAR_INTXBAR29_G1 Register (Offset = 844h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1694. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5844h

Figure 3-826. CONTROLSS_INTXBAR_INTXBAR29_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1695. INTXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.207 CONTROLSS_INTXBAR_INTXBAR29_G2 Register (Offset = 848h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1696. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5848h

Figure 3-827. CONTROLSS_INTXBAR_INTXBAR29_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1697. INTXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.208 CONTROLSS_INTXBAR_INTXBAR29_G3 Register (Offset = 84Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1698. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 584Ch

Figure 3-828. CONTROLSS_INTXBAR_INTXBAR29_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1699. INTXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.209 CONTROLSS_INTXBAR_INTXBAR29_G4 Register (Offset = 850h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1700. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5850h

Figure 3-829. CONTROLSS_INTXBAR_INTXBAR29_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1701. INTXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.210 CONTROLSS_INTXBAR_INTXBAR29_G5 Register (Offset = 854h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1702. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5854h

Figure 3-830. CONTROLSS_INTXBAR_INTXBAR29_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1703. INTXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.211 CONTROLSS_INTXBAR_INTXBAR29_G6 Register (Offset = 858h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1704. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5858h

Figure 3-831. CONTROLSS_INTXBAR_INTXBAR29_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1705. INTXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.212 CONTROLSS_INTXBAR_INTXBAR30_G0 Register (Offset = 880h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1706. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5880h

Figure 3-832. CONTROLSS_INTXBAR_INTXBAR30_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1707. INTXBAR30_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.213 CONTROLSS_INTXBAR_INTXBAR30_G1 Register (Offset = 884h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1708. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5884h

Figure 3-833. CONTROLSS_INTXBAR_INTXBAR30_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1709. INTXBAR30_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.214 CONTROLSS_INTXBAR_INTXBAR30_G2 Register (Offset = 888h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1710. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5888h

Figure 3-834. CONTROLSS_INTXBAR_INTXBAR30_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1711. INTXBAR30_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.215 CONTROLSS_INTXBAR_INTXBAR30_G3 Register (Offset = 88Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1712. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 588Ch

Figure 3-835. CONTROLSS_INTXBAR_INTXBAR30_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1713. INTXBAR30_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.216 CONTROLSS_INTXBAR_INTXBAR30_G4 Register (Offset = 890h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1714. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5890h

Figure 3-836. CONTROLSS_INTXBAR_INTXBAR30_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1715. INTXBAR30_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.217 CONTROLSS_INTXBAR_INTXBAR30_G5 Register (Offset = 894h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1716. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5894h

Figure 3-837. CONTROLSS_INTXBAR_INTXBAR30_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1717. INTXBAR30_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.218 CONTROLSS_INTXBAR_INTXBAR30_G6 Register (Offset = 898h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1718. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5898h

Figure 3-838. CONTROLSS_INTXBAR_INTXBAR30_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1719. INTXBAR30_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.13.219 CONTROLSS_INTXBAR_INTXBAR31_G0 Register (Offset = 8C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1720. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C0h

Figure 3-839. CONTROLSS_INTXBAR_INTXBAR31_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1721. INTXBAR31_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

3.13.220 CONTROLSS_INTXBAR_INTXBAR31_G1 Register (Offset = 8C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1722. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C4h

Figure 3-840. CONTROLSS_INTXBAR_INTXBAR31_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1723. INTXBAR31_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

3.13.221 CONTROLSS_INTXBAR_INTXBAR31_G2 Register (Offset = 8C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1724. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C8h

Figure 3-841. CONTROLSS_INTXBAR_INTXBAR31_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1725. INTXBAR31_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

3.13.222 CONTROLSS_INTXBAR_INTXBAR31_G3 Register (Offset = 8CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1726. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58CCh

Figure 3-842. CONTROLSS_INTXBAR_INTXBAR31_G3 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1727. INTXBAR31_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

3.13.223 CONTROLSS_INTXBAR_INTXBAR31_G4 Register (Offset = 8D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1728. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D0h

Figure 3-843. CONTROLSS_INTXBAR_INTXBAR31_G4 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1729. INTXBAR31_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

3.13.224 CONTROLSS_INTXBAR_INTXBAR31_G5 Register (Offset = 8D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1730. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D4h

Figure 3-844. CONTROLSS_INTXBAR_INTXBAR31_G5 Name Register

15	14	13	12	11	10	9	8
RESERVED						SEL	
NONE						RW	
0						0	
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1731. INTXBAR31_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

3.13.225 CONTROLSS_INTXBAR_INTXBAR31_G6 Register (Offset = 8D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1732. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D8h

Figure 3-845. CONTROLSS_INTXBAR_INTXBAR31_G6 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SEL	
NONE						RW	
0						0	

Access Types Legend

Table 3-1733. INTXBAR31_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

Table 3-1734. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.14 C2K_MDLXBAR Registers

Table 3-1735. CONTROLSS_MDLXBAR, CONTROLSS_MDLXBAR_CONTROLSS_MDLXBAR Registers, Base Address=502D 3000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_MDLXBAR Physical Address
0h	32	CONTROLSS_MDLXBAR_PID	PID register	502D 3000h
100h	32	CONTROLSS_MDLXBAR_MDLXBAR0_G0	RW	502D 3100h
104h	32	CONTROLSS_MDLXBAR_MDLXBAR0_G1	RW	502D 3104h
108h	32	CONTROLSS_MDLXBAR_MDLXBAR0_G2	RW	502D 3108h
140h	32	CONTROLSS_MDLXBAR_MDLXBAR1_G0	RW	502D 3140h
144h	32	CONTROLSS_MDLXBAR_MDLXBAR1_G1	RW	502D 3144h
148h	32	CONTROLSS_MDLXBAR_MDLXBAR1_G2	RW	502D 3148h
180h	32	CONTROLSS_MDLXBAR_MDLXBAR2_G0	RW	502D 3180h
184h	32	CONTROLSS_MDLXBAR_MDLXBAR2_G1	RW	502D 3184h
188h	32	CONTROLSS_MDLXBAR_MDLXBAR2_G2	RW	502D 3188h
1C0h	32	CONTROLSS_MDLXBAR_MDLXBAR3_G0	RW	502D 31C0h
1C4h	32	CONTROLSS_MDLXBAR_MDLXBAR3_G1	RW	502D 31C4h
1C8h	32	CONTROLSS_MDLXBAR_MDLXBAR3_G2	RW	502D 31C8h
200h	32	CONTROLSS_MDLXBAR_MDLXBAR4_G0	RW	502D 3200h
204h	32	CONTROLSS_MDLXBAR_MDLXBAR4_G1	RW	502D 3204h
208h	32	CONTROLSS_MDLXBAR_MDLXBAR4_G2	RW	502D 3208h
240h	32	CONTROLSS_MDLXBAR_MDLXBAR5_G0	RW	502D 3240h
244h	32	CONTROLSS_MDLXBAR_MDLXBAR5_G1	RW	502D 3244h
248h	32	CONTROLSS_MDLXBAR_MDLXBAR5_G2	RW	502D 3248h
280h	32	CONTROLSS_MDLXBAR_MDLXBAR6_G0	RW	502D 3280h
284h	32	CONTROLSS_MDLXBAR_MDLXBAR6_G1	RW	502D 3284h
288h	32	CONTROLSS_MDLXBAR_MDLXBAR6_G2	RW	502D 3288h
2C0h	32	CONTROLSS_MDLXBAR_MDLXBAR7_G0	RW	502D 32C0h
2C4h	32	CONTROLSS_MDLXBAR_MDLXBAR7_G1	RW	502D 32C4h
2C8h	32	CONTROLSS_MDLXBAR_MDLXBAR7_G2	RW	502D 32C8h
300h	32	CONTROLSS_MDLXBAR_MDLXBAR8_G0	RW	502D 3300h
304h	32	CONTROLSS_MDLXBAR_MDLXBAR8_G1	RW	502D 3304h
308h	32	CONTROLSS_MDLXBAR_MDLXBAR8_G2	RW	502D 3308h
340h	32	CONTROLSS_MDLXBAR_MDLXBAR9_G0	RW	502D 3340h
344h	32	CONTROLSS_MDLXBAR_MDLXBAR9_G1	RW	502D 3344h
348h	32	CONTROLSS_MDLXBAR_MDLXBAR9_G2	RW	502D 3348h
380h	32	CONTROLSS_MDLXBAR_MDLXBAR10_G0	RW	502D 3380h
384h	32	CONTROLSS_MDLXBAR_MDLXBAR10_G1	RW	502D 3384h
388h	32	CONTROLSS_MDLXBAR_MDLXBAR10_G2	RW	502D 3388h
3C0h	32	CONTROLSS_MDLXBAR_MDLXBAR11_G0	RW	502D 33C0h
3C4h	32	CONTROLSS_MDLXBAR_MDLXBAR11_G1	RW	502D 33C4h
3C8h	32	CONTROLSS_MDLXBAR_MDLXBAR11_G2	RW	502D 33C8h
400h	32	CONTROLSS_MDLXBAR_MDLXBAR12_G0	RW	502D 3400h

Table 3-1735. CONTROLSS_MDLXBAR, CONTROLSS_MDLXBAR_CONTROLSS_MDLXBAR Registers, Base Address=502D 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_MDLXBAR Physical Address
404h	32	CONTROLSS_MDLXBAR_MDLXBAR12_G1	RW	502D 3404h
408h	32	CONTROLSS_MDLXBAR_MDLXBAR12_G2	RW	502D 3408h
440h	32	CONTROLSS_MDLXBAR_MDLXBAR13_G0	RW	502D 3440h
444h	32	CONTROLSS_MDLXBAR_MDLXBAR13_G1	RW	502D 3444h
448h	32	CONTROLSS_MDLXBAR_MDLXBAR13_G2	RW	502D 3448h
480h	32	CONTROLSS_MDLXBAR_MDLXBAR14_G0	RW	502D 3480h
484h	32	CONTROLSS_MDLXBAR_MDLXBAR14_G1	RW	502D 3484h
488h	32	CONTROLSS_MDLXBAR_MDLXBAR14_G2	RW	502D 3488h
4C0h	32	CONTROLSS_MDLXBAR_MDLXBAR15_G0	RW	502D 34C0h
4C4h	32	CONTROLSS_MDLXBAR_MDLXBAR15_G1	RW	502D 34C4h
4C8h	32	CONTROLSS_MDLXBAR_MDLXBAR15_G2	RW	502D 34C8h

3.14.1 CONTROLSS_MDLXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1736. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3000h

Figure 3-846. CONTROLSS_MDLXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-1737. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.14.2 CONTROLSS_MDLXBAR_MDLXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1738. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3100h

Figure 3-847. CONTROLSS_MDLXBAR_MDLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1739. MDLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.3 CONTROLSS_MDLXBAR_MDLXBAR0_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1740. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3104h

Figure 3-848. CONTROLSS_MDLXBAR_MDLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1741. MDLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.4 CONTROLSS_MDLXBAR_MDLXBAR0_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1742. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3108h

Figure 3-849. CONTROLSS_MDLXBAR_MDLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1743. MDLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.5 CONTROLSS_MDLXBAR_MDLXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1744. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3140h

Figure 3-850. CONTROLSS_MDLXBAR_MDLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1745. MDLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar1 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.6 CONTROLSS_MDLXBAR_MDLXBAR1_G1 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1746. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3144h

Figure 3-851. CONTROLSS_MDLXBAR_MDLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1747. MDLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar1 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.7 CONTROLSS_MDLXBAR_MDLXBAR1_G2 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1748. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3148h

Figure 3-852. CONTROLSS_MDLXBAR_MDLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1749. MDLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar1 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.8 CONTROLSS_MDLXBAR_MDLXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1750. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3180h

Figure 3-853. CONTROLSS_MDLXBAR_MDLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1751. MDLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar2 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.9 CONTROLSS_MDLXBAR_MDLXBAR2_G1 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1752. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3184h

Figure 3-854. CONTROLSS_MDLXBAR_MDLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1753. MDLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar2 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.10 CONTROLSS_MDLXBAR_MDLXBAR2_G2 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1754. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3188h

Figure 3-855. CONTROLSS_MDLXBAR_MDLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1755. MDLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar2 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.11 CONTROLSS_MDLXBAR_MDLXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1756. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C0h

Figure 3-856. CONTROLSS_MDLXBAR_MDLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1757. MDLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar3 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.12 CONTROLSS_MDLXBAR_MDLXBAR3_G1 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1758. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C4h

Figure 3-857. CONTROLSS_MDLXBAR_MDLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1759. MDLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar3 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.13 CONTROLSS_MDLXBAR_MDLXBAR3_G2 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1760. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C8h

Figure 3-858. CONTROLSS_MDLXBAR_MDLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1761. MDLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar3 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.14 CONTROLSS_MDLXBAR_MDLXBAR4_G0 Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1762. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3200h

Figure 3-859. CONTROLSS_MDLXBAR_MDLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1763. MDLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar4 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.15 CONTROLSS_MDLXBAR_MDLXBAR4_G1 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1764. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3204h

Figure 3-860. CONTROLSS_MDLXBAR_MDLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1765. MDLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar4 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.16 CONTROLSS_MDLXBAR_MDLXBAR4_G2 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1766. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3208h

Figure 3-861. CONTROLSS_MDLXBAR_MDLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1767. MDLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar4 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.17 CONTROLSS_MDLXBAR_MDLXBAR5_G0 Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1768. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3240h

Figure 3-862. CONTROLSS_MDLXBAR_MDLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1769. MDLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar5 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.18 CONTROLSS_MDLXBAR_MDLXBAR5_G1 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1770. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3244h

Figure 3-863. CONTROLSS_MDLXBAR_MDLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1771. MDLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar5 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.19 CONTROLSS_MDLXBAR_MDLXBAR5_G2 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1772. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3248h

Figure 3-864. CONTROLSS_MDLXBAR_MDLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1773. MDLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar5 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.20 CONTROLSS_MDLXBAR_MDLXBAR6_G0 Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1774. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3280h

Figure 3-865. CONTROLSS_MDLXBAR_MDLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1775. MDLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar6 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.21 CONTROLSS_MDLXBAR_MDLXBAR6_G1 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1776. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3284h

Figure 3-866. CONTROLSS_MDLXBAR_MDLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1777. MDLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar6 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.22 CONTROLSS_MDLXBAR_MDLXBAR6_G2 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1778. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3288h

Figure 3-867. CONTROLSS_MDLXBAR_MDLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1779. MDLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar6 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.23 CONTROLSS_MDLXBAR_MDLXBAR7_G0 Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1780. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C0h

Figure 3-868. CONTROLSS_MDLXBAR_MDLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1781. MDLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar7 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.24 CONTROLSS_MDLXBAR_MDLXBAR7_G1 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1782. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C4h

Figure 3-869. CONTROLSS_MDLXBAR_MDLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1783. MDLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar7 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.25 CONTROLSS_MDLXBAR_MDLXBAR7_G2 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1784. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C8h

Figure 3-870. CONTROLSS_MDLXBAR_MDLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1785. MDLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar7 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.26 CONTROLSS_MDLXBAR_MDLXBAR8_G0 Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1786. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3300h

Figure 3-871. CONTROLSS_MDLXBAR_MDLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1787. MDLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar8 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.27 CONTROLSS_MDLXBAR_MDLXBAR8_G1 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1788. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3304h

Figure 3-872. CONTROLSS_MDLXBAR_MDLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1789. MDLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar8 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.28 CONTROLSS_MDLXBAR_MDLXBAR8_G2 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1790. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3308h

Figure 3-873. CONTROLSS_MDLXBAR_MDLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1791. MDLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar8 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.29 CONTROLSS_MDLXBAR_MDLXBAR9_G0 Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1792. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3340h

Figure 3-874. CONTROLSS_MDLXBAR_MDLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1793. MDLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar9 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.30 CONTROLSS_MDLXBAR_MDLXBAR9_G1 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1794. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3344h

Figure 3-875. CONTROLSS_MDLXBAR_MDLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1795. MDLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar9 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.31 CONTROLSS_MDLXBAR_MDLXBAR9_G2 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1796. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3348h

Figure 3-876. CONTROLSS_MDLXBAR_MDLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1797. MDLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar9 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.32 CONTROLSS_MDLXBAR_MDLXBAR10_G0 Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1798. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3380h

Figure 3-877. CONTROLSS_MDLXBAR_MDLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1799. MDLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar10 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.33 CONTROLSS_MDLXBAR_MDLXBAR10_G1 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1800. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3384h

Figure 3-878. CONTROLSS_MDLXBAR_MDLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1801. MDLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar10 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.34 CONTROLSS_MDLXBAR_MDLXBAR10_G2 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1802. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3388h

Figure 3-879. CONTROLSS_MDLXBAR_MDLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1803. MDLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar10 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.35 CONTROLSS_MDLXBAR_MDLXBAR11_G0 Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1804. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C0h

Figure 3-880. CONTROLSS_MDLXBAR_MDLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1805. MDLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar11 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.36 CONTROLSS_MDLXBAR_MDLXBAR11_G1 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1806. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C4h

Figure 3-881. CONTROLSS_MDLXBAR_MDLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1807. MDLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar11 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.37 CONTROLSS_MDLXBAR_MDLXBAR11_G2 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1808. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C8h

Figure 3-882. CONTROLSS_MDLXBAR_MDLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1809. MDLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar11 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.38 CONTROLSS_MDLXBAR_MDLXBAR12_G0 Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1810. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3400h

Figure 3-883. CONTROLSS_MDLXBAR_MDLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1811. MDLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar12 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.39 CONTROLSS_MDLXBAR_MDLXBAR12_G1 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1812. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3404h

Figure 3-884. CONTROLSS_MDLXBAR_MDLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1813. MDLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar12 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.40 CONTROLSS_MDLXBAR_MDLXBAR12_G2 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1814. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3408h

Figure 3-885. CONTROLSS_MDLXBAR_MDLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1815. MDLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar12 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.41 CONTROLSS_MDLXBAR_MDLXBAR13_G0 Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1816. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3440h

Figure 3-886. CONTROLSS_MDLXBAR_MDLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1817. MDLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar13 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.42 CONTROLSS_MDLXBAR_MDLXBAR13_G1 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1818. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3444h

Figure 3-887. CONTROLSS_MDLXBAR_MDLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1819. MDLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar13 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.43 CONTROLSS_MDLXBAR_MDLXBAR13_G2 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1820. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3448h

Figure 3-888. CONTROLSS_MDLXBAR_MDLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1821. MDLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar13 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.44 CONTROLSS_MDLXBAR_MDLXBAR14_G0 Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1822. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3480h

Figure 3-889. CONTROLSS_MDLXBAR_MDLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1823. MDLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar14 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.45 CONTROLSS_MDLXBAR_MDLXBAR14_G1 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1824. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3484h

Figure 3-890. CONTROLSS_MDLXBAR_MDLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1825. MDLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar14 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.46 CONTROLSS_MDLXBAR_MDLXBAR14_G2 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1826. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3488h

Figure 3-891. CONTROLSS_MDLXBAR_MDLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1827. MDLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar14 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.14.47 CONTROLSS_MDLXBAR_MDLXBAR15_G0 Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1828. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C0h

Figure 3-892. CONTROLSS_MDLXBAR_MDLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1829. MDLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar15 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

3.14.48 CONTROLSS_MDLXBAR_MDLXBAR15_G1 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1830. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C4h

Figure 3-893. CONTROLSS_MDLXBAR_MDLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1831. MDLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar15 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

3.14.49 CONTROLSS_MDLXBAR_MDLXBAR15_G2 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1832. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C8h

Figure 3-894. CONTROLSS_MDLXBAR_MDLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1833. MDLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar15 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

Table 3-1834. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.15 C2K_OTTOCAL Registers

Table 3-1835. CONTROLSS_OTTOCAL0, CONTROLSS_OTTOCAL0_CONTROLSS_OTTOCAL Registers, Base Address=502E 0000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
42h	16	CONTROLSS_OTTOCAL0_HRPWR	HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.	502E 0042h	502E 1042h	502E 2042h
44h	16	CONTROLSS_OTTOCAL0_HRCAL	HRPWM Calibration Register	502E 0044h	502E 1044h	502E 2044h
46h	16	CONTROLSS_OTTOCAL0_HRPRD	HRPWM Period Register	502E 0046h	502E 1046h	502E 2046h
48h	16	CONTROLSS_OTTOCAL0_HRCNT0	HRPWM Counter 0 Register	502E 0048h	502E 1048h	502E 2048h
4Ah	16	CONTROLSS_OTTOCAL0_HRCNT1	HRPWM Counter 1 Register	502E 004Ah	502E 104Ah	502E 204Ah
4Ch	16	CONTROLSS_OTTOCAL0_HRMSTEP	HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.	502E 004Ch	502E 104Ch	502E 204Ch

Table 3-1836. CONTROLSS_OTTOCAL1, CONTROLSS_OTTOCAL1_CONTROLSS_OTTOCAL Registers, Base Address=502E 1000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
42h	16	CONTROLSS_OTTOCAL1_HRPWR	HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.	502E 0042h	502E 1042h	502E 2042h
44h	16	CONTROLSS_OTTOCAL1_HRCAL	HRPWM Calibration Register	502E 0044h	502E 1044h	502E 2044h
46h	16	CONTROLSS_OTTOCAL1_HRPRD	HRPWM Period Register	502E 0046h	502E 1046h	502E 2046h
48h	16	CONTROLSS_OTTOCAL1_HRCNT0	HRPWM Counter 0 Register	502E 0048h	502E 1048h	502E 2048h
4Ah	16	CONTROLSS_OTTOCAL1_HRCNT1	HRPWM Counter 1 Register	502E 004Ah	502E 104Ah	502E 204Ah

Table 3-1836. CONTROLSS_OTTOCAL1, CONTROLSS_OTTOCAL1_CONTROLSS_OTTOCAL Registers, Base Address=502E 1000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
4Ch	16	CONTROLSS_OTTOCAL1_HRMSTEP	HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.	502E 004Ch	502E 104Ch	502E 204Ch

Table 3-1837. CONTROLSS_OTTOCAL2, CONTROLSS_OTTOCAL2_CONTROLSS_OTTOCAL Registers, Base Address=502E 2000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
42h	16	CONTROLSS_OTTOCAL2_HRPWR	HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.	502E 0042h	502E 1042h	502E 2042h
44h	16	CONTROLSS_OTTOCAL2_HRCAL	HRPWM Calibration Register	502E 0044h	502E 1044h	502E 2044h
46h	16	CONTROLSS_OTTOCAL2_HRPRD	HRPWM Period Register	502E 0046h	502E 1046h	502E 2046h
48h	16	CONTROLSS_OTTOCAL2_HRCNT0	HRPWM Counter 0 Register	502E 0048h	502E 1048h	502E 2048h
4Ah	16	CONTROLSS_OTTOCAL2_HRCNT1	HRPWM Counter 1 Register	502E 004Ah	502E 104Ah	502E 204Ah
4Ch	16	CONTROLSS_OTTOCAL2_HRMSTEP	HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.	502E 004Ch	502E 104Ch	502E 204Ch

Table 3-1838. CONTROLSS_OTTOCAL3, CONTROLSS_OTTOCAL3_CONTROLSS_OTTOCAL Registers, Base Address=502E 3000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
42h	16	CONTROLSS_OTTOCAL3_HRPWR	HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.	502E 0042h	502E 1042h	502E 2042h
44h	16	CONTROLSS_OTTOCAL3_HRCAL	HRPWM Calibration Register	502E 0044h	502E 1044h	502E 2044h
46h	16	CONTROLSS_OTTOCAL3_HRPRD	HRPWM Period Register	502E 0046h	502E 1046h	502E 2046h

Table 3-1838. CONTROLSS_OTTOCAL3, CONTROLSS_OTTOCAL3_CONTROLSS_OTTOCAL Registers, Base Address=502E 3000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OTTOCAL0 Physical Address	CONTROLSS_OTTOCAL1 Physical Address	CONTROLSS_OTTOCAL2 Physical Address
48h	16	CONTROLSS_OTTOCAL3_HRCNT0	HRPWM Counter 0 Register	502E 0048h	502E 1048h	502E 2048h
4Ah	16	CONTROLSS_OTTOCAL3_HRCNT1	HRPWM Counter 1 Register	502E 004Ah	502E 104Ah	502E 204Ah
4Ch	16	CONTROLSS_OTTOCAL3_HRMSTEP	HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.	502E 004Ch	502E 104Ch	502E 204Ch

3.15.1 CONTROLSS_OTTOCAL0_HRPWR Register (Offset = 42h) [reset = h]

Short Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

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Table 3-1839. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0042h
CONTROLSS_OTTOCAL1	502E 1042h
CONTROLSS_OTTOCAL2	502E 2042h
CONTROLSS_OTTOCAL3	502E 3042h

Figure 3-895. CONTROLSS_OTTOCAL0_HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED					CALSEL	
RW	RO RRETURNS0S					RW	
0	0					0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
RW		RW	RO	RW	RW	RW	
0		0	0	0	0	0	

Access Types Legend

Table 3-1840. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	RW	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic
14 - 10	RESERVED	RO RRETURNS 0S		Reserved
9 - 6	CALSEL	RW	0h	EPWM Delay Line Selection for Calibration:
5	TESTSEL	RW	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:
4	CALSTS	RO	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:
3	CNTSEL	RW	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts:
2	CALSTART	RW	0h	Calibration Start/Stop Bit:
1 - 0	CALMODE	RW	0h	Note: CALMODE bits in HRPWM Module. Not used here.

3.15.2 CONTROLSS_OTTOCAL0_HRCAL Register (Offset = 44h) [reset = h]

Short Description: HRPWM Calibration Register

Long Description:

Return to Summary Table

Table 3-1841. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0044h
CONTROLSS_OTTOCAL1	502E 1044h
CONTROLSS_OTTOCAL2	502E 2044h
CONTROLSS_OTTOCAL3	502E 3044h

Figure 3-896. CONTROLSS_OTTOCAL0_HRCAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRCAL							
RW							
0							

Access Types Legend

Table 3-1842. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRCAL	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run.

3.15.3 CONTROLSS_OTTOCAL0_HRPRD Register (Offset = 46h) [reset = h]

Short Description: HRPWM Period Register

Long Description:

Return to Summary Table

Table 3-1843. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0046h
CONTROLSS_OTTOCAL1	502E 1046h
CONTROLSS_OTTOCAL2	502E 2046h
CONTROLSS_OTTOCAL3	502E 3046h

Figure 3-897. CONTROLSS_OTTOCAL0_HRPRD Name Register

15	14	13	12	11	10	9	8
HRPRD							
RW							
0							
7	6	5	4	3	2	1	0
HRPRD							
RW							
0							

Access Types Legend

Table 3-1844. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRPRD	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only.

3.15.4 CONTROLSS_OTTOCAL0_HRCNT0 Register (Offset = 48h) [reset = h]

Short Description: HRPWM Counter 0 Register

Long Description:

Return to Summary Table

Table 3-1845. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0048h
CONTROLSS_OTTOCAL1	502E 1048h
CONTROLSS_OTTOCAL2	502E 2048h
CONTROLSS_OTTOCAL3	502E 3048h

Figure 3-898. CONTROLSS_OTTOCAL0_HRCNT0 Name Register

15	14	13	12	11	10	9	8
HRCNT0							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT0							
RW							
0							

Access Types Legend

Table 3-1846. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT0	RW	0h	The HRCNT0 counter increments on every ring oscillator clock pulse.

3.15.5 CONTROLSS_OTTOCAL0_HRCNT1 Register (Offset = 4Ah) [reset = h]

Short Description: HRPWM Counter 1 Register

Long Description:

Return to Summary Table

Table 3-1847. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ah
CONTROLSS_OTTOCAL1	502E 104Ah
CONTROLSS_OTTOCAL2	502E 204Ah
CONTROLSS_OTTOCAL3	502E 304Ah

Figure 3-899. CONTROLSS_OTTOCAL0_HRCNT1 Name Register

15	14	13	12	11	10	9	8
HRCNT1							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT1							
RW							
0							

Access Types Legend

Table 3-1848. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT1	RW	0h	The HRCNT1 counter increments on every system clock pulse.

3.15.6 CONTROLSS_OTTOCAL0_HRMSTEP Register (Offset = 4Ch) [reset = h]

Short Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

Return to Summary Table

Table 3-1849. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ch
CONTROLSS_OTTOCAL1	502E 104Ch
CONTROLSS_OTTOCAL2	502E 204Ch
CONTROLSS_OTTOCAL3	502E 304Ch

Figure 3-900. CONTROLSS_OTTOCAL0_HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRMSTEP							
RW							
0							

Access Types Legend

Table 3-1850. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRMSTEP	RW	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

3.15.7 CONTROLSS_OTTOCAL1_HRPWR Register (Offset = 42h) [reset = h]

Short Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-1851. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0042h
CONTROLSS_OTTOCAL1	502E 1042h
CONTROLSS_OTTOCAL2	502E 2042h
CONTROLSS_OTTOCAL3	502E 3042h

Figure 3-901. CONTROLSS_OTTOCAL1_HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED					CALSEL	
RW	RO RRETURNS0S					RW	
0	0					0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
RW		RW	RO	RW	RW	RW	
0		0	0	0	0	0	

Access Types Legend

Table 3-1852. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	RW	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic
14 - 10	RESERVED	RO RRETURNS 0S		Reserved
9 - 6	CALSEL	RW	0h	EPWM Delay Line Selection for Calibration:
5	TESTSEL	RW	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:
4	CALSTS	RO	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:
3	CNTSEL	RW	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts:
2	CALSTART	RW	0h	Calibration Start/Stop Bit:
1 - 0	CALMODE	RW	0h	Note: CALMODE bits in HRPWM Module. Not used here.

3.15.8 CONTROLSS_OTTOCAL1_HRCAL Register (Offset = 44h) [reset = h]

Short Description: HRPWM Calibration Register

Long Description:

Return to Summary Table

Table 3-1853. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0044h
CONTROLSS_OTTOCAL1	502E 1044h
CONTROLSS_OTTOCAL2	502E 2044h
CONTROLSS_OTTOCAL3	502E 3044h

Figure 3-902. CONTROLSS_OTTOCAL1_HRCAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRCAL							
RW							
0							

Access Types Legend

Table 3-1854. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRCAL	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run.

3.15.9 CONTROLSS_OTTOCAL1_HRPRD Register (Offset = 46h) [reset = h]

Short Description: HRPWM Period Register

Long Description:

Return to Summary Table

Table 3-1855. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0046h
CONTROLSS_OTTOCAL1	502E 1046h
CONTROLSS_OTTOCAL2	502E 2046h
CONTROLSS_OTTOCAL3	502E 3046h

Figure 3-903. CONTROLSS_OTTOCAL1_HRPRD Name Register

15	14	13	12	11	10	9	8
HRPRD							
RW							
0							
7	6	5	4	3	2	1	0
HRPRD							
RW							
0							

Access Types Legend

Table 3-1856. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRPRD	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only.

3.15.10 CONTROLSS_OTTOCAL1_HRCNT0 Register (Offset = 48h) [reset = h]

Short Description: HRPWM Counter 0 Register

Long Description:

Return to Summary Table

Table 3-1857. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0048h
CONTROLSS_OTTOCAL1	502E 1048h
CONTROLSS_OTTOCAL2	502E 2048h
CONTROLSS_OTTOCAL3	502E 3048h

Figure 3-904. CONTROLSS_OTTOCAL1_HRCNT0 Name Register

15	14	13	12	11	10	9	8
HRCNT0							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT0							
RW							
0							

Access Types Legend

Table 3-1858. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT0	RW	0h	The HRCNT0 counter increments on every ring oscillator clock pulse.

3.15.11 CONTROLSS_OTTOCAL1_HRCNT1 Register (Offset = 4Ah) [reset = h]

Short Description: HRPWM Counter 1 Register

Long Description:

Return to Summary Table

Table 3-1859. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ah
CONTROLSS_OTTOCAL1	502E 104Ah
CONTROLSS_OTTOCAL2	502E 204Ah
CONTROLSS_OTTOCAL3	502E 304Ah

Figure 3-905. CONTROLSS_OTTOCAL1_HRCNT1 Name Register

15	14	13	12	11	10	9	8
HRCNT1							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT1							
RW							
0							

Access Types Legend

Table 3-1860. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT1	RW	0h	The HRCNT1 counter increments on every system clock pulse.

3.15.12 CONTROLSS_OTTOCAL1_HRMSTEP Register (Offset = 4Ch) [reset = h]

Short Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

Return to Summary Table

Table 3-1861. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ch
CONTROLSS_OTTOCAL1	502E 104Ch
CONTROLSS_OTTOCAL2	502E 204Ch
CONTROLSS_OTTOCAL3	502E 304Ch

Figure 3-906. CONTROLSS_OTTOCAL1_HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRMSTEP							
RW							
0							

Access Types Legend

Table 3-1862. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRMSTEP	RW	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

3.15.13 CONTROLSS_OTTOCAL2_HRPWR Register (Offset = 42h) [reset = h]

Short Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-1863. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0042h
CONTROLSS_OTTOCAL1	502E 1042h
CONTROLSS_OTTOCAL2	502E 2042h
CONTROLSS_OTTOCAL3	502E 3042h

Figure 3-907. CONTROLSS_OTTOCAL2_HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED					CALSEL	
RW	RO RRETURNS0S					RW	
0	0					0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
RW		RW	RO	RW	RW	RW	
0		0	0	0	0	0	

Access Types Legend

Table 3-1864. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	RW	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic
14 - 10	RESERVED	RO RRETURNS 0S		Reserved
9 - 6	CALSEL	RW	0h	EPWM Delay Line Selection for Calibration:
5	TESTSEL	RW	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:
4	CALSTS	RO	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:
3	CNTSEL	RW	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts:
2	CALSTART	RW	0h	Calibration Start/Stop Bit:
1 - 0	CALMODE	RW	0h	Note: CALMODE bits in HRPWM Module. Not used here.

3.15.14 CONTROLSS_OTTOCAL2_HRCAL Register (Offset = 44h) [reset = h]

Short Description: HRPWM Calibration Register

Long Description:

Return to Summary Table

Table 3-1865. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0044h
CONTROLSS_OTTOCAL1	502E 1044h
CONTROLSS_OTTOCAL2	502E 2044h
CONTROLSS_OTTOCAL3	502E 3044h

Figure 3-908. CONTROLSS_OTTOCAL2_HRCAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRCAL							
RW							
0							

Access Types Legend

Table 3-1866. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRCAL	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run.

3.15.15 CONTROLSS_OTTOCAL2_HRPRD Register (Offset = 46h) [reset = h]

Short Description: HRPWM Period Register

Long Description:

Return to Summary Table

Table 3-1867. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0046h
CONTROLSS_OTTOCAL1	502E 1046h
CONTROLSS_OTTOCAL2	502E 2046h
CONTROLSS_OTTOCAL3	502E 3046h

Figure 3-909. CONTROLSS_OTTOCAL2_HRPRD Name Register

15	14	13	12	11	10	9	8
HRPRD							
RW							
0							
7	6	5	4	3	2	1	0
HRPRD							
RW							
0							

Access Types Legend

Table 3-1868. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRPRD	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only.

3.15.16 CONTROLSS_OTTOCAL2_HRCNT0 Register (Offset = 48h) [reset = h]

Short Description: HRPWM Counter 0 Register

Long Description:

Return to Summary Table

Table 3-1869. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0048h
CONTROLSS_OTTOCAL1	502E 1048h
CONTROLSS_OTTOCAL2	502E 2048h
CONTROLSS_OTTOCAL3	502E 3048h

Figure 3-910. CONTROLSS_OTTOCAL2_HRCNT0 Name Register

15	14	13	12	11	10	9	8
HRCNT0							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT0							
RW							
0							

Access Types Legend

Table 3-1870. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT0	RW	0h	The HRCNT0 counter increments on every ring oscillator clock pulse.

3.15.17 CONTROLSS_OTTOCAL2_HRCNT1 Register (Offset = 4Ah) [reset = h]

Short Description: HRPWM Counter 1 Register

Long Description:

Return to Summary Table

Table 3-1871. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ah
CONTROLSS_OTTOCAL1	502E 104Ah
CONTROLSS_OTTOCAL2	502E 204Ah
CONTROLSS_OTTOCAL3	502E 304Ah

Figure 3-911. CONTROLSS_OTTOCAL2_HRCNT1 Name Register

15	14	13	12	11	10	9	8
HRCNT1							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT1							
RW							
0							

Access Types Legend

Table 3-1872. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT1	RW	0h	The HRCNT1 counter increments on every system clock pulse.

3.15.18 CONTROLSS_OTTOCAL2_HRMSTEP Register (Offset = 4Ch) [reset = h]

Short Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

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Table 3-1873. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ch
CONTROLSS_OTTOCAL1	502E 104Ch
CONTROLSS_OTTOCAL2	502E 204Ch
CONTROLSS_OTTOCAL3	502E 304Ch

Figure 3-912. CONTROLSS_OTTOCAL2_HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRMSTEP							
RW							
0							

Access Types Legend

Table 3-1874. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRMSTEP	RW	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

3.15.19 CONTROLSS_OTTOCAL3_HRPWR Register (Offset = 42h) [reset = h]

Short Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

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Table 3-1875. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0042h
CONTROLSS_OTTOCAL1	502E 1042h
CONTROLSS_OTTOCAL2	502E 2042h
CONTROLSS_OTTOCAL3	502E 3042h

Figure 3-913. CONTROLSS_OTTOCAL3_HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED					CALSEL	
RW	RO RRETURNS0S					RW	
0	0					0	
7	6	5	4	3	2	1	0
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
RW		RW	RO	RW	RW	RW	
0		0	0	0	0	0	

Access Types Legend

Table 3-1876. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	RW	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic
14 - 10	RESERVED	RO RRETURNS 0S		Reserved
9 - 6	CALSEL	RW	0h	EPWM Delay Line Selection for Calibration:
5	TESTSEL	RW	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:
4	CALSTS	RO	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:
3	CNTSEL	RW	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts:
2	CALSTART	RW	0h	Calibration Start/Stop Bit:
1 - 0	CALMODE	RW	0h	Note: CALMODE bits in HRPWM Module. Not used here.

3.15.20 CONTROLSS_OTTOCAL3_HRCAL Register (Offset = 44h) [reset = h]

Short Description: HRPWM Calibration Register

Long Description:

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Table 3-1877. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0044h
CONTROLSS_OTTOCAL1	502E 1044h
CONTROLSS_OTTOCAL2	502E 2044h
CONTROLSS_OTTOCAL3	502E 3044h

Figure 3-914. CONTROLSS_OTTOCAL3_HRCAL Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRCAL							
RW							
0							

Access Types Legend

Table 3-1878. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRCAL	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run.

3.15.21 CONTROLSS_OTTOCAL3_HRPRD Register (Offset = 46h) [reset = h]

Short Description: HRPWM Period Register

Long Description:

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Table 3-1879. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0046h
CONTROLSS_OTTOCAL1	502E 1046h
CONTROLSS_OTTOCAL2	502E 2046h
CONTROLSS_OTTOCAL3	502E 3046h

Figure 3-915. CONTROLSS_OTTOCAL3_HRPRD Name Register

15	14	13	12	11	10	9	8
HRPRD							
RW							
0							
7	6	5	4	3	2	1	0
HRPRD							
RW							
0							

Access Types Legend

Table 3-1880. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRPRD	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only.

3.15.22 CONTROLSS_OTTOCAL3_HRCNT0 Register (Offset = 48h) [reset = h]

Short Description: HRPWM Counter 0 Register

Long Description:

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Table 3-1881. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0048h
CONTROLSS_OTTOCAL1	502E 1048h
CONTROLSS_OTTOCAL2	502E 2048h
CONTROLSS_OTTOCAL3	502E 3048h

Figure 3-916. CONTROLSS_OTTOCAL3_HRCNT0 Name Register

15	14	13	12	11	10	9	8
HRCNT0							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT0							
RW							
0							

Access Types Legend

Table 3-1882. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT0	RW	0h	The HRCNT0 counter increments on every ring oscillator clock pulse.

3.15.23 CONTROLSS_OTTOCAL3_HRCNT1 Register (Offset = 4Ah) [reset = h]

Short Description: HRPWM Counter 1 Register

Long Description:

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Table 3-1883. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ah
CONTROLSS_OTTOCAL1	502E 104Ah
CONTROLSS_OTTOCAL2	502E 204Ah
CONTROLSS_OTTOCAL3	502E 304Ah

Figure 3-917. CONTROLSS_OTTOCAL3_HRCNT1 Name Register

15	14	13	12	11	10	9	8
HRCNT1							
RW							
0							
7	6	5	4	3	2	1	0
HRCNT1							
RW							
0							

Access Types Legend

Table 3-1884. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT1	RW	0h	The HRCNT1 counter increments on every system clock pulse.

3.15.24 CONTROLSS_OTTOCAL3_HRMSTEP Register (Offset = 4Ch) [reset = h]

Short Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

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Table 3-1885. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ch
CONTROLSS_OTTOCAL1	502E 104Ch
CONTROLSS_OTTOCAL2	502E 204Ch
CONTROLSS_OTTOCAL3	502E 304Ch

Figure 3-918. CONTROLSS_OTTOCAL3_HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO RRETURNS0S							
0							
7	6	5	4	3	2	1	0
HRMSTEP							
RW							
0							

Access Types Legend

Table 3-1886. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRMSTEP	RW	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

Table 3-1887. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO RRETURNS0S	RO RRETURNS0S	Undefined
RO	RO	Undefined

3.16 C2K_OUTPUTXBAR Registers

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
0h	32	CONTROLSS_OUTPUTXBAR_PID	PID register	502D 8000h
10h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_STATUS	RO	502D 8010h
14h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGINVERT	RW	502D 8014h
18h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG	RW	502D 8018h
1Ch	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG_CLR	RW	502D 801Ch
20h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGFORCE	RW	502D 8020h
24h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLATCH	RW	502D 8024h
28h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTSTRETCH	RW	502D 8028h
2Ch	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLENGTH	RW	502D 802Ch
30h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTINVERT	RW	502D 8030h
100h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G0	RW	502D 8100h
104h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G1	RW	502D 8104h
108h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G2	RW	502D 8108h
10Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G3	RW	502D 810Ch
110h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G4	RW	502D 8110h
114h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G5	RW	502D 8114h
118h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G6	RW	502D 8118h
11Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G7	RW	502D 811Ch
120h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G8	RW	502D 8120h
124h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G9	RW	502D 8124h
128h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G10	RW	502D 8128h
140h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G0	RW	502D 8140h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
144h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G1	RW	502D 8144h
148h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G2	RW	502D 8148h
14Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G3	RW	502D 814Ch
150h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G4	RW	502D 8150h
154h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G5	RW	502D 8154h
158h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G6	RW	502D 8158h
15Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G7	RW	502D 815Ch
160h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G8	RW	502D 8160h
164h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G9	RW	502D 8164h
168h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G10	RW	502D 8168h
180h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G0	RW	502D 8180h
184h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G1	RW	502D 8184h
188h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G2	RW	502D 8188h
18Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G3	RW	502D 818Ch
190h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G4	RW	502D 8190h
194h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G5	RW	502D 8194h
198h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G6	RW	502D 8198h
19Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G7	RW	502D 819Ch
1A0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G8	RW	502D 81A0h
1A4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G9	RW	502D 81A4h
1A8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G10	RW	502D 81A8h
1C0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G0	RW	502D 81C0h
1C4h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G1	RW	502D 81C4h
1C8h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G2	RW	502D 81C8h
1CCh	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G3	RW	502D 81CCh
1D0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G4	RW	502D 81D0h
1D4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G5	RW	502D 81D4h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
1D8h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G6	RW	502D 81D8h
1DCh	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G7	RW	502D 81DCh
1E0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G8	RW	502D 81E0h
1E4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G9	RW	502D 81E4h
1E8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G10	RW	502D 81E8h
200h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G0	RW	502D 8200h
204h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G1	RW	502D 8204h
208h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G2	RW	502D 8208h
20Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G3	RW	502D 820Ch
210h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G4	RW	502D 8210h
214h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G5	RW	502D 8214h
218h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G6	RW	502D 8218h
21Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G7	RW	502D 821Ch
220h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G8	RW	502D 8220h
224h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G9	RW	502D 8224h
228h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G10	RW	502D 8228h
240h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G0	RW	502D 8240h
244h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G1	RW	502D 8244h
248h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G2	RW	502D 8248h
24Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G3	RW	502D 824Ch
250h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G4	RW	502D 8250h
254h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G5	RW	502D 8254h
258h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G6	RW	502D 8258h
25Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G7	RW	502D 825Ch
260h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G8	RW	502D 8260h
264h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G9	RW	502D 8264h
268h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G10	RW	502D 8268h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
280h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G0	RW	502D 8280h
284h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G1	RW	502D 8284h
288h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G2	RW	502D 8288h
28Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G3	RW	502D 828Ch
290h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G4	RW	502D 8290h
294h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G5	RW	502D 8294h
298h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G6	RW	502D 8298h
29Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G7	RW	502D 829Ch
2A0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G8	RW	502D 82A0h
2A4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G9	RW	502D 82A4h
2A8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G10	RW	502D 82A8h
2C0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G0	RW	502D 82C0h
2C4h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G1	RW	502D 82C4h
2C8h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G2	RW	502D 82C8h
2CCh	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G3	RW	502D 82CCh
2D0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G4	RW	502D 82D0h
2D4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G5	RW	502D 82D4h
2D8h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G6	RW	502D 82D8h
2DCh	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G7	RW	502D 82DCh
2E0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G8	RW	502D 82E0h
2E4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G9	RW	502D 82E4h
2E8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G10	RW	502D 82E8h
300h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G0	RW	502D 8300h
304h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G1	RW	502D 8304h
308h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G2	RW	502D 8308h
30Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G3	RW	502D 830Ch
310h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G4	RW	502D 8310h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
314h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G5	RW	502D 8314h
318h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G6	RW	502D 8318h
31Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G7	RW	502D 831Ch
320h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G8	RW	502D 8320h
324h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G9	RW	502D 8324h
328h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G10	RW	502D 8328h
340h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G0	RW	502D 8340h
344h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G1	RW	502D 8344h
348h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G2	RW	502D 8348h
34Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G3	RW	502D 834Ch
350h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G4	RW	502D 8350h
354h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G5	RW	502D 8354h
358h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G6	RW	502D 8358h
35Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G7	RW	502D 835Ch
360h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G8	RW	502D 8360h
364h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G9	RW	502D 8364h
368h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G10	RW	502D 8368h
380h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G0	RW	502D 8380h
384h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G1	RW	502D 8384h
388h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G2	RW	502D 8388h
38Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G3	RW	502D 838Ch
390h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G4	RW	502D 8390h
394h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G5	RW	502D 8394h
398h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G6	RW	502D 8398h
39Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G7	RW	502D 839Ch
3A0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G8	RW	502D 83A0h
3A4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G9	RW	502D 83A4h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
3A8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G10	RW	502D 83A8h
3C0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G0	RW	502D 83C0h
3C4h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G1	RW	502D 83C4h
3C8h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G2	RW	502D 83C8h
3CCh	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G3	RW	502D 83CCh
3D0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G4	RW	502D 83D0h
3D4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G5	RW	502D 83D4h
3D8h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G6	RW	502D 83D8h
3DCh	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G7	RW	502D 83DCh
3E0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G8	RW	502D 83E0h
3E4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G9	RW	502D 83E4h
3E8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G10	RW	502D 83E8h
400h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G0	RW	502D 8400h
404h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G1	RW	502D 8404h
408h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G2	RW	502D 8408h
40Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G3	RW	502D 840Ch
410h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G4	RW	502D 8410h
414h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G5	RW	502D 8414h
418h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G6	RW	502D 8418h
41Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G7	RW	502D 841Ch
420h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G8	RW	502D 8420h
424h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G9	RW	502D 8424h
428h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G10	RW	502D 8428h
440h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G0	RW	502D 8440h
444h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G1	RW	502D 8444h
448h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G2	RW	502D 8448h
44Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G3	RW	502D 844Ch

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
450h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G4	RW	502D 8450h
454h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G5	RW	502D 8454h
458h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G6	RW	502D 8458h
45Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G7	RW	502D 845Ch
460h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G8	RW	502D 8460h
464h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G9	RW	502D 8464h
468h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G10	RW	502D 8468h
480h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G0	RW	502D 8480h
484h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G1	RW	502D 8484h
488h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G2	RW	502D 8488h
48Ch	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G3	RW	502D 848Ch
490h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G4	RW	502D 8490h
494h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G5	RW	502D 8494h
498h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G6	RW	502D 8498h
49Ch	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G7	RW	502D 849Ch
4A0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G8	RW	502D 84A0h
4A4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G9	RW	502D 84A4h
4A8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G10	RW	502D 84A8h
4C0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G0	RW	502D 84C0h
4C4h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G1	RW	502D 84C4h
4C8h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G2	RW	502D 84C8h
4CCh	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G3	RW	502D 84CCh
4D0h	32	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G4	RW	502D 84D0h
4D4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G5	RW	502D 84D4h
4D8h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G6	RW	502D 84D8h
4DCh	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G7	RW	502D 84DCh
4E0h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G8	RW	502D 84E0h

Table 3-1888. CONTROLSS_OUTPUTXBAR, CONTROLSS_OUTPUTXBAR_CONTROLSS_OUTPUTXBAR Registers, Base Address=502D 8000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
4E4h	24	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G9	RW	502D 84E4h
4E8h	16	CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G10	RW	502D 84E8h

3.16.1 CONTROLSS_OUTPUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-1889. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8000h

Figure 3-919. CONTROLSS_OUTPUTXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-1890. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.16.2 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_STATUS Register (Offset = 10h) [reset = h]

Short Description: RO

Long Description:

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Table 3-1891. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8010h

Figure 3-920. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_STATUS Name Register

15	14	13	12	11	10	9	8
STS							
RO							
0							
7	6	5	4	3	2	1	0
STS							
RO							
0							

Access Types Legend

Table 3-1892. OUTPUTXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	STS	RO	0h	Status

3.16.3 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGINVERT Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1893. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8014h

Figure 3-921. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGINVERT Name Register

15	14	13	12	11	10	9	8
INVERT							
RW							
0							
7	6	5	4	3	2	1	0
INVERT							
RW							
0							

Access Types Legend

Table 3-1894. OUTPUTXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	INVERT	RW	0h	FlagInvert

3.16.4 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1895. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8018h

Figure 3-922. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG Name Register

15	14	13	12	11	10	9	8
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-1896. OUTPUTXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15	RW	0h	output xbar flag
14	BIT14	RW	0h	output xbar flag
13	BIT13	RW	0h	output xbar flag
12	BIT12	RW	0h	output xbar flag
11	BIT11	RW	0h	output xbar flag
10	BIT10	RW	0h	output xbar flag
9	BIT9	RW	0h	output xbar flag
8	BIT8	RW	0h	output xbar flag
7	BIT7	RW	0h	output xbar flag
6	BIT6	RW	0h	output xbar flag
5	BIT5	RW	0h	output xbar flag
4	BIT4	RW	0h	output xbar flag
3	BIT3	RW	0h	output xbar flag
2	BIT2	RW	0h	output xbar flag
1	BIT1	RW	0h	output xbar flag
0	BIT0	RW	0h	output xbar flag

3.16.5 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1897. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 801Ch

Figure 3-923. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAG_CLR Name Register

15	14	13	12	11	10	9	8
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-1898. OUTPUTXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15	RW	0h	output xbar flag clear
14	BIT14	RW	0h	output xbar flag clear
13	BIT13	RW	0h	output xbar flag clear
12	BIT12	RW	0h	output xbar flag clear
11	BIT11	RW	0h	output xbar flag clear
10	BIT10	RW	0h	output xbar flag clear
9	BIT9	RW	0h	output xbar flag clear
8	BIT8	RW	0h	output xbar flag clear
7	BIT7	RW	0h	output xbar flag clear
6	BIT6	RW	0h	output xbar flag clear
5	BIT5	RW	0h	output xbar flag clear
4	BIT4	RW	0h	output xbar flag clear
3	BIT3	RW	0h	output xbar flag clear
2	BIT2	RW	0h	output xbar flag clear
1	BIT1	RW	0h	output xbar flag clear
0	BIT0	RW	0h	output xbar flag clear

3.16.6 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGFORCE Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1899. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8020h

Figure 3-924. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_FLAGFORCE Name Register

15	14	13	12	11	10	9	8
FRC							
RW							
0							
7	6	5	4	3	2	1	0
FRC							
RW							
0							

Access Types Legend

Table 3-1900. OUTPUTXBAR_FLAGFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FRC	RW	0h	FlagForce

3.16.7 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLATCH Register (Offset = 24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1901. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8024h

Figure 3-925. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLATCH Name Register

15	14	13	12	11	10	9	8
LATCHSEL							
RW							
0							
7	6	5	4	3	2	1	0
LATCHSEL							
RW							
0							

Access Types Legend

Table 3-1902. OUTPUTXBAR_OUTLATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LATCHSEL	RW	0h	OutLatch

3.16.8 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTSTRETCH Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1903. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8028h

Figure 3-926. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTSTRETCH Name Register

15	14	13	12	11	10	9	8
STRETCHSEL							
RW							
0							
7	6	5	4	3	2	1	0
STRETCHSEL							
RW							
0							

Access Types Legend

Table 3-1904. OUTPUTXBAR_OUTSTRETCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	STRETCHSEL	RW	0h	OutStretch

3.16.9 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLENGTH Register (Offset = 2Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1905. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 802Ch

Figure 3-927. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTLENGTH Name Register

15	14	13	12	11	10	9	8
LENGTHSEL							
RW							
0							
7	6	5	4	3	2	1	0
LENGTHSEL							
RW							
0							

Access Types Legend

Table 3-1906. OUTPUTXBAR_OUTLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LENGTHSEL	RW	0h	OutLength

3.16.10 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTINVERT Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1907. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8030h

Figure 3-928. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR_OUTINVERT Name Register

15	14	13	12	11	10	9	8
OUTINVERT							
RW							
0							
7	6	5	4	3	2	1	0
OUTINVERT							
RW							
0							

Access Types Legend

Table 3-1908. OUTPUTXBAR_OUTINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OUTINVERT	RW	0h	OutInvert

3.16.11 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1909. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8100h

Figure 3-929. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1910. OUTPUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar0 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.12 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1911. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8104h

Figure 3-930. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1912. OUTPUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar0 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.13 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1913. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8108h

Figure 3-931. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1914. OUTPUTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar0 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.14 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1915. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 810Ch

Figure 3-932. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1916. OUTPUTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar0 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.15 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1917. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8110h

Figure 3-933. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1918. OUTPUTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar0 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.16 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1919. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8114h

Figure 3-934. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1920. OUTPUTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar0 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.17 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1921. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8118h

Figure 3-935. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1922. OUTPUTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar0 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.18 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G7 Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1923. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 811Ch

Figure 3-936. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1924. OUTPUTXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar0 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.19 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G8 Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1925. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8120h

Figure 3-937. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1926. OUTPUTXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar0 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.20 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G9 Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

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Table 3-1927. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8124h

Figure 3-938. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1928. OUTPUTXBAR0_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar0 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.21 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G10 Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1929. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8128h

Figure 3-939. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR0_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1930. OUTPUTXBAR0_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar0 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.22 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1931. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8140h

Figure 3-940. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1932. OUTPUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar1 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.23 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G1 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1933. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8144h

Figure 3-941. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1934. OUTPUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar1 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.24 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G2 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1935. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8148h

Figure 3-942. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1936. OUTPUTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar1 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.25 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G3 Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1937. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 814Ch

Figure 3-943. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1938. OUTPUTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar1 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.26 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G4 Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1939. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8150h

Figure 3-944. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1940. OUTPUTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar1 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.27 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G5 Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1941. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8154h

Figure 3-945. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1942. OUTPUTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar1 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.28 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G6 Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1943. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8158h

Figure 3-946. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1944. OUTPUTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar1 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.29 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G7 Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1945. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 815Ch

Figure 3-947. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1946. OUTPUTXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar1 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.30 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G8 Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1947. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8160h

Figure 3-948. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1948. OUTPUTXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar1 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.31 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G9 Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1949. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8164h

Figure 3-949. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1950. OUTPUTXBAR1_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar1 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.32 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G10 Register (Offset = 168h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1951. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8168h

Figure 3-950. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR1_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1952. OUTPUTXBAR1_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar1 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.33 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1953. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8180h

Figure 3-951. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1954. OUTPUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar2 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.34 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G1 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1955. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8184h

Figure 3-952. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1956. OUTPUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar2 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.35 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G2 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1957. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8188h

Figure 3-953. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1958. OUTPUTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar2 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.36 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G3 Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1959. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 818Ch

Figure 3-954. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1960. OUTPUTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar2 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.37 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G4 Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1961. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8190h

Figure 3-955. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1962. OUTPUTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar2 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.38 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G5 Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1963. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8194h

Figure 3-956. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1964. OUTPUTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar2 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.39 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G6 Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1965. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8198h

Figure 3-957. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1966. OUTPUTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar2 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.40 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G7 Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1967. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 819Ch

Figure 3-958. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1968. OUTPUTXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar2 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.41 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G8 Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1969. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A0h

Figure 3-959. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1970. OUTPUTXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar2 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.42 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G9 Register (Offset = 1A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1971. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A4h

Figure 3-960. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1972. OUTPUTXBAR2_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar2 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.43 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G10 Register (Offset = 1A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1973. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A8h

Figure 3-961. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR2_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1974. OUTPUTXBAR2_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar2 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.44 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1975. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C0h

Figure 3-962. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1976. OUTPUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar3 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.45 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G1 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1977. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C4h

Figure 3-963. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1978. OUTPUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar3 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.46 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G2 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1979. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C8h

Figure 3-964. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1980. OUTPUTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar3 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.47 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G3 Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1981. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81CCh

Figure 3-965. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1982. OUTPUTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar3 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.48 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G4 Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1983. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D0h

Figure 3-966. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1984. OUTPUTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar3 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.49 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G5 Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1985. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D4h

Figure 3-967. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1986. OUTPUTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar3 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.50 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G6 Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1987. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D8h

Figure 3-968. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1988. OUTPUTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar3 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.51 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G7 Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1989. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81DCh

Figure 3-969. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1990. OUTPUTXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar3 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.52 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G8 Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1991. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E0h

Figure 3-970. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1992. OUTPUTXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar3 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.53 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G9 Register (Offset = 1E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1993. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E4h

Figure 3-971. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1994. OUTPUTXBAR3_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar3 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.54 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G10 Register (Offset = 1E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1995. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E8h

Figure 3-972. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR3_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-1996. OUTPUTXBAR3_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar3 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.55 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G0 Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1997. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8200h

Figure 3-973. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-1998. OUTPUTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar4 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.56 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G1 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1999. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8204h

Figure 3-974. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2000. OUTPUTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar4 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.57 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G2 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2001. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8208h

Figure 3-975. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2002. OUTPUTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar4 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.58 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G3 Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2003. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 820Ch

Figure 3-976. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2004. OUTPUTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar4 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.59 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G4 Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2005. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8210h

Figure 3-977. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2006. OUTPUTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar4 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.60 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G5 Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2007. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8214h

Figure 3-978. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2008. OUTPUTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar4 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.61 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G6 Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2009. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8218h

Figure 3-979. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2010. OUTPUTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar4 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.62 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G7 Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2011. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 821Ch

Figure 3-980. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2012. OUTPUTXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar4 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.63 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G8 Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2013. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8220h

Figure 3-981. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2014. OUTPUTXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar4 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.64 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G9 Register (Offset = 224h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2015. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8224h

Figure 3-982. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2016. OUTPUTXBAR4_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar4 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.65 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G10 Register (Offset = 228h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2017. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8228h

Figure 3-983. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR4_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2018. OUTPUTXBAR4_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar4 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.66 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G0 Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2019. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8240h

Figure 3-984. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2020. OUTPUTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar5 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.67 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G1 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2021. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8244h

Figure 3-985. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2022. OUTPUTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar5 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.68 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G2 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2023. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8248h

Figure 3-986. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2024. OUTPUTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar5 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.69 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G3 Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2025. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 824Ch

Figure 3-987. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2026. OUTPUTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar5 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.70 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G4 Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2027. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8250h

Figure 3-988. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2028. OUTPUTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar5 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.71 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G5 Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2029. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8254h

Figure 3-989. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2030. OUTPUTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar5 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.72 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G6 Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2031. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8258h

Figure 3-990. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2032. OUTPUTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar5 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.73 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G7 Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2033. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 825Ch

Figure 3-991. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2034. OUTPUTXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar5 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.74 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G8 Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2035. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8260h

Figure 3-992. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2036. OUTPUTXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar5 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.75 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G9 Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2037. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8264h

Figure 3-993. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2038. OUTPUTXBAR5_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar5 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.76 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G10 Register (Offset = 268h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2039. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8268h

Figure 3-994. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR5_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2040. OUTPUTXBAR5_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar5 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.77 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G0 Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2041. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8280h

Figure 3-995. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2042. OUTPUTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar6 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.78 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G1 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2043. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8284h

Figure 3-996. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2044. OUTPUTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar6 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.79 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G2 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2045. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8288h

Figure 3-997. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2046. OUTPUTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar6 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.80 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G3 Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2047. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 828Ch

Figure 3-998. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2048. OUTPUTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar6 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.81 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G4 Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2049. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8290h

Figure 3-999. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2050. OUTPUTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar6 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.82 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G5 Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2051. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8294h

Figure 3-1000. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2052. OUTPUTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar6 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.83 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G6 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2053. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8298h

Figure 3-1001. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2054. OUTPUTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar6 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.84 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G7 Register (Offset = 29Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2055. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 829Ch

Figure 3-1002. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2056. OUTPUTXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar6 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.85 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G8 Register (Offset = 2A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2057. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A0h

Figure 3-1003. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2058. OUTPUTXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar6 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.86 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G9 Register (Offset = 2A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2059. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A4h

Figure 3-1004. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2060. OUTPUTXBAR6_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar6 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.87 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G10 Register (Offset = 2A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2061. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A8h

Figure 3-1005. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR6_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2062. OUTPUTXBAR6_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar6 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.88 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G0 Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2063. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C0h

Figure 3-1006. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2064. OUTPUTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar7 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.89 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G1 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2065. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C4h

Figure 3-1007. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2066. OUTPUTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar7 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.90 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G2 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2067. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C8h

Figure 3-1008. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2068. OUTPUTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar7 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.91 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G3 Register (Offset = 2CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2069. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82CCh

Figure 3-1009. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2070. OUTPUTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar7 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.92 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G4 Register (Offset = 2D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2071. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D0h

Figure 3-1010. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2072. OUTPUTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar7 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.93 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G5 Register (Offset = 2D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2073. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D4h

Figure 3-1011. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2074. OUTPUTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar7 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.94 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G6 Register (Offset = 2D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2075. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D8h

Figure 3-1012. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2076. OUTPUTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar7 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.95 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G7 Register (Offset = 2DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2077. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82DCh

Figure 3-1013. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2078. OUTPUTXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar7 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.96 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G8 Register (Offset = 2E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2079. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E0h

Figure 3-1014. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2080. OUTPUTXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar7 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.97 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G9 Register (Offset = 2E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2081. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E4h

Figure 3-1015. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2082. OUTPUTXBAR7_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar7 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.98 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G10 Register (Offset = 2E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2083. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E8h

Figure 3-1016. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR7_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2084. OUTPUTXBAR7_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar7 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.99 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G0 Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2085. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8300h

Figure 3-1017. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2086. OUTPUTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar8 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.100 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G1 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2087. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8304h

Figure 3-1018. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2088. OUTPUTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar8 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.101 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G2 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2089. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8308h

Figure 3-1019. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2090. OUTPUTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar8 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.102 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G3 Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2091. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 830Ch

Figure 3-1020. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2092. OUTPUTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar8 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.103 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G4 Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2093. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8310h

Figure 3-1021. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2094. OUTPUTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar8 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.104 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G5 Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2095. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8314h

Figure 3-1022. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2096. OUTPUTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar8 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.105 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G6 Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2097. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8318h

Figure 3-1023. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2098. OUTPUTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar8 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.106 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G7 Register (Offset = 31Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2099. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 831Ch

Figure 3-1024. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2100. OUTPUTXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar8 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.107 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G8 Register (Offset = 320h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2101. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8320h

Figure 3-1025. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2102. OUTPUTXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar8 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.108 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G9 Register (Offset = 324h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2103. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8324h

Figure 3-1026. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2104. OUTPUTXBAR8_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar8 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.109 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G10 Register (Offset = 328h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2105. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8328h

Figure 3-1027. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR8_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2106. OUTPUTXBAR8_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar8 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.110 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G0 Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2107. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8340h

Figure 3-1028. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2108. OUTPUTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar9 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.111 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G1 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2109. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8344h

Figure 3-1029. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2110. OUTPUTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar9 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.112 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G2 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2111. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8348h

Figure 3-1030. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2112. OUTPUTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar9 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.113 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G3 Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2113. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 834Ch

Figure 3-1031. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2114. OUTPUTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar9 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.114 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G4 Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2115. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8350h

Figure 3-1032. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2116. OUTPUTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar9 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.115 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G5 Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2117. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8354h

Figure 3-1033. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2118. OUTPUTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar9 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.116 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G6 Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2119. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8358h

Figure 3-1034. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2120. OUTPUTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar9 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.117 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G7 Register (Offset = 35Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2121. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 835Ch

Figure 3-1035. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2122. OUTPUTXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar9 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.118 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G8 Register (Offset = 360h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2123. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8360h

Figure 3-1036. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2124. OUTPUTXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar9 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.119 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G9 Register (Offset = 364h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2125. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8364h

Figure 3-1037. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2126. OUTPUTXBAR9_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar9 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.120 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G10 Register (Offset = 368h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2127. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8368h

Figure 3-1038. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR9_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2128. OUTPUTXBAR9_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar9 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.121 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G0 Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2129. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8380h

Figure 3-1039. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2130. OUTPUTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar10 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.122 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G1 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2131. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8384h

Figure 3-1040. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2132. OUTPUTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar10 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.123 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G2 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2133. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8388h

Figure 3-1041. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2134. OUTPUTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar10 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.124 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G3 Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2135. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 838Ch

Figure 3-1042. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2136. OUTPUTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar10 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.125 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G4 Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2137. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8390h

Figure 3-1043. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2138. OUTPUTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar10 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.126 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G5 Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2139. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8394h

Figure 3-1044. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2140. OUTPUTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar10 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.127 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G6 Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2141. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8398h

Figure 3-1045. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2142. OUTPUTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar10 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.128 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G7 Register (Offset = 39Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2143. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 839Ch

Figure 3-1046. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2144. OUTPUTXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar10 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.129 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G8 Register (Offset = 3A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2145. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A0h

Figure 3-1047. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2146. OUTPUTXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar10 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.130 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G9 Register (Offset = 3A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2147. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A4h

Figure 3-1048. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2148. OUTPUTXBAR10_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar10 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.131 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G10 Register (Offset = 3A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2149. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A8h

Figure 3-1049. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR10_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2150. OUTPUTXBAR10_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar10 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.132 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G0 Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2151. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C0h

Figure 3-1050. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2152. OUTPUTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar11 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.133 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G1 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2153. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C4h

Figure 3-1051. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2154. OUTPUTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar11 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.134 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G2 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2155. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C8h

Figure 3-1052. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2156. OUTPUTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar11 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.135 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G3 Register (Offset = 3CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2157. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83CCh

Figure 3-1053. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2158. OUTPUTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar11 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.136 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G4 Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2159. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D0h

Figure 3-1054. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2160. OUTPUTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar11 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.137 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G5 Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2161. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D4h

Figure 3-1055. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2162. OUTPUTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar11 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.138 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G6 Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2163. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D8h

Figure 3-1056. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2164. OUTPUTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar11 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.139 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G7 Register (Offset = 3DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2165. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83DCh

Figure 3-1057. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2166. OUTPUTXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar11 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.140 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G8 Register (Offset = 3E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2167. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E0h

Figure 3-1058. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2168. OUTPUTXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar11 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.141 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G9 Register (Offset = 3E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2169. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E4h

Figure 3-1059. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2170. OUTPUTXBAR11_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar11 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.142 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G10 Register (Offset = 3E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2171. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E8h

Figure 3-1060. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR11_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2172. OUTPUTXBAR11_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar11 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.143 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G0 Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2173. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8400h

Figure 3-1061. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2174. OUTPUTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar12 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.144 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G1 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2175. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8404h

Figure 3-1062. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2176. OUTPUTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar12 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.145 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G2 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2177. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8408h

Figure 3-1063. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2178. OUTPUTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar12 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.146 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G3 Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2179. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 840Ch

Figure 3-1064. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2180. OUTPUTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar12 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.147 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G4 Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2181. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8410h

Figure 3-1065. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2182. OUTPUTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar12 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.148 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G5 Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2183. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8414h

Figure 3-1066. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2184. OUTPUTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar12 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.149 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G6 Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2185. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8418h

Figure 3-1067. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2186. OUTPUTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar12 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.150 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G7 Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2187. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 841Ch

Figure 3-1068. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2188. OUTPUTXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar12 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.151 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G8 Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2189. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8420h

Figure 3-1069. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2190. OUTPUTXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar12 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.152 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G9 Register (Offset = 424h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2191. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8424h

Figure 3-1070. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2192. OUTPUTXBAR12_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar12 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.153 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G10 Register (Offset = 428h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2193. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8428h

Figure 3-1071. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR12_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2194. OUTPUTXBAR12_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar12 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.154 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G0 Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2195. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8440h

Figure 3-1072. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2196. OUTPUTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar13 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.155 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G1 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2197. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8444h

Figure 3-1073. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2198. OUTPUTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar13 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.156 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G2 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2199. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8448h

Figure 3-1074. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2200. OUTPUTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar13 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.157 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G3 Register (Offset = 44Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2201. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 844Ch

Figure 3-1075. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2202. OUTPUTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar13 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.158 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G4 Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2203. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8450h

Figure 3-1076. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2204. OUTPUTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar13 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.159 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G5 Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2205. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8454h

Figure 3-1077. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2206. OUTPUTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar13 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.160 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G6 Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2207. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8458h

Figure 3-1078. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2208. OUTPUTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar13 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.161 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G7 Register (Offset = 45Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2209. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 845Ch

Figure 3-1079. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2210. OUTPUTXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar13 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.162 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G8 Register (Offset = 460h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2211. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8460h

Figure 3-1080. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2212. OUTPUTXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar13 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.163 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G9 Register (Offset = 464h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2213. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8464h

Figure 3-1081. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2214. OUTPUTXBAR13_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar13 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.164 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G10 Register (Offset = 468h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2215. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8468h

Figure 3-1082. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR13_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2216. OUTPUTXBAR13_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar13 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.165 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G0 Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2217. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8480h

Figure 3-1083. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2218. OUTPUTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar14 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.166 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G1 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2219. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8484h

Figure 3-1084. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2220. OUTPUTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar14 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.167 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G2 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2221. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8488h

Figure 3-1085. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2222. OUTPUTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar14 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.168 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G3 Register (Offset = 48Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2223. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 848Ch

Figure 3-1086. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2224. OUTPUTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar14 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.169 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G4 Register (Offset = 490h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2225. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8490h

Figure 3-1087. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2226. OUTPUTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar14 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.170 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G5 Register (Offset = 494h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2227. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8494h

Figure 3-1088. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2228. OUTPUTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar14 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.171 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G6 Register (Offset = 498h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2229. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8498h

Figure 3-1089. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2230. OUTPUTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar14 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.172 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G7 Register (Offset = 49Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2231. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 849Ch

Figure 3-1090. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2232. OUTPUTXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar14 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.173 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G8 Register (Offset = 4A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2233. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A0h

Figure 3-1091. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2234. OUTPUTXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar14 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.174 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G9 Register (Offset = 4A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2235. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A4h

Figure 3-1092. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2236. OUTPUTXBAR14_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar14 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.175 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G10 Register (Offset = 4A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2237. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A8h

Figure 3-1093. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR14_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2238. OUTPUTXBAR14_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar14 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.16.176 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G0 Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2239. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C0h

Figure 3-1094. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2240. OUTPUTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar15 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

3.16.177 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G1 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2241. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C4h

Figure 3-1095. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2242. OUTPUTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar15 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

3.16.178 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G2 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2243. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C8h

Figure 3-1096. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2244. OUTPUTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar15 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

3.16.179 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G3 Register (Offset = 4CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2245. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84CCh

Figure 3-1097. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2246. OUTPUTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar15 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

3.16.180 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G4 Register (Offset = 4D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2247. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D0h

Figure 3-1098. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2248. OUTPUTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar15 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

3.16.181 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G5 Register (Offset = 4D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2249. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D4h

Figure 3-1099. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2250. OUTPUTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar15 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.16.182 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G6 Register (Offset = 4D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2251. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D8h

Figure 3-1100. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2252. OUTPUTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar15 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

3.16.183 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G7 Register (Offset = 4DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2253. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84DCh

Figure 3-1101. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2254. OUTPUTXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar15 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

3.16.184 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G8 Register (Offset = 4E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2255. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E0h

Figure 3-1102. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2256. OUTPUTXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar15 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.16.185 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G9 Register (Offset = 4E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2257. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E4h

Figure 3-1103. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2258. OUTPUTXBAR15_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar15 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

3.16.186 CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G10 Register (Offset = 4E8h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2259. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E8h

Figure 3-1104. CONTROLSS_OUTPUTXBAR_OUTPUTXBAR15_G10 Name Register

15	14	13	12	11	10	9	8
SEL							
RW							
0							
7	6	5	4	3	2	1	0
SEL							
RW							
0							

Access Types Legend

Table 3-2260. OUTPUTXBAR15_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar15 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

Table 3-2261. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.17 C2K_PWMSYNCOUTXBAR Registers

Table 3-2262. CONTROLSS_PWMSYNCOUTXBAR, CONTROLSS_PWMSYNCOUTXBAR_CONTROLSS_PWMSYNCOUTXBAR Registers, Base Address=502D 2000H, Length=4

Offset	Length	Acronym	Register Name	CONTROLSS_PWMSYNCOUTXBAR Physical Address
0h	32	CONTROLSS_PWMSYNCOUTXBAR_PID	PID register	502D 2000h
100h	32	CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR0_G0	RW	502D 2100h
140h	32	CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR1_G0	RW	502D 2140h
180h	32	CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR2_G0	RW	502D 2180h
1C0h	32	CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR3_G0	RW	502D 21C0h

3.17.1 CONTROLSS_PWMSYNCOUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-2263. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2000h

Figure 3-1105. CONTROLSS_PWMSYNCOUTXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-2264. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.17.2 CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2265. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2100h

Figure 3-1106. CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2266. PWMSYNCOUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar0 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

3.17.3 CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2267. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2140h

Figure 3-1107. CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2268. PWMSYNCOUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar1 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

3.17.4 CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2269. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2180h

Figure 3-1108. CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2270. PWMSYNCOUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar2 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

3.17.5 CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2271. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 21C0h

Figure 3-1109. CONTROLSS_PWMSYNCOUTXBAR_PWMSYNCOUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2272. PWMSYNCOUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar3 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

Table 3-2273. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.18 C2K_PWMXBAR Registers

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
0h	32	CONTROLSS_PWMXBAR_PID	PID register	502D 1000h
10h	32	CONTROLSS_PWMXBAR_PWMXBAR_STATUS	RO	502D 1010h
14h	32	CONTROLSS_PWMXBAR_PWMXBAR_FLAGINVERT	RW	502D 1014h
18h	32	CONTROLSS_PWMXBAR_PWMXBAR_FLAG	RW	502D 1018h
1Ch	32	CONTROLSS_PWMXBAR_PWMXBAR_FLAG_CLR	RW	502D 101Ch
100h	24	CONTROLSS_PWMXBAR_PWMXBAR0_G0	RW	502D 1100h
104h	24	CONTROLSS_PWMXBAR_PWMXBAR0_G1	RW	502D 1104h
108h	24	CONTROLSS_PWMXBAR_PWMXBAR0_G2	RW	502D 1108h
10Ch	24	CONTROLSS_PWMXBAR_PWMXBAR0_G3	RW	502D 110Ch
110h	32	CONTROLSS_PWMXBAR_PWMXBAR0_G4	RW	502D 1110h
114h	32	CONTROLSS_PWMXBAR_PWMXBAR0_G5	RW	502D 1114h
118h	32	CONTROLSS_PWMXBAR_PWMXBAR0_G6	RW	502D 1118h
11Ch	32	CONTROLSS_PWMXBAR_PWMXBAR0_G7	RW	502D 111Ch
120h	32	CONTROLSS_PWMXBAR_PWMXBAR0_G8	RW	502D 1120h
140h	24	CONTROLSS_PWMXBAR_PWMXBAR1_G0	RW	502D 1140h
144h	24	CONTROLSS_PWMXBAR_PWMXBAR1_G1	RW	502D 1144h
148h	24	CONTROLSS_PWMXBAR_PWMXBAR1_G2	RW	502D 1148h
14Ch	24	CONTROLSS_PWMXBAR_PWMXBAR1_G3	RW	502D 114Ch
150h	32	CONTROLSS_PWMXBAR_PWMXBAR1_G4	RW	502D 1150h
154h	32	CONTROLSS_PWMXBAR_PWMXBAR1_G5	RW	502D 1154h
158h	32	CONTROLSS_PWMXBAR_PWMXBAR1_G6	RW	502D 1158h
15Ch	32	CONTROLSS_PWMXBAR_PWMXBAR1_G7	RW	502D 115Ch
160h	32	CONTROLSS_PWMXBAR_PWMXBAR1_G8	RW	502D 1160h
180h	24	CONTROLSS_PWMXBAR_PWMXBAR2_G0	RW	502D 1180h
184h	24	CONTROLSS_PWMXBAR_PWMXBAR2_G1	RW	502D 1184h
188h	24	CONTROLSS_PWMXBAR_PWMXBAR2_G2	RW	502D 1188h
18Ch	24	CONTROLSS_PWMXBAR_PWMXBAR2_G3	RW	502D 118Ch
190h	32	CONTROLSS_PWMXBAR_PWMXBAR2_G4	RW	502D 1190h
194h	32	CONTROLSS_PWMXBAR_PWMXBAR2_G5	RW	502D 1194h
198h	32	CONTROLSS_PWMXBAR_PWMXBAR2_G6	RW	502D 1198h
19Ch	32	CONTROLSS_PWMXBAR_PWMXBAR2_G7	RW	502D 119Ch
1A0h	32	CONTROLSS_PWMXBAR_PWMXBAR2_G8	RW	502D 11A0h
1C0h	24	CONTROLSS_PWMXBAR_PWMXBAR3_G0	RW	502D 11C0h
1C4h	24	CONTROLSS_PWMXBAR_PWMXBAR3_G1	RW	502D 11C4h
1C8h	24	CONTROLSS_PWMXBAR_PWMXBAR3_G2	RW	502D 11C8h
1CCh	24	CONTROLSS_PWMXBAR_PWMXBAR3_G3	RW	502D 11CCh

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
1D0h	32	CONTROLSS_PWMXBAR_PWMXBAR3_G4	RW	502D 11D0h
1D4h	32	CONTROLSS_PWMXBAR_PWMXBAR3_G5	RW	502D 11D4h
1D8h	32	CONTROLSS_PWMXBAR_PWMXBAR3_G6	RW	502D 11D8h
1DCh	32	CONTROLSS_PWMXBAR_PWMXBAR3_G7	RW	502D 11DCh
1E0h	32	CONTROLSS_PWMXBAR_PWMXBAR3_G8	RW	502D 11E0h
200h	24	CONTROLSS_PWMXBAR_PWMXBAR4_G0	RW	502D 1200h
204h	24	CONTROLSS_PWMXBAR_PWMXBAR4_G1	RW	502D 1204h
208h	24	CONTROLSS_PWMXBAR_PWMXBAR4_G2	RW	502D 1208h
20Ch	24	CONTROLSS_PWMXBAR_PWMXBAR4_G3	RW	502D 120Ch
210h	32	CONTROLSS_PWMXBAR_PWMXBAR4_G4	RW	502D 1210h
214h	32	CONTROLSS_PWMXBAR_PWMXBAR4_G5	RW	502D 1214h
218h	32	CONTROLSS_PWMXBAR_PWMXBAR4_G6	RW	502D 1218h
21Ch	32	CONTROLSS_PWMXBAR_PWMXBAR4_G7	RW	502D 121Ch
220h	32	CONTROLSS_PWMXBAR_PWMXBAR4_G8	RW	502D 1220h
240h	24	CONTROLSS_PWMXBAR_PWMXBAR5_G0	RW	502D 1240h
244h	24	CONTROLSS_PWMXBAR_PWMXBAR5_G1	RW	502D 1244h
248h	24	CONTROLSS_PWMXBAR_PWMXBAR5_G2	RW	502D 1248h
24Ch	24	CONTROLSS_PWMXBAR_PWMXBAR5_G3	RW	502D 124Ch
250h	32	CONTROLSS_PWMXBAR_PWMXBAR5_G4	RW	502D 1250h
254h	32	CONTROLSS_PWMXBAR_PWMXBAR5_G5	RW	502D 1254h
258h	32	CONTROLSS_PWMXBAR_PWMXBAR5_G6	RW	502D 1258h
25Ch	32	CONTROLSS_PWMXBAR_PWMXBAR5_G7	RW	502D 125Ch
260h	32	CONTROLSS_PWMXBAR_PWMXBAR5_G8	RW	502D 1260h
280h	24	CONTROLSS_PWMXBAR_PWMXBAR6_G0	RW	502D 1280h
284h	24	CONTROLSS_PWMXBAR_PWMXBAR6_G1	RW	502D 1284h
288h	24	CONTROLSS_PWMXBAR_PWMXBAR6_G2	RW	502D 1288h
28Ch	24	CONTROLSS_PWMXBAR_PWMXBAR6_G3	RW	502D 128Ch
290h	32	CONTROLSS_PWMXBAR_PWMXBAR6_G4	RW	502D 1290h
294h	32	CONTROLSS_PWMXBAR_PWMXBAR6_G5	RW	502D 1294h
298h	32	CONTROLSS_PWMXBAR_PWMXBAR6_G6	RW	502D 1298h
29Ch	32	CONTROLSS_PWMXBAR_PWMXBAR6_G7	RW	502D 129Ch
2A0h	32	CONTROLSS_PWMXBAR_PWMXBAR6_G8	RW	502D 12A0h
2C0h	24	CONTROLSS_PWMXBAR_PWMXBAR7_G0	RW	502D 12C0h
2C4h	24	CONTROLSS_PWMXBAR_PWMXBAR7_G1	RW	502D 12C4h
2C8h	24	CONTROLSS_PWMXBAR_PWMXBAR7_G2	RW	502D 12C8h
2CCh	24	CONTROLSS_PWMXBAR_PWMXBAR7_G3	RW	502D 12CCh
2D0h	32	CONTROLSS_PWMXBAR_PWMXBAR7_G4	RW	502D 12D0h
2D4h	32	CONTROLSS_PWMXBAR_PWMXBAR7_G5	RW	502D 12D4h
2D8h	32	CONTROLSS_PWMXBAR_PWMXBAR7_G6	RW	502D 12D8h
2DCh	32	CONTROLSS_PWMXBAR_PWMXBAR7_G7	RW	502D 12DCh
2E0h	32	CONTROLSS_PWMXBAR_PWMXBAR7_G8	RW	502D 12E0h
300h	24	CONTROLSS_PWMXBAR_PWMXBAR8_G0	RW	502D 1300h
304h	24	CONTROLSS_PWMXBAR_PWMXBAR8_G1	RW	502D 1304h
308h	24	CONTROLSS_PWMXBAR_PWMXBAR8_G2	RW	502D 1308h
30Ch	24	CONTROLSS_PWMXBAR_PWMXBAR8_G3	RW	502D 130Ch

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
310h	32	CONTROLSS_PWMXBAR_PWMXBAR8_G4	RW	502D 1310h
314h	32	CONTROLSS_PWMXBAR_PWMXBAR8_G5	RW	502D 1314h
318h	32	CONTROLSS_PWMXBAR_PWMXBAR8_G6	RW	502D 1318h
31Ch	32	CONTROLSS_PWMXBAR_PWMXBAR8_G7	RW	502D 131Ch
320h	32	CONTROLSS_PWMXBAR_PWMXBAR8_G8	RW	502D 1320h
340h	24	CONTROLSS_PWMXBAR_PWMXBAR9_G0	RW	502D 1340h
344h	24	CONTROLSS_PWMXBAR_PWMXBAR9_G1	RW	502D 1344h
348h	24	CONTROLSS_PWMXBAR_PWMXBAR9_G2	RW	502D 1348h
34Ch	24	CONTROLSS_PWMXBAR_PWMXBAR9_G3	RW	502D 134Ch
350h	32	CONTROLSS_PWMXBAR_PWMXBAR9_G4	RW	502D 1350h
354h	32	CONTROLSS_PWMXBAR_PWMXBAR9_G5	RW	502D 1354h
358h	32	CONTROLSS_PWMXBAR_PWMXBAR9_G6	RW	502D 1358h
35Ch	32	CONTROLSS_PWMXBAR_PWMXBAR9_G7	RW	502D 135Ch
360h	32	CONTROLSS_PWMXBAR_PWMXBAR9_G8	RW	502D 1360h
380h	24	CONTROLSS_PWMXBAR_PWMXBAR10_G0	RW	502D 1380h
384h	24	CONTROLSS_PWMXBAR_PWMXBAR10_G1	RW	502D 1384h
388h	24	CONTROLSS_PWMXBAR_PWMXBAR10_G2	RW	502D 1388h
38Ch	24	CONTROLSS_PWMXBAR_PWMXBAR10_G3	RW	502D 138Ch
390h	32	CONTROLSS_PWMXBAR_PWMXBAR10_G4	RW	502D 1390h
394h	32	CONTROLSS_PWMXBAR_PWMXBAR10_G5	RW	502D 1394h
398h	32	CONTROLSS_PWMXBAR_PWMXBAR10_G6	RW	502D 1398h
39Ch	32	CONTROLSS_PWMXBAR_PWMXBAR10_G7	RW	502D 139Ch
3A0h	32	CONTROLSS_PWMXBAR_PWMXBAR10_G8	RW	502D 13A0h
3C0h	24	CONTROLSS_PWMXBAR_PWMXBAR11_G0	RW	502D 13C0h
3C4h	24	CONTROLSS_PWMXBAR_PWMXBAR11_G1	RW	502D 13C4h
3C8h	24	CONTROLSS_PWMXBAR_PWMXBAR11_G2	RW	502D 13C8h
3CCh	24	CONTROLSS_PWMXBAR_PWMXBAR11_G3	RW	502D 13CCh
3D0h	32	CONTROLSS_PWMXBAR_PWMXBAR11_G4	RW	502D 13D0h
3D4h	32	CONTROLSS_PWMXBAR_PWMXBAR11_G5	RW	502D 13D4h
3D8h	32	CONTROLSS_PWMXBAR_PWMXBAR11_G6	RW	502D 13D8h
3DCh	32	CONTROLSS_PWMXBAR_PWMXBAR11_G7	RW	502D 13DCh
3E0h	32	CONTROLSS_PWMXBAR_PWMXBAR11_G8	RW	502D 13E0h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
400h	24	CONTROLSS_PWMXBAR_PWMXBAR12_G0	RW	502D 1400h
404h	24	CONTROLSS_PWMXBAR_PWMXBAR12_G1	RW	502D 1404h
408h	24	CONTROLSS_PWMXBAR_PWMXBAR12_G2	RW	502D 1408h
40Ch	24	CONTROLSS_PWMXBAR_PWMXBAR12_G3	RW	502D 140Ch
410h	32	CONTROLSS_PWMXBAR_PWMXBAR12_G4	RW	502D 1410h
414h	32	CONTROLSS_PWMXBAR_PWMXBAR12_G5	RW	502D 1414h
418h	32	CONTROLSS_PWMXBAR_PWMXBAR12_G6	RW	502D 1418h
41Ch	32	CONTROLSS_PWMXBAR_PWMXBAR12_G7	RW	502D 141Ch
420h	32	CONTROLSS_PWMXBAR_PWMXBAR12_G8	RW	502D 1420h
440h	24	CONTROLSS_PWMXBAR_PWMXBAR13_G0	RW	502D 1440h
444h	24	CONTROLSS_PWMXBAR_PWMXBAR13_G1	RW	502D 1444h
448h	24	CONTROLSS_PWMXBAR_PWMXBAR13_G2	RW	502D 1448h
44Ch	24	CONTROLSS_PWMXBAR_PWMXBAR13_G3	RW	502D 144Ch
450h	32	CONTROLSS_PWMXBAR_PWMXBAR13_G4	RW	502D 1450h
454h	32	CONTROLSS_PWMXBAR_PWMXBAR13_G5	RW	502D 1454h
458h	32	CONTROLSS_PWMXBAR_PWMXBAR13_G6	RW	502D 1458h
45Ch	32	CONTROLSS_PWMXBAR_PWMXBAR13_G7	RW	502D 145Ch
460h	32	CONTROLSS_PWMXBAR_PWMXBAR13_G8	RW	502D 1460h
480h	24	CONTROLSS_PWMXBAR_PWMXBAR14_G0	RW	502D 1480h
484h	24	CONTROLSS_PWMXBAR_PWMXBAR14_G1	RW	502D 1484h
488h	24	CONTROLSS_PWMXBAR_PWMXBAR14_G2	RW	502D 1488h
48Ch	24	CONTROLSS_PWMXBAR_PWMXBAR14_G3	RW	502D 148Ch
490h	32	CONTROLSS_PWMXBAR_PWMXBAR14_G4	RW	502D 1490h
494h	32	CONTROLSS_PWMXBAR_PWMXBAR14_G5	RW	502D 1494h
498h	32	CONTROLSS_PWMXBAR_PWMXBAR14_G6	RW	502D 1498h
49Ch	32	CONTROLSS_PWMXBAR_PWMXBAR14_G7	RW	502D 149Ch
4A0h	32	CONTROLSS_PWMXBAR_PWMXBAR14_G8	RW	502D 14A0h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
4C0h	24	CONTROLSS_PWMXBAR_PWMXBAR15_G 0	RW	502D 14C0h
4C4h	24	CONTROLSS_PWMXBAR_PWMXBAR15_G 1	RW	502D 14C4h
4C8h	24	CONTROLSS_PWMXBAR_PWMXBAR15_G 2	RW	502D 14C8h
4CCh	24	CONTROLSS_PWMXBAR_PWMXBAR15_G 3	RW	502D 14CCh
4D0h	32	CONTROLSS_PWMXBAR_PWMXBAR15_G 4	RW	502D 14D0h
4D4h	32	CONTROLSS_PWMXBAR_PWMXBAR15_G 5	RW	502D 14D4h
4D8h	32	CONTROLSS_PWMXBAR_PWMXBAR15_G 6	RW	502D 14D8h
4DCh	32	CONTROLSS_PWMXBAR_PWMXBAR15_G 7	RW	502D 14DCh
4E0h	32	CONTROLSS_PWMXBAR_PWMXBAR15_G 8	RW	502D 14E0h
500h	24	CONTROLSS_PWMXBAR_PWMXBAR16_G 0	RW	502D 1500h
504h	24	CONTROLSS_PWMXBAR_PWMXBAR16_G 1	RW	502D 1504h
508h	24	CONTROLSS_PWMXBAR_PWMXBAR16_G 2	RW	502D 1508h
50Ch	24	CONTROLSS_PWMXBAR_PWMXBAR16_G 3	RW	502D 150Ch
510h	32	CONTROLSS_PWMXBAR_PWMXBAR16_G 4	RW	502D 1510h
514h	32	CONTROLSS_PWMXBAR_PWMXBAR16_G 5	RW	502D 1514h
518h	32	CONTROLSS_PWMXBAR_PWMXBAR16_G 6	RW	502D 1518h
51Ch	32	CONTROLSS_PWMXBAR_PWMXBAR16_G 7	RW	502D 151Ch
520h	32	CONTROLSS_PWMXBAR_PWMXBAR16_G 8	RW	502D 1520h
540h	24	CONTROLSS_PWMXBAR_PWMXBAR17_G 0	RW	502D 1540h
544h	24	CONTROLSS_PWMXBAR_PWMXBAR17_G 1	RW	502D 1544h
548h	24	CONTROLSS_PWMXBAR_PWMXBAR17_G 2	RW	502D 1548h
54Ch	24	CONTROLSS_PWMXBAR_PWMXBAR17_G 3	RW	502D 154Ch
550h	32	CONTROLSS_PWMXBAR_PWMXBAR17_G 4	RW	502D 1550h
554h	32	CONTROLSS_PWMXBAR_PWMXBAR17_G 5	RW	502D 1554h
558h	32	CONTROLSS_PWMXBAR_PWMXBAR17_G 6	RW	502D 1558h
55Ch	32	CONTROLSS_PWMXBAR_PWMXBAR17_G 7	RW	502D 155Ch
560h	32	CONTROLSS_PWMXBAR_PWMXBAR17_G 8	RW	502D 1560h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
580h	24	CONTROLSS_PWMXBAR_PWMXBAR18_G0	RW	502D 1580h
584h	24	CONTROLSS_PWMXBAR_PWMXBAR18_G1	RW	502D 1584h
588h	24	CONTROLSS_PWMXBAR_PWMXBAR18_G2	RW	502D 1588h
58Ch	24	CONTROLSS_PWMXBAR_PWMXBAR18_G3	RW	502D 158Ch
590h	32	CONTROLSS_PWMXBAR_PWMXBAR18_G4	RW	502D 1590h
594h	32	CONTROLSS_PWMXBAR_PWMXBAR18_G5	RW	502D 1594h
598h	32	CONTROLSS_PWMXBAR_PWMXBAR18_G6	RW	502D 1598h
59Ch	32	CONTROLSS_PWMXBAR_PWMXBAR18_G7	RW	502D 159Ch
5A0h	32	CONTROLSS_PWMXBAR_PWMXBAR18_G8	RW	502D 15A0h
5C0h	24	CONTROLSS_PWMXBAR_PWMXBAR19_G0	RW	502D 15C0h
5C4h	24	CONTROLSS_PWMXBAR_PWMXBAR19_G1	RW	502D 15C4h
5C8h	24	CONTROLSS_PWMXBAR_PWMXBAR19_G2	RW	502D 15C8h
5CCh	24	CONTROLSS_PWMXBAR_PWMXBAR19_G3	RW	502D 15CCh
5D0h	32	CONTROLSS_PWMXBAR_PWMXBAR19_G4	RW	502D 15D0h
5D4h	32	CONTROLSS_PWMXBAR_PWMXBAR19_G5	RW	502D 15D4h
5D8h	32	CONTROLSS_PWMXBAR_PWMXBAR19_G6	RW	502D 15D8h
5DCh	32	CONTROLSS_PWMXBAR_PWMXBAR19_G7	RW	502D 15DCh
5E0h	32	CONTROLSS_PWMXBAR_PWMXBAR19_G8	RW	502D 15E0h
600h	24	CONTROLSS_PWMXBAR_PWMXBAR20_G0	RW	502D 1600h
604h	24	CONTROLSS_PWMXBAR_PWMXBAR20_G1	RW	502D 1604h
608h	24	CONTROLSS_PWMXBAR_PWMXBAR20_G2	RW	502D 1608h
60Ch	24	CONTROLSS_PWMXBAR_PWMXBAR20_G3	RW	502D 160Ch
610h	32	CONTROLSS_PWMXBAR_PWMXBAR20_G4	RW	502D 1610h
614h	32	CONTROLSS_PWMXBAR_PWMXBAR20_G5	RW	502D 1614h
618h	32	CONTROLSS_PWMXBAR_PWMXBAR20_G6	RW	502D 1618h
61Ch	32	CONTROLSS_PWMXBAR_PWMXBAR20_G7	RW	502D 161Ch
620h	32	CONTROLSS_PWMXBAR_PWMXBAR20_G8	RW	502D 1620h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
640h	24	CONTROLSS_PWMXBAR_PWMXBAR21_G0	RW	502D 1640h
644h	24	CONTROLSS_PWMXBAR_PWMXBAR21_G1	RW	502D 1644h
648h	24	CONTROLSS_PWMXBAR_PWMXBAR21_G2	RW	502D 1648h
64Ch	24	CONTROLSS_PWMXBAR_PWMXBAR21_G3	RW	502D 164Ch
650h	32	CONTROLSS_PWMXBAR_PWMXBAR21_G4	RW	502D 1650h
654h	32	CONTROLSS_PWMXBAR_PWMXBAR21_G5	RW	502D 1654h
658h	32	CONTROLSS_PWMXBAR_PWMXBAR21_G6	RW	502D 1658h
65Ch	32	CONTROLSS_PWMXBAR_PWMXBAR21_G7	RW	502D 165Ch
660h	32	CONTROLSS_PWMXBAR_PWMXBAR21_G8	RW	502D 1660h
680h	24	CONTROLSS_PWMXBAR_PWMXBAR22_G0	RW	502D 1680h
684h	24	CONTROLSS_PWMXBAR_PWMXBAR22_G1	RW	502D 1684h
688h	24	CONTROLSS_PWMXBAR_PWMXBAR22_G2	RW	502D 1688h
68Ch	24	CONTROLSS_PWMXBAR_PWMXBAR22_G3	RW	502D 168Ch
690h	32	CONTROLSS_PWMXBAR_PWMXBAR22_G4	RW	502D 1690h
694h	32	CONTROLSS_PWMXBAR_PWMXBAR22_G5	RW	502D 1694h
698h	32	CONTROLSS_PWMXBAR_PWMXBAR22_G6	RW	502D 1698h
69Ch	32	CONTROLSS_PWMXBAR_PWMXBAR22_G7	RW	502D 169Ch
6A0h	32	CONTROLSS_PWMXBAR_PWMXBAR22_G8	RW	502D 16A0h
6C0h	24	CONTROLSS_PWMXBAR_PWMXBAR23_G0	RW	502D 16C0h
6C4h	24	CONTROLSS_PWMXBAR_PWMXBAR23_G1	RW	502D 16C4h
6C8h	24	CONTROLSS_PWMXBAR_PWMXBAR23_G2	RW	502D 16C8h
6CCh	24	CONTROLSS_PWMXBAR_PWMXBAR23_G3	RW	502D 16CCh
6D0h	32	CONTROLSS_PWMXBAR_PWMXBAR23_G4	RW	502D 16D0h
6D4h	32	CONTROLSS_PWMXBAR_PWMXBAR23_G5	RW	502D 16D4h
6D8h	32	CONTROLSS_PWMXBAR_PWMXBAR23_G6	RW	502D 16D8h
6DCh	32	CONTROLSS_PWMXBAR_PWMXBAR23_G7	RW	502D 16DCh
6E0h	32	CONTROLSS_PWMXBAR_PWMXBAR23_G8	RW	502D 16E0h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
700h	24	CONTROLSS_PWMXBAR_PWMXBAR24_G0	RW	502D 1700h
704h	24	CONTROLSS_PWMXBAR_PWMXBAR24_G1	RW	502D 1704h
708h	24	CONTROLSS_PWMXBAR_PWMXBAR24_G2	RW	502D 1708h
70Ch	24	CONTROLSS_PWMXBAR_PWMXBAR24_G3	RW	502D 170Ch
710h	32	CONTROLSS_PWMXBAR_PWMXBAR24_G4	RW	502D 1710h
714h	32	CONTROLSS_PWMXBAR_PWMXBAR24_G5	RW	502D 1714h
718h	32	CONTROLSS_PWMXBAR_PWMXBAR24_G6	RW	502D 1718h
71Ch	32	CONTROLSS_PWMXBAR_PWMXBAR24_G7	RW	502D 171Ch
720h	32	CONTROLSS_PWMXBAR_PWMXBAR24_G8	RW	502D 1720h
740h	24	CONTROLSS_PWMXBAR_PWMXBAR25_G0	RW	502D 1740h
744h	24	CONTROLSS_PWMXBAR_PWMXBAR25_G1	RW	502D 1744h
748h	24	CONTROLSS_PWMXBAR_PWMXBAR25_G2	RW	502D 1748h
74Ch	24	CONTROLSS_PWMXBAR_PWMXBAR25_G3	RW	502D 174Ch
750h	32	CONTROLSS_PWMXBAR_PWMXBAR25_G4	RW	502D 1750h
754h	32	CONTROLSS_PWMXBAR_PWMXBAR25_G5	RW	502D 1754h
758h	32	CONTROLSS_PWMXBAR_PWMXBAR25_G6	RW	502D 1758h
75Ch	32	CONTROLSS_PWMXBAR_PWMXBAR25_G7	RW	502D 175Ch
760h	32	CONTROLSS_PWMXBAR_PWMXBAR25_G8	RW	502D 1760h
780h	24	CONTROLSS_PWMXBAR_PWMXBAR26_G0	RW	502D 1780h
784h	24	CONTROLSS_PWMXBAR_PWMXBAR26_G1	RW	502D 1784h
788h	24	CONTROLSS_PWMXBAR_PWMXBAR26_G2	RW	502D 1788h
78Ch	24	CONTROLSS_PWMXBAR_PWMXBAR26_G3	RW	502D 178Ch
790h	32	CONTROLSS_PWMXBAR_PWMXBAR26_G4	RW	502D 1790h
794h	32	CONTROLSS_PWMXBAR_PWMXBAR26_G5	RW	502D 1794h
798h	32	CONTROLSS_PWMXBAR_PWMXBAR26_G6	RW	502D 1798h
79Ch	32	CONTROLSS_PWMXBAR_PWMXBAR26_G7	RW	502D 179Ch
7A0h	32	CONTROLSS_PWMXBAR_PWMXBAR26_G8	RW	502D 17A0h

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
7C0h	24	CONTROLSS_PWMXBAR_PWMXBAR27_G 0	RW	502D 17C0h
7C4h	24	CONTROLSS_PWMXBAR_PWMXBAR27_G 1	RW	502D 17C4h
7C8h	24	CONTROLSS_PWMXBAR_PWMXBAR27_G 2	RW	502D 17C8h
7CCh	24	CONTROLSS_PWMXBAR_PWMXBAR27_G 3	RW	502D 17CCh
7D0h	32	CONTROLSS_PWMXBAR_PWMXBAR27_G 4	RW	502D 17D0h
7D4h	32	CONTROLSS_PWMXBAR_PWMXBAR27_G 5	RW	502D 17D4h
7D8h	32	CONTROLSS_PWMXBAR_PWMXBAR27_G 6	RW	502D 17D8h
7DCh	32	CONTROLSS_PWMXBAR_PWMXBAR27_G 7	RW	502D 17DCh
7E0h	32	CONTROLSS_PWMXBAR_PWMXBAR27_G 8	RW	502D 17E0h
800h	24	CONTROLSS_PWMXBAR_PWMXBAR28_G 0	RW	502D 1800h
804h	24	CONTROLSS_PWMXBAR_PWMXBAR28_G 1	RW	502D 1804h
808h	24	CONTROLSS_PWMXBAR_PWMXBAR28_G 2	RW	502D 1808h
80Ch	24	CONTROLSS_PWMXBAR_PWMXBAR28_G 3	RW	502D 180Ch
810h	32	CONTROLSS_PWMXBAR_PWMXBAR28_G 4	RW	502D 1810h
814h	32	CONTROLSS_PWMXBAR_PWMXBAR28_G 5	RW	502D 1814h
818h	32	CONTROLSS_PWMXBAR_PWMXBAR28_G 6	RW	502D 1818h
81Ch	32	CONTROLSS_PWMXBAR_PWMXBAR28_G 7	RW	502D 181Ch
820h	32	CONTROLSS_PWMXBAR_PWMXBAR28_G 8	RW	502D 1820h
840h	24	CONTROLSS_PWMXBAR_PWMXBAR29_G 0	RW	502D 1840h
844h	24	CONTROLSS_PWMXBAR_PWMXBAR29_G 1	RW	502D 1844h
848h	24	CONTROLSS_PWMXBAR_PWMXBAR29_G 2	RW	502D 1848h
84Ch	24	CONTROLSS_PWMXBAR_PWMXBAR29_G 3	RW	502D 184Ch
850h	32	CONTROLSS_PWMXBAR_PWMXBAR29_G 4	RW	502D 1850h
854h	32	CONTROLSS_PWMXBAR_PWMXBAR29_G 5	RW	502D 1854h
858h	32	CONTROLSS_PWMXBAR_PWMXBAR29_G 6	RW	502D 1858h
85Ch	32	CONTROLSS_PWMXBAR_PWMXBAR29_G 7	RW	502D 185Ch

Table 3-2274. CONTROLSS_PWMXBAR, CONTROLSS_PWMXBAR_CONTROLSS_PWMXBAR Registers, Base Address=502D 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_PWMXBAR Physical Address
860h	32	CONTROLSS_PWMXBAR_PWMXBAR29_G8	RW	502D 1860h

3.18.1 CONTROLSS_PWMXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

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Table 3-2275. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1000h

Figure 3-1110. CONTROLSS_PWMXBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PID_MSB16															
RO															
110000110000000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MISC					PID_MAJOR			PID_CUSTOM		PID_MINOR					
RO					RO			RO		RO					
0					10			0		10100					

Access Types Legend

Table 3-2276. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

3.18.2 CONTROLSS_PWMXBAR_PWMXBAR_STATUS Register (Offset = 10h) [reset = h]

Short Description: RO

Long Description:

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Table 3-2277. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1010h

Figure 3-1111. CONTROLSS_PWMXBAR_PWMXBAR_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		STS													
NONE		RO													
0		0													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 3-2278. PWMXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	STS	RO	0h	Output Signal Status

3.18.3 CONTROLSS_PWMXBAR_PWMXBAR_FLAGINVERT Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2279. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1014h

Figure 3-1112. CONTROLSS_PWMXBAR_PWMXBAR_FLAGINVERT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		INVERT													
NONE		RW													
0		0													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INVERT															
RW															
0															

Access Types Legend

Table 3-2280. PWMXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	INVERT	RW	0h	Output Signal Invert Before Latch

3.18.4 CONTROLSS_PWMXBAR_PWMXBAR_FLAG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2281. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1018h

Figure 3-1113. CONTROLSS_PWMXBAR_PWMXBAR_FLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
NONE		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 3-2282. PWMXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29	BIT29	RW	0h	Output Signal Latched Flag
28	BIT28	RW	0h	Output Signal Latched Flag
27	BIT27	RW	0h	Output Signal Latched Flag
26	BIT26	RW	0h	Output Signal Latched Flag
25	BIT25	RW	0h	Output Signal Latched Flag
24	BIT24	RW	0h	Output Signal Latched Flag
23	BIT23	RW	0h	Output Signal Latched Flag
22	BIT22	RW	0h	Output Signal Latched Flag
21	BIT21	RW	0h	Output Signal Latched Flag
20	BIT20	RW	0h	Output Signal Latched Flag
19	BIT19	RW	0h	Output Signal Latched Flag
18	BIT18	RW	0h	Output Signal Latched Flag
17	BIT17	RW	0h	Output Signal Latched Flag
16	BIT16	RW	0h	Output Signal Latched Flag
15	BIT15	RW	0h	Output Signal Latched Flag
14	BIT14	RW	0h	Output Signal Latched Flag
13	BIT13	RW	0h	Output Signal Latched Flag
12	BIT12	RW	0h	Output Signal Latched Flag
11	BIT11	RW	0h	Output Signal Latched Flag
10	BIT10	RW	0h	Output Signal Latched Flag
9	BIT9	RW	0h	Output Signal Latched Flag
8	BIT8	RW	0h	Output Signal Latched Flag
7	BIT7	RW	0h	Output Signal Latched Flag
6	BIT6	RW	0h	Output Signal Latched Flag
5	BIT5	RW	0h	Output Signal Latched Flag
4	BIT4	RW	0h	Output Signal Latched Flag

Table 3-2282. PWMXBAR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BIT3	RW	0h	Output Signal Latched Flag
2	BIT2	RW	0h	Output Signal Latched Flag
1	BIT1	RW	0h	Output Signal Latched Flag
0	BIT0	RW	0h	Output Signal Latched Flag

3.18.5 CONTROLSS_PWMXBAR_PWMXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

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Table 3-2283. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 101Ch

Figure 3-1114. CONTROLSS_PWMXBAR_PWMXBAR_FLAG_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
NONE		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 3-2284. PWMXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29	BIT29	RW	0h	Output Signal Latched Flag Clear
28	BIT28	RW	0h	Output Signal Latched Flag Clear
27	BIT27	RW	0h	Output Signal Latched Flag Clear
26	BIT26	RW	0h	Output Signal Latched Flag Clear
25	BIT25	RW	0h	Output Signal Latched Flag Clear
24	BIT24	RW	0h	Output Signal Latched Flag Clear
23	BIT23	RW	0h	Output Signal Latched Flag Clear
22	BIT22	RW	0h	Output Signal Latched Flag Clear
21	BIT21	RW	0h	Output Signal Latched Flag Clear
20	BIT20	RW	0h	Output Signal Latched Flag Clear
19	BIT19	RW	0h	Output Signal Latched Flag Clear
18	BIT18	RW	0h	Output Signal Latched Flag Clear
17	BIT17	RW	0h	Output Signal Latched Flag Clear
16	BIT16	RW	0h	Output Signal Latched Flag Clear
15	BIT15	RW	0h	Output Signal Latched Flag Clear
14	BIT14	RW	0h	Output Signal Latched Flag Clear
13	BIT13	RW	0h	Output Signal Latched Flag Clear
12	BIT12	RW	0h	Output Signal Latched Flag Clear
11	BIT11	RW	0h	Output Signal Latched Flag Clear
10	BIT10	RW	0h	Output Signal Latched Flag Clear
9	BIT9	RW	0h	Output Signal Latched Flag Clear
8	BIT8	RW	0h	Output Signal Latched Flag Clear
7	BIT7	RW	0h	Output Signal Latched Flag Clear
6	BIT6	RW	0h	Output Signal Latched Flag Clear
5	BIT5	RW	0h	Output Signal Latched Flag Clear
4	BIT4	RW	0h	Output Signal Latched Flag Clear

Table 3-2284. PWMXBAR_FLAG_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BIT3	RW	0h	Output Signal Latched Flag Clear
2	BIT2	RW	0h	Output Signal Latched Flag Clear
1	BIT1	RW	0h	Output Signal Latched Flag Clear
0	BIT0	RW	0h	Output Signal Latched Flag Clear

3.18.6 CONTROLSS_PWMXBAR_PWMXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2285. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1100h

Figure 3-1115. CONTROLSS_PWMXBAR_PWMXBAR0_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2286. PWMXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.7 CONTROLSS_PWMXBAR_PWMXBAR0_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2287. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1104h

Figure 3-1116. CONTROLSS_PWMXBAR_PWMXBAR0_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2288. PWMXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.8 CONTROLSS_PWMXBAR_PWMXBAR0_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2289. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1108h

Figure 3-1117. CONTROLSS_PWMXBAR_PWMXBAR0_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2290. PWMXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar0 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.9 CONTROLSS_PWMXBAR_PWMXBAR0_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2291. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 110Ch

Figure 3-1118. CONTROLSS_PWMXBAR_PWMXBAR0_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2292. PWMXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.10 CONTROLSS_PWMXBAR_PWMXBAR0_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2293. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1110h

Figure 3-1119. CONTROLSS_PWMXBAR_PWMXBAR0_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2294. PWMXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.11 CONTROLSS_PWMXBAR_PWMXBAR0_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2295. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1114h

Figure 3-1120. CONTROLSS_PWMXBAR_PWMXBAR0_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2296. PWMXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.12 CONTROLSS_PWMXBAR_PWMXBAR0_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2297. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1118h

Figure 3-1121. CONTROLSS_PWMXBAR_PWMXBAR0_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2298. PWMXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.13 CONTROLSS_PWMXBAR_PWMXBAR0_G7 Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2299. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 111Ch

Figure 3-1122. CONTROLSS_PWMXBAR_PWMXBAR0_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2300. PWMXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.14 CONTROLSS_PWMXBAR_PWMXBAR0_G8 Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2301. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1120h

Figure 3-1123. CONTROLSS_PWMXBAR_PWMXBAR0_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2302. PWMXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar0 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG428:19: ECAP[9:0].TRIPOUT

3.18.15 CONTROLSS_PWMXBAR_PWMXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2303. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1140h

Figure 3-1124. CONTROLSS_PWMXBAR_PWMXBAR1_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2304. PWMXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar1 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.16 CONTROLSS_PWMXBAR_PWMXBAR1_G1 Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2305. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1144h

Figure 3-1125. CONTROLSS_PWMXBAR_PWMXBAR1_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2306. PWMXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar1 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.17 CONTROLSS_PWMXBAR_PWMXBAR1_G2 Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2307. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1148h

Figure 3-1126. CONTROLSS_PWMXBAR_PWMXBAR1_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2308. PWMXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar1 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.18 CONTROLSS_PWMXBAR_PWMXBAR1_G3 Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2309. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 114Ch

Figure 3-1127. CONTROLSS_PWMXBAR_PWMXBAR1_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2310. PWMXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar1 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.19 CONTROLSS_PWMXBAR_PWMXBAR1_G4 Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2311. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1150h

Figure 3-1128. CONTROLSS_PWMXBAR_PWMXBAR1_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2312. PWMXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar1 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.20 CONTROLSS_PWMXBAR_PWMXBAR1_G5 Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2313. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1154h

Figure 3-1129. CONTROLSS_PWMXBAR_PWMXBAR1_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2314. PWMXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar1 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.21 CONTROLSS_PWMXBAR_PWMXBAR1_G6 Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2315. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1158h

Figure 3-1130. CONTROLSS_PWMXBAR_PWMXBAR1_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2316. PWMXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar1 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.22 CONTROLSS_PWMXBAR_PWMXBAR1_G7 Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2317. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 115Ch

Figure 3-1131. CONTROLSS_PWMXBAR_PWMXBAR1_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2318. PWMXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar1 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.23 CONTROLSS_PWMXBAR_PWMXBAR1_G8 Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2319. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1160h

Figure 3-1132. CONTROLSS_PWMXBAR_PWMXBAR1_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2320. PWMXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar1 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.24 CONTROLSS_PWMXBAR_PWMXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2321. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1180h

Figure 3-1133. CONTROLSS_PWMXBAR_PWMXBAR2_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2322. PWMXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar2 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.25 CONTROLSS_PWMXBAR_PWMXBAR2_G1 Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2323. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1184h

Figure 3-1134. CONTROLSS_PWMXBAR_PWMXBAR2_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2324. PWMXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar2 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.26 CONTROLSS_PWMXBAR_PWMXBAR2_G2 Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2325. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1188h

Figure 3-1135. CONTROLSS_PWMXBAR_PWMXBAR2_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2326. PWMXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar2 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.27 CONTROLSS_PWMXBAR_PWMXBAR2_G3 Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2327. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 118Ch

Figure 3-1136. CONTROLSS_PWMXBAR_PWMXBAR2_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2328. PWMXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar2 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.28 CONTROLSS_PWMXBAR_PWMXBAR2_G4 Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2329. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1190h

Figure 3-1137. CONTROLSS_PWMXBAR_PWMXBAR2_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2330. PWMXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar2 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.29 CONTROLSS_PWMXBAR_PWMXBAR2_G5 Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2331. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1194h

Figure 3-1138. CONTROLSS_PWMXBAR_PWMXBAR2_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2332. PWMXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar2 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.30 CONTROLSS_PWMXBAR_PWMXBAR2_G6 Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2333. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1198h

Figure 3-1139. CONTROLSS_PWMXBAR_PWMXBAR2_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2334. PWMXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar2 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.31 CONTROLSS_PWMXBAR_PWMXBAR2_G7 Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2335. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 119Ch

Figure 3-1140. CONTROLSS_PWMXBAR_PWMXBAR2_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2336. PWMXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar2 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.32 CONTROLSS_PWMXBAR_PWMXBAR2_G8 Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2337. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11A0h

Figure 3-1141. CONTROLSS_PWMXBAR_PWMXBAR2_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2338. PWMXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar2 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.33 CONTROLSS_PWMXBAR_PWMXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2339. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C0h

Figure 3-1142. CONTROLSS_PWMXBAR_PWMXBAR3_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2340. PWMXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar3 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.34 CONTROLSS_PWMXBAR_PWMXBAR3_G1 Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2341. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C4h

Figure 3-1143. CONTROLSS_PWMXBAR_PWMXBAR3_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2342. PWMXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar3 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.35 CONTROLSS_PWMXBAR_PWMXBAR3_G2 Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2343. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C8h

Figure 3-1144. CONTROLSS_PWMXBAR_PWMXBAR3_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2344. PWMXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar3 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.36 CONTROLSS_PWMXBAR_PWMXBAR3_G3 Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2345. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11CCh

Figure 3-1145. CONTROLSS_PWMXBAR_PWMXBAR3_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2346. PWMXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar3 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.37 CONTROLSS_PWMXBAR_PWMXBAR3_G4 Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2347. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D0h

Figure 3-1146. CONTROLSS_PWMXBAR_PWMXBAR3_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2348. PWMXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar3 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.38 CONTROLSS_PWMXBAR_PWMXBAR3_G5 Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2349. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D4h

Figure 3-1147. CONTROLSS_PWMXBAR_PWMXBAR3_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2350. PWMXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar3 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.39 CONTROLSS_PWMXBAR_PWMXBAR3_G6 Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2351. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D8h

Figure 3-1148. CONTROLSS_PWMXBAR_PWMXBAR3_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2352. PWMXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar3 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.40 CONTROLSS_PWMXBAR_PWMXBAR3_G7 Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2353. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11DCh

Figure 3-1149. CONTROLSS_PWMXBAR_PWMXBAR3_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2354. PWMXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar3 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.41 CONTROLSS_PWMXBAR_PWMXBAR3_G8 Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2355. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11E0h

Figure 3-1150. CONTROLSS_PWMXBAR_PWMXBAR3_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2356. PWMXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar3 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.42 CONTROLSS_PWMXBAR_PWMXBAR4_G0 Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2357. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1200h

Figure 3-1151. CONTROLSS_PWMXBAR_PWMXBAR4_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2358. PWMXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar4 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.43 CONTROLSS_PWMXBAR_PWMXBAR4_G1 Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2359. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1204h

Figure 3-1152. CONTROLSS_PWMXBAR_PWMXBAR4_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2360. PWMXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar4 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.44 CONTROLSS_PWMXBAR_PWMXBAR4_G2 Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2361. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1208h

Figure 3-1153. CONTROLSS_PWMXBAR_PWMXBAR4_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2362. PWMXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar4 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.45 CONTROLSS_PWMXBAR_PWMXBAR4_G3 Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2363. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 120Ch

Figure 3-1154. CONTROLSS_PWMXBAR_PWMXBAR4_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2364. PWMXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar4 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.46 CONTROLSS_PWMXBAR_PWMXBAR4_G4 Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2365. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1210h

Figure 3-1155. CONTROLSS_PWMXBAR_PWMXBAR4_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2366. PWMXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar4 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.47 CONTROLSS_PWMXBAR_PWMXBAR4_G5 Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2367. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1214h

Figure 3-1156. CONTROLSS_PWMXBAR_PWMXBAR4_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2368. PWMXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar4 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.48 CONTROLSS_PWMXBAR_PWMXBAR4_G6 Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2369. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1218h

Figure 3-1157. CONTROLSS_PWMXBAR_PWMXBAR4_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2370. PWMXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar4 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.49 CONTROLSS_PWMXBAR_PWMXBAR4_G7 Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2371. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 121Ch

Figure 3-1158. CONTROLSS_PWMXBAR_PWMXBAR4_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2372. PWMXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar4 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.50 CONTROLSS_PWMXBAR_PWMXBAR4_G8 Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2373. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1220h

Figure 3-1159. CONTROLSS_PWMXBAR_PWMXBAR4_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2374. PWMXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar4 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.51 CONTROLSS_PWMXBAR_PWMXBAR5_G0 Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2375. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1240h

Figure 3-1160. CONTROLSS_PWMXBAR_PWMXBAR5_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2376. PWMXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar5 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.52 CONTROLSS_PWMXBAR_PWMXBAR5_G1 Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2377. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1244h

Figure 3-1161. CONTROLSS_PWMXBAR_PWMXBAR5_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2378. PWMXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar5 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.53 CONTROLSS_PWMXBAR_PWMXBAR5_G2 Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2379. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1248h

Figure 3-1162. CONTROLSS_PWMXBAR_PWMXBAR5_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2380. PWMXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar5 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.54 CONTROLSS_PWMXBAR_PWMXBAR5_G3 Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2381. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 124Ch

Figure 3-1163. CONTROLSS_PWMXBAR_PWMXBAR5_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2382. PWMXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar5 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.55 CONTROLSS_PWMXBAR_PWMXBAR5_G4 Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2383. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1250h

Figure 3-1164. CONTROLSS_PWMXBAR_PWMXBAR5_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2384. PWMXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar5 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.56 CONTROLSS_PWMXBAR_PWMXBAR5_G5 Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2385. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1254h

Figure 3-1165. CONTROLSS_PWMXBAR_PWMXBAR5_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2386. PWMXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar5 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.57 CONTROLSS_PWMXBAR_PWMXBAR5_G6 Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2387. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1258h

Figure 3-1166. CONTROLSS_PWMXBAR_PWMXBAR5_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2388. PWMXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar5 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.58 CONTROLSS_PWMXBAR_PWMXBAR5_G7 Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2389. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 125Ch

Figure 3-1167. CONTROLSS_PWMXBAR_PWMXBAR5_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2390. PWMXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar5 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.59 CONTROLSS_PWMXBAR_PWMXBAR5_G8 Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2391. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1260h

Figure 3-1168. CONTROLSS_PWMXBAR_PWMXBAR5_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2392. PWMXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar5 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.60 CONTROLSS_PWMXBAR_PWMXBAR6_G0 Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2393. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1280h

Figure 3-1169. CONTROLSS_PWMXBAR_PWMXBAR6_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2394. PWMXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar6 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.61 CONTROLSS_PWMXBAR_PWMXBAR6_G1 Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2395. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1284h

Figure 3-1170. CONTROLSS_PWMXBAR_PWMXBAR6_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2396. PWMXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar6 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.62 CONTROLSS_PWMXBAR_PWMXBAR6_G2 Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2397. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1288h

Figure 3-1171. CONTROLSS_PWMXBAR_PWMXBAR6_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2398. PWMXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar6 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.63 CONTROLSS_PWMXBAR_PWMXBAR6_G3 Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2399. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 128Ch

Figure 3-1172. CONTROLSS_PWMXBAR_PWMXBAR6_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2400. PWMXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar6 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.64 CONTROLSS_PWMXBAR_PWMXBAR6_G4 Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2401. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1290h

Figure 3-1173. CONTROLSS_PWMXBAR_PWMXBAR6_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2402. PWMXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar6 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.65 CONTROLSS_PWMXBAR_PWMXBAR6_G5 Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2403. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1294h

Figure 3-1174. CONTROLSS_PWMXBAR_PWMXBAR6_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2404. PWMXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar6 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.66 CONTROLSS_PWMXBAR_PWMXBAR6_G6 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2405. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1298h

Figure 3-1175. CONTROLSS_PWMXBAR_PWMXBAR6_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2406. PWMXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar6 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.67 CONTROLSS_PWMXBAR_PWMXBAR6_G7 Register (Offset = 29Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2407. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 129Ch

Figure 3-1176. CONTROLSS_PWMXBAR_PWMXBAR6_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2408. PWMXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar6 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.68 CONTROLSS_PWMXBAR_PWMXBAR6_G8 Register (Offset = 2A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2409. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12A0h

Figure 3-1177. CONTROLSS_PWMXBAR_PWMXBAR6_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2410. PWMXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar6 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.69 CONTROLSS_PWMXBAR_PWMXBAR7_G0 Register (Offset = 2C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2411. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C0h

Figure 3-1178. CONTROLSS_PWMXBAR_PWMXBAR7_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2412. PWMXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar7 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.70 CONTROLSS_PWMXBAR_PWMXBAR7_G1 Register (Offset = 2C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2413. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C4h

Figure 3-1179. CONTROLSS_PWMXBAR_PWMXBAR7_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2414. PWMXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar7 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.71 CONTROLSS_PWMXBAR_PWMXBAR7_G2 Register (Offset = 2C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2415. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C8h

Figure 3-1180. CONTROLSS_PWMXBAR_PWMXBAR7_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2416. PWMXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar7 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.72 CONTROLSS_PWMXBAR_PWMXBAR7_G3 Register (Offset = 2CCh) [reset = h]

Short Description: RW

Long Description:

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Table 3-2417. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12CCh

Figure 3-1181. CONTROLSS_PWMXBAR_PWMXBAR7_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2418. PWMXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar7 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.73 CONTROLSS_PWMXBAR_PWMXBAR7_G4 Register (Offset = 2D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2419. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D0h

Figure 3-1182. CONTROLSS_PWMXBAR_PWMXBAR7_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2420. PWMXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar7 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.74 CONTROLSS_PWMXBAR_PWMXBAR7_G5 Register (Offset = 2D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2421. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D4h

Figure 3-1183. CONTROLSS_PWMXBAR_PWMXBAR7_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2422. PWMXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar7 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.75 CONTROLSS_PWMXBAR_PWMXBAR7_G6 Register (Offset = 2D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2423. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D8h

Figure 3-1184. CONTROLSS_PWMXBAR_PWMXBAR7_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2424. PWMXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar7 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.76 CONTROLSS_PWMXBAR_PWMXBAR7_G7 Register (Offset = 2DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2425. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12DCh

Figure 3-1185. CONTROLSS_PWMXBAR_PWMXBAR7_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2426. PWMXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar7 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.77 CONTROLSS_PWMXBAR_PWMXBAR7_G8 Register (Offset = 2E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2427. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12E0h

Figure 3-1186. CONTROLSS_PWMXBAR_PWMXBAR7_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2428. PWMXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar7 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.78 CONTROLSS_PWMXBAR_PWMXBAR8_G0 Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2429. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1300h

Figure 3-1187. CONTROLSS_PWMXBAR_PWMXBAR8_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2430. PWMXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar8 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.79 CONTROLSS_PWMXBAR_PWMXBAR8_G1 Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2431. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1304h

Figure 3-1188. CONTROLSS_PWMXBAR_PWMXBAR8_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2432. PWMXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar8 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.80 CONTROLSS_PWMXBAR_PWMXBAR8_G2 Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2433. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1308h

Figure 3-1189. CONTROLSS_PWMXBAR_PWMXBAR8_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2434. PWMXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar8 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.81 CONTROLSS_PWMXBAR_PWMXBAR8_G3 Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2435. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 130Ch

Figure 3-1190. CONTROLSS_PWMXBAR_PWMXBAR8_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2436. PWMXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar8 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.82 CONTROLSS_PWMXBAR_PWMXBAR8_G4 Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2437. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1310h

Figure 3-1191. CONTROLSS_PWMXBAR_PWMXBAR8_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2438. PWMXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar8 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.83 CONTROLSS_PWMXBAR_PWMXBAR8_G5 Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2439. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1314h

Figure 3-1192. CONTROLSS_PWMXBAR_PWMXBAR8_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2440. PWMXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar8 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.84 CONTROLSS_PWMXBAR_PWMXBAR8_G6 Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2441. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1318h

Figure 3-1193. CONTROLSS_PWMXBAR_PWMXBAR8_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2442. PWMXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar8 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.85 CONTROLSS_PWMXBAR_PWMXBAR8_G7 Register (Offset = 31Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2443. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 131Ch

Figure 3-1194. CONTROLSS_PWMXBAR_PWMXBAR8_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2444. PWMXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar8 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.86 CONTROLSS_PWMXBAR_PWMXBAR8_G8 Register (Offset = 320h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2445. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1320h

Figure 3-1195. CONTROLSS_PWMXBAR_PWMXBAR8_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2446. PWMXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar8 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.87 CONTROLSS_PWMXBAR_PWMXBAR9_G0 Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2447. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1340h

Figure 3-1196. CONTROLSS_PWMXBAR_PWMXBAR9_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2448. PWMXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar9 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.88 CONTROLSS_PWMXBAR_PWMXBAR9_G1 Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2449. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1344h

Figure 3-1197. CONTROLSS_PWMXBAR_PWMXBAR9_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2450. PWMXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar9 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.89 CONTROLSS_PWMXBAR_PWMXBAR9_G2 Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2451. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1348h

Figure 3-1198. CONTROLSS_PWMXBAR_PWMXBAR9_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2452. PWMXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar9 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.90 CONTROLSS_PWMXBAR_PWMXBAR9_G3 Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2453. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 134Ch

Figure 3-1199. CONTROLSS_PWMXBAR_PWMXBAR9_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2454. PWMXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar9 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.91 CONTROLSS_PWMXBAR_PWMXBAR9_G4 Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2455. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1350h

Figure 3-1200. CONTROLSS_PWMXBAR_PWMXBAR9_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2456. PWMXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar9 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.92 CONTROLSS_PWMXBAR_PWMXBAR9_G5 Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2457. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1354h

Figure 3-1201. CONTROLSS_PWMXBAR_PWMXBAR9_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2458. PWMXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar9 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.93 CONTROLSS_PWMXBAR_PWMXBAR9_G6 Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2459. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1358h

Figure 3-1202. CONTROLSS_PWMXBAR_PWMXBAR9_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2460. PWMXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar9 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.94 CONTROLSS_PWMXBAR_PWMXBAR9_G7 Register (Offset = 35Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2461. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 135Ch

Figure 3-1203. CONTROLSS_PWMXBAR_PWMXBAR9_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2462. PWMXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar9 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.95 CONTROLSS_PWMXBAR_PWMXBAR9_G8 Register (Offset = 360h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2463. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1360h

Figure 3-1204. CONTROLSS_PWMXBAR_PWMXBAR9_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2464. PWMXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar9 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.96 CONTROLSS_PWMXBAR_PWMXBAR10_G0 Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2465. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1380h

Figure 3-1205. CONTROLSS_PWMXBAR_PWMXBAR10_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2466. PWMXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar10 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.97 CONTROLSS_PWMXBAR_PWMXBAR10_G1 Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2467. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1384h

Figure 3-1206. CONTROLSS_PWMXBAR_PWMXBAR10_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2468. PWMXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar10 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.98 CONTROLSS_PWMXBAR_PWMXBAR10_G2 Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2469. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1388h

Figure 3-1207. CONTROLSS_PWMXBAR_PWMXBAR10_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2470. PWMXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar10 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.99 CONTROLSS_PWMXBAR_PWMXBAR10_G3 Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2471. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 138Ch

Figure 3-1208. CONTROLSS_PWMXBAR_PWMXBAR10_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2472. PWMXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar10 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.100 CONTROLSS_PWMXBAR_PWMXBAR10_G4 Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2473. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1390h

Figure 3-1209. CONTROLSS_PWMXBAR_PWMXBAR10_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2474. PWMXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar10 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.101 CONTROLSS_PWMXBAR_PWMXBAR10_G5 Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2475. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1394h

Figure 3-1210. CONTROLSS_PWMXBAR_PWMXBAR10_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2476. PWMXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar10 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.102 CONTROLSS_PWMXBAR_PWMXBAR10_G6 Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2477. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1398h

Figure 3-1211. CONTROLSS_PWMXBAR_PWMXBAR10_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2478. PWMXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar10 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.103 CONTROLSS_PWMXBAR_PWMXBAR10_G7 Register (Offset = 39Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2479. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 139Ch

Figure 3-1212. CONTROLSS_PWMXBAR_PWMXBAR10_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2480. PWMXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar10 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.104 CONTROLSS_PWMXBAR_PWMXBAR10_G8 Register (Offset = 3A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2481. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13A0h

Figure 3-1213. CONTROLSS_PWMXBAR_PWMXBAR10_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2482. PWMXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar10 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.105 CONTROLSS_PWMXBAR_PWMXBAR11_G0 Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2483. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C0h

Figure 3-1214. CONTROLSS_PWMXBAR_PWMXBAR11_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2484. PWMXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar11 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.106 CONTROLSS_PWMXBAR_PWMXBAR11_G1 Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2485. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C4h

Figure 3-1215. CONTROLSS_PWMXBAR_PWMXBAR11_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2486. PWMXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar11 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.107 CONTROLSS_PWMXBAR_PWMXBAR11_G2 Register (Offset = 3C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2487. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C8h

Figure 3-1216. CONTROLSS_PWMXBAR_PWMXBAR11_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2488. PWMXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar11 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.108 CONTROLSS_PWMXBAR_PWMXBAR11_G3 Register (Offset = 3CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2489. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13CCh

Figure 3-1217. CONTROLSS_PWMXBAR_PWMXBAR11_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2490. PWMXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar11 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.109 CONTROLSS_PWMXBAR_PWMXBAR11_G4 Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2491. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D0h

Figure 3-1218. CONTROLSS_PWMXBAR_PWMXBAR11_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2492. PWMXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar11 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.110 CONTROLSS_PWMXBAR_PWMXBAR11_G5 Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2493. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D4h

Figure 3-1219. CONTROLSS_PWMXBAR_PWMXBAR11_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2494. PWMXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar11 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.111 CONTROLSS_PWMXBAR_PWMXBAR11_G6 Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2495. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D8h

Figure 3-1220. CONTROLSS_PWMXBAR_PWMXBAR11_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2496. PWMXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar11 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.112 CONTROLSS_PWMXBAR_PWMXBAR11_G7 Register (Offset = 3DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2497. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13DCh

Figure 3-1221. CONTROLSS_PWMXBAR_PWMXBAR11_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2498. PWMXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar11 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.113 CONTROLSS_PWMXBAR_PWMXBAR11_G8 Register (Offset = 3E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2499. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13E0h

Figure 3-1222. CONTROLSS_PWMXBAR_PWMXBAR11_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2500. PWMXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar11 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.114 CONTROLSS_PWMXBAR_PWMXBAR12_G0 Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2501. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1400h

Figure 3-1223. CONTROLSS_PWMXBAR_PWMXBAR12_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2502. PWMXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar12 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.115 CONTROLSS_PWMXBAR_PWMXBAR12_G1 Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2503. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1404h

Figure 3-1224. CONTROLSS_PWMXBAR_PWMXBAR12_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2504. PWMXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar12 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.116 CONTROLSS_PWMXBAR_PWMXBAR12_G2 Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2505. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1408h

Figure 3-1225. CONTROLSS_PWMXBAR_PWMXBAR12_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2506. PWMXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar12 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.117 CONTROLSS_PWMXBAR_PWMXBAR12_G3 Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2507. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 140Ch

Figure 3-1226. CONTROLSS_PWMXBAR_PWMXBAR12_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2508. PWMXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar12 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.118 CONTROLSS_PWMXBAR_PWMXBAR12_G4 Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2509. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1410h

Figure 3-1227. CONTROLSS_PWMXBAR_PWMXBAR12_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2510. PWMXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar12 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.119 CONTROLSS_PWMXBAR_PWMXBAR12_G5 Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2511. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1414h

Figure 3-1228. CONTROLSS_PWMXBAR_PWMXBAR12_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2512. PWMXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar12 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.120 CONTROLSS_PWMXBAR_PWMXBAR12_G6 Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2513. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1418h

Figure 3-1229. CONTROLSS_PWMXBAR_PWMXBAR12_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2514. PWMXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar12 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.121 CONTROLSS_PWMXBAR_PWMXBAR12_G7 Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2515. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 141Ch

Figure 3-1230. CONTROLSS_PWMXBAR_PWMXBAR12_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2516. PWMXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar12 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.122 CONTROLSS_PWMXBAR_PWMXBAR12_G8 Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2517. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1420h

Figure 3-1231. CONTROLSS_PWMXBAR_PWMXBAR12_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2518. PWMXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar12 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.123 CONTROLSS_PWMXBAR_PWMXBAR13_G0 Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2519. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1440h

Figure 3-1232. CONTROLSS_PWMXBAR_PWMXBAR13_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2520. PWMXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar13 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.124 CONTROLSS_PWMXBAR_PWMXBAR13_G1 Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2521. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1444h

Figure 3-1233. CONTROLSS_PWMXBAR_PWMXBAR13_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2522. PWMXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar13 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.125 CONTROLSS_PWMXBAR_PWMXBAR13_G2 Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2523. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1448h

Figure 3-1234. CONTROLSS_PWMXBAR_PWMXBAR13_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2524. PWMXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar13 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.126 CONTROLSS_PWMXBAR_PWMXBAR13_G3 Register (Offset = 44Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2525. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 144Ch

Figure 3-1235. CONTROLSS_PWMXBAR_PWMXBAR13_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2526. PWMXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar13 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.127 CONTROLSS_PWMXBAR_PWMXBAR13_G4 Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2527. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1450h

Figure 3-1236. CONTROLSS_PWMXBAR_PWMXBAR13_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2528. PWMXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar13 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.128 CONTROLSS_PWMXBAR_PWMXBAR13_G5 Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2529. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1454h

Figure 3-1237. CONTROLSS_PWMXBAR_PWMXBAR13_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2530. PWMXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar13 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.129 CONTROLSS_PWMXBAR_PWMXBAR13_G6 Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2531. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1458h

Figure 3-1238. CONTROLSS_PWMXBAR_PWMXBAR13_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2532. PWMXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar13 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.130 CONTROLSS_PWMXBAR_PWMXBAR13_G7 Register (Offset = 45Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2533. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 145Ch

Figure 3-1239. CONTROLSS_PWMXBAR_PWMXBAR13_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2534. PWMXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar13 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.131 CONTROLSS_PWMXBAR_PWMXBAR13_G8 Register (Offset = 460h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2535. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1460h

Figure 3-1240. CONTROLSS_PWMXBAR_PWMXBAR13_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2536. PWMXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar13 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.132 CONTROLSS_PWMXBAR_PWMXBAR14_G0 Register (Offset = 480h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2537. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1480h

Figure 3-1241. CONTROLSS_PWMXBAR_PWMXBAR14_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2538. PWMXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar14 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.133 CONTROLSS_PWMXBAR_PWMXBAR14_G1 Register (Offset = 484h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2539. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1484h

Figure 3-1242. CONTROLSS_PWMXBAR_PWMXBAR14_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2540. PWMXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar14 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.134 CONTROLSS_PWMXBAR_PWMXBAR14_G2 Register (Offset = 488h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2541. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1488h

Figure 3-1243. CONTROLSS_PWMXBAR_PWMXBAR14_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2542. PWMXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar14 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.135 CONTROLSS_PWMXBAR_PWMXBAR14_G3 Register (Offset = 48Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2543. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 148Ch

Figure 3-1244. CONTROLSS_PWMXBAR_PWMXBAR14_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2544. PWMXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar14 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.136 CONTROLSS_PWMXBAR_PWMXBAR14_G4 Register (Offset = 490h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2545. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1490h

Figure 3-1245. CONTROLSS_PWMXBAR_PWMXBAR14_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2546. PWMXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar14 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.137 CONTROLSS_PWMXBAR_PWMXBAR14_G5 Register (Offset = 494h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2547. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1494h

Figure 3-1246. CONTROLSS_PWMXBAR_PWMXBAR14_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2548. PWMXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar14 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.138 CONTROLSS_PWMXBAR_PWMXBAR14_G6 Register (Offset = 498h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2549. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1498h

Figure 3-1247. CONTROLSS_PWMXBAR_PWMXBAR14_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2550. PWMXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar14 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.139 CONTROLSS_PWMXBAR_PWMXBAR14_G7 Register (Offset = 49Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2551. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 149Ch

Figure 3-1248. CONTROLSS_PWMXBAR_PWMXBAR14_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2552. PWMXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar14 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.140 CONTROLSS_PWMXBAR_PWMXBAR14_G8 Register (Offset = 4A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2553. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14A0h

Figure 3-1249. CONTROLSS_PWMXBAR_PWMXBAR14_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2554. PWMXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar14 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.141 CONTROLSS_PWMXBAR_PWMXBAR15_G0 Register (Offset = 4C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2555. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C0h

Figure 3-1250. CONTROLSS_PWMXBAR_PWMXBAR15_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2556. PWMXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar15 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.142 CONTROLSS_PWMXBAR_PWMXBAR15_G1 Register (Offset = 4C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2557. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C4h

Figure 3-1251. CONTROLSS_PWMXBAR_PWMXBAR15_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2558. PWMXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar15 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.143 CONTROLSS_PWMXBAR_PWMXBAR15_G2 Register (Offset = 4C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2559. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C8h

Figure 3-1252. CONTROLSS_PWMXBAR_PWMXBAR15_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2560. PWMXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar15 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.144 CONTROLSS_PWMXBAR_PWMXBAR15_G3 Register (Offset = 4CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2561. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14CCh

Figure 3-1253. CONTROLSS_PWMXBAR_PWMXBAR15_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2562. PWMXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar15 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.145 CONTROLSS_PWMXBAR_PWMXBAR15_G4 Register (Offset = 4D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2563. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D0h

Figure 3-1254. CONTROLSS_PWMXBAR_PWMXBAR15_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2564. PWMXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar15 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.146 CONTROLSS_PWMXBAR_PWMXBAR15_G5 Register (Offset = 4D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2565. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D4h

Figure 3-1255. CONTROLSS_PWMXBAR_PWMXBAR15_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2566. PWMXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar15 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.147 CONTROLSS_PWMXBAR_PWMXBAR15_G6 Register (Offset = 4D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2567. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D8h

Figure 3-1256. CONTROLSS_PWMXBAR_PWMXBAR15_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2568. PWMXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar15 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.148 CONTROLSS_PWMXBAR_PWMXBAR15_G7 Register (Offset = 4DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2569. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14DCh

Figure 3-1257. CONTROLSS_PWMXBAR_PWMXBAR15_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2570. PWMXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar15 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.149 CONTROLSS_PWMXBAR_PWMXBAR15_G8 Register (Offset = 4E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2571. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14E0h

Figure 3-1258. CONTROLSS_PWMXBAR_PWMXBAR15_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2572. PWMXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar15 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.150 CONTROLSS_PWMXBAR_PWMXBAR16_G0 Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2573. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1500h

Figure 3-1259. CONTROLSS_PWMXBAR_PWMXBAR16_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2574. PWMXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar16 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.151 CONTROLSS_PWMXBAR_PWMXBAR16_G1 Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2575. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1504h

Figure 3-1260. CONTROLSS_PWMXBAR_PWMXBAR16_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2576. PWMXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar16 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.152 CONTROLSS_PWMXBAR_PWMXBAR16_G2 Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2577. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1508h

Figure 3-1261. CONTROLSS_PWMXBAR_PWMXBAR16_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2578. PWMXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar16 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.153 CONTROLSS_PWMXBAR_PWMXBAR16_G3 Register (Offset = 50Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2579. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 150Ch

Figure 3-1262. CONTROLSS_PWMXBAR_PWMXBAR16_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2580. PWMXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar16 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.154 CONTROLSS_PWMXBAR_PWMXBAR16_G4 Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2581. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1510h

Figure 3-1263. CONTROLSS_PWMXBAR_PWMXBAR16_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2582. PWMXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar16 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.155 CONTROLSS_PWMXBAR_PWMXBAR16_G5 Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2583. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1514h

Figure 3-1264. CONTROLSS_PWMXBAR_PWMXBAR16_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2584. PWMXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar16 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.156 CONTROLSS_PWMXBAR_PWMXBAR16_G6 Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2585. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1518h

Figure 3-1265. CONTROLSS_PWMXBAR_PWMXBAR16_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2586. PWMXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar16 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.157 CONTROLSS_PWMXBAR_PWMXBAR16_G7 Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2587. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 151Ch

Figure 3-1266. CONTROLSS_PWMXBAR_PWMXBAR16_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2588. PWMXBAR16_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar16 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.158 CONTROLSS_PWMXBAR_PWMXBAR16_G8 Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2589. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1520h

Figure 3-1267. CONTROLSS_PWMXBAR_PWMXBAR16_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2590. PWMXBAR16_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar16 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.159 CONTROLSS_PWMXBAR_PWMXBAR17_G0 Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2591. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1540h

Figure 3-1268. CONTROLSS_PWMXBAR_PWMXBAR17_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2592. PWMXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar17 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.160 CONTROLSS_PWMXBAR_PWMXBAR17_G1 Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2593. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1544h

Figure 3-1269. CONTROLSS_PWMXBAR_PWMXBAR17_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2594. PWMXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar17 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.161 CONTROLSS_PWMXBAR_PWMXBAR17_G2 Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2595. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1548h

Figure 3-1270. CONTROLSS_PWMXBAR_PWMXBAR17_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2596. PWMXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar17 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.162 CONTROLSS_PWMXBAR_PWMXBAR17_G3 Register (Offset = 54Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2597. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 154Ch

Figure 3-1271. CONTROLSS_PWMXBAR_PWMXBAR17_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2598. PWMXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar17 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.163 CONTROLSS_PWMXBAR_PWMXBAR17_G4 Register (Offset = 550h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2599. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1550h

Figure 3-1272. CONTROLSS_PWMXBAR_PWMXBAR17_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2600. PWMXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar17 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.164 CONTROLSS_PWMXBAR_PWMXBAR17_G5 Register (Offset = 554h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2601. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1554h

Figure 3-1273. CONTROLSS_PWMXBAR_PWMXBAR17_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2602. PWMXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar17 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.165 CONTROLSS_PWMXBAR_PWMXBAR17_G6 Register (Offset = 558h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2603. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1558h

Figure 3-1274. CONTROLSS_PWMXBAR_PWMXBAR17_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2604. PWMXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar17 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.166 CONTROLSS_PWMXBAR_PWMXBAR17_G7 Register (Offset = 55Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2605. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 155Ch

Figure 3-1275. CONTROLSS_PWMXBAR_PWMXBAR17_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2606. PWMXBAR17_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar17 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.167 CONTROLSS_PWMXBAR_PWMXBAR17_G8 Register (Offset = 560h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2607. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1560h

Figure 3-1276. CONTROLSS_PWMXBAR_PWMXBAR17_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2608. PWMXBAR17_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar17 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.168 CONTROLSS_PWMXBAR_PWMXBAR18_G0 Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2609. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1580h

Figure 3-1277. CONTROLSS_PWMXBAR_PWMXBAR18_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2610. PWMXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar18 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.169 CONTROLSS_PWMXBAR_PWMXBAR18_G1 Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2611. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1584h

Figure 3-1278. CONTROLSS_PWMXBAR_PWMXBAR18_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2612. PWMXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar18 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.170 CONTROLSS_PWMXBAR_PWMXBAR18_G2 Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2613. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1588h

Figure 3-1279. CONTROLSS_PWMXBAR_PWMXBAR18_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2614. PWMXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar18 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.171 CONTROLSS_PWMXBAR_PWMXBAR18_G3 Register (Offset = 58Ch) [reset = h]

Short Description: RW

Long Description:

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Table 3-2615. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 158Ch

Figure 3-1280. CONTROLSS_PWMXBAR_PWMXBAR18_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2616. PWMXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar18 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.172 CONTROLSS_PWMXBAR_PWMXBAR18_G4 Register (Offset = 590h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2617. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1590h

Figure 3-1281. CONTROLSS_PWMXBAR_PWMXBAR18_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2618. PWMXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar18 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.173 CONTROLSS_PWMXBAR_PWMXBAR18_G5 Register (Offset = 594h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2619. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1594h

Figure 3-1282. CONTROLSS_PWMXBAR_PWMXBAR18_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2620. PWMXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar18 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.174 CONTROLSS_PWMXBAR_PWMXBAR18_G6 Register (Offset = 598h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2621. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1598h

Figure 3-1283. CONTROLSS_PWMXBAR_PWMXBAR18_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2622. PWMXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar18 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.175 CONTROLSS_PWMXBAR_PWMXBAR18_G7 Register (Offset = 59Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2623. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 159Ch

Figure 3-1284. CONTROLSS_PWMXBAR_PWMXBAR18_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2624. PWMXBAR18_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar18 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.176 CONTROLSS_PWMXBAR_PWMXBAR18_G8 Register (Offset = 5A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2625. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15A0h

Figure 3-1285. CONTROLSS_PWMXBAR_PWMXBAR18_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2626. PWMXBAR18_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar18 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.177 CONTROLSS_PWMXBAR_PWMXBAR19_G0 Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2627. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C0h

Figure 3-1286. CONTROLSS_PWMXBAR_PWMXBAR19_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2628. PWMXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar19 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.178 CONTROLSS_PWMXBAR_PWMXBAR19_G1 Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2629. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C4h

Figure 3-1287. CONTROLSS_PWMXBAR_PWMXBAR19_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2630. PWMXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar19 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.179 CONTROLSS_PWMXBAR_PWMXBAR19_G2 Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2631. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C8h

Figure 3-1288. CONTROLSS_PWMXBAR_PWMXBAR19_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2632. PWMXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar19 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.180 CONTROLSS_PWMXBAR_PWMXBAR19_G3 Register (Offset = 5CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2633. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15CCh

Figure 3-1289. CONTROLSS_PWMXBAR_PWMXBAR19_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2634. PWMXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar19 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.181 CONTROLSS_PWMXBAR_PWMXBAR19_G4 Register (Offset = 5D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2635. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D0h

Figure 3-1290. CONTROLSS_PWMXBAR_PWMXBAR19_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2636. PWMXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar19 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.182 CONTROLSS_PWMXBAR_PWMXBAR19_G5 Register (Offset = 5D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2637. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D4h

Figure 3-1291. CONTROLSS_PWMXBAR_PWMXBAR19_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2638. PWMXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar19 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.183 CONTROLSS_PWMXBAR_PWMXBAR19_G6 Register (Offset = 5D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2639. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D8h

Figure 3-1292. CONTROLSS_PWMXBAR_PWMXBAR19_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2640. PWMXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar19 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.184 CONTROLSS_PWMXBAR_PWMXBAR19_G7 Register (Offset = 5DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2641. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15DCh

Figure 3-1293. CONTROLSS_PWMXBAR_PWMXBAR19_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2642. PWMXBAR19_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar19 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.185 CONTROLSS_PWMXBAR_PWMXBAR19_G8 Register (Offset = 5E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2643. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15E0h

Figure 3-1294. CONTROLSS_PWMXBAR_PWMXBAR19_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2644. PWMXBAR19_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar19 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.186 CONTROLSS_PWMXBAR_PWMXBAR20_G0 Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2645. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1600h

Figure 3-1295. CONTROLSS_PWMXBAR_PWMXBAR20_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2646. PWMXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar20 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.187 CONTROLSS_PWMXBAR_PWMXBAR20_G1 Register (Offset = 604h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2647. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1604h

Figure 3-1296. CONTROLSS_PWMXBAR_PWMXBAR20_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2648. PWMXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar20 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.188 CONTROLSS_PWMXBAR_PWMXBAR20_G2 Register (Offset = 608h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2649. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1608h

Figure 3-1297. CONTROLSS_PWMXBAR_PWMXBAR20_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2650. PWMXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar20 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.189 CONTROLSS_PWMXBAR_PWMXBAR20_G3 Register (Offset = 60Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2651. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 160Ch

Figure 3-1298. CONTROLSS_PWMXBAR_PWMXBAR20_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2652. PWMXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar20 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.190 CONTROLSS_PWMXBAR_PWMXBAR20_G4 Register (Offset = 610h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2653. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1610h

Figure 3-1299. CONTROLSS_PWMXBAR_PWMXBAR20_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2654. PWMXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar20 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.191 CONTROLSS_PWMXBAR_PWMXBAR20_G5 Register (Offset = 614h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2655. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1614h

Figure 3-1300. CONTROLSS_PWMXBAR_PWMXBAR20_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2656. PWMXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar20 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.192 CONTROLSS_PWMXBAR_PWMXBAR20_G6 Register (Offset = 618h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2657. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1618h

Figure 3-1301. CONTROLSS_PWMXBAR_PWMXBAR20_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2658. PWMXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar20 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.193 CONTROLSS_PWMXBAR_PWMXBAR20_G7 Register (Offset = 61Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2659. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 161Ch

Figure 3-1302. CONTROLSS_PWMXBAR_PWMXBAR20_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2660. PWMXBAR20_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar20 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.194 CONTROLSS_PWMXBAR_PWMXBAR20_G8 Register (Offset = 620h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2661. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1620h

Figure 3-1303. CONTROLSS_PWMXBAR_PWMXBAR20_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2662. PWMXBAR20_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar20 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.195 CONTROLSS_PWMXBAR_PWMXBAR21_G0 Register (Offset = 640h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2663. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1640h

Figure 3-1304. CONTROLSS_PWMXBAR_PWMXBAR21_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2664. PWMXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar21 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.196 CONTROLSS_PWMXBAR_PWMXBAR21_G1 Register (Offset = 644h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2665. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1644h

Figure 3-1305. CONTROLSS_PWMXBAR_PWMXBAR21_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2666. PWMXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar21 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.197 CONTROLSS_PWMXBAR_PWMXBAR21_G2 Register (Offset = 648h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2667. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1648h

Figure 3-1306. CONTROLSS_PWMXBAR_PWMXBAR21_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2668. PWMXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar21 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.198 CONTROLSS_PWMXBAR_PWMXBAR21_G3 Register (Offset = 64Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2669. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 164Ch

Figure 3-1307. CONTROLSS_PWMXBAR_PWMXBAR21_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2670. PWMXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar21 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.199 CONTROLSS_PWMXBAR_PWMXBAR21_G4 Register (Offset = 650h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2671. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1650h

Figure 3-1308. CONTROLSS_PWMXBAR_PWMXBAR21_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2672. PWMXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar21 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.200 CONTROLSS_PWMXBAR_PWMXBAR21_G5 Register (Offset = 654h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2673. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1654h

Figure 3-1309. CONTROLSS_PWMXBAR_PWMXBAR21_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2674. PWMXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar21 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.201 CONTROLSS_PWMXBAR_PWMXBAR21_G6 Register (Offset = 658h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2675. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1658h

Figure 3-1310. CONTROLSS_PWMXBAR_PWMXBAR21_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2676. PWMXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar21 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.202 CONTROLSS_PWMXBAR_PWMXBAR21_G7 Register (Offset = 65Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2677. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 165Ch

Figure 3-1311. CONTROLSS_PWMXBAR_PWMXBAR21_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2678. PWMXBAR21_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar21 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.203 CONTROLSS_PWMXBAR_PWMXBAR21_G8 Register (Offset = 660h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2679. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1660h

Figure 3-1312. CONTROLSS_PWMXBAR_PWMXBAR21_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2680. PWMXBAR21_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar21 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.204 CONTROLSS_PWMXBAR_PWMXBAR22_G0 Register (Offset = 680h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2681. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1680h

Figure 3-1313. CONTROLSS_PWMXBAR_PWMXBAR22_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2682. PWMXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar22 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.205 CONTROLSS_PWMXBAR_PWMXBAR22_G1 Register (Offset = 684h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2683. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1684h

Figure 3-1314. CONTROLSS_PWMXBAR_PWMXBAR22_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2684. PWMXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar22 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.206 CONTROLSS_PWMXBAR_PWMXBAR22_G2 Register (Offset = 688h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2685. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1688h

Figure 3-1315. CONTROLSS_PWMXBAR_PWMXBAR22_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2686. PWMXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar22 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.207 CONTROLSS_PWMXBAR_PWMXBAR22_G3 Register (Offset = 68Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2687. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 168Ch

Figure 3-1316. CONTROLSS_PWMXBAR_PWMXBAR22_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2688. PWMXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar22 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.208 CONTROLSS_PWMXBAR_PWMXBAR22_G4 Register (Offset = 690h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2689. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1690h

Figure 3-1317. CONTROLSS_PWMXBAR_PWMXBAR22_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2690. PWMXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar22 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.209 CONTROLSS_PWMXBAR_PWMXBAR22_G5 Register (Offset = 694h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2691. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1694h

Figure 3-1318. CONTROLSS_PWMXBAR_PWMXBAR22_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2692. PWMXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar22 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.210 CONTROLSS_PWMXBAR_PWMXBAR22_G6 Register (Offset = 698h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2693. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1698h

Figure 3-1319. CONTROLSS_PWMXBAR_PWMXBAR22_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2694. PWMXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar22 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.211 CONTROLSS_PWMXBAR_PWMXBAR22_G7 Register (Offset = 69Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2695. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 169Ch

Figure 3-1320. CONTROLSS_PWMXBAR_PWMXBAR22_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2696. PWMXBAR22_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar22 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.212 CONTROLSS_PWMXBAR_PWMXBAR22_G8 Register (Offset = 6A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2697. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16A0h

Figure 3-1321. CONTROLSS_PWMXBAR_PWMXBAR22_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2698. PWMXBAR22_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar22 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.213 CONTROLSS_PWMXBAR_PWMXBAR23_G0 Register (Offset = 6C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2699. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C0h

Figure 3-1322. CONTROLSS_PWMXBAR_PWMXBAR23_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2700. PWMXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar23 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.214 CONTROLSS_PWMXBAR_PWMXBAR23_G1 Register (Offset = 6C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2701. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C4h

Figure 3-1323. CONTROLSS_PWMXBAR_PWMXBAR23_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2702. PWMXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar23 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.215 CONTROLSS_PWMXBAR_PWMXBAR23_G2 Register (Offset = 6C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2703. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C8h

Figure 3-1324. CONTROLSS_PWMXBAR_PWMXBAR23_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2704. PWMXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar23 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.216 CONTROLSS_PWMXBAR_PWMXBAR23_G3 Register (Offset = 6CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2705. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16CCh

Figure 3-1325. CONTROLSS_PWMXBAR_PWMXBAR23_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2706. PWMXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar23 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.217 CONTROLSS_PWMXBAR_PWMXBAR23_G4 Register (Offset = 6D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2707. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D0h

Figure 3-1326. CONTROLSS_PWMXBAR_PWMXBAR23_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2708. PWMXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar23 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.218 CONTROLSS_PWMXBAR_PWMXBAR23_G5 Register (Offset = 6D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2709. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D4h

Figure 3-1327. CONTROLSS_PWMXBAR_PWMXBAR23_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2710. PWMXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar23 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.219 CONTROLSS_PWMXBAR_PWMXBAR23_G6 Register (Offset = 6D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2711. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D8h

Figure 3-1328. CONTROLSS_PWMXBAR_PWMXBAR23_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2712. PWMXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar23 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.220 CONTROLSS_PWMXBAR_PWMXBAR23_G7 Register (Offset = 6DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2713. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16DCh

Figure 3-1329. CONTROLSS_PWMXBAR_PWMXBAR23_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2714. PWMXBAR23_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar23 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.221 CONTROLSS_PWMXBAR_PWMXBAR23_G8 Register (Offset = 6E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2715. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16E0h

Figure 3-1330. CONTROLSS_PWMXBAR_PWMXBAR23_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2716. PWMXBAR23_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar23 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.222 CONTROLSS_PWMXBAR_PWMXBAR24_G0 Register (Offset = 700h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2717. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1700h

Figure 3-1331. CONTROLSS_PWMXBAR_PWMXBAR24_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2718. PWMXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar24 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.223 CONTROLSS_PWMXBAR_PWMXBAR24_G1 Register (Offset = 704h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2719. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1704h

Figure 3-1332. CONTROLSS_PWMXBAR_PWMXBAR24_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2720. PWMXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar24 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.224 CONTROLSS_PWMXBAR_PWMXBAR24_G2 Register (Offset = 708h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2721. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1708h

Figure 3-1333. CONTROLSS_PWMXBAR_PWMXBAR24_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2722. PWMXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar24 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.225 CONTROLSS_PWMXBAR_PWMXBAR24_G3 Register (Offset = 70Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2723. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 170Ch

Figure 3-1334. CONTROLSS_PWMXBAR_PWMXBAR24_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2724. PWMXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar24 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.226 CONTROLSS_PWMXBAR_PWMXBAR24_G4 Register (Offset = 710h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2725. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1710h

Figure 3-1335. CONTROLSS_PWMXBAR_PWMXBAR24_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2726. PWMXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar24 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.227 CONTROLSS_PWMXBAR_PWMXBAR24_G5 Register (Offset = 714h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2727. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1714h

Figure 3-1336. CONTROLSS_PWMXBAR_PWMXBAR24_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2728. PWMXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar24 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.228 CONTROLSS_PWMXBAR_PWMXBAR24_G6 Register (Offset = 718h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2729. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1718h

Figure 3-1337. CONTROLSS_PWMXBAR_PWMXBAR24_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2730. PWMXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar24 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.229 CONTROLSS_PWMXBAR_PWMXBAR24_G7 Register (Offset = 71Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2731. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 171Ch

Figure 3-1338. CONTROLSS_PWMXBAR_PWMXBAR24_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2732. PWMXBAR24_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar24 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.230 CONTROLSS_PWMXBAR_PWMXBAR24_G8 Register (Offset = 720h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2733. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1720h

Figure 3-1339. CONTROLSS_PWMXBAR_PWMXBAR24_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2734. PWMXBAR24_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar24 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.231 CONTROLSS_PWMXBAR_PWMXBAR25_G0 Register (Offset = 740h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2735. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1740h

Figure 3-1340. CONTROLSS_PWMXBAR_PWMXBAR25_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2736. PWMXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar25 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.232 CONTROLSS_PWMXBAR_PWMXBAR25_G1 Register (Offset = 744h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2737. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1744h

Figure 3-1341. CONTROLSS_PWMXBAR_PWMXBAR25_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2738. PWMXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar25 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.233 CONTROLSS_PWMXBAR_PWMXBAR25_G2 Register (Offset = 748h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2739. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1748h

Figure 3-1342. CONTROLSS_PWMXBAR_PWMXBAR25_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2740. PWMXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar25 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.234 CONTROLSS_PWMXBAR_PWMXBAR25_G3 Register (Offset = 74Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2741. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 174Ch

Figure 3-1343. CONTROLSS_PWMXBAR_PWMXBAR25_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2742. PWMXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar25 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.235 CONTROLSS_PWMXBAR_PWMXBAR25_G4 Register (Offset = 750h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2743. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1750h

Figure 3-1344. CONTROLSS_PWMXBAR_PWMXBAR25_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2744. PWMXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar25 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.236 CONTROLSS_PWMXBAR_PWMXBAR25_G5 Register (Offset = 754h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2745. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1754h

Figure 3-1345. CONTROLSS_PWMXBAR_PWMXBAR25_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2746. PWMXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar25 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.237 CONTROLSS_PWMXBAR_PWMXBAR25_G6 Register (Offset = 758h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2747. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1758h

Figure 3-1346. CONTROLSS_PWMXBAR_PWMXBAR25_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2748. PWMXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar25 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.238 CONTROLSS_PWMXBAR_PWMXBAR25_G7 Register (Offset = 75Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2749. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 175Ch

Figure 3-1347. CONTROLSS_PWMXBAR_PWMXBAR25_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2750. PWMXBAR25_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar25 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.239 CONTROLSS_PWMXBAR_PWMXBAR25_G8 Register (Offset = 760h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2751. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1760h

Figure 3-1348. CONTROLSS_PWMXBAR_PWMXBAR25_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2752. PWMXBAR25_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar25 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.240 CONTROLSS_PWMXBAR_PWMXBAR26_G0 Register (Offset = 780h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2753. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1780h

Figure 3-1349. CONTROLSS_PWMXBAR_PWMXBAR26_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2754. PWMXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar26 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.241 CONTROLSS_PWMXBAR_PWMXBAR26_G1 Register (Offset = 784h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2755. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1784h

Figure 3-1350. CONTROLSS_PWMXBAR_PWMXBAR26_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2756. PWMXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar26 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.242 CONTROLSS_PWMXBAR_PWMXBAR26_G2 Register (Offset = 788h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2757. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1788h

Figure 3-1351. CONTROLSS_PWMXBAR_PWMXBAR26_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2758. PWMXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar26 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.243 CONTROLSS_PWMXBAR_PWMXBAR26_G3 Register (Offset = 78Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2759. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 178Ch

Figure 3-1352. CONTROLSS_PWMXBAR_PWMXBAR26_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2760. PWMXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar26 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.244 CONTROLSS_PWMXBAR_PWMXBAR26_G4 Register (Offset = 790h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2761. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1790h

Figure 3-1353. CONTROLSS_PWMXBAR_PWMXBAR26_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2762. PWMXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar26 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.245 CONTROLSS_PWMXBAR_PWMXBAR26_G5 Register (Offset = 794h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2763. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1794h

Figure 3-1354. CONTROLSS_PWMXBAR_PWMXBAR26_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2764. PWMXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar26 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.246 CONTROLSS_PWMXBAR_PWMXBAR26_G6 Register (Offset = 798h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2765. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1798h

Figure 3-1355. CONTROLSS_PWMXBAR_PWMXBAR26_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2766. PWMXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar26 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.247 CONTROLSS_PWMXBAR_PWMXBAR26_G7 Register (Offset = 79Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2767. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 179Ch

Figure 3-1356. CONTROLSS_PWMXBAR_PWMXBAR26_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2768. PWMXBAR26_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar26 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.248 CONTROLSS_PWMXBAR_PWMXBAR26_G8 Register (Offset = 7A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2769. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17A0h

Figure 3-1357. CONTROLSS_PWMXBAR_PWMXBAR26_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2770. PWMXBAR26_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar26 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.249 CONTROLSS_PWMXBAR_PWMXBAR27_G0 Register (Offset = 7C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2771. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C0h

Figure 3-1358. CONTROLSS_PWMXBAR_PWMXBAR27_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2772. PWMXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar27 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.250 CONTROLSS_PWMXBAR_PWMXBAR27_G1 Register (Offset = 7C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2773. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C4h

Figure 3-1359. CONTROLSS_PWMXBAR_PWMXBAR27_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2774. PWMXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar27 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.251 CONTROLSS_PWMXBAR_PWMXBAR27_G2 Register (Offset = 7C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2775. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C8h

Figure 3-1360. CONTROLSS_PWMXBAR_PWMXBAR27_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2776. PWMXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar27 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.252 CONTROLSS_PWMXBAR_PWMXBAR27_G3 Register (Offset = 7CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2777. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17CCh

Figure 3-1361. CONTROLSS_PWMXBAR_PWMXBAR27_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2778. PWMXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar27 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.253 CONTROLSS_PWMXBAR_PWMXBAR27_G4 Register (Offset = 7D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2779. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D0h

Figure 3-1362. CONTROLSS_PWMXBAR_PWMXBAR27_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2780. PWMXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar27 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.254 CONTROLSS_PWMXBAR_PWMXBAR27_G5 Register (Offset = 7D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2781. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D4h

Figure 3-1363. CONTROLSS_PWMXBAR_PWMXBAR27_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2782. PWMXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar27 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.255 CONTROLSS_PWMXBAR_PWMXBAR27_G6 Register (Offset = 7D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2783. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D8h

Figure 3-1364. CONTROLSS_PWMXBAR_PWMXBAR27_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2784. PWMXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar27 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.256 CONTROLSS_PWMXBAR_PWMXBAR27_G7 Register (Offset = 7DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2785. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17DCh

Figure 3-1365. CONTROLSS_PWMXBAR_PWMXBAR27_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2786. PWMXBAR27_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar27 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.257 CONTROLSS_PWMXBAR_PWMXBAR27_G8 Register (Offset = 7E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2787. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17E0h

Figure 3-1366. CONTROLSS_PWMXBAR_PWMXBAR27_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2788. PWMXBAR27_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar27 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.258 CONTROLSS_PWMXBAR_PWMXBAR28_G0 Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2789. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1800h

Figure 3-1367. CONTROLSS_PWMXBAR_PWMXBAR28_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2790. PWMXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar28 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.259 CONTROLSS_PWMXBAR_PWMXBAR28_G1 Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2791. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1804h

Figure 3-1368. CONTROLSS_PWMXBAR_PWMXBAR28_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2792. PWMXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar28 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.260 CONTROLSS_PWMXBAR_PWMXBAR28_G2 Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2793. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1808h

Figure 3-1369. CONTROLSS_PWMXBAR_PWMXBAR28_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2794. PWMXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar28 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.261 CONTROLSS_PWMXBAR_PWMXBAR28_G3 Register (Offset = 80Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2795. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 180Ch

Figure 3-1370. CONTROLSS_PWMXBAR_PWMXBAR28_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2796. PWMXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar28 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.262 CONTROLSS_PWMXBAR_PWMXBAR28_G4 Register (Offset = 810h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2797. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1810h

Figure 3-1371. CONTROLSS_PWMXBAR_PWMXBAR28_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2798. PWMXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar28 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.263 CONTROLSS_PWMXBAR_PWMXBAR28_G5 Register (Offset = 814h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2799. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1814h

Figure 3-1372. CONTROLSS_PWMXBAR_PWMXBAR28_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2800. PWMXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar28 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.264 CONTROLSS_PWMXBAR_PWMXBAR28_G6 Register (Offset = 818h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2801. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1818h

Figure 3-1373. CONTROLSS_PWMXBAR_PWMXBAR28_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2802. PWMXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar28 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.265 CONTROLSS_PWMXBAR_PWMXBAR28_G7 Register (Offset = 81Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2803. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 181Ch

Figure 3-1374. CONTROLSS_PWMXBAR_PWMXBAR28_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2804. PWMXBAR28_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar28 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.266 CONTROLSS_PWMXBAR_PWMXBAR28_G8 Register (Offset = 820h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2805. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1820h

Figure 3-1375. CONTROLSS_PWMXBAR_PWMXBAR28_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2806. PWMXBAR28_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar28 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

3.18.267 CONTROLSS_PWMXBAR_PWMXBAR29_G0 Register (Offset = 840h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2807. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1840h

Figure 3-1376. CONTROLSS_PWMXBAR_PWMXBAR29_G0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2808. PWMXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar29 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

3.18.268 CONTROLSS_PWMXBAR_PWMXBAR29_G1 Register (Offset = 844h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2809. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1844h

Figure 3-1377. CONTROLSS_PWMXBAR_PWMXBAR29_G1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2810. PWMXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar29 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

3.18.269 CONTROLSS_PWMXBAR_PWMXBAR29_G2 Register (Offset = 848h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2811. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1848h

Figure 3-1378. CONTROLSS_PWMXBAR_PWMXBAR29_G2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2812. PWMXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar29 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

3.18.270 CONTROLSS_PWMXBAR_PWMXBAR29_G3 Register (Offset = 84Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2813. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 184Ch

Figure 3-1379. CONTROLSS_PWMXBAR_PWMXBAR29_G3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SEL											
NONE				RW											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2814. PWMXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar29 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

3.18.271 CONTROLSS_PWMXBAR_PWMXBAR29_G4 Register (Offset = 850h) [reset = h]

Short Description: RW

Long Description:

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Table 3-2815. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1850h

Figure 3-1380. CONTROLSS_PWMXBAR_PWMXBAR29_G4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2816. PWMXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar29 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

3.18.272 CONTROLSS_PWMXBAR_PWMXBAR29_G5 Register (Offset = 854h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2817. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1854h

Figure 3-1381. CONTROLSS_PWMXBAR_PWMXBAR29_G5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2818. PWMXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar29 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

3.18.273 CONTROLSS_PWMXBAR_PWMXBAR29_G6 Register (Offset = 858h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2819. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1858h

Figure 3-1382. CONTROLSS_PWMXBAR_PWMXBAR29_G6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2820. PWMXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar29 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

3.18.274 CONTROLSS_PWMXBAR_PWMXBAR29_G7 Register (Offset = 85Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2821. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 185Ch

Figure 3-1383. CONTROLSS_PWMXBAR_PWMXBAR29_G7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2822. PWMXBAR29_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar29 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

3.18.275 CONTROLSS_PWMXBAR_PWMXBAR29_G8 Register (Offset = 860h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-2823. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1860h

Figure 3-1384. CONTROLSS_PWMXBAR_PWMXBAR29_G8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SEL												
NONE			RW												
0			0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL															
RW															
0															

Access Types Legend

Table 3-2824. PWMXBAR29_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar29 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG4 28:19: ECAP[9:0].TRIPOUT

Table 3-2825. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

3.19 C2K_SDFM Registers

Table 3-2826. CONTROLSS_SDFM0, CONTROLSS_SDFM0_CONTROLSS_SDFM Registers, Base Address=5026 8000H, Length=2

Offset	Length	Acronym	Register Name	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
0h	32	CONTROLSS_SDFM0_SDIFLG	SD Interrupt Flag Register	5026 8000h	5026 9000h
4h	32	CONTROLSS_SDFM0_SDIFLGCLR	SD Module Interrupt Flag Clear Bits: Writing a "1" will clear the respective flag bit in the SDIFLG register. Writes of "0" are ignored. Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.	5026 8004h	5026 9004h
8h	16	CONTROLSS_SDFM0_SDCTL	SD Control Register	5026 8008h	5026 9008h
Ch	16	CONTROLSS_SDFM0_SDMFILEN	SD Master Filter Enable	5026 800Ch	5026 900Ch
Eh	16	CONTROLSS_SDFM0_SDSTATUS	SD Status Register	5026 800Eh	5026 900Eh
20h	16	CONTROLSS_SDFM0_SDCTLPARM1	Control Parameter Register for Ch1	5026 8020h	5026 9020h
22h	16	CONTROLSS_SDFM0_SDDFPARM1	Data Filter Parameter Register for Ch1	5026 8022h	5026 9022h
24h	16	CONTROLSS_SDFM0_SDDPARM1	Data Parameter Register for Ch1	5026 8024h	5026 9024h
26h	16	CONTROLSS_SDFM0_SDFLT1CMPH1	High-level Threshold Register for Ch1	5026 8026h	5026 9026h
28h	16	CONTROLSS_SDFM0_SDFLT1CMPL1	Low-level Threshold Register for Ch1	5026 8028h	5026 9028h
2Ah	16	CONTROLSS_SDFM0_SDCPARM1	Comparator Filter Parameter Register for Ch1	5026 802Ah	5026 902Ah
2Ch	32	CONTROLSS_SDFM0_SDDATA1	Data Filter Data Register (16 or 32bit) for Ch1	5026 802Ch	5026 902Ch
30h	32	CONTROLSS_SDFM0_SDDATFIFO1	Filter Data FIFO Output(32b) for Ch1	5026 8030h	5026 9030h
34h	16	CONTROLSS_SDFM0_SDCDATA1	Comparator Filter Data Register (16b) for Ch1	5026 8034h	5026 9034h
36h	16	CONTROLSS_SDFM0_SDFLT1CMPH2	Second high level threhold for CH1	5026 8036h	5026 9036h
38h	16	CONTROLSS_SDFM0_SDFLT1CMPHZ	High-level (Z) Threshold Register for Ch1	5026 8038h	5026 9038h
3Ah	16	CONTROLSS_SDFM0_SDFIFOCTL1	FIFO Control Register for Ch1	5026 803Ah	5026 903Ah
3Ch	16	CONTROLSS_SDFM0_SDSYNC1	SD Filter Sync control for Ch1	5026 803Ch	5026 903Ch
3Eh	16	CONTROLSS_SDFM0_SDFLT1CMPL2	Second low level threhold for CH1	5026 803Eh	5026 903Eh
40h	16	CONTROLSS_SDFM0_SDCTLPARM2	Control Parameter Register for Ch2	5026 8040h	5026 9040h

Table 3-2826. CONTROLSS_SDFM0, CONTROLSS_SDFM0_CONTROLSS_SDFM Registers, Base Address=5026 8000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
42h	16	CONTROLSS_SDFM0_SDDFPARM2	Data Filter Parameter Register for Ch2	5026 8042h	5026 9042h
44h	16	CONTROLSS_SDFM0_SDDPARM2	Data Parameter Register for Ch2	5026 8044h	5026 9044h
46h	16	CONTROLSS_SDFM0_SDFLT2CMPH1	High-level Threshold Register for Ch2	5026 8046h	5026 9046h
48h	16	CONTROLSS_SDFM0_SDFLT2CMPL1	Low-level Threshold Register for Ch2	5026 8048h	5026 9048h
4Ah	16	CONTROLSS_SDFM0_SDCPARM2	Comparator Filter Parameter Register for Ch2	5026 804Ah	5026 904Ah
4Ch	32	CONTROLSS_SDFM0_SDDATA2	Data Filter Data Register (16 or 32bit) for Ch2	5026 804Ch	5026 904Ch
50h	32	CONTROLSS_SDFM0_SDDATFIFO2	Filter Data FIFO Output(32b) for Ch2	5026 8050h	5026 9050h
54h	16	CONTROLSS_SDFM0_SDCDATA2	Comparator Filter Data Register (16b) for Ch2	5026 8054h	5026 9054h
56h	16	CONTROLSS_SDFM0_SDFLT2CMPH2	Second high level threhold for CH2	5026 8056h	5026 9056h
58h	16	CONTROLSS_SDFM0_SDFLT2CMPHZ	High-level (Z) Threshold Register for Ch2	5026 8058h	5026 9058h
5Ah	16	CONTROLSS_SDFM0_SDFIFOCTL2	FIFO Control Register for Ch2	5026 805Ah	5026 905Ah
5Ch	16	CONTROLSS_SDFM0_SDSYNC2	SD Filter Sync control for Ch2	5026 805Ch	5026 905Ch
5Eh	16	CONTROLSS_SDFM0_SDFLT2CMPL2	Second low level threhold for CH2	5026 805Eh	5026 905Eh
60h	16	CONTROLSS_SDFM0_SDCTLPARM3	Control Parameter Register for Ch3	5026 8060h	5026 9060h
62h	16	CONTROLSS_SDFM0_SDDFPARM3	Data Filter Parameter Register for Ch3	5026 8062h	5026 9062h
64h	16	CONTROLSS_SDFM0_SDDPARM3	Data Parameter Register for Ch3	5026 8064h	5026 9064h
66h	16	CONTROLSS_SDFM0_SDFLT3CMPH1	High-level Threshold Register for Ch3	5026 8066h	5026 9066h
68h	16	CONTROLSS_SDFM0_SDFLT3CMPL1	Low-level Threshold Register for Ch3	5026 8068h	5026 9068h
6Ah	16	CONTROLSS_SDFM0_SDCPARM3	Comparator Filter Parameter Register for Ch3	5026 806Ah	5026 906Ah
6Ch	32	CONTROLSS_SDFM0_SDDATA3	Data Filter Data Register (16 or 32bit) for Ch3	5026 806Ch	5026 906Ch
70h	32	CONTROLSS_SDFM0_SDDATFIFO3	Filter Data FIFO Output(32b) for Ch3	5026 8070h	5026 9070h
74h	16	CONTROLSS_SDFM0_SDCDATA3	Comparator Filter Data Register (16b) for Ch3	5026 8074h	5026 9074h
76h	16	CONTROLSS_SDFM0_SDFLT3CMPH2	Second high level threhold for CH3	5026 8076h	5026 9076h
78h	16	CONTROLSS_SDFM0_SDFLT3CMPHZ	High-level (Z) Threshold Register for Ch3	5026 8078h	5026 9078h
7Ah	16	CONTROLSS_SDFM0_SDFIFOCTL3	FIFO Control Register for Ch3	5026 807Ah	5026 907Ah
7Ch	16	CONTROLSS_SDFM0_SDSYNC3	SD Filter Sync control for Ch3	5026 807Ch	5026 907Ch

Table 3-2826. CONTROLSS_SDFM0, CONTROLSS_SDFM0_CONTROLSS_SDFM Registers, Base Address=5026 8000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
7Eh	16	CONTROLSS_SDFM0_SDFLT3CMPL2	Second low level threhold for CH3	5026 807Eh	5026 907Eh
80h	16	CONTROLSS_SDFM0_SDCTLPARM4	Control Parameter Register for Ch4	5026 8080h	5026 9080h
82h	16	CONTROLSS_SDFM0_SDDFPARM4	Data Filter Parameter Register for Ch4	5026 8082h	5026 9082h
84h	16	CONTROLSS_SDFM0_SDDPARM4	Data Parameter Register for Ch4	5026 8084h	5026 9084h
86h	16	CONTROLSS_SDFM0_SDFLT4CMPH1	High-level Threshold Register for Ch4	5026 8086h	5026 9086h
88h	16	CONTROLSS_SDFM0_SDFLT4CMPL1	Low-level Threshold Register for Ch4	5026 8088h	5026 9088h
8Ah	16	CONTROLSS_SDFM0_SDCPARM4	Comparator Filter Parameter Register for Ch4	5026 808Ah	5026 908Ah
8Ch	32	CONTROLSS_SDFM0_SDDATA4	Data Filter Data Register (16 or 32bit) for Ch4	5026 808Ch	5026 908Ch
90h	32	CONTROLSS_SDFM0_SDDATFIFO4	Filter Data FIFO Output(32b) for Ch4	5026 8090h	5026 9090h
94h	16	CONTROLSS_SDFM0_SDCDATA4	Comparator Filter Data Register (16b) for Ch4	5026 8094h	5026 9094h
96h	16	CONTROLSS_SDFM0_SDFLT4CMPH2	Second high level threhold for CH4	5026 8096h	5026 9096h
98h	16	CONTROLSS_SDFM0_SDFLT4CMPHZ	High-level (Z) Threshold Register for Ch4	5026 8098h	5026 9098h
9Ah	16	CONTROLSS_SDFM0_SDFIFOCTL4	FIFO Control Register for Ch4	5026 809Ah	5026 909Ah
9Ch	16	CONTROLSS_SDFM0_SDSYNC4	SD Filter Sync control for Ch4	5026 809Ch	5026 909Ch
9Eh	16	CONTROLSS_SDFM0_SDFLT4CMPL2	Second low level threhold for CH4	5026 809Eh	5026 909Eh
C0h	16	CONTROLSS_SDFM0_SDCOMP1CTL	SD Comparator event filter1 Control Register	5026 80C0h	5026 90C0h
C2h	16	CONTROLSS_SDFM0_SDCOMP1EVT2FLTCTL	COMPL/CEVT2 Digital filter1 Control Register	5026 80C2h	5026 90C2h
C4h	16	CONTROLSS_SDFM0_SDCOMP1EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter1 Clock Control Register	5026 80C4h	5026 90C4h
C6h	16	CONTROLSS_SDFM0_SDCOMP1EVT1FLTCTL	COMPH/CEVT1 Digital filter1 Control Register	5026 80C6h	5026 90C6h
C8h	16	CONTROLSS_SDFM0_SDCOMP1EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter1 Clock Control Register	5026 80C8h	5026 90C8h
CEh	16	CONTROLSS_SDFM0_SDCOMP1LOCK	SD compartor event filter1 Lock Register	5026 80CEh	5026 90CEh
D0h	16	CONTROLSS_SDFM0_SDCOMP2CTL	SD Comparator event filter2 Control Register	5026 80D0h	5026 90D0h
D2h	16	CONTROLSS_SDFM0_SDCOMP2EVT2FLTCTL	COMPL/CEVT2 Digital filter2 Control Register	5026 80D2h	5026 90D2h
D4h	16	CONTROLSS_SDFM0_SDCOMP2EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter2 Clock Control Register	5026 80D4h	5026 90D4h
D6h	16	CONTROLSS_SDFM0_SDCOMP2EVT1FLTCTL	COMPH/CEVT1 Digital filter2 Control Register	5026 80D6h	5026 90D6h

Table 3-2826. CONTROLSS_SDFM0, CONTROLSS_SDFM0_CONTROLSS_SDFM Registers, Base Address=5026 8000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
D8h	16	CONTROLSS_SDFM0_SDCOMP2EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter2 Clock Control Register	5026 80D8h	5026 90D8h
DEh	16	CONTROLSS_SDFM0_SDCOMP2LOCK	SD compartor event filter2 Lock Register	5026 80DEh	5026 90DEh
E0h	16	CONTROLSS_SDFM0_SDCOMP3CTL	SD Comparator event filter3 Control Register	5026 80E0h	5026 90E0h
E2h	16	CONTROLSS_SDFM0_SDCOMP3EVT2FLTCTL	COMPL/CEVT2 Digital filter3 Control Register	5026 80E2h	5026 90E2h
E4h	16	CONTROLSS_SDFM0_SDCOMP3EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter3 Clock Control Register	5026 80E4h	5026 90E4h
E6h	16	CONTROLSS_SDFM0_SDCOMP3EVT1FLTCTL	COMPH/CEVT1 Digital filter3 Control Register	5026 80E6h	5026 90E6h
E8h	16	CONTROLSS_SDFM0_SDCOMP3EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter3 Clock Control Register	5026 80E8h	5026 90E8h
EEh	16	CONTROLSS_SDFM0_SDCOMP3LOCK	SD compartor event filter3 Lock Register	5026 80EEh	5026 90EEh
F0h	16	CONTROLSS_SDFM0_SDCOMP4CTL	SD Comparator event filter4 Control Register	5026 80F0h	5026 90F0h
F2h	16	CONTROLSS_SDFM0_SDCOMP4EVT2FLTCTL	COMPL/CEVT2 Digital filter4 Control Register	5026 80F2h	5026 90F2h
F4h	16	CONTROLSS_SDFM0_SDCOMP4EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter4 Clock Control Register	5026 80F4h	5026 90F4h
F6h	16	CONTROLSS_SDFM0_SDCOMP4EVT1FLTCTL	COMPH/CEVT1 Digital filter4 Control Register	5026 80F6h	5026 90F6h
F8h	16	CONTROLSS_SDFM0_SDCOMP4EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter4 Clock Control Register	5026 80F8h	5026 90F8h
FEh	16	CONTROLSS_SDFM0_SDCOMP4LOCK	SD compartor event filter4 Lock Register	5026 80FEh	5026 90FEh

3.19.1 CONTROLSS_SDFM0_SDIFLGCLR Register (Offset = 4h) [reset = h]

Short Description: SD Module Interrupt Flag Clear Bits: Writing a "1" will clear the respective flag bit in the SDIFLG register. Writes of "0" are ignored. Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.

Long Description:

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Table 3-2827. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8004h
CONTROLSS_SDFM1	5026 9004h

Figure 3-1385. CONTROLSS_SDFM0_SDIFLGCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIF	RESERVED							SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
RWRRETURNS0S	RO RRETURNS0S							RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S
0	0							0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1	FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S	RWRRETURNS0S
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 3-2828. SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	RW RRETURNS0S	0h	Flag-clear bit for SDFM Master Interrupt flag. Writing a 1 to clear MIF flag in SDIFLG register Writes of "0" are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted (pulsed low)
30 - 24	RESERVED	RO RRETURNS0S		Reserved
23	SDFFINT4	RW RRETURNS0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch4
22	SDFFINT3	RW RRETURNS0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch3
21	SDFFINT2	RW RRETURNS0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch2
20	SDFFINT1	RW RRETURNS0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch1
19	SDFFOVF4	RW RRETURNS0S	0h	SDFIFO overflow clear Ch4

Table 3-2828. SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	SDFFOVF3	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch3
17	SDFFOVF2	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch2
16	SDFFOVF1	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch1
15	AF4	RW RRETURNS 0S	0h	Flag-clear bit for Acknowledge flag for Filter 4
14	AF3	RW RRETURNS 0S	0h	Flag Clear bit for AF3
13	AF2	RW RRETURNS 0S	0h	Flag Clear bit for AF2
12	AF1	RW RRETURNS 0S	0h	Flag Clear bit for AF1
11	MF4	RW RRETURNS 0S	0h	Flag Clear bit for MF4
10	MF3	RW RRETURNS 0S	0h	Flag Clear bit for MF3
9	MF2	RW RRETURNS 0S	0h	Flag Clear bit for MF2
8	MF1	RW RRETURNS 0S	0h	Flag Clear bit for MF1
7	FLT4_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT4_FLG_CEVT2
6	FLT4_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT4_FLG_CEVT1
5	FLT3_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT3_FLG_CEVT2
4	FLT3_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT3_FLG_CEVT1
3	FLT2_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT2_FLG_CEVT2
2	FLT2_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT2_FLG_CEVT1
1	FLT1_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT1_FLG_CEVT2
0	FLT1_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT1_FLG_CEVT1

3.19.2 CONTROLSS_SDFM0_SDCTL Register (Offset = 8h) [reset = h]

Short Description: SD Control Register

Long Description:

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Table 3-2829. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8008h
CONTROLSS_SDFM1	5026 9008h

Figure 3-1386. CONTROLSS_SDFM0_SDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	MIE	RESERVED				
RO RRETURNS0S	RO RRETURNS0S	RW	RO RRETURNS0S				
0	0	0	0				
7	6	5	4	3	2	1	0
RESERVED				HZ4	HZ3	HZ2	HZ1
RO RRETURNS0S				RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S	RW RRETURNS0S
0				0	0	0	0

Access Types Legend

Table 3-2830. SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14	RESERVED	RO RRETURNS 0S		Reserved
13	MIE	RW	0h	Master SDy_ERR interrupt enable 0: SDy_ERR Interrupt and interrupt flags are disabled 1: SDy_ERR Interrupt and interrupt flags are enabled
12 - 4	RESERVED	RO RRETURNS 0S		Reserved
3	HZ4	RW RRETURNS 0S	0h	Flag Clear bit for HZ4
2	HZ3	RW RRETURNS 0S	0h	Flag Clear bit for HZ3
1	HZ2	RW RRETURNS 0S	0h	Flag Clear bit for HZ2
0	HZ1	RW RRETURNS 0S	0h	Flag Clear bit for HZ1

3.19.3 CONTROLSS_SDFM0_SDMFILEN Register (Offset = Ch) [reset = h]

Short Description: SD Master Filter Enable

Long Description:

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Table 3-2831. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 800Ch
CONTROLSS_SDFM1	5026 900Ch

Figure 3-1387. CONTROLSS_SDFM0_SDMFILEN Name Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED	MFE	RESERVED	RESERVED	RESERVED
RO RRETURNS0S			RO RRETURNS0S	RW	RO RRETURNS0S	RO RRETURNS0S	RO RRETURNS0S
0			0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED			
RO RRETURNS0S	RO RRETURNS0S			RO RRETURNS0S			
0	0			0			

Access Types Legend

Table 3-2832. SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO RRETURNS 0S		Reserved
12	RESERVED	RO RRETURNS 0S		Reserved
11	MFE	RW	0h	Master Filter Enable 0: All the four data filter units of SDFM module are disabled. All FIFOs are cleared 1: Data filter units can be enabled if bit FEN is '1'.
10	RESERVED	RO RRETURNS 0S		Reserved
9	RESERVED	RO RRETURNS 0S		Reserved
8 - 7	RESERVED	RO RRETURNS 0S		Reserved
6 - 4	RESERVED	RO RRETURNS 0S		Reserved
3 - 0	RESERVED	RO RRETURNS 0S		Reserved

3.19.4 CONTROLSS_SDFM0_SDSTATUS Register (Offset = Eh) [reset = h]

Short Description: SD Status Register

Long Description:

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Table 3-2833. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 800Eh
CONTROLSS_SDFM1	5026 900Eh

Figure 3-1388. CONTROLSS_SDFM0_SDSTATUS Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED				HZ4	HZ3	HZ2	HZ1
RO RRETURNS0S				RO	RO	RO	RO
0				0	0	0	0

Access Types Legend

Table 3-2834. SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13	RESERVED	RO		Reserved
12	RESERVED	RO		Reserved
11	RESERVED	RO		Reserved
10	RESERVED	RO		Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7 - 4	RESERVED	RO RRETURNS 0S		Reserved
3	HZ4	RO	0h	High-level Threshold crossing (Z) flag Ch4 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ4.HLTZ 1: Comparator filter output '= SDCMPHZ4.HLTZ
2	HZ3	RO	0h	High-level Threshold crossing (Z) flag Ch3 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ3.HLTZ 1: Comparator filter output '= SDCMPHZ3.HLTZ
1	HZ2	RO	0h	High-level Threshold crossing (Z) flag Ch2 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ2.HLTZ 1: Comparator filter output '= SDCMPHZ2.HLTZ
0	HZ1	RO	0h	High-level Threshold crossing (Z) flag Ch1 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ1.HLTZ 1: Comparator filter output '= SDCMPHZ1.HLTZ

3.19.5 CONTROLSS_SDFM0_SDCTLPARM1 Register (Offset = 20h) [reset = h]

Short Description: Control Parameter Register for Ch1

Long Description:

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Table 3-2835. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8020h
CONTROLSS_SDFM1	5026 9020h

Figure 3-1389. CONTROLSS_SDFM0_SDCTLPARM1 Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
RO RRETURNS0S	RW	RO RRETURNS0S	RW	RW	RW	RW	
0	0	0	0	0	0	0	

Access Types Legend

Table 3-2836. SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD1 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

3.19.6 CONTROLSS_SDFM0_SDDFPARM1 Register (Offset = 22h) [reset = h]

Short Description: Data Filter Parameter Register for Ch1

Long Description:

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Table 3-2837. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8022h
CONTROLSS_SDFM1	5026 9022h

Figure 3-1390. CONTROLSS_SDFM0_SDDFPARM1 Name Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
RO			RW	RW		RW	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
DOSR							
RW							
0							

Access Types Legend

Table 3-2838. SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

3.19.7 CONTROLSS_SDFM0_SDDPARM1 Register (Offset = 24h) [reset = h]

Short Description: Data Parameter Register for Ch1

Long Description:

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Table 3-2839. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8024h
CONTROLSS_SDFM1	5026 9024h

Figure 3-1391. CONTROLSS_SDFM0_SDDPARM1 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
RW					RW	RO RRETURNS0S	
0					0	0	
7	6	5	4	3	2	1	0
RESERVED							
RO RRETURNS0S							
0							

Access Types Legend

Table 3-2840. SDDPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

3.19.8 CONTROLSS_SDFM0_SDFLT1CMPH1 Register (Offset = 26h) [reset = h]

Short Description: High-level Threshold Register for Ch1

Long Description:

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Table 3-2841. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8026h
CONTROLSS_SDFM1	5026 9026h

Figure 3-1392. CONTROLSS_SDFM0_SDFLT1CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT							
RW							
111111111111111							

Access Types Legend

Table 3-2842. SDFLT1CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	650E124EF 1C7h	Unsigned high-level threshold for the comparator filter output.

3.19.9 CONTROLSS_SDFM0_SDFLT1CMPL1 Register (Offset = 28h) [reset = h]

Short Description: Low-level Threshold Register for Ch1

Long Description:

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Table 3-2843. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8028h
CONTROLSS_SDFM1	5026 9028h

Figure 3-1393. CONTROLSS_SDFM0_SDFLT1CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT							
RW							
0							

Access Types Legend

Table 3-2844. SDFLT1CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

3.19.10 CONTROLSS_SDFM0_SDCPARM1 Register (Offset = 2Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch1

Long Description:

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Table 3-2845. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 802Ah
CONTROLSS_SDFM1	5026 902Ah

Figure 3-1394. CONTROLSS_SDFM0_SDCPARM1 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
RW		RW	RW		RW	RW	RW
0		0	0		0	0	0
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
RW	RW	RW	RW				
0	0	0	0				

Access Types Legend

Table 3-2846. SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

3.19.11 CONTROLSS_SDFM0_SDDATA1 Register (Offset = 2Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch1

Long Description:

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Table 3-2847. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 802Ch
CONTROLSS_SDFM1	5026 902Ch

Figure 3-1395. CONTROLSS_SDFM0_SDDATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2848. SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.12 CONTROLSS_SDFM0_SDDATFIFO1 Register (Offset = 30h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch1

Long Description:

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Table 3-2849. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8030h
CONTROLSS_SDFM1	5026 9030h

Figure 3-1396. CONTROLSS_SDFM0_SDDATFIFO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2850. SDDATFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.13 CONTROLSS_SDFM0_SDCDATA1 Register (Offset = 34h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch1

Long Description:

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Table 3-2851. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8034h
CONTROLSS_SDFM1	5026 9034h

Figure 3-1397. CONTROLSS_SDFM0_SDCDATA1 Name Register

15	14	13	12	11	10	9	8
DATA16							
RO							
0							
7	6	5	4	3	2	1	0
DATA16							
RO							
0							

Access Types Legend

Table 3-2852. SDCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

3.19.14 CONTROLSS_SDFM0_SDFLT1CMPH2 Register (Offset = 36h) [reset = h]

Short Description: Second high level threhold for CH1

Long Description:

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Table 3-2853. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8036h
CONTROLSS_SDFM1	5026 9036h

Figure 3-1398. CONTROLSS_SDFM0_SDFLT1CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
RO RRETURNS0S	RW						
0	11111111111111						
7	6	5	4	3	2	1	0
HLT2							
RW							
11111111111111							

Access Types Legend

Table 3-2854. SDFLT1CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	650E124EF 1C7h	Second Unsigned high-level threshold for the comparator filter output.

3.19.15 CONTROLSS_SDFM0_SDFLT1CMPHZ Register (Offset = 38h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch1

Long Description:

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Table 3-2855. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8038h
CONTROLSS_SDFM1	5026 9038h

Figure 3-1399. CONTROLSS_SDFM0_SDFLT1CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
HLTZ							
RW							
0							

Access Types Legend

Table 3-2856. SDFLT1CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

3.19.16 CONTROLSS_SDFM0_SDFIFOCTL1 Register (Offset = 3Ah) [reset = h]

Short Description: FIFO Control Register for Ch1

Long Description:

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Table 3-2857. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Ah
CONTROLSS_SDFM1	5026 903Ah

Figure 3-1400. CONTROLSS_SDFM0_SDFIFOCTL1 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
RW	RW	RW	RW	RO RRETURNS0S	RO		
0	0	0	0	0	0		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
RO		RO RRETURNS0S	RW				
0		0	0				

Access Types Legend

Table 3-2858. SDFIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

ADVANCE INFORMATION

3.19.17 CONTROLSS_SDFM0_SDSYNC1 Register (Offset = 3Ch) [reset = h]

Short Description: SD Filter Sync control for Ch1

Long Description:

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Table 3-2859. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Ch
CONTROLSS_SDFM1	5026 903Ch

Figure 3-1401. CONTROLSS_SDFM0_SDSYNC1 Name Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
RO RRETURNS0S					RW	RW	RW RRETURNS0S
0					1	0	0
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
RO	RW	RW					
0	0	0					

Access Types Legend

Table 3-2860. SDSYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

3.19.18 CONTROLSS_SDFM0_SDFLT1CMPL2 Register (Offset = 3Eh) [reset = h]

Short Description: Second low level threhold for CH1

Long Description:

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Table 3-2861. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Eh
CONTROLSS_SDFM1	5026 903Eh

Figure 3-1402. CONTROLSS_SDFM0_SDFLT1CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT2							
RW							
0							

Access Types Legend

Table 3-2862. SDFLT1CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

3.19.19 CONTROLSS_SDFM0_SDCTLPARM2 Register (Offset = 40h) [reset = h]

Short Description: Control Parameter Register for Ch2

Long Description:

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Table 3-2863. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8040h
CONTROLSS_SDFM1	5026 9040h

Figure 3-1403. CONTROLSS_SDFM0_SDCTLPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
RO RRETURNS0S	RW	RO RRETURNS0S	RW	RW	RW	RW	
0	0	0	0	0	0	0	

Access Types Legend

Table 3-2864. SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD2 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

3.19.20 CONTROLSS_SDFM0_SDDFPARM2 Register (Offset = 42h) [reset = h]

Short Description: Data Filter Parameter Register for Ch2

Long Description:

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Table 3-2865. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8042h
CONTROLSS_SDFM1	5026 9042h

Figure 3-1404. CONTROLSS_SDFM0_SDDFPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
RO			RW	RW		RW	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
DOSR							
RW							
0							

Access Types Legend

Table 3-2866. SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

3.19.21 CONTROLSS_SDFM0_SDDPARM2 Register (Offset = 44h) [reset = h]

Short Description: Data Parameter Register for Ch2

Long Description:

Return to Summary Table

Table 3-2867. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8044h
CONTROLSS_SDFM1	5026 9044h

Figure 3-1405. CONTROLSS_SDFM0_SDDPARM2 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
RW					RW	RO RRETURNS0S	
0					0	0	
7	6	5	4	3	2	1	0
RESERVED							
RO RRETURNS0S							
0							

Access Types Legend

Table 3-2868. SDDPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

3.19.22 CONTROLSS_SDFM0_SDFLT2CMPH1 Register (Offset = 46h) [reset = h]

Short Description: High-level Threshold Register for Ch2

Long Description:

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Table 3-2869. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8046h
CONTROLSS_SDFM1	5026 9046h

Figure 3-1406. CONTROLSS_SDFM0_SDFLT2CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT							
RW							
111111111111111							

Access Types Legend

Table 3-2870. SDFLT2CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	650E124EF 1C7h	Unsigned high-level threshold for the comparator filter output.

3.19.23 CONTROLSS_SDFM0_SDFLT2CMPL1 Register (Offset = 48h) [reset = h]

Short Description: Low-level Threshold Register for Ch2

Long Description:

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Table 3-2871. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8048h
CONTROLSS_SDFM1	5026 9048h

Figure 3-1407. CONTROLSS_SDFM0_SDFLT2CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT							
RW							
0							

Access Types Legend

Table 3-2872. SDFLT2CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

3.19.24 CONTROLSS_SDFM0_SDCPARM2 Register (Offset = 4Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch2

Long Description:

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Table 3-2873. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 804Ah
CONTROLSS_SDFM1	5026 904Ah

Figure 3-1408. CONTROLSS_SDFM0_SDCPARM2 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
RW		RW	RW		RW	RW	RW
0		0	0		0	0	0
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
RW	RW	RW	RW				
0	0	0	0				

Access Types Legend

Table 3-2874. SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

3.19.25 CONTROLSS_SDFM0_SDDATA2 Register (Offset = 4Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch2

Long Description:

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Table 3-2875. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 804Ch
CONTROLSS_SDFM1	5026 904Ch

Figure 3-1409. CONTROLSS_SDFM0_SDDATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2876. SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.26 CONTROLSS_SDFM0_SDDATFIFO2 Register (Offset = 50h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch2

Long Description:

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Table 3-2877. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8050h
CONTROLSS_SDFM1	5026 9050h

Figure 3-1410. CONTROLSS_SDFM0_SDDATFIFO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2878. SDDATFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.27 CONTROLSS_SDFM0_SDCDATA2 Register (Offset = 54h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch2

Long Description:

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Table 3-2879. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8054h
CONTROLSS_SDFM1	5026 9054h

Figure 3-1411. CONTROLSS_SDFM0_SDCDATA2 Name Register

15	14	13	12	11	10	9	8
DATA16							
RO							
0							
7	6	5	4	3	2	1	0
DATA16							
RO							
0							

Access Types Legend

Table 3-2880. SDCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

3.19.28 CONTROLSS_SDFM0_SDFLT2CMPH2 Register (Offset = 56h) [reset = h]

Short Description: Second high level threhold for CH2

Long Description:

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Table 3-2881. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8056h
CONTROLSS_SDFM1	5026 9056h

Figure 3-1412. CONTROLSS_SDFM0_SDFLT2CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT2							
RW							
111111111111111							

Access Types Legend

Table 3-2882. SDFLT2CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	650E124EF 1C7h	Second Unsigned high-level threshold for the comparator filter output.

3.19.29 CONTROLSS_SDFM0_SDFLT2CMPHZ Register (Offset = 58h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch2

Long Description:

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Table 3-2883. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8058h
CONTROLSS_SDFM1	5026 9058h

Figure 3-1413. CONTROLSS_SDFM0_SDFLT2CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
HLTZ							
RW							
0							

Access Types Legend

Table 3-2884. SDFLT2CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

3.19.30 CONTROLSS_SDFM0_SDFIFOCTL2 Register (Offset = 5Ah) [reset = h]

Short Description: FIFO Control Register for Ch2

Long Description:

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Table 3-2885. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Ah
CONTROLSS_SDFM1	5026 905Ah

Figure 3-1414. CONTROLSS_SDFM0_SDFIFOCTL2 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
RW	RW	RW	RW	RO RRETURNS0S	RO		
0	0	0	0	0	0		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
RO		RO RRETURNS0S	RW				
0		0	0				

Access Types Legend

Table 3-2886. SDFIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

ADVANCE INFORMATION

3.19.31 CONTROLSS_SDFM0_SDSYNC2 Register (Offset = 5Ch) [reset = h]

Short Description: SD Filter Sync control for Ch2

Long Description:

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Table 3-2887. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Ch
CONTROLSS_SDFM1	5026 905Ch

Figure 3-1415. CONTROLSS_SDFM0_SDSYNC2 Name Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
RO RRETURNS0S					RW	RW	RW RRETURNS0S
0					1	0	0
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
RO	RW	RW					
0	0	0					

Access Types Legend

Table 3-2888. SDSYNC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

3.19.32 CONTROLSS_SDFM0_SDFLT2CMPL2 Register (Offset = 5Eh) [reset = h]

Short Description: Second low level threhold for CH2

Long Description:

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Table 3-2889. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Eh
CONTROLSS_SDFM1	5026 905Eh

Figure 3-1416. CONTROLSS_SDFM0_SDFLT2CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT2							
RW							
0							

Access Types Legend

Table 3-2890. SDFLT2CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

3.19.33 CONTROLSS_SDFM0_SDCTLPARM3 Register (Offset = 60h) [reset = h]

Short Description: Control Parameter Register for Ch3

Long Description:

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Table 3-2891. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8060h
CONTROLSS_SDFM1	5026 9060h

Figure 3-1417. CONTROLSS_SDFM0_SDCTLPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
RO RRETURNS0S	RW	RO RRETURNS0S	RW	RW	RW	RW	
0	0	0	0	0	0	0	

Access Types Legend

Table 3-2892. SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD3 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

3.19.34 CONTROLSS_SDFM0_SDDFPARM3 Register (Offset = 62h) [reset = h]

Short Description: Data Filter Parameter Register for Ch3

Long Description:

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Table 3-2893. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8062h
CONTROLSS_SDFM1	5026 9062h

Figure 3-1418. CONTROLSS_SDFM0_SDDFPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
RO			RW	RW		RW	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
DOSR							
RW							
0							

Access Types Legend

Table 3-2894. SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

3.19.35 CONTROLSS_SDFM0_SDDPARM3 Register (Offset = 64h) [reset = h]

Short Description: Data Parameter Register for Ch3

Long Description:

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Table 3-2895. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8064h
CONTROLSS_SDFM1	5026 9064h

Figure 3-1419. CONTROLSS_SDFM0_SDDPARM3 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
RW					RW	RO RRETURNS0S	
0					0	0	
7	6	5	4	3	2	1	0
RESERVED							
RO RRETURNS0S							
0							

Access Types Legend

Table 3-2896. SDDPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

3.19.36 CONTROLSS_SDFM0_SDFLT3CMPH1 Register (Offset = 66h) [reset = h]

Short Description: High-level Threshold Register for Ch3

Long Description:

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Table 3-2897. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8066h
CONTROLSS_SDFM1	5026 9066h

Figure 3-1420. CONTROLSS_SDFM0_SDFLT3CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT							
RW							
111111111111111							

Access Types Legend

Table 3-2898. SDFLT3CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	650E124EF 1C7h	Unsigned high-level threshold for the comparator filter output.

3.19.37 CONTROLSS_SDFM0_SDFLT3CMPL1 Register (Offset = 68h) [reset = h]

Short Description: Low-level Threshold Register for Ch3

Long Description:

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Table 3-2899. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8068h
CONTROLSS_SDFM1	5026 9068h

Figure 3-1421. CONTROLSS_SDFM0_SDFLT3CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT							
RW							
0							

Access Types Legend

Table 3-2900. SDFLT3CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

3.19.38 CONTROLSS_SDFM0_SDCPARM3 Register (Offset = 6Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch3

Long Description:

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Table 3-2901. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 806Ah
CONTROLSS_SDFM1	5026 906Ah

Figure 3-1422. CONTROLSS_SDFM0_SDCPARM3 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
RW		RW	RW		RW	RW	RW
0		0	0		0	0	0
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
RW	RW	RW	RW				
0	0	0	0				

Access Types Legend

Table 3-2902. SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

3.19.39 CONTROLSS_SDFM0_SDDATA3 Register (Offset = 6Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch3

Long Description:

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Table 3-2903. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 806Ch
CONTROLSS_SDFM1	5026 906Ch

Figure 3-1423. CONTROLSS_SDFM0_SDDATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2904. SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.40 CONTROLSS_SDFM0_SDDATFIFO3 Register (Offset = 70h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch3

Long Description:

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Table 3-2905. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8070h
CONTROLSS_SDFM1	5026 9070h

Figure 3-1424. CONTROLSS_SDFM0_SDDATFIFO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2906. SDDATFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.41 CONTROLSS_SDFM0_SDCDATA3 Register (Offset = 74h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch3

Long Description:

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Table 3-2907. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8074h
CONTROLSS_SDFM1	5026 9074h

Figure 3-1425. CONTROLSS_SDFM0_SDCDATA3 Name Register

15	14	13	12	11	10	9	8
DATA16							
RO							
0							
7	6	5	4	3	2	1	0
DATA16							
RO							
0							

Access Types Legend

Table 3-2908. SDCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

3.19.42 CONTROLSS_SDFM0_SDFLT3CMPH2 Register (Offset = 76h) [reset = h]

Short Description: Second high level threhold for CH3

Long Description:

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Table 3-2909. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8076h
CONTROLSS_SDFM1	5026 9076h

Figure 3-1426. CONTROLSS_SDFM0_SDFLT3CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT2							
RW							
111111111111111							

Access Types Legend

Table 3-2910. SDFLT3CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	650E124EF 1C7h	Second Unsigned high-level threshold for the comparator filter output.

3.19.43 CONTROLSS_SDFM0_SDFLT3CMPHZ Register (Offset = 78h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch3

Long Description:

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Table 3-2911. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8078h
CONTROLSS_SDFM1	5026 9078h

Figure 3-1427. CONTROLSS_SDFM0_SDFLT3CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
HLTZ							
RW							
0							

Access Types Legend

Table 3-2912. SDFLT3CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

3.19.44 CONTROLSS_SDFM0_SDFIFOCTL3 Register (Offset = 7Ah) [reset = h]

Short Description: FIFO Control Register for Ch3

Long Description:

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Table 3-2913. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Ah
CONTROLSS_SDFM1	5026 907Ah

Figure 3-1428. CONTROLSS_SDFM0_SDFIFOCTL3 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
RW	RW	RW	RW	RO RRETURNS0S	RO		
0	0	0	0	0	0		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
RO		RO RRETURNS0S	RW				
0		0	0				

Access Types Legend

Table 3-2914. SDFIFOCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

ADVANCE INFORMATION

3.19.45 CONTROLSS_SDFM0_SDSYNC3 Register (Offset = 7Ch) [reset = h]

Short Description: SD Filter Sync control for Ch3

Long Description:

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Table 3-2915. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Ch
CONTROLSS_SDFM1	5026 907Ch

Figure 3-1429. CONTROLSS_SDFM0_SDSYNC3 Name Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
RO RRETURNS0S					RW	RW	RW RRETURNS0S
0					1	0	0
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
RO	RW	RW					
0	0	0					

Access Types Legend

Table 3-2916. SDSYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

3.19.46 CONTROLSS_SDFM0_SDFLT3CMPL2 Register (Offset = 7Eh) [reset = h]

Short Description: Second low level threhold for CH3

Long Description:

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Table 3-2917. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Eh
CONTROLSS_SDFM1	5026 907Eh

Figure 3-1430. CONTROLSS_SDFM0_SDFLT3CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT2							
RW							
0							

Access Types Legend

Table 3-2918. SDFLT3CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

3.19.47 CONTROLSS_SDFM0_SDCTLPARM4 Register (Offset = 80h) [reset = h]

Short Description: Control Parameter Register for Ch4

Long Description:

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Table 3-2919. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8080h
CONTROLSS_SDFM1	5026 9080h

Figure 3-1431. CONTROLSS_SDFM0_SDCTLPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
RO RRETURNS0S	RW	RO RRETURNS0S	RW	RW	RW	RW	
0	0	0	0	0	0	0	

Access Types Legend

Table 3-2920. SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD4 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

3.19.48 CONTROLSS_SDFM0_SDDFPARM4 Register (Offset = 82h) [reset = h]

Short Description: Data Filter Parameter Register for Ch4

Long Description:

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Table 3-2921. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8082h
CONTROLSS_SDFM1	5026 9082h

Figure 3-1432. CONTROLSS_SDFM0_SDDFPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
RO			RW	RW		RW	RW
0			0	0		0	0
7	6	5	4	3	2	1	0
DOSR							
RW							
0							

Access Types Legend

Table 3-2922. SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

3.19.49 CONTROLSS_SDFM0_SDDPARM4 Register (Offset = 84h) [reset = h]

Short Description: Data Parameter Register for Ch4

Long Description:

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Table 3-2923. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8084h
CONTROLSS_SDFM1	5026 9084h

Figure 3-1433. CONTROLSS_SDFM0_SDDPARM4 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
RW					RW	RO RRETURNS0S	
0					0	0	
7	6	5	4	3	2	1	0
RESERVED							
RO RRETURNS0S							
0							

Access Types Legend

Table 3-2924. SDDPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

3.19.50 CONTROLSS_SDFM0_SDFLT4CMPH1 Register (Offset = 86h) [reset = h]

Short Description: High-level Threshold Register for Ch4

Long Description:

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Table 3-2925. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8086h
CONTROLSS_SDFM1	5026 9086h

Figure 3-1434. CONTROLSS_SDFM0_SDFLT4CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
RO RRETURNS0S	RW						
0	111111111111111						
7	6	5	4	3	2	1	0
HLT							
RW							
111111111111111							

Access Types Legend

Table 3-2926. SDFLT4CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	650E124EF 1C7h	Unsigned high-level threshold for the comparator filter output.

3.19.51 CONTROLSS_SDFM0_SDFLT4CMPL1 Register (Offset = 88h) [reset = h]

Short Description: Low-level Threshold Register for Ch4

Long Description:

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Table 3-2927. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8088h
CONTROLSS_SDFM1	5026 9088h

Figure 3-1435. CONTROLSS_SDFM0_SDFLT4CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT							
RW							
0							

Access Types Legend

Table 3-2928. SDFLT4CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

3.19.52 CONTROLSS_SDFM0_SDCPARM4 Register (Offset = 8Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch4

Long Description:

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Table 3-2929. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 808Ah
CONTROLSS_SDFM1	5026 908Ah

Figure 3-1436. CONTROLSS_SDFM0_SDCPARM4 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
RW		RW	RW		RW	RW	RW
0		0	0		0	0	0
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
RW	RW	RW	RW				
0	0	0	0				

Access Types Legend

Table 3-2930. SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

3.19.53 CONTROLSS_SDFM0_SDDATA4 Register (Offset = 8Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch4

Long Description:

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Table 3-2931. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 808Ch
CONTROLSS_SDFM1	5026 908Ch

Figure 3-1437. CONTROLSS_SDFM0_SDDATA4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2932. SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.54 CONTROLSS_SDFM0_SDDATFIFO4 Register (Offset = 90h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch4

Long Description:

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Table 3-2933. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8090h
CONTROLSS_SDFM1	5026 9090h

Figure 3-1438. CONTROLSS_SDFM0_SDDATFIFO4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA32HI															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA16															
RO															
0															

Access Types Legend

Table 3-2934. SDDATFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

3.19.55 CONTROLSS_SDFM0_SDCDATA4 Register (Offset = 94h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch4

Long Description:

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Table 3-2935. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8094h
CONTROLSS_SDFM1	5026 9094h

Figure 3-1439. CONTROLSS_SDFM0_SDCDATA4 Name Register

15	14	13	12	11	10	9	8
DATA16							
RO							
0							
7	6	5	4	3	2	1	0
DATA16							
RO							
0							

Access Types Legend

Table 3-2936. SDCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

3.19.56 CONTROLSS_SDFM0_SDFLT4CMPH2 Register (Offset = 96h) [reset = h]

Short Description: Second high level threhold for CH4

Long Description:

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Table 3-2937. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8096h
CONTROLSS_SDFM1	5026 9096h

Figure 3-1440. CONTROLSS_SDFM0_SDFLT4CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
RO RRETURNS0S	RW						
0	11111111111111						
7	6	5	4	3	2	1	0
HLT2							
RW							
11111111111111							

Access Types Legend

Table 3-2938. SDFLT4CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	650E124EF 1C7h	Second Unsigned high-level threshold for the comparator filter output.

3.19.57 CONTROLSS_SDFM0_SDFLT4CMPHZ Register (Offset = 98h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch4

Long Description:

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Table 3-2939. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8098h
CONTROLSS_SDFM1	5026 9098h

Figure 3-1441. CONTROLSS_SDFM0_SDFLT4CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
HLTZ							
RW							
0							

Access Types Legend

Table 3-2940. SDFLT4CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

3.19.58 CONTROLSS_SDFM0_SDFIFOCTL4 Register (Offset = 9Ah) [reset = h]

Short Description: FIFO Control Register for Ch4

Long Description:

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Table 3-2941. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Ah
CONTROLSS_SDFM1	5026 909Ah

Figure 3-1442. CONTROLSS_SDFM0_SDFIFOCTL4 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
RW	RW	RW	RW	RO RRETURNS0S	RO		
0	0	0	0	0	0		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
RO		RO RRETURNS0S	RW				
0		0	0				

Access Types Legend

Table 3-2942. SDFIFOCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

3.19.59 CONTROLSS_SDFM0_SDSYNC4 Register (Offset = 9Ch) [reset = h]

Short Description: SD Filter Sync control for Ch4

Long Description:

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Table 3-2943. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Ch
CONTROLSS_SDFM1	5026 909Ch

Figure 3-1443. CONTROLSS_SDFM0_SDSYNC4 Name Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
RO RRETURNS0S					RW	RW	RW RRETURNS0S
0					1	0	0
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
RO	RW	RW					
0	0	0					

Access Types Legend

Table 3-2944. SDSYNC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

3.19.60 CONTROLSS_SDFM0_SDFLT4CMPL2 Register (Offset = 9Eh) [reset = h]

Short Description: Second low level threhold for CH4

Long Description:

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Table 3-2945. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Eh
CONTROLSS_SDFM1	5026 909Eh

Figure 3-1444. CONTROLSS_SDFM0_SDFLT4CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
RO RRETURNS0S	RW						
0	0						
7	6	5	4	3	2	1	0
LLT2							
RW							
0							

Access Types Legend

Table 3-2946. SDFLT4CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

3.19.61 CONTROLSS_SDFM0_SDCOMP1CTL Register (Offset = C0h) [reset = h]

Short Description: SD Comparator event filter1 Control Register

Long Description:

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Table 3-2947. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C0h
CONTROLSS_SDFM1	5026 90C0h

Figure 3-1445. CONTROLSS_SDFM0_SDCOMP1CTL Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0

Access Types Legend

Table 3-2948. SDCOMP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

3.19.62 CONTROLSS_SDFM0_SDCOMP1EVT2FLTCTL Register (Offset = C2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter1 Control Register

Long Description:

Return to Summary Table

Table 3-2949. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C2h
CONTROLSS_SDFM1	5026 90C2h

Figure 3-1446. CONTROLSS_SDFM0_SDCOMP1EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2950. SDCOMP1EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.63 CONTROLSS_SDFM0_SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter1 Clock Control Register

Long Description:

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Table 3-2951. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C4h
CONTROLSS_SDFM1	5026 90C4h

Figure 3-1447. CONTROLSS_SDFM0_SDCOMP1EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2952. SDCOMP1EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

3.19.64 CONTROLSS_SDFM0_SDCOMP1EVT1FLTCTL Register (Offset = C6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter1 Control Register

Long Description:

Return to Summary Table

Table 3-2953. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C6h
CONTROLSS_SDFM1	5026 90C6h

Figure 3-1448. CONTROLSS_SDFM0_SDCOMP1EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2954. SDCOMP1EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.65 CONTROLSS_SDFM0_SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter1 Clock Control Register

Long Description:

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Table 3-2955. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C8h
CONTROLSS_SDFM1	5026 90C8h

Figure 3-1449. CONTROLSS_SDFM0_SDCOMP1EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2956. SDCOMP1EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

3.19.66 CONTROLSS_SDFM0_SDCOMP1LOCK Register (Offset = CEh) [reset = h]

Short Description: SD compartor event filter1 Lock Register

Long Description:

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Table 3-2957. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80CEh
CONTROLSS_SDFM1	5026 90CEh

Figure 3-1450. CONTROLSS_SDFM0_SDCOMP1LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP1CTL
RO			RO	RW SONCE	RO	RO	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-2958. SDCOMP1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP1EVT1/2FLTTCTL and COMP1FILCLKCTL registers. 0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP1CTL	RW SONCE	0h	Lock write-access to the SDCOMP1CTL register. 0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP1CTL register is locked. Only a system reset can clear this bit.

3.19.67 CONTROLSS_SDFM0_SDCOMP2CTL Register (Offset = D0h) [reset = h]

Short Description: SD Comparator event filter2 Control Register

Long Description:

Return to Summary Table

Table 3-2959. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D0h
CONTROLSS_SDFM1	5026 90D0h

Figure 3-1451. CONTROLSS_SDFM0_SDCOMP2CTL Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0

Access Types Legend

Table 3-2960. SDCOMP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

3.19.68 CONTROLSS_SDFM0_SDCOMP2EVT2FLTCTL Register (Offset = D2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter2 Control Register

Long Description:

Return to Summary Table

Table 3-2961. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D2h
CONTROLSS_SDFM1	5026 90D2h

Figure 3-1452. CONTROLSS_SDFM0_SDCOMP2EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2962. SDCOMP2EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.69 CONTROLSS_SDFM0_SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter2 Clock Control Register

Long Description:

Return to Summary Table

Table 3-2963. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D4h
CONTROLSS_SDFM1	5026 90D4h

Figure 3-1453. CONTROLSS_SDFM0_SDCOMP2EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2964. SDCOMP2EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

3.19.70 CONTROLSS_SDFM0_SDCOMP2EVT1FLTCTL Register (Offset = D6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter2 Control Register

Long Description:

Return to Summary Table

Table 3-2965. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D6h
CONTROLSS_SDFM1	5026 90D6h

Figure 3-1454. CONTROLSS_SDFM0_SDCOMP2EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2966. SDCOMP2EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.71 CONTROLSS_SDFM0_SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter2 Clock Control Register

Long Description:

Return to Summary Table

Table 3-2967. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D8h
CONTROLSS_SDFM1	5026 90D8h

Figure 3-1455. CONTROLSS_SDFM0_SDCOMP2EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2968. SDCOMP2EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

3.19.72 CONTROLSS_SDFM0_SDCOMP2LOCK Register (Offset = DEh) [reset = h]

Short Description: SD compartor event filter2 Lock Register

Long Description:

Return to Summary Table

Table 3-2969. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80DEh
CONTROLSS_SDFM1	5026 90DEh

Figure 3-1456. CONTROLSS_SDFM0_SDCOMP2LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP2CTL
RO			RO	RW SONCE	RO	RO	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-2970. SDCOMP2LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP2EVT1/2FLTTCTL and COMP2FILCLKCTL registers. 0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP2CTL	RW SONCE	0h	Lock write-access to the SDCOMP2CTL register. 0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP2CTL register is locked. Only a system reset can clear this bit.

3.19.73 CONTROLSS_SDFM0_SDCOMP3CTL Register (Offset = E0h) [reset = h]

Short Description: SD Comparator event filter3 Control Register

Long Description:

Return to Summary Table

Table 3-2971. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E0h
CONTROLSS_SDFM1	5026 90E0h

Figure 3-1457. CONTROLSS_SDFM0_SDCOMP3CTL Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0

Access Types Legend

Table 3-2972. SDCOMP3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

3.19.74 CONTROLSS_SDFM0_SDCOMP3EVT2FLTCTL Register (Offset = E2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter3 Control Register

Long Description:

Return to Summary Table

Table 3-2973. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E2h
CONTROLSS_SDFM1	5026 90E2h

Figure 3-1458. CONTROLSS_SDFM0_SDCOMP3EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2974. SDCOMP3EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.75 CONTROLSS_SDFM0_SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter3 Clock Control Register

Long Description:

Return to Summary Table

Table 3-2975. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E4h
CONTROLSS_SDFM1	5026 90E4h

Figure 3-1459. CONTROLSS_SDFM0_SDCOMP3EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2976. SDCOMP3EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

3.19.76 CONTROLSS_SDFM0_SDCOMP3EVT1FLTCTL Register (Offset = E6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter3 Control Register

Long Description:

Return to Summary Table

Table 3-2977. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E6h
CONTROLSS_SDFM1	5026 90E6h

Figure 3-1460. CONTROLSS_SDFM0_SDCOMP3EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2978. SDCOMP3EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.77 CONTROLSS_SDFM0_SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter3 Clock Control Register

Long Description:

Return to Summary Table

Table 3-2979. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E8h
CONTROLSS_SDFM1	5026 90E8h

Figure 3-1461. CONTROLSS_SDFM0_SDCOMP3EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2980. SDCOMP3EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

3.19.78 CONTROLSS_SDFM0_SDCOMP3LOCK Register (Offset = EEh) [reset = h]

Short Description: SD compartor event filter3 Lock Register

Long Description:

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Table 3-2981. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80EEh
CONTROLSS_SDFM1	5026 90EEh

Figure 3-1462. CONTROLSS_SDFM0_SDCOMP3LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP3CTL
RO			RO	RW SONCE	RO	RO	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-2982. SDCOMP3LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP3EVT1/2FLTTCTL and COMP3FILCLKCTL registers. 0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP3CTL	RW SONCE	0h	Lock write-access to the SDCOMP3CTL register. 0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP3CTL register is locked. Only a system reset can clear this bit.

3.19.79 CONTROLSS_SDFM0_SDCOMP4CTL Register (Offset = F0h) [reset = h]

Short Description: SD Comparator event filter4 Control Register

Long Description:

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Table 3-2983. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F0h
CONTROLSS_SDFM1	5026 90F0h

Figure 3-1463. CONTROLSS_SDFM0_SDCOMP4CTL Name Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
RO	RO	RO		RW		RO	RO
0	0	0		0		0	0

Access Types Legend

Table 3-2984. SDCOMP4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

3.19.80 CONTROLSS_SDFM0_SDCOMP4EVT2FLTCTL Register (Offset = F2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter4 Control Register

Long Description:

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Table 3-2985. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F2h
CONTROLSS_SDFM1	5026 90F2h

Figure 3-1464. CONTROLSS_SDFM0_SDCOMP4EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2986. SDCOMP4EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.81 CONTROLSS_SDFM0_SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter4 Clock Control Register

Long Description:

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Table 3-2987. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F4h
CONTROLSS_SDFM1	5026 90F4h

Figure 3-1465. CONTROLSS_SDFM0_SDCOMP4EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2988. SDCOMP4EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

3.19.82 CONTROLSS_SDFM0_SDCOMP4EVT1FLTCTL Register (Offset = F6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter4 Control Register

Long Description:

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Table 3-2989. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F6h
CONTROLSS_SDFM1	5026 90F6h

Figure 3-1466. CONTROLSS_SDFM0_SDCOMP4EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
RW RRETURNS0S	RO	RW					RW
0	0	0					0
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
RW				RO			
0				0			

Access Types Legend

Table 3-2990. SDCOMP4EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

3.19.83 CONTROLSS_SDFM0_SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter4 Clock Control Register

Long Description:

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Table 3-2991. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F8h
CONTROLSS_SDFM1	5026 90F8h

Figure 3-1467. CONTROLSS_SDFM0_SDCOMP4EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
RO						RW	
0						0	
7	6	5	4	3	2	1	0
CLKPRESCALE							
RW							
0							

Access Types Legend

Table 3-2992. SDCOMP4EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

3.19.84 CONTROLSS_SDFM0_SDCOMP4LOCK Register (Offset = FEh) [reset = h]

Short Description: SD compartor event filter4 Lock Register

Long Description:

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Table 3-2993. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80FEh
CONTROLSS_SDFM1	5026 90FEh

Figure 3-1468. CONTROLSS_SDFM0_SDCOMP4LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED							
RO							
0							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP4CTL
RO			RO	RW SONCE	RO	RO	RW SONCE
0			0	0	0	0	0

Access Types Legend

Table 3-2994. SDCOMP4LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP4EVT1/2FLTTCTL and COMP4FILCLKCTL registers. 0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP4CTL	RW SONCE	0h	Lock write-access to the SDCOMP4CTL register. 0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP4CTL register is locked. Only a system reset can clear this bit.

3.19.85 CONTROLSS_SDFM1_SDIFLG Register (Offset = 0h) [reset = h]

Short Description: SD Interrupt Flag Register

Long Description:

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Table 3-2995. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8000h
CONTROLSS_SDFM1	5026 9000h

Figure 3-1469. CONTROLSS_SDFM1_SDIFLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIF	RESERVED							SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
RO	RO RRETURNS0S							RO	RO	RO	RO	RO	RO	RO	RO
0	0							0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1	FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 3-2996. SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	RO	0h	Set whenever any "error" interrupt (MF1-4,IFL1-4,IFH1-4,SDFFOVF1-4) is active
30 - 24	RESERVED	RO RRETURNS 0S		Reserved
23	SDFFINT4	RO	0h	SDFIFO data ready interrupt for Ch4
22	SDFFINT3	RO	0h	SDFIFO data ready interrupt for Ch3
21	SDFFINT2	RO	0h	SDFIFO data ready interrupt for Ch2
20	SDFFINT1	RO	0h	SDFIFO data ready interrupt for Ch1 0: SDFIFO data ready interrupt has NOT occurred 1: SDFIFO data ready interrupt has occurred
19	SDFFOVF4	RO	0h	FIFO Overflow Flag for Ch4
18	SDFFOVF3	RO	0h	FIFO Overflow Flag for Ch3
17	SDFFOVF2	RO	0h	FIFO Overflow Flag for Ch2
16	SDFFOVF1	RO	0h	FIFO Overflow Flag for Ch1 0 - FIFO has not overflowed 1 - FIFO overflowed. # words received in FIFO ' FIFO depth (16), NEW word is lost
15	AF4	RO	0h	Acknowledge flag for Filter 4 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
14	AF3	RO	0h	Acknowledge flag for Filter 3 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
13	AF2	RO	0h	Acknowledge flag for Filter 2 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
12	AF1	RO	0h	Acknowledge flag for Filter 1 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
11	MF4	RO	0h	Modulator Failure for Filter 4 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
10	MF3	RO	0h	Modulator Failure for Filter 3 0: Modulator is operating normally for Filter 1: Modulator failure for Filter

Table 3-2996. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MF2	RO	0h	Modulator Failure for Filter 2 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
8	MF1	RO	0h	Modulator Failure for Filter 1 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
7	FLT4_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter4 0: CEVT2 event has not occured 1: CEVT2 event has occurred
6	FLT4_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter4 0: CEVT1 event has not occured 1: CEVT1 event has occurred
5	FLT3_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter3 0: CEVT2 event has not occured 1: CEVT2 event has occurred
4	FLT3_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter3 0: CEVT1 event has not occured 1: CEVT1 event has occurred
3	FLT2_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter2 0: CEVT2 event has not occured 1: CEVT2 event has occurred
2	FLT2_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter2 0: CEVT1 event has not occured 1: CEVT1 event has occurred
1	FLT1_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter1 0: CEVT2 event has not occured 1: CEVT2 event has occurred
0	FLT1_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter1 0: CEVT1 event has not occured 1: CEVT1 event has occurred

Table 3-2997. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RO RRETURNS0S	RO RRETURNS0S	Undefined
RW RRETURNS0S	RW RRETURNS0S	Undefined
RW	RW	Undefined
RW SONCE	RW SONCE	Undefined

3.20 C2K_TSXBAR_INTR Registers

Table 3-2998. SOC_TIMESYNC_XBAR0, SOC_TIMESYNC_XBAR0_SOC_TIMESYNC_XBAR Registers, Base Address=52E0 0000H, Length=5

Offset	Length	Acronym	Register Name	SOC_TIMESYNC_XBAR0 Physical Address
0h	32	SOC_TIMESYNC_XBAR0_PID	Identification register	52E0 0000h
4h	16	SOC_TIMESYNC_XBAR0_MUXCNTL	Interrupt mux control register	52E0 0004h

3.20.1 SOC_TIMESYNC_XBAR0_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

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Table 3-2999. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0000h

Figure 3-1470. SOC_TIMESYNC_XBAR0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
RO		RO		RO											
1		10		11010010100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
RO					RO			RO		RO					
10000					1			0		0					

Access Types Legend

Table 3-3000. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	Ah	bu
27 - 16	FUNCTION	RO	2903F6BF4h	function
15 - 11	RTLVER	RO	2710h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

3.20.2 SOC_TIMESYNC_XBAR0_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

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Table 3-3001. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0004h

Figure 3-1471. SOC_TIMESYNC_XBAR0_MUXCNTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0							
7	6	5	4	3	2	1	0
RESERVED			ENABLE				
NONE			RW				
0			0				

Access Types Legend

Table 3-3002. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
4 - 0	ENABLE	RW	0h	Mux control for interrupt N

Table 3-3003. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4 AM263x SoC Registers

The AM263x SoC module registers are described below.

4.1 EDMA_TRIGXBAR_INTR Registers

Table 4-1. EDMA_TRIG_XBAR, EDMA_TRIG_XBAR_EDMA_TRIG_XBAR Registers, Base Address=52E0 1000H, Length=2

Offset	Length	Acronym	Register Name	EDMA_TRIG_XBAR Physical Address
0h	32	EDMA_TRIG_XBAR_PID	Identification register	52E0 1000h
4h	16	EDMA_TRIG_XBAR_MUXCNTL	Interrupt mux control register	52E0 1004h

4.1.1 EDMA_TRIG_XBAR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

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Table 4-2. Instance Table

Instance Name	Physical Address
EDMA_TRIG_XBAR	52E0 1000h

Figure 4-1. EDMA_TRIG_XBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
RO		RO		RO											
1		10		11010010100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
RO					RO			RO		RO					
10000					1			0		0					

Access Types Legend

Table 4-3. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	Ah	bu
27 - 16	FUNCTION	RO	2903F6BF4h	function
15 - 11	RTLVER	RO	2710h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.1.2 EDMA_TRIG_XBAR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

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Table 4-4. Instance Table

Instance Name	Physical Address
EDMA_TRIG_XBAR	52E0 1004h

Figure 4-2. EDMA_TRIG_XBAR_MUXCNTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0							
7	6	5	4	3	2	1	0
ENABLE							
RW							
0							

Access Types Legend

Table 4-5. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
7 - 0	ENABLE	RW	0h	Mux control for interrupt N

Table 4-6. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.2 EXT_FLASH Registers

Table 4-7. EXT_FLASH0, EXT_FLASH0_EXT_FLASH Registers, Base Address=6000 0000H, Length=3

Offset	Length	Acronym	Register Name	EXT_FLASH0 Physical Address	EXT_FLASH1 Physical Address
0h	32	EXT_FLASH0_EXT_FLASH_START	RW	6000 0000h	6200 0000h
1FFFFFCh	32	EXT_FLASH0_EXT_FLASH_END	RW	61FF FFFCh	63FF FFFCh

Table 4-8. EXT_FLASH1, EXT_FLASH1_EXT_FLASH Registers, Base Address=6200 0000H, Length=3

Offset	Length	Acronym	Register Name	EXT_FLASH0 Physical Address	EXT_FLASH1 Physical Address
0h	32	EXT_FLASH1_EXT_FLASH_START	RW	6000 0000h	6200 0000h
1FFFFFCh	32	EXT_FLASH1_EXT_FLASH_END	RW	61FF FFFCh	63FF FFFCh

4.2.1 EXT_FLASH0_EXT_FLASH_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-9. Instance Table

Instance Name	Physical Address
EXT_FLASH0	6000 0000h
EXT_FLASH1	6200 0000h

Figure 4-3. EXT_FLASH0_EXT_FLASH_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_START															
RW															
0															

Access Types Legend

Table 4-10. EXT_FLASH_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_START	RW	0h	External flash start Address

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4.2.2 EXT_FLASH0_EXT_FLASH_END Register (Offset = 1FFFFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-11. Instance Table

Instance Name	Physical Address
EXT_FLASH0	61FF FFFCh
EXT_FLASH1	63FF FFFCh

Figure 4-4. EXT_FLASH0_EXT_FLASH_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_END															
RW															
0															

Access Types Legend

Table 4-12. EXT_FLASH_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_END	RW	0h	External flash end address

4.2.3 EXT_FLASH1_EXT_FLASH_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-13. Instance Table

Instance Name	Physical Address
EXT_FLASH0	6000 0000h
EXT_FLASH1	6200 0000h

Figure 4-5. EXT_FLASH1_EXT_FLASH_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_START															
RW															
0															

Access Types Legend

Table 4-14. EXT_FLASH_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_START	RW	0h	External flash start Address

4.2.4 EXT_FLASH1_EXT_FLASH_END Register (Offset = 1FFFFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-15. Instance Table

Instance Name	Physical Address
EXT_FLASH0	61FF FFFCh
EXT_FLASH1	63FF FFFCh

Figure 4-6. EXT_FLASH1_EXT_FLASH_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MEM_END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_END															
RW															
0															

Access Types Legend

Table 4-16. EXT_FLASH_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_END	RW	0h	External flash end address

Table 4-17. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.3 GPIO_XBAR_INTR Registers

Table 4-18. GPIO_INTR_XBAR, GPIO_INTR_XBAR_GPIO_INTR_XBAR Registers, Base Address=52E0 2000H, Length=1

Offset	Length	Acronym	Register Name	GPIO_INTR_XBAR Physical Address
0h	32	GPIO_INTR_XBAR_PID	Identification register	52E0 2000h
4h	16	GPIO_INTR_XBAR_MUXCNTL	Interrupt mux control register	52E0 2004h

4.3.1 GPIO_INTR_XBAR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

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Table 4-19. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2000h

Figure 4-7. GPIO_INTR_XBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
RO		RO		RO											
1		10		11010010100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER				MAJREV				CUSTOM		MINREV					
RO				RO				RO		RO					
10000				1				0		0					

Access Types Legend

Table 4-20. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	Ah	bu
27 - 16	FUNCTION	RO	2903F6BF4h	function
15 - 11	RTLVER	RO	2710h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.3.2 GPIO_INTR_XBAR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

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Table 4-21. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2004h

Figure 4-8. GPIO_INTR_XBAR_MUXCNTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0							
7	6	5	4	3	2	1	0
ENABLE							
RW							
0							

Access Types Legend

Table 4-22. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
7 - 0	ENABLE	RW	0h	Mux control for interrupt N

Table 4-23. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.4 ICSSM_XBAR_INTR Registers

Table 4-24. ICSSM_INTR_XBAR, ICSSM_INTR_XBAR_ICSSM_INTR_XBAR Registers, Base Address=52E0 3000H, Length=6

Offset	Length	Acronym	Register Name	ICSSM_INTR_XBAR Physical Address
0h	32	ICSSM_INTR_XBAR_PID	Identification register	52E0 3000h
4h	16	ICSSM_INTR_XBAR_MUXCNTL	Interrupt mux control register	52E0 3004h

4.4.1 ICSSM_INTR_XBAR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

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Table 4-25. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3000h

Figure 4-9. ICSSM_INTR_XBAR_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
RO		RO		RO											
1		10		11010010100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
RO					RO			RO		RO					
10000					1			0		0					

Access Types Legend

Table 4-26. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	Ah	bu
27 - 16	FUNCTION	RO	2903F6BF4h	function
15 - 11	RTLVER	RO	2710h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.4.2 ICSSM_INTR_XBAR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

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Table 4-27. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3004h

Figure 4-10. ICSSM_INTR_XBAR_MUXCNTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0							
7	6	5	4	3	2	1	0
RESERVED		ENABLE					
NONE		RW					
0		0					

Access Types Legend

Table 4-28. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
5 - 0	ENABLE	RW	0h	Mux control for interrupt N

Table 4-29. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.5 MSS_CCMR Registers

Table 4-30. R5SS0_CCMR, R5SS0_CCMR_R5SS0_CCMR Registers, Base Address=5321 0000H, Length=2

Offset	Length	Acronym	Register Name	R5SS0_CCMR Physical Address
0h	32	R5SS0_CCMR_CCMSR1	CPU Compare Status Register	5321 0000h
4h	32	R5SS0_CCMR_CCMKEYR1	CPU Compare Key Register	5321 0004h
8h	32	R5SS0_CCMR_CCMSR2	VIM Compare Status Register	5321 0008h
Ch	32	R5SS0_CCMR_CCMKEYR2	VIM Compare Key Register	5321 000Ch
10h	32	R5SS0_CCMR_CCMSR3	Inactivity Monitor Status Register	5321 0010h
14h	32	R5SS0_CCMR_CCMKEYR3	Inactivity Monitor Key Register	5321 0014h
18h	32	R5SS0_CCMR_CCMPOLCNTRL	CPU Compare Polarity Control Register	5321 0018h

Table 4-31. R5SS0_CCMR, R5SS0_CCMR_R5SS0_CCMR Registers, Base Address=5321 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	R5SS0_CCMR_CCMSR1	CPU Compare Status Register
4h	32	R5SS0_CCMR_CCMKEYR1	CPU Compare Key Register
8h	32	R5SS0_CCMR_CCMSR2	VIM Compare Status Register
Ch	32	R5SS0_CCMR_CCMKEYR2	VIM Compare Key Register
10h	32	R5SS0_CCMR_CCMSR3	Inactivity Monitor Status Register
14h	32	R5SS0_CCMR_CCMKEYR3	Inactivity Monitor Key Register
18h	32	R5SS0_CCMR_CCMPOLCNTRL	CPU Compare Polarity Control Register

Table 4-32. R5SS1_CCMR, R5SS1_CCMR_R5SS1_CCMR Registers, Base Address=5321 1000H, Length=2

Offset	Length	Acronym	Register Name	R5SS1_CCMR Physical Address
0h	32	R5SS1_CCMR_CCMSR1	CPU Compare Status Register	5321 1000h
4h	32	R5SS1_CCMR_CCMKEYR1	CPU Compare Key Register	5321 1004h
8h	32	R5SS1_CCMR_CCMSR2	VIM Compare Status Register	5321 1008h
Ch	32	R5SS1_CCMR_CCMKEYR2	VIM Compare Key Register	5321 100Ch
10h	32	R5SS1_CCMR_CCMSR3	Inactivity Monitor Status Register	5321 1010h
14h	32	R5SS1_CCMR_CCMKEYR3	Inactivity Monitor Key Register	5321 1014h
18h	32	R5SS1_CCMR_CCMPOLCNTRL	CPU Compare Polarity Control Register	5321 1018h

Table 4-33. R5SS1_CCMR, R5SS1_CCMR_R5SS1_CCMR Registers, Base Address=5321 1000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	R5SS1_CCMR_CCMSR1	CPU Compare Status Register
4h	32	R5SS1_CCMR_CCMKEYR1	CPU Compare Key Register
8h	32	R5SS1_CCMR_CCMSR2	VIM Compare Status Register
Ch	32	R5SS1_CCMR_CCMKEYR2	VIM Compare Key Register

Table 4-33. R5SS1_CCMR, R5SS1_CCMR_R5SS1_CCMR Registers, Base Address=5321 1000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
10h	32	R5SS1_CCMR_CCMSR3	Inactivity Monitor Status Register
14h	32	R5SS1_CCMR_CCMKEYR3	Inactivity Monitor Key Register
18h	32	R5SS1_CCMR_CCMPOLCNTRL	CPU Compare Polarity Control Register

Table 4-34. TOP_PBIST, TOP_PBIST_TOP_PBIST Registers, Base Address=5330 0000H, Length=4

Offset	Length	Acronym	Register Name	TOP_PBIST Physical Address
100h	16	TOP_PBIST_PBIST_A0	Variable Address Register0	5330 0100h
104h	16	TOP_PBIST_PBIST_A1	Variable Address Register1	5330 0104h
108h	32	TOP_PBIST_PBIST_A2	Variable Address Register2	5330 0108h
10Ch	16	TOP_PBIST_PBIST_A3	Variable Address Register3	5330 010Ch
110h	8	TOP_PBIST_PBIST_L0	Variable Loop Count Register L0	5330 0110h
114h	8	TOP_PBIST_PBIST_L1	Variable Loop Count Register L1	5330 0114h
118h	32	TOP_PBIST_PBIST_L2	Variable Loop Count Register L2	5330 0118h
11Ch	32	TOP_PBIST_PBIST_L3	Variable Loop Count Register L3	5330 011Ch
120h	32	TOP_PBIST_PBIST_DD10	DD0 Data Register 16 (D0)	5330 0120h
124h	8	TOP_PBIST_PBIST_DE10	DE0 Data Register 16 (D0)	5330 0124h
130h	0	TOP_PBIST_PBIST_CA0	Constant Address Register0	5330 0130h
134h	8	TOP_PBIST_PBIST_CA1	Constant Address Register1	5330 0134h
138h	0	TOP_PBIST_PBIST_CA2	Constant Address Register2	5330 0138h
13Ch	0	TOP_PBIST_PBIST_CA3	Constant Address Register3	5330 013Ch
140h	8	TOP_PBIST_PBIST_CL0	Constant Loop Count Register0	5330 0140h
144h	8	TOP_PBIST_PBIST_CL1	Constant Loop Count Register1	5330 0144h
148h	16	TOP_PBIST_PBIST_CL2	Constant Loop Count Register2	5330 0148h
14Ch	32	TOP_PBIST_PBIST_CL3	Constant Loop Count Register3	5330 014Ch
150h	32	TOP_PBIST_PBIST_CI0	Constant Increment Register0	5330 0150h
154h	8	TOP_PBIST_PBIST_CI1	Constant Increment Register1	5330 0154h
158h	32	TOP_PBIST_PBIST_CI2	Constant Increment Register2	5330 0158h
15Ch	32	TOP_PBIST_PBIST_CI3	Constant Increment Register3	5330 015Ch
160h	32	TOP_PBIST_PBIST_RAMT	RAM Configuration (RAMT -RAM)	5330 0160h

Table 4-35. TOP_PBIST, TOP_PBIST_TOP_PBIST Registers, Base Address=5330 0000H, Length=4

Offset	Length	Acronym	Register Name
100h	16	TOP_PBIST_PBIST_A0	Variable Address Register0
104h	16	TOP_PBIST_PBIST_A1	Variable Address Register1
108h	32	TOP_PBIST_PBIST_A2	Variable Address Register2
10Ch	16	TOP_PBIST_PBIST_A3	Variable Address Register3
110h	8	TOP_PBIST_PBIST_L0	Variable Loop Count Register L0
114h	8	TOP_PBIST_PBIST_L1	Variable Loop Count Register L1
118h	32	TOP_PBIST_PBIST_L2	Variable Loop Count Register L2
11Ch	32	TOP_PBIST_PBIST_L3	Variable Loop Count Register L3
120h	32	TOP_PBIST_PBIST_DD10	DD0 Data Register 16 (D0)
124h	8	TOP_PBIST_PBIST_DE10	DE0 Data Register 16 (D0)
130h	0	TOP_PBIST_PBIST_CA0	Constant Address Register0
134h	8	TOP_PBIST_PBIST_CA1	Constant Address Register1

Table 4-35. TOP_PBIST, TOP_PBIST_TOP_PBIST Registers, Base Address=5330 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
138h	0	TOP_PBIST_PBIST_CA2	Constant Address Register2
13Ch	0	TOP_PBIST_PBIST_CA3	Constant Address Register3
140h	8	TOP_PBIST_PBIST_CL0	Constant Loop Count Register0
144h	8	TOP_PBIST_PBIST_CL1	Constant Loop Count Register1
148h	16	TOP_PBIST_PBIST_CL2	Constant Loop Count Register2
14Ch	32	TOP_PBIST_PBIST_CL3	Constant Loop Count Register3
150h	32	TOP_PBIST_PBIST_CI0	Constant Increment Register0
154h	8	TOP_PBIST_PBIST_CI1	Constant Increment Register1
158h	32	TOP_PBIST_PBIST_CI2	Constant Increment Register2
15Ch	32	TOP_PBIST_PBIST_CI3	Constant Increment Register3
160h	32	TOP_PBIST_PBIST_RAMT	RAM Configuration (RAMT -RAM)

Table 4-36. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2

Offset	Length	Acronym	Register Name	R5SS0_STC Physical Address
0h	32	R5SS0_STC_STCGCR0	Self test Global control Reg0. *NOT BYTE ACCESSIBLE	5350 0000h
4h	32	R5SS0_STC_STCGCR1	Self test Global control Reg1	5350 0004h
8h	32	R5SS0_STC_STCTPR	Time out counter preload register	5350 0008h
Ch	32	R5SS0_STC_STC_CADDR	Current Address register for CORE1	5350 000Ch
10h	32	R5SS0_STC_STCCICR	Current Interval count register	5350 0010h
14h	32	R5SS0_STC_STCGSTAT	Global Status Register	5350 0014h
18h	32	R5SS0_STC_STCFSTAT	Fail Status Register	5350 0018h
1Ch	32	R5SS0_STC_STCSCSCR	Signature compare Self Check Register	5350 001Ch
20h	32	R5SS0_STC_STC_CADDR2	Current Address register for CORE2	5350 0020h
24h	32	R5SS0_STC_STC_CLKDIV	Clock Divider Register	5350 0024h
28h	32	R5SS0_STC_STC_SEGPLR	Segment 1st interval Preload Register	5350 0028h
2Ch	32	R5SS0_STC_SEG0_START_ADDR	ROM Start address for Segment0	5350 002Ch
30h	32	R5SS0_STC_SEG1_START_ADDR	ROM Start address for Segment1	5350 0030h
34h	32	R5SS0_STC_SEG2_START_ADDR	ROM Start address for Segment2	5350 0034h
38h	32	R5SS0_STC_SEG3_START_ADDR	ROM Start address for Segment3	5350 0038h
3Ch	32	R5SS0_STC_CORE1_CURMISR_0	Holds the MISR signature for CORE1	5350 003Ch
40h	32	R5SS0_STC_CORE1_CURMISR_1	Holds the MISR signature for CORE1	5350 0040h
44h	32	R5SS0_STC_CORE1_CURMISR_2	Holds the MISR signature for CORE1	5350 0044h
48h	32	R5SS0_STC_CORE1_CURMISR_3	Holds the MISR signature for CORE1	5350 0048h
4Ch	32	R5SS0_STC_CORE1_CURMISR_4	Holds the MISR signature for CORE1	5350 004Ch
50h	32	R5SS0_STC_CORE1_CURMISR_5	Holds the MISR signature for CORE1	5350 0050h
54h	32	R5SS0_STC_CORE1_CURMISR_6	Holds the MISR signature for CORE1	5350 0054h
58h	32	R5SS0_STC_CORE1_CURMISR_7	Holds the MISR signature for CORE1	5350 0058h

Table 4-36. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	R5SS0_STC Physical Address
5Ch	32	R5SS0_STC_CORE1_CURMISR_8	Holds the MISR signature for CORE1	5350 005Ch
60h	32	R5SS0_STC_CORE1_CURMISR_9	Holds the MISR signature for CORE1	5350 0060h
64h	32	R5SS0_STC_CORE1_CURMISR_10	Holds the MISR signature for CORE1	5350 0064h
68h	32	R5SS0_STC_CORE1_CURMISR_11	Holds the MISR signature for CORE1	5350 0068h
6Ch	32	R5SS0_STC_CORE1_CURMISR_12	Holds the MISR signature for CORE1	5350 006Ch
70h	32	R5SS0_STC_CORE1_CURMISR_13	Holds the MISR signature for CORE1	5350 0070h
74h	32	R5SS0_STC_CORE1_CURMISR_14	Holds the MISR signature for CORE1	5350 0074h
78h	32	R5SS0_STC_CORE1_CURMISR_15	Holds the MISR signature for CORE1	5350 0078h
7Ch	32	R5SS0_STC_CORE1_CURMISR_16	Holds the MISR signature for CORE1	5350 007Ch
80h	32	R5SS0_STC_CORE1_CURMISR_17	Holds the MISR signature for CORE1	5350 0080h
84h	32	R5SS0_STC_CORE1_CURMISR_18	Holds the MISR signature for CORE1	5350 0084h
88h	32	R5SS0_STC_CORE1_CURMISR_19	Holds the MISR signature for CORE1	5350 0088h
8Ch	32	R5SS0_STC_CORE1_CURMISR_20	Holds the MISR signature for CORE1	5350 008Ch
90h	32	R5SS0_STC_CORE1_CURMISR_21	Holds the MISR signature for CORE1	5350 0090h
94h	32	R5SS0_STC_CORE1_CURMISR_22	Holds the MISR signature for CORE1	5350 0094h
98h	32	R5SS0_STC_CORE1_CURMISR_23	Holds the MISR signature for CORE1	5350 0098h
9Ch	32	R5SS0_STC_CORE1_CURMISR_24	Holds the MISR signature for CORE1	5350 009Ch
A0h	32	R5SS0_STC_CORE1_CURMISR_25	Holds the MISR signature for CORE1	5350 00A0h
A4h	32	R5SS0_STC_CORE1_CURMISR_26	Holds the MISR signature for CORE1	5350 00A4h
A8h	32	R5SS0_STC_CORE1_CURMISR_27	Holds the MISR signature for CORE1	5350 00A8h
ACh	32	R5SS0_STC_CORE2_CURMISR_0	Holds the MISR signature for CORE2	5350 00ACh
B0h	32	R5SS0_STC_CORE2_CURMISR_1	Holds the MISR signature for CORE2	5350 00B0h
B4h	32	R5SS0_STC_CORE2_CURMISR_2	Holds the MISR signature for CORE2	5350 00B4h
B8h	32	R5SS0_STC_CORE2_CURMISR_3	Holds the MISR signature for CORE2	5350 00B8h
BCh	32	R5SS0_STC_CORE2_CURMISR_4	Holds the MISR signature for CORE2	5350 00BCh
C0h	32	R5SS0_STC_CORE2_CURMISR_5	Holds the MISR signature for CORE2	5350 00C0h
C4h	32	R5SS0_STC_CORE2_CURMISR_6	Holds the MISR signature for CORE2	5350 00C4h

Table 4-36. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	R5SS0_STC Physical Address
C8h	32	R5SS0_STC_CORE2_CURMISR_7	Holds the MISR signature for CORE2	5350 00C8h
CCh	32	R5SS0_STC_CORE2_CURMISR_8	Holds the MISR signature for CORE2	5350 00CCh
D0h	32	R5SS0_STC_CORE2_CURMISR_9	Holds the MISR signature for CORE2	5350 00D0h
D4h	32	R5SS0_STC_CORE2_CURMISR_10	Holds the MISR signature for CORE2	5350 00D4h
D8h	32	R5SS0_STC_CORE2_CURMISR_11	Holds the MISR signature for CORE2	5350 00D8h
DCh	32	R5SS0_STC_CORE2_CURMISR_12	Holds the MISR signature for CORE2	5350 00DCh
E0h	32	R5SS0_STC_CORE2_CURMISR_13	Holds the MISR signature for CORE2	5350 00E0h
E4h	32	R5SS0_STC_CORE2_CURMISR_14	Holds the MISR signature for CORE2	5350 00E4h
E8h	32	R5SS0_STC_CORE2_CURMISR_15	Holds the MISR signature for CORE2	5350 00E8h
ECh	32	R5SS0_STC_CORE2_CURMISR_16	Holds the MISR signature for CORE2	5350 00ECh
F0h	32	R5SS0_STC_CORE2_CURMISR_17	Holds the MISR signature for CORE2	5350 00F0h
F4h	32	R5SS0_STC_CORE2_CURMISR_18	Holds the MISR signature for CORE2	5350 00F4h
F8h	32	R5SS0_STC_CORE2_CURMISR_19	Holds the MISR signature for CORE2	5350 00F8h
FCh	32	R5SS0_STC_CORE2_CURMISR_20	Holds the MISR signature for CORE2	5350 00FCh
100h	32	R5SS0_STC_CORE2_CURMISR_21	Holds the MISR signature for CORE2	5350 0100h
104h	32	R5SS0_STC_CORE2_CURMISR_22	Holds the MISR signature for CORE2	5350 0104h
108h	32	R5SS0_STC_CORE2_CURMISR_23	Holds the MISR signature for CORE2	5350 0108h
10Ch	32	R5SS0_STC_CORE2_CURMISR_24	Holds the MISR signature for CORE2	5350 010Ch
110h	32	R5SS0_STC_CORE2_CURMISR_25	Holds the MISR signature for CORE2	5350 0110h
114h	32	R5SS0_STC_CORE2_CURMISR_26	Holds the MISR signature for CORE2	5350 0114h
118h	32	R5SS0_STC_CORE2_CURMISR_27	Holds the MISR signature for CORE2	5350 0118h

Table 4-37. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	R5SS0_STC_STCGCR0	Self test Global control Reg0. *NOT BYTE ACCESSIBLE
4h	32	R5SS0_STC_STCGCR1	Self test Global control Reg1
8h	32	R5SS0_STC_STCTPR	Time out counter preload register
Ch	32	R5SS0_STC_STC_CADDR	Current Address register for CORE1
10h	32	R5SS0_STC_STCCICR	Current Interval count register

Table 4-37. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
14h	32	R5SS0_STC_STCGSTAT	Global Status Register
18h	32	R5SS0_STC_STCFSTAT	Fail Status Register
1Ch	32	R5SS0_STC_STCSCSCR	Signature compare Self Check Register
20h	32	R5SS0_STC_STC_CADDR2	Current Address register for CORE2
24h	32	R5SS0_STC_STC_CLKDIV	Clock Divider Register
28h	32	R5SS0_STC_STC_SEGPLR	Segment 1st interval Preload Register
2Ch	32	R5SS0_STC_SEG0_START_ADDR	ROM Start address for Segment0
30h	32	R5SS0_STC_SEG1_START_ADDR	ROM Start address for Segment1
34h	32	R5SS0_STC_SEG2_START_ADDR	ROM Start address for Segment2
38h	32	R5SS0_STC_SEG3_START_ADDR	ROM Start address for Segment3
3Ch	32	R5SS0_STC_CORE1_CURMISR_0	Holds the MISR signature for CORE1
40h	32	R5SS0_STC_CORE1_CURMISR_1	Holds the MISR signature for CORE1
44h	32	R5SS0_STC_CORE1_CURMISR_2	Holds the MISR signature for CORE1
48h	32	R5SS0_STC_CORE1_CURMISR_3	Holds the MISR signature for CORE1
4Ch	32	R5SS0_STC_CORE1_CURMISR_4	Holds the MISR signature for CORE1
50h	32	R5SS0_STC_CORE1_CURMISR_5	Holds the MISR signature for CORE1
54h	32	R5SS0_STC_CORE1_CURMISR_6	Holds the MISR signature for CORE1
58h	32	R5SS0_STC_CORE1_CURMISR_7	Holds the MISR signature for CORE1
5Ch	32	R5SS0_STC_CORE1_CURMISR_8	Holds the MISR signature for CORE1
60h	32	R5SS0_STC_CORE1_CURMISR_9	Holds the MISR signature for CORE1
64h	32	R5SS0_STC_CORE1_CURMISR_10	Holds the MISR signature for CORE1
68h	32	R5SS0_STC_CORE1_CURMISR_11	Holds the MISR signature for CORE1
6Ch	32	R5SS0_STC_CORE1_CURMISR_12	Holds the MISR signature for CORE1
70h	32	R5SS0_STC_CORE1_CURMISR_13	Holds the MISR signature for CORE1
74h	32	R5SS0_STC_CORE1_CURMISR_14	Holds the MISR signature for CORE1
78h	32	R5SS0_STC_CORE1_CURMISR_15	Holds the MISR signature for CORE1
7Ch	32	R5SS0_STC_CORE1_CURMISR_16	Holds the MISR signature for CORE1
80h	32	R5SS0_STC_CORE1_CURMISR_17	Holds the MISR signature for CORE1
84h	32	R5SS0_STC_CORE1_CURMISR_18	Holds the MISR signature for CORE1
88h	32	R5SS0_STC_CORE1_CURMISR_19	Holds the MISR signature for CORE1

Table 4-37. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
8Ch	32	R5SS0_STC_CORE1_CURMISR_20	Holds the MISR signature for CORE1
90h	32	R5SS0_STC_CORE1_CURMISR_21	Holds the MISR signature for CORE1
94h	32	R5SS0_STC_CORE1_CURMISR_22	Holds the MISR signature for CORE1
98h	32	R5SS0_STC_CORE1_CURMISR_23	Holds the MISR signature for CORE1
9Ch	32	R5SS0_STC_CORE1_CURMISR_24	Holds the MISR signature for CORE1
A0h	32	R5SS0_STC_CORE1_CURMISR_25	Holds the MISR signature for CORE1
A4h	32	R5SS0_STC_CORE1_CURMISR_26	Holds the MISR signature for CORE1
A8h	32	R5SS0_STC_CORE1_CURMISR_27	Holds the MISR signature for CORE1
ACh	32	R5SS0_STC_CORE2_CURMISR_0	Holds the MISR signature for CORE2
B0h	32	R5SS0_STC_CORE2_CURMISR_1	Holds the MISR signature for CORE2
B4h	32	R5SS0_STC_CORE2_CURMISR_2	Holds the MISR signature for CORE2
B8h	32	R5SS0_STC_CORE2_CURMISR_3	Holds the MISR signature for CORE2
BCh	32	R5SS0_STC_CORE2_CURMISR_4	Holds the MISR signature for CORE2
C0h	32	R5SS0_STC_CORE2_CURMISR_5	Holds the MISR signature for CORE2
C4h	32	R5SS0_STC_CORE2_CURMISR_6	Holds the MISR signature for CORE2
C8h	32	R5SS0_STC_CORE2_CURMISR_7	Holds the MISR signature for CORE2
CCh	32	R5SS0_STC_CORE2_CURMISR_8	Holds the MISR signature for CORE2
D0h	32	R5SS0_STC_CORE2_CURMISR_9	Holds the MISR signature for CORE2
D4h	32	R5SS0_STC_CORE2_CURMISR_10	Holds the MISR signature for CORE2
D8h	32	R5SS0_STC_CORE2_CURMISR_11	Holds the MISR signature for CORE2
DCh	32	R5SS0_STC_CORE2_CURMISR_12	Holds the MISR signature for CORE2
E0h	32	R5SS0_STC_CORE2_CURMISR_13	Holds the MISR signature for CORE2
E4h	32	R5SS0_STC_CORE2_CURMISR_14	Holds the MISR signature for CORE2
E8h	32	R5SS0_STC_CORE2_CURMISR_15	Holds the MISR signature for CORE2
ECh	32	R5SS0_STC_CORE2_CURMISR_16	Holds the MISR signature for CORE2
F0h	32	R5SS0_STC_CORE2_CURMISR_17	Holds the MISR signature for CORE2
F4h	32	R5SS0_STC_CORE2_CURMISR_18	Holds the MISR signature for CORE2

Table 4-37. R5SS0_STC, R5SS0_STC_R5SS0_STC Registers, Base Address=5350 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
F8h	32	R5SS0_STC_CORE2_CURMISR_19	Holds the MISR signature for CORE2
FCh	32	R5SS0_STC_CORE2_CURMISR_20	Holds the MISR signature for CORE2
100h	32	R5SS0_STC_CORE2_CURMISR_21	Holds the MISR signature for CORE2
104h	32	R5SS0_STC_CORE2_CURMISR_22	Holds the MISR signature for CORE2
108h	32	R5SS0_STC_CORE2_CURMISR_23	Holds the MISR signature for CORE2
10Ch	32	R5SS0_STC_CORE2_CURMISR_24	Holds the MISR signature for CORE2
110h	32	R5SS0_STC_CORE2_CURMISR_25	Holds the MISR signature for CORE2
114h	32	R5SS0_STC_CORE2_CURMISR_26	Holds the MISR signature for CORE2
118h	32	R5SS0_STC_CORE2_CURMISR_27	Holds the MISR signature for CORE2

Table 4-38. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2

Offset	Length	Acronym	Register Name	R5SS1_STC Physical Address
0h	32	R5SS1_STC_STCGCR0	Self test Global control Reg0. *NOT BYTE ACCESSIBLE	5351 0000h
4h	32	R5SS1_STC_STCGCR1	Self test Global control Reg1	5351 0004h
8h	32	R5SS1_STC_STCTPR	Time out counter preload register	5351 0008h
Ch	32	R5SS1_STC_STC_CADDR	Current Address register for CORE1	5351 000Ch
10h	32	R5SS1_STC_STCCICR	Current Interval count register	5351 0010h
14h	32	R5SS1_STC_STCGSTAT	Global Status Register	5351 0014h
18h	32	R5SS1_STC_STCFSTAT	Fail Status Register	5351 0018h
1Ch	32	R5SS1_STC_STCSCSCR	Signature compare Self Check Register	5351 001Ch
20h	32	R5SS1_STC_STC_CADDR2	Current Address register for CORE2	5351 0020h
24h	32	R5SS1_STC_STC_CLKDIV	Clock Divider Register	5351 0024h
28h	32	R5SS1_STC_STC_SEGPLR	Segment 1st interval Preload Register	5351 0028h
2Ch	32	R5SS1_STC_SEG0_START_ADDR	ROM Start address for Segment0	5351 002Ch
30h	32	R5SS1_STC_SEG1_START_ADDR	ROM Start address for Segment1	5351 0030h
34h	32	R5SS1_STC_SEG2_START_ADDR	ROM Start address for Segment2	5351 0034h
38h	32	R5SS1_STC_SEG3_START_ADDR	ROM Start address for Segment3	5351 0038h
3Ch	32	R5SS1_STC_CORE1_CURMISR_0	Holds the MISR signature for CORE1	5351 003Ch
40h	32	R5SS1_STC_CORE1_CURMISR_1	Holds the MISR signature for CORE1	5351 0040h
44h	32	R5SS1_STC_CORE1_CURMISR_2	Holds the MISR signature for CORE1	5351 0044h
48h	32	R5SS1_STC_CORE1_CURMISR_3	Holds the MISR signature for CORE1	5351 0048h
4Ch	32	R5SS1_STC_CORE1_CURMISR_4	Holds the MISR signature for CORE1	5351 004Ch

Table 4-38. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	R5SS1_STC Physical Address
50h	32	R5SS1_STC_CORE1_CURMISR_5	Holds the MISR signature for CORE1	5351 0050h
54h	32	R5SS1_STC_CORE1_CURMISR_6	Holds the MISR signature for CORE1	5351 0054h
58h	32	R5SS1_STC_CORE1_CURMISR_7	Holds the MISR signature for CORE1	5351 0058h
5Ch	32	R5SS1_STC_CORE1_CURMISR_8	Holds the MISR signature for CORE1	5351 005Ch
60h	32	R5SS1_STC_CORE1_CURMISR_9	Holds the MISR signature for CORE1	5351 0060h
64h	32	R5SS1_STC_CORE1_CURMISR_10	Holds the MISR signature for CORE1	5351 0064h
68h	32	R5SS1_STC_CORE1_CURMISR_11	Holds the MISR signature for CORE1	5351 0068h
6Ch	32	R5SS1_STC_CORE1_CURMISR_12	Holds the MISR signature for CORE1	5351 006Ch
70h	32	R5SS1_STC_CORE1_CURMISR_13	Holds the MISR signature for CORE1	5351 0070h
74h	32	R5SS1_STC_CORE1_CURMISR_14	Holds the MISR signature for CORE1	5351 0074h
78h	32	R5SS1_STC_CORE1_CURMISR_15	Holds the MISR signature for CORE1	5351 0078h
7Ch	32	R5SS1_STC_CORE1_CURMISR_16	Holds the MISR signature for CORE1	5351 007Ch
80h	32	R5SS1_STC_CORE1_CURMISR_17	Holds the MISR signature for CORE1	5351 0080h
84h	32	R5SS1_STC_CORE1_CURMISR_18	Holds the MISR signature for CORE1	5351 0084h
88h	32	R5SS1_STC_CORE1_CURMISR_19	Holds the MISR signature for CORE1	5351 0088h
8Ch	32	R5SS1_STC_CORE1_CURMISR_20	Holds the MISR signature for CORE1	5351 008Ch
90h	32	R5SS1_STC_CORE1_CURMISR_21	Holds the MISR signature for CORE1	5351 0090h
94h	32	R5SS1_STC_CORE1_CURMISR_22	Holds the MISR signature for CORE1	5351 0094h
98h	32	R5SS1_STC_CORE1_CURMISR_23	Holds the MISR signature for CORE1	5351 0098h
9Ch	32	R5SS1_STC_CORE1_CURMISR_24	Holds the MISR signature for CORE1	5351 009Ch
A0h	32	R5SS1_STC_CORE1_CURMISR_25	Holds the MISR signature for CORE1	5351 00A0h
A4h	32	R5SS1_STC_CORE1_CURMISR_26	Holds the MISR signature for CORE1	5351 00A4h
A8h	32	R5SS1_STC_CORE1_CURMISR_27	Holds the MISR signature for CORE1	5351 00A8h
ACh	32	R5SS1_STC_CORE2_CURMISR_0	Holds the MISR signature for CORE2	5351 00ACh
B0h	32	R5SS1_STC_CORE2_CURMISR_1	Holds the MISR signature for CORE2	5351 00B0h
B4h	32	R5SS1_STC_CORE2_CURMISR_2	Holds the MISR signature for CORE2	5351 00B4h
B8h	32	R5SS1_STC_CORE2_CURMISR_3	Holds the MISR signature for CORE2	5351 00B8h

Table 4-38. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	R5SS1_STC Physical Address
BCh	32	R5SS1_STC_CORE2_CURMISR_4	Holds the MISR signature for CORE2	5351 00BCh
C0h	32	R5SS1_STC_CORE2_CURMISR_5	Holds the MISR signature for CORE2	5351 00C0h
C4h	32	R5SS1_STC_CORE2_CURMISR_6	Holds the MISR signature for CORE2	5351 00C4h
C8h	32	R5SS1_STC_CORE2_CURMISR_7	Holds the MISR signature for CORE2	5351 00C8h
CCh	32	R5SS1_STC_CORE2_CURMISR_8	Holds the MISR signature for CORE2	5351 00CCh
D0h	32	R5SS1_STC_CORE2_CURMISR_9	Holds the MISR signature for CORE2	5351 00D0h
D4h	32	R5SS1_STC_CORE2_CURMISR_10	Holds the MISR signature for CORE2	5351 00D4h
D8h	32	R5SS1_STC_CORE2_CURMISR_11	Holds the MISR signature for CORE2	5351 00D8h
DCh	32	R5SS1_STC_CORE2_CURMISR_12	Holds the MISR signature for CORE2	5351 00DCh
E0h	32	R5SS1_STC_CORE2_CURMISR_13	Holds the MISR signature for CORE2	5351 00E0h
E4h	32	R5SS1_STC_CORE2_CURMISR_14	Holds the MISR signature for CORE2	5351 00E4h
E8h	32	R5SS1_STC_CORE2_CURMISR_15	Holds the MISR signature for CORE2	5351 00E8h
ECh	32	R5SS1_STC_CORE2_CURMISR_16	Holds the MISR signature for CORE2	5351 00ECh
F0h	32	R5SS1_STC_CORE2_CURMISR_17	Holds the MISR signature for CORE2	5351 00F0h
F4h	32	R5SS1_STC_CORE2_CURMISR_18	Holds the MISR signature for CORE2	5351 00F4h
F8h	32	R5SS1_STC_CORE2_CURMISR_19	Holds the MISR signature for CORE2	5351 00F8h
FCh	32	R5SS1_STC_CORE2_CURMISR_20	Holds the MISR signature for CORE2	5351 00FCh
100h	32	R5SS1_STC_CORE2_CURMISR_21	Holds the MISR signature for CORE2	5351 0100h
104h	32	R5SS1_STC_CORE2_CURMISR_22	Holds the MISR signature for CORE2	5351 0104h
108h	32	R5SS1_STC_CORE2_CURMISR_23	Holds the MISR signature for CORE2	5351 0108h
10Ch	32	R5SS1_STC_CORE2_CURMISR_24	Holds the MISR signature for CORE2	5351 010Ch
110h	32	R5SS1_STC_CORE2_CURMISR_25	Holds the MISR signature for CORE2	5351 0110h
114h	32	R5SS1_STC_CORE2_CURMISR_26	Holds the MISR signature for CORE2	5351 0114h
118h	32	R5SS1_STC_CORE2_CURMISR_27	Holds the MISR signature for CORE2	5351 0118h

Table 4-39. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	R5SS1_STC_STCGCR0	Self test Global control Reg0. *NOT BYTE ACCESSIBLE
4h	32	R5SS1_STC_STCGCR1	Self test Global control Reg1
8h	32	R5SS1_STC_STCTPR	Time out counter preload register
Ch	32	R5SS1_STC_STC_CADDR	Current Address register for CORE1
10h	32	R5SS1_STC_STCCICR	Current Interval count register
14h	32	R5SS1_STC_STCGSTAT	Global Status Register
18h	32	R5SS1_STC_STCFSTAT	Fail Status Register
1Ch	32	R5SS1_STC_STCSCSCR	Signature compare Self Check Register
20h	32	R5SS1_STC_STC_CADDR2	Current Address register for CORE2
24h	32	R5SS1_STC_STC_CLKDIV	Clock Divider Register
28h	32	R5SS1_STC_STC_SEGPLR	Segment 1st interval Preload Register
2Ch	32	R5SS1_STC_SEG0_START_ADDR	ROM Start address for Segment0
30h	32	R5SS1_STC_SEG1_START_ADDR	ROM Start address for Segment1
34h	32	R5SS1_STC_SEG2_START_ADDR	ROM Start address for Segment2
38h	32	R5SS1_STC_SEG3_START_ADDR	ROM Start address for Segment3
3Ch	32	R5SS1_STC_CORE1_CURMISR_0	Holds the MISR signature for CORE1
40h	32	R5SS1_STC_CORE1_CURMISR_1	Holds the MISR signature for CORE1
44h	32	R5SS1_STC_CORE1_CURMISR_2	Holds the MISR signature for CORE1
48h	32	R5SS1_STC_CORE1_CURMISR_3	Holds the MISR signature for CORE1
4Ch	32	R5SS1_STC_CORE1_CURMISR_4	Holds the MISR signature for CORE1
50h	32	R5SS1_STC_CORE1_CURMISR_5	Holds the MISR signature for CORE1
54h	32	R5SS1_STC_CORE1_CURMISR_6	Holds the MISR signature for CORE1
58h	32	R5SS1_STC_CORE1_CURMISR_7	Holds the MISR signature for CORE1
5Ch	32	R5SS1_STC_CORE1_CURMISR_8	Holds the MISR signature for CORE1
60h	32	R5SS1_STC_CORE1_CURMISR_9	Holds the MISR signature for CORE1
64h	32	R5SS1_STC_CORE1_CURMISR_10	Holds the MISR signature for CORE1
68h	32	R5SS1_STC_CORE1_CURMISR_11	Holds the MISR signature for CORE1
6Ch	32	R5SS1_STC_CORE1_CURMISR_12	Holds the MISR signature for CORE1
70h	32	R5SS1_STC_CORE1_CURMISR_13	Holds the MISR signature for CORE1
74h	32	R5SS1_STC_CORE1_CURMISR_14	Holds the MISR signature for CORE1
78h	32	R5SS1_STC_CORE1_CURMISR_15	Holds the MISR signature for CORE1

Table 4-39. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
7Ch	32	R5SS1_STC_CORE1_CURMISR_16	Holds the MISR signature for CORE1
80h	32	R5SS1_STC_CORE1_CURMISR_17	Holds the MISR signature for CORE1
84h	32	R5SS1_STC_CORE1_CURMISR_18	Holds the MISR signature for CORE1
88h	32	R5SS1_STC_CORE1_CURMISR_19	Holds the MISR signature for CORE1
8Ch	32	R5SS1_STC_CORE1_CURMISR_20	Holds the MISR signature for CORE1
90h	32	R5SS1_STC_CORE1_CURMISR_21	Holds the MISR signature for CORE1
94h	32	R5SS1_STC_CORE1_CURMISR_22	Holds the MISR signature for CORE1
98h	32	R5SS1_STC_CORE1_CURMISR_23	Holds the MISR signature for CORE1
9Ch	32	R5SS1_STC_CORE1_CURMISR_24	Holds the MISR signature for CORE1
A0h	32	R5SS1_STC_CORE1_CURMISR_25	Holds the MISR signature for CORE1
A4h	32	R5SS1_STC_CORE1_CURMISR_26	Holds the MISR signature for CORE1
A8h	32	R5SS1_STC_CORE1_CURMISR_27	Holds the MISR signature for CORE1
ACh	32	R5SS1_STC_CORE2_CURMISR_0	Holds the MISR signature for CORE2
B0h	32	R5SS1_STC_CORE2_CURMISR_1	Holds the MISR signature for CORE2
B4h	32	R5SS1_STC_CORE2_CURMISR_2	Holds the MISR signature for CORE2
B8h	32	R5SS1_STC_CORE2_CURMISR_3	Holds the MISR signature for CORE2
BCh	32	R5SS1_STC_CORE2_CURMISR_4	Holds the MISR signature for CORE2
C0h	32	R5SS1_STC_CORE2_CURMISR_5	Holds the MISR signature for CORE2
C4h	32	R5SS1_STC_CORE2_CURMISR_6	Holds the MISR signature for CORE2
C8h	32	R5SS1_STC_CORE2_CURMISR_7	Holds the MISR signature for CORE2
CCh	32	R5SS1_STC_CORE2_CURMISR_8	Holds the MISR signature for CORE2
D0h	32	R5SS1_STC_CORE2_CURMISR_9	Holds the MISR signature for CORE2
D4h	32	R5SS1_STC_CORE2_CURMISR_10	Holds the MISR signature for CORE2
D8h	32	R5SS1_STC_CORE2_CURMISR_11	Holds the MISR signature for CORE2
DCh	32	R5SS1_STC_CORE2_CURMISR_12	Holds the MISR signature for CORE2
E0h	32	R5SS1_STC_CORE2_CURMISR_13	Holds the MISR signature for CORE2
E4h	32	R5SS1_STC_CORE2_CURMISR_14	Holds the MISR signature for CORE2

Table 4-39. R5SS1_STC, R5SS1_STC_R5SS1_STC Registers, Base Address=5351 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
E8h	32	R5SS1_STC_CORE2_CURMISR_15	Holds the MISR signature for CORE2
ECh	32	R5SS1_STC_CORE2_CURMISR_16	Holds the MISR signature for CORE2
F0h	32	R5SS1_STC_CORE2_CURMISR_17	Holds the MISR signature for CORE2
F4h	32	R5SS1_STC_CORE2_CURMISR_18	Holds the MISR signature for CORE2
F8h	32	R5SS1_STC_CORE2_CURMISR_19	Holds the MISR signature for CORE2
FCh	32	R5SS1_STC_CORE2_CURMISR_20	Holds the MISR signature for CORE2
100h	32	R5SS1_STC_CORE2_CURMISR_21	Holds the MISR signature for CORE2
104h	32	R5SS1_STC_CORE2_CURMISR_22	Holds the MISR signature for CORE2
108h	32	R5SS1_STC_CORE2_CURMISR_23	Holds the MISR signature for CORE2
10Ch	32	R5SS1_STC_CORE2_CURMISR_24	Holds the MISR signature for CORE2
110h	32	R5SS1_STC_CORE2_CURMISR_25	Holds the MISR signature for CORE2
114h	32	R5SS1_STC_CORE2_CURMISR_26	Holds the MISR signature for CORE2
118h	32	R5SS1_STC_CORE2_CURMISR_27	Holds the MISR signature for CORE2

4.5.1 R5SS0_CCMR_CCMSR1 Register (Offset = 0h) [reset = h]

Short Description: CPU Compare Status Register

Long Description:

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Table 4-40. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0000h

Figure 4-11. R5SS0_CCMR_CCMSR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															CMPE1
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1							STC1	NU0						STET1	STE1
RW							RW	RW						RW	RO
0							0	0						0	0

Access Types Legend

Table 4-41. CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU2	RW	0h	Reserved
16	CMPE1	RW	0h	Compare Error0 = CPU signals are identical1= CPU signal compare mismatchWrites '1' to clear this bit
15 - 9	NU1	RW	0h	Reserved
8	STC1	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU0	RW	0h	Reserved
1	STET1	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE1	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.2 R5SS0_CCMR_CCMKEYR1 Register (Offset = 4h) [reset = h]

Short Description: CPU Compare Key Register

Long Description:

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Table 4-42. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0004h

Figure 4-12. R5SS0_CCMR_CCMKEYR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3												MKEY1			
RW												RW			
0												0			

Access Types Legend

Table 4-43. CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU3	RW	0h	Reserved
3 - 0	MKEY1	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.3 R5SS0_CCMR_CCMSR2 Register (Offset = 8h) [reset = h]

Short Description: VIM Compare Status Register

Long Description:

Return to Summary Table

Table 4-44. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0008h

Figure 4-13. R5SS0_CCMR_CCMSR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															CMPE2
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5							STC2	NU4						STET2	STE2
RW							RW	RW						RW	RW
0							0	0						0	0

Access Types Legend

Table 4-45. CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU6	RW	0h	Reserved
16	CMPE2	RW	0h	Compare Error0 = VIM signals are identical1= VIM signal compare mismatchWrites '1' to clear this bit
15 - 9	NU5	RW	0h	Reserved
8	STC2	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU4	RW	0h	Reserved
1	STET2	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE2	RW	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.4 R5SS0_CCMR_CCMKEYR2 Register (Offset = Ch) [reset = h]

Short Description: VIM Compare Key Register

Long Description:

Return to Summary Table

Table 4-46. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 000Ch

Figure 4-14. R5SS0_CCMR_CCMKEYR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7												MKEY2			
RW												RW			
0												0			

Access Types Legend

Table 4-47. CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU7	RW	0h	Reserved
3 - 0	MKEY2	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.5 R5SS0_CCMR_CCMSR3 Register (Offset = 10h) [reset = h]

Short Description: Inactivity Monitor Status Register

Long Description:

Return to Summary Table

Table 4-48. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0010h

Figure 4-15. R5SS0_CCMR_CCMSR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															CMPE3
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9							STC3	NU8						STET3	STE3
RW							RW	RW						RW	RO
0							0	0						0	0

Access Types Legend

Table 4-49. CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU10	RW	0h	Reserved
16	CMPE3	RW	0h	Compare Error0 = Inactivity monitor signals are identical1= Inactivity monitor signal compare mismatchWrites '1' to clear this bit
15 - 9	NU9	RW	0h	Reserved
8	STC3	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU8	RW	0h	Reserved
1	STET3	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE3	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.6 R5SS0_CCMR_CCMKEYR3 Register (Offset = 14h) [reset = h]

Short Description: Inactivity Monitor Key Register

Long Description:

Return to Summary Table

Table 4-50. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0014h

Figure 4-16. R5SS0_CCMR_CCMKEYR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11												MKEY3			
RW												RW			
0												0			

Access Types Legend

Table 4-51. CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU11	RW	0h	Reserved
3 - 0	MKEY3	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.7 R5SS0_CCMR_CCMPOLCNTRL Register (Offset = 18h) [reset = h]

Short Description: CPU Compare Polarity Control Register

Long Description:

Return to Summary Table

Table 4-52. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0018h

Figure 4-17. R5SS0_CCMR_CCMPOLCNTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12								POL_INV							
RW								RO							
0								0							

Access Types Legend

Table 4-53. CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU12	RW	0h	Reserved
7 - 0	POL_INV	RO	0h	This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode. User and privilege mode read = Returns current value of the POL INVPrivilege mode write = Update the values of POL INV

4.5.8 R5SS1_CCMR_CCMSR1 Register (Offset = 0h) [reset = h]

Short Description: CPU Compare Status Register

Long Description:

Return to Summary Table

Table 4-54. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1000h

Figure 4-18. R5SS1_CCMR_CCMSR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															CMPE1
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1							STC1	NU0						STET1	STE1
RW							RW	RW						RW	RO
0							0	0						0	0

Access Types Legend

Table 4-55. CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU2	RW	0h	Reserved
16	CMPE1	RW	0h	Compare Error0 = CPU signals are identical1= CPU signal compare mismatchWrites '1' to clear this bit
15 - 9	NU1	RW	0h	Reserved
8	STC1	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU0	RW	0h	Reserved
1	STET1	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE1	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.9 R5SS1_CCMR_CCMKEYR1 Register (Offset = 4h) [reset = h]

Short Description: CPU Compare Key Register

Long Description:

Return to Summary Table

Table 4-56. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1004h

Figure 4-19. R5SS1_CCMR_CCMKEYR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3												MKEY1			
RW												RW			
0												0			

Access Types Legend

Table 4-57. CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU3	RW	0h	Reserved
3 - 0	MKEY1	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.10 R5SS1_CCMR_CCMSR2 Register (Offset = 8h) [reset = h]

Short Description: VIM Compare Status Register

Long Description:

Return to Summary Table

Table 4-58. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1008h

Figure 4-20. R5SS1_CCMR_CCMSR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															CMPE2
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5							STC2	NU4						STET2	STE2
RW							RW	RW						RW	RW
0							0	0						0	0

Access Types Legend

Table 4-59. CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU6	RW	0h	Reserved
16	CMPE2	RW	0h	Compare Error0 = VIM signals are identical1= VIM signal compare mismatchWrites '1' to clear this bit
15 - 9	NU5	RW	0h	Reserved
8	STC2	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU4	RW	0h	Reserved
1	STET2	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE2	RW	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.11 R5SS1_CCMR_CCMKEYR2 Register (Offset = Ch) [reset = h]

Short Description: VIM Compare Key Register

Long Description:

Return to Summary Table

Table 4-60. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 100Ch

Figure 4-21. R5SS1_CCMR_CCMKEYR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7												MKEY2			
RW												RW			
0												0			

Access Types Legend

Table 4-61. CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU7	RW	0h	Reserved
3 - 0	MKEY2	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.12 R5SS1_CCMR_CCMSR3 Register (Offset = 10h) [reset = h]

Short Description: Inactivity Monitor Status Register

Long Description:

Return to Summary Table

Table 4-62. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1010h

Figure 4-22. R5SS1_CCMR_CCMSR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															CMPE3
RW															RW
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9							STC3	NU8						STET3	STE3
RW							RW	RW						RW	RO
0							0	0						0	0

Access Types Legend

Table 4-63. CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU10	RW	0h	Reserved
16	CMPE3	RW	0h	Compare Error0 = Inactivity monitor signals are identical1= Inactivity monitor signal compare mismatchWrites '1' to clear this bit
15 - 9	NU9	RW	0h	Reserved
8	STC3	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU8	RW	0h	Reserved
1	STET3	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE3	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

4.5.13 R5SS1_CCMR_CCMKEYR3 Register (Offset = 14h) [reset = h]

Short Description: Inactivity Monitor Key Register

Long Description:

Return to Summary Table

Table 4-64. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1014h

Figure 4-23. R5SS1_CCMR_CCMKEYR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11												MKEY3			
RW												RW			
0												0			

Access Types Legend

Table 4-65. CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU11	RW	0h	Reserved
3 - 0	MKEY3	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

4.5.14 R5SS1_CCMR_CCMPOLCNTRL Register (Offset = 18h) [reset = h]

Short Description: CPU Compare Polarity Control Register

Long Description:

Return to Summary Table

Table 4-66. Instance Table

Instance Name	Physical Address
R5SS1_CCMR	5321 1018h

Figure 4-24. R5SS1_CCMR_CCMPOLCNTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12								POL_INV							
RW								RO							
0								0							

Access Types Legend

Table 4-67. CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU12	RW	0h	Reserved
7 - 0	POL_INV	RO	0h	This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode. User and privilege mode read = Returns current value of the POL INVPrivilege mode write = Update the values of POL INV

4.5.15 TOP_PBIST_PBIST_A0 Register (Offset = 100h) [reset = h]

Short Description: Variable Address Register0

Long Description:

Return to Summary Table

Table 4-68. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0100h

Figure 4-25. TOP_PBIST_PBIST_A0 Name Register

15	14	13	12	11	10	9	8
PBIST_CI2							
RW							
0							
7	6	5	4	3	2	1	0
PBIST_CI2							
RW							
0							

Access Types Legend

Table 4-69. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_CI2	RW	0h	TI Internal Register.Reserved for HW RnD

4.5.16 TOP_PBIST_PBIST_A1 Register (Offset = 104h) [reset = h]

Short Description: Variable Address Register1

Long Description:

Return to Summary Table

Table 4-70. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0104h

Figure 4-26. TOP_PBIST_PBIST_A1 Name Register

15	14	13	12	11	10	9	8
PBIST_CI3							
RW							
0							
7	6	5	4	3	2	1	0
PBIST_CI3							
RW							
0							

Access Types Legend

Table 4-71. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_CI3	RW	0h	TI Internal Register.Reserved for HW RnD

4.5.17 TOP_PBIST_PBIST_A2 Register (Offset = 108h) [reset = h]

Short Description: Variable Address Register2

Long Description:

Return to Summary Table

Table 4-72. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0108h

Figure 4-27. TOP_PBIST_PBIST_A2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RGS								RDS							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWR								RAM							
RW								RW							
0								0							

Access Types Legend

Table 4-73. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RGS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
23 - 16	RDS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
15 - 8	DWR	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
7 - 0	RAM	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

4.5.18 TOP_PBIST_PBIST_A3 Register (Offset = 10Ch) [reset = h]

Short Description: Variable Address Register3

Long Description:

Return to Summary Table

Table 4-74. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 010Ch

Figure 4-28. TOP_PBIST_PBIST_A3 Name Register

15	14	13	12	11	10	9	8
DLR1							
RW							
10							
7	6	5	4	3	2	1	0
DLR0							
RW							
1000							

Access Types Legend

Table 4-75. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	DLR1	RW	Ah	Datalogger Register[8] : Reserevd[9] : Default Testing Mode. When in this mode, ROM-based testing is kicked off. If the intention is to perform go/no-go testing via config, write to both this bit and bit [2] ofthe Datalogger Register simultaneously[15:10] : Reserevd
7 - 0	DLR0	RW	3E8h	Datalogger Register[1:0] : Reserved[2] : ROM-based testing mode. Setting this bit to 1 enables the PBIST controller to execute test algorithms that arestored in the PBIST ROM[3] : Do not change this bit from its default value of 1[4] : Config access mode. Setting this bit allows the host processor to configure the PBIST controller registers[7:5] : Reserved

4.5.19 TOP_PBIST_PBIST_L0 Register (Offset = 110h) [reset = h]

Short Description: Variable Loop Count Register L0

Long Description:

Return to Summary Table

Table 4-76. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0110h

Figure 4-29. TOP_PBIST_PBIST_L0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_CMS			
NONE				RW			
0				0			

Access Types Legend

Table 4-77. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_CMS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

4.5.20 TOP_PBIST_PBIST_L1 Register (Offset = 114h) [reset = h]

Short Description: Variable Loop Count Register L1

Long Description:

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Table 4-78. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0114h

Figure 4-30. TOP_PBIST_PBIST_L1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			PBIST_PC				
NONE			RW				
0			0				

Access Types Legend

Table 4-79. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	PBIST_PC	RW	0h	TI Internal Register.Reserved for HW RnD

4.5.21 TOP_PBIST_PBIST_L2 Register (Offset = 118h) [reset = h]

Short Description: Variable Loop Count Register L2

Long Description:

Return to Summary Table

Table 4-80. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0118h

Figure 4-31. TOP_PBIST_PBIST_L2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCR3								SCR2							
RW								RW							
1110110								1010100							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR1								SCR0							
RW								RW							
110010								10000							

Access Types Legend

Table 4-81. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SCR3	RW	10F05Eh	TI Internal Register.Reserved for HW RnD
23 - 16	SCR2	RW	F69B4h	TI Internal Register.Reserved for HW RnD
15 - 8	SCR1	RW	1ADBAh	TI Internal Register.Reserved for HW RnD
7 - 0	SCR0	RW	2710h	TI Internal Register.Reserved for HW RnD

4.5.22 TOP_PBIST_PBIST_L3 Register (Offset = 11Ch) [reset = h]

Short Description: Variable Loop Count Register L3

Long Description:

Return to Summary Table

Table 4-82. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 011Ch

Figure 4-32. TOP_PBIST_PBIST_L3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCR7								SCR6							
RW								RW							
11111110								11011100							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR5								SCR4							
RW								RW							
10111010								10011000							

Access Types Legend

Table 4-83. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SCR7	RW	A98AC6h	TI Internal Register.Reserved for HW RnD
23 - 16	SCR6	RW	A8041Ch	TI Internal Register.Reserved for HW RnD
15 - 8	SCR5	RW	9A4822h	TI Internal Register.Reserved for HW RnD
7 - 0	SCR4	RW	98C178h	TI Internal Register.Reserved for HW RnD

4.5.23 TOP_PBIST_PBIST_DD10 Register (Offset = 120h) [reset = h]

Short Description: DD0 Data Register 16 (D0)

Long Description:

Return to Summary Table

Table 4-84. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0120h

Figure 4-33. TOP_PBIST_PBIST_DD10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS3								CS2							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS1								CS0							
RW								RW							
0								0							

Access Types Legend

Table 4-85. PBIST_DD10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	CS3	RW	0h	TI Internal Register.Reserved for HW RnD
23 - 16	CS2	RW	0h	TI Internal Register.Reserved for HW RnD
15 - 8	CS1	RW	0h	TI Internal Register.Reserved for HW RnD
7 - 0	CS0	RW	0h	TI Internal Register.Reserved for HW RnD

4.5.24 TOP_PBIST_PBIST_DE10 Register (Offset = 124h) [reset = h]

Short Description: DE0 Data Register 16 (D0)

Long Description:

Return to Summary Table

Table 4-86. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0124h

Figure 4-34. TOP_PBIST_PBIST_DE10 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PBIST_FDLY							
RW							
1001000							

Access Types Legend

Table 4-87. PBIST_DE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PBIST_FDLY	RW	F4628h	TI Internal Register.Reserved for HW RnD

4.5.25 TOP_PBIST_PBIST_CA0 Register (Offset = 130h) [reset = h]

Short Description: Constant Address Register0

Long Description:

Return to Summary Table

Table 4-88. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0130h

Figure 4-35. TOP_PBIST_PBIST_CA0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PBIST_PACT							
RW							
0							

Access Types Legend

Table 4-89. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_PACT	RW	0h	Pbist Active/ROM Clock Enable Register[0]: This bit must be set to turn on internal PBIST clocks. Setting this bit asserts an internal signal that is usedas the clock gate enable. As long as this bit is 0, any access to PBIST will not go through, and PBIST willremain in an almost zero-power mode.Value 0 = Disable internal PBIST clocksValue 1 = Enable internal PBIST clocks

4.5.26 TOP_PBIST_PBIST_CA1 Register (Offset = 134h) [reset = h]

Short Description: Constant Address Register1

Long Description:

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Table 4-90. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0134h

Figure 4-36. TOP_PBIST_PBIST_CA1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			PBIST_ID				
NONE			RW				
0			1				

Access Types Legend

Table 4-91. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	PBIST_ID	RW	1h	PBIST ID.This is a unique ID assigned to each PBIST controller in a device with multiple PBIST controllers. The value of this register does not affect the functionality of the CPU interface.

4.5.27 TOP_PBIST_PBIST_CA2 Register (Offset = 138h) [reset = h]

Short Description: Constant Address Register2

Long Description:

Return to Summary Table

Table 4-92. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0138h

Figure 4-37. TOP_PBIST_PBIST_CA2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PBIST_FSFR0							
RO							
0							

Access Types Legend

Table 4-93. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_FSFR0	RO	0h	Fail Status Fail Register- Port 0 This register indicates if a failure occurred during a memory self-test.Value 0 = No failure occurredValue 1 = Indicates a failure

4.5.28 TOP_PBIST_PBIST_CA3 Register (Offset = 13Ch) [reset = h]

Short Description: Constant Address Register3

Long Description:

Return to Summary Table

Table 4-94. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 013Ch

Figure 4-38. TOP_PBIST_PBIST_CA3 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PBIST_FSFR1							
RO							
0							

Access Types Legend

Table 4-95. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_FSFR1	RO	0h	Fail Status Fail Register- Port 1 This register indicates if a failure occurred during a memory self-test.Value 0 = No failure occurredValue 1 = Indicates a failure

4.5.29 TOP_PBIST_PBIST_CL0 Register (Offset = 140h) [reset = h]

Short Description: Constant Loop Count Register0

Long Description:

Return to Summary Table

Table 4-96. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0140h

Figure 4-39. TOP_PBIST_PBIST_CL0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR0			
NONE				RO			
0				0			

Access Types Legend

Table 4-97. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_FSRCR0	RO	0h	Fail Status Count - Port 0 These registers keep count of the number of failures observed during the memory self-test. The PBISTcontroller stops executing the memory self-test whenever a failure occurs in any memory instance for anyof the test algorithms. The value in gets incremented by one whenever a failure occurs

4.5.30 TOP_PBIST_PBIST_CL1 Register (Offset = 144h) [reset = h]

Short Description: Constant Loop Count Register1

Long Description:

Return to Summary Table

Table 4-98. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0144h

Figure 4-40. TOP_PBIST_PBIST_CL1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR1			
NONE				RO			
0				0			

Access Types Legend

Table 4-99. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_FSRCR1	RO	0h	Fail Status Count - Port 1These registers keep count of the number of failures observed during the memory self-test. The PBISTcontroller stops executing the memory self-test whenever a failure occurs in any memory instance for anyof the test algorithms. The value in gets incremented by one whenever a failure occurs

4.5.31 TOP_PBIST_PBIST_CL2 Register (Offset = 148h) [reset = h]

Short Description: Constant Loop Count Register2

Long Description:

Return to Summary Table

Table 4-100. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0148h

Figure 4-41. TOP_PBIST_PBIST_CL2 Name Register

15	14	13	12	11	10	9	8
PBIST_FSRA1							
RO							
0							
7	6	5	4	3	2	1	0
PBIST_FSRA1							
RO							
0							

Access Types Legend

Table 4-101. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_FSRA1	RO	0h	TI Internal Register.Reserved for HW RnD

4.5.32 TOP_PBIST_PBIST_CL3 Register (Offset = 14Ch) [reset = h]

Short Description: Constant Loop Count Register3

Long Description:

Return to Summary Table

Table 4-102. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 014Ch

Figure 4-42. TOP_PBIST_PBIST_CL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBIST_FSRDL0															
RO															
10101010101010101010101010101010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBIST_FSRDL0															
RO															
10101010101010101010101010101010															

Access Types Legend

Table 4-103. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_FSRDL0	RO	7F7E1FB90 6A8A772B2 8676F312h	TI Internal Register.Reserved for HW RnD

4.5.33 TOP_PBIST_PBIST_CI0 Register (Offset = 150h) [reset = h]

Short Description: Constant Increment Register0

Long Description:

Return to Summary Table

Table 4-104. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0150h

Figure 4-43. TOP_PBIST_PBIST_CI0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBIST_FSRDL1															
RO															
10101010101010101010101010101010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBIST_FSRDL1															
RO															
10101010101010101010101010101010															

Access Types Legend

Table 4-105. PBIST_CI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_FSRDL1	RO	7F7E1FB90 6A8A772B2 8676F312h	TI Internal Register.Reserved for HW RnD

4.5.34 TOP_PBIST_PBIST_CI1 Register (Offset = 154h) [reset = h]

Short Description: Constant Increment Register1

Long Description:

Return to Summary Table

Table 4-106. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0154h

Figure 4-44. TOP_PBIST_PBIST_CI1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						PBIST_ROM	
NONE						RW	
0						11	

Access Types Legend

Table 4-107. PBIST_CI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	PBIST_ROM	RW	Bh	Rom Mask .This two-bit register sets appropriate ROM access modes for the PBIST controller.Value 0h = No information is used from ROMValue 1h = Only RAM Group information from ROMVaule 2h = Only Algorithm information from ROMValue 3h = Both Algorithm and RAM information from ROM. This option should be selected for application self-test.

4.5.35 TOP_PBIST_PBIST_CI2 Register (Offset = 158h) [reset = h]

Short Description: Constant Increment Register2

Long Description:

Return to Summary Table

Table 4-108. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0158h

Figure 4-45. TOP_PBIST_PBIST_CI2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALGO3								ALGO2							
RW								RW							
11111111								11111111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALGO1								ALGO0							
RW								RW							
11111111								11111111							

Access Types Legend

Table 4-109. PBIST_CI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	ALGO3	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
23 - 16	ALGO2	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
15 - 8	ALGO1	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
7 - 0	ALGO0	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.

4.5.36 TOP_PBIST_PBIST_CI3 Register (Offset = 15Ch) [reset = h]

Short Description: Constant Increment Register3

Long Description:

Return to Summary Table

Table 4-110. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 015Ch

Figure 4-46. TOP_PBIST_PBIST_CI3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RINFOL3								RINFOL2							
RW								RW							
11111111								11111111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINFOL1								RINFOL0							
RW								RW							
11111111								11111111							

Access Types Legend

Table 4-111. PBIST_CI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RINFOL3	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23 - 16	RINFOL2	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15 - 8	RINFOL1	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7 - 0	RINFOL0	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

4.5.37 TOP_PBIST_PBIST_RAMT Register (Offset = 160h) [reset = h]

Short Description: RAM Configuration (RAMT -RAM)

Long Description:

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Table 4-112. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0160h

Figure 4-47. TOP_PBIST_PBIST_RAMT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RINFOU3								RINFOU2							
RW								RW							
11111111								11111111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINFOU1								RINFOU0							
RW								RW							
11111111								11111111							

Access Types Legend

Table 4-113. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RINFOU3	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23 - 16	RINFOU2	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15 - 8	RINFOU1	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7 - 0	RINFOU0	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

4.5.38 R5SS0_STC_STCGCR0 Register (Offset = 0h) [reset = h]

Short Description: Self test Global control Reg0. *NOT BYTE ACCESSIBLE

Long Description:

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Table 4-114. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0000h

Figure 4-48. R5SS0_STC_STCGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTCOUNT_B16															
RW															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0					CAP_IDLE_CYCLE			SCANEN_HIGH_CAP_IDLE_CYCLE			NU1			RS_CNT_B1	
RO					RW			RW			RO			RW	
0					1			1			0			0	

Access Types Legend

Table 4-115. STCGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	INTCOUNT_B16	RW	1h	Number of intervals of the self test run (RWP - Read, Priviledge Mode Write only)Count of intervals that need to be covered for a specific selftest run.The selftest controller sends out ?complete? indication once it runs all of the intervals programmed in this field.INTCOUNT_B16=0 is an invalid configuration for a selftest.
15 - 11	NU0	RO	0h	Reserved bits
10 - 8	CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only)Idle Cycles before and after capture clock. This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
7 - 5	SCANEN_HIGH_CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only). *NOT BYTE ACCESSIBLEIdle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation. This value is used to insert that many idle cycles in the shift clock (scan_en going high to func_clk_en generation) and misr_log_clk (scan_en going high to misr_log_en generation) generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
4 - 2	NU1	RO	0h	Reserved bits
1 - 0	RS_CNT_B1	RW	0h	Restart/Continue or preload (RWP - Read, Priviledge Mode Write only)This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run.00 = Continue NSTC run from previous interval01 = Restart NSTC run from ROM address 01X = Start from segment number specified in STC_SEGPLR register

4.5.39 R5SS0_STC_STCGCR1 Register (Offset = 4h) [reset = h]

Short Description: Self test Global control Reg1

Long Description:

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Table 4-116. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0004h

Figure 4-49. R5SS0_STC_STCGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2				SEG0_CORE_SEL				NU3	CODEC_SPREAD_MODE	LP_SCAN_MODE	ROM_ACCESS_INV	ST_ENA_B4			
RO				RW				RO	RW	RW	RW	RW			
0				0				0	0	1	0	101			

Access Types Legend

Table 4-117. STCGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RO	0h	Reserved bits
11 - 8	SEG0_CORE_SEL	RW	0h	Selects the Segment0 CORE for self test (RWP - Read, Priviledge Mode Write only)Select the Segment0 CORE for Self -Test0001 = Select CORE for selftestOther = CORE not selected.
7	NU3	RO	0h	Reserved bits
6	CODEC_SPREAD_MODE	RW	0h	Codec Spread Mode control signal (RWP - Read, Priviledge Mode Write only)This bit is used to configure the codec in spread / X-OR mode.1 = Spread mode0 = XOR mode
5	LP_SCAN_MODE	RW	1h	LP scan mode (RWP - Read, Priviledge Mode Write only)This bit is used to decide the scan configuration:1 = Operates in Low Power Scan Mode. 0 = Operates in Normal Scan Mode.
4	ROM_ACCESS_INV	RW	0h	Rom access inversion mode (RWP - Read, Priviledge Mode Write only)- NOT SUPPORTED
3 - 0	ST_ENA_B4	RW	65h	Self test enable key (RWP - Read, Priviledge Mode Write only)1010 = Self test run enabled All values other than 1010 = Self test run disabled

4.5.40 R5SS0_STC_STCTPR Register (Offset = 8h) [reset = h]

Short Description: Time out counter preload register

Long Description:

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Table 4-118. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0008h

Figure 4-50. R5SS0_STC_STCTPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_PRELOAD															
RW															
11111111111111111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_PRELOAD															
RW															
11111111111111111111111111111111															

Access Types Legend

Table 4-119. STCTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_PRELOAD	RW	8C3DEFB1 EDB984FE2 AC71C71C7 h	Self test time out preload (RWP - Read, Priviledge Mode Write only)This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective.This register value (preload count value) gets loaded into the self test timeout down counter whenever a self test run is initiated (ST_ENA is enabled). and gets disabled on completion of a self test run.

4.5.41 R5SS0_STC_STC_CADDR Register (Offset = Ch) [reset = h]

Short Description: Current Address register for CORE1

Long Description:

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Table 4-120. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 000Ch

Figure 4-51. R5SS0_STC_STC_CADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
RO															
0															

Access Types Legend

Table 4-121. STC_CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE1This register reflects the current ROM address (for micro code load) accessed during selftest for CORE1 in of case segment0 and all the remaining segmentsn where n = 1 to 3).

4.5.42 R5SS0_STC_STCCICR Register (Offset = 10h) [reset = h]

Short Description: Current Interval count register

Long Description:

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Table 4-122. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0010h

Figure 4-52. R5SS0_STC_STCCICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CORE2_ICOUNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE1_ICOUNT															
RO															
0															

Access Types Legend

Table 4-123. STCCICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CORE2_ICOUNT	RO	0h	Specifies the last interval number for CORE2This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0.
15 - 0	CORE1_ICOUNT	RO	0h	Specifies the last interval number for CORE1This specifies the Last executed Interval number of a self-test run.

4.5.43 R5SS0_STC_STCGSTAT Register (Offset = 14h) [reset = h]

Short Description: Global Status Register

Long Description:

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Table 4-124. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0014h

Figure 4-53. R5SS0_STC_STCGSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4				ST_ACTIVE				NU5						TEST_FAIL	TEST_DONE
RO				RO				RO						RO	RO
0				101				0						0	0

Access Types Legend

Table 4-125. STCGSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU4	RO	0h	Reserved bits
11 - 8	ST_ACTIVE	RO	65h	Tells whether self test is currently active or not.1010 = Self test is activeOthers = SelfTest is not activeOnce the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value.
7 - 2	NU5	RO	0h	Reserved bits
1	TEST_FAIL	RO	0h	Test_fail flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Self test run has not failed1 = SelfTest run has failed. Write Clear.
0	TEST_DONE	RO	0h	Test_done_flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Not completed1 = SelfTest run Completed

4.5.44 R5SS0_STC_STCFSTAT Register (Offset = 18h) [reset = h]

Short Description: Fail Status Register

Long Description:

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Table 4-126. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0018h

Figure 4-54. R5SS0_STC_STCFSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6											FSEG_ID		TO_ER_B1	CPU2_FAIL_B1	CPU1_FAIL_B1
RO											RO		RO	RO	RO
0											0		0	0	0

Access Types Legend

Table 4-127. STCFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU6	RO	0h	Reserved bits
4 - 3	FSEG_ID	RO	0h	Failed Segment ID (RCP - Read, Clear on Writing in Priviledge Mode)This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur.00 = Failure on Segment 001 = Failure on Segment 110 = Failure on Segment 211 = Failure on Segment 3
2	TO_ER_B1	RO	0h	Tells whether self test failed because of time out error (RCP - Read, Clear on Writing in Priviledge Mode)0 = No time out error occurred1 = SelfTest run failed due to a timeout error
1	CPU2_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE2 when in Segment0 mode (RCP - Read, Clear on Writing in Priviledge Mode)0 = No MISR mismatch for CORE21 = Self test run failed due to MISR mismatch for CORE2
0	CPU1_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE1 (RCP - Read, Clear on Writing in Priviledge Mode)Applicable to all segments.0 = No MISR mismatch for CORE11 = Self test run failed due to MISR mismatch for CORE1

4.5.45 R5SS0_STC_STCSCSCR Register (Offset = 1Ch) [reset = h]

Short Description: Signature compare Self Check Register

Long Description:

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Table 4-128. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 001Ch

Figure 4-55. R5SS0_STC_STCSCSCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7											FAULT_INS_B1	SELF_CHECK_KEY_B4			
RO											RW	RW			
0											0	101			

Access Types Legend

Table 4-129. STCSCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU7	RO	0h	Reserved bits
4	FAULT_INS_B1	RW	0h	Fault Insertion bit (RWP - Read, Priviledge Mode Write only)0 = No fault insertion.1 = Inserts fault in the logic unedr test which will make signature compare fail. This feature is used as diagnostic check of the STC IP.
3 - 0	SELF_CHECK_KEY_B4	RW	65h	Signature compare logic self check key enable/disable (RWP - Read, Priviledge Mode Write only)1010 = Signature compare logic Self Check is enabledAll values other than 1010 = Signature compare logic Self Check is disabled

4.5.46 R5SS0_STC_STC_CADDR2 Register (Offset = 20h) [reset = h]

Short Description: Current Address register for CORE2

Long Description:

Return to Summary Table

Table 4-130. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0020h

Figure 4-56. R5SS0_STC_STC_CADDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
RO															
0															

Access Types Legend

Table 4-131. STC_CADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE2This register reflects the current ROM address(for micro code load) accessed during selftest for CORE2 in of case segment0.

4.5.47 R5SS0_STC_STC_CLKDIV Register (Offset = 24h) [reset = h]

Short Description: Clock Divider Register

Long Description:

Return to Summary Table

Table 4-132. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0024h

Figure 4-57. R5SS0_STC_STC_CLKDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8					CLKDIV0			NU9					CLKDIV1		
RO					RW			RO					RW		
0					0			0					0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10					CLKDIV2			NU11					CLKDIV3		
RO					RW			RO					RW		
0					0			0					0		

Access Types Legend

Table 4-133. STC_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	NU8	RO	0h	Reserved bits
26 - 24	CLKDIV0	RW	0h	Clock division for Seg0 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 0
23 - 19	NU9	RO	0h	Reserved bits
18 - 16	CLKDIV1	RW	0h	Clock division for Seg1 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 1
15 - 11	NU10	RO	0h	Reserved bits
10 - 8	CLKDIV2	RW	0h	Clock division for Seg2 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 2
7 - 3	NU11	RO	0h	Reserved bits
2 - 0	CLKDIV3	RW	0h	Clock division for Seg3 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 3

4.5.48 R5SS0_STC_STC_SEGPLR Register (Offset = 28h) [reset = h]

Short Description: Segment 1st interval Preload Register

Long Description:

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Table 4-134. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0028h

Figure 4-58. R5SS0_STC_STC_SEGPLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														SEGID_PLOAD	
RO														RW	
0														0	

Access Types Legend

Table 4-135. STC_SEGPLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved bits
1 - 0	SEGID_PLOAD	RW	0h	Segment number for which preload is to be started (RWP - Read, Priviledge Mode Write only)This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register.The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X00 = Preload the address of the 1st interval of segment 0.01 = Preload the address of the 1st interval of segment 1.10 = Preload the address of the 1st interval of segment 2.11 = Preload the address of the 1st interval of segment 3.

4.5.49 R5SS0_STC_SEG0_START_ADDR Register (Offset = 2Ch) [reset = h]

Short Description: ROM Start address for Segment0

Long Description:

Return to Summary Table

Table 4-136. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 002Ch

Figure 4-59. R5SS0_STC_SEG0_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-137. SEG0_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU13	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 0 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR

4.5.50 R5SS0_STC_SEG1_START_ADDR Register (Offset = 30h) [reset = h]

Short Description: ROM Start address for Segment1

Long Description:

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Table 4-138. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0030h

Figure 4-60. R5SS0_STC_SEG1_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-139. SEG1_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU14	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 1 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 1.

4.5.51 R5SS0_STC_SEG2_START_ADDR Register (Offset = 34h) [reset = h]

Short Description: ROM Start address for Segment2

Long Description:

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Table 4-140. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0034h

Figure 4-61. R5SS0_STC_SEG2_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-141. SEG2_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU15	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 2 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 2.

4.5.52 R5SS0_STC_SEG3_START_ADDR Register (Offset = 38h) [reset = h]

Short Description: ROM Start address for Segment3

Long Description:

Return to Summary Table

Table 4-142. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0038h

Figure 4-62. R5SS0_STC_SEG3_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-143. SEG3_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU16	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 3 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 3.

4.5.53 R5SS0_STC_CORE1_CURMISR_0 Register (Offset = 3Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-144. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 003Ch

Figure 4-63. R5SS0_STC_CORE1_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR0															
RO															
0															

Access Types Legend

Table 4-145. CORE1_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR0	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.54 R5SS0_STC_CORE1_CURMISR_1 Register (Offset = 40h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-146. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0040h

Figure 4-64. R5SS0_STC_CORE1_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR1															
RO															
0															

Access Types Legend

Table 4-147. CORE1_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR1	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.55 R5SS0_STC_CORE1_CURMISR_2 Register (Offset = 44h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-148. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0044h

Figure 4-65. R5SS0_STC_CORE1_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR2															
RO															
0															

Access Types Legend

Table 4-149. CORE1_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR2	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.56 R5SS0_STC_CORE1_CURMISR_3 Register (Offset = 48h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-150. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0048h

Figure 4-66. R5SS0_STC_CORE1_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR3															
RO															
0															

Access Types Legend

Table 4-151. CORE1_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR3	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.57 R5SS0_STC_CORE1_CURMISR_4 Register (Offset = 4Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-152. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 004Ch

Figure 4-67. R5SS0_STC_CORE1_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR4															
RO															
0															

Access Types Legend

Table 4-153. CORE1_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR4	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.58 R5SS0_STC_CORE1_CURMISR_5 Register (Offset = 50h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-154. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0050h

Figure 4-68. R5SS0_STC_CORE1_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR5															
RO															
0															

Access Types Legend

Table 4-155. CORE1_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR5	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.59 R5SS0_STC_CORE1_CURMISR_6 Register (Offset = 54h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-156. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0054h

Figure 4-69. R5SS0_STC_CORE1_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR6															
RO															
0															

Access Types Legend

Table 4-157. CORE1_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR6	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.60 R5SS0_STC_CORE1_CURMISR_7 Register (Offset = 58h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-158. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0058h

Figure 4-70. R5SS0_STC_CORE1_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR7															
RO															
0															

Access Types Legend

Table 4-159. CORE1_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR7	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.61 R5SS0_STC_CORE1_CURMISR_8 Register (Offset = 5Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-160. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 005Ch

Figure 4-71. R5SS0_STC_CORE1_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR8															
RO															
0															

Access Types Legend

Table 4-161. CORE1_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR8	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.62 R5SS0_STC_CORE1_CURMISR_9 Register (Offset = 60h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-162. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0060h

Figure 4-72. R5SS0_STC_CORE1_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR9															
RO															
0															

Access Types Legend

Table 4-163. CORE1_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR9	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.63 R5SS0_STC_CORE1_CURMISR_10 Register (Offset = 64h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-164. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0064h

Figure 4-73. R5SS0_STC_CORE1_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR10															
RO															
0															

Access Types Legend

Table 4-165. CORE1_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR10	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.64 R5SS0_STC_CORE1_CURMISR_11 Register (Offset = 68h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-166. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0068h

Figure 4-74. R5SS0_STC_CORE1_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR11															
RO															
0															

Access Types Legend

Table 4-167. CORE1_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR11	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.65 R5SS0_STC_CORE1_CURMISR_12 Register (Offset = 6Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-168. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 006Ch

Figure 4-75. R5SS0_STC_CORE1_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR12															
RO															
0															

Access Types Legend

Table 4-169. CORE1_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR12	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.66 R5SS0_STC_CORE1_CURMISR_13 Register (Offset = 70h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-170. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0070h

Figure 4-76. R5SS0_STC_CORE1_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR13															
RO															
0															

Access Types Legend

Table 4-171. CORE1_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR13	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.67 R5SS0_STC_CORE1_CURMISR_14 Register (Offset = 74h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-172. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0074h

Figure 4-77. R5SS0_STC_CORE1_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR14															
RO															
0															

Access Types Legend

Table 4-173. CORE1_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR14	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.68 R5SS0_STC_CORE1_CURMISR_15 Register (Offset = 78h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-174. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0078h

Figure 4-78. R5SS0_STC_CORE1_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR15															
RO															
0															

Access Types Legend

Table 4-175. CORE1_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR15	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.69 R5SS0_STC_CORE1_CURMISR_16 Register (Offset = 7Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-176. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 007Ch

Figure 4-79. R5SS0_STC_CORE1_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR16															
RO															
0															

Access Types Legend

Table 4-177. CORE1_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR16	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.70 R5SS0_STC_CORE1_CURMISR_17 Register (Offset = 80h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-178. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0080h

Figure 4-80. R5SS0_STC_CORE1_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR17															
RO															
0															

Access Types Legend

Table 4-179. CORE1_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR17	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.71 R5SS0_STC_CORE1_CURMISR_18 Register (Offset = 84h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-180. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0084h

Figure 4-81. R5SS0_STC_CORE1_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR18															
RO															
0															

Access Types Legend

Table 4-181. CORE1_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR18	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.72 R5SS0_STC_CORE1_CURMISR_19 Register (Offset = 88h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-182. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0088h

Figure 4-82. R5SS0_STC_CORE1_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR19															
RO															
0															

Access Types Legend

Table 4-183. CORE1_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR19	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.73 R5SS0_STC_CORE1_CURMISR_20 Register (Offset = 8Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-184. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 008Ch

Figure 4-83. R5SS0_STC_CORE1_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR20															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR20															
RO															
0															

Access Types Legend

Table 4-185. CORE1_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR20	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.74 R5SS0_STC_CORE1_CURMISR_21 Register (Offset = 90h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-186. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0090h

Figure 4-84. R5SS0_STC_CORE1_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR21															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR21															
RO															
0															

Access Types Legend

Table 4-187. CORE1_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR21	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.75 R5SS0_STC_CORE1_CURMISR_22 Register (Offset = 94h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-188. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0094h

Figure 4-85. R5SS0_STC_CORE1_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR22															
RO															
0															

Access Types Legend

Table 4-189. CORE1_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR22	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.76 R5SS0_STC_CORE1_CURMISR_23 Register (Offset = 98h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-190. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0098h

Figure 4-86. R5SS0_STC_CORE1_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR23															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR23															
RO															
0															

Access Types Legend

Table 4-191. CORE1_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR23	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.77 R5SS0_STC_CORE1_CURMISR_24 Register (Offset = 9Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-192. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 009Ch

Figure 4-87. R5SS0_STC_CORE1_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR24															
RO															
0															

Access Types Legend

Table 4-193. CORE1_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR24	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.78 R5SS0_STC_CORE1_CURMISR_25 Register (Offset = A0h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-194. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A0h

Figure 4-88. R5SS0_STC_CORE1_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR25															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR25															
RO															
0															

Access Types Legend

Table 4-195. CORE1_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR25	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.79 R5SS0_STC_CORE1_CURMISR_26 Register (Offset = A4h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-196. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A4h

Figure 4-89. R5SS0_STC_CORE1_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR26															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR26															
RO															
0															

Access Types Legend

Table 4-197. CORE1_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR26	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.80 R5SS0_STC_CORE1_CURMISR_27 Register (Offset = A8h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-198. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A8h

Figure 4-90. R5SS0_STC_CORE1_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR27															
RO															
0															

Access Types Legend

Table 4-199. CORE1_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR27	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.81 R5SS0_STC_CORE2_CURMISR_0 Register (Offset = ACh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-200. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00ACh

Figure 4-91. R5SS0_STC_CORE2_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR0															
RO															
0															

Access Types Legend

Table 4-201. CORE2_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR0	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.82 R5SS0_STC_CORE2_CURMISR_1 Register (Offset = B0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-202. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B0h

Figure 4-92. R5SS0_STC_CORE2_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR1															
RO															
0															

Access Types Legend

Table 4-203. CORE2_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR1	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.83 R5SS0_STC_CORE2_CURMISR_2 Register (Offset = B4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-204. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B4h

Figure 4-93. R5SS0_STC_CORE2_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR2															
RO															
0															

Access Types Legend

Table 4-205. CORE2_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR2	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.84 R5SS0_STC_CORE2_CURMISR_3 Register (Offset = B8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-206. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B8h

Figure 4-94. R5SS0_STC_CORE2_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR3															
RO															
0															

Access Types Legend

Table 4-207. CORE2_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR3	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.85 R5SS0_STC_CORE2_CURMISR_4 Register (Offset = BCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-208. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00BCh

Figure 4-95. R5SS0_STC_CORE2_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR4															
RO															
0															

Access Types Legend

Table 4-209. CORE2_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR4	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.86 R5SS0_STC_CORE2_CURMISR_5 Register (Offset = C0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-210. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C0h

Figure 4-96. R5SS0_STC_CORE2_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR5															
RO															
0															

Access Types Legend

Table 4-211. CORE2_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR5	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.87 R5SS0_STC_CORE2_CURMISR_6 Register (Offset = C4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-212. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C4h

Figure 4-97. R5SS0_STC_CORE2_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR6															
RO															
0															

Access Types Legend

Table 4-213. CORE2_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR6	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.88 R5SS0_STC_CORE2_CURMISR_7 Register (Offset = C8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-214. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C8h

Figure 4-98. R5SS0_STC_CORE2_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR7															
RO															
0															

Access Types Legend

Table 4-215. CORE2_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR7	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.89 R5SS0_STC_CORE2_CURMISR_8 Register (Offset = CCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-216. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00CCh

Figure 4-99. R5SS0_STC_CORE2_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR8															
RO															
0															

Access Types Legend

Table 4-217. CORE2_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR8	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.90 R5SS0_STC_CORE2_CURMISR_9 Register (Offset = D0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-218. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D0h

Figure 4-100. R5SS0_STC_CORE2_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR9															
RO															
0															

Access Types Legend

Table 4-219. CORE2_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR9	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.91 R5SS0_STC_CORE2_CURMISR_10 Register (Offset = D4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-220. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D4h

Figure 4-101. R5SS0_STC_CORE2_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR10															
RO															
0															

Access Types Legend

Table 4-221. CORE2_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR10	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.92 R5SS0_STC_CORE2_CURMISR_11 Register (Offset = D8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-222. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D8h

Figure 4-102. R5SS0_STC_CORE2_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR11															
RO															
0															

Access Types Legend

Table 4-223. CORE2_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR11	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.93 R5SS0_STC_CORE2_CURMISR_12 Register (Offset = DCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-224. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00DCh

Figure 4-103. R5SS0_STC_CORE2_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR12															
RO															
0															

Access Types Legend

Table 4-225. CORE2_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR12	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.94 R5SS0_STC_CORE2_CURMISR_13 Register (Offset = E0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-226. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E0h

Figure 4-104. R5SS0_STC_CORE2_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR13															
RO															
0															

Access Types Legend

Table 4-227. CORE2_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR13	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.95 R5SS0_STC_CORE2_CURMISR_14 Register (Offset = E4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-228. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E4h

Figure 4-105. R5SS0_STC_CORE2_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR14															
RO															
0															

Access Types Legend

Table 4-229. CORE2_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR14	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.96 R5SS0_STC_CORE2_CURMISR_15 Register (Offset = E8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-230. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E8h

Figure 4-106. R5SS0_STC_CORE2_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR15															
RO															
0															

Access Types Legend

Table 4-231. CORE2_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR15	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.97 R5SS0_STC_CORE2_CURMISR_16 Register (Offset = ECh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-232. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00ECh

Figure 4-107. R5SS0_STC_CORE2_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR16															
RO															
0															

Access Types Legend

Table 4-233. CORE2_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR16	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.98 R5SS0_STC_CORE2_CURMISR_17 Register (Offset = F0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-234. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F0h

Figure 4-108. R5SS0_STC_CORE2_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR17															
RO															
0															

Access Types Legend

Table 4-235. CORE2_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR17	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.99 R5SS0_STC_CORE2_CURMISR_18 Register (Offset = F4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-236. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F4h

Figure 4-109. R5SS0_STC_CORE2_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR18															
RO															
0															

Access Types Legend

Table 4-237. CORE2_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR18	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.100 R5SS0_STC_CORE2_CURMISR_19 Register (Offset = F8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-238. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F8h

Figure 4-110. R5SS0_STC_CORE2_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR19															
RO															
0															

Access Types Legend

Table 4-239. CORE2_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR19	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.101 R5SS0_STC_CORE2_CURMISR_20 Register (Offset = FCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-240. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00FCh

Figure 4-111. R5SS0_STC_CORE2_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR20															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR20															
RO															
0															

Access Types Legend

Table 4-241. CORE2_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR20	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.102 R5SS0_STC_CORE2_CURMISR_21 Register (Offset = 100h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-242. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0100h

Figure 4-112. R5SS0_STC_CORE2_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR21															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR21															
RO															
0															

Access Types Legend

Table 4-243. CORE2_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR21	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.103 R5SS0_STC_CORE2_CURMISR_22 Register (Offset = 104h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-244. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0104h

Figure 4-113. R5SS0_STC_CORE2_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR22															
RO															
0															

Access Types Legend

Table 4-245. CORE2_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR22	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.104 R5SS0_STC_CORE2_CURMISR_23 Register (Offset = 108h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-246. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0108h

Figure 4-114. R5SS0_STC_CORE2_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR23															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR23															
RO															
0															

Access Types Legend

Table 4-247. CORE2_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR23	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.105 R5SS0_STC_CORE2_CURMISR_24 Register (Offset = 10Ch) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-248. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 010Ch

Figure 4-115. R5SS0_STC_CORE2_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR24															
RO															
0															

Access Types Legend

Table 4-249. CORE2_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR24	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.106 R5SS0_STC_CORE2_CURMISR_25 Register (Offset = 110h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-250. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0110h

Figure 4-116. R5SS0_STC_CORE2_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR25															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR25															
RO															
0															

Access Types Legend

Table 4-251. CORE2_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR25	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.107 R5SS0_STC_CORE2_CURMISR_26 Register (Offset = 114h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-252. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0114h

Figure 4-117. R5SS0_STC_CORE2_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR26															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR26															
RO															
0															

Access Types Legend

Table 4-253. CORE2_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR26	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.108 R5SS0_STC_CORE2_CURMISR_27 Register (Offset = 118h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-254. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0118h

Figure 4-118. R5SS0_STC_CORE2_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR27															
RO															
0															

Access Types Legend

Table 4-255. CORE2_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR27	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.109 R5SS1_STC_STCGCR0 Register (Offset = 0h) [reset = h]

Short Description: Self test Global control Reg0. *NOT BYTE ACCESSIBLE

Long Description:

Return to Summary Table

Table 4-256. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0000h

Figure 4-119. R5SS1_STC_STCGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTCOUNT_B16															
RW															
1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0					CAP_IDLE_CYCLE			SCANEN_HIGH_CAP_IDLE_CYCLE			NU1			RS_CNT_B1	
RO					RW			RW			RO			RW	
0					1			1			0			0	

Access Types Legend

Table 4-257. STCGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	INTCOUNT_B16	RW	1h	Number of intervals of the self test run (RWP - Read, Priviledge Mode Write only)Count of intervals that need to be covered for a specific selftest run.The selftest controller sends out ?complete? indication once it runs all of the intervals programmed in this field.INTCOUNT_B16=0 is an invalid configuration for a selftest.
15 - 11	NU0	RO	0h	Reserved bits
10 - 8	CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only)Idle Cycles before and after capture clock. This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
7 - 5	SCANEN_HIGH_CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only). *NOT BYTE ACCESSIBLEIdle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation. This value is used to insert that many idle cycles in the shift clock (scan_en going high to func_clk_en generation) and misr_log_clk (scan_en going high to misr_log_en generation) generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
4 - 2	NU1	RO	0h	Reserved bits
1 - 0	RS_CNT_B1	RW	0h	Restart/Continue or preload (RWP - Read, Priviledge Mode Write only)This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run.00 = Continue NSTC run from previous interval01 = Restart NSTC run from ROM address 01X = Start from segment number specified in STC_SEGPLR register

4.5.110 R5SS1_STC_STCGCR1 Register (Offset = 4h) [reset = h]

Short Description: Self test Global control Reg1

Long Description:

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Table 4-258. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0004h

Figure 4-120. R5SS1_STC_STCGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2				SEG0_CORE_SEL				NU3	CODEC_SPREAD_MODE	LP_SCAN_MODE	ROM_ACCESS_INV	ST_ENA_B4			
RO				RW				RO	RW	RW	RW	RW			
0				0				0	0	1	0	101			

Access Types Legend

Table 4-259. STCGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RO	0h	Reserved bits
11 - 8	SEG0_CORE_SEL	RW	0h	Selects the Segment0 CORE for self test (RWP - Read, Priviledge Mode Write only)Select the Segment0 CORE for Self -Test0001 = Select CORE for selftestOther = CORE not selected.
7	NU3	RO	0h	Reserved bits
6	CODEC_SPREAD_MODE	RW	0h	Codec Spread Mode control signal (RWP - Read, Priviledge Mode Write only)This bit is used to configure the codec in spread / X-OR mode.1 = Spread mode0 = XOR mode
5	LP_SCAN_MODE	RW	1h	LP scan mode (RWP - Read, Priviledge Mode Write only)This bit is used to decide the scan configuration:1 = Operates in Low Power Scan Mode. 0 = Operates in Normal Scan Mode.
4	ROM_ACCESS_INV	RW	0h	Rom access inversion mode (RWP - Read, Priviledge Mode Write only)- NOT SUPPORTED
3 - 0	ST_ENA_B4	RW	65h	Self test enable key (RWP - Read, Priviledge Mode Write only)1010 = Self test run enabled All values other than 1010 = Self test run disabled

4.5.111 R5SS1_STC_STCTPR Register (Offset = 8h) [reset = h]

Short Description: Time out counter preload register

Long Description:

Return to Summary Table

Table 4-260. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0008h

Figure 4-121. R5SS1_STC_STCTPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO_PRELOAD															
RW															
11111111111111111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_PRELOAD															
RW															
11111111111111111111111111111111															

Access Types Legend

Table 4-261. STCTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_PRELOAD	RW	8C3DEFB1 EDB984FE2 AC71C71C7 h	Self test time out preload (RWP - Read, Priviledge Mode Write only)This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective.This register value (preload count value) gets loaded into the self test timeout down counter whenever a self test run is initiated (ST_ENA is enabled). and gets disabled on completion of a self test run.

4.5.112 R5SS1_STC_STC_CADDR Register (Offset = Ch) [reset = h]

Short Description: Current Address register for CORE1

Long Description:

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Table 4-262. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 000Ch

Figure 4-122. R5SS1_STC_STC_CADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
RO															
0															

Access Types Legend

Table 4-263. STC_CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE1This register reflects the current ROM address (for micro code load) accessed during selftest for CORE1 in of case segment0 and all the remaining segmentsn where n = 1 to 3).

4.5.113 R5SS1_STC_STCCICR Register (Offset = 10h) [reset = h]

Short Description: Current Interval count register

Long Description:

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Table 4-264. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0010h

Figure 4-123. R5SS1_STC_STCCICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CORE2_ICOUNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE1_ICOUNT															
RO															
0															

Access Types Legend

Table 4-265. STCCICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CORE2_ICOUNT	RO	0h	Specifies the last interval number for CORE2This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0.
15 - 0	CORE1_ICOUNT	RO	0h	Specifies the last interval number for CORE1This specifies the Last executed Interval number of a self-test run.

4.5.114 R5SS1_STC_STCGSTAT Register (Offset = 14h) [reset = h]

Short Description: Global Status Register

Long Description:

Return to Summary Table

Table 4-266. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0014h

Figure 4-124. R5SS1_STC_STCGSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4				ST_ACTIVE				NU5						TEST_FAIL	TEST_DONE
RO				RO				RO						RO	RO
0				101				0						0	0

Access Types Legend

Table 4-267. STCGSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU4	RO	0h	Reserved bits
11 - 8	ST_ACTIVE	RO	65h	Tells whether self test is currently active or not.1010 = Self test is activeOthers = SelfTest is not activeOnce the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value.
7 - 2	NU5	RO	0h	Reserved bits
1	TEST_FAIL	RO	0h	Test_fail flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Self test run has not failed1 = SelfTest run has failed. Write Clear.
0	TEST_DONE	RO	0h	Test_done_flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Not completed1 = SelfTest run Completed

4.5.115 R5SS1_STC_STCFSTAT Register (Offset = 18h) [reset = h]

Short Description: Fail Status Register

Long Description:

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Table 4-268. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0018h

Figure 4-125. R5SS1_STC_STCFSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6											FSEG_ID		TO_ER_B1	CPU2_FAIL_B1	CPU1_FAIL_B1
RO											RO		RO	RO	RO
0											0		0	0	0

Access Types Legend

Table 4-269. STCFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU6	RO	0h	Reserved bits
4 - 3	FSEG_ID	RO	0h	Failed Segment ID (RCP - Read, Clear on Writing in Priviledge Mode)This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur.00 = Failure on Segment 001 = Failure on Segment 110 = Failure on Segment 211 = Failure on Segment 3
2	TO_ER_B1	RO	0h	Tells whether self test failed because of time out error (RCP - Read, Clear on Writing in Priviledge Mode)0 = No time out error occurred1 = SelfTest run failed due to a timeout error
1	CPU2_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE2 when in Segment0 mode (RCP - Read, Clear on Writing in Priviledge Mode)0 = No MISR mismatch for CORE21 = Self test run failed due to MISR mismatch for CORE2
0	CPU1_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE1 (RCP - Read, Clear on Writing in Priviledge Mode)Applicable to all segments.0 = No MISR mismatch for CORE11 = Self test run failed due to MISR mismatch for CORE1

4.5.116 R5SS1_STC_STCSCSCR Register (Offset = 1Ch) [reset = h]

Short Description: Signature compare Self Check Register

Long Description:

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Table 4-270. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 001Ch

Figure 4-126. R5SS1_STC_STCSCSCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7											FAULT_INS_B1	SELF_CHECK_KEY_B4			
RO											RW	RW			
0											0	101			

Access Types Legend

Table 4-271. STCSCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU7	RO	0h	Reserved bits
4	FAULT_INS_B1	RW	0h	Fault Insertion bit (RWP - Read, Priviledge Mode Write only)0 = No fault insertion.1 = Inserts fault in the logic unedr test which will make signature compare fail. This feature is used as diagnostic check of the STC IP.
3 - 0	SELF_CHECK_KEY_B4	RW	65h	Signature compare logic self check key enable/disable (RWP - Read, Priviledge Mode Write only)1010 = Signature compare logic Self Check is enabledAll values other than 1010 = Signature compare logic Self Check is disabled

4.5.117 R5SS1_STC_STC_CADDR2 Register (Offset = 20h) [reset = h]

Short Description: Current Address register for CORE2

Long Description:

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Table 4-272. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0020h

Figure 4-127. R5SS1_STC_STC_CADDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
RO															
0															

Access Types Legend

Table 4-273. STC_CADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE2This register reflects the current ROM address(for micro code load) accessed during selftest for CORE2 in of case segment0.

4.5.118 R5SS1_STC_STC_CLKDIV Register (Offset = 24h) [reset = h]

Short Description: Clock Divider Register

Long Description:

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Table 4-274. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0024h

Figure 4-128. R5SS1_STC_STC_CLKDIV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8					CLKDIV0			NU9					CLKDIV1		
RO					RW			RO					RW		
0					0			0					0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10					CLKDIV2			NU11					CLKDIV3		
RO					RW			RO					RW		
0					0			0					0		

Access Types Legend

Table 4-275. STC_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	NU8	RO	0h	Reserved bits
26 - 24	CLKDIV0	RW	0h	Clock division for Seg0 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 0
23 - 19	NU9	RO	0h	Reserved bits
18 - 16	CLKDIV1	RW	0h	Clock division for Seg1 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 1
15 - 11	NU10	RO	0h	Reserved bits
10 - 8	CLKDIV2	RW	0h	Clock division for Seg2 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 2
7 - 3	NU11	RO	0h	Reserved bits
2 - 0	CLKDIV3	RW	0h	Clock division for Seg3 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 3

4.5.119 R5SS1_STC_STC_SEGPLR Register (Offset = 28h) [reset = h]

Short Description: Segment 1st interval Preload Register

Long Description:

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Table 4-276. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0028h

Figure 4-129. R5SS1_STC_STC_SEGPLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														SEGID_PLOAD	
RO														RW	
0														0	

Access Types Legend

Table 4-277. STC_SEGPLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved bits
1 - 0	SEGID_PLOAD	RW	0h	Segment number for which preload is to be started (RWP - Read, Priviledge Mode Write only)This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register.The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X00 = Preload the address of the 1st interval of segment 0.01 = Preload the address of the 1st interval of segment 1.10 = Preload the address of the 1st interval of segment 2.11 = Preload the address of the 1st interval of segment 3.

4.5.120 R5SS1_STC_SEG0_START_ADDR Register (Offset = 2Ch) [reset = h]

Short Description: ROM Start address for Segment0

Long Description:

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Table 4-278. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 002Ch

Figure 4-130. R5SS1_STC_SEG0_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-279. SEG0_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU13	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 0 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR

4.5.121 R5SS1_STC_SEG1_START_ADDR Register (Offset = 30h) [reset = h]

Short Description: ROM Start address for Segment1

Long Description:

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Table 4-280. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0030h

Figure 4-131. R5SS1_STC_SEG1_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-281. SEG1_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU14	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 1 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 1.

4.5.122 R5SS1_STC_SEG2_START_ADDR Register (Offset = 34h) [reset = h]

Short Description: ROM Start address for Segment2

Long Description:

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Table 4-282. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0034h

Figure 4-132. R5SS1_STC_SEG2_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-283. SEG2_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU15	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 2 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 2.

4.5.123 R5SS1_STC_SEG3_START_ADDR Register (Offset = 38h) [reset = h]

Short Description: ROM Start address for Segment3

Long Description:

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Table 4-284. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0038h

Figure 4-133. R5SS1_STC_SEG3_START_ADDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16												SEG_START_ADDR			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEG_START_ADDR															
RW															
0															

Access Types Legend

Table 4-285. SEG3_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU16	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 3 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 3.

4.5.124 R5SS1_STC_CORE1_CURMISR_0 Register (Offset = 3Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

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Table 4-286. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 003Ch

Figure 4-134. R5SS1_STC_CORE1_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR0															
RO															
0															

Access Types Legend

Table 4-287. CORE1_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR0	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.125 R5SS1_STC_CORE1_CURMISR_1 Register (Offset = 40h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

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Table 4-288. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0040h

Figure 4-135. R5SS1_STC_CORE1_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR1															
RO															
0															

Access Types Legend

Table 4-289. CORE1_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR1	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.126 R5SS1_STC_CORE1_CURMISR_2 Register (Offset = 44h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-290. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0044h

Figure 4-136. R5SS1_STC_CORE1_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR2															
RO															
0															

Access Types Legend

Table 4-291. CORE1_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR2	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.127 R5SS1_STC_CORE1_CURMISR_3 Register (Offset = 48h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

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Table 4-292. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0048h

Figure 4-137. R5SS1_STC_CORE1_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR3															
RO															
0															

Access Types Legend

Table 4-293. CORE1_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR3	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.128 R5SS1_STC_CORE1_CURMISR_4 Register (Offset = 4Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-294. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 004Ch

Figure 4-138. R5SS1_STC_CORE1_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR4															
RO															
0															

Access Types Legend

Table 4-295. CORE1_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR4	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.129 R5SS1_STC_CORE1_CURMISR_5 Register (Offset = 50h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-296. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0050h

Figure 4-139. R5SS1_STC_CORE1_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR5															
RO															
0															

Access Types Legend

Table 4-297. CORE1_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR5	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.130 R5SS1_STC_CORE1_CURMISR_6 Register (Offset = 54h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-298. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0054h

Figure 4-140. R5SS1_STC_CORE1_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR6															
RO															
0															

Access Types Legend

Table 4-299. CORE1_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR6	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.131 R5SS1_STC_CORE1_CURMISR_7 Register (Offset = 58h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-300. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0058h

Figure 4-141. R5SS1_STC_CORE1_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR7															
RO															
0															

Access Types Legend

Table 4-301. CORE1_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR7	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.132 R5SS1_STC_CORE1_CURMISR_8 Register (Offset = 5Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-302. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 005Ch

Figure 4-142. R5SS1_STC_CORE1_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR8															
RO															
0															

Access Types Legend

Table 4-303. CORE1_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR8	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.133 R5SS1_STC_CORE1_CURMISR_9 Register (Offset = 60h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-304. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0060h

Figure 4-143. R5SS1_STC_CORE1_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR9															
RO															
0															

Access Types Legend

Table 4-305. CORE1_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR9	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.134 R5SS1_STC_CORE1_CURMISR_10 Register (Offset = 64h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-306. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0064h

Figure 4-144. R5SS1_STC_CORE1_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR10															
RO															
0															

Access Types Legend

Table 4-307. CORE1_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR10	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.135 R5SS1_STC_CORE1_CURMISR_11 Register (Offset = 68h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-308. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0068h

Figure 4-145. R5SS1_STC_CORE1_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR11															
RO															
0															

Access Types Legend

Table 4-309. CORE1_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR11	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.136 R5SS1_STC_CORE1_CURMISR_12 Register (Offset = 6Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-310. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 006Ch

Figure 4-146. R5SS1_STC_CORE1_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR12															
RO															
0															

Access Types Legend

Table 4-311. CORE1_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR12	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.137 R5SS1_STC_CORE1_CURMISR_13 Register (Offset = 70h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-312. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0070h

Figure 4-147. R5SS1_STC_CORE1_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR13															
RO															
0															

Access Types Legend

Table 4-313. CORE1_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR13	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.138 R5SS1_STC_CORE1_CURMISR_14 Register (Offset = 74h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-314. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0074h

Figure 4-148. R5SS1_STC_CORE1_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR14															
RO															
0															

Access Types Legend

Table 4-315. CORE1_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR14	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.139 R5SS1_STC_CORE1_CURMISR_15 Register (Offset = 78h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-316. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0078h

Figure 4-149. R5SS1_STC_CORE1_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR15															
RO															
0															

Access Types Legend

Table 4-317. CORE1_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR15	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.140 R5SS1_STC_CORE1_CURMISR_16 Register (Offset = 7Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-318. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 007Ch

Figure 4-150. R5SS1_STC_CORE1_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR16															
RO															
0															

Access Types Legend

Table 4-319. CORE1_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR16	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.141 R5SS1_STC_CORE1_CURMISR_17 Register (Offset = 80h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-320. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0080h

Figure 4-151. R5SS1_STC_CORE1_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR17															
RO															
0															

Access Types Legend

Table 4-321. CORE1_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR17	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.142 R5SS1_STC_CORE1_CURMISR_18 Register (Offset = 84h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-322. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0084h

Figure 4-152. R5SS1_STC_CORE1_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR18															
RO															
0															

Access Types Legend

Table 4-323. CORE1_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR18	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.143 R5SS1_STC_CORE1_CURMISR_19 Register (Offset = 88h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-324. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0088h

Figure 4-153. R5SS1_STC_CORE1_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR19															
RO															
0															

Access Types Legend

Table 4-325. CORE1_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR19	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.144 R5SS1_STC_CORE1_CURMISR_20 Register (Offset = 8Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-326. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 008Ch

Figure 4-154. R5SS1_STC_CORE1_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR20															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR20															
RO															
0															

Access Types Legend

Table 4-327. CORE1_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR20	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.145 R5SS1_STC_CORE1_CURMISR_21 Register (Offset = 90h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-328. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0090h

Figure 4-155. R5SS1_STC_CORE1_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR21															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR21															
RO															
0															

Access Types Legend

Table 4-329. CORE1_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR21	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.146 R5SS1_STC_CORE1_CURMISR_22 Register (Offset = 94h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-330. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0094h

Figure 4-156. R5SS1_STC_CORE1_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR22															
RO															
0															

Access Types Legend

Table 4-331. CORE1_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR22	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.147 R5SS1_STC_CORE1_CURMISR_23 Register (Offset = 98h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-332. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0098h

Figure 4-157. R5SS1_STC_CORE1_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR23															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR23															
RO															
0															

Access Types Legend

Table 4-333. CORE1_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR23	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.148 R5SS1_STC_CORE1_CURMISR_24 Register (Offset = 9Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-334. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 009Ch

Figure 4-158. R5SS1_STC_CORE1_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR24															
RO															
0															

Access Types Legend

Table 4-335. CORE1_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR24	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.149 R5SS1_STC_CORE1_CURMISR_25 Register (Offset = A0h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-336. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00A0h

Figure 4-159. R5SS1_STC_CORE1_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR25															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR25															
RO															
0															

Access Types Legend

Table 4-337. CORE1_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR25	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.150 R5SS1_STC_CORE1_CURMISR_26 Register (Offset = A4h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-338. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00A4h

Figure 4-160. R5SS1_STC_CORE1_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR26															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR26															
RO															
0															

Access Types Legend

Table 4-339. CORE1_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR26	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.151 R5SS1_STC_CORE1_CURMISR_27 Register (Offset = A8h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-340. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00A8h

Figure 4-161. R5SS1_STC_CORE1_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C1MISR27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1MISR27															
RO															
0															

Access Types Legend

Table 4-341. CORE1_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR27	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.152 R5SS1_STC_CORE2_CURMISR_0 Register (Offset = ACh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-342. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00ACh

Figure 4-162. R5SS1_STC_CORE2_CURMISR_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR0															
RO															
0															

Access Types Legend

Table 4-343. CORE2_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR0	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.153 R5SS1_STC_CORE2_CURMISR_1 Register (Offset = B0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-344. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00B0h

Figure 4-163. R5SS1_STC_CORE2_CURMISR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR1															
RO															
0															

Access Types Legend

Table 4-345. CORE2_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR1	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.154 R5SS1_STC_CORE2_CURMISR_2 Register (Offset = B4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-346. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00B4h

Figure 4-164. R5SS1_STC_CORE2_CURMISR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR2															
RO															
0															

Access Types Legend

Table 4-347. CORE2_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR2	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.155 R5SS1_STC_CORE2_CURMISR_3 Register (Offset = B8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-348. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00B8h

Figure 4-165. R5SS1_STC_CORE2_CURMISR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR3															
RO															
0															

Access Types Legend

Table 4-349. CORE2_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR3	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.156 R5SS1_STC_CORE2_CURMISR_4 Register (Offset = BCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-350. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00BCh

Figure 4-166. R5SS1_STC_CORE2_CURMISR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR4															
RO															
0															

Access Types Legend

Table 4-351. CORE2_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR4	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.157 R5SS1_STC_CORE2_CURMISR_5 Register (Offset = C0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-352. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00C0h

Figure 4-167. R5SS1_STC_CORE2_CURMISR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR5															
RO															
0															

Access Types Legend

Table 4-353. CORE2_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR5	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.158 R5SS1_STC_CORE2_CURMISR_6 Register (Offset = C4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-354. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00C4h

Figure 4-168. R5SS1_STC_CORE2_CURMISR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR6															
RO															
0															

Access Types Legend

Table 4-355. CORE2_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR6	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.159 R5SS1_STC_CORE2_CURMISR_7 Register (Offset = C8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-356. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00C8h

Figure 4-169. R5SS1_STC_CORE2_CURMISR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR7															
RO															
0															

Access Types Legend

Table 4-357. CORE2_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR7	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.160 R5SS1_STC_CORE2_CURMISR_8 Register (Offset = CCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-358. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00CCh

Figure 4-170. R5SS1_STC_CORE2_CURMISR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR8															
RO															
0															

Access Types Legend

Table 4-359. CORE2_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR8	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.161 R5SS1_STC_CORE2_CURMISR_9 Register (Offset = D0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-360. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00D0h

Figure 4-171. R5SS1_STC_CORE2_CURMISR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR9															
RO															
0															

Access Types Legend

Table 4-361. CORE2_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR9	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.162 R5SS1_STC_CORE2_CURMISR_10 Register (Offset = D4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-362. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00D4h

Figure 4-172. R5SS1_STC_CORE2_CURMISR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR10															
RO															
0															

Access Types Legend

Table 4-363. CORE2_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR10	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.163 R5SS1_STC_CORE2_CURMISR_11 Register (Offset = D8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-364. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00D8h

Figure 4-173. R5SS1_STC_CORE2_CURMISR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR11															
RO															
0															

Access Types Legend

Table 4-365. CORE2_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR11	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.164 R5SS1_STC_CORE2_CURMISR_12 Register (Offset = DCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-366. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00DCh

Figure 4-174. R5SS1_STC_CORE2_CURMISR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR12															
RO															
0															

Access Types Legend

Table 4-367. CORE2_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR12	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.165 R5SS1_STC_CORE2_CURMISR_13 Register (Offset = E0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-368. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00E0h

Figure 4-175. R5SS1_STC_CORE2_CURMISR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR13															
RO															
0															

Access Types Legend

Table 4-369. CORE2_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR13	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.166 R5SS1_STC_CORE2_CURMISR_14 Register (Offset = E4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-370. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00E4h

Figure 4-176. R5SS1_STC_CORE2_CURMISR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR14															
RO															
0															

Access Types Legend

Table 4-371. CORE2_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR14	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.167 R5SS1_STC_CORE2_CURMISR_15 Register (Offset = E8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-372. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00E8h

Figure 4-177. R5SS1_STC_CORE2_CURMISR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR15															
RO															
0															

Access Types Legend

Table 4-373. CORE2_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR15	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.168 R5SS1_STC_CORE2_CURMISR_16 Register (Offset = ECh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-374. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00ECh

Figure 4-178. R5SS1_STC_CORE2_CURMISR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR16															
RO															
0															

Access Types Legend

Table 4-375. CORE2_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR16	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.169 R5SS1_STC_CORE2_CURMISR_17 Register (Offset = F0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-376. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00F0h

Figure 4-179. R5SS1_STC_CORE2_CURMISR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR17															
RO															
0															

Access Types Legend

Table 4-377. CORE2_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR17	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.170 R5SS1_STC_CORE2_CURMISR_18 Register (Offset = F4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-378. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00F4h

Figure 4-180. R5SS1_STC_CORE2_CURMISR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR18															
RO															
0															

Access Types Legend

Table 4-379. CORE2_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR18	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.171 R5SS1_STC_CORE2_CURMISR_19 Register (Offset = F8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-380. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00F8h

Figure 4-181. R5SS1_STC_CORE2_CURMISR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR19															
RO															
0															

Access Types Legend

Table 4-381. CORE2_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR19	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.172 R5SS1_STC_CORE2_CURMISR_20 Register (Offset = FCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-382. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 00FCh

Figure 4-182. R5SS1_STC_CORE2_CURMISR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR20															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR20															
RO															
0															

Access Types Legend

Table 4-383. CORE2_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR20	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.173 R5SS1_STC_CORE2_CURMISR_21 Register (Offset = 100h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-384. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0100h

Figure 4-183. R5SS1_STC_CORE2_CURMISR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR21															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR21															
RO															
0															

Access Types Legend

Table 4-385. CORE2_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR21	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.174 R5SS1_STC_CORE2_CURMISR_22 Register (Offset = 104h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-386. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0104h

Figure 4-184. R5SS1_STC_CORE2_CURMISR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR22															
RO															
0															

Access Types Legend

Table 4-387. CORE2_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR22	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.175 R5SS1_STC_CORE2_CURMISR_23 Register (Offset = 108h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-388. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0108h

Figure 4-185. R5SS1_STC_CORE2_CURMISR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR23															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR23															
RO															
0															

Access Types Legend

Table 4-389. CORE2_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR23	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.176 R5SS1_STC_CORE2_CURMISR_24 Register (Offset = 10Ch) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-390. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 010Ch

Figure 4-186. R5SS1_STC_CORE2_CURMISR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR24															
RO															
0															

Access Types Legend

Table 4-391. CORE2_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR24	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.177 R5SS1_STC_CORE2_CURMISR_25 Register (Offset = 110h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-392. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0110h

Figure 4-187. R5SS1_STC_CORE2_CURMISR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR25															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR25															
RO															
0															

Access Types Legend

Table 4-393. CORE2_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR25	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.178 R5SS1_STC_CORE2_CURMISR_26 Register (Offset = 114h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-394. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0114h

Figure 4-188. R5SS1_STC_CORE2_CURMISR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR26															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR26															
RO															
0															

Access Types Legend

Table 4-395. CORE2_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR26	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.5.179 R5SS1_STC_CORE2_CURMISR_27 Register (Offset = 118h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-396. Instance Table

Instance Name	Physical Address
R5SS1_STC	5351 0118h

Figure 4-189. R5SS1_STC_CORE2_CURMISR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2MISR27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2MISR27															
RO															
0															

Access Types Legend

Table 4-397. CORE2_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR27	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

Table 4-398. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined

4.6 MSS_CPSW Registers

Table 4-399. CPSW0, CPSW0_CPSW Registers, Base Address=5280 0000H, Length=2

Offset	Length	Acronym	Register Name	CPSW0 Physical Address
0h	32	CPSW0_CPSW_NUSS_IDVER_REG	ID Version Register	5280 0000h
4h	32	CPSW0_SS_SYNCE_COUNT_REG	SS SYNCE Count Register	5280 0004h
8h	8	CPSW0_SS_SYNCE_MUX_REG	SS Synce Mux Register	5280 0008h
Ch	8	CPSW0_SS_CONTROL_REG	SS Control Register	5280 000Ch
18h	32	CPSW0_SS_INT_CONTROL_REG	SS Interrupt Control Register	5280 0018h
1Ch	0	CPSW0_SS_STATUS_REG	SS Status Register	5280 001Ch
20h	32	CPSW0_SUBSYSTEM_CONFIG_REG	Subsystem Configuration Register	5280 0020h
30h	8	CPSW0_RGMII1_STATUS_REG	RGMII1 Status Register	5280 0030h
34h	8	CPSW0_RGMII2_STATUS_REG	RGMII2 Status Register	5280 0034h

Table 4-400. CPSW0, CPSW0_CPSW Registers, Base Address=5280 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	CPSW0_CPSW_NUSS_IDVER_REG	ID Version Register
4h	32	CPSW0_SS_SYNCE_COUNT_REG	SS SYNCE Count Register
8h	8	CPSW0_SS_SYNCE_MUX_REG	SS Synce Mux Register
Ch	8	CPSW0_SS_CONTROL_REG	SS Control Register
18h	32	CPSW0_SS_INT_CONTROL_REG	SS Interrupt Control Register
1Ch	0	CPSW0_SS_STATUS_REG	SS Status Register
20h	32	CPSW0_SUBSYSTEM_CONFIG_REG	Subsystem Configuration Register
30h	8	CPSW0_RGMII1_STATUS_REG	RGMII1 Status Register
34h	8	CPSW0_RGMII2_STATUS_REG	RGMII2 Status Register

Table 4-401. CPSW0, CPSW0_CPSW Registers, Base Address=5280 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	CPSW0_CPSW_NUSS_IDVER_REG	ID Version Register
4h	32	CPSW0_SS_SYNCE_COUNT_REG	SS SYNCE Count Register
8h	8	CPSW0_SS_SYNCE_MUX_REG	SS Synce Mux Register
Ch	8	CPSW0_SS_CONTROL_REG	SS Control Register
18h	32	CPSW0_SS_INT_CONTROL_REG	SS Interrupt Control Register
1Ch	0	CPSW0_SS_STATUS_REG	SS Status Register
20h	32	CPSW0_SUBSYSTEM_CONFIG_REG	Subsystem Configuration Register
30h	8	CPSW0_RGMII1_STATUS_REG	RGMII1 Status Register
34h	8	CPSW0_RGMII2_STATUS_REG	RGMII2 Status Register

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
0h	32	TPCC0_PID	Peripheral ID Register	52A0 0000h
4h	32	TPCC0_CCCFG	CC Configuration Register	52A0 0004h
200h	32	TPCC0_QCHMAPN	QDMA Channel N Mapping Register	52A0 0200h
240h	32	TPCC0_DMAQNUMN	DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.	52A0 0240h
260h	32	TPCC0_QDMAQNUM	QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.	52A0 0260h
280h	32	TPCC0_QUETCMAP	Queue to TC Mapping	52A0 0280h
284h	32	TPCC0_QUEPRI	Queue Priority	52A0 0284h
300h	32	TPCC0_EMR	Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	52A0 0300h
304h	32	TPCC0_EMRH	Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	52A0 0304h
308h	32	TPCC0_EMCR	Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	52A0 0308h
30Ch	32	TPCC0_EMCRH	Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	52A0 030Ch

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
310h	32	TPCC0_QEMR	QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	52A0 0310h
314h	32	TPCC0_QEMCR	QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	52A0 0314h
318h	32	TPCC0_CCERR	CC Error Register	52A0 0318h
31Ch	32	TPCC0_CCERRCLR	CC Error Clear Register	52A0 031Ch
320h	32	TPCC0_EEVAL	Error Eval Register	52A0 0320h
340h	32	TPCC0_DRAEM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.	52A0 0340h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
344h	32	TPCC0_DRAEHM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.	52A0 0344h
380h	32	TPCC0_QRAEN	QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.	52A0 0380h
400h	32	TPCC0_QNE0	Event Queue Entry Diagram for Queue n - Entry 0	52A0 0400h
404h	32	TPCC0_QNE1	Event Queue Entry Diagram for Queue n - Entry 1	52A0 0404h
408h	32	TPCC0_QNE2	Event Queue Entry Diagram for Queue n - Entry 2	52A0 0408h
40Ch	32	TPCC0_QNE3	Event Queue Entry Diagram for Queue n - Entry 3	52A0 040Ch
410h	32	TPCC0_QNE4	Event Queue Entry Diagram for Queue n - Entry 4	52A0 0410h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
414h	32	TPCC0_QNE5	Event Queue Entry Diagram for Queue n - Entry 5	52A0 0414h
418h	32	TPCC0_QNE6	Event Queue Entry Diagram for Queue n - Entry 6	52A0 0418h
41Ch	32	TPCC0_QNE7	Event Queue Entry Diagram for Queue n - Entry 7	52A0 041Ch
420h	32	TPCC0_QNE8	Event Queue Entry Diagram for Queue n - Entry 8	52A0 0420h
424h	32	TPCC0_QNE9	Event Queue Entry Diagram for Queue n - Entry 9	52A0 0424h
428h	32	TPCC0_QNE10	Event Queue Entry Diagram for Queue n - Entry 0	52A0 0428h
42Ch	32	TPCC0_QNE11	Event Queue Entry Diagram for Queue n - Entry 11	52A0 042Ch
430h	32	TPCC0_QNE12	Event Queue Entry Diagram for Queue n - Entry 12	52A0 0430h
434h	32	TPCC0_QNE13	Event Queue Entry Diagram for Queue n - Entry 13	52A0 0434h
438h	32	TPCC0_QNE14	Event Queue Entry Diagram for Queue n - Entry 14	52A0 0438h
43Ch	32	TPCC0_QNE15	Event Queue Entry Diagram for Queue n - Entry 15	52A0 043Ch
600h	32	TPCC0_QSTATN	QSTATn Register Set	52A0 0600h
620h	32	TPCC0_QWMTHRA	Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.	52A0 0620h
640h	32	TPCC0_CCSTAT	CC Status Register	52A0 0640h
700h	32	TPCC0_AETCTL	Advanced Event Trigger Control	52A0 0700h
704h	32	TPCC0_AETSTAT	Advanced Event Trigger Stat	52A0 0704h
708h	32	TPCC0_AETCMD	AET Command	52A0 0708h
1000h	32	TPCC0_ER	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.	52A0 1000h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
1004h	32	TPCC0_ERH	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.	52A0 1004h
1008h	32	TPCC0_ECR	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.	52A0 1008h
100Ch	32	TPCC0_ECRH	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.	52A0 100Ch
1010h	32	TPCC0_ESR	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.	52A0 1010h
1014h	32	TPCC0_ESRH	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.	52A0 1014h
1018h	32	TPCC0_CER	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.	52A0 1018h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
101Ch	32	TPCC0_CERH	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.	52A0 101Ch
1020h	32	TPCC0_EER	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.	52A0 1020h
1024h	32	TPCC0_EERH	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.	52A0 1024h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
1028h	32	TPCC0_EECR	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..	52A0 1028h
102Ch	32	TPCC0_EECRH	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..	52A0 102Ch
1030h	32	TPCC0_EESR	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..	52A0 1030h
1034h	32	TPCC0_EESRH	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..	52A0 1034h
1038h	32	TPCC0_SER	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 1038h
103Ch	32	TPCC0_SERH	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 103Ch
1040h	32	TPCC0_SECR	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.	52A0 1040h
1044h	32	TPCC0_SECRH	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.	52A0 1044h
1050h	32	TPCC0_IER	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.	52A0 1050h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
1054h	32	TPCC0_IERH	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.	52A0 1054h
1058h	32	TPCC0_IECR	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..	52A0 1058h
105Ch	32	TPCC0_IECRH	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..	52A0 105Ch
1060h	32	TPCC0_IESR	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..	52A0 1060h
1064h	32	TPCC0_IESRH	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..	52A0 1064h
1068h	32	TPCC0_IPR	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.	52A0 1068h
106Ch	32	TPCC0_IPRH	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.	52A0 106Ch
1070h	32	TPCC0_ICR	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.	52A0 1070h
1074h	32	TPCC0_ICRH	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.	52A0 1074h
1078h	32	TPCC0_IEVAL	Interrupt Eval Register	52A0 1078h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
1080h	32	TPCC0_QER	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.	52A0 1080h
1084h	32	TPCC0_QEER	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.	52A0 1084h
1088h	32	TPCC0_QEECR	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..	52A0 1088h
108Ch	32	TPCC0_QEESR	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..	52A0 108Ch
1090h	32	TPCC0_QSER	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 1090h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
1094h	32	TPCC0_QSECR	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..	52A0 1094h
2000h	32	TPCC0_ER_RN	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.	52A0 2000h
2004h	32	TPCC0_ERH_RN	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.	52A0 2004h
2008h	32	TPCC0_ECR_RN	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.	52A0 2008h
200Ch	32	TPCC0_ECRH_RN	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.	52A0 200Ch

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
2010h	32	TPCC0_ESR_RN	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.	52A0 2010h
2014h	32	TPCC0_ESRH_RN	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.	52A0 2014h
2018h	32	TPCC0_CER_RN	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.	52A0 2018h
201Ch	32	TPCC0_CERH_RN	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.	52A0 201Ch

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
2020h	32	TPCC0_EER_RN	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.	52A0 2020h
2024h	32	TPCC0_EERH_RN	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.	52A0 2024h
2028h	32	TPCC0_EECR_RN	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..	52A0 2028h
202Ch	32	TPCC0_EECRH_RN	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..	52A0 202Ch
2030h	32	TPCC0_EESR_RN	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..	52A0 2030h
2034h	32	TPCC0_EESRH_RN	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..	52A0 2034h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
2038h	32	TPCC0_SER_RN	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 2038h
203Ch	32	TPCC0_SERH_RN	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 203Ch
2040h	32	TPCC0_SECR_RN	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.	52A0 2040h
2044h	32	TPCC0_SECRH_RN	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.	52A0 2044h
2050h	32	TPCC0_IER_RN	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.	52A0 2050h
2054h	32	TPCC0_IERH_RN	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.	52A0 2054h
2058h	32	TPCC0_IECR_RN	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..	52A0 2058h
205Ch	32	TPCC0_IECRH_RN	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..	52A0 205Ch

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
2060h	32	TPCC0_IESR_RN	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..	52A0 2060h
2064h	32	TPCC0_IESRH_RN	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..	52A0 2064h
2068h	32	TPCC0_IPR_RN	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.	52A0 2068h
206Ch	32	TPCC0_IPRH_RN	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.	52A0 206Ch
2070h	32	TPCC0_ICR_RN	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.	52A0 2070h
2074h	32	TPCC0_ICRH_RN	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.	52A0 2074h
2078h	32	TPCC0_IEVAL_RN	Interrupt Eval Register	52A0 2078h
2080h	32	TPCC0_QER_RN	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.	52A0 2080h

Table 4-402. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TPCC0 Physical Address
2084h	32	TPCC0_QEER_RN	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.	52A0 2084h
2088h	32	TPCC0_QEECR_RN	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..	52A0 2088h
208Ch	32	TPCC0_QEESR_RN	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..	52A0 208Ch
2090h	32	TPCC0_QSER_RN	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	52A0 2090h
2094h	32	TPCC0_QSECR_RN	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..	52A0 2094h
4000h	32	TPCC0_OPT	Options Parameter	52A0 4000h
4004h	32	TPCC0_SRC	Source Address	52A0 4004h
4008h	32	TPCC0_ABCNT	A and B byte count	52A0 4008h
400Ch	32	TPCC0_DST	Destination Address	52A0 400Ch
4010h	32	TPCC0_BIDX	Register description is not available	52A0 4010h
4014h	32	TPCC0_LNK	Link and Reload parameters	52A0 4014h
4018h	32	TPCC0_CIDX	Register description is not available	52A0 4018h
401Ch	32	TPCC0_CCNT	C byte count	52A0 401Ch

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1

Offset	Length	Acronym	Register Name
0h	32	TPCC0_PID	Peripheral ID Register
4h	32	TPCC0_CCCFG	CC Configuration Register
200h	32	TPCC0_QCHMAPN	QDMA Channel N Mapping Register
240h	32	TPCC0_DMAQNUMN	DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.
260h	32	TPCC0_QDMAQNUM	QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.
280h	32	TPCC0_QUETCMAP	Queue to TC Mapping
284h	32	TPCC0_QUEPRI	Queue Priority
300h	32	TPCC0_EMR	Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
304h	32	TPCC0_EMRH	Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
308h	32	TPCC0_EMCR	Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
30Ch	32	TPCC0_EMCRH	Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
310h	32	TPCC0_QEMR	QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
314h	32	TPCC0_QEMCR	QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
318h	32	TPCC0_CCERR	CC Error Register
31Ch	32	TPCC0_CCERRCLR	CC Error Clear Register
320h	32	TPCC0_EEVAL	Error Eval Register
340h	32	TPCC0_DRAEM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
344h	32	TPCC0_DRAEHM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.
380h	32	TPCC0_QRAEN	QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.
400h	32	TPCC0_QNE0	Event Queue Entry Diagram for Queue n - Entry 0
404h	32	TPCC0_QNE1	Event Queue Entry Diagram for Queue n - Entry 1
408h	32	TPCC0_QNE2	Event Queue Entry Diagram for Queue n - Entry 2
40Ch	32	TPCC0_QNE3	Event Queue Entry Diagram for Queue n - Entry 3

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
410h	32	TPCC0_QNE4	Event Queue Entry Diagram for Queue n - Entry 4
414h	32	TPCC0_QNE5	Event Queue Entry Diagram for Queue n - Entry 5
418h	32	TPCC0_QNE6	Event Queue Entry Diagram for Queue n - Entry 6
41Ch	32	TPCC0_QNE7	Event Queue Entry Diagram for Queue n - Entry 7
420h	32	TPCC0_QNE8	Event Queue Entry Diagram for Queue n - Entry 8
424h	32	TPCC0_QNE9	Event Queue Entry Diagram for Queue n - Entry 9
428h	32	TPCC0_QNE10	Event Queue Entry Diagram for Queue n - Entry 0
42Ch	32	TPCC0_QNE11	Event Queue Entry Diagram for Queue n - Entry 11
430h	32	TPCC0_QNE12	Event Queue Entry Diagram for Queue n - Entry 12
434h	32	TPCC0_QNE13	Event Queue Entry Diagram for Queue n - Entry 13
438h	32	TPCC0_QNE14	Event Queue Entry Diagram for Queue n - Entry 14
43Ch	32	TPCC0_QNE15	Event Queue Entry Diagram for Queue n - Entry 15
600h	32	TPCC0_QSTATN	QSTATn Register Set
620h	32	TPCC0_QWMTHRA	Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.
640h	32	TPCC0_CCSTAT	CC Status Register
700h	32	TPCC0_AETCTL	Advanced Event Trigger Control
704h	32	TPCC0_AETSTAT	Advanced Event Trigger Stat
708h	32	TPCC0_AETCMD	AET Command

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1000h	32	TPCC0_ER	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.
1004h	32	TPCC0_ERH	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.
1008h	32	TPCC0_ECR	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.
100Ch	32	TPCC0_ECRH	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.
1010h	32	TPCC0_ESR	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.
1014h	32	TPCC0_ESRH	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1018h	32	TPCC0_CER	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.
101Ch	32	TPCC0_CERH	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.
1020h	32	TPCC0_EER	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1024h	32	TPCC0_EERH	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.
1028h	32	TPCC0_EECR	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..
102Ch	32	TPCC0_EECRH	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..
1030h	32	TPCC0_EESR	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..
1034h	32	TPCC0_EESRH	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..
1038h	32	TPCC0_SER	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
103Ch	32	TPCC0_SERH	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1040h	32	TPCC0_SECR	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.
1044h	32	TPCC0_SECRH	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.
1050h	32	TPCC0_IER	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.
1054h	32	TPCC0_IERH	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.
1058h	32	TPCC0_IECR	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..
105Ch	32	TPCC0_IECRH	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..
1060h	32	TPCC0_IESR	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..
1064h	32	TPCC0_IESRH	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..
1068h	32	TPCC0_IPR	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.
106Ch	32	TPCC0_IPRH	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1070h	32	TPCC0_ICR	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.
1074h	32	TPCC0_ICRH	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.
1078h	32	TPCC0_IEVAL	Interrupt Eval Register
1080h	32	TPCC0_QER	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.
1084h	32	TPCC0_QEER	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.
1088h	32	TPCC0_QEECR	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..
108Ch	32	TPCC0_QEESR	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1090h	32	TPCC0_QSER	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
1094h	32	TPCC0_QSECR	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..
2000h	32	TPCC0_ER_RN	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2004h	32	TPCC0_ERH_RN	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.
2008h	32	TPCC0_ECR_RN	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.
200Ch	32	TPCC0_ECRH_RN	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.
2010h	32	TPCC0_ESR_RN	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.
2014h	32	TPCC0_ESRH_RN	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.
2018h	32	TPCC0_CER_RN	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
201Ch	32	TPCC0_CERH_RN	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.
2020h	32	TPCC0_EER_RN	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2024h	32	TPCC0_EERH_RN	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.
2028h	32	TPCC0_EECR_RN	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..
202Ch	32	TPCC0_EECRH_RN	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..
2030h	32	TPCC0_EESR_RN	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..
2034h	32	TPCC0_EESRH_RN	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..
2038h	32	TPCC0_SER_RN	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
203Ch	32	TPCC0_SERH_RN	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2040h	32	TPCC0_SECR_RN	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.
2044h	32	TPCC0_SECRH_RN	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.
2050h	32	TPCC0_IER_RN	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.
2054h	32	TPCC0_IERH_RN	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.
2058h	32	TPCC0_IECR_RN	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..
205Ch	32	TPCC0_IECRH_RN	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..
2060h	32	TPCC0_IESR_RN	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..
2064h	32	TPCC0_IESRH_RN	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..
2068h	32	TPCC0_IPR_RN	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.
206Ch	32	TPCC0_IPRH_RN	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2070h	32	TPCC0_ICR_RN	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.
2074h	32	TPCC0_ICRH_RN	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.
2078h	32	TPCC0_IEVAL_RN	Interrupt Eval Register
2080h	32	TPCC0_QER_RN	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.
2084h	32	TPCC0_QEER_RN	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.
2088h	32	TPCC0_QEECR_RN	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..
208Ch	32	TPCC0_QEESR_RN	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Table 4-403. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2090h	32	TPCC0_QSER_RN	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
2094h	32	TPCC0_QSECR_RN	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..
4000h	32	TPCC0_OPT	Options Parameter
4004h	32	TPCC0_SRC	Source Address
4008h	32	TPCC0_ABCNT	A and B byte count
400Ch	32	TPCC0_DST	Destination Address
4010h	32	TPCC0_BIDX	Register description is not available
4014h	32	TPCC0_LNK	Link and Reload parameters
4018h	32	TPCC0_CIDX	Register description is not available
401Ch	32	TPCC0_CCNT	C byte count

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1

Offset	Length	Acronym	Register Name
0h	32	TPCC0_PID	Peripheral ID Register
4h	32	TPCC0_CCCFG	CC Configuration Register
200h	32	TPCC0_QCHMAPN	QDMA Channel N Mapping Register
240h	32	TPCC0_DMAQNUMN	DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.
260h	32	TPCC0_QDMAQNUM	QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.
280h	32	TPCC0_QUETCMAP	Queue to TC Mapping
284h	32	TPCC0_QUEPRI	Queue Priority

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
300h	32	TPCC0_EMR	Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
304h	32	TPCC0_EMRH	Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
308h	32	TPCC0_EMCR	Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
30Ch	32	TPCC0_EMCRH	Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
310h	32	TPCC0_QEMR	QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.
314h	32	TPCC0_QEMCR	QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
318h	32	TPCC0_CCERR	CC Error Register
31Ch	32	TPCC0_CCERRCLR	CC Error Clear Register
320h	32	TPCC0_EEVAL	Error Eval Register

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
340h	32	TPCC0_DRAEM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.
344h	32	TPCC0_DRAEHM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
380h	32	TPCC0_QRAEN	QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.
400h	32	TPCC0_QNE0	Event Queue Entry Diagram for Queue n - Entry 0
404h	32	TPCC0_QNE1	Event Queue Entry Diagram for Queue n - Entry 1
408h	32	TPCC0_QNE2	Event Queue Entry Diagram for Queue n - Entry 2
40Ch	32	TPCC0_QNE3	Event Queue Entry Diagram for Queue n - Entry 3
410h	32	TPCC0_QNE4	Event Queue Entry Diagram for Queue n - Entry 4
414h	32	TPCC0_QNE5	Event Queue Entry Diagram for Queue n - Entry 5
418h	32	TPCC0_QNE6	Event Queue Entry Diagram for Queue n - Entry 6
41Ch	32	TPCC0_QNE7	Event Queue Entry Diagram for Queue n - Entry 7
420h	32	TPCC0_QNE8	Event Queue Entry Diagram for Queue n - Entry 8
424h	32	TPCC0_QNE9	Event Queue Entry Diagram for Queue n - Entry 9
428h	32	TPCC0_QNE10	Event Queue Entry Diagram for Queue n - Entry 0
42Ch	32	TPCC0_QNE11	Event Queue Entry Diagram for Queue n - Entry 11
430h	32	TPCC0_QNE12	Event Queue Entry Diagram for Queue n - Entry 12
434h	32	TPCC0_QNE13	Event Queue Entry Diagram for Queue n - Entry 13
438h	32	TPCC0_QNE14	Event Queue Entry Diagram for Queue n - Entry 14
43Ch	32	TPCC0_QNE15	Event Queue Entry Diagram for Queue n - Entry 15
600h	32	TPCC0_QSTATN	QSTATn Register Set

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
620h	32	TPCC0_QWMTHRA	Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.
640h	32	TPCC0_CCSTAT	CC Status Register
700h	32	TPCC0_AETCTL	Advanced Event Trigger Control
704h	32	TPCC0_AETSTAT	Advanced Event Trigger Stat
708h	32	TPCC0_AETCMD	AET Command
1000h	32	TPCC0_ER	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.
1004h	32	TPCC0_ERH	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.
1008h	32	TPCC0_ECR	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
100Ch	32	TPCC0_ECRH	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.
1010h	32	TPCC0_ESR	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.
1014h	32	TPCC0_ESRH	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.
1018h	32	TPCC0_CER	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.
101Ch	32	TPCC0_CERH	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1020h	32	TPCC0_EER	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.
1024h	32	TPCC0_EERH	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.
1028h	32	TPCC0_EECR	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..
102Ch	32	TPCC0_EECRH	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..
1030h	32	TPCC0_EESR	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..
1034h	32	TPCC0_EESRH	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1038h	32	TPCC0_SER	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
103Ch	32	TPCC0_SERH	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
1040h	32	TPCC0_SECR	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.
1044h	32	TPCC0_SECRH	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.
1050h	32	TPCC0_IER	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.
1054h	32	TPCC0_IERH	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.
1058h	32	TPCC0_IECR	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..
105Ch	32	TPCC0_IECRH	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1060h	32	TPCC0_IESR	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..
1064h	32	TPCC0_IESRH	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..
1068h	32	TPCC0_IPR	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.
106Ch	32	TPCC0_IPRH	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.
1070h	32	TPCC0_ICR	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.
1074h	32	TPCC0_ICRH	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.
1078h	32	TPCC0_IEVAL	Interrupt Eval Register
1080h	32	TPCC0_QER	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
1084h	32	TPCC0_QEER	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.
1088h	32	TPCC0_QEECR	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..
108Ch	32	TPCC0_QEESR	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..
1090h	32	TPCC0_QSER	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
1094h	32	TPCC0_QSECR	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2000h	32	TPCC0_ER_RN	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.
2004h	32	TPCC0_ERH_RN	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.
2008h	32	TPCC0_ECR_RN	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.
200Ch	32	TPCC0_ECRH_RN	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.
2010h	32	TPCC0_ESR_RN	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.
2014h	32	TPCC0_ESRH_RN	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2018h	32	TPCC0_CER_RN	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.
201Ch	32	TPCC0_CERH_RN	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.
2020h	32	TPCC0_EER_RN	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2024h	32	TPCC0_EERH_RN	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.
2028h	32	TPCC0_EECR_RN	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..
202Ch	32	TPCC0_EECRH_RN	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..
2030h	32	TPCC0_EESR_RN	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..
2034h	32	TPCC0_EESRH_RN	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..
2038h	32	TPCC0_SER_RN	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
203Ch	32	TPCC0_SERH_RN	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2040h	32	TPCC0_SECR_RN	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.
2044h	32	TPCC0_SECRH_RN	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.
2050h	32	TPCC0_IER_RN	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.
2054h	32	TPCC0_IERH_RN	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.
2058h	32	TPCC0_IECR_RN	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..
205Ch	32	TPCC0_IECRH_RN	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..
2060h	32	TPCC0_IESR_RN	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..
2064h	32	TPCC0_IESRH_RN	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..
2068h	32	TPCC0_IPR_RN	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.
206Ch	32	TPCC0_IPRH_RN	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2070h	32	TPCC0_ICR_RN	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.
2074h	32	TPCC0_ICRH_RN	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.
2078h	32	TPCC0_IEVAL_RN	Interrupt Eval Register
2080h	32	TPCC0_QER_RN	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.
2084h	32	TPCC0_QEER_RN	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.
2088h	32	TPCC0_QEECR_RN	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..
208Ch	32	TPCC0_QEESR_RN	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Table 4-404. TPCC0, TPCC0_TPCC Registers, Base Address=52A0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name
2090h	32	TPCC0_QSER_RN	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
2094h	32	TPCC0_QSECR_RN	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..
4000h	32	TPCC0_OPT	Options Parameter
4004h	32	TPCC0_SRC	Source Address
4008h	32	TPCC0_ABCNT	A and B byte count
400Ch	32	TPCC0_DST	Destination Address
4010h	32	TPCC0_BIDX	Register description is not available
4014h	32	TPCC0_LNK	Link and Reload parameters
4018h	32	TPCC0_CIDX	Register description is not available
401Ch	32	TPCC0_CCNT	C byte count

Table 4-405. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8

Offset	Length	Acronym	Register Name	TPTC00 Physical Address	TPTC01 Physical Address
0h	32	TPTC00_PID	Peripheral ID Register	52A4 0000h	52A6 0000h
4h	16	TPTC00_TCCFG	TC Configuration Register	52A4 0004h	52A6 0004h
100h	16	TPTC00_TCSTAT	TC Status Register	52A4 0100h	52A6 0100h
104h	8	TPTC00_INTSTAT	Interrupt Status Register	52A4 0104h	52A6 0104h
108h	8	TPTC00_INTEN	Interrupt Enable Register	52A4 0108h	52A6 0108h
10Ch	8	TPTC00_INTCLR	Interrupt Clear Register	52A4 010Ch	52A6 010Ch
110h	8	TPTC00_INTCMD	Interrupt Command Register	52A4 0110h	52A6 0110h
120h	8	TPTC00_ERRSTAT	Error Status Register	52A4 0120h	52A6 0120h
124h	8	TPTC00_ERREN	Error Enable Register	52A4 0124h	52A6 0124h
128h	8	TPTC00_ERRCLR	Error Clear Register	52A4 0128h	52A6 0128h
12Ch	24	TPTC00_ERRDET	Error Details Register	52A4 012Ch	52A6 012Ch
130h	8	TPTC00_ERRCMD	Error Command Register	52A4 0130h	52A6 0130h
140h	8	TPTC00_RDRATE	Read Rate Register	52A4 0140h	52A6 0140h
200h	32	TPTC00_POPT	Prog Set Options	52A4 0200h	52A6 0200h
204h	32	TPTC00_PSRC	Prog Set Src Address	52A4 0204h	52A6 0204h

Table 4-405. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name	TPTC00 Physical Address	TPTC01 Physical Address
208h	32	TPTC00_PCNT	Prog Set Count	52A4 0208h	52A6 0208h
20Ch	32	TPTC00_PDST	Prog Set Dst Address	52A4 020Ch	52A6 020Ch
210h	32	TPTC00_PBIDX	Prog Set B-Dim Idx	52A4 0210h	52A6 0210h
214h	16	TPTC00_PMPPRXY	Prog Set Mem Protect Proxy	52A4 0214h	52A6 0214h
240h	32	TPTC00_SAOPT	Src Actv Set Options	52A4 0240h	52A6 0240h
244h	32	TPTC00_SASRC	Src Actv Set Src Address	52A4 0244h	52A6 0244h
248h	24	TPTC00_SACNT	Src Actv Set A-Count	52A4 0248h	52A6 0248h
24Ch	32	TPTC00_SADST	Src Actv Set Dst Address	52A4 024Ch	52A6 024Ch
250h	32	TPTC00_SABIDX	Src Actv Set B-Dim Idx	52A4 0250h	52A6 0250h
254h	16	TPTC00_SAMPPRXY	Src Actv Set Mem Protect Proxy	52A4 0254h	52A6 0254h
258h	16	TPTC00_SACNTRLD	Src Actv Set Cnt Reload	52A4 0258h	52A6 0258h
25Ch	32	TPTC00_SASRCBREF	Src Actv Set Src Addr B-Reference	52A4 025Ch	52A6 025Ch
260h	32	TPTC00_SADSTBREF	Src Actv Set Dst Addr B-Reference	52A4 0260h	52A6 0260h
264h	16	TPTC00_SABCNT	Src Actv Set B-Count	52A4 0264h	52A6 0264h
280h	16	TPTC00_DFCNTRLD	Dst FIFO Set Cnt Reload	52A4 0280h	52A6 0280h
284h	32	TPTC00_DFSRCBREF	Dst FIFO Set Src Addr B-Reference	52A4 0284h	52A6 0284h
300h	32	TPTC00_DFOPT0	Dst FIFO Set Options	52A4 0300h	52A6 0300h
304h	32	TPTC00_DFSRC0	Dst FIFO Set Src Address	52A4 0304h	52A6 0304h
308h	24	TPTC00_DFACNT0	Dst FIFO Set A-Count	52A4 0308h	52A6 0308h
30Ch	32	TPTC00_DFDST0	Dst FIFO Set Dst Address	52A4 030Ch	52A6 030Ch
310h	32	TPTC00_DFBIDX0	Dst FIFO Set B-Dim Idx	52A4 0310h	52A6 0310h
314h	16	TPTC00_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy	52A4 0314h	52A6 0314h
318h	16	TPTC00_DFBCNT0	Dst FIFO Set B-Count	52A4 0318h	52A6 0318h
340h	32	TPTC00_DFOPT1	Dst FIFO Set Options	52A4 0340h	52A6 0340h
344h	32	TPTC00_DFSRC1	Dst FIFO Set Src Address	52A4 0344h	52A6 0344h
348h	24	TPTC00_DFACNT1	Dst FIFO Set A-Count	52A4 0348h	52A6 0348h
34Ch	32	TPTC00_DFDST1	Dst FIFO Set Dst Address	52A4 034Ch	52A6 034Ch
350h	32	TPTC00_DFBIDX1	Dst FIFO Set B-Dim Idx	52A4 0350h	52A6 0350h
354h	16	TPTC00_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy	52A4 0354h	52A6 0354h
358h	16	TPTC00_DFBCNT1	Dst FIFO Set B-Count	52A4 0358h	52A6 0358h

Table 4-406. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8

Offset	Length	Acronym	Register Name
0h	32	TPTC00_PID	Peripheral ID Register
4h	16	TPTC00_TCCFG	TC Configuration Register
100h	16	TPTC00_TCSTAT	TC Status Register
104h	8	TPTC00_INTSTAT	Interrupt Status Register
108h	8	TPTC00_INTEN	Interrupt Enable Register
10Ch	8	TPTC00_INTCLR	Interrupt Clear Register
110h	8	TPTC00_INTCMD	Interrupt Command Register

Table 4-406. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name
120h	8	TPTC00_ERRSTAT	Error Status Register
124h	8	TPTC00_ERREN	Error Enable Register
128h	8	TPTC00_ERRCLR	Error Clear Register
12Ch	24	TPTC00_ERRDET	Error Details Register
130h	8	TPTC00_ERRCMD	Error Command Register
140h	8	TPTC00_RDRATE	Read Rate Register
200h	32	TPTC00_POPT	Prog Set Options
204h	32	TPTC00_PSRC	Prog Set Src Address
208h	32	TPTC00_PCNT	Prog Set Count
20Ch	32	TPTC00_PDST	Prog Set Dst Address
210h	32	TPTC00_PBIDX	Prog Set B-Dim Idx
214h	16	TPTC00_PMPPRXY	Prog Set Mem Protect Proxy
240h	32	TPTC00_SAOPT	Src Actv Set Options
244h	32	TPTC00_SASRC	Src Actv Set Src Address
248h	24	TPTC00_SACNT	Src Actv Set A-Count
24Ch	32	TPTC00_SADST	Src Actv Set Dst Address
250h	32	TPTC00_SABIDX	Src Actv Set B-Dim Idx
254h	16	TPTC00_SAMPPRXY	Src Actv Set Mem Protect Proxy
258h	16	TPTC00_SACNTRLD	Src Actv Set Cnt Reload
25Ch	32	TPTC00_SASRCBREF	Src Actv Set Src Addr B-Reference
260h	32	TPTC00_SADSTBREF	Src Actv Set Dst Addr B-Reference
264h	16	TPTC00_SABCNT	Src Actv Set B-Count
280h	16	TPTC00_DFCNTRLD	Dst FIFO Set Cnt Reload
284h	32	TPTC00_DFSRCBREF	Dst FIFO Set Src Addr B-Reference
300h	32	TPTC00_DFOPT0	Dst FIFO Set Options
304h	32	TPTC00_DFSRC0	Dst FIFO Set Src Address
308h	24	TPTC00_DFACNT0	Dst FIFO Set A-Count
30Ch	32	TPTC00_DFDST0	Dst FIFO Set Dst Address
310h	32	TPTC00_DFBIDX0	Dst FIFO Set B-Dim Idx
314h	16	TPTC00_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy
318h	16	TPTC00_DFBCNT0	Dst FIFO Set B-Count
340h	32	TPTC00_DFOPT1	Dst FIFO Set Options
344h	32	TPTC00_DFSRC1	Dst FIFO Set Src Address
348h	24	TPTC00_DFACNT1	Dst FIFO Set A-Count
34Ch	32	TPTC00_DFDST1	Dst FIFO Set Dst Address
350h	32	TPTC00_DFBIDX1	Dst FIFO Set B-Dim Idx
354h	16	TPTC00_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy
358h	16	TPTC00_DFBCNT1	Dst FIFO Set B-Count

Table 4-407. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8

Offset	Length	Acronym	Register Name
0h	32	TPTC00_PID	Peripheral ID Register
4h	16	TPTC00_TCCFG	TC Configuration Register

Table 4-407. TPTC00, TPTC00_TPTC Registers, Base Address=52A4 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name
100h	16	TPTC00_TCSTAT	TC Status Register
104h	8	TPTC00_INTSTAT	Interrupt Status Register
108h	8	TPTC00_INTEN	Interrupt Enable Register
10Ch	8	TPTC00_INTCLR	Interrupt Clear Register
110h	8	TPTC00_INTCMD	Interrupt Command Register
120h	8	TPTC00_ERRSTAT	Error Status Register
124h	8	TPTC00_ERREN	Error Enable Register
128h	8	TPTC00_ERRCLR	Error Clear Register
12Ch	24	TPTC00_ERRDET	Error Details Register
130h	8	TPTC00_ERRCMD	Error Command Register
140h	8	TPTC00_RDRATE	Read Rate Register
200h	32	TPTC00_POPT	Prog Set Options
204h	32	TPTC00_PSRC	Prog Set Src Address
208h	32	TPTC00_PCNT	Prog Set Count
20Ch	32	TPTC00_PDST	Prog Set Dst Address
210h	32	TPTC00_PBIDX	Prog Set B-Dim Idx
214h	16	TPTC00_PMPPRXY	Prog Set Mem Protect Proxy
240h	32	TPTC00_SAOPT	Src Actv Set Options
244h	32	TPTC00_SASRC	Src Actv Set Src Address
248h	24	TPTC00_SACNT	Src Actv Set A-Count
24Ch	32	TPTC00_SADST	Src Actv Set Dst Address
250h	32	TPTC00_SABIDX	Src Actv Set B-Dim Idx
254h	16	TPTC00_SAMPPRXY	Src Actv Set Mem Protect Proxy
258h	16	TPTC00_SACNTRLD	Src Actv Set Cnt Reload
25Ch	32	TPTC00_SASRCBREF	Src Actv Set Src Addr B-Reference
260h	32	TPTC00_SADSTBREF	Src Actv Set Dst Addr B-Reference
264h	16	TPTC00_SABCNT	Src Actv Set B-Count
280h	16	TPTC00_DFCNTRLD	Dst FIFO Set Cnt Reload
284h	32	TPTC00_DFSRCBREF	Dst FIFO Set Src Addr B-Reference
300h	32	TPTC00_DFOPT0	Dst FIFO Set Options
304h	32	TPTC00_DFSRC0	Dst FIFO Set Src Address
308h	24	TPTC00_DFACNT0	Dst FIFO Set A-Count
30Ch	32	TPTC00_DFDST0	Dst FIFO Set Dst Address
310h	32	TPTC00_DFBIDX0	Dst FIFO Set B-Dim Idx
314h	16	TPTC00_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy
318h	16	TPTC00_DFBCNT0	Dst FIFO Set B-Count
340h	32	TPTC00_DFOPT1	Dst FIFO Set Options
344h	32	TPTC00_DFSRC1	Dst FIFO Set Src Address
348h	24	TPTC00_DFACNT1	Dst FIFO Set A-Count
34Ch	32	TPTC00_DFDST1	Dst FIFO Set Dst Address
350h	32	TPTC00_DFBIDX1	Dst FIFO Set B-Dim Idx
354h	16	TPTC00_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy
358h	16	TPTC00_DFBCNT1	Dst FIFO Set B-Count

Table 4-408. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8

Offset	Length	Acronym	Register Name	TPTC00 Physical Address	TPTC01 Physical Address
0h	32	TPTC01_PID	Peripheral ID Register	52A4 0000h	52A6 0000h
4h	16	TPTC01_TCCFG	TC Configuration Register	52A4 0004h	52A6 0004h
100h	16	TPTC01_TCSTAT	TC Status Register	52A4 0100h	52A6 0100h
104h	8	TPTC01_INTSTAT	Interrupt Status Register	52A4 0104h	52A6 0104h
108h	8	TPTC01_INTEN	Interrupt Enable Register	52A4 0108h	52A6 0108h
10Ch	8	TPTC01_INTCLR	Interrupt Clear Register	52A4 010Ch	52A6 010Ch
110h	8	TPTC01_INTCMD	Interrupt Command Register	52A4 0110h	52A6 0110h
120h	8	TPTC01_ERRSTAT	Error Status Register	52A4 0120h	52A6 0120h
124h	8	TPTC01_ERREN	Error Enable Register	52A4 0124h	52A6 0124h
128h	8	TPTC01_ERRCLR	Error Clear Register	52A4 0128h	52A6 0128h
12Ch	24	TPTC01_ERRDET	Error Details Register	52A4 012Ch	52A6 012Ch
130h	8	TPTC01_ERRCMD	Error Command Register	52A4 0130h	52A6 0130h
140h	8	TPTC01_RDRATE	Read Rate Register	52A4 0140h	52A6 0140h
200h	32	TPTC01_POPT	Prog Set Options	52A4 0200h	52A6 0200h
204h	32	TPTC01_PSRC	Prog Set Src Address	52A4 0204h	52A6 0204h
208h	32	TPTC01_PCNT	Prog Set Count	52A4 0208h	52A6 0208h
20Ch	32	TPTC01_PDST	Prog Set Dst Address	52A4 020Ch	52A6 020Ch
210h	32	TPTC01_PBIDX	Prog Set B-Dim Idx	52A4 0210h	52A6 0210h
214h	16	TPTC01_PMPPRXY	Prog Set Mem Protect Proxy	52A4 0214h	52A6 0214h
240h	32	TPTC01_SAOPT	Src Actv Set Options	52A4 0240h	52A6 0240h
244h	32	TPTC01_SASRC	Src Actv Set Src Address	52A4 0244h	52A6 0244h
248h	24	TPTC01_SACNT	Src Actv Set A-Count	52A4 0248h	52A6 0248h
24Ch	32	TPTC01_SADST	Src Actv Set Dst Address	52A4 024Ch	52A6 024Ch
250h	32	TPTC01_SABIDX	Src Actv Set B-Dim Idx	52A4 0250h	52A6 0250h
254h	16	TPTC01_SAMPPRXY	Src Actv Set Mem Protect Proxy	52A4 0254h	52A6 0254h
258h	16	TPTC01_SACNTRLD	Src Actv Set Cnt Reload	52A4 0258h	52A6 0258h
25Ch	32	TPTC01_SASRCBREF	Src Actv Set Src Addr B-Reference	52A4 025Ch	52A6 025Ch
260h	32	TPTC01_SADSTBREF	Src Actv Set Dst Addr B-Reference	52A4 0260h	52A6 0260h
264h	16	TPTC01_SABCNT	Src Actv Set B-Count	52A4 0264h	52A6 0264h
280h	16	TPTC01_DFCNTRLD	Dst FIFO Set Cnt Reload	52A4 0280h	52A6 0280h
284h	32	TPTC01_DFSRCBREF	Dst FIFO Set Src Addr B-Reference	52A4 0284h	52A6 0284h
300h	32	TPTC01_DFOPT0	Dst FIFO Set Options	52A4 0300h	52A6 0300h
304h	32	TPTC01_DFSRC0	Dst FIFO Set Src Address	52A4 0304h	52A6 0304h
308h	24	TPTC01_DFACNT0	Dst FIFO Set A-Count	52A4 0308h	52A6 0308h
30Ch	32	TPTC01_DFDST0	Dst FIFO Set Dst Address	52A4 030Ch	52A6 030Ch
310h	32	TPTC01_DFBIDX0	Dst FIFO Set B-Dim Idx	52A4 0310h	52A6 0310h
314h	16	TPTC01_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy	52A4 0314h	52A6 0314h
318h	16	TPTC01_DFBCNT0	Dst FIFO Set B-Count	52A4 0318h	52A6 0318h
340h	32	TPTC01_DFOPT1	Dst FIFO Set Options	52A4 0340h	52A6 0340h
344h	32	TPTC01_DFSRC1	Dst FIFO Set Src Address	52A4 0344h	52A6 0344h
348h	24	TPTC01_DFACNT1	Dst FIFO Set A-Count	52A4 0348h	52A6 0348h

Table 4-408. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name	TPTC00 Physical Address	TPTC01 Physical Address
34Ch	32	TPTC01_DFDST1	Dst FIFO Set Dst Address	52A4 034Ch	52A6 034Ch
350h	32	TPTC01_DFBIDX1	Dst FIFO Set B-Dim Idx	52A4 0350h	52A6 0350h
354h	16	TPTC01_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy	52A4 0354h	52A6 0354h
358h	16	TPTC01_DFBCNT1	Dst FIFO Set B-Count	52A4 0358h	52A6 0358h

Table 4-409. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8

Offset	Length	Acronym	Register Name
0h	32	TPTC01_PID	Peripheral ID Register
4h	16	TPTC01_TCCFG	TC Configuration Register
100h	16	TPTC01_TCSTAT	TC Status Register
104h	8	TPTC01_INTSTAT	Interrupt Status Register
108h	8	TPTC01_INTEN	Interrupt Enable Register
10Ch	8	TPTC01_INTCLR	Interrupt Clear Register
110h	8	TPTC01_INTCMD	Interrupt Command Register
120h	8	TPTC01_ERRSTAT	Error Status Register
124h	8	TPTC01_ERREN	Error Enable Register
128h	8	TPTC01_ERRCLR	Error Clear Register
12Ch	24	TPTC01_ERRDET	Error Details Register
130h	8	TPTC01_ERRCMD	Error Command Register
140h	8	TPTC01_RDRATE	Read Rate Register
200h	32	TPTC01_POPT	Prog Set Options
204h	32	TPTC01_PSRC	Prog Set Src Address
208h	32	TPTC01_PCNT	Prog Set Count
20Ch	32	TPTC01_PDST	Prog Set Dst Address
210h	32	TPTC01_PBIDX	Prog Set B-Dim Idx
214h	16	TPTC01_PMPPRXY	Prog Set Mem Protect Proxy
240h	32	TPTC01_SAOPT	Src Actv Set Options
244h	32	TPTC01_SASRC	Src Actv Set Src Address
248h	24	TPTC01_SACNT	Src Actv Set A-Count
24Ch	32	TPTC01_SADST	Src Actv Set Dst Address
250h	32	TPTC01_SABIDX	Src Actv Set B-Dim Idx
254h	16	TPTC01_SAMPPRXY	Src Actv Set Mem Protect Proxy
258h	16	TPTC01_SACNTRLD	Src Actv Set Cnt Reload
25Ch	32	TPTC01_SASRCBREF	Src Actv Set Src Addr B-Reference
260h	32	TPTC01_SADSTBREF	Src Actv Set Dst Addr B-Reference
264h	16	TPTC01_SABCNT	Src Actv Set B-Count
280h	16	TPTC01_DFCNTRLD	Dst FIFO Set Cnt Reload
284h	32	TPTC01_DFSRCBREF	Dst FIFO Set Src Addr B-Reference
300h	32	TPTC01_DFOPT0	Dst FIFO Set Options
304h	32	TPTC01_DFSRC0	Dst FIFO Set Src Address
308h	24	TPTC01_DFACNT0	Dst FIFO Set A-Count
30Ch	32	TPTC01_DFDST0	Dst FIFO Set Dst Address

Table 4-409. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name
310h	32	TPTC01_DFBIDX0	Dst FIFO Set B-Dim Idx
314h	16	TPTC01_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy
318h	16	TPTC01_DFBCNT0	Dst FIFO Set B-Count
340h	32	TPTC01_DFOPT1	Dst FIFO Set Options
344h	32	TPTC01_DFSRC1	Dst FIFO Set Src Address
348h	24	TPTC01_DFACNT1	Dst FIFO Set A-Count
34Ch	32	TPTC01_DFDST1	Dst FIFO Set Dst Address
350h	32	TPTC01_DFBIDX1	Dst FIFO Set B-Dim Idx
354h	16	TPTC01_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy
358h	16	TPTC01_DFBCNT1	Dst FIFO Set B-Count

Table 4-410. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8

Offset	Length	Acronym	Register Name
0h	32	TPTC01_PID	Peripheral ID Register
4h	16	TPTC01_TCCFG	TC Configuration Register
100h	16	TPTC01_TCSTAT	TC Status Register
104h	8	TPTC01_INTSTAT	Interrupt Status Register
108h	8	TPTC01_INTEN	Interrupt Enable Register
10Ch	8	TPTC01_INTCLR	Interrupt Clear Register
110h	8	TPTC01_INTCMD	Interrupt Command Register
120h	8	TPTC01_ERRSTAT	Error Status Register
124h	8	TPTC01_ERREN	Error Enable Register
128h	8	TPTC01_ERRCLR	Error Clear Register
12Ch	24	TPTC01_ERRDET	Error Details Register
130h	8	TPTC01_ERRCMD	Error Command Register
140h	8	TPTC01_RDRATE	Read Rate Register
200h	32	TPTC01_POPT	Prog Set Options
204h	32	TPTC01_PSRC	Prog Set Src Address
208h	32	TPTC01_PCNT	Prog Set Count
20Ch	32	TPTC01_PDST	Prog Set Dst Address
210h	32	TPTC01_PBIDX	Prog Set B-Dim Idx
214h	16	TPTC01_PMPPRXY	Prog Set Mem Protect Proxy
240h	32	TPTC01_SAOPT	Src Actv Set Options
244h	32	TPTC01_SASRC	Src Actv Set Src Address
248h	24	TPTC01_SACNT	Src Actv Set A-Count
24Ch	32	TPTC01_SADST	Src Actv Set Dst Address
250h	32	TPTC01_SABIDX	Src Actv Set B-Dim Idx
254h	16	TPTC01_SAMPPRXY	Src Actv Set Mem Protect Proxy
258h	16	TPTC01_SACNTRLD	Src Actv Set Cnt Reload
25Ch	32	TPTC01_SASRCBREF	Src Actv Set Src Addr B-Reference
260h	32	TPTC01_SADSTBREF	Src Actv Set Dst Addr B-Reference
264h	16	TPTC01_SABCNT	Src Actv Set B-Count
280h	16	TPTC01_DFCNTRLD	Dst FIFO Set Cnt Reload

Table 4-410. TPTC01, TPTC01_TPTC Registers, Base Address=52A6 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name
284h	32	TPTC01_DFSRCBREF	Dst FIFO Set Src Addr B-Reference
300h	32	TPTC01_DFOPT0	Dst FIFO Set Options
304h	32	TPTC01_DFSRC0	Dst FIFO Set Src Address
308h	24	TPTC01_DFACNT0	Dst FIFO Set A-Count
30Ch	32	TPTC01_DFDST0	Dst FIFO Set Dst Address
310h	32	TPTC01_DFBIDX0	Dst FIFO Set B-Dim Idx
314h	16	TPTC01_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy
318h	16	TPTC01_DFBCNT0	Dst FIFO Set B-Count
340h	32	TPTC01_DFOPT1	Dst FIFO Set Options
344h	32	TPTC01_DFSRC1	Dst FIFO Set Src Address
348h	24	TPTC01_DFACNT1	Dst FIFO Set A-Count
34Ch	32	TPTC01_DFDST1	Dst FIFO Set Dst Address
350h	32	TPTC01_DFBIDX1	Dst FIFO Set B-Dim Idx
354h	16	TPTC01_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy
358h	16	TPTC01_DFBCNT1	Dst FIFO Set B-Count

Table 4-411. DCC0, DCC0_DCC Registers, Base Address=52B0 0000H, Length=4

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC0_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC0_DCCREV	Module version	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	DCC0_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 0008h	52B0 1008h	52B0 2008h
Ch	32	DCC0_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC0_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC0_DCCSTAT	Contains the error & done flag bit	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC0_DCCCNT0	Value of the counter attached to clock source 0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC0_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC0_DCCCNT1	Value of the counter attached to clock source 1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC0_DCCCLKSSRC1	Clock source1 selection control	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC0_DCCCLKSSRC0	Clock source0 selection control	52B0 0028h	52B0 1028h	52B0 2028h

Table 4-412. DCC0, DCC0_DCC Registers, Base Address=52B0 0000H, Length=4

Offset	Length	Acronym	Register Name	DCC3 Physical Address
0h	32	DCC0_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 3000h
4h	32	DCC0_DCCREV	Module version	52B0 3004h
8h	32	DCC0_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 3008h
Ch	32	DCC0_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 300Ch
10h	32	DCC0_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 3010h
14h	32	DCC0_DCCSTAT	Contains the error & done flag bit	52B0 3014h
18h	32	DCC0_DCCCNT0	Value of the counter attached to clock source 0	52B0 3018h
1Ch	32	DCC0_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 301Ch
20h	32	DCC0_DCCCNT1	Value of the counter attached to clock source 1	52B0 3020h
24h	32	DCC0_DCCCLKSSRC1	Clock source1 selection control	52B0 3024h
28h	32	DCC0_DCCCLKSSRC0	Clock source0 selection control	52B0 3028h

Table 4-413. DCC0, DCC0_DCC Registers, Base Address=52B0 0000H, Length=4

Offset	Length	Acronym	Register Name
0h	32	DCC0_DCCGCTRL	Starts / stops the counters clears the error signal
4h	32	DCC0_DCCREV	Module version
8h	32	DCC0_DCCCNTSEED0	Seed value for the counter attached to clock source 0
Ch	32	DCC0_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0
10h	32	DCC0_DCCCNTSEED1	Seed value for the counter attached to clock source 1
14h	32	DCC0_DCCSTAT	Contains the error & done flag bit
18h	32	DCC0_DCCCNT0	Value of the counter attached to clock source 0
1Ch	32	DCC0_DCCVALID0	Value of the valid counter attached to clock source 0
20h	32	DCC0_DCCCNT1	Value of the counter attached to clock source 1
24h	32	DCC0_DCCCLKSSRC1	Clock source1 selection control
28h	32	DCC0_DCCCLKSSRC0	Clock source0 selection control

Table 4-414. DCC1, DCC1_DCC Registers, Base Address=52B0 1000H, Length=4

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC1_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC1_DCCREV	Module version	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	DCC1_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 0008h	52B0 1008h	52B0 2008h

Table 4-414. DCC1, DCC1_DCC Registers, Base Address=52B0 1000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
Ch	32	DCC1_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC1_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC1_DCCSTAT	Contains the error & done flag bit	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC1_DCCCNT0	Value of the counter attached to clock source 0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC1_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC1_DCCCNT1	Value of the counter attached to clock source 1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC1_DCCCLKSSRC1	Clock source1 selection control	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC1_DCCCLKSSRC0	Clock source0 selection control	52B0 0028h	52B0 1028h	52B0 2028h

Table 4-415. DCC1, DCC1_DCC Registers, Base Address=52B0 1000H, Length=4

Offset	Length	Acronym	Register Name	DCC3 Physical Address
0h	32	DCC1_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 3000h
4h	32	DCC1_DCCREV	Module version	52B0 3004h
8h	32	DCC1_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 3008h
Ch	32	DCC1_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 300Ch
10h	32	DCC1_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 3010h
14h	32	DCC1_DCCSTAT	Contains the error & done flag bit	52B0 3014h
18h	32	DCC1_DCCCNT0	Value of the counter attached to clock source 0	52B0 3018h
1Ch	32	DCC1_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 301Ch
20h	32	DCC1_DCCCNT1	Value of the counter attached to clock source 1	52B0 3020h
24h	32	DCC1_DCCCLKSSRC1	Clock source1 selection control	52B0 3024h
28h	32	DCC1_DCCCLKSSRC0	Clock source0 selection control	52B0 3028h

Table 4-416. DCC1, DCC1_DCC Registers, Base Address=52B0 1000H, Length=4

Offset	Length	Acronym	Register Name
0h	32	DCC1_DCCGCTRL	Starts / stops the counters clears the error signal
4h	32	DCC1_DCCREV	Module version
8h	32	DCC1_DCCCNTSEED0	Seed value for the counter attached to clock source 0

Table 4-416. DCC1, DCC1_DCC Registers, Base Address=52B0 1000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
Ch	32	DCC1_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0
10h	32	DCC1_DCCCNTSEED1	Seed value for the counter attached to clock source 1
14h	32	DCC1_DCCSTAT	Contains the error & done flag bit
18h	32	DCC1_DCCCNT0	Value of the counter attached to clock source 0
1Ch	32	DCC1_DCCVALID0	Value of the valid counter attached to clock source 0
20h	32	DCC1_DCCCNT1	Value of the counter attached to clock source 1
24h	32	DCC1_DCCCLKSSRC1	Clock source1 selection control
28h	32	DCC1_DCCCLKSSRC0	Clock source0 selection control

Table 4-417. DCC2, DCC2_DCC Registers, Base Address=52B0 2000H, Length=4

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC2_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC2_DCCREV	Module version	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	DCC2_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 0008h	52B0 1008h	52B0 2008h
Ch	32	DCC2_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC2_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC2_DCCSTAT	Contains the error & done flag bit	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC2_DCCCNT0	Value of the counter attached to clock source 0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC2_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC2_DCCCNT1	Value of the counter attached to clock source 1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC2_DCCCLKSSRC1	Clock source1 selection control	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC2_DCCCLKSSRC0	Clock source0 selection control	52B0 0028h	52B0 1028h	52B0 2028h

Table 4-418. DCC2, DCC2_DCC Registers, Base Address=52B0 2000H, Length=4

Offset	Length	Acronym	Register Name	DCC3 Physical Address
0h	32	DCC2_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 3000h
4h	32	DCC2_DCCREV	Module version	52B0 3004h

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Table 4-418. DCC2, DCC2_DCC Registers, Base Address=52B0 2000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	DCC3 Physical Address
8h	32	DCC2_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 3008h
Ch	32	DCC2_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 300Ch
10h	32	DCC2_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 3010h
14h	32	DCC2_DCCSTAT	Contains the error & done flag bit	52B0 3014h
18h	32	DCC2_DCCCNT0	Value of the counter attached to clock source 0	52B0 3018h
1Ch	32	DCC2_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 301Ch
20h	32	DCC2_DCCCNT1	Value of the counter attached to clock source 1	52B0 3020h
24h	32	DCC2_DCCCLKSSRC1	Clock source1 selection control	52B0 3024h
28h	32	DCC2_DCCCLKSSRC0	Clock source0 selection control	52B0 3028h

Table 4-419. DCC2, DCC2_DCC Registers, Base Address=52B0 2000H, Length=4

Offset	Length	Acronym	Register Name
0h	32	DCC2_DCCGCTRL	Starts / stops the counters clears the error signal
4h	32	DCC2_DCCREV	Module version
8h	32	DCC2_DCCCNTSEED0	Seed value for the counter attached to clock source 0
Ch	32	DCC2_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0
10h	32	DCC2_DCCCNTSEED1	Seed value for the counter attached to clock source 1
14h	32	DCC2_DCCSTAT	Contains the error & done flag bit
18h	32	DCC2_DCCCNT0	Value of the counter attached to clock source 0
1Ch	32	DCC2_DCCVALID0	Value of the valid counter attached to clock source 0
20h	32	DCC2_DCCCNT1	Value of the counter attached to clock source 1
24h	32	DCC2_DCCCLKSSRC1	Clock source1 selection control
28h	32	DCC2_DCCCLKSSRC0	Clock source0 selection control

Table 4-420. DCC3, DCC3_DCC Registers, Base Address=52B0 3000H, Length=4

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	DCC3_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC3_DCCREV	Module version	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	DCC3_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 0008h	52B0 1008h	52B0 2008h

Table 4-420. DCC3, DCC3_DCC Registers, Base Address=52B0 3000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
Ch	32	DCC3_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC3_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC3_DCCSTAT	Contains the error & done flag bit	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC3_DCCCNT0	Value of the counter attached to clock source 0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC3_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC3_DCCCNT1	Value of the counter attached to clock source 1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC3_DCCCLKSSRC1	Clock source1 selection control	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC3_DCCCLKSSRC0	Clock source0 selection control	52B0 0028h	52B0 1028h	52B0 2028h

Table 4-421. DCC3, DCC3_DCC Registers, Base Address=52B0 3000H, Length=4

Offset	Length	Acronym	Register Name	DCC3 Physical Address
0h	32	DCC3_DCCGCTRL	Starts / stops the counters clears the error signal	52B0 3000h
4h	32	DCC3_DCCREV	Module version	52B0 3004h
8h	32	DCC3_DCCCNTSEED0	Seed value for the counter attached to clock source 0	52B0 3008h
Ch	32	DCC3_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	52B0 300Ch
10h	32	DCC3_DCCCNTSEED1	Seed value for the counter attached to clock source 1	52B0 3010h
14h	32	DCC3_DCCSTAT	Contains the error & done flag bit	52B0 3014h
18h	32	DCC3_DCCCNT0	Value of the counter attached to clock source 0	52B0 3018h
1Ch	32	DCC3_DCCVALID0	Value of the valid counter attached to clock source 0	52B0 301Ch
20h	32	DCC3_DCCCNT1	Value of the counter attached to clock source 1	52B0 3020h
24h	32	DCC3_DCCCLKSSRC1	Clock source1 selection control	52B0 3024h
28h	32	DCC3_DCCCLKSSRC0	Clock source0 selection control	52B0 3028h

Table 4-422. DCC3, DCC3_DCC Registers, Base Address=52B0 3000H, Length=4

Offset	Length	Acronym	Register Name
0h	32	DCC3_DCCGCTRL	Starts / stops the counters clears the error signal
4h	32	DCC3_DCCREV	Module version
8h	32	DCC3_DCCCNTSEED0	Seed value for the counter attached to clock source 0

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Table 4-422. DCC3, DCC3_DCC Registers, Base Address=52B0 3000H, Length=4 (continued)

Offset	Length	Acronym	Register Name
Ch	32	DCC3_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0
10h	32	DCC3_DCCCNTSEED1	Seed value for the counter attached to clock source 1
14h	32	DCC3_DCCSTAT	Contains the error & done flag bit
18h	32	DCC3_DCCCNT0	Value of the counter attached to clock source 0
1Ch	32	DCC3_DCCVALID0	Value of the valid counter attached to clock source 0
20h	32	DCC3_DCCCNT1	Value of the counter attached to clock source 1
24h	32	DCC3_DCCCLKSSRC1	Clock source1 selection control
28h	32	DCC3_DCCCLKSSRC0	Clock source0 selection control

4.6.1 CPSW0_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = h]

Short Description: ID Version Register

Long Description:

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Table 4-423. Instance Table

Instance Name	Physical Address
CPSW0	5280 0000h

Figure 4-190. CPSW0_CPSW_NUSS_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
RO															
110101110100000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
RO					RO			RO							
11					1			11							

Access Types Legend

Table 4-424. CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IDENT	RO	6422E98E9020h	Identification value
15 - 11	RTL_VER	RO	Bh	RTL version value
10 - 8	MAJOR_VER	RO	1h	Major version value
7 - 0	MINOR_VER	RO	Bh	Minor version value

4.6.2 CPSW0_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = h]

Short Description: SS SYNCE Count Register

Long Description:

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Table 4-425. Instance Table

Instance Name	Physical Address
CPSW0	5280 0004h

Figure 4-191. CPSW0_SS_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNCE_CNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCE_CNT															
RW															
0															

Access Types Legend

Table 4-426. SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SYNCE_CNT	RW	0h	Sync E Count Value

4.6.3 CPSW0_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = h]

Short Description: SS Synce Mux Register

Long Description:

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Table 4-427. Instance Table

Instance Name	Physical Address
CPSW0	5280 0008h

Figure 4-192. CPSW0_SS_SYNCE_MUX_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED		SYNCE_SEL					
NONE		RW					
0		0					

Access Types Legend

Table 4-428. SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5 - 0	SYNCE_SEL	RW	0h	Sync E Select Value

4.6.4 CPSW0_SS_CONTROL_REG Register (Offset = Ch) [reset = h]

Short Description: SS Control Register

Long Description:

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Table 4-429. Instance Table

Instance Name	Physical Address
CPSW0	5280 000Ch

Figure 4-193. CPSW0_SS_CONTROL_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						EEE_PHY_ONLY	EEE_EN
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-430. SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	EEE_PHY_ONLY	RW	0h	Energy Efficient Enable Phy Only Mode: 0=The low power indicate state includes gating off the CPPI_GCLK to the CPSW, 1=The low power indicate state does not gate the clock to the CPSW
0	EEE_EN	RW	0h	Energy Efficient Ethernet Enable: 0=EEE is disabled, 1=EEE is enabled

4.6.5 CPSW0_SS_INT_CONTROL_REG Register (Offset = 18h) [reset = h]

Short Description: SS Interrupt Control Register

Long Description:

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Table 4-431. Instance Table

Instance Name	Physical Address
CPSW0	5280 0018h

Figure 4-194. CPSW0_SS_INT_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT_TEST	INT_SEL_VEC_EN	RESERVED								INT_BYPASS					
RW	RW	NONE								RW					
0	0	0								0					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				INT_PRESCALE											
NONE				RW											
0				0											

Access Types Legend

Table 4-432. SS_INT_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_TEST	RW	0h	Interrupt Test
30	INT_SEL_VEC_EN	RW	0h	Interrupt Sel Vector Enable
	RESERVED	NONE		Reserved
21 - 16	INT_BYPASS	RW	0h	Interrupt Bypass Value
	RESERVED	NONE		Reserved
11 - 0	INT_PRESCALE	RW	0h	Interrupt Prescale Value

4.6.6 CPSW0_SS_STATUS_REG Register (Offset = 1Ch) [reset = h]

Short Description: SS Status Register

Long Description:

Return to Summary Table

Table 4-433. Instance Table

Instance Name	Physical Address
CPSW0	5280 001Ch

Figure 4-195. CPSW0_SS_STATUS_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EEE_CLKSTOP_ACK							
RO							
0							

Access Types Legend

Table 4-434. SS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EEE_CLKSTOP_ACK	RO	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

4.6.7 CPSW0_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = h]

Short Description: Subsystem Configuration Register

Long Description:

Return to Summary Table

Table 4-435. Instance Table

Instance Name	Physical Address
CPSW0	5280 0020h

Figure 4-196. CPSW0_SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				XGMII								QSGMII	SGMII	RGMII	RMII
NONE				RO								RO	RO	RO	RO
0				0								0	0	1	1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			NUM_GENF					NUM_PORTS							
NONE			RO					RO							
0			10					11							

Access Types Legend

Table 4-436. SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 20	XGMII	RO	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	RO	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	RO	0h	SGMII is included in the CPSW_NUSS
17	RGMII	RO	1h	RGMII is included in the CPSW_NUSS
16	RMII	RO	1h	RMII is included in the CPSW_NUSS
	RESERVED	NONE		Reserved
12 - 8	NUM_GENF	RO	Ah	The number of CPTS GENF outputs
7 - 0	NUM_PORTS	RO	Bh	The total number of ports including the host port 0

4.6.8 CPSW0_RGMII1_STATUS_REG Register (Offset = 30h) [reset = h]

Short Description: RGMII1 Status Register

Long Description:

Return to Summary Table

Table 4-437. Instance Table

Instance Name	Physical Address
CPSW0	5280 0030h

Figure 4-197. CPSW0_RGMII1_STATUS_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				RO	RO		RO
0				0	0		0

Access Types Legend

Table 4-438. RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	RO	0h	Rgmii1 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	RO	0h	Rgmii1 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	RO	0h	Rgmii1 link indicator: 0=Link is down, 1=Link is up

4.6.9 CPSW0_RGMII2_STATUS_REG Register (Offset = 34h) [reset = h]

Short Description: RGMII2 Status Register

Long Description:

Return to Summary Table

Table 4-439. Instance Table

Instance Name	Physical Address
CPSW0	5280 0034h

Figure 4-198. CPSW0_RGMII2_STATUS_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				RO	RO		RO
0				0	0		0

Access Types Legend

Table 4-440. RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	RO	0h	Rgmii2 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	RO	0h	Rgmii2 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	RO	0h	Rgmii2 link indicator: 0=Link is down, 1=Link is up

4.6.10 TPCC0_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-441. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0000h

Figure 4-199. TPCC0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RES1		FUNC											
RO		RO		RO											
1		0		1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
10101					11			0		0					

Access Types Legend

Table 4-442. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
29 - 28	RES1	RO	0h	RESERVE FIELD
27 - 16	FUNC	RO	1h	Function indicates a software compatible module family.
15 - 11	RTL	RO	2775h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	0h	Minor Revision

4.6.11 TPCC0_CCCFG Register (Offset = 4h) [reset = h]

Short Description: CC Configuration Register

Long Description:

Return to Summary Table

Table 4-443. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0004h

Figure 4-200. TPCC0_CCCFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES2						MPEXIST	CHMAPEXIST	RES3		NUMREGN		RES4	NUMTC		
RO						RO	RO	RO		RO		RO	RO		
0						0	0	0		10		0	1		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES5	NUMPAENTRY			RES6	NUMINTCH			RES7	NUMQDMACH			RES8	NUMDMACH		
RO	RO			RO	RO			RO	RO			RO	RO		
0	11			0	100			0	100			0	101		

Access Types Legend

Table 4-444. CCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RES2	RO	0h	RESERVE FIELD
25	MPEXIST	RO	0h	Memory Protection Existence MPEXIST = 0 : No memory protection. MPEXIST = 1 : Memory Protection logic included.
24	CHMAPEXIST	RO	0h	Channel Mapping Existence CHMAPEXIST = 0 : No Channel mapping. CHMAPEXIST = 1 : Channel mapping logic included.
23 - 22	RES3	RO	0h	RESERVE FIELD
21 - 20	NUMREGN	RO	Ah	Number of MP and Shadow regions
19	RES4	RO	0h	RESERVE FIELD
18 - 16	NUMTC	RO	1h	Number of Queues/Number of TCs
15	RES5	RO	0h	RESERVE FIELD
14 - 12	NUMPAENTRY	RO	Bh	Number of PaRAM entries
11	RES6	RO	0h	RESERVE FIELD
10 - 8	NUMINTCH	RO	64h	Number of Interrupt Channels
7	RES7	RO	0h	RESERVE FIELD
6 - 4	NUMQDMACH	RO	64h	Number of QDMA Channels
3	RES8	RO	0h	RESERVE FIELD
2 - 0	NUMDMACH	RO	65h	Number of DMA Channels

4.6.12 TPCC0_QCHMAPN Register (Offset = 200h) [reset = h]

Short Description: QDMA Channel N Mapping Register

Long Description:

Return to Summary Table

Table 4-445. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0200h

Figure 4-201. TPCC0_QCHMAPN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10		PAENTRY									TRWORD			RESERVED	
RO		RW									RW			NONE	
0		0									0			0	

Access Types Legend

Table 4-446. QCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 14	RES10	RO	0h	RESERVE FIELD
13 - 5	PAENTRY	RW	0h	PaRAM Entry number for QDMA Channel N.
4 - 2	TRWORD	RW	0h	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized.
	RESERVED	NONE		Reserved

4.6.13 TPCC0_DMAQNUMN Register (Offset = 240h) [reset = h]

Short Description: DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

Long Description:

Return to Summary Table

Table 4-447. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0240h

Figure 4-202. TPCC0_DMAQNUMN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11		E7		RES12		E6		RES13		E5		RES14		E4	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15		E3		RES16		E2		RES17		E1		RES18		E0	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-448. DMAQNUMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES11	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	DMA Queue Number for event #7
27	RES12	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	DMA Queue Number for event #6
23	RES13	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	DMA Queue Number for event #5
19	RES14	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	DMA Queue Number for event #4
15	RES15	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	DMA Queue Number for event #3
11	RES16	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	DMA Queue Number for event #2
7	RES17	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	DMA Queue Number for event #1
3	RES18	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	DMA Queue Number for event #0

4.6.14 TPCC0_QDMAQNUM Register (Offset = 260h) [reset = h]

Short Description: QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

Long Description:

Return to Summary Table

Table 4-449. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0260h

Figure 4-203. TPCC0_QDMAQNUM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19		E7		RES20		E6		RES21		E5		RES22		E4	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES23		E3		RES24		E2		RES25		E1		RES26		E0	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-450. QDMAQNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES19	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	QDMA Queue Number for event #7
27	RES20	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	QDMA Queue Number for event #6
23	RES21	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	QDMA Queue Number for event #5
19	RES22	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	QDMA Queue Number for event #4
15	RES23	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	QDMA Queue Number for event #3
11	RES24	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	QDMA Queue Number for event #2
7	RES25	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	QDMA Queue Number for event #1
3	RES26	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	QDMA Queue Number for event #0

4.6.15 TPCC0_QUETCMAP Register (Offset = 280h) [reset = h]

Short Description: Queue to TC Mapping

Long Description:

Return to Summary Table

Table 4-451. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0280h

Figure 4-204. TPCC0_QUETCMAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES27									TCNUMQ1			RES28	TCNUMQ0		
RO									RW			RO	RW		
0									1			0	0		

Access Types Legend

Table 4-452. QUETCMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES27	RO	0h	RESERVE FIELD
6 - 4	TCNUMQ1	RW	1h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.
3	RES28	RO	0h	RESERVE FIELD
2 - 0	TCNUMQ0	RW	0h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.

4.6.16 TPCC0_QUEPRI Register (Offset = 284h) [reset = h]

Short Description: Queue Priority

Long Description:

Return to Summary Table

Table 4-453. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0284h

Figure 4-205. TPCC0_QUEPRI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES29									PRIQ1			RES30	PRIQ0		
RO									RW			RO	RW		
0									0			0	0		

Access Types Legend

Table 4-454. QUEPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES29	RO	0h	RESERVE FIELD
6 - 4	PRIQ1	RW	0h	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.
3	RES30	RO	0h	RESERVE FIELD
2 - 0	PRIQ0	RW	0h	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.

4.6.17 TPCC0_EMR Register (Offset = 300h) [reset = h]

Short Description: Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-455. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0300h

Figure 4-206. TPCC0_EMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-456. EMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event Missed #31
30	E30	RO	0h	Event Missed #30
29	E29	RO	0h	Event Missed #29
28	E28	RO	0h	Event Missed #28
27	E27	RO	0h	Event Missed #27
26	E26	RO	0h	Event Missed #26
25	E25	RO	0h	Event Missed #25
24	E24	RO	0h	Event Missed #24
23	E23	RO	0h	Event Missed #23
22	E22	RO	0h	Event Missed #22
21	E21	RO	0h	Event Missed #21
20	E20	RO	0h	Event Missed #20
19	E19	RO	0h	Event Missed #19
18	E18	RO	0h	Event Missed #18
17	E17	RO	0h	Event Missed #17
16	E16	RO	0h	Event Missed #16
15	E15	RO	0h	Event Missed #15
14	E14	RO	0h	Event Missed #14
13	E13	RO	0h	Event Missed #13
12	E12	RO	0h	Event Missed #12
11	E11	RO	0h	Event Missed #11
10	E10	RO	0h	Event Missed #10
9	E9	RO	0h	Event Missed #9
8	E8	RO	0h	Event Missed #8

Table 4-456. EMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1
0	E0	RO	0h	Event Missed #0

4.6.18 TPCC0_EMRH Register (Offset = 304h) [reset = h]

Short Description: Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-457. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0304h

Figure 4-207. TPCC0_EMRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-458. EMRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event Missed #63
30	E62	RO	0h	Event Missed #62
29	E61	RO	0h	Event Missed #61
28	E60	RO	0h	Event Missed #60
27	E59	RO	0h	Event Missed #59
26	E58	RO	0h	Event Missed #58
25	E57	RO	0h	Event Missed #57
24	E56	RO	0h	Event Missed #56
23	E55	RO	0h	Event Missed #55
22	E54	RO	0h	Event Missed #54
21	E53	RO	0h	Event Missed #53
20	E52	RO	0h	Event Missed #52
19	E51	RO	0h	Event Missed #51
18	E50	RO	0h	Event Missed #50
17	E49	RO	0h	Event Missed #49
16	E48	RO	0h	Event Missed #48
15	E47	RO	0h	Event Missed #47
14	E46	RO	0h	Event Missed #46
13	E45	RO	0h	Event Missed #45
12	E44	RO	0h	Event Missed #44
11	E43	RO	0h	Event Missed #43
10	E42	RO	0h	Event Missed #42
9	E41	RO	0h	Event Missed #41
8	E40	RO	0h	Event Missed #40

Table 4-458. EMRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	RO	0h	Event Missed #39
6	E38	RO	0h	Event Missed #38
5	E37	RO	0h	Event Missed #37
4	E36	RO	0h	Event Missed #36
3	E35	RO	0h	Event Missed #35
2	E34	RO	0h	Event Missed #34
1	E33	RO	0h	Event Missed #33
0	E32	RO	0h	Event Missed #32

4.6.19 TPCC0_EMCR Register (Offset = 308h) [reset = h]

Short Description: Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-459. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0308h

Figure 4-208. TPCC0_EMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-460. EMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event Missed Clear #31
30	E30	WO	0h	Event Missed Clear #30
29	E29	WO	0h	Event Missed Clear #29
28	E28	WO	0h	Event Missed Clear #28
27	E27	WO	0h	Event Missed Clear #27
26	E26	WO	0h	Event Missed Clear #26
25	E25	WO	0h	Event Missed Clear #25
24	E24	WO	0h	Event Missed Clear #24
23	E23	WO	0h	Event Missed Clear #23
22	E22	WO	0h	Event Missed Clear #22
21	E21	WO	0h	Event Missed Clear #21
20	E20	WO	0h	Event Missed Clear #20
19	E19	WO	0h	Event Missed Clear #19
18	E18	WO	0h	Event Missed Clear #18
17	E17	WO	0h	Event Missed Clear #17
16	E16	WO	0h	Event Missed Clear #16
15	E15	WO	0h	Event Missed Clear #15
14	E14	WO	0h	Event Missed Clear #14
13	E13	WO	0h	Event Missed Clear #13
12	E12	WO	0h	Event Missed Clear #12
11	E11	WO	0h	Event Missed Clear #11
10	E10	WO	0h	Event Missed Clear #10
9	E9	WO	0h	Event Missed Clear #9
8	E8	WO	0h	Event Missed Clear #8
7	E7	WO	0h	Event Missed Clear #7

Table 4-460. EMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

4.6.20 TPCC0_EMCRH Register (Offset = 30Ch) [reset = h]

Short Description: Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-461. Instance Table

Instance Name	Physical Address
TPCC0	52A0 030Ch

Figure 4-209. TPCC0_EMCRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-462. EMCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event Missed Clear #63
30	E62	WO	0h	Event Missed Clear #62
29	E61	WO	0h	Event Missed Clear #61
28	E60	WO	0h	Event Missed Clear #60
27	E59	WO	0h	Event Missed Clear #59
26	E58	WO	0h	Event Missed Clear #58
25	E57	WO	0h	Event Missed Clear #57
24	E56	WO	0h	Event Missed Clear #56
23	E55	WO	0h	Event Missed Clear #55
22	E54	WO	0h	Event Missed Clear #54
21	E53	WO	0h	Event Missed Clear #53
20	E52	WO	0h	Event Missed Clear #52
19	E51	WO	0h	Event Missed Clear #51
18	E50	WO	0h	Event Missed Clear #50
17	E49	WO	0h	Event Missed Clear #49
16	E48	WO	0h	Event Missed Clear #48
15	E47	WO	0h	Event Missed Clear #47
14	E46	WO	0h	Event Missed Clear #46
13	E45	WO	0h	Event Missed Clear #45
12	E44	WO	0h	Event Missed Clear #44
11	E43	WO	0h	Event Missed Clear #43
10	E42	WO	0h	Event Missed Clear #42
9	E41	WO	0h	Event Missed Clear #41
8	E40	WO	0h	Event Missed Clear #40
7	E39	WO	0h	Event Missed Clear #39

Table 4-462. EMCRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event Missed Clear #38
5	E37	WO	0h	Event Missed Clear #37
4	E36	WO	0h	Event Missed Clear #36
3	E35	WO	0h	Event Missed Clear #35
2	E34	WO	0h	Event Missed Clear #34
1	E33	WO	0h	Event Missed Clear #33
0	E32	WO	0h	Event Missed Clear #32

4.6.21 TPCC0_QEMR Register (Offset = 310h) [reset = h]

Short Description: QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-463. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0310h

Figure 4-210. TPCC0_QEMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES31								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-464. QEMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES31	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1
0	E0	RO	0h	Event Missed #0

4.6.22 TPCC0_QEMCR Register (Offset = 314h) [reset = h]

Short Description: QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-465. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0314h

Figure 4-211. TPCC0_QEMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES32								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-466. QEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES32	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event Missed Clear #7
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

4.6.23 TPCC0_CCERR Register (Offset = 318h) [reset = h]

Short Description: CC Error Register

Long Description:

Return to Summary Table

Table 4-467. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0318h

Figure 4-212. TPCC0_CCERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES33															TCERR
RO															RO
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES34								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-468. CCERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES33	RO	0h	RESERVE FIELD
16	TCERR	RO	0h	Transfer Completion Code Error: TCCERR = 0 : Total number of allowed TCCs outstanding has not been reached. TCCERR = 1 : Total number of allowed TCCs has been reached. TCCERR can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors were previously clear) then an error will be signaled with TPCC error interrupt.
15 - 8	RES34	RO	0h	RESERVE FIELD
7	QTHRXCD7	RO	0h	Queue Threshold Error for Q7: QTHRXCD7 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD7 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
6	QTHRXCD6	RO	0h	Queue Threshold Error for Q6: QTHRXCD6 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD6 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
5	QTHRXCD5	RO	0h	Queue Threshold Error for Q5: QTHRXCD5 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD5 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD5 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

Table 4-468. CCERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	QTHRXCD4	RO	0h	Queue Threshold Error for Q4: QTHRXCD4 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD4 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD4 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
3	QTHRXCD3	RO	0h	Queue Threshold Error for Q3: QTHRXCD3 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD3 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD3 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
2	QTHRXCD2	RO	0h	Queue Threshold Error for Q2: QTHRXCD2 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD2 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD2 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
1	QTHRXCD1	RO	0h	Queue Threshold Error for Q1: QTHRXCD1 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD1 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD1 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
0	QTHRXCD0	RO	0h	Queue Threshold Error for Q0: QTHRXCD0 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD0 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD0 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

4.6.24 TPCC0_CCERRCLR Register (Offset = 31Ch) [reset = h]

Short Description: CC Error Clear Register

Long Description:

Return to Summary Table

Table 4-469. Instance Table

Instance Name	Physical Address
TPCC0	52A0 031Ch

Figure 4-213. TPCC0_CCERRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES35															TCERR
RO															WO
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES36								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-470. CCERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES35	RO	0h	RESERVE FIELD
16	TCERR	WO	0h	Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect.
15 - 8	RES36	RO	0h	RESERVE FIELD
7	QTHRXCD7	WO	0h	Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect.
6	QTHRXCD6	WO	0h	Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect.
5	QTHRXCD5	WO	0h	Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect.
4	QTHRXCD4	WO	0h	Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect.
3	QTHRXCD3	WO	0h	Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect.
2	QTHRXCD2	WO	0h	Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect.
1	QTHRXCD1	WO	0h	Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect.
0	QTHRXCD0	WO	0h	Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect.

4.6.25 TPCC0_EEVAL Register (Offset = 320h) [reset = h]

Short Description: Error Eval Register

Long Description:

Return to Summary Table

Table 4-471. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0320h

Figure 4-214. TPCC0_EEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES37															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES37														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-472. EEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES37	RO	0h	RESERVE FIELD
1	SET	WO	0h	Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect.
0	EVAL	WO	0h	Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect.

4.6.26 TPCC0_DRAEM Register (Offset = 340h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-473. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0340h

Figure 4-215. TPCC0_DRAEM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-474. DRAEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RW	0h	DMA Region Access enable for Region M bit #31
30	E30	RW	0h	DMA Region Access enable for Region M bit #30
29	E29	RW	0h	DMA Region Access enable for Region M bit #29
28	E28	RW	0h	DMA Region Access enable for Region M bit #28
27	E27	RW	0h	DMA Region Access enable for Region M bit #27
26	E26	RW	0h	DMA Region Access enable for Region M bit #26
25	E25	RW	0h	DMA Region Access enable for Region M bit #25
24	E24	RW	0h	DMA Region Access enable for Region M bit #24
23	E23	RW	0h	DMA Region Access enable for Region M bit #23
22	E22	RW	0h	DMA Region Access enable for Region M bit #22
21	E21	RW	0h	DMA Region Access enable for Region M bit #21
20	E20	RW	0h	DMA Region Access enable for Region M bit #20
19	E19	RW	0h	DMA Region Access enable for Region M bit #19
18	E18	RW	0h	DMA Region Access enable for Region M bit #18
17	E17	RW	0h	DMA Region Access enable for Region M bit #17
16	E16	RW	0h	DMA Region Access enable for Region M bit #16
15	E15	RW	0h	DMA Region Access enable for Region M bit #15
14	E14	RW	0h	DMA Region Access enable for Region M bit #14
13	E13	RW	0h	DMA Region Access enable for Region M bit #13
12	E12	RW	0h	DMA Region Access enable for Region M bit #12
11	E11	RW	0h	DMA Region Access enable for Region M bit #11
10	E10	RW	0h	DMA Region Access enable for Region M bit #10
9	E9	RW	0h	DMA Region Access enable for Region M bit #9

Table 4-474. DRAEM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	RW	0h	DMA Region Access enable for Region M bit #8
7	E7	RW	0h	DMA Region Access enable for Region M bit #7
6	E6	RW	0h	DMA Region Access enable for Region M bit #6
5	E5	RW	0h	DMA Region Access enable for Region M bit #5
4	E4	RW	0h	DMA Region Access enable for Region M bit #4
3	E3	RW	0h	DMA Region Access enable for Region M bit #3
2	E2	RW	0h	DMA Region Access enable for Region M bit #2
1	E1	RW	0h	DMA Region Access enable for Region M bit #1
0	E0	RW	0h	DMA Region Access enable for Region M bit #0

4.6.27 TPCC0_DRAEHM Register (Offset = 344h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-475. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0344h

Figure 4-216. TPCC0_DRAEHM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-476. DRAEHM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RW	0h	DMA Region Access enable for Region M bit #63
30	E62	RW	0h	DMA Region Access enable for Region M bit #62
29	E61	RW	0h	DMA Region Access enable for Region M bit #61
28	E60	RW	0h	DMA Region Access enable for Region M bit #60
27	E59	RW	0h	DMA Region Access enable for Region M bit #59
26	E58	RW	0h	DMA Region Access enable for Region M bit #58
25	E57	RW	0h	DMA Region Access enable for Region M bit #57
24	E56	RW	0h	DMA Region Access enable for Region M bit #56
23	E55	RW	0h	DMA Region Access enable for Region M bit #55
22	E54	RW	0h	DMA Region Access enable for Region M bit #54
21	E53	RW	0h	DMA Region Access enable for Region M bit #53
20	E52	RW	0h	DMA Region Access enable for Region M bit #52
19	E51	RW	0h	DMA Region Access enable for Region M bit #51
18	E50	RW	0h	DMA Region Access enable for Region M bit #50
17	E49	RW	0h	DMA Region Access enable for Region M bit #49
16	E48	RW	0h	DMA Region Access enable for Region M bit #48
15	E47	RW	0h	DMA Region Access enable for Region M bit #47
14	E46	RW	0h	DMA Region Access enable for Region M bit #46

Table 4-476. DRAEHM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E45	RW	0h	DMA Region Access enable for Region M bit #45
12	E44	RW	0h	DMA Region Access enable for Region M bit #44
11	E43	RW	0h	DMA Region Access enable for Region M bit #43
10	E42	RW	0h	DMA Region Access enable for Region M bit #42
9	E41	RW	0h	DMA Region Access enable for Region M bit #41
8	E40	RW	0h	DMA Region Access enable for Region M bit #40
7	E39	RW	0h	DMA Region Access enable for Region M bit #39
6	E38	RW	0h	DMA Region Access enable for Region M bit #38
5	E37	RW	0h	DMA Region Access enable for Region M bit #37
4	E36	RW	0h	DMA Region Access enable for Region M bit #36
3	E35	RW	0h	DMA Region Access enable for Region M bit #35
2	E34	RW	0h	DMA Region Access enable for Region M bit #34
1	E33	RW	0h	DMA Region Access enable for Region M bit #33
0	E32	RW	0h	DMA Region Access enable for Region M bit #32

4.6.28 TPCC0_QRAEN Register (Offset = 380h) [reset = h]

Short Description: QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

Long Description:

Return to Summary Table

Table 4-477. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0380h

Figure 4-217. TPCC0_QRAEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES38															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES38								E7	E6	E5	E4	E3	E2	E1	E0
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-478. QRAEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES38	RO	0h	RESERVE FIELD
7	E7	RW	0h	QDMA Region Access enable for Region M bit #7
6	E6	RW	0h	QDMA Region Access enable for Region M bit #6
5	E5	RW	0h	QDMA Region Access enable for Region M bit #5
4	E4	RW	0h	QDMA Region Access enable for Region M bit #4
3	E3	RW	0h	QDMA Region Access enable for Region M bit #3
2	E2	RW	0h	QDMA Region Access enable for Region M bit #2
1	E1	RW	0h	QDMA Region Access enable for Region M bit #1
0	E0	RW	0h	QDMA Region Access enable for Region M bit #0

4.6.29 TPCC0_QNE0 Register (Offset = 400h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-479. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0400h

Figure 4-218. TPCC0_QNE0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES39															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES39								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-480. QNE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES39	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.30 TPCC0_QNE1 Register (Offset = 404h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 1

Long Description:

Return to Summary Table

Table 4-481. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0404h

Figure 4-219. TPCC0_QNE1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES40								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-482. QNE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES40	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.31 TPCC0_QNE2 Register (Offset = 408h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 2

Long Description:

Return to Summary Table

Table 4-483. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0408h

Figure 4-220. TPCC0_QNE2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES41															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES41								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-484. QNE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES41	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.32 TPCC0_QNE3 Register (Offset = 40Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 3

Long Description:

Return to Summary Table

Table 4-485. Instance Table

Instance Name	Physical Address
TPCC0	52A0 040Ch

Figure 4-221. TPCC0_QNE3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES42															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES42								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-486. QNE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES42	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.33 TPCC0_QNE4 Register (Offset = 410h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 4

Long Description:

Return to Summary Table

Table 4-487. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0410h

Figure 4-222. TPCC0_QNE4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES43															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES43								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-488. QNE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES43	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.34 TPCC0_QNE5 Register (Offset = 414h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 5

Long Description:

Return to Summary Table

Table 4-489. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0414h

Figure 4-223. TPCC0_QNE5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES44															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES44								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-490. QNE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES44	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.35 TPCC0_QNE6 Register (Offset = 418h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 6

Long Description:

Return to Summary Table

Table 4-491. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0418h

Figure 4-224. TPCC0_QNE6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES45															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES45								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-492. QNE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES45	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.36 TPCC0_QNE7 Register (Offset = 41Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 7

Long Description:

Return to Summary Table

Table 4-493. Instance Table

Instance Name	Physical Address
TPCC0	52A0 041Ch

Figure 4-225. TPCC0_QNE7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES46															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES46								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-494. QNE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES46	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.37 TPCC0_QNE8 Register (Offset = 420h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 8

Long Description:

Return to Summary Table

Table 4-495. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0420h

Figure 4-226. TPCC0_QNE8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES47								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-496. QNE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES47	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.38 TPCC0_QNE9 Register (Offset = 424h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 9

Long Description:

Return to Summary Table

Table 4-497. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0424h

Figure 4-227. TPCC0_QNE9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES48															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES48								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-498. QNE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES48	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.39 TPCC0_QNE10 Register (Offset = 428h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-499. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0428h

Figure 4-228. TPCC0_QNE10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES49								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-500. QNE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES49	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.40 TPCC0_QNE11 Register (Offset = 42Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 11

Long Description:

Return to Summary Table

Table 4-501. Instance Table

Instance Name	Physical Address
TPCC0	52A0 042Ch

Figure 4-229. TPCC0_QNE11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES50															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES50								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-502. QNE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES50	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.41 TPCC0_QNE12 Register (Offset = 430h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 12

Long Description:

Return to Summary Table

Table 4-503. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0430h

Figure 4-230. TPCC0_QNE12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES51															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES51								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-504. QNE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES51	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.42 TPCC0_QNE13 Register (Offset = 434h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 13

Long Description:

Return to Summary Table

Table 4-505. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0434h

Figure 4-231. TPCC0_QNE13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES52															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES52								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-506. QNE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES52	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.43 TPCC0_QNE14 Register (Offset = 438h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 14

Long Description:

Return to Summary Table

Table 4-507. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0438h

Figure 4-232. TPCC0_QNE14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES53															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES53								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-508. QNE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES53	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.44 TPCC0_QNE15 Register (Offset = 43Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 15

Long Description:

Return to Summary Table

Table 4-509. Instance Table

Instance Name	Physical Address
TPCC0	52A0 043Ch

Figure 4-233. TPCC0_QNE15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES54															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES54								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-510. QNE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES54	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.6.45 TPCC0_QSTATN Register (Offset = 600h) [reset = h]

Short Description: QSTATn Register Set

Long Description:

Return to Summary Table

Table 4-511. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0600h

Figure 4-234. TPCC0_QSTATN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES55							THRXCD	RES56			WM				
RO							RO	RO			RO				
0							0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES57			NUMVAL					RES58				STRTPTR			
RO			RO					RO				RO			
0			0					0				0			

Access Types Legend

Table 4-512. QSTATN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RES55	RO	0h	RESERVE FIELD
24	THRXCD	RO	0h	Threshold Exceeded: THRXCD = 0 : Threshold specified by QWMTHR(A B).Qn has not been exceeded. THRXCD = 1 : Threshold specified by QWMTHR(A B).Qn has been exceeded. QSTATn.THRXCD is cleared via CCERR.WMCLRn bit.
23 - 21	RES56	RO	0h	RESERVE FIELD
20 - 16	WM	RO	0h	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark (WM) was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 (empty) to 0x10 (full)
15 - 13	RES57	RO	0h	RESERVE FIELD
12 - 8	NUMVAL	RO	0h	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 (empty) to 0x10 (full)
7 - 4	RES58	RO	0h	RESERVE FIELD
3 - 0	STRTPTR	RO	0h	Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 (0th entry) to 0xF (15th entry)

4.6.46 TPCC0_QWMTHRA Register (Offset = 620h) [reset = h]

Short Description: Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

Long Description:

Return to Summary Table

Table 4-513. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0620h

Figure 4-235. TPCC0_QWMTHRA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES59															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES59			Q1					RES60			Q0				
RO			RW					RO			RW				
0			10000					0			10000				

Access Types Legend

Table 4-514. QWMTHRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RES59	RO	0h	RESERVE FIELD
12 - 8	Q1	RW	2710h	Queue Threshold for Q1 value
7 - 5	RES60	RO	0h	RESERVE FIELD
4 - 0	Q0	RW	2710h	Queue Threshold for Q0 value

4.6.47 TPCC0_CCSTAT Register (Offset = 640h) [reset = h]

Short Description: CC Status Register

Long Description:

Return to Summary Table

Table 4-515. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0640h

Figure 4-236. TPCC0_CCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES61								QUEACTV7	QUEACTV6	QUEACTV5	QUEACTV4	QUEACTV3	QUEACTV2	QUEACTV1	QUEACTV0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES62		COMPACTV						RES63			ACTV	RES64	TRACTV	QEVTACTV	EVTACTV
RO		RO						RO			RO	RO	RO	RO	RO
0		0						0			0	0	0	0	0

Access Types Legend

Table 4-516. CCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RES61	RO	0h	RESERVE FIELD
23	QUEACTV7	RO	0h	Queue 7 Active QUEACTV7 = 0 : No Evts are queued in Q7. QUEACTV7 = 1 : At least one TR is queued in Q7.
22	QUEACTV6	RO	0h	Queue 6 Active QUEACTV6 = 0 : No Evts are queued in Q6. QUEACTV6 = 1 : At least one TR is queued in Q6.
21	QUEACTV5	RO	0h	Queue 5 Active QUEACTV5 = 0 : No Evts are queued in Q5. QUEACTV5 = 1 : At least one TR is queued in Q5.
20	QUEACTV4	RO	0h	Queue 4 Active QUEACTV4 = 0 : No Evts are queued in Q4. QUEACTV4 = 1 : At least one TR is queued in Q4.
19	QUEACTV3	RO	0h	Queue 3 Active QUEACTV3 = 0 : No Evts are queued in Q3. QUEACTV3 = 1 : At least one TR is queued in Q3.
18	QUEACTV2	RO	0h	Queue 2 Active QUEACTV2 = 0 : No Evts are queued in Q2. QUEACTV2 = 1 : At least one TR is queued in Q2.
17	QUEACTV1	RO	0h	Queue 1 Active QUEACTV1 = 0 : No Evts are queued in Q1. QUEACTV1 = 1 : At least one TR is queued in Q1.
16	QUEACTV0	RO	0h	Queue 0 Active QUEACTV0 = 0 : No Evts are queued in Q0. QUEACTV0 = 1 : At least one TR is queued in Q0.
15 - 14	RES62	RO	0h	RESERVE FIELD
13 - 8	COMPACTV	RO	0h	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV = 0 : No completion requests outstanding. COMPACTV = 1: Total of '1' completion request outstanding. ... COMPACTV = 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63.
7 - 5	RES63	RO	0h	RESERVE FIELD

Table 4-516. CCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ACTV	RO	0h	Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy.
3	RES64	RO	0h	RESERVE FIELD
2	TRACTV	RO	0h	Transfer Request Active: TRACTV = 0 : Transfer Request processing/submission logic is inactive. TRACTV = 1 : Transfer Request processing/submission logic is active.
1	QEVTACTV	RO	0h	QDMA Event Active: QEVTACTV = 0 : No enabled QDMA Events are active within the CC. QEVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.
0	EVTACTV	RO	0h	DMA Event Active: EVTACTV = 0 : No enabled DMA Events are active within the CC. EVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.

4.6.48 TPCC0_AETCTL Register (Offset = 700h) [reset = h]

Short Description: Advanced Event Trigger Control

Long Description:

Return to Summary Table

Table 4-517. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0700h

Figure 4-237. TPCC0_AETCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RES65														
RW	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES65		ENDINT						RES66	TYPE	STRTEVT					
RO		RW						RO	RW	RW					
0		0						0	0	0					

Access Types Legend

Table 4-518. AETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	RW	0h	AET Enable: EN = 0 : AET event generation is disabled. EN = 1 : AET event generation is enabled.
30 - 14	RES65	RO	0h	RESERVE FIELD
13 - 8	ENDINT	RW	0h	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted (low)
7	RES66	RO	0h	RESERVE FIELD
6	TYPE	RW	0h	AET Event Type: TYPE = 0 : Event specified by STARTEVT applies to DMA Events (set by ER ESR or CER) TYPE = 1 : Event specified by STARTEVT applies to QDMA Events
5 - 0	STRTEVT	RW	0h	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted (high)

4.6.49 TPCC0_AETSTAT Register (Offset = 704h) [reset = h]

Short Description: Advanced Event Trigger Stat

Long Description:

Return to Summary Table

Table 4-519. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0704h

Figure 4-238. TPCC0_AETSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES67															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES67															STAT
RO															RO
0															0

Access Types Legend

Table 4-520. AETSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES67	RO	0h	RESERVE FIELD
0	STAT	RO	0h	AET Status: AETSTAT = 0 : tpcc_aet is currently low. AETSTAT = 1 : tpcc_aet is currently high.

4.6.50 TPCC0_AETCMD Register (Offset = 708h) [reset = h]

Short Description: AET Command

Long Description:

Return to Summary Table

Table 4-521. Instance Table

Instance Name	Physical Address
TPCC0	52A0 0708h

Figure 4-239. TPCC0_AETCMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES68															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES68															CLR
RO															WO
0															0

Access Types Legend

Table 4-522. AETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES68	RO	0h	RESERVE FIELD
0	CLR	WO	0h	AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect..

4.6.51 TPCC0_ER Register (Offset = 1000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

Return to Summary Table

Table 4-523. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1000h

Figure 4-240. TPCC0_ER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-524. ER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-524. ER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.52 TPCC0_ERH Register (Offset = 1004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-525. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1004h

Figure 4-241. TPCC0_ERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-526. ERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-526. ERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.53 TPCC0_ECR Register (Offset = 1008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-527. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1008h

Figure 4-242. TPCC0_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-528. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-528. ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.54 TPCC0_ECRH Register (Offset = 100Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-529. Instance Table

Instance Name	Physical Address
TPCC0	52A0 100Ch

Figure 4-243. TPCC0_ECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-530. ECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-530. ECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.55 TPCC0_ESR Register (Offset = 1010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-531. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1010h

Figure 4-244. TPCC0_ESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-532. ESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-532. ESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.56 TPCC0_ESRH Register (Offset = 1014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-533. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1014h

Figure 4-245. TPCC0_ESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-534. ESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-534. ESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.57 TPCC0_CER Register (Offset = 1018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-535. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1018h

Figure 4-246. TPCC0_CER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-536. CER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-536. CER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.58 TPCC0_CERH Register (Offset = 101Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-537. Instance Table

Instance Name	Physical Address
TPCC0	52A0 101Ch

Figure 4-247. TPCC0_CERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-538. CERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-538. CERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.59 TPCC0_EER Register (Offset = 1020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-539. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1020h

Figure 4-248. TPCC0_EER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-540. EER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-540. EER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.60 TPCC0_EERH Register (Offset = 1024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-541. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1024h

Figure 4-249. TPCC0_EERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-542. EERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-542. EERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.61 TPCC0_EECR Register (Offset = 1028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-543. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1028h

Figure 4-250. TPCC0_EECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-544. EECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-544. EECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.62 TPCC0_EECRH Register (Offset = 102Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-545. Instance Table

Instance Name	Physical Address
TPCC0	52A0 102Ch

Figure 4-251. TPCC0_EECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-546. EECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-546. EECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.63 TPCC0_EESR Register (Offset = 1030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-547. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1030h

Figure 4-252. TPCC0_EESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-548. EESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-548. EESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.64 TPCC0_EESRH Register (Offset = 1034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-549. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1034h

Figure 4-253. TPCC0_EESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-550. EESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-550. EESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.65 TPCC0_SER Register (Offset = 1038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-551. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1038h

Figure 4-254. TPCC0_SER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-552. SER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7

Table 4-552. SER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.66 TPCC0_SERH Register (Offset = 103Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-553. Instance Table

Instance Name	Physical Address
TPCC0	52A0 103Ch

Figure 4-255. TPCC0_SERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-554. SERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39

Table 4-554. SERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.67 TPCC0_SECR Register (Offset = 1040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-555. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1040h

Figure 4-256. TPCC0_SECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-556. SECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7

Table 4-556. SECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.68 TPCC0_SECRH Register (Offset = 1044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-557. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1044h

Figure 4-257. TPCC0_SECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-558. SECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39

Table 4-558. SECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.69 TPCC0_IER Register (Offset = 1050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-559. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1050h

Figure 4-258. TPCC0_IER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-560. IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7

Table 4-560. IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.6.70 TPCC0_IERH Register (Offset = 1054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-561. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1054h

Figure 4-259. TPCC0_IERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-562. IERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39

Table 4-562. IERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.6.71 TPCC0_IECR Register (Offset = 1058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-563. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1058h

Figure 4-260. TPCC0_IECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-564. IECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-564. IECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.72 TPCC0_IECRH Register (Offset = 105Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-565. Instance Table

Instance Name	Physical Address
TPCC0	52A0 105Ch

Figure 4-261. TPCC0_IECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-566. IECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-566. IECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.73 TPCC0_IESR Register (Offset = 1060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-567. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1060h

Figure 4-262. TPCC0_IESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-568. IESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-568. IESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.74 TPCC0_IESRH Register (Offset = 1064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-569. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1064h

Figure 4-263. TPCC0_IESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-570. IESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-570. IESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.75 TPCC0_IPR Register (Offset = 1068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-571. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1068h

Figure 4-264. TPCC0_IPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-572. IPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6

Table 4-572. IPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.6.76 TPCC0_IPRH Register (Offset = 106Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-573. Instance Table

Instance Name	Physical Address
TPCC0	52A0 106Ch

Figure 4-265. TPCC0_IPRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-574. IPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38

Table 4-574. IPRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.6.77 TPCC0_ICR Register (Offset = 1070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-575. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1070h

Figure 4-266. TPCC0_ICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-576. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-576. ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.78 TPCC0_ICRH Register (Offset = 1074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-577. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1074h

Figure 4-267. TPCC0_ICRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-578. ICRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39

Table 4-578. ICRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.79 TPCC0_IEVAL Register (Offset = 1078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

Return to Summary Table

Table 4-579. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1078h

Figure 4-268. TPCC0_IEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES69															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES69														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-580. IEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES69	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

4.6.80 TPCC0_QER Register (Offset = 1080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

Return to Summary Table

Table 4-581. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1080h

Figure 4-269. TPCC0_QER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES70															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES70								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-582. QER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES70	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.81 TPCC0_QEER Register (Offset = 1084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

Return to Summary Table

Table 4-583. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1084h

Figure 4-270. TPCC0_QEER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES71															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES71								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-584. QEER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES71	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.82 TPCC0_QEECR Register (Offset = 1088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-585. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1088h

Figure 4-271. TPCC0_QEECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES72															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES72								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-586. QEECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES72	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.83 TPCC0_QEESR Register (Offset = 108Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-587. Instance Table

Instance Name	Physical Address
TPCC0	52A0 108Ch

Figure 4-272. TPCC0_QEESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES73								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-588. QEESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES73	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.84 TPCC0_QSER Register (Offset = 1090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-589. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1090h

Figure 4-273. TPCC0_QSER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES74															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES74								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-590. QSER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES74	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.85 TPCC0_QSECR Register (Offset = 1094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-591. Instance Table

Instance Name	Physical Address
TPCC0	52A0 1094h

Figure 4-274. TPCC0_QSECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES75															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES75								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-592. QSECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES75	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.86 TPCC0_ER_RN Register (Offset = 2000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

Return to Summary Table

Table 4-593. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2000h

Figure 4-275. TPCC0_ER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-594. ER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-594. ER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.87 TPCC0_ERH_RN Register (Offset = 2004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-595. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2004h

Figure 4-276. TPCC0_ERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-596. ERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-596. ERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.88 TPCC0_ECR_RN Register (Offset = 2008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-597. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2008h

Figure 4-277. TPCC0_ECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-598. ECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-598. ECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.89 TPCC0_ECRH_RN Register (Offset = 200Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-599. Instance Table

Instance Name	Physical Address
TPCC0	52A0 200Ch

Figure 4-278. TPCC0_ECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-600. ECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-600. ECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.90 TPCC0_ESR_RN Register (Offset = 2010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-601. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2010h

Figure 4-279. TPCC0_ESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-602. ESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-602. ESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.91 TPCC0_ESRH_RN Register (Offset = 2014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-603. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2014h

Figure 4-280. TPCC0_ESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-604. ESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-604. ESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.92 TPCC0_CER_RN Register (Offset = 2018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-605. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2018h

Figure 4-281. TPCC0_CER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-606. CER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-606. CER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.93 TPCC0_CERH_RN Register (Offset = 201Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-607. Instance Table

Instance Name	Physical Address
TPCC0	52A0 201Ch

Figure 4-282. TPCC0_CERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-608. CERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-608. CERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.94 TPCC0_EER_RN Register (Offset = 2020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-609. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2020h

Figure 4-283. TPCC0_EER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-610. EER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-610. EER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.95 TPCC0_EERH_RN Register (Offset = 2024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-611. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2024h

Figure 4-284. TPCC0_EERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-612. EERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-612. EERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.96 TPCC0_EECR_RN Register (Offset = 2028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-613. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2028h

Figure 4-285. TPCC0_EECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-614. EECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-614. EECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.97 TPCC0_EECRH_RN Register (Offset = 202Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-615. Instance Table

Instance Name	Physical Address
TPCC0	52A0 202Ch

Figure 4-286. TPCC0_EECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-616. EECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-616. EECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.98 TPCC0_EESR_RN Register (Offset = 2030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-617. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2030h

Figure 4-287. TPCC0_EESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-618. EESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-618. EESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.99 TPCC0_EESRH_RN Register (Offset = 2034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-619. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2034h

Figure 4-288. TPCC0_EESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-620. EESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-620. EESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.100 TPCC0_SER_RN Register (Offset = 2038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-621. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2038h

Figure 4-289. TPCC0_SER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-622. SER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7

Table 4-622. SER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.101 TPCC0_SERH_RN Register (Offset = 203Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-623. Instance Table

Instance Name	Physical Address
TPCC0	52A0 203Ch

Figure 4-290. TPCC0_SERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-624. SERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39

Table 4-624. SERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.6.102 TPCC0_SECR_RN Register (Offset = 2040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-625. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2040h

Figure 4-291. TPCC0_SECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-626. SECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7

Table 4-626. SECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.103 TPCC0_SECRH_RN Register (Offset = 2044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-627. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2044h

Figure 4-292. TPCC0_SECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-628. SECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39

Table 4-628. SECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.6.104 TPCC0_IER_RN Register (Offset = 2050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-629. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2050h

Figure 4-293. TPCC0_IER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-630. IER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7

Table 4-630. IER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.6.105 TPCC0_IERH_RN Register (Offset = 2054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-631. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2054h

Figure 4-294. TPCC0_IERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-632. IERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39

Table 4-632. IERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.6.106 TPCC0_IECR_RN Register (Offset = 2058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-633. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2058h

Figure 4-295. TPCC0_IECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-634. IECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-634. IECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.107 TPCC0_IECRH_RN Register (Offset = 205Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-635. Instance Table

Instance Name	Physical Address
TPCC0	52A0 205Ch

Figure 4-296. TPCC0_IECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-636. IECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-636. IECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.108 TPCC0_IESR_RN Register (Offset = 2060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-637. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2060h

Figure 4-297. TPCC0_IESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-638. IESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-638. IESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.109 TPCC0_IESRH_RN Register (Offset = 2064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-639. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2064h

Figure 4-298. TPCC0_IESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-640. IESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-640. IESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.110 TPCC0_IPR_RN Register (Offset = 2068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-641. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2068h

Figure 4-299. TPCC0_IPR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-642. IPR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6

Table 4-642. IPR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.6.111 TPCC0_IPRH_RN Register (Offset = 206Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-643. Instance Table

Instance Name	Physical Address
TPCC0	52A0 206Ch

Figure 4-300. TPCC0_IPRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-644. IPRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38

Table 4-644. IPRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.6.112 TPCC0_ICR_RN Register (Offset = 2070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-645. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2070h

Figure 4-301. TPCC0_ICR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-646. ICR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-646. ICR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.6.113 TPCC0_ICRH_RN Register (Offset = 2074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-647. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2074h

Figure 4-302. TPCC0_ICRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-648. ICRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39

Table 4-648. ICRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.6.114 TPCC0_IEVAL_RN Register (Offset = 2078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

Return to Summary Table

Table 4-649. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2078h

Figure 4-303. TPCC0_IEVAL_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES76															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES76														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-650. IEVAL_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES76	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

4.6.115 TPCC0_QER_RN Register (Offset = 2080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

Return to Summary Table

Table 4-651. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2080h

Figure 4-304. TPCC0_QER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES77															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES77								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-652. QER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES77	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.116 TPCC0_QEER_RN Register (Offset = 2084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

Return to Summary Table

Table 4-653. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2084h

Figure 4-305. TPCC0_QEER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES78															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES78								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-654. QEER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES78	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.117 TPCC0_QEECR_RN Register (Offset = 2088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-655. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2088h

Figure 4-306. TPCC0_QEECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES79															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES79								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-656. QEECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES79	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.118 TPCC0_QEESR_RN Register (Offset = 208Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-657. Instance Table

Instance Name	Physical Address
TPCC0	52A0 208Ch

Figure 4-307. TPCC0_QEESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES80															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES80								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-658. QEESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES80	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.119 TPCC0_QSER_RN Register (Offset = 2090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-659. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2090h

Figure 4-308. TPCC0_QSER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES81															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES81								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-660. QSER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES81	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.6.120 TPCC0_QSECR_RN Register (Offset = 2094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-661. Instance Table

Instance Name	Physical Address
TPCC0	52A0 2094h

Figure 4-309. TPCC0_QSECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES82															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES82								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-662. QSECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES82	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.6.121 TPCC0_OPT Register (Offset = 4000h) [reset = h]

Short Description: Options Parameter

Long Description:

Return to Summary Table

Table 4-663. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4000h

Figure 4-310. TPCC0_OPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRIV	RES83			PRIVID				ITCCHEN	TCCHEN	ITCINTEN	TCINTEN	WIMODE	RES84	TCC	
RO	RO			RO				RW	RW	RW	RW	RW	RO	RW	
0	0			0				0	0	0	0	0	0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				TCCMODE	FWID			RES85				STATIC	SYNCDIM	DAM	SAM
RW				RW	RW			RO				RW	RW	RW	RW
0				0	0			0				0	0	0	0

Access Types Legend

Table 4-664. OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV	RO	0h	Privilege level: privilege level (supervisor vs. user) for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege
30 - 28	RES83	RO	0h	RESERVE FIELD
27 - 24	PRIVID	RO	0h	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.
23	ITCCHEN	RW	0h	Intermediate transfer completion chaining enable: 0: Intermediate transfer complete chaining is disabled. 1: Intermediate transfer complete chaining is enabled.
22	TCCHEN	RW	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled.
21	ITCINTEN	RW	0h	Intermediate transfer completion interrupt enable: 0: Intermediate transfer complete interrupt is disabled. 1: Intermediate transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
20	TCINTEN	RW	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
19	WIMODE	RW	0h	Backward compatibility mode: 0: Normal operation 1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission (0 means 1 1 means 2 ...) and forces ACNT to be treated as a word-count (left shifted by 2 by hardware to create byte cnt for TR submission)
18	RES84	RO	0h	RESERVE FIELD
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER (bit CER[TCC]) for chaining or in IER (bit IER[TCC]) for interrupts.

Table 4-664. OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TCCMODE	RW	0h	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0: Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC (which was returned from the peripheral). 1: Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally .
10 - 8	FWID	RW	0h	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC.
7 - 4	RES85	RO	0h	RESERVE FIELD
3	STATIC	RW	0h	Static Entry: 0: Entry is updated as normal 1: Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed.
2	SYNCDIM	RW	0h	Transfer Synchronization Dimension: 0: A-Sync Each event triggers the transfer of ACNT elements. 1: AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements
1	DAM	RW	0h	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0: INCR Dst addressing within an array increments. Dst is not a FIFO. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0: INCR Src addressing within an array increments. Source is not a FIFO. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.122 TPCC0_SRC Register (Offset = 4004h) [reset = h]

Short Description: Source Address

Long Description:

Return to Summary Table

Table 4-665. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4004h

Figure 4-311. TPCC0_SRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRC															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC															
RW															
0															

Access Types Legend

Table 4-666. SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SRC	RW	0h	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

4.6.123 TPCC0_ABCNT Register (Offset = 4008h) [reset = h]

Short Description: A and B byte count

Long Description:

Return to Summary Table

Table 4-667. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4008h

Figure 4-312. TPCC0_ABCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-668. ABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 (64K-1 arrays). BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ...
15 - 0	ACNT	RW	0h	ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes (64K-1 bytes). ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation (to translate between a word count and a byte count) will dropthe 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT.

4.6.124 TPCC0_DST Register (Offset = 400Ch) [reset = h]

Short Description: Destination Address

Long Description:

Return to Summary Table

Table 4-669. Instance Table

Instance Name	Physical Address
TPCC0	52A0 400Ch

Figure 4-313. TPCC0_DST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DST															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST															
RW															
0															

Access Types Legend

Table 4-670. DST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DST	RW	0h	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

4.6.125 TPCC0_BIDX Register (Offset = 4010h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-671. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4010h

Figure 4-314. TPCC0_BIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-672. BIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value (2's complement) used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers.
15 - 0	SBIDX	RW	0h	Source 2nd Dimension Index: SBIDX is a 16-bit signed value (2's complement) used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.

4.6.126 TPCC0_LNK Register (Offset = 4014h) [reset = h]

Short Description: Link and Reload parameters

Long Description:

Return to Summary Table

Table 4-673. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4014h

Figure 4-315. TPCC0_LNK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNTRLD															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK															
RW															
0															

Access Types Legend

Table 4-674. LNK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNTRLD	RW	0h	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT (conceptually) reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field.
15 - 0	LINK	RW	0h	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination (i.e. after count fields are decremented to '0') with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000 thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case (5-lsbs) behavior is undefined forthe user (i.e. don't have to test it). In the former case (2 msbs) user should be able to take advantage of this feature (i.e. do have to test it). If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field.

4.6.127 TPCC0_CIDX Register (Offset = 4018h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-675. Instance Table

Instance Name	Physical Address
TPCC0	52A0 4018h

Figure 4-316. TPCC0_CIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCIDX															
RW															
0															

Access Types Legend

Table 4-676. CIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DCIDX	RW	0h	Destination Frame Index: DCIDX is a 16-bit signed value (2's complement) used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by DST address) to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame.
15 - 0	SCIDX	RW	0h	Source Frame Index: SCIDX is a 16-bit signed value (2's complement) used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by SRC address) to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame.

4.6.128 TPCC0_CCNT Register (Offset = 401Ch) [reset = h]

Short Description: C byte count

Long Description:

Return to Summary Table

Table 4-677. Instance Table

Instance Name	Physical Address
TPCC0	52A0 401Ch

Figure 4-317. TPCC0_CCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES86															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT															
RW															
0															

Access Types Legend

Table 4-678. CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES86	RO	0h	RESERVE FIELD
15 - 0	CCNT	RW	0h	CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 (64K-1 frames). CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no affect on CCNT operation.

4.6.129 TPTC00_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

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Table 4-679. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0000h
TPTC01	52A6 0000h

Figure 4-318. TPTC00_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		NONE		RO											
1		0		0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
1				11				0		1					

Access Types Legend

Table 4-680. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
	RESERVED	NONE		Reserved
27 - 16	FUNC	RO	0h	Function indicates a software compatible module family.
15 - 11	RTL	RO	1h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	1h	Minor Revision

4.6.130 TPTC00_TCCFG Register (Offset = 4h) [reset = h]

Short Description: TC Configuration Register

Long Description:

Return to Summary Table

Table 4-681. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0004h
TPTC01	52A6 0004h

Figure 4-319. TPTC00_TCCFG Name Register

15	14	13	12	11	10	9	8
RESERVED						DREGDEPTH	
NONE						RO	
0						10	
7	6	5	4	3	2	1	0
RESERVED		BUSWIDTH		RESERVED		FIFOSIZE	
NONE		RO		NONE		RO	
0		10		0		100	

Access Types Legend

Table 4-682. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 8	DREGDEPTH	RO	Ah	Dst Register FIFO Depth Parameterization
	RESERVED	NONE		Reserved
5 - 4	BUSWIDTH	RO	Ah	Bus Width Parameterization
	RESERVED	NONE		Reserved
2 - 0	FIFOSIZE	RO	64h	Fifo Size Parameterization

4.6.131 TPTC00_TCSTAT Register (Offset = 100h) [reset = h]

Short Description: TC Status Register

Long Description:

Return to Summary Table

Table 4-683. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0100h
TPTC01	52A6 0100h

Figure 4-320. TPTC00_TCSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED		DFSTRTPTR		RESERVED			ACTV
NONE		RO		NONE			RO
0		0		0			1
7	6	5	4	3	2	1	0
RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE	RO			NONE	RO	RO	RO
0	0			0	0	0	0

Access Types Legend

Table 4-684. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 12	DFSTRTPTR	RO	0h	Dst FIFO Start PointerRepresents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
	RESERVED	NONE		Reserved
8	ACTV	RO	1h	Channel ActiveChannel Active is a logical-OR of each of the BUSY/ ACTV signals. The ACTV bit must remain high through the life of a TR.ACTV = 0 : Channel is idle.ACTV = 1 : Channel is busy.
	RESERVED	NONE		Reserved
6 - 4	DSTACTV	RO	0h	Destination Active StateSpecifies the number of TRs that are resident in the Dst Register FIFO at a given instant.Legal values are constrained by the DSTREGDEPTH parameter.
	RESERVED	NONE		Reserved
2	WSACTV	RO	0h	Write Status ActiveWSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands.WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	RO	0h	Source Active StateSRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	RO	0h	Program Register Set BusyPROGBUSY = 0 : Prog set idle and is available for programming.PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

4.6.132 TPTC00_INTSTAT Register (Offset = 104h) [reset = h]

Short Description: Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-685. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0104h
TPTC01	52A6 0104h

Figure 4-321. TPTC00_INTSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RO	RO
0						0	0

Access Types Legend

Table 4-686. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RO	0h	TR Done Event Status:TRDONE = 0 : Condition not detected.TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	RO	0h	Program Set Empty Event Status:PROGEMPTY = 0 : Condition not detected.PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

4.6.133 TPTC00_INTEN Register (Offset = 108h) [reset = h]

Short Description: Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-687. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0108h
TPTC01	52A6 0108h

Figure 4-322. TPTC00_INTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-688. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RW	0h	TR Done Event Enable:INTEN.TRDONE = 0 : TRDONE Event is disabled.INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	RW	0h	Program Set Empty Event Enable:INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled.INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

4.6.134 TPTC00_INTCLR Register (Offset = 10Ch) [reset = h]

Short Description: Interrupt Clear Register

Long Description:

Return to Summary Table

Table 4-689. Instance Table

Instance Name	Physical Address
TPTC00	52A4 010Ch
TPTC01	52A6 010Ch

Figure 4-323. TPTC00_INTCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-690. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	WO	0h	TR Done Event Clear:INTCLR.TRDONE = 0 : Writes of '0' have no effect.INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	WO	0h	Program Set Empty Event Clear:INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect.INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

4.6.135 TPTC00_INTCMD Register (Offset = 110h) [reset = h]

Short Description: Interrupt Command Register

Long Description:

Return to Summary Table

Table 4-691. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0110h
TPTC01	52A6 0110h

Figure 4-324. TPTC00_INTCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-692. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC interrupt:Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC interruptWrite of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.Writes of '0' have no affect.

4.6.136 TPTC00_ERRSTAT Register (Offset = 120h) [reset = h]

Short Description: Error Status Register

Long Description:

Return to Summary Table

Table 4-693. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0120h
TPTC01	52A6 0120h

Figure 4-325. TPTC00_ERRSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RO	RO	NONE	RO
0				0	0	0	0

Access Types Legend

Table 4-694. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RO	0h	MMR Address Error:MMRAERR = 0 : Condition not detected.MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	RO	0h	TR Error:TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
	RESERVED	NONE		Reserved
0	BUSERR	RO	0h	Bus Error Event:BUSERR = 0: Condition not detected.BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

4.6.137 TPTC00_ERREN Register (Offset = 124h) [reset = h]

Short Description: Error Enable Register

Long Description:

Return to Summary Table

Table 4-695. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0124h
TPTC01	52A6 0124h

Figure 4-326. TPTC00_ERREN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RW	RW	NONE	RW
0				0	0	0	0

Access Types Legend

Table 4-696. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RW	0h	Interrupt enable for ERRSTAT.MMRAERR:ERREN.MMRAERR = 0 : BUSERR is disabled.ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	RW	0h	Interrupt enable for ERRSTAT.TRERR:ERREN.TRERR = 0 : BUSERR is disabled.ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
	RESERVED	NONE		Reserved
0	BUSERR	RW	0h	Interrupt enable for ERRSTAT.BUSERR:ERREN.BUSERR = 0 : BUSERR is disabled.ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

4.6.138 TPTC00_ERRCLR Register (Offset = 128h) [reset = h]

Short Description: Error Clear Register

Long Description:

Return to Summary Table

Table 4-697. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0128h
TPTC01	52A6 0128h

Figure 4-327. TPTC00_ERRCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				WO	WO	NONE	WO
0				0	0	0	0

Access Types Legend

Table 4-698. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	WO	0h	Interrupt clear for ERRSTAT.MMRAERR:ERRCLR.MMRAERR = 0 : Writes of '0' have no effect.ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	WO	0h	Interrupt clear for ERRSTAT.TRERR:ERRCLR.TRERR = 0 : Writes of '0' have no effect.ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
	RESERVED	NONE		Reserved
0	BUSERR	WO	0h	Interrupt clear for ERRSTAT.BUSERR:ERRCLR.BUSERR = 0 : Writes of '0' have no effect.ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

4.6.139 TPTC00_ERRDET Register (Offset = 12Ch) [reset = h]

Short Description: Error Details Register

Long Description:

Return to Summary Table

Table 4-699. Instance Table

Instance Name	Physical Address
TPTC00	52A4 012Ch
TPTC01	52A6 012Ch

Figure 4-328. TPTC00_ERRDET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TCCHEN	TCINTEN								
NONE						RO	RO								
0						0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TCC						RESERVED				STAT			
NONE		RO						NONE				RO			
0		0						0				0			

Access Types Legend

Table 4-700. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TCCHEN	RO	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	RO	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
13 - 8	TCC	RO	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
3 - 0	STAT	RO	0h	Transaction Status:Stores the non-zero status/error code that was detected on the read status or write status bus.MS-bit effectively serves as the read vs. write error code.If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.Encoding of errors matches the CBA spec.

4.6.140 TPTC00_ERRCMD Register (Offset = 130h) [reset = h]

Short Description: Error Command Register

Long Description:

Return to Summary Table

Table 4-701. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0130h
TPTC01	52A6 0130h

Figure 4-329. TPTC00_ERRCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-702. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC error interrupt:Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC error interruptWrite of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.Writes of '0' have no affect.

4.6.141 TPTC00_RDRATE Register (Offset = 140h) [reset = h]

Short Description: Read Rate Register

Long Description:

Return to Summary Table

Table 4-703. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0140h
TPTC01	52A6 0140h

Figure 4-330. TPTC00_RDRATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RDRATE		
NONE					RW		
0					0		

Access Types Legend

Table 4-704. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RDRATE	RW	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

4.6.142 TPTC00_POPT Register (Offset = 200h) [reset = h]

Short Description: Prog Set Options

Long Description:

Return to Summary Table

Table 4-705. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0200h
TPTC01	52A6 0200h

Figure 4-331. TPTC00_POPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-706. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.143 TPTC00_PSRC Register (Offset = 204h) [reset = h]

Short Description: Prog Set Src Address

Long Description:

Return to Summary Table

Table 4-707. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0204h
TPTC01	52A6 0204h

Figure 4-332. TPTC00_PSRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RW															
0															

Access Types Legend

Table 4-708. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RW	0h	Source address for Program Register Set

4.6.144 TPTC00_PCNT Register (Offset = 208h) [reset = h]

Short Description: Prog Set Count

Long Description:

Return to Summary Table

Table 4-709. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0208h
TPTC01	52A6 0208h

Figure 4-333. TPTC00_PCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-710. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15 - 0	ACNT	RW	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.6.145 TPTC00_PDST Register (Offset = 20Ch) [reset = h]

Short Description: Prog Set Dst Address

Long Description:

Return to Summary Table

Table 4-711. Instance Table

Instance Name	Physical Address
TPTC00	52A4 020Ch
TPTC01	52A6 020Ch

Figure 4-334. TPTC00_PDST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RW															
0															

Access Types Legend

Table 4-712. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RW	0h	Destination address for Program Register Set

4.6.146 TPTC00_PBIDX Register (Offset = 210h) [reset = h]

Short Description: Prog Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-713. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0210h
TPTC01	52A6 0210h

Figure 4-335. TPTC00_PBIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-714. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Dest B-Idx for Program Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RW	0h	Source B-Idx for Program Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.147 TPTC00_PMPPRXY Register (Offset = 214h) [reset = h]

Short Description: Prog Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-715. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0214h
TPTC01	52A6 0214h

Figure 4-336. TPTC00_PMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-716. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.148 TPTC00_SAOPT Register (Offset = 240h) [reset = h]

Short Description: Src Actv Set Options

Long Description:

Return to Summary Table

Table 4-717. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0240h
TPTC01	52A6 0240h

Figure 4-337. TPTC00_SAOPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-718. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.149 TPTC00_SASRC Register (Offset = 244h) [reset = h]

Short Description: Src Actv Set Src Address

Long Description:

Return to Summary Table

Table 4-719. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0244h
TPTC01	52A6 0244h

Figure 4-338. TPTC00_SASRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-720. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address for Source Active Register Set

4.6.150 TPTC00_SACNT Register (Offset = 248h) [reset = h]

Short Description: Src Actv Set A-Count

Long Description:

Return to Summary Table

Table 4-721. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0248h
TPTC01	52A6 0248h

Figure 4-339. TPTC00_SACNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-722. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.6.151 TPTC00_SADST Register (Offset = 24Ch) [reset = h]

Short Description: Src Actv Set Dst Address

Long Description:

Return to Summary Table

Table 4-723. Instance Table

Instance Name	Physical Address
TPTC00	52A4 024Ch
TPTC01	52A6 024Ch

Figure 4-340. TPTC00_SADST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-724. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Source Active Register Set

4.6.152 TPTC00_SABIDX Register (Offset = 250h) [reset = h]

Short Description: Src Actv Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-725. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0250h
TPTC01	52A6 0250h

Figure 4-341. TPTC00_SABIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-726. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Source Active Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Source B-Idx for Source Active Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.153 TPTC00_SAMPPRXY Register (Offset = 254h) [reset = h]

Short Description: Src Actv Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-727. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0254h
TPTC01	52A6 0254h

Figure 4-342. TPTC00_SAMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-728. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.154 TPTC00_SACNTRLD Register (Offset = 258h) [reset = h]

Short Description: Src Actv Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-729. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0258h
TPTC01	52A6 0258h

Figure 4-343. TPTC00_SACNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-730. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.6.155 TPTC00_SASRCBREF Register (Offset = 25Ch) [reset = h]

Short Description: Src Actv Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-731. Instance Table

Instance Name	Physical Address
TPTC00	52A4 025Ch
TPTC01	52A6 025Ch

Figure 4-344. TPTC00_SASRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-732. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Source Active Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.6.156 TPTC00_SADSTBREF Register (Offset = 260h) [reset = h]

Short Description: Src Actv Set Dst Addr B-Reference

Long Description:

Return to Summary Table

Table 4-733. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0260h
TPTC01	52A6 0260h

Figure 4-345. TPTC00_SADSTBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF															
RO															
0															

Access Types Legend

Table 4-734. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDRBREF	RO	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

4.6.157 TPTC00_SABCNT Register (Offset = 264h) [reset = h]

Short Description: Src Actv Set B-Count

Long Description:

Return to Summary Table

Table 4-735. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0264h
TPTC01	52A6 0264h

Figure 4-346. TPTC00_SABCNT Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-736. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Dimension count:Number of arrays to be transferred where each array is ACNT in length.Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

4.6.158 TPTC00_DFCNTRLD Register (Offset = 280h) [reset = h]

Short Description: Dst FIFO Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-737. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0280h
TPTC01	52A6 0280h

Figure 4-347. TPTC00_DFCNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-738. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.6.159 TPTC00_DFSRCBREF Register (Offset = 284h) [reset = h]

Short Description: Dst FIFO Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-739. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0284h
TPTC01	52A6 0284h

Figure 4-348. TPTC00_DFSRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-740. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Destination FIFO Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.6.160 TPTC00_DFOPT0 Register (Offset = 300h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-741. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0300h
TPTC01	52A6 0300h

Figure 4-349. TPTC00_DFOPT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-742. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.161 TPTC00_DFSRC0 Register (Offset = 304h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-743. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0304h
TPTC01	52A6 0304h

Figure 4-350. TPTC00_DFSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-744. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.6.162 TPTC00_DFACNT0 Register (Offset = 308h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-745. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0308h
TPTC01	52A6 0308h

Figure 4-351. TPTC00_DFACNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-746. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.6.163 TPTC00_DFDST0 Register (Offset = 30Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-747. Instance Table

Instance Name	Physical Address
TPTC00	52A4 030Ch
TPTC01	52A6 030Ch

Figure 4-352. TPTC00_DFDST0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-748. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.6.164 TPTC00_DFBIDX0 Register (Offset = 310h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-749. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0310h
TPTC01	52A6 0310h

Figure 4-353. TPTC00_DFBIDX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-750. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.165 TPTC00_DFMPPRXY0 Register (Offset = 314h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-751. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0314h
TPTC01	52A6 0314h

Figure 4-354. TPTC00_DFMPPRXY0 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-752. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.166 TPTC00_DFBCNT0 Register (Offset = 318h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-753. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0318h
TPTC01	52A6 0318h

Figure 4-355. TPTC00_DFBCNT0 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-754. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.6.167 TPTC00_DFOPT1 Register (Offset = 340h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-755. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0340h
TPTC01	52A6 0340h

Figure 4-356. TPTC00_DFOPT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-756. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.168 TPTC00_DFSRC1 Register (Offset = 344h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-757. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0344h
TPTC01	52A6 0344h

Figure 4-357. TPTC00_DFSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-758. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.6.169 TPTC00_DFACNT1 Register (Offset = 348h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-759. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0348h
TPTC01	52A6 0348h

Figure 4-358. TPTC00_DFACNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-760. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.6.170 TPTC00_DFDST1 Register (Offset = 34Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-761. Instance Table

Instance Name	Physical Address
TPTC00	52A4 034Ch
TPTC01	52A6 034Ch

Figure 4-359. TPTC00_DFDST1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-762. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.6.171 TPTC00_DFBIDX1 Register (Offset = 350h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-763. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0350h
TPTC01	52A6 0350h

Figure 4-360. TPTC00_DFBIDX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-764. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.172 TPTC00_DFMPPRXY1 Register (Offset = 354h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-765. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0354h
TPTC01	52A6 0354h

Figure 4-361. TPTC00_DFMPPRXY1 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-766. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.173 TPTC00_DFBCNT1 Register (Offset = 358h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-767. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0358h
TPTC01	52A6 0358h

Figure 4-362. TPTC00_DFBCNT1 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-768. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.6.174 TPTC01_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-769. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0000h
TPTC01	52A6 0000h

Figure 4-363. TPTC01_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		NONE		RO											
1		0		0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
1				11				0		1					

Access Types Legend

Table 4-770. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
	RESERVED	NONE		Reserved
27 - 16	FUNC	RO	0h	Function indicates a software compatible module family.
15 - 11	RTL	RO	1h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	1h	Minor Revision

4.6.175 TPTC01_TCCFG Register (Offset = 4h) [reset = h]

Short Description: TC Configuration Register

Long Description:

Return to Summary Table

Table 4-771. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0004h
TPTC01	52A6 0004h

Figure 4-364. TPTC01_TCCFG Name Register

15	14	13	12	11	10	9	8
RESERVED						DREGDEPTH	
NONE						RO	
0						10	
7	6	5	4	3	2	1	0
RESERVED		BUSWIDTH		RESERVED		FIFOSIZE	
NONE		RO		NONE		RO	
0		10		0		100	

Access Types Legend

Table 4-772. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 8	DREGDEPTH	RO	Ah	Dst Register FIFO Depth Parameterization
	RESERVED	NONE		Reserved
5 - 4	BUSWIDTH	RO	Ah	Bus Width Parameterization
	RESERVED	NONE		Reserved
2 - 0	FIFOSIZE	RO	64h	Fifo Size Parameterization

4.6.176 TPTC01_TCSTAT Register (Offset = 100h) [reset = h]

Short Description: TC Status Register

Long Description:

Return to Summary Table

Table 4-773. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0100h
TPTC01	52A6 0100h

Figure 4-365. TPTC01_TCSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED		DFSTRTPTR		RESERVED			ACTV
NONE		RO		NONE			RO
0		0		0			1
7	6	5	4	3	2	1	0
RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE	RO			NONE	RO	RO	RO
0	0			0	0	0	0

Access Types Legend

Table 4-774. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 12	DFSTRTPTR	RO	0h	Dst FIFO Start PointerRepresents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
	RESERVED	NONE		Reserved
8	ACTV	RO	1h	Channel ActiveChannel Active is a logical-OR of each of the BUSY/ ACTV signals. The ACTV bit must remain high through the life of a TR.ACTV = 0 : Channel is idle.ACTV = 1 : Channel is busy.
	RESERVED	NONE		Reserved
6 - 4	DSTACTV	RO	0h	Destination Active StateSpecifies the number of TRs that are resident in the Dst Register FIFO at a given instant.Legal values are constrained by the DSTREGDEPTH parameter.
	RESERVED	NONE		Reserved
2	WSACTV	RO	0h	Write Status ActiveWSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands.WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	RO	0h	Source Active StateSRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	RO	0h	Program Register Set BusyPROGBUSY = 0 : Prog set idle and is available for programming.PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

4.6.177 TPTC01_INTSTAT Register (Offset = 104h) [reset = h]

Short Description: Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-775. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0104h
TPTC01	52A6 0104h

Figure 4-366. TPTC01_INTSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RO	RO
0						0	0

Access Types Legend

Table 4-776. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RO	0h	TR Done Event Status:TRDONE = 0 : Condition not detected.TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	RO	0h	Program Set Empty Event Status:PROGEMPTY = 0 : Condition not detected.PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

4.6.178 TPTC01_INTEN Register (Offset = 108h) [reset = h]

Short Description: Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-777. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0108h
TPTC01	52A6 0108h

Figure 4-367. TPTC01_INTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-778. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RW	0h	TR Done Event Enable:INTEN.TRDONE = 0 : TRDONE Event is disabled.INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	RW	0h	Program Set Empty Event Enable:INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled.INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

4.6.179 TPTC01_INTCLR Register (Offset = 10Ch) [reset = h]

Short Description: Interrupt Clear Register

Long Description:

Return to Summary Table

Table 4-779. Instance Table

Instance Name	Physical Address
TPTC00	52A4 010Ch
TPTC01	52A6 010Ch

Figure 4-368. TPTC01_INTCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-780. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	WO	0h	TR Done Event Clear:INTCLR.TRDONE = 0 : Writes of '0' have no effect.INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	WO	0h	Program Set Empty Event Clear:INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect.INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

4.6.180 TPTC01_INTCMD Register (Offset = 110h) [reset = h]

Short Description: Interrupt Command Register

Long Description:

Return to Summary Table

Table 4-781. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0110h
TPTC01	52A6 0110h

Figure 4-369. TPTC01_INTCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-782. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC interrupt:Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC interruptWrite of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.Writes of '0' have no affect.

4.6.181 TPTC01_ERRSTAT Register (Offset = 120h) [reset = h]

Short Description: Error Status Register

Long Description:

Return to Summary Table

Table 4-783. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0120h
TPTC01	52A6 0120h

Figure 4-370. TPTC01_ERRSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RO	RO	NONE	RO
0				0	0	0	0

Access Types Legend

Table 4-784. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RO	0h	MMR Address Error:MMRAERR = 0 : Condition not detected.MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	RO	0h	TR Error:TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
	RESERVED	NONE		Reserved
0	BUSERR	RO	0h	Bus Error Event:BUSERR = 0: Condition not detected.BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

4.6.182 TPTC01_ERREN Register (Offset = 124h) [reset = h]

Short Description: Error Enable Register

Long Description:

Return to Summary Table

Table 4-785. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0124h
TPTC01	52A6 0124h

Figure 4-371. TPTC01_ERREN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RW	RW	NONE	RW
0				0	0	0	0

Access Types Legend

Table 4-786. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RW	0h	Interrupt enable for ERRSTAT.MMRAERR:ERREN.MMRAERR = 0 : BUSERR is disabled.ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	RW	0h	Interrupt enable for ERRSTAT.TRERR:ERREN.TRERR = 0 : BUSERR is disabled.ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
	RESERVED	NONE		Reserved
0	BUSERR	RW	0h	Interrupt enable for ERRSTAT.BUSERR:ERREN.BUSERR = 0 : BUSERR is disabled.ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

4.6.183 TPTC01_ERRCLR Register (Offset = 128h) [reset = h]

Short Description: Error Clear Register

Long Description:

Return to Summary Table

Table 4-787. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0128h
TPTC01	52A6 0128h

Figure 4-372. TPTC01_ERRCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				WO	WO	NONE	WO
0				0	0	0	0

Access Types Legend

Table 4-788. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	WO	0h	Interrupt clear for ERRSTAT.MMRAERR:ERRCLR.MMRAERR = 0 : Writes of '0' have no effect.ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	WO	0h	Interrupt clear for ERRSTAT.TRERR:ERRCLR.TRERR = 0 : Writes of '0' have no effect.ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
	RESERVED	NONE		Reserved
0	BUSERR	WO	0h	Interrupt clear for ERRSTAT.BUSERR:ERRCLR.BUSERR = 0 : Writes of '0' have no effect.ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

4.6.184 TPTC01_ERRDET Register (Offset = 12Ch) [reset = h]

Short Description: Error Details Register

Long Description:

Return to Summary Table

Table 4-789. Instance Table

Instance Name	Physical Address
TPTC00	52A4 012Ch
TPTC01	52A6 012Ch

Figure 4-373. TPTC01_ERRDET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TCCHEN	TCINTEN								
NONE						RO	RO								
0						0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TCC						RESERVED				STAT			
NONE		RO						NONE				RO			
0		0						0				0			

Access Types Legend

Table 4-790. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TCCHEN	RO	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	RO	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
13 - 8	TCC	RO	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
3 - 0	STAT	RO	0h	Transaction Status:Stores the non-zero status/error code that was detected on the read status or write status bus.MS-bit effectively serves as the read vs. write error code.If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.Encoding of errors matches the CBA spec.

4.6.185 TPTC01_ERRCMD Register (Offset = 130h) [reset = h]

Short Description: Error Command Register

Long Description:

Return to Summary Table

Table 4-791. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0130h
TPTC01	52A6 0130h

Figure 4-374. TPTC01_ERRCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-792. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC error interrupt:Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC error interruptWrite of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.Writes of '0' have no affect.

4.6.186 TPTC01_RDRATE Register (Offset = 140h) [reset = h]

Short Description: Read Rate Register

Long Description:

Return to Summary Table

Table 4-793. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0140h
TPTC01	52A6 0140h

Figure 4-375. TPTC01_RDRATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RDRATE		
NONE					RW		
0					0		

Access Types Legend

Table 4-794. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RDRATE	RW	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

4.6.187 TPTC01_POPT Register (Offset = 200h) [reset = h]

Short Description: Prog Set Options

Long Description:

Return to Summary Table

Table 4-795. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0200h
TPTC01	52A6 0200h

Figure 4-376. TPTC01_POPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-796. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.188 TPTC01_PSRC Register (Offset = 204h) [reset = h]

Short Description: Prog Set Src Address

Long Description:

Return to Summary Table

Table 4-797. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0204h
TPTC01	52A6 0204h

Figure 4-377. TPTC01_PSRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RW															
0															

Access Types Legend

Table 4-798. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RW	0h	Source address for Program Register Set

4.6.189 TPTC01_PCNT Register (Offset = 208h) [reset = h]

Short Description: Prog Set Count

Long Description:

Return to Summary Table

Table 4-799. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0208h
TPTC01	52A6 0208h

Figure 4-378. TPTC01_PCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-800. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15 - 0	ACNT	RW	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.6.190 TPTC01_PDST Register (Offset = 20Ch) [reset = h]

Short Description: Prog Set Dst Address

Long Description:

Return to Summary Table

Table 4-801. Instance Table

Instance Name	Physical Address
TPTC00	52A4 020Ch
TPTC01	52A6 020Ch

Figure 4-379. TPTC01_PDST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RW															
0															

Access Types Legend

Table 4-802. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RW	0h	Destination address for Program Register Set

4.6.191 TPTC01_PBIDX Register (Offset = 210h) [reset = h]

Short Description: Prog Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-803. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0210h
TPTC01	52A6 0210h

Figure 4-380. TPTC01_PBIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-804. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Dest B-Idx for Program Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RW	0h	Source B-Idx for Program Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.192 TPTC01_PMPPRXY Register (Offset = 214h) [reset = h]

Short Description: Prog Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-805. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0214h
TPTC01	52A6 0214h

Figure 4-381. TPTC01_PMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-806. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.193 TPTC01_SAOPT Register (Offset = 240h) [reset = h]

Short Description: Src Actv Set Options

Long Description:

Return to Summary Table

Table 4-807. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0240h
TPTC01	52A6 0240h

Figure 4-382. TPTC01_SAOPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-808. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.194 TPTC01_SASRC Register (Offset = 244h) [reset = h]

Short Description: Src Actv Set Src Address

Long Description:

Return to Summary Table

Table 4-809. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0244h
TPTC01	52A6 0244h

Figure 4-383. TPTC01_SASRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-810. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address for Source Active Register Set

4.6.195 TPTC01_SACNT Register (Offset = 248h) [reset = h]

Short Description: Src Actv Set A-Count

Long Description:

Return to Summary Table

Table 4-811. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0248h
TPTC01	52A6 0248h

Figure 4-384. TPTC01_SACNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-812. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.6.196 TPTC01_SADST Register (Offset = 24Ch) [reset = h]

Short Description: Src Actv Set Dst Address

Long Description:

Return to Summary Table

Table 4-813. Instance Table

Instance Name	Physical Address
TPTC00	52A4 024Ch
TPTC01	52A6 024Ch

Figure 4-385. TPTC01_SADST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-814. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Source Active Register Set

4.6.197 TPTC01_SABIDX Register (Offset = 250h) [reset = h]

Short Description: Src Actv Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-815. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0250h
TPTC01	52A6 0250h

Figure 4-386. TPTC01_SABIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-816. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Source Active Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Source B-Idx for Source Active Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.198 TPTC01_SAMPPRXY Register (Offset = 254h) [reset = h]

Short Description: Src Actv Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-817. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0254h
TPTC01	52A6 0254h

Figure 4-387. TPTC01_SAMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-818. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.199 TPTC01_SACNTRLD Register (Offset = 258h) [reset = h]

Short Description: Src Actv Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-819. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0258h
TPTC01	52A6 0258h

Figure 4-388. TPTC01_SACNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-820. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.6.200 TPTC01_SASRCBREF Register (Offset = 25Ch) [reset = h]

Short Description: Src Actv Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-821. Instance Table

Instance Name	Physical Address
TPTC00	52A4 025Ch
TPTC01	52A6 025Ch

Figure 4-389. TPTC01_SASRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-822. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Source Active Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.6.201 TPTC01_SADSTBREF Register (Offset = 260h) [reset = h]

Short Description: Src Actv Set Dst Addr B-Reference

Long Description:

Return to Summary Table

Table 4-823. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0260h
TPTC01	52A6 0260h

Figure 4-390. TPTC01_SADSTBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF															
RO															
0															

Access Types Legend

Table 4-824. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDRBREF	RO	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

4.6.202 TPTC01_SABCNT Register (Offset = 264h) [reset = h]

Short Description: Src Actv Set B-Count

Long Description:

Return to Summary Table

Table 4-825. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0264h
TPTC01	52A6 0264h

Figure 4-391. TPTC01_SABCNT Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-826. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Dimension count:Number of arrays to be transferred where each array is ACNT in length.Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

4.6.203 TPTC01_DFCNTRLD Register (Offset = 280h) [reset = h]

Short Description: Dst FIFO Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-827. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0280h
TPTC01	52A6 0280h

Figure 4-392. TPTC01_DFCNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-828. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.6.204 TPTC01_DFSRCBREF Register (Offset = 284h) [reset = h]

Short Description: Dst FIFO Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-829. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0284h
TPTC01	52A6 0284h

Figure 4-393. TPTC01_DFSRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-830. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Destination FIFO Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.6.205 TPTC01_DFOPT0 Register (Offset = 300h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-831. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0300h
TPTC01	52A6 0300h

Figure 4-394. TPTC01_DFOPT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-832. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.206 TPTC01_DFSRC0 Register (Offset = 304h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-833. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0304h
TPTC01	52A6 0304h

Figure 4-395. TPTC01_DFSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-834. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.6.207 TPTC01_DFACNT0 Register (Offset = 308h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-835. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0308h
TPTC01	52A6 0308h

Figure 4-396. TPTC01_DFACNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-836. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.6.208 TPTC01_DFDST0 Register (Offset = 30Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-837. Instance Table

Instance Name	Physical Address
TPTC00	52A4 030Ch
TPTC01	52A6 030Ch

Figure 4-397. TPTC01_DFDST0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-838. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.6.209 TPTC01_DFBIDX0 Register (Offset = 310h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-839. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0310h
TPTC01	52A6 0310h

Figure 4-398. TPTC01_DFBIDX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-840. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.210 TPTC01_DFMPPRXY0 Register (Offset = 314h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-841. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0314h
TPTC01	52A6 0314h

Figure 4-399. TPTC01_DFMPPRXY0 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-842. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.211 TPTC01_DFBCNT0 Register (Offset = 318h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-843. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0318h
TPTC01	52A6 0318h

Figure 4-400. TPTC01_DFBCNT0 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-844. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.6.212 TPTC01_DFOPT1 Register (Offset = 340h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-845. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0340h
TPTC01	52A6 0340h

Figure 4-401. TPTC01_DFOPT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-846. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.6.213 TPTC01_DFSRC1 Register (Offset = 344h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-847. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0344h
TPTC01	52A6 0344h

Figure 4-402. TPTC01_DFSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-848. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.6.214 TPTC01_DFACNT1 Register (Offset = 348h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-849. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0348h
TPTC01	52A6 0348h

Figure 4-403. TPTC01_DFACNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-850. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.6.215 TPTC01_DFDST1 Register (Offset = 34Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-851. Instance Table

Instance Name	Physical Address
TPTC00	52A4 034Ch
TPTC01	52A6 034Ch

Figure 4-404. TPTC01_DFDST1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-852. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.6.216 TPTC01_DFBIDX1 Register (Offset = 350h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-853. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0350h
TPTC01	52A6 0350h

Figure 4-405. TPTC01_DFBIDX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-854. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.6.217 TPTC01_DFMPPRXY1 Register (Offset = 354h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-855. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0354h
TPTC01	52A6 0354h

Figure 4-406. TPTC01_DFMPPRXY1 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-856. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.6.218 TPTC01_DFBCNT1 Register (Offset = 358h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-857. Instance Table

Instance Name	Physical Address
TPTC00	52A4 0358h
TPTC01	52A6 0358h

Figure 4-407. TPTC01_DFBCNT1 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-858. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.6.219 DCC0_DCCGCTRL Register (Offset = 0h) [reset = h]

Short Description: Starts / stops the counters clears the error signal

Long Description:

Return to Summary Table

Table 4-859. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-408. DCC0_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONENA				SINGLESHOT				ERRENA				DCCENA			
RW				RW				RW				RW			
101				101				101				101			

Access Types Legend

Table 4-860. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RO	0h	Reserved
15 - 12	DONENA	RW	65h	The DONEENA bit enables/disables the done signal. 0101 = disabled & 1010 = enabled
11 - 8	SINGLESHOT	RW	65h	Single/Continuous checking mode. 0101 = Continuous & 1010 = Single
7 - 4	ERRENA	RW	65h	The ERRENA bit enables/disables the error signal. 0101 = disabled & 1010 = enabled
3 - 0	DCCENA	RW	65h	The DCCENA bit starts and stops the operation of the dcc 0101 = disabled & 1010 = enabled

4.6.220 DCC0_DCCREV Register (Offset = 4h) [reset = h]

Short Description: Module version

Long Description:

Return to Summary Table

Table 4-861. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-409. DCC0_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2	SCHEME			NU1		FUNC									
RO	RO			RO		RO									
0	100			0		0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		RTL				MAJOR				CUSTOM	MINOR				
RO		RO				RO				RO	RO				
0		1				0				0	100				

Access Types Legend

Table 4-862. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU2	RO	0h	Reserved
30 - 28	SCHEME	RO	64h	SCHEME. - (RO)
27 - 26	NU1	RO	0h	Reserved
25 - 14	FUNC	RO	0h	Functional release number - (RO)
13 - 9	RTL	RO	1h	Design Release Number - (RO)
8 - 6	MAJOR	RO	0h	Major Revision Number - (RO)
5	CUSTOM	RO	0h	Indicates a special version of the module. May not be supported by standard software - (RO)
4 - 0	MINOR	RO	64h	Minor revision number. - (RO)

4.6.221 DCC0_DCCCNTSEED0 Register (Offset = 8h) [reset = h]

Short Description: Seed value for the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-863. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-410. DCC0_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3												COUNTSEED0			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
RW															
0															

Access Types Legend

Table 4-864. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU3	RO	0h	Reserved
19 - 0	COUNTSEED0	RW	0h	The seed value for Counter 0. The seed value that gets loaded into counter 0 (clock source 0)

4.6.222 DCC0_DCCVALIDSEED0 Register (Offset = Ch) [reset = h]

Short Description: Seed value for the timeout counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-865. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-411. DCC0_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
RW															
0															

Access Types Legend

Table 4-866. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU4	RO	0h	Reserved
15 - 0	VALIDSEED0	RW	0h	The seed value for Valid Duration Counter 0.The seed value that gets loaded into the valid duration counter for clock source 0

4.6.223 DCC0_DCCCNTSEED1 Register (Offset = 10h) [reset = h]

Short Description: Seed value for the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-867. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-412. DCC0_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5												COUNTSEED1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
RW															
0															

Access Types Legend

Table 4-868. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU5	RO	0h	Reserved
19 - 0	COUNTSEED1	RW	0h	The seed value for Counter 1. The seed value that gets loaded into counter 1 (clock source 1

4.6.224 DCC0_DCCSTAT Register (Offset = 14h) [reset = h]

Short Description: Contains the error & done flag bit

Long Description:

Return to Summary Table

Table 4-869. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-413. DCC0_DCCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6														DONE	ERR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-870. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU6	RO	0h	Reserved
1	DONE	RW	0h	Indicates whether or not an done has occured. Writing a 1 to this bit clears the flag.
0	ERR	RW	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag.

4.6.225 DCC0_DCCCNT0 Register (Offset = 18h) [reset = h]

Short Description: Value of the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-871. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-414. DCC0_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7												COUNT0			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
RO															
0															

Access Types Legend

Table 4-872. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU7	RO	0h	Reserved
19 - 0	COUNT0	RO	0h	This field contains the current value of counter 0. - (RO)

4.6.226 DCC0_DCCVALID0 Register (Offset = 1Ch) [reset = h]

Short Description: Value of the valid counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-873. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-415. DCC0_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
RO															
0															

Access Types Legend

Table 4-874. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU8	RO	0h	Reserved
15 - 0	VALID0	RO	0h	This field contains the current value of valid counter 0. - (RO)

4.6.227 DCC0_DCCCNT1 Register (Offset = 20h) [reset = h]

Short Description: Value of the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-875. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-416. DCC0_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9												COUNT1			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
RO															
0															

Access Types Legend

Table 4-876. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU9	RO	0h	Reserved
19 - 0	COUNT1	RO	0h	This field contains the current value of counter 1. - (RO)

4.6.228 DCC0_DCCCLKSSRC1 Register (Offset = 24h) [reset = h]

Short Description: Clock source1 selection control

Long Description:

Return to Summary Table

Table 4-877. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-417. DCC0_DCCCLKSSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY_B4				NU10								CLK_SRC1			
RW				RO								RW			
101				0								0			

Access Types Legend

Table 4-878. DCCCLKSSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU11	RO	0h	Reserved
15 - 12	KEY_B4	RW	65h	Key Programing (1010 is the KEY Value)
11 - 4	NU10	RO	0h	Reserved
3 - 0	CLK_SRC1	RW	0h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0x0 - REF_CLK0x1 - CPU_CLK0x2 - RC_CLK0x3 - RC_CLK0x4 - RC_CLK0x5 - RC_CLK0x6 - RC_CLK0x7 - RC_CLKDCC-B Clock source-0 selection Program value and its respective clock selected 0x0 - VCLK0x1 - DSS_CLK0x2 - BSS_CLK0x3 - QSPI_CLK0x4 - FDCAN_CLK0x5 - REF_CLK0x6 - CPU_CLK0x7 - RC_CLK

4.6.229 DCC0_DCCCLKSSRC0 Register (Offset = 28h) [reset = h]

Short Description: Clock source0 selection control

Long Description:

Return to Summary Table

Table 4-879. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-418. DCC0_DCCCLKSSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12												CLK_SRC0			
RO												RW			
0												101			

Access Types Legend

Table 4-880. DCCCLKSSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU12	RO	0h	Reserved
3 - 0	CLK_SRC0	RW	65h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0 - REF_CLKA - PLL_6005 - PLL_240DCC-B Clock source-0 selection Program value and its respective clock selected 0 - PLL_600A - VCLK5 - CPU_CLK

4.6.230 DCC1_DCCGCTRL Register (Offset = 0h) [reset = h]

Short Description: Starts / stops the counters clears the error signal

Long Description:

Return to Summary Table

Table 4-881. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-419. DCC1_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONENA				SINGLESHOT				ERRENA				DCCENA			
RW				RW				RW				RW			
101				101				101				101			

Access Types Legend

Table 4-882. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RO	0h	Reserved
15 - 12	DONENA	RW	65h	The DONEENA bit enables/disables the done signal. 0101 = disabled & 1010 = enabled
11 - 8	SINGLESHOT	RW	65h	Single/Continuous checking mode. 0101 = Continuous & 1010 = Single
7 - 4	ERRENA	RW	65h	The ERRENA bit enables/disables the error signal. 0101 = disabled & 1010 = enabled
3 - 0	DCCENA	RW	65h	The DCCENA bit starts and stops the operation of the dcc 0101 = disabled & 1010 = enabled

4.6.231 DCC1_DCCREV Register (Offset = 4h) [reset = h]

Short Description: Module version

Long Description:

Return to Summary Table

Table 4-883. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-420. DCC1_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2	SCHEME			NU1		FUNC									
RO	RO			RO		RO									
0	100			0		0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		RTL				MAJOR				CUSTOM	MINOR				
RO		RO				RO				RO	RO				
0		1				0				0	100				

Access Types Legend

Table 4-884. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU2	RO	0h	Reserved
30 - 28	SCHEME	RO	64h	SCHEME. - (RO)
27 - 26	NU1	RO	0h	Reserved
25 - 14	FUNC	RO	0h	Functional release number - (RO)
13 - 9	RTL	RO	1h	Design Release Number - (RO)
8 - 6	MAJOR	RO	0h	Major Revision Number - (RO)
5	CUSTOM	RO	0h	Indicates a special version of the module. May not be supported by standard software - (RO)
4 - 0	MINOR	RO	64h	Minor revision number. - (RO)

4.6.232 DCC1_DCCCNTSEED0 Register (Offset = 8h) [reset = h]

Short Description: Seed value for the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-885. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-421. DCC1_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3												COUNTSEED0			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
RW															
0															

Access Types Legend

Table 4-886. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU3	RO	0h	Reserved
19 - 0	COUNTSEED0	RW	0h	The seed value for Counter 0. The seed value that gets loaded into counter 0 (clock source 0)

4.6.233 DCC1_DCCVALIDSEED0 Register (Offset = Ch) [reset = h]

Short Description: Seed value for the timeout counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-887. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-422. DCC1_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
RW															
0															

Access Types Legend

Table 4-888. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU4	RO	0h	Reserved
15 - 0	VALIDSEED0	RW	0h	The seed value for Valid Duration Counter 0.The seed value that gets loaded into the valid duration counter for clock source 0

4.6.234 DCC1_DCCCNTSEED1 Register (Offset = 10h) [reset = h]

Short Description: Seed value for the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-889. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-423. DCC1_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5												COUNTSEED1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
RW															
0															

Access Types Legend

Table 4-890. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU5	RO	0h	Reserved
19 - 0	COUNTSEED1	RW	0h	The seed value for Counter 1. The seed value that gets loaded into counter 1 (clock source 1

4.6.235 DCC1_DCCSTAT Register (Offset = 14h) [reset = h]

Short Description: Contains the error & done flag bit

Long Description:

Return to Summary Table

Table 4-891. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-424. DCC1_DCCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6														DONE	ERR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-892. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU6	RO	0h	Reserved
1	DONE	RW	0h	Indicates whether or not an done has occured. Writing a 1 to this bit clears the flag.
0	ERR	RW	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag.

4.6.236 DCC1_DCCCNT0 Register (Offset = 18h) [reset = h]

Short Description: Value of the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-893. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-425. DCC1_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7												COUNT0			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
RO															
0															

Access Types Legend

Table 4-894. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU7	RO	0h	Reserved
19 - 0	COUNT0	RO	0h	This field contains the current value of counter 0. - (RO)

4.6.237 DCC1_DCCVALID0 Register (Offset = 1Ch) [reset = h]

Short Description: Value of the valid counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-895. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-426. DCC1_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
RO															
0															

Access Types Legend

Table 4-896. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU8	RO	0h	Reserved
15 - 0	VALID0	RO	0h	This field contains the current value of valid counter 0. - (RO)

4.6.238 DCC1_DCCCNT1 Register (Offset = 20h) [reset = h]

Short Description: Value of the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-897. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-427. DCC1_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9												COUNT1			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
RO															
0															

Access Types Legend

Table 4-898. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU9	RO	0h	Reserved
19 - 0	COUNT1	RO	0h	This field contains the current value of counter 1. - (RO)

4.6.239 DCC1_DCCCLKSSRC1 Register (Offset = 24h) [reset = h]

Short Description: Clock source1 selection control

Long Description:

Return to Summary Table

Table 4-899. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-428. DCC1_DCCCLKSSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY_B4				NU10								CLK_SRC1			
RW				RO								RW			
101				0								0			

Access Types Legend

Table 4-900. DCCCLKSSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU11	RO	0h	Reserved
15 - 12	KEY_B4	RW	65h	Key Programing (1010 is the KEY Value)
11 - 4	NU10	RO	0h	Reserved
3 - 0	CLK_SRC1	RW	0h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0x0 - REF_CLK0x1 - CPU_CLK0x2 - RC_CLK0x3 - RC_CLK0x4 - RC_CLK0x5 - RC_CLK0x6 - RC_CLK0x7 - RC_CLKDCC-B Clock source-0 selection Program value and its respective clock selected 0x0 - VCLK0x1 - DSS_CLK0x2 - BSS_CLK0x3 - QSPI_CLK0x4 - FDCAN_CLK0x5 - REF_CLK0x6 - CPU_CLK0x7 - RC_CLK

4.6.240 DCC1_DCCCLKSSRC0 Register (Offset = 28h) [reset = h]

Short Description: Clock source0 selection control

Long Description:

Return to Summary Table

Table 4-901. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-429. DCC1_DCCCLKSSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12												CLK_SRC0			
RO												RW			
0												101			

Access Types Legend

Table 4-902. DCCCLKSSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU12	RO	0h	Reserved
3 - 0	CLK_SRC0	RW	65h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0 - REF_CLKA - PLL_6005 - PLL_240DCC-B Clock source-0 selection Program value and its respective clock selected 0 - PLL_600A - VCLK5 - CPU_CLK

4.6.241 DCC2_DCCGCTRL Register (Offset = 0h) [reset = h]

Short Description: Starts / stops the counters clears the error signal

Long Description:

Return to Summary Table

Table 4-903. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-430. DCC2_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONENA				SINGLESHOT				ERRENA				DCCENA			
RW				RW				RW				RW			
101				101				101				101			

Access Types Legend

Table 4-904. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RO	0h	Reserved
15 - 12	DONENA	RW	65h	The DONEENA bit enables/disables the done signal. 0101 = disabled & 1010 = enabled
11 - 8	SINGLESHOT	RW	65h	Single/Continuous checking mode. 0101 = Continuous & 1010 = Single
7 - 4	ERRENA	RW	65h	The ERRENA bit enables/disables the error signal. 0101 = disabled & 1010 = enabled
3 - 0	DCCENA	RW	65h	The DCCENA bit starts and stops the operation of the dcc 0101 = disabled & 1010 = enabled

4.6.242 DCC2_DCCREV Register (Offset = 4h) [reset = h]

Short Description: Module version

Long Description:

Return to Summary Table

Table 4-905. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-431. DCC2_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2	SCHEME			NU1		FUNC									
RO	RO			RO		RO									
0	100			0		0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		RTL				MAJOR				CUSTOM	MINOR				
RO		RO				RO				RO	RO				
0		1				0				0	100				

Access Types Legend

Table 4-906. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU2	RO	0h	Reserved
30 - 28	SCHEME	RO	64h	SCHEME. - (RO)
27 - 26	NU1	RO	0h	Reserved
25 - 14	FUNC	RO	0h	Functional release number - (RO)
13 - 9	RTL	RO	1h	Design Release Number - (RO)
8 - 6	MAJOR	RO	0h	Major Revision Number - (RO)
5	CUSTOM	RO	0h	Indicates a special version of the module. May not be supported by standard software - (RO)
4 - 0	MINOR	RO	64h	Minor revision number. - (RO)

4.6.243 DCC2_DCCCNTSEED0 Register (Offset = 8h) [reset = h]

Short Description: Seed value for the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-907. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-432. DCC2_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3												COUNTSEED0			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
RW															
0															

Access Types Legend

Table 4-908. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU3	RO	0h	Reserved
19 - 0	COUNTSEED0	RW	0h	The seed value for Counter 0. The seed value that gets loaded into counter 0 (clock source 0)

4.6.244 DCC2_DCCVALIDSEED0 Register (Offset = Ch) [reset = h]

Short Description: Seed value for the timeout counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-909. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-433. DCC2_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
RW															
0															

Access Types Legend

Table 4-910. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU4	RO	0h	Reserved
15 - 0	VALIDSEED0	RW	0h	The seed value for Valid Duration Counter 0.The seed value that gets loaded into the valid duration counter for clock source 0

4.6.245 DCC2_DCCCNTSEED1 Register (Offset = 10h) [reset = h]

Short Description: Seed value for the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-911. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-434. DCC2_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5												COUNTSEED1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
RW															
0															

Access Types Legend

Table 4-912. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU5	RO	0h	Reserved
19 - 0	COUNTSEED1	RW	0h	The seed value for Counter 1. The seed value that gets loaded into counter 1 (clock source 1

4.6.246 DCC2_DCCSTAT Register (Offset = 14h) [reset = h]

Short Description: Contains the error & done flag bit

Long Description:

Return to Summary Table

Table 4-913. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-435. DCC2_DCCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6														DONE	ERR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-914. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU6	RO	0h	Reserved
1	DONE	RW	0h	Indicates whether or not an done has occured. Writing a 1 to this bit clears the flag.
0	ERR	RW	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag.

4.6.247 DCC2_DCCCNT0 Register (Offset = 18h) [reset = h]

Short Description: Value of the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-915. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-436. DCC2_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7												COUNT0			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
RO															
0															

Access Types Legend

Table 4-916. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU7	RO	0h	Reserved
19 - 0	COUNT0	RO	0h	This field contains the current value of counter 0. - (RO)

4.6.248 DCC2_DCCVALID0 Register (Offset = 1Ch) [reset = h]

Short Description: Value of the valid counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-917. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-437. DCC2_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
RO															
0															

Access Types Legend

Table 4-918. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU8	RO	0h	Reserved
15 - 0	VALID0	RO	0h	This field contains the current value of valid counter 0. - (RO)

4.6.249 DCC2_DCCCNT1 Register (Offset = 20h) [reset = h]

Short Description: Value of the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-919. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-438. DCC2_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9												COUNT1			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
RO															
0															

Access Types Legend

Table 4-920. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU9	RO	0h	Reserved
19 - 0	COUNT1	RO	0h	This field contains the current value of counter 1. - (RO)

4.6.250 DCC2_DCCCLKSSRC1 Register (Offset = 24h) [reset = h]

Short Description: Clock source1 selection control

Long Description:

Return to Summary Table

Table 4-921. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-439. DCC2_DCCCLKSSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY_B4				NU10								CLK_SRC1			
RW				RO								RW			
101				0								0			

Access Types Legend

Table 4-922. DCCCLKSSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU11	RO	0h	Reserved
15 - 12	KEY_B4	RW	65h	Key Programing (1010 is the KEY Value)
11 - 4	NU10	RO	0h	Reserved
3 - 0	CLK_SRC1	RW	0h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0x0 - REF_CLK0x1 - CPU_CLK0x2 - RC_CLK0x3 - RC_CLK0x4 - RC_CLK0x5 - RC_CLK0x6 - RC_CLK0x7 - RC_CLKDCC-B Clock source-0 selection Program value and its respective clock selected 0x0 - VCLK0x1 - DSS_CLK0x2 - BSS_CLK0x3 - QSPI_CLK0x4 - FDCAN_CLK0x5 - REF_CLK0x6 - CPU_CLK0x7 - RC_CLK

4.6.251 DCC2_DCCCLKSSRC0 Register (Offset = 28h) [reset = h]

Short Description: Clock source0 selection control

Long Description:

Return to Summary Table

Table 4-923. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-440. DCC2_DCCCLKSSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12												CLK_SRC0			
RO												RW			
0												101			

Access Types Legend

Table 4-924. DCCCLKSSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU12	RO	0h	Reserved
3 - 0	CLK_SRC0	RW	65h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0 - REF_CLKA - PLL_6005 - PLL_240DCC-B Clock source-0 selection Program value and its respective clock selected 0 - PLL_600A - VCLK5 - CPU_CLK

4.6.252 DCC3_DCCGCTRL Register (Offset = 0h) [reset = h]

Short Description: Starts / stops the counters clears the error signal

Long Description:

Return to Summary Table

Table 4-925. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-441. DCC3_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONENA				SINGLESHOT				ERRENA				DCCENA			
RW				RW				RW				RW			
101				101				101				101			

Access Types Legend

Table 4-926. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RO	0h	Reserved
15 - 12	DONENA	RW	65h	The DONEENA bit enables/disables the done signal. 0101 = disabled & 1010 = enabled
11 - 8	SINGLESHOT	RW	65h	Single/Continuous checking mode. 0101 = Continuous & 1010 = Single
7 - 4	ERRENA	RW	65h	The ERRENA bit enables/disables the error signal. 0101 = disabled & 1010 = enabled
3 - 0	DCCENA	RW	65h	The DCCENA bit starts and stops the operation of the dcc 0101 = disabled & 1010 = enabled

4.6.253 DCC3_DCCREV Register (Offset = 4h) [reset = h]

Short Description: Module version

Long Description:

Return to Summary Table

Table 4-927. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-442. DCC3_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2	SCHEME			NU1		FUNC									
RO	RO			RO		RO									
0	100			0		0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		RTL				MAJOR				CUSTOM	MINOR				
RO		RO				RO				RO	RO				
0		1				0				0	100				

Access Types Legend

Table 4-928. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU2	RO	0h	Reserved
30 - 28	SCHEME	RO	64h	SCHEME. - (RO)
27 - 26	NU1	RO	0h	Reserved
25 - 14	FUNC	RO	0h	Functional release number - (RO)
13 - 9	RTL	RO	1h	Design Release Number - (RO)
8 - 6	MAJOR	RO	0h	Major Revision Number - (RO)
5	CUSTOM	RO	0h	Indicates a special version of the module. May not be supported by standard software - (RO)
4 - 0	MINOR	RO	64h	Minor revision number. - (RO)

4.6.254 DCC3_DCCCNTSEED0 Register (Offset = 8h) [reset = h]

Short Description: Seed value for the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-929. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-443. DCC3_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3												COUNTSEED0			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
RW															
0															

Access Types Legend

Table 4-930. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU3	RO	0h	Reserved
19 - 0	COUNTSEED0	RW	0h	The seed value for Counter 0. The seed value that gets loaded into counter 0 (clock source 0)

4.6.255 DCC3_DCCVALIDSEED0 Register (Offset = Ch) [reset = h]

Short Description: Seed value for the timeout counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-931. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-444. DCC3_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
RW															
0															

Access Types Legend

Table 4-932. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU4	RO	0h	Reserved
15 - 0	VALIDSEED0	RW	0h	The seed value for Valid Duration Counter 0.The seed value that gets loaded into the valid duration counter for clock source 0

4.6.256 DCC3_DCCCNTSEED1 Register (Offset = 10h) [reset = h]

Short Description: Seed value for the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-933. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-445. DCC3_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5												COUNTSEED1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
RW															
0															

Access Types Legend

Table 4-934. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU5	RO	0h	Reserved
19 - 0	COUNTSEED1	RW	0h	The seed value for Counter 1. The seed value that gets loaded into counter 1 (clock source 1

4.6.257 DCC3_DCCSTAT Register (Offset = 14h) [reset = h]

Short Description: Contains the error & done flag bit

Long Description:

Return to Summary Table

Table 4-935. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-446. DCC3_DCCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6														DONE	ERR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-936. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU6	RO	0h	Reserved
1	DONE	RW	0h	Indicates whether or not an done has occured. Writing a 1 to this bit clears the flag.
0	ERR	RW	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag.

ADVANCE INFORMATION

4.6.258 DCC3_DCCCNT0 Register (Offset = 18h) [reset = h]

Short Description: Value of the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-937. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-447. DCC3_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7												COUNT0			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
RO															
0															

Access Types Legend

Table 4-938. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU7	RO	0h	Reserved
19 - 0	COUNT0	RO	0h	This field contains the current value of counter 0. - (RO)

4.6.259 DCC3_DCCVALID0 Register (Offset = 1Ch) [reset = h]

Short Description: Value of the valid counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-939. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-448. DCC3_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
RO															
0															

Access Types Legend

Table 4-940. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU8	RO	0h	Reserved
15 - 0	VALID0	RO	0h	This field contains the current value of valid counter 0. - (RO)

4.6.260 DCC3_DCCCNT1 Register (Offset = 20h) [reset = h]

Short Description: Value of the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-941. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-449. DCC3_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9												COUNT1			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
RO															
0															

Access Types Legend

Table 4-942. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU9	RO	0h	Reserved
19 - 0	COUNT1	RO	0h	This field contains the current value of counter 1. - (RO)

4.6.261 DCC3_DCCCLKSSRC1 Register (Offset = 24h) [reset = h]

Short Description: Clock source1 selection control

Long Description:

Return to Summary Table

Table 4-943. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-450. DCC3_DCCCLKSSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY_B4				NU10								CLK_SRC1			
RW				RO								RW			
101				0								0			

Access Types Legend

Table 4-944. DCCCLKSSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU11	RO	0h	Reserved
15 - 12	KEY_B4	RW	65h	Key Programing (1010 is the KEY Value)
11 - 4	NU10	RO	0h	Reserved
3 - 0	CLK_SRC1	RW	0h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0x0 - REF_CLK0x1 - CPU_CLK0x2 - RC_CLK0x3 - RC_CLK0x4 - RC_CLK0x5 - RC_CLK0x6 - RC_CLK0x7 - RC_CLKDCC-B Clock source-0 selection Program value and its respective clock selected 0x0 - VCLK0x1 - DSS_CLK0x2 - BSS_CLK0x3 - QSPI_CLK0x4 - FDCAN_CLK0x5 - REF_CLK0x6 - CPU_CLK0x7 - RC_CLK

4.6.262 DCC3_DCCCLKSSRC0 Register (Offset = 28h) [reset = h]

Short Description: Clock source0 selection control

Long Description:

Return to Summary Table

Table 4-945. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-451. DCC3_DCCCLKSSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12												CLK_SRC0			
RO												RW			
0												101			

Access Types Legend

Table 4-946. DCCCLKSSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU12	RO	0h	Reserved
3 - 0	CLK_SRC0	RW	65h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0 - REF_CLKA - PLL_6005 - PLL_240DCC-B Clock source-0 selection Program value and its respective clock selected 0 - PLL_600A - VCLK5 - CPU_CLK

Table 4-947. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

4.7 MSS_DCC Registers

Table 4-948. HSM_DCC0, HSM_DCC0_HSM_DCC Registers, Base Address=47F7 9000H, Length=4

Offset	Length	Acronym	Register Name	HSM_DCC0 Physical Address
0h	32	HSM_DCC0_DCCGCTRL	Starts / stops the counters clears the error signal	47F7 9000h
4h	32	HSM_DCC0_DCCREV	Module version	47F7 9004h
8h	32	HSM_DCC0_DCCCNTSEED0	Seed value for the counter attached to clock source 0	47F7 9008h
Ch	32	HSM_DCC0_DCCVALIDSEED0	Seed value for the timeout counter attached to clock source 0	47F7 900Ch
10h	32	HSM_DCC0_DCCCNTSEED1	Seed value for the counter attached to clock source 1	47F7 9010h
14h	32	HSM_DCC0_DCCSTAT	Contains the error & done flag bit	47F7 9014h
18h	32	HSM_DCC0_DCCCNT0	Value of the counter attached to clock source 0	47F7 9018h
1Ch	32	HSM_DCC0_DCCVALID0	Value of the valid counter attached to clock source 0	47F7 901Ch
20h	32	HSM_DCC0_DCCCNT1	Value of the counter attached to clock source 1	47F7 9020h
24h	32	HSM_DCC0_DCCCLKSSRC1	Clock source1 selection control	47F7 9024h
28h	32	HSM_DCC0_DCCCLKSSRC0	Clock source0 selection control	47F7 9028h

4.7.1 HSM_DCC0_DCCGCTRL Register (Offset = 0h) [reset = h]

Short Description: Starts / stops the counters clears the error signal

Long Description:

Return to Summary Table

Table 4-949. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9000h

Figure 4-452. HSM_DCC0_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONENA				SINGLESHOT				ERRENA				DCCENA			
RW				RW				RW				RW			
101				101				101				101			

Access Types Legend

Table 4-950. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RO	0h	Reserved
15 - 12	DONENA	RW	65h	The DONEENA bit enables/disables the done signal. 0101 = disabled & 1010 = enabled
11 - 8	SINGLESHOT	RW	65h	Single/Continuous checking mode. 0101 = Continuous & 1010 = Single
7 - 4	ERRENA	RW	65h	The ERRENA bit enables/disables the error signal. 0101 = disabled & 1010 = enabled
3 - 0	DCCENA	RW	65h	The DCCENA bit starts and stops the operation of the dcc 0101 = disabled & 1010 = enabled

4.7.2 HSM_DCC0_DCCREV Register (Offset = 4h) [reset = h]

Short Description: Module version

Long Description:

Return to Summary Table

Table 4-951. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9004h

Figure 4-453. HSM_DCC0_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2	SCHEME			NU1		FUNC									
RO	RO			RO		RO									
0	100			0		0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		RTL				MAJOR				CUSTOM	MINOR				
RO		RO				RO				RO	RO				
0		1				0				0	100				

Access Types Legend

Table 4-952. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU2	RO	0h	Reserved
30 - 28	SCHEME	RO	64h	SCHEME. - (RO)
27 - 26	NU1	RO	0h	Reserved
25 - 14	FUNC	RO	0h	Functional release number - (RO)
13 - 9	RTL	RO	1h	Design Release Number - (RO)
8 - 6	MAJOR	RO	0h	Major Revision Number - (RO)
5	CUSTOM	RO	0h	Indicates a special version of the module. May not be supported by standard software - (RO)
4 - 0	MINOR	RO	64h	Minor revision number. - (RO)

4.7.3 HSM_DCC0_DCCCNTSEED0 Register (Offset = 8h) [reset = h]

Short Description: Seed value for the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-953. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9008h

Figure 4-454. HSM_DCC0_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3												COUNTSEED0			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
RW															
0															

Access Types Legend

Table 4-954. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU3	RO	0h	Reserved
19 - 0	COUNTSEED0	RW	0h	The seed value for Counter 0. The seed value that gets loaded into counter 0 (clock source 0)

4.7.4 HSM_DCC0_DCCVALIDSEED0 Register (Offset = Ch) [reset = h]

Short Description: Seed value for the timeout counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-955. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 900Ch

Figure 4-455. HSM_DCC0_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
RW															
0															

Access Types Legend

Table 4-956. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU4	RO	0h	Reserved
15 - 0	VALIDSEED0	RW	0h	The seed value for Valid Duration Counter 0.The seed value that gets loaded into the valid duration counter for clock source 0

4.7.5 HSM_DCC0_DCCCNTSEED1 Register (Offset = 10h) [reset = h]

Short Description: Seed value for the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-957. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9010h

Figure 4-456. HSM_DCC0_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5												COUNTSEED1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
RW															
0															

Access Types Legend

Table 4-958. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU5	RO	0h	Reserved
19 - 0	COUNTSEED1	RW	0h	The seed value for Counter 1. The seed value that gets loaded into counter 1 (clock source 1

4.7.6 HSM_DCC0_DCCSTAT Register (Offset = 14h) [reset = h]

Short Description: Contains the error & done flag bit

Long Description:

Return to Summary Table

Table 4-959. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9014h

Figure 4-457. HSM_DCC0_DCCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6														DONE	ERR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-960. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU6	RO	0h	Reserved
1	DONE	RW	0h	Indicates whether or not an done has occured. Writing a 1 to this bit clears the flag.
0	ERR	RW	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag.

4.7.7 HSM_DCC0_DCCCNT0 Register (Offset = 18h) [reset = h]

Short Description: Value of the counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-961. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9018h

Figure 4-458. HSM_DCC0_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7												COUNT0			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
RO															
0															

Access Types Legend

Table 4-962. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU7	RO	0h	Reserved
19 - 0	COUNT0	RO	0h	This field contains the current value of counter 0. - (RO)

4.7.8 HSM_DCC0_DCCVALID0 Register (Offset = 1Ch) [reset = h]

Short Description: Value of the valid counter attached to clock source 0

Long Description:

Return to Summary Table

Table 4-963. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 901Ch

Figure 4-459. HSM_DCC0_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
RO															
0															

Access Types Legend

Table 4-964. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU8	RO	0h	Reserved
15 - 0	VALID0	RO	0h	This field contains the current value of valid counter 0. - (RO)

4.7.9 HSM_DCC0_DCCCNT1 Register (Offset = 20h) [reset = h]

Short Description: Value of the counter attached to clock source 1

Long Description:

Return to Summary Table

Table 4-965. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9020h

Figure 4-460. HSM_DCC0_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9												COUNT1			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
RO															
0															

Access Types Legend

Table 4-966. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU9	RO	0h	Reserved
19 - 0	COUNT1	RO	0h	This field contains the current value of counter 1. - (RO)

4.7.10 HSM_DCC0_DCCCLKSSRC1 Register (Offset = 24h) [reset = h]

Short Description: Clock source1 selection control

Long Description:

Return to Summary Table

Table 4-967. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9024h

Figure 4-461. HSM_DCC0_DCCCLKSSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY_B4				NU10								CLK_SRC1			
RW				RO								RW			
101				0								0			

Access Types Legend

Table 4-968. DCCCLKSSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU11	RO	0h	Reserved
15 - 12	KEY_B4	RW	65h	Key Programing (1010 is the KEY Value)
11 - 4	NU10	RO	0h	Reserved
3 - 0	CLK_SRC1	RW	0h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0x0 - REF_CLK0x1 - CPU_CLK0x2 - RC_CLK0x3 - RC_CLK0x4 - RC_CLK0x5 - RC_CLK0x6 - RC_CLK0x7 - RC_CLKDCC-B Clock source-0 selection Program value and its respective clock selected 0x0 - VCLK0x1 - DSS_CLK0x2 - BSS_CLK0x3 - QSPI_CLK0x4 - FDCAN_CLK0x5 - REF_CLK0x6 - CPU_CLK0x7 - RC_CLK

4.7.11 HSM_DCC0_DCCCLKSSRC0 Register (Offset = 28h) [reset = h]

Short Description: Clock source0 selection control

Long Description:

Return to Summary Table

Table 4-969. Instance Table

Instance Name	Physical Address
HSM_DCC0	47F7 9028h

Figure 4-462. HSM_DCC0_DCCCLKSSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12												CLK_SRC0			
RO												RW			
0												101			

Access Types Legend

Table 4-970. DCCCLKSSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU12	RO	0h	Reserved
3 - 0	CLK_SRC0	RW	65h	Clock source selection for Source 0DCC-A Clock source-0 selection Program value and its respective clock selected 0 - REF_CLKA - PLL_6005 - PLL_240DCC-B Clock source-0 selection Program value and its respective clock selected 0 - PLL_600A - VCLK5 - CPU_CLK

Table 4-971. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.8 MSS_ECC_AGG_MSS Registers

Table 4-972. ECC_AGG_TOP, ECC_AGG_TOP_ECC_AGG_TOP Registers, Base Address=5301 0000H, Length=5

Offset	Length	Acronym	Register Name	ECC_AGG_TOP Physical Address
0h	32	ECC_AGG_TOP_REV	Revision parameters	5301 0000h
8h	24	ECC_AGG_TOP_VECTOR	ECC Vector Register	5301 0008h
Ch	16	ECC_AGG_TOP_STAT	Misc Status	5301 000Ch
14h	8	ECC_AGG_TOP_CTRL	ECC Control Register	5301 0014h
18h	32	ECC_AGG_TOP_ERR_CTRL1	ECC Error Control1 Register	5301 0018h
1Ch	32	ECC_AGG_TOP_ERR_CTRL2	ECC Error Control2 Register	5301 001Ch
20h	32	ECC_AGG_TOP_ERR_STAT1	ECC Error Status1 Register	5301 0020h
24h	32	ECC_AGG_TOP_ERR_STAT2	ECC Error Status2 Register	5301 0024h
28h	16	ECC_AGG_TOP_ERR_STAT3	ECC Error Status3 Register	5301 0028h
3Ch	0	ECC_AGG_TOP_SEC_EOI_REG	EOI Register	5301 003Ch
40h	8	ECC_AGG_TOP_SEC_STATUS_REG0	Interrupt Status Register 0	5301 0040h
80h	8	ECC_AGG_TOP_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5301 0080h
C0h	8	ECC_AGG_TOP_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5301 00C0h
13Ch	0	ECC_AGG_TOP_DED_EOI_REG	EOI Register	5301 013Ch
140h	8	ECC_AGG_TOP_DED_STATUS_REG0	Interrupt Status Register 0	5301 0140h
180h	8	ECC_AGG_TOP_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5301 0180h
1C0h	8	ECC_AGG_TOP_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5301 01C0h
200h	8	ECC_AGG_TOP_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5301 0200h
204h	8	ECC_AGG_TOP_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5301 0204h
208h	8	ECC_AGG_TOP_AGGR_STATUS_SET	AGGR interrupt status set Register	5301 0208h
20Ch	8	ECC_AGG_TOP_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5301 020Ch

4.8.1 ECC_AGG_TOP_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-973. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0000h

Figure 4-463. ECC_AGG_TOP_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11101					10			0		0					

Access Types Legend

Table 4-974. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.8.2 ECC_AGG_TOP_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-975. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0008h

Figure 4-464. ECC_AGG_TOP_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD_SVBUS_DONE	RD_SVBUS_ADDRESS														
RW	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
RW	NONE				RW										
0	0				0										

Access Types Legend

Table 4-976. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.8.3 ECC_AGG_TOP_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

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Table 4-977. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 000Ch

Figure 4-465. ECC_AGG_TOP_STAT Name Register

15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					RO		
0					1001		
7	6	5	4	3	2	1	0
NUM_RAMS							
RO							
1001							

Access Types Legend

Table 4-978. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	3E9h	Indicates the number of RAMS serviced by the ECC aggregator

4.8.4 ECC_AGG_TOP_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

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Table 4-979. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0014h

Figure 4-466. ECC_AGG_TOP_CTRL Name Register

15	14	13	12	11	10	9	8
CHECK_SVBUS_TIMEOUT							
RW							
1							
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
RW	RW	RW	RW	RW	RW	RW	RW
1	0	0	0	0	1	1	1

Access Types Legend

Table 4-980. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.8.5 ECC_AGG_TOP_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

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Table 4-981. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0018h

Figure 4-467. ECC_AGG_TOP_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-982. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.8.6 ECC_AGG_TOP_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

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Table 4-983. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 001Ch

Figure 4-468. ECC_AGG_TOP_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-984. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.8.7 ECC_AGG_TOP_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

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Table 4-985. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0020h

Figure 4-469. ECC_AGG_TOP_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
RW	RW DECR		RW	RW DECR		RW DECR		RW	RW		RW	RW INCR		RW INCR	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-986. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.8.8 ECC_AGG_TOP_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

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Table 4-987. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0024h

Figure 4-470. ECC_AGG_TOP_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-988. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.8.9 ECC_AGG_TOP_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

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Table 4-989. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0028h

Figure 4-471. ECC_AGG_TOP_ERR_STAT3 Name Register

15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						RW	NONE
0						0	0
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						RW	RO
0						0	0

Access Types Legend

Table 4-990. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.8.10 ECC_AGG_TOP_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-991. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 003Ch

Figure 4-472. ECC_AGG_TOP_SEC_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-992. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.8.11 ECC_AGG_TOP_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-993. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0040h

Figure 4-473. ECC_AGG_TOP_SEC_STATUS_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_PEND	TPTC_A0_PEND	MSS_MBOX_PEND	MSS_L2SLV3_PEND	MSS_L2SLV2_PEND	MSS_L2SLV1_PEND	MSS_L2SLV0_PEND
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-994. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

4.8.12 ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-995. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0080h

Figure 4-474. ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_ENABLE_SET	TPTC_A0_ENABLE_SET	MSS_MBOX_ENABLE_SET	MSS_L2SLV3_ENABLE_SET	MSS_L2SLV2_ENABLE_SET	MSS_L2SLV1_ENABLE_SET	MSS_L2SLV0_ENABLE_SET
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-996. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

4.8.13 ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-997. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 00C0h

Figure 4-475. ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_ENABLE_CLR	TPTC_A0_ENABLE_CLR	MSS_MBOX_ENABLE_CLR	MSS_L2SLV3_ENABLE_CLR	MSS_L2SLV2_ENABLE_CLR	MSS_L2SLV1_ENABLE_CLR	MSS_L2SLV0_ENABLE_CLR
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-998. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

4.8.14 ECC_AGG_TOP_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-999. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 013Ch

Figure 4-476. ECC_AGG_TOP_DED_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1000. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.8.15 ECC_AGG_TOP_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1001. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0140h

Figure 4-477. ECC_AGG_TOP_DED_STATUS_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_PEND	TPTC_A0_PEND	MSS_MBOX_PEND	MSS_L2SLV3_PEND	MSS_L2SLV2_PEND	MSS_L2SLV1_PEND	MSS_L2SLV0_PEND
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1002. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

4.8.16 ECC_AGG_TOP_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1003. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0180h

Figure 4-478. ECC_AGG_TOP_DED_ENABLE_SET_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_ENABLE_SET	TPTC_A0_ENABLE_SET	MSS_MBOX_ENABLE_SET	MSS_L2SLV3_ENABLE_SET	MSS_L2SLV2_ENABLE_SET	MSS_L2SLV1_ENABLE_SET	MSS_L2SLV0_ENABLE_SET
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1004. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

4.8.17 ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1005. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 01C0h

Figure 4-479. ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED	TPTC_A1_ENABLE_CLR	TPTC_A0_ENABLE_CLR	MSS_MBOX_ENABLE_CLR	MSS_L2SLV3_ENABLE_CLR	MSS_L2SLV2_ENABLE_CLR	MSS_L2SLV1_ENABLE_CLR	MSS_L2SLV0_ENABLE_CLR
NONE	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1006. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

4.8.18 ECC_AGG_TOP_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-1007. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0200h

Figure 4-480. ECC_AGG_TOP_AGGR_ENABLE_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1008. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.8.19 ECC_AGG_TOP_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1009. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0204h

Figure 4-481. ECC_AGG_TOP_AGGR_ENABLE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1010. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.8.20 ECC_AGG_TOP_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-1011. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0208h

Figure 4-482. ECC_AGG_TOP_AGGR_STATUS_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW INCR		RW INCR	
0				0		0	

Access Types Legend

Table 4-1012. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.8.21 ECC_AGG_TOP_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1013. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 020Ch

Figure 4-483. ECC_AGG_TOP_AGGR_STATUS_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW DECR		RW DECR	
0				0		0	

Access Types Legend

Table 4-1014. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

Table 4-1015. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
RW DECR	RW DECR	Undefined
RW INCR	RW INCR	Undefined

4.9 MSS_ECC_AGGA Registers

Table 4-1016. ECC_AGG_R5SS0_CORE0, ECC_AGG_R5SS0_CORE0_ECC_AGG_R5SS0_CORE Registers, Base Address=5300 0000H, Length=5

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS0_CORE0 Physical Address
0h	32	ECC_AGG_R5SS0_CORE0_REV	Revision parameters	5300 0000h
8h	24	ECC_AGG_R5SS0_CORE0_VECTOR	ECC Vector Register	5300 0008h
Ch	16	ECC_AGG_R5SS0_CORE0_STAT	Misc Status	5300 000Ch
10h	32	ECC_AGG_R5SS0_CORE0_WRAP_REV	Revision parameters	5300 0010h
14h	8	ECC_AGG_R5SS0_CORE0_CTRL	ECC Control Register	5300 0014h
18h	32	ECC_AGG_R5SS0_CORE0_ERR_CTRL1	ECC Error Control1 Register	5300 0018h
1Ch	32	ECC_AGG_R5SS0_CORE0_ERR_CTRL2	ECC Error Control2 Register	5300 001Ch
20h	32	ECC_AGG_R5SS0_CORE0_ERR_STAT1	ECC Error Status1 Register	5300 0020h
24h	32	ECC_AGG_R5SS0_CORE0_ERR_STAT2	ECC Error Status2 Register	5300 0024h
28h	16	ECC_AGG_R5SS0_CORE0_ERR_STAT3	ECC Error Status3 Register	5300 0028h
3Ch	0	ECC_AGG_R5SS0_CORE0_SEC_EOI_REG	EOI Register	5300 003Ch
40h	32	ECC_AGG_R5SS0_CORE0_SEC_STATUS_REG0	Interrupt Status Register 0	5300 0040h
80h	32	ECC_AGG_R5SS0_CORE0_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 0080h
C0h	32	ECC_AGG_R5SS0_CORE0_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 00C0h
13Ch	0	ECC_AGG_R5SS0_CORE0_DED_EOI_REG	EOI Register	5300 013Ch
140h	32	ECC_AGG_R5SS0_CORE0_DED_STATUS_REG0	Interrupt Status Register 0	5300 0140h
180h	32	ECC_AGG_R5SS0_CORE0_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 0180h
1C0h	32	ECC_AGG_R5SS0_CORE0_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 01C0h
200h	8	ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5300 0200h
204h	8	ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5300 0204h
208h	8	ECC_AGG_R5SS0_CORE0_AGGR_STATUS_SET	AGGR interrupt status set Register	5300 0208h
20Ch	8	ECC_AGG_R5SS0_CORE0_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5300 020Ch

4.9.1 ECC_AGG_R5SS0_CORE0_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1017. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0000h

Figure 4-484. ECC_AGG_R5SS0_CORE0_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11000					10			0		0					

Access Types Legend

Table 4-1018. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2AF8h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.9.2 ECC_AGG_R5SS0_CORE0_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-1019. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0008h

Figure 4-485. ECC_AGG_R5SS0_CORE0_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD_SVBUS_DONE	RD_SVBUS_ADDRESS														
RO	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
RW	NONE				RW										
0	0				0										

Access Types Legend

Table 4-1020. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.9.3 ECC_AGG_R5SS0_CORE0_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

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Table 4-1021. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 000Ch

Figure 4-486. ECC_AGG_R5SS0_CORE0_STAT Name Register

15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					RO		
0					11100		
7	6	5	4	3	2	1	0
NUM_RAMS							
RO							
11100							

Access Types Legend

Table 4-1022. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	2B5Ch	Indicates the number of RAMS serviced by the ECC aggregator

4.9.4 ECC_AGG_R5SS0_CORE0_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1023. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0010h

Figure 4-487. ECC_AGG_R5SS0_CORE0_WRAP_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
RO				RO				RO		RO					
0				10				0		10					

Access Types Legend

Table 4-1024. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB84h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

4.9.5 ECC_AGG_R5SS0_CORE0_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

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Table 4-1025. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0014h

Figure 4-488. ECC_AGG_R5SS0_CORE0_CTRL Name Register

15	14	13	12	11	10	9	8
CHECK_SVBUS_TIMEOUT							
RW							
1							
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
RW	RW	RW	RW	RW	RW	RW	RW
1	0	0	0	0	1	1	1

Access Types Legend

Table 4-1026. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.9.6 ECC_AGG_R5SS0_CORE0_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

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Table 4-1027. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0018h

Figure 4-489. ECC_AGG_R5SS0_CORE0_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-1028. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.9.7 ECC_AGG_R5SS0_CORE0_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1029. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 001Ch

Figure 4-490. ECC_AGG_R5SS0_CORE0_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-1030. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.9.8 ECC_AGG_R5SS0_CORE0_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

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Table 4-1031. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0020h

Figure 4-491. ECC_AGG_R5SS0_CORE0_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
RW	RW DECR		RW	RW DECR		RW DECR		RW	RW		RW	RW INCR		RW INCR	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-1032. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.9.9 ECC_AGG_R5SS0_CORE0_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

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Table 4-1033. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0024h

Figure 4-492. ECC_AGG_R5SS0_CORE0_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-1034. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.9.10 ECC_AGG_R5SS0_CORE0_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1035. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0028h

Figure 4-493. ECC_AGG_R5SS0_CORE0_ERR_STAT3 Name Register

15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						RW	NONE
0						0	0
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						RW	RO
0						0	0

Access Types Legend

Table 4-1036. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.9.11 ECC_AGG_R5SS0_CORE0_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1037. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 003Ch

Figure 4-494. ECC_AGG_R5SS0_CORE0_SEC_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1038. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.9.12 ECC_AGG_R5SS0_CORE0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1039. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0040h

Figure 4-495. ECC_AGG_R5SS0_CORE0_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1040. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend

Table 4-1040. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

4.9.13 ECC_AGG_R5SS0_CORE0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1041. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0080h

Figure 4-496. ECC_AGG_R5SS0_CORE0_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1042. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend

Table 4-1042. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

4.9.14 ECC_AGG_R5SS0_CORE0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1043. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 00C0h

Figure 4-497. ECC_AGG_R5SS0_CORE0_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1044. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend

Table 4-1044. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

4.9.15 ECC_AGG_R5SS0_CORE0_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-1045. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 013Ch

Figure 4-498. ECC_AGG_R5SS0_CORE0_DED_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1046. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.9.16 ECC_AGG_R5SS0_CORE0_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1047. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0140h

Figure 4-499. ECC_AGG_R5SS0_CORE0_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1048. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend

Table 4-1048. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

4.9.17 ECC_AGG_R5SS0_CORE0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1049. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0180h

Figure 4-500. ECC_AGG_R5SS0_CORE0_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1050. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend

Table 4-1050. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

4.9.18 ECC_AGG_R5SS0_CORE0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1051. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 01C0h

Figure 4-501. ECC_AGG_R5SS0_CORE0_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1052. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend

Table 4-1052. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

4.9.19 ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-1053. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0200h

Figure 4-502. ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1054. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.9.20 ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

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Table 4-1055. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0204h

Figure 4-503. ECC_AGG_R5SS0_CORE0_AGGR_ENABLE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1056. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.9.21 ECC_AGG_R5SS0_CORE0_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-1057. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0208h

Figure 4-504. ECC_AGG_R5SS0_CORE0_AGGR_STATUS_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW INCR		RW INCR	
0				0		0	

Access Types Legend

Table 4-1058. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.9.22 ECC_AGG_R5SS0_CORE0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-1059. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 020Ch

Figure 4-505. ECC_AGG_R5SS0_CORE0_AGGR_STATUS_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW DECR		RW DECR	
0				0		0	

Access Types Legend

Table 4-1060. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

Table 4-1061. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
RW DECR	RW DECR	Undefined
RW INCR	RW INCR	Undefined

4.10 MSS_ECC_AGGB Registers

Table 4-1062. ECC_AGG_R5SS0_CORE1, ECC_AGG_R5SS0_CORE1_ECC_AGG_R5SS0_CORE Registers, Base Address=5300 3000H, Length=5

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS0_CORE1 Physical Address
0h	32	ECC_AGG_R5SS0_CORE1_REV	Revision parameters	5300 3000h
8h	24	ECC_AGG_R5SS0_CORE1_VECTOR	ECC Vector Register	5300 3008h
Ch	16	ECC_AGG_R5SS0_CORE1_STAT	Misc Status	5300 300Ch
10h	32	ECC_AGG_R5SS0_CORE1_WRAP_REV	Revision parameters	5300 3010h
14h	8	ECC_AGG_R5SS0_CORE1_CTRL	ECC Control Register	5300 3014h
18h	32	ECC_AGG_R5SS0_CORE1_ERR_CTRL1	ECC Error Control1 Register	5300 3018h
1Ch	32	ECC_AGG_R5SS0_CORE1_ERR_CTRL2	ECC Error Control2 Register	5300 301Ch
20h	32	ECC_AGG_R5SS0_CORE1_ERR_STAT1	ECC Error Status1 Register	5300 3020h
24h	32	ECC_AGG_R5SS0_CORE1_ERR_STAT2	ECC Error Status2 Register	5300 3024h
28h	16	ECC_AGG_R5SS0_CORE1_ERR_STAT3	ECC Error Status3 Register	5300 3028h
3Ch	0	ECC_AGG_R5SS0_CORE1_SEC_EOI_REG	EOI Register	5300 303Ch
40h	32	ECC_AGG_R5SS0_CORE1_SEC_STATUS_REG0	Interrupt Status Register 0	5300 3040h
80h	32	ECC_AGG_R5SS0_CORE1_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 3080h
C0h	32	ECC_AGG_R5SS0_CORE1_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 30C0h
13Ch	0	ECC_AGG_R5SS0_CORE1_DED_EOI_REG	EOI Register	5300 313Ch
140h	32	ECC_AGG_R5SS0_CORE1_DED_STATUS_REG0	Interrupt Status Register 0	5300 3140h
180h	32	ECC_AGG_R5SS0_CORE1_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 3180h
1C0h	32	ECC_AGG_R5SS0_CORE1_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 31C0h
200h	8	ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5300 3200h
204h	8	ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5300 3204h
208h	8	ECC_AGG_R5SS0_CORE1_AGGR_STATUS_SET	AGGR interrupt status set Register	5300 3208h
20Ch	8	ECC_AGG_R5SS0_CORE1_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5300 320Ch

Table 4-1063. ECC_AGG_R5SS1_CORE0, ECC_AGG_R5SS1_CORE0_ECC_AGG_R5SS1_CORE Registers, Base Address=5300 4000H, Length=5

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS1_CORE0 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
0h	32	ECC_AGG_R5SS1_CORE0_REV	Revision parameters	5300 4000h	5300 7000h

Table 4-1063. ECC_AGG_R5SS1_CORE0, ECC_AGG_R5SS1_CORE0_ECC_AGG_R5SS1_CORE Registers, Base Address=5300 4000H, Length=5 (continued)

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS1_CORE0 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
8h	24	ECC_AGG_R5SS1_CORE0_VECTOR	ECC Vector Register	5300 4008h	5300 7008h
Ch	16	ECC_AGG_R5SS1_CORE0_STAT	Misc Status	5300 400Ch	5300 700Ch
10h	32	ECC_AGG_R5SS1_CORE0_WRAP_REV	Revision parameters	5300 4010h	5300 7010h
14h	8	ECC_AGG_R5SS1_CORE0_CTRL	ECC Control Register	5300 4014h	5300 7014h
18h	32	ECC_AGG_R5SS1_CORE0_ERR_CTRL1	ECC Error Control1 Register	5300 4018h	5300 7018h
1Ch	32	ECC_AGG_R5SS1_CORE0_ERR_CTRL2	ECC Error Control2 Register	5300 401Ch	5300 701Ch
20h	32	ECC_AGG_R5SS1_CORE0_ERR_STAT1	ECC Error Status1 Register	5300 4020h	5300 7020h
24h	32	ECC_AGG_R5SS1_CORE0_ERR_STAT2	ECC Error Status2 Register	5300 4024h	5300 7024h
28h	16	ECC_AGG_R5SS1_CORE0_ERR_STAT3	ECC Error Status3 Register	5300 4028h	5300 7028h
3Ch	0	ECC_AGG_R5SS1_CORE0_SEC_EOI_REG	EOI Register	5300 403Ch	5300 703Ch
40h	32	ECC_AGG_R5SS1_CORE0_SEC_STATUS_REG0	Interrupt Status Register 0	5300 4040h	5300 7040h
80h	32	ECC_AGG_R5SS1_CORE0_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 4080h	5300 7080h
C0h	32	ECC_AGG_R5SS1_CORE0_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 40C0h	5300 70C0h
13Ch	0	ECC_AGG_R5SS1_CORE0_DED_EOI_REG	EOI Register	5300 413Ch	5300 713Ch
140h	32	ECC_AGG_R5SS1_CORE0_DED_STATUS_REG0	Interrupt Status Register 0	5300 4140h	5300 7140h
180h	32	ECC_AGG_R5SS1_CORE0_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 4180h	5300 7180h
1C0h	32	ECC_AGG_R5SS1_CORE0_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 41C0h	5300 71C0h
200h	8	ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5300 4200h	5300 7200h
204h	8	ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5300 4204h	5300 7204h
208h	8	ECC_AGG_R5SS1_CORE0_AGGR_STATUS_SET	AGGR interrupt status set Register	5300 4208h	5300 7208h
20Ch	8	ECC_AGG_R5SS1_CORE0_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5300 420Ch	5300 720Ch

Table 4-1064. ECC_AGG_R5SS1_CORE1, ECC_AGG_R5SS1_CORE1_ECC_AGG_R5SS1_CORE Registers, Base Address=5300 7000H, Length=5

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS1_CORE0 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
0h	32	ECC_AGG_R5SS1_CORE1_REV	Revision parameters	5300 4000h	5300 7000h
8h	24	ECC_AGG_R5SS1_CORE1_VECTOR	ECC Vector Register	5300 4008h	5300 7008h
Ch	16	ECC_AGG_R5SS1_CORE1_STAT	Misc Status	5300 400Ch	5300 700Ch
10h	32	ECC_AGG_R5SS1_CORE1_WRAP_REV	Revision parameters	5300 4010h	5300 7010h
14h	8	ECC_AGG_R5SS1_CORE1_CTRL	ECC Control Register	5300 4014h	5300 7014h

Table 4-1064. ECC_AGG_R5SS1_CORE1, ECC_AGG_R5SS1_CORE1_ECC_AGG_R5SS1_CORE Registers, Base Address=5300 7000H, Length=5 (continued)

Offset	Length	Acronym	Register Name	ECC_AGG_R5SS1_CORE0 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
18h	32	ECC_AGG_R5SS1_CORE1_ERR_CTRL1	ECC Error Control1 Register	5300 4018h	5300 7018h
1Ch	32	ECC_AGG_R5SS1_CORE1_ERR_CTRL2	ECC Error Control2 Register	5300 401Ch	5300 701Ch
20h	32	ECC_AGG_R5SS1_CORE1_ERR_STAT1	ECC Error Status1 Register	5300 4020h	5300 7020h
24h	32	ECC_AGG_R5SS1_CORE1_ERR_STAT2	ECC Error Status2 Register	5300 4024h	5300 7024h
28h	16	ECC_AGG_R5SS1_CORE1_ERR_STAT3	ECC Error Status3 Register	5300 4028h	5300 7028h
3Ch	0	ECC_AGG_R5SS1_CORE1_SEC_EOI_REG	EOI Register	5300 403Ch	5300 703Ch
40h	32	ECC_AGG_R5SS1_CORE1_SEC_STATUS_REG0	Interrupt Status Register 0	5300 4040h	5300 7040h
80h	32	ECC_AGG_R5SS1_CORE1_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 4080h	5300 7080h
C0h	32	ECC_AGG_R5SS1_CORE1_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 40C0h	5300 70C0h
13Ch	0	ECC_AGG_R5SS1_CORE1_DED_EOI_REG	EOI Register	5300 413Ch	5300 713Ch
140h	32	ECC_AGG_R5SS1_CORE1_DED_STATUS_REG0	Interrupt Status Register 0	5300 4140h	5300 7140h
180h	32	ECC_AGG_R5SS1_CORE1_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5300 4180h	5300 7180h
1C0h	32	ECC_AGG_R5SS1_CORE1_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5300 41C0h	5300 71C0h
200h	8	ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5300 4200h	5300 7200h
204h	8	ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5300 4204h	5300 7204h
208h	8	ECC_AGG_R5SS1_CORE1_AGGR_STATUS_SET	AGGR interrupt status set Register	5300 4208h	5300 7208h
20Ch	8	ECC_AGG_R5SS1_CORE1_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5300 420Ch	5300 720Ch

4.10.1 ECC_AGG_R5SS0_CORE1_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1065. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3000h

Figure 4-506. ECC_AGG_R5SS0_CORE1_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11000					10			0		0					

Access Types Legend

Table 4-1066. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2AF8h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.10.2 ECC_AGG_R5SS0_CORE1_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-1067. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3008h

Figure 4-507. ECC_AGG_R5SS0_CORE1_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD_SVBUS_DONE	RD_SVBUS_ADDRESS														
RO	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
RW	NONE				RW										
0	0				0										

Access Types Legend

Table 4-1068. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.10.3 ECC_AGG_R5SS0_CORE1_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

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Table 4-1069. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 300Ch

Figure 4-508. ECC_AGG_R5SS0_CORE1_STAT Name Register

15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					RO		
0					11100		
7	6	5	4	3	2	1	0
NUM_RAMS							
RO							
11100							

Access Types Legend

Table 4-1070. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	2B5Ch	Indicates the number of RAMS serviced by the ECC aggregator

4.10.4 ECC_AGG_R5SS0_CORE1_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1071. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3010h

Figure 4-509. ECC_AGG_R5SS0_CORE1_WRAP_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
0					10			0		10					

Access Types Legend

Table 4-1072. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB84h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

4.10.5 ECC_AGG_R5SS0_CORE1_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

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Table 4-1073. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3014h

Figure 4-510. ECC_AGG_R5SS0_CORE1_CTRL Name Register

15	14	13	12	11	10	9	8
CHECK_SVBUS_TIMEOUT							
RW							
1							

7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
RW	RW	RW	RW	RW	RW	RW	RW
1	0	0	0	0	1	1	1

Access Types Legend

Table 4-1074. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.10.6 ECC_AGG_R5SS0_CORE1_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

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Table 4-1075. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3018h

Figure 4-511. ECC_AGG_R5SS0_CORE1_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-1076. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.10.7 ECC_AGG_R5SS0_CORE1_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

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Table 4-1077. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 301Ch

Figure 4-512. ECC_AGG_R5SS0_CORE1_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-1078. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.10.8 ECC_AGG_R5SS0_CORE1_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

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Table 4-1079. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3020h

Figure 4-513. ECC_AGG_R5SS0_CORE1_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
RW	RW DECR		RW	RW DECR		RW DECR		RW	RW		RW	RW INCR		RW INCR	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-1080. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.10.9 ECC_AGG_R5SS0_CORE1_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1081. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3024h

Figure 4-514. ECC_AGG_R5SS0_CORE1_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-1082. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.10.10 ECC_AGG_R5SS0_CORE1_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

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Table 4-1083. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3028h

Figure 4-515. ECC_AGG_R5SS0_CORE1_ERR_STAT3 Name Register

15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						RW	NONE
0						0	0
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						RW	RO
0						0	0

Access Types Legend

Table 4-1084. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.10.11 ECC_AGG_R5SS0_CORE1_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-1085. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 303Ch

Figure 4-516. ECC_AGG_R5SS0_CORE1_SEC_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1086. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.12 ECC_AGG_R5SS0_CORE1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1087. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3040h

Figure 4-517. ECC_AGG_R5SS0_CORE1_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1088. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend

Table 4-1088. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

4.10.13 ECC_AGG_R5SS0_CORE1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1089. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3080h

Figure 4-518. ECC_AGG_R5SS0_CORE1_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1090. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend

Table 4-1090. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

4.10.14 ECC_AGG_R5SS0_CORE1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1091. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 30C0h

Figure 4-519. ECC_AGG_R5SS0_CORE1_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1092. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend

Table 4-1092. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

4.10.15 ECC_AGG_R5SS0_CORE1_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-1093. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 313Ch

Figure 4-520. ECC_AGG_R5SS0_CORE1_DED_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1094. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.16 ECC_AGG_R5SS0_CORE1_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1095. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3140h

Figure 4-521. ECC_AGG_R5SS0_CORE1_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1096. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend

Table 4-1096. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

4.10.17 ECC_AGG_R5SS0_CORE1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1097. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3180h

Figure 4-522. ECC_AGG_R5SS0_CORE1_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1098. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend

Table 4-1098. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

4.10.18 ECC_AGG_R5SS0_CORE1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1099. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 31C0h

Figure 4-523. ECC_AGG_R5SS0_CORE1_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1100. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend

Table 4-1100. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

4.10.19 ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-1101. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3200h

Figure 4-524. ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1102. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.10.20 ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

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Table 4-1103. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3204h

Figure 4-525. ECC_AGG_R5SS0_CORE1_AGGR_ENABLE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1104. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.10.21 ECC_AGG_R5SS0_CORE1_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-1105. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3208h

Figure 4-526. ECC_AGG_R5SS0_CORE1_AGGR_STATUS_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW INCR		RW INCR	
0				0		0	

Access Types Legend

Table 4-1106. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.10.22 ECC_AGG_R5SS0_CORE1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-1107. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 320Ch

Figure 4-527. ECC_AGG_R5SS0_CORE1_AGGR_STATUS_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW DECR		RW DECR	
0				0		0	

Access Types Legend

Table 4-1108. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.10.23 ECC_AGG_R5SS1_CORE0_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1109. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4000h
ECC_AGG_R5SS1_CORE1	5300 7000h

Figure 4-528. ECC_AGG_R5SS1_CORE0_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11000					10			0		0					

Access Types Legend

Table 4-1110. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2AF8h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.10.24 ECC_AGG_R5SS1_CORE0_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-1111. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4008h
ECC_AGG_R5SS1_CORE1	5300 7008h

Figure 4-529. ECC_AGG_R5SS1_CORE0_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD_SVBUS_DONE	RD_SVBUS_ADDRESS														
RO	RW														
0	0														
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RD_SVBUS	RESERVED				ECC_VECTOR										
RW	NONE				RW										
0	0				0										

Access Types Legend

Table 4-1112. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.10.25 ECC_AGG_R5SS1_CORE0_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

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Table 4-1113. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 400Ch
ECC_AGG_R5SS1_CORE1	5300 700Ch

Figure 4-530. ECC_AGG_R5SS1_CORE0_STAT Name Register

15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					RO		
0					11100		
7	6	5	4	3	2	1	0
NUM_RAMS							
RO							
11100							

Access Types Legend

Table 4-1114. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	2B5Ch	Indicates the number of RAMS serviced by the ECC aggregator

4.10.26 ECC_AGG_R5SS1_CORE0_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1115. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4010h
ECC_AGG_R5SS1_CORE1	5300 7010h

Figure 4-531. ECC_AGG_R5SS1_CORE0_WRAP_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
RO				RO				RO		RO					
0				10				0		10					

Access Types Legend

Table 4-1116. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB84h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

4.10.27 ECC_AGG_R5SS1_CORE0_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1117. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4014h
ECC_AGG_R5SS1_CORE1	5300 7014h

Figure 4-532. ECC_AGG_R5SS1_CORE0_CTRL Name Register

15	14	13	12	11	10	9	8
CHECK_SVBUS_TIMEOUT							
RW							
1							
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
RW	RW	RW	RW	RW	RW	RW	RW
1	0	0	0	0	1	1	1

Access Types Legend

Table 4-1118. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.10.28 ECC_AGG_R5SS1_CORE0_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1119. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4018h
ECC_AGG_R5SS1_CORE1	5300 7018h

Figure 4-533. ECC_AGG_R5SS1_CORE0_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-1120. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.10.29 ECC_AGG_R5SS1_CORE0_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1121. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 401Ch
ECC_AGG_R5SS1_CORE1	5300 701Ch

Figure 4-534. ECC_AGG_R5SS1_CORE0_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-1122. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.10.30 ECC_AGG_R5SS1_CORE0_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

Return to Summary Table

Table 4-1123. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4020h
ECC_AGG_R5SS1_CORE1	5300 7020h

Figure 4-535. ECC_AGG_R5SS1_CORE0_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
RW	RW DECR		RW	RW DECR		RW DECR		RW	RW		RW	RW INCR		RW INCR	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-1124. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.10.31 ECC_AGG_R5SS1_CORE0_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1125. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4024h
ECC_AGG_R5SS1_CORE1	5300 7024h

Figure 4-536. ECC_AGG_R5SS1_CORE0_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-1126. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.10.32 ECC_AGG_R5SS1_CORE0_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1127. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4028h
ECC_AGG_R5SS1_CORE1	5300 7028h

Figure 4-537. ECC_AGG_R5SS1_CORE0_ERR_STAT3 Name Register

15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						RW	NONE
0						0	0
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						RW	RO
0						0	0

Access Types Legend

Table 4-1128. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.10.33 ECC_AGG_R5SS1_CORE0_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1129. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 403Ch
ECC_AGG_R5SS1_CORE1	5300 703Ch

Figure 4-538. ECC_AGG_R5SS1_CORE0_SEC_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1130. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.34 ECC_AGG_R5SS1_CORE0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1131. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4040h
ECC_AGG_R5SS1_CORE1	5300 7040h

Figure 4-539. ECC_AGG_R5SS1_CORE0_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1132. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend

Table 4-1132. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

4.10.35 ECC_AGG_R5SS1_CORE0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1133. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4080h
ECC_AGG_R5SS1_CORE1	5300 7080h

Figure 4-540. ECC_AGG_R5SS1_CORE0_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1134. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend

Table 4-1134. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

4.10.36 ECC_AGG_R5SS1_CORE0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1135. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 40C0h
ECC_AGG_R5SS1_CORE1	5300 70C0h

Figure 4-541. ECC_AGG_R5SS1_CORE0_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1136. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend

Table 4-1136. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

4.10.37 ECC_AGG_R5SS1_CORE0_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-1137. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 413Ch
ECC_AGG_R5SS1_CORE1	5300 713Ch

Figure 4-542. ECC_AGG_R5SS1_CORE0_DED_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1138. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.38 ECC_AGG_R5SS1_CORE0_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1139. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4140h
ECC_AGG_R5SS1_CORE1	5300 7140h

Figure 4-543. ECC_AGG_R5SS1_CORE0_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND	B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND	CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1140. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend

Table 4-1140. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

4.10.39 ECC_AGG_R5SS1_CORE0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1141. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4180h
ECC_AGG_R5SS1_CORE1	5300 7180h

Figure 4-544. ECC_AGG_R5SS1_CORE0_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET	B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET	CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1142. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend

Table 4-1142. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

4.10.40 ECC_AGG_R5SS1_CORE0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1143. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 41C0h
ECC_AGG_R5SS1_CORE1	5300 71C0h

Figure 4-545. ECC_AGG_R5SS1_CORE0_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR	B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR	CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1144. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend

Table 4-1144. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

4.10.41 ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-1145. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4200h
ECC_AGG_R5SS1_CORE1	5300 7200h

Figure 4-546. ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1146. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.10.42 ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

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Table 4-1147. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4204h
ECC_AGG_R5SS1_CORE1	5300 7204h

Figure 4-547. ECC_AGG_R5SS1_CORE0_AGGR_ENABLE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1148. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.10.43 ECC_AGG_R5SS1_CORE0_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-1149. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4208h
ECC_AGG_R5SS1_CORE1	5300 7208h

Figure 4-548. ECC_AGG_R5SS1_CORE0_AGGR_STATUS_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW INCR		RW INCR	
0				0		0	

Access Types Legend

Table 4-1150. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.10.44 ECC_AGG_R5SS1_CORE0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-1151. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 420Ch
ECC_AGG_R5SS1_CORE1	5300 720Ch

Figure 4-549. ECC_AGG_R5SS1_CORE0_AGGR_STATUS_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW DECR		RW DECR	
0				0		0	

Access Types Legend

Table 4-1152. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.10.45 ECC_AGG_R5SS1_CORE1_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

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Table 4-1153. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4000h
ECC_AGG_R5SS1_CORE1	5300 7000h

Figure 4-550. ECC_AGG_R5SS1_CORE1_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11000					10			0		0					

Access Types Legend

Table 4-1154. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2AF8h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.10.46 ECC_AGG_R5SS1_CORE1_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-1155. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4008h
ECC_AGG_R5SS1_CORE1	5300 7008h

Figure 4-551. ECC_AGG_R5SS1_CORE1_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD_SVBUS_DONE	RD_SVBUS_ADDRESS														
RO	RW														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
RW	NONE				RW										
0	0				0										

Access Types Legend

Table 4-1156. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.10.47 ECC_AGG_R5SS1_CORE1_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1157. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 400Ch
ECC_AGG_R5SS1_CORE1	5300 700Ch

Figure 4-552. ECC_AGG_R5SS1_CORE1_STAT Name Register

15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					RO		
0					11100		
7	6	5	4	3	2	1	0
NUM_RAMS							
RO							
11100							

Access Types Legend

Table 4-1158. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	2B5Ch	Indicates the number of RAMS serviced by the ECC aggregator

4.10.48 ECC_AGG_R5SS1_CORE1_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1159. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4010h
ECC_AGG_R5SS1_CORE1	5300 7010h

Figure 4-553. ECC_AGG_R5SS1_CORE1_WRAP_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
RO				RO				RO		RO					
0				10				0		10					

Access Types Legend

Table 4-1160. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB84h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

4.10.49 ECC_AGG_R5SS1_CORE1_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1161. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4014h
ECC_AGG_R5SS1_CORE1	5300 7014h

Figure 4-554. ECC_AGG_R5SS1_CORE1_CTRL Name Register

15	14	13	12	11	10	9	8
CHECK_SVBUS_TIMEOUT							
RW							
1							
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
RW	RW	RW	RW	RW	RW	RW	RW
1	0	0	0	0	1	1	1

Access Types Legend

Table 4-1162. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

4.10.50 ECC_AGG_R5SS1_CORE1_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1163. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4018h
ECC_AGG_R5SS1_CORE1	5300 7018h

Figure 4-555. ECC_AGG_R5SS1_CORE1_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-1164. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.10.51 ECC_AGG_R5SS1_CORE1_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1165. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 401Ch
ECC_AGG_R5SS1_CORE1	5300 701Ch

Figure 4-556. ECC_AGG_R5SS1_CORE1_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-1166. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

4.10.52 ECC_AGG_R5SS1_CORE1_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

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Table 4-1167. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4020h
ECC_AGG_R5SS1_CORE1	5300 7020h

Figure 4-557. ECC_AGG_R5SS1_CORE1_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
RW	RW DECR		RW	RW DECR		RW DECR		RW	RW		RW	RW INCR		RW INCR	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-1168. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

4.10.53 ECC_AGG_R5SS1_CORE1_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1169. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4024h
ECC_AGG_R5SS1_CORE1	5300 7024h

Figure 4-558. ECC_AGG_R5SS1_CORE1_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-1170. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

4.10.54 ECC_AGG_R5SS1_CORE1_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1171. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4028h
ECC_AGG_R5SS1_CORE1	5300 7028h

Figure 4-559. ECC_AGG_R5SS1_CORE1_ERR_STAT3 Name Register

15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						RW	NONE
0						0	0
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						RW	RO
0						0	0

Access Types Legend

Table 4-1172. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

4.10.55 ECC_AGG_R5SS1_CORE1_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1173. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 403Ch
ECC_AGG_R5SS1_CORE1	5300 703Ch

Figure 4-560. ECC_AGG_R5SS1_CORE1_SEC_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1174. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.56 ECC_AGG_R5SS1_CORE1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1175. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4040h
ECC_AGG_R5SS1_CORE1	5300 7040h

Figure 4-561. ECC_AGG_R5SS1_CORE1_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1176. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend

Table 4-1176. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

4.10.57 ECC_AGG_R5SS1_CORE1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1177. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4080h
ECC_AGG_R5SS1_CORE1	5300 7080h

Figure 4-562. ECC_AGG_R5SS1_CORE1_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1178. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend

Table 4-1178. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

4.10.58 ECC_AGG_R5SS1_CORE1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1179. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 40C0h
ECC_AGG_R5SS1_CORE1	5300 70C0h

Figure 4-563. ECC_AGG_R5SS1_CORE1_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1180. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend

Table 4-1180. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

4.10.59 ECC_AGG_R5SS1_CORE1_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-1181. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 413Ch
ECC_AGG_R5SS1_CORE1	5300 713Ch

Figure 4-564. ECC_AGG_R5SS1_CORE1_DED_EOI_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOI_WR							
RW							
0							

Access Types Legend

Table 4-1182. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

4.10.60 ECC_AGG_R5SS1_CORE1_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-1183. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4140h
ECC_AGG_R5SS1_CORE1	5300 7140h

Figure 4-565. ECC_AGG_R5SS1_CORE1_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND	B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND	CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1184. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend

Table 4-1184. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

4.10.61 ECC_AGG_R5SS1_CORE1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

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Table 4-1185. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4180h
ECC_AGG_R5SS1_CORE1	5300 7180h

Figure 4-566. ECC_AGG_R5SS1_CORE1_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET	B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET	CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1186. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend

Table 4-1186. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

4.10.62 ECC_AGG_R5SS1_CORE1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-1187. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 41C0h
ECC_AGG_R5SS1_CORE1	5300 71C0h

Figure 4-567. ECC_AGG_R5SS1_CORE1_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR	B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
NONE				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR	CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1188. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend

Table 4-1188. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

4.10.63 ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-1189. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4200h
ECC_AGG_R5SS1_CORE1	5300 7200h

Figure 4-568. ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1190. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

4.10.64 ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

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Table 4-1191. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4204h
ECC_AGG_R5SS1_CORE1	5300 7204h

Figure 4-569. ECC_AGG_R5SS1_CORE1_AGGR_ENABLE_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-1192. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

4.10.65 ECC_AGG_R5SS1_CORE1_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-1193. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 4208h
ECC_AGG_R5SS1_CORE1	5300 7208h

Figure 4-570. ECC_AGG_R5SS1_CORE1_AGGR_STATUS_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW INCR		RW INCR	
0				0		0	

Access Types Legend

Table 4-1194. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

4.10.66 ECC_AGG_R5SS1_CORE1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1195. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS1_CORE0	5300 420Ch
ECC_AGG_R5SS1_CORE1	5300 720Ch

Figure 4-571. ECC_AGG_R5SS1_CORE1_AGGR_STATUS_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				RW DECR		RW DECR	
0				0		0	

Access Types Legend

Table 4-1196. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

Table 4-1197. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
RW DECR	RW DECR	Undefined
RW INCR	RW INCR	Undefined

4.11 MSS_GPIO Registers

Table 4-1198. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2

Offset	Length	Acronym	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
0h	32	GPIO0_PID	GPIO Peripheral ID Register	5200 0000h	5200 1000h	5200 2000h
4h	8	GPIO0_PCR	Peripheral Control Register	5200 0004h	5200 1004h	5200 2004h
8h	32	GPIO0_BINTEN	Bit Interrupt Enable Register	5200 0008h	5200 1008h	5200 2008h
10h	32	GPIO0_DIR01	Direction Register	5200 0010h	5200 1010h	5200 2010h
14h	32	GPIO0_OUT_DATA01	Output Drive State Register	5200 0014h	5200 1014h	5200 2014h
18h	32	GPIO0_SET_DATA01	Set Output Drive State Register	5200 0018h	5200 1018h	5200 2018h
1Ch	32	GPIO0_CLR_DATA01	Clear Output Drive State Register	5200 001Ch	5200 101Ch	5200 201Ch
20h	32	GPIO0_IN_DATA01	Bank Status Register	5200 0020h	5200 1020h	5200 2020h
24h	32	GPIO0_SET_RIS_TRIG01	Set Rising Edge Detection Register	5200 0024h	5200 1024h	5200 2024h
28h	32	GPIO0_CLR_RIS_TRIG01	Clear Rising Edge Detection Register	5200 0028h	5200 1028h	5200 2028h
2Ch	32	GPIO0_SET_FAL_TRIG01	Set Falling Edge Detection Register	5200 002Ch	5200 102Ch	5200 202Ch
30h	32	GPIO0_CLR_FAL_TRIG01	Clear Falling Edge Detection Register	5200 0030h	5200 1030h	5200 2030h
34h	32	GPIO0_INTSTAT01	Bank Interrupt Status Register	5200 0034h	5200 1034h	5200 2034h
38h	32	GPIO0_DIR23	Direction Register	5200 0038h	5200 1038h	5200 2038h
3Ch	32	GPIO0_OUT_DATA23	Output Drive State Register	5200 003Ch	5200 103Ch	5200 203Ch
40h	32	GPIO0_SET_DATA23	Set Output Drive State Register	5200 0040h	5200 1040h	5200 2040h
44h	32	GPIO0_CLR_DATA23	Clear Output Drive State Register	5200 0044h	5200 1044h	5200 2044h
48h	32	GPIO0_IN_DATA23	Bank Status Register	5200 0048h	5200 1048h	5200 2048h
4Ch	32	GPIO0_SET_RIS_TRIG23	Set Rising Edge Detection Register	5200 004Ch	5200 104Ch	5200 204Ch
50h	32	GPIO0_CLR_RIS_TRIG23	Clear Rising Edge Detection Register	5200 0050h	5200 1050h	5200 2050h
54h	32	GPIO0_SET_FAL_TRIG23	Set Falling Edge Detection Register	5200 0054h	5200 1054h	5200 2054h
58h	32	GPIO0_CLR_FAL_TRIG23	Clear Falling Edge Detection Register	5200 0058h	5200 1058h	5200 2058h
5Ch	32	GPIO0_INTSTAT23	Bank Interrupt Status Register	5200 005Ch	5200 105Ch	5200 205Ch
60h	32	GPIO0_DIR45	Direction Register	5200 0060h	5200 1060h	5200 2060h

Table 4-1198. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
64h	32	GPIO0_OUT_DATA45	Output Drive State Register	5200 0064h	5200 1064h	5200 2064h
68h	32	GPIO0_SET_DATA45	Set Output Drive State Register	5200 0068h	5200 1068h	5200 2068h
6Ch	32	GPIO0_CLR_DATA45	Clear Output Drive State Register	5200 006Ch	5200 106Ch	5200 206Ch
70h	32	GPIO0_IN_DATA45	Bank Status Register	5200 0070h	5200 1070h	5200 2070h
74h	32	GPIO0_SET_RIS_TRIG45	Set Rising Edge Detection Register	5200 0074h	5200 1074h	5200 2074h
78h	32	GPIO0_CLR_RIS_TRIG45	Clear Rising Edge Detection Register	5200 0078h	5200 1078h	5200 2078h
7Ch	32	GPIO0_SET_FAL_TRIG45	Set Falling Edge Detection Register	5200 007Ch	5200 107Ch	5200 207Ch
80h	32	GPIO0_CLR_FAL_TRIG45	Clear Falling Edge Detection Register	5200 0080h	5200 1080h	5200 2080h
84h	32	GPIO0_INTSTAT45	Bank Interrupt Status Register	5200 0084h	5200 1084h	5200 2084h
88h	32	GPIO0_DIR67	Direction Register	5200 0088h	5200 1088h	5200 2088h
8Ch	32	GPIO0_OUT_DATA67	Output Drive State Register	5200 008Ch	5200 108Ch	5200 208Ch
90h	32	GPIO0_SET_DATA67	Set Output Drive State Register	5200 0090h	5200 1090h	5200 2090h
94h	32	GPIO0_CLR_DATA67	Clear Output Drive State Register	5200 0094h	5200 1094h	5200 2094h
98h	32	GPIO0_IN_DATA67	Bank Status Register	5200 0098h	5200 1098h	5200 2098h
9Ch	32	GPIO0_SET_RIS_TRIG67	Set Rising Edge Detection Register	5200 009Ch	5200 109Ch	5200 209Ch
A0h	32	GPIO0_CLR_RIS_TRIG67	Clear Rising Edge Detection Register	5200 00A0h	5200 10A0h	5200 20A0h
A4h	32	GPIO0_SET_FAL_TRIG67	Set Falling Edge Detection Register	5200 00A4h	5200 10A4h	5200 20A4h
A8h	32	GPIO0_CLR_FAL_TRIG67	Clear Falling Edge Detection Register	5200 00A8h	5200 10A8h	5200 20A8h
ACh	32	GPIO0_INTSTAT67	Bank Interrupt Status Register	5200 00ACh	5200 10ACh	5200 20ACh
B0h	32	GPIO0_DIR8	Direction Register	5200 00B0h	5200 10B0h	5200 20B0h
B4h	32	GPIO0_OUT_DATA8	Output Drive State Register	5200 00B4h	5200 10B4h	5200 20B4h
B8h	32	GPIO0_SET_DATA8	Set Output Drive State Register	5200 00B8h	5200 10B8h	5200 20B8h
BCh	32	GPIO0_CLR_DATA8	Clear Output Drive State Register	5200 00BCh	5200 10BCh	5200 20BCh
C0h	32	GPIO0_IN_DATA8	Bank Status Register	5200 00C0h	5200 10C0h	5200 20C0h
C4h	16	GPIO0_SET_RIS_TRIG8	Set Rising Edge Detection Register	5200 00C4h	5200 10C4h	5200 20C4h
C8h	16	GPIO0_CLR_RIS_TRIG8	Clear Rising Edge Detection Register	5200 00C8h	5200 10C8h	5200 20C8h
CCh	16	GPIO0_SET_FAL_TRIG8	Set Falling Edge Detection Register	5200 00CCh	5200 10CCh	5200 20CCh
D0h	16	GPIO0_CLR_FAL_TRIG8	Clear Falling Edge Detection Register	5200 00D0h	5200 10D0h	5200 20D0h
D4h	32	GPIO0_INTSTAT8	Bank Interrupt Status Register	5200 00D4h	5200 10D4h	5200 20D4h

Table 4-1199. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2

Offset	Length	Acronym	Register Name	GPIO3 Physical Address
0h	32	GPIO0_PID	GPIO Peripheral ID Register	5200 3000h
4h	8	GPIO0_PCR	Peripheral Control Register	5200 3004h
8h	32	GPIO0_BINTEN	Bit Interrupt Enable Register	5200 3008h
10h	32	GPIO0_DIR01	Direction Register	5200 3010h
14h	32	GPIO0_OUT_DATA01	Output Drive State Register	5200 3014h
18h	32	GPIO0_SET_DATA01	Set Output Drive State Register	5200 3018h
1Ch	32	GPIO0_CLR_DATA01	Clear Output Drive State Register	5200 301Ch
20h	32	GPIO0_IN_DATA01	Bank Status Register	5200 3020h
24h	32	GPIO0_SET_RIS_TRIG01	Set Rising Edge Detection Register	5200 3024h
28h	32	GPIO0_CLR_RIS_TRIG01	Clear Rising Edge Detection Register	5200 3028h
2Ch	32	GPIO0_SET_FAL_TRIG01	Set Falling Edge Detection Register	5200 302Ch
30h	32	GPIO0_CLR_FAL_TRIG01	Clear Falling Edge Detection Register	5200 3030h
34h	32	GPIO0_INTSTAT01	Bank Interrupt Status Register	5200 3034h
38h	32	GPIO0_DIR23	Direction Register	5200 3038h
3Ch	32	GPIO0_OUT_DATA23	Output Drive State Register	5200 303Ch
40h	32	GPIO0_SET_DATA23	Set Output Drive State Register	5200 3040h
44h	32	GPIO0_CLR_DATA23	Clear Output Drive State Register	5200 3044h
48h	32	GPIO0_IN_DATA23	Bank Status Register	5200 3048h
4Ch	32	GPIO0_SET_RIS_TRIG23	Set Rising Edge Detection Register	5200 304Ch
50h	32	GPIO0_CLR_RIS_TRIG23	Clear Rising Edge Detection Register	5200 3050h
54h	32	GPIO0_SET_FAL_TRIG23	Set Falling Edge Detection Register	5200 3054h
58h	32	GPIO0_CLR_FAL_TRIG23	Clear Falling Edge Detection Register	5200 3058h
5Ch	32	GPIO0_INTSTAT23	Bank Interrupt Status Register	5200 305Ch
60h	32	GPIO0_DIR45	Direction Register	5200 3060h
64h	32	GPIO0_OUT_DATA45	Output Drive State Register	5200 3064h
68h	32	GPIO0_SET_DATA45	Set Output Drive State Register	5200 3068h
6Ch	32	GPIO0_CLR_DATA45	Clear Output Drive State Register	5200 306Ch
70h	32	GPIO0_IN_DATA45	Bank Status Register	5200 3070h
74h	32	GPIO0_SET_RIS_TRIG45	Set Rising Edge Detection Register	5200 3074h
78h	32	GPIO0_CLR_RIS_TRIG45	Clear Rising Edge Detection Register	5200 3078h
7Ch	32	GPIO0_SET_FAL_TRIG45	Set Falling Edge Detection Register	5200 307Ch
80h	32	GPIO0_CLR_FAL_TRIG45	Clear Falling Edge Detection Register	5200 3080h
84h	32	GPIO0_INTSTAT45	Bank Interrupt Status Register	5200 3084h
88h	32	GPIO0_DIR67	Direction Register	5200 3088h
8Ch	32	GPIO0_OUT_DATA67	Output Drive State Register	5200 308Ch
90h	32	GPIO0_SET_DATA67	Set Output Drive State Register	5200 3090h
94h	32	GPIO0_CLR_DATA67	Clear Output Drive State Register	5200 3094h
98h	32	GPIO0_IN_DATA67	Bank Status Register	5200 3098h

Table 4-1199. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	GPIO3 Physical Address
9Ch	32	GPIO0_SET_RIS_TRIG67	Set Rising Edge Detection Register	5200 309Ch
A0h	32	GPIO0_CLR_RIS_TRIG67	Clear Rising Edge Detection Register	5200 30A0h
A4h	32	GPIO0_SET_FAL_TRIG67	Set Falling Edge Detection Register	5200 30A4h
A8h	32	GPIO0_CLR_FAL_TRIG67	Clear Falling Edge Detection Register	5200 30A8h
ACh	32	GPIO0_INTSTAT67	Bank Interrupt Status Register	5200 30ACh
B0h	32	GPIO0_DIR8	Direction Register	5200 30B0h
B4h	32	GPIO0_OUT_DATA8	Output Drive State Register	5200 30B4h
B8h	32	GPIO0_SET_DATA8	Set Output Drive State Register	5200 30B8h
BCh	32	GPIO0_CLR_DATA8	Clear Output Drive State Register	5200 30BCh
C0h	32	GPIO0_IN_DATA8	Bank Status Register	5200 30C0h
C4h	16	GPIO0_SET_RIS_TRIG8	Set Rising Edge Detection Register	5200 30C4h
C8h	16	GPIO0_CLR_RIS_TRIG8	Clear Rising Edge Detection Register	5200 30C8h
CCh	16	GPIO0_SET_FAL_TRIG8	Set Falling Edge Detection Register	5200 30CCh
D0h	16	GPIO0_CLR_FAL_TRIG8	Clear Falling Edge Detection Register	5200 30D0h
D4h	32	GPIO0_INTSTAT8	Bank Interrupt Status Register	5200 30D4h

Table 4-1200. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	GPIO0_PID	GPIO Peripheral ID Register
4h	8	GPIO0_PCR	Peripheral Control Register
8h	32	GPIO0_BINTEN	Bit Interrupt Enable Register
10h	32	GPIO0_DIR01	Direction Register
14h	32	GPIO0_OUT_DATA01	Output Drive State Register
18h	32	GPIO0_SET_DATA01	Set Output Drive State Register
1Ch	32	GPIO0_CLR_DATA01	Clear Output Drive State Register
20h	32	GPIO0_IN_DATA01	Bank Status Register
24h	32	GPIO0_SET_RIS_TRIG01	Set Rising Edge Detection Register
28h	32	GPIO0_CLR_RIS_TRIG01	Clear Rising Edge Detection Register
2Ch	32	GPIO0_SET_FAL_TRIG01	Set Falling Edge Detection Register
30h	32	GPIO0_CLR_FAL_TRIG01	Clear Falling Edge Detection Register
34h	32	GPIO0_INTSTAT01	Bank Interrupt Status Register
38h	32	GPIO0_DIR23	Direction Register
3Ch	32	GPIO0_OUT_DATA23	Output Drive State Register
40h	32	GPIO0_SET_DATA23	Set Output Drive State Register
44h	32	GPIO0_CLR_DATA23	Clear Output Drive State Register
48h	32	GPIO0_IN_DATA23	Bank Status Register
4Ch	32	GPIO0_SET_RIS_TRIG23	Set Rising Edge Detection Register

Table 4-1200. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
50h	32	GPIO0_CLR_RIS_TRIG23	Clear Rising Edge Detection Register
54h	32	GPIO0_SET_FAL_TRIG23	Set Falling Edge Detection Register
58h	32	GPIO0_CLR_FAL_TRIG23	Clear Falling Edge Detection Register
5Ch	32	GPIO0_INTSTAT23	Bank Interrupt Status Register
60h	32	GPIO0_DIR45	Direction Register
64h	32	GPIO0_OUT_DATA45	Output Drive State Register
68h	32	GPIO0_SET_DATA45	Set Output Drive State Register
6Ch	32	GPIO0_CLR_DATA45	Clear Output Drive State Register
70h	32	GPIO0_IN_DATA45	Bank Status Register
74h	32	GPIO0_SET_RIS_TRIG45	Set Rising Edge Detection Register
78h	32	GPIO0_CLR_RIS_TRIG45	Clear Rising Edge Detection Register
7Ch	32	GPIO0_SET_FAL_TRIG45	Set Falling Edge Detection Register
80h	32	GPIO0_CLR_FAL_TRIG45	Clear Falling Edge Detection Register
84h	32	GPIO0_INTSTAT45	Bank Interrupt Status Register
88h	32	GPIO0_DIR67	Direction Register
8Ch	32	GPIO0_OUT_DATA67	Output Drive State Register
90h	32	GPIO0_SET_DATA67	Set Output Drive State Register
94h	32	GPIO0_CLR_DATA67	Clear Output Drive State Register
98h	32	GPIO0_IN_DATA67	Bank Status Register
9Ch	32	GPIO0_SET_RIS_TRIG67	Set Rising Edge Detection Register
A0h	32	GPIO0_CLR_RIS_TRIG67	Clear Rising Edge Detection Register
A4h	32	GPIO0_SET_FAL_TRIG67	Set Falling Edge Detection Register
A8h	32	GPIO0_CLR_FAL_TRIG67	Clear Falling Edge Detection Register
ACh	32	GPIO0_INTSTAT67	Bank Interrupt Status Register
B0h	32	GPIO0_DIR8	Direction Register
B4h	32	GPIO0_OUT_DATA8	Output Drive State Register
B8h	32	GPIO0_SET_DATA8	Set Output Drive State Register
BCh	32	GPIO0_CLR_DATA8	Clear Output Drive State Register
C0h	32	GPIO0_IN_DATA8	Bank Status Register
C4h	16	GPIO0_SET_RIS_TRIG8	Set Rising Edge Detection Register
C8h	16	GPIO0_CLR_RIS_TRIG8	Clear Rising Edge Detection Register
CCh	16	GPIO0_SET_FAL_TRIG8	Set Falling Edge Detection Register
D0h	16	GPIO0_CLR_FAL_TRIG8	Clear Falling Edge Detection Register
D4h	32	GPIO0_INTSTAT8	Bank Interrupt Status Register

Table 4-1201. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2

Offset	Length	Acronym	Register Name
0h	32	GPIO0_PID	GPIO Peripheral ID Register
4h	8	GPIO0_PCR	Peripheral Control Register
8h	32	GPIO0_BINTEN	Bit Interrupt Enable Register
10h	32	GPIO0_DIR01	Direction Register
14h	32	GPIO0_OUT_DATA01	Output Drive State Register
18h	32	GPIO0_SET_DATA01	Set Output Drive State Register
1Ch	32	GPIO0_CLR_DATA01	Clear Output Drive State Register
20h	32	GPIO0_IN_DATA01	Bank Status Register
24h	32	GPIO0_SET_RIS_TRIG01	Set Rising Edge Detection Register
28h	32	GPIO0_CLR_RIS_TRIG01	Clear Rising Edge Detection Register
2Ch	32	GPIO0_SET_FAL_TRIG01	Set Falling Edge Detection Register
30h	32	GPIO0_CLR_FAL_TRIG01	Clear Falling Edge Detection Register
34h	32	GPIO0_INTSTAT01	Bank Interrupt Status Register
38h	32	GPIO0_DIR23	Direction Register
3Ch	32	GPIO0_OUT_DATA23	Output Drive State Register
40h	32	GPIO0_SET_DATA23	Set Output Drive State Register
44h	32	GPIO0_CLR_DATA23	Clear Output Drive State Register
48h	32	GPIO0_IN_DATA23	Bank Status Register
4Ch	32	GPIO0_SET_RIS_TRIG23	Set Rising Edge Detection Register
50h	32	GPIO0_CLR_RIS_TRIG23	Clear Rising Edge Detection Register
54h	32	GPIO0_SET_FAL_TRIG23	Set Falling Edge Detection Register
58h	32	GPIO0_CLR_FAL_TRIG23	Clear Falling Edge Detection Register
5Ch	32	GPIO0_INTSTAT23	Bank Interrupt Status Register
60h	32	GPIO0_DIR45	Direction Register
64h	32	GPIO0_OUT_DATA45	Output Drive State Register
68h	32	GPIO0_SET_DATA45	Set Output Drive State Register
6Ch	32	GPIO0_CLR_DATA45	Clear Output Drive State Register
70h	32	GPIO0_IN_DATA45	Bank Status Register
74h	32	GPIO0_SET_RIS_TRIG45	Set Rising Edge Detection Register
78h	32	GPIO0_CLR_RIS_TRIG45	Clear Rising Edge Detection Register
7Ch	32	GPIO0_SET_FAL_TRIG45	Set Falling Edge Detection Register
80h	32	GPIO0_CLR_FAL_TRIG45	Clear Falling Edge Detection Register
84h	32	GPIO0_INTSTAT45	Bank Interrupt Status Register
88h	32	GPIO0_DIR67	Direction Register
8Ch	32	GPIO0_OUT_DATA67	Output Drive State Register
90h	32	GPIO0_SET_DATA67	Set Output Drive State Register
94h	32	GPIO0_CLR_DATA67	Clear Output Drive State Register
98h	32	GPIO0_IN_DATA67	Bank Status Register

Table 4-1201. GPIO0, GPIO0_GPIO Registers, Base Address=5200 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name
9Ch	32	GPIO0_SET_RIS_TRIG67	Set Rising Edge Detection Register
A0h	32	GPIO0_CLR_RIS_TRIG67	Clear Rising Edge Detection Register
A4h	32	GPIO0_SET_FAL_TRIG67	Set Falling Edge Detection Register
A8h	32	GPIO0_CLR_FAL_TRIG67	Clear Falling Edge Detection Register
ACh	32	GPIO0_INTSTAT67	Bank Interrupt Status Register
B0h	32	GPIO0_DIR8	Direction Register
B4h	32	GPIO0_OUT_DATA8	Output Drive State Register
B8h	32	GPIO0_SET_DATA8	Set Output Drive State Register
BCh	32	GPIO0_CLR_DATA8	Clear Output Drive State Register
C0h	32	GPIO0_IN_DATA8	Bank Status Register
C4h	16	GPIO0_SET_RIS_TRIG8	Set Rising Edge Detection Register
C8h	16	GPIO0_CLR_RIS_TRIG8	Clear Rising Edge Detection Register
CCh	16	GPIO0_SET_FAL_TRIG8	Set Falling Edge Detection Register
D0h	16	GPIO0_CLR_FAL_TRIG8	Clear Falling Edge Detection Register
D4h	32	GPIO0_INTSTAT8	Bank Interrupt Status Register

4.11.1 GPIO0_PID Register (Offset = 0h) [reset = h]

Short Description: GPIO Peripheral ID Register

Long Description:

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Table 4-1202. Instance Table

Instance Name	Physical Address
GPIO0	5200 0000h
GPIO1	5200 1000h
GPIO2	5200 2000h
GPIO3	5200 3000h

Figure 4-572. GPIO0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		RO		RO											
1		0		10010000011											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
101					1			0		101					

Access Types Legend

Table 4-1203. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Current scheme
29 - 28	RESERVED	RO		RESERVED
27 - 16	FUNC	RO	254A47A8Bh	Function code assigned to TCP3
15 - 11	RTL	RO	65h	RTL Version R code
10 - 8	MAJOR	RO	1h	Major revision X code
7 - 6	CUSTOM	RO	0h	Custom version code
5 - 0	MINOR	RO	65h	Minor revision Y code

4.11.2 GPIO0_PCR Register (Offset = 4h) [reset = h]

Short Description: Peripheral Control Register

Long Description:

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Table 4-1204. Instance Table

Instance Name	Physical Address
GPIO0	5200 0004h
GPIO1	5200 1004h
GPIO2	5200 2004h
GPIO3	5200 3004h

Figure 4-573. GPIO0_PCR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						RO	RO
0						0	1

Access Types Legend

Table 4-1205. PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFT	RO	0h	Used in conjunction with FREE bit to determine the emulation suspend mode.
0	FREE	RO	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend.

4.11.3 GPIO0_BINTEN Register (Offset = 8h) [reset = h]

Short Description: Bit Interrupt Enable Register

Long Description:

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Table 4-1206. Instance Table

Instance Name	Physical Address
GPIO0	5200 0008h
GPIO1	5200 1008h
GPIO2	5200 2008h
GPIO3	5200 3008h

Figure 4-574. GPIO0_BINTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN															
RW															
0															

Access Types Legend

Table 4-1207. BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	EN	RW	0h	Per bank interrupt enable. 0 = disable, 1 = enable.

4.11.4 GPIO0_DIR01 Register (Offset = 10h) [reset = h]

Short Description: Direction Register

Long Description:

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Table 4-1208. Instance Table

Instance Name	Physical Address
GPIO0	5200 0010h
GPIO1	5200 1010h
GPIO2	5200 2010h
GPIO3	5200 3010h

Figure 4-575. GPIO0_DIR01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR1															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR0															
RW															
1111111111111111															

Access Types Legend

Table 4-1209. DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR1	RW	3F28CB715 71C7h	Direction of GPIO bank 1 bits, 0 = output, 1 = input.
15 - 0	DIR0	RW	3F28CB715 71C7h	Direction of GPIO bank 0 bits, 0 = output, 1 = input.

4.11.5 GPIO0_OUT_DATA01 Register (Offset = 14h) [reset = h]

Short Description: Output Drive State Register

Long Description:

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Table 4-1210. Instance Table

Instance Name	Physical Address
GPIO0	5200 0014h
GPIO1	5200 1014h
GPIO2	5200 2014h
GPIO3	5200 3014h

Figure 4-576. GPIO0_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT0															
RW															
0															

Access Types Legend

Table 4-1211. OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT1	RW	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT0	RW	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

4.11.6 GPIO0_SET_DATA01 Register (Offset = 18h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1212. Instance Table

Instance Name	Physical Address
GPIO0	5200 0018h
GPIO1	5200 1018h
GPIO2	5200 2018h
GPIO3	5200 3018h

Figure 4-577. GPIO0_SET_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET0															
RW															
0															

Access Types Legend

Table 4-1213. SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET1	RW	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state.
15 - 0	SET0	RW	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state.

4.11.7 GPIO0_CLR_DATA01 Register (Offset = 1Ch) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1214. Instance Table

Instance Name	Physical Address
GPIO0	5200 001Ch
GPIO1	5200 101Ch
GPIO2	5200 201Ch
GPIO3	5200 301Ch

Figure 4-578. GPIO0_CLR_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR0															
RW															
0															

Access Types Legend

Table 4-1215. CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR1	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR0	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

4.11.8 GPIO0_IN_DATA01 Register (Offset = 20h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1216. Instance Table

Instance Name	Physical Address
GPIO0	5200 0020h
GPIO1	5200 1020h
GPIO2	5200 2020h
GPIO3	5200 3020h

Figure 4-579. GPIO0_IN_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN0															
RO															
0															

Access Types Legend

Table 4-1217. IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN1	RO	0h	Status of GPIO bank 1 bits.
15 - 0	IN0	RO	0h	Status of GPIO bank 0 bits.

4.11.9 GPIO0_SET_RIS_TRIG01 Register (Offset = 24h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1218. Instance Table

Instance Name	Physical Address
GPIO0	5200 0024h
GPIO1	5200 1024h
GPIO2	5200 2024h
GPIO3	5200 3024h

Figure 4-580. GPIO0_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS0															
RW															
0															

Access Types Legend

Table 4-1219. SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS1	RW	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits.
15 - 0	SETRIS0	RW	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits.

4.11.10 GPIO0_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1220. Instance Table

Instance Name	Physical Address
GPIO0	5200 0028h
GPIO1	5200 1028h
GPIO2	5200 2028h
GPIO3	5200 3028h

Figure 4-581. GPIO0_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS0															
RW															
0															

Access Types Legend

Table 4-1221. CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS1	RW	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits.
15 - 0	CLRRIS0	RW	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits.

4.11.11 GPIO0_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1222. Instance Table

Instance Name	Physical Address
GPIO0	5200 002Ch
GPIO1	5200 102Ch
GPIO2	5200 202Ch
GPIO3	5200 302Ch

Figure 4-582. GPIO0_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL0															
RW															
0															

Access Types Legend

Table 4-1223. SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL1	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits.
15 - 0	SETFAL0	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits.

4.11.12 GPIO0_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1224. Instance Table

Instance Name	Physical Address
GPIO0	5200 0030h
GPIO1	5200 1030h
GPIO2	5200 2030h
GPIO3	5200 3030h

Figure 4-583. GPIO0_CLR_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL0															
RW															
0															

Access Types Legend

Table 4-1225. CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL1	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits.
15 - 0	CLRFAL0	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits.

4.11.13 GPIO0_INTSTAT01 Register (Offset = 34h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1226. Instance Table

Instance Name	Physical Address
GPIO0	5200 0034h
GPIO1	5200 1034h
GPIO2	5200 2034h
GPIO3	5200 3034h

Figure 4-584. GPIO0_INTSTAT01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT0															
RW															
0															

Access Types Legend

Table 4-1227. INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT1	RW	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT0	RW	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

4.11.14 GPIO0_DIR23 Register (Offset = 38h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1228. Instance Table

Instance Name	Physical Address
GPIO0	5200 0038h
GPIO1	5200 1038h
GPIO2	5200 2038h
GPIO3	5200 3038h

Figure 4-585. GPIO0_DIR23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR3															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR2															
RW															
1111111111111111															

Access Types Legend

Table 4-1229. DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR3	RW	3F28CB715 71C7h	Direction of GPIO bank 3 bits, 0 = output, 1 = input.
15 - 0	DIR2	RW	3F28CB715 71C7h	Direction of GPIO bank 2 bits, 0 = output, 1 = input.

4.11.15 GPIO0_OUT_DATA23 Register (Offset = 3Ch) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1230. Instance Table

Instance Name	Physical Address
GPIO0	5200 003Ch
GPIO1	5200 103Ch
GPIO2	5200 203Ch
GPIO3	5200 303Ch

Figure 4-586. GPIO0_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT2															
RW															
0															

Access Types Legend

Table 4-1231. OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT3	RW	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT2	RW	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

4.11.16 GPIO0_SET_DATA23 Register (Offset = 40h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1232. Instance Table

Instance Name	Physical Address
GPIO0	5200 0040h
GPIO1	5200 1040h
GPIO2	5200 2040h
GPIO3	5200 3040h

Figure 4-587. GPIO0_SET_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET2															
RW															
0															

Access Types Legend

Table 4-1233. SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET3	RW	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state.
15 - 0	SET2	RW	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state.

4.11.17 GPIO0_CLR_DATA23 Register (Offset = 44h) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1234. Instance Table

Instance Name	Physical Address
GPIO0	5200 0044h
GPIO1	5200 1044h
GPIO2	5200 2044h
GPIO3	5200 3044h

Figure 4-588. GPIO0_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR2															
RW															
0															

Access Types Legend

Table 4-1235. CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR3	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR2	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

4.11.18 GPIO0_IN_DATA23 Register (Offset = 48h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1236. Instance Table

Instance Name	Physical Address
GPIO0	5200 0048h
GPIO1	5200 1048h
GPIO2	5200 2048h
GPIO3	5200 3048h

Figure 4-589. GPIO0_IN_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN2															
RO															
0															

Access Types Legend

Table 4-1237. IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN3	RO	0h	Status of GPIO bank 3 bits.
15 - 0	IN2	RO	0h	Status of GPIO bank 2 bits.

4.11.19 GPIO0_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1238. Instance Table

Instance Name	Physical Address
GPIO0	5200 004Ch
GPIO1	5200 104Ch
GPIO2	5200 204Ch
GPIO3	5200 304Ch

Figure 4-590. GPIO0_SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS2															
RW															
0															

Access Types Legend

Table 4-1239. SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS3	RW	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits.
15 - 0	SETRIS2	RW	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits.

4.11.20 GPIO0_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1240. Instance Table

Instance Name	Physical Address
GPIO0	5200 0050h
GPIO1	5200 1050h
GPIO2	5200 2050h
GPIO3	5200 3050h

Figure 4-591. GPIO0_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS2															
RW															
0															

Access Types Legend

Table 4-1241. CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS3	RW	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits.
15 - 0	CLRRIS2	RW	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits.

4.11.21 GPIO0_SET_FAL_TRIG23 Register (Offset = 54h) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1242. Instance Table

Instance Name	Physical Address
GPIO0	5200 0054h
GPIO1	5200 1054h
GPIO2	5200 2054h
GPIO3	5200 3054h

Figure 4-592. GPIO0_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL2															
RW															
0															

Access Types Legend

Table 4-1243. SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL3	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits.
15 - 0	SETFAL2	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits.

4.11.22 GPIO0_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1244. Instance Table

Instance Name	Physical Address
GPIO0	5200 0058h
GPIO1	5200 1058h
GPIO2	5200 2058h
GPIO3	5200 3058h

Figure 4-593. GPIO0_CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL2															
RW															
0															

Access Types Legend

Table 4-1245. CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL3	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits.
15 - 0	CLRFAL2	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits.

4.11.23 GPIO0_INTSTAT23 Register (Offset = 5Ch) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1246. Instance Table

Instance Name	Physical Address
GPIO0	5200 005Ch
GPIO1	5200 105Ch
GPIO2	5200 205Ch
GPIO3	5200 305Ch

Figure 4-594. GPIO0_INTSTAT23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT2															
RW															
0															

Access Types Legend

Table 4-1247. INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT3	RW	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT2	RW	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

4.11.24 GPIO0_DIR45 Register (Offset = 60h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1248. Instance Table

Instance Name	Physical Address
GPIO0	5200 0060h
GPIO1	5200 1060h
GPIO2	5200 2060h
GPIO3	5200 3060h

Figure 4-595. GPIO0_DIR45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR5															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR4															
RW															
1111111111111111															

Access Types Legend

Table 4-1249. DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR5	RW	3F28CB715 71C7h	Direction of GPIO bank 5 bits, 0 = output, 1 = input.
15 - 0	DIR4	RW	3F28CB715 71C7h	Direction of GPIO bank 4 bits, 0 = output, 1 = input.

4.11.25 GPIO0_OUT_DATA45 Register (Offset = 64h) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1250. Instance Table

Instance Name	Physical Address
GPIO0	5200 0064h
GPIO1	5200 1064h
GPIO2	5200 2064h
GPIO3	5200 3064h

Figure 4-596. GPIO0_OUT_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT4															
RW															
0															

Access Types Legend

Table 4-1251. OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT5	RW	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT4	RW	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

4.11.26 GPIO0_SET_DATA45 Register (Offset = 68h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1252. Instance Table

Instance Name	Physical Address
GPIO0	5200 0068h
GPIO1	5200 1068h
GPIO2	5200 2068h
GPIO3	5200 3068h

Figure 4-597. GPIO0_SET_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET4															
RW															
0															

Access Types Legend

Table 4-1253. SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET5	RW	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state.
15 - 0	SET4	RW	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state.

4.11.27 GPIO0_CLR_DATA45 Register (Offset = 6Ch) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1254. Instance Table

Instance Name	Physical Address
GPIO0	5200 006Ch
GPIO1	5200 106Ch
GPIO2	5200 206Ch
GPIO3	5200 306Ch

Figure 4-598. GPIO0_CLR_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR4															
RW															
0															

Access Types Legend

Table 4-1255. CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR5	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR4	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

4.11.28 GPIO0_IN_DATA45 Register (Offset = 70h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1256. Instance Table

Instance Name	Physical Address
GPIO0	5200 0070h
GPIO1	5200 1070h
GPIO2	5200 2070h
GPIO3	5200 3070h

Figure 4-599. GPIO0_IN_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN4															
RO															
0															

Access Types Legend

Table 4-1257. IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN5	RO	0h	Status of GPIO bank 5 bits.
15 - 0	IN4	RO	0h	Status of GPIO bank 4 bits.

4.11.29 GPIO0_SET_RIS_TRIG45 Register (Offset = 74h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1258. Instance Table

Instance Name	Physical Address
GPIO0	5200 0074h
GPIO1	5200 1074h
GPIO2	5200 2074h
GPIO3	5200 3074h

Figure 4-600. GPIO0_SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS4															
RW															
0															

Access Types Legend

Table 4-1259. SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS5	RW	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits.
15 - 0	SETRIS4	RW	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits.

4.11.30 GPIO0_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1260. Instance Table

Instance Name	Physical Address
GPIO0	5200 0078h
GPIO1	5200 1078h
GPIO2	5200 2078h
GPIO3	5200 3078h

Figure 4-601. GPIO0_CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS4															
RW															
0															

Access Types Legend

Table 4-1261. CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS5	RW	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits.
15 - 0	CLRRIS4	RW	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits.

4.11.31 GPIO0_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1262. Instance Table

Instance Name	Physical Address
GPIO0	5200 007Ch
GPIO1	5200 107Ch
GPIO2	5200 207Ch
GPIO3	5200 307Ch

Figure 4-602. GPIO0_SET_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL4															
RW															
0															

Access Types Legend

Table 4-1263. SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL5	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits.
15 - 0	SETFAL4	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits.

4.11.32 GPIO0_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1264. Instance Table

Instance Name	Physical Address
GPIO0	5200 0080h
GPIO1	5200 1080h
GPIO2	5200 2080h
GPIO3	5200 3080h

Figure 4-603. GPIO0_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL4															
RW															
0															

Access Types Legend

Table 4-1265. CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL5	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits.
15 - 0	CLRFAL4	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits.

4.11.33 GPIO0_INTSTAT45 Register (Offset = 84h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1266. Instance Table

Instance Name	Physical Address
GPIO0	5200 0084h
GPIO1	5200 1084h
GPIO2	5200 2084h
GPIO3	5200 3084h

Figure 4-604. GPIO0_INTSTAT45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT4															
RW															
0															

Access Types Legend

Table 4-1267. INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT5	RW	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT4	RW	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

4.11.34 GPIO0_DIR67 Register (Offset = 88h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1268. Instance Table

Instance Name	Physical Address
GPIO0	5200 0088h
GPIO1	5200 1088h
GPIO2	5200 2088h
GPIO3	5200 3088h

Figure 4-605. GPIO0_DIR67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR7															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR6															
RW															
1111111111111111															

Access Types Legend

Table 4-1269. DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR7	RW	3F28CB715 71C7h	Direction of GPIO bank 7 bits, 0 = output, 1 = input.
15 - 0	DIR6	RW	3F28CB715 71C7h	Direction of GPIO bank 6 bits, 0 = output, 1 = input.

4.11.35 GPIO0_OUT_DATA67 Register (Offset = 8Ch) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1270. Instance Table

Instance Name	Physical Address
GPIO0	5200 008Ch
GPIO1	5200 108Ch
GPIO2	5200 208Ch
GPIO3	5200 308Ch

Figure 4-606. GPIO0_OUT_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT6															
RW															
0															

Access Types Legend

Table 4-1271. OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT7	RW	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT6	RW	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

4.11.36 GPIO0_SET_DATA67 Register (Offset = 90h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1272. Instance Table

Instance Name	Physical Address
GPIO0	5200 0090h
GPIO1	5200 1090h
GPIO2	5200 2090h
GPIO3	5200 3090h

Figure 4-607. GPIO0_SET_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET6															
RW															
0															

Access Types Legend

Table 4-1273. SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET7	RW	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state.
15 - 0	SET6	RW	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state.

4.11.37 GPIO0_CLR_DATA67 Register (Offset = 94h) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1274. Instance Table

Instance Name	Physical Address
GPIO0	5200 0094h
GPIO1	5200 1094h
GPIO2	5200 2094h
GPIO3	5200 3094h

Figure 4-608. GPIO0_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR6															
RW															
0															

Access Types Legend

Table 4-1275. CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR7	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR6	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

4.11.38 GPIO0_IN_DATA67 Register (Offset = 98h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1276. Instance Table

Instance Name	Physical Address
GPIO0	5200 0098h
GPIO1	5200 1098h
GPIO2	5200 2098h
GPIO3	5200 3098h

Figure 4-609. GPIO0_IN_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN6															
RO															
0															

Access Types Legend

Table 4-1277. IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN7	RO	0h	Status of GPIO bank 7 bits.
15 - 0	IN6	RO	0h	Status of GPIO bank 6 bits.

4.11.39 GPIO0_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1278. Instance Table

Instance Name	Physical Address
GPIO0	5200 009Ch
GPIO1	5200 109Ch
GPIO2	5200 209Ch
GPIO3	5200 309Ch

Figure 4-610. GPIO0_SET_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS6															
RW															
0															

Access Types Legend

Table 4-1279. SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS7	RW	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits.
15 - 0	SETRIS6	RW	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits.

4.11.40 GPIO0_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1280. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A0h
GPIO1	5200 10A0h
GPIO2	5200 20A0h
GPIO3	5200 30A0h

Figure 4-611. GPIO0_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS6															
RW															
0															

Access Types Legend

Table 4-1281. CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS7	RW	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits.
15 - 0	CLRRIS6	RW	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits.

4.11.41 GPIO0_SET_FAL_TRIG67 Register (Offset = A4h) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1282. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A4h
GPIO1	5200 10A4h
GPIO2	5200 20A4h
GPIO3	5200 30A4h

Figure 4-612. GPIO0_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL6															
RW															
0															

Access Types Legend

Table 4-1283. SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL7	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits.
15 - 0	SETFAL6	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits.

4.11.42 GPIO0_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1284. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A8h
GPIO1	5200 10A8h
GPIO2	5200 20A8h
GPIO3	5200 30A8h

Figure 4-613. GPIO0_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL6															
RW															
0															

Access Types Legend

Table 4-1285. CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL7	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits.
15 - 0	CLRFAL6	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits.

4.11.43 GPIO0_INTSTAT67 Register (Offset = ACh) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1286. Instance Table

Instance Name	Physical Address
GPIO0	5200 00ACh
GPIO1	5200 10ACh
GPIO2	5200 20ACh
GPIO3	5200 30ACh

Figure 4-614. GPIO0_INTSTAT67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT6															
RW															
0															

Access Types Legend

Table 4-1287. INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT7	RW	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT6	RW	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

4.11.44 GPIO0_DIR8 Register (Offset = B0h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1288. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B0h
GPIO1	5200 10B0h
GPIO2	5200 20B0h
GPIO3	5200 30B0h

Figure 4-615. GPIO0_DIR8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR8															
RW															
1111111111111111															

Access Types Legend

Table 4-1289. DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	DIR8	RW	3F28CB715 71C7h	Direction of GPIO bank 8 bits, 0 = output, 1 = input.

4.11.45 GPIO0_OUT_DATA8 Register (Offset = B4h) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1290. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B4h
GPIO1	5200 10B4h
GPIO2	5200 20B4h
GPIO3	5200 30B4h

Figure 4-616. GPIO0_OUT_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT8															
RW															
0															

Access Types Legend

Table 4-1291. OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	OUT8	RW	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

4.11.46 GPIO0_SET_DATA8 Register (Offset = B8h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1292. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B8h
GPIO1	5200 10B8h
GPIO2	5200 20B8h
GPIO3	5200 30B8h

Figure 4-617. GPIO0_SET_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET8															
RW															
0															

Access Types Legend

Table 4-1293. SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	SET8	RW	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state.

4.11.47 GPIO0_CLR_DATA8 Register (Offset = BCh) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1294. Instance Table

Instance Name	Physical Address
GPIO0	5200 00BCh
GPIO1	5200 10BCh
GPIO2	5200 20BCh
GPIO3	5200 30BCh

Figure 4-618. GPIO0_CLR_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR8															
RW															
0															

Access Types Legend

Table 4-1295. CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	CLR8	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

4.11.48 GPIO0_IN_DATA8 Register (Offset = C0h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1296. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C0h
GPIO1	5200 10C0h
GPIO2	5200 20C0h
GPIO3	5200 30C0h

Figure 4-619. GPIO0_IN_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN8															
RO															
0															

Access Types Legend

Table 4-1297. IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	IN8	RO	0h	Status of GPIO bank 8 bits.

4.11.49 GPIO0_SET_RIS_TRIG8 Register (Offset = C4h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1298. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C4h
GPIO1	5200 10C4h
GPIO2	5200 20C4h
GPIO3	5200 30C4h

Figure 4-620. GPIO0_SET_RIS_TRIG8 Name Register

15	14	13	12	11	10	9	8
SETRIS8							
RW							
0							
7	6	5	4	3	2	1	0
SETRIS8							
RW							
0							

Access Types Legend

Table 4-1299. SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SETRIS8	RW	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits.

4.11.50 GPIO0_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1300. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C8h
GPIO1	5200 10C8h
GPIO2	5200 20C8h
GPIO3	5200 30C8h

Figure 4-621. GPIO0_CLR_RIS_TRIG8 Name Register

15	14	13	12	11	10	9	8
CLRRIS8							
RW							
0							
7	6	5	4	3	2	1	0
CLRRIS8							
RW							
0							

Access Types Legend

Table 4-1301. CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLRRIS8	RW	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits.

4.11.51 GPIO0_SET_FAL_TRIG8 Register (Offset = CCh) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1302. Instance Table

Instance Name	Physical Address
GPIO0	5200 00CCh
GPIO1	5200 10CCh
GPIO2	5200 20CCh
GPIO3	5200 30CCh

Figure 4-622. GPIO0_SET_FAL_TRIG8 Name Register

15	14	13	12	11	10	9	8
SETFAL8							
RW							
0							
7	6	5	4	3	2	1	0
SETFAL8							
RW							
0							

Access Types Legend

Table 4-1303. SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SETFAL8	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits.

4.11.52 GPIO0_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1304. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D0h
GPIO1	5200 10D0h
GPIO2	5200 20D0h
GPIO3	5200 30D0h

Figure 4-623. GPIO0_CLR_FAL_TRIG8 Name Register

15	14	13	12	11	10	9	8
CLRFAL8							
RW							
0							
7	6	5	4	3	2	1	0
CLRFAL8							
RW							
0							

Access Types Legend

Table 4-1305. CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLRFAL8	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits.

4.11.53 GPIO0_INTSTAT8 Register (Offset = D4h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1306. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D4h
GPIO1	5200 10D4h
GPIO2	5200 20D4h
GPIO3	5200 30D4h

Figure 4-624. GPIO0_INTSTAT8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT8															
RW															
0															

Access Types Legend

Table 4-1307. INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	STAT8	RW	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

Table 4-1308. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.12 MSS_I2C Registers

Table 4-1309. I2C0, I2C0_I2C Registers, Base Address=5250 0000H, Length=1

Offset	Length	Acronym	Register Name	I2C0 Physical Address	I2C1 Physical Address	I2C2 Physical Address
0h	32	I2C0_ICOAR	I2C Own Address register	5250 0000h	5250 1000h	5250 2000h
4h	32	I2C0_ICIMR	I2C Interrupt Mask/ Status register	5250 0004h	5250 1004h	5250 2004h
8h	32	I2C0_ICSTR	I2C Interrupt Status register	5250 0008h	5250 1008h	5250 2008h
Ch	32	I2C0_ICCLKL	I2C Clock Divider Low register	5250 000Ch	5250 100Ch	5250 200Ch
10h	32	I2C0_ICCLKH	I2C Clock Divider High register	5250 0010h	5250 1010h	5250 2010h
14h	32	I2C0_ICCNT	I2C Data Count register	5250 0014h	5250 1014h	5250 2014h
18h	32	I2C0_ICDRR	I2C Data Receive register	5250 0018h	5250 1018h	5250 2018h
1Ch	32	I2C0_ICSAR	I2C Slave Address register	5250 001Ch	5250 101Ch	5250 201Ch
20h	32	I2C0_ICDXR	I2C Data Transmit register	5250 0020h	5250 1020h	5250 2020h
24h	32	I2C0_ICMDR	I2C Mode register	5250 0024h	5250 1024h	5250 2024h
28h	32	I2C0_ICIVR	I2C Interrupt Vector register	5250 0028h	5250 1028h	5250 2028h
2Ch	32	I2C0_ICEMDR	I2C Extended Mode register	5250 002Ch	5250 102Ch	5250 202Ch
30h	32	I2C0_ICPSC	I2C Prescaler register	5250 0030h	5250 1030h	5250 2030h
34h	32	I2C0_ICPID1	I2C Peripheral ID register 1	5250 0034h	5250 1034h	5250 2034h
38h	32	I2C0_ICPID2	I2C Peripheral ID register 2	5250 0038h	5250 1038h	5250 2038h
3Ch	32	I2C0_ICDMAC	I2C DMA Control Register	5250 003Ch	5250 103Ch	5250 203Ch
40h	32	I2C0_I2C_RESERVED1	Reserved	5250 0040h	5250 1040h	5250 2040h
44h	32	I2C0_I2C_RESERVED2	Reserved	5250 0044h	5250 1044h	5250 2044h
48h	32	I2C0_ICPFUNC	I2C Pin Function register	5250 0048h	5250 1048h	5250 2048h
4Ch	32	I2C0_ICPDIR	I2C Pin Direction register	5250 004Ch	5250 104Ch	5250 204Ch
50h	32	I2C0_ICPDIN	I2C Pin Data In register	5250 0050h	5250 1050h	5250 2050h
54h	32	I2C0_ICPDOUT	I2C Pin Data Out register	5250 0054h	5250 1054h	5250 2054h
58h	32	I2C0_ICPDSET	I2C Pin Data Set register	5250 0058h	5250 1058h	5250 2058h
5Ch	32	I2C0_ICPDCLR	I2C Pin Data Clear register	5250 005Ch	5250 105Ch	5250 205Ch

Table 4-1309. I2C0, I2C0_I2C Registers, Base Address=5250 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	I2C0 Physical Address	I2C1 Physical Address	I2C2 Physical Address
60h	32	I2C0_ICPDRV	I2C Pin Driver Mode Register	5250 0060h	5250 1060h	5250 2060h

4.12.1 I2C0_ICOAR Register (Offset = 0h) [reset = h]

Short Description: I2C Own Address register

Long Description:

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Table 4-1310. Instance Table

Instance Name	Physical Address
I2C0	5250 0000h
I2C1	5250 1000h
I2C2	5250 2000h
I2C3	5250 3000h

Figure 4-625. I2C0_ICOAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						A9_A0									
RW						RW									
0						0									

Access Types Legend

Table 4-1311. ICOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Own address. Use in both 7- and 10-bit address mode. Note that usercan program the I2C own address to any value as long as it does notconflict with other components in the system.

4.12.2 I2C0_ICIMR Register (Offset = 4h) [reset = h]

Short Description: I2C Interrupt Mask/Status register

Long Description:

Return to Summary Table

Table 4-1312. Instance Table

Instance Name	Physical Address
I2C0	5250 0004h
I2C1	5250 1004h
I2C2	5250 2004h
I2C3	5250 3004h

Figure 4-626. I2C0_ICIMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									AAS	SCD	ICXRDY	ICRRDY	ARDY	NACK	AL
RW									RW	RW	RW	RW	RW	RW	RW
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-1313. ICIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU	RW	0h	Reserved
6	AAS	RW	0h	Address As Slave interrupt mask bit. Setting a"1" to this bit unmasks the Address As Slave interrupt. Setting a"0" to this bit masks the Address As Slave interrupt.
5	SCD	RW	0h	Stop Condition Detection mask bit. Setting a"1" to this bit unmasks the Stop Condition Detection interrupt. Setting a "0" to this bit masks the Stop Condition Detection interrupt.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Transmit Data Ready interrupt. Setting a"0" to this bit masks the Transmit Data Ready interrupt.
3	ICRRDY	RW	0h	Receive Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Receive Data Ready interrupt. Setting a"0" to this bit masks the Receive Data Ready interrupt.
2	ARDY	RW	0h	Register access ready interrupt mask bit. Setting a"1" to this bit unmasks the Register access ready interrupt. Setting a"0" to this bit masks the Register access ready interrupt.
1	NACK	RW	0h	No Acknowledgement interrupt mask bit. Setting a"1" to this bit unmasks the No Acknowledgement interrupt. Setting a"0" to this bit masks the No Acknowledgement interrupt.
0	AL	RW	0h	Arbitration Lost interrupt mask bit. Setting a"1" to this bit unmasks the Arbitration Lost interrupt. Setting a"0" to this bit masks the Arbitration Lost interrupt.

4.12.3 I2C0_ICSTR Register (Offset = 8h) [reset = h]

Short Description: I2C Interrupt Status register

Long Description:

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Table 4-1314. Instance Table

Instance Name	Physical Address
I2C0	5250 0008h
I2C1	5250 1008h
I2C2	5250 2008h
I2C3	5250 3008h

Figure 4-627. I2C0_ICSTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2	SDIR	NACKSNT	BB	RSFULL	XSMT	AAS	AD0	NU1		SCD	ICXRDY	ICRRDY	ARDY	NACK	AL
RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0		0	0	0	0	0	0

Access Types Legend

Table 4-1315. ICSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU2	RW	0h	Reserved
14	SDIR	RW	0h	Slave Direction. This bit is clear to '0' indicating the I2C is a master transmitter/receiver or a slave receiver. This bit is also clear by STOP condition or START condition. It is set to '1' when the I2C slave is a transmitter. In DLB mode (which the configuration should be master-transmitter slave-receiver) this bit is clear to '0'. Writing a"1" to this bit to clear it.
13	NACKSNT	RW	0h	A No Acknowledge is sent due to NACKMOD is set to a"1". NACKSNT =0: A No Acknowledge is not sent. NACKSNT =1: A No Acknowledge is sent. Writing a"1" to this bit to clear it.
12	BB	RW	0h	Bus Busy. This bit indicates the state of the serial bus. BB=0: The bus is free. BB=1: The bus is occupied. On reception of a"start" condition the device sets BB to 1. This bit is also set if the I2C detects SCL low state. BB is clear to 0 after reception of a"stop" condition. BB is kept to"0" regardless SCL state when the I2C is in reset (IRS_=0). If the IRS_ is set to"1" during transaction between other I2C devices the BB bit is set at the first falling edge of SCL or START condition. - (RW)
11	RSFULL	RW	0h	Receive shift full. This bit indicates whether the receiver has experienced overrun. Overrun occurs when the receive shift register (ICRSR) is full and ICDRR has not been read since the ICRSR-to-ICDRR transfer. The FSM is holding for ICDRR read access. RSFULL is clear when reading the ICDRR. RSFULL is set to"1" when the I2C has recognized an overrun. The contents of ICDRR are NOT lost in this case. In repeat mode since double buffer (ICRSR and ICDRR) behaves like a single buffer RSFULL is set to"1" every time the data is received. RSFULL is clear as a result of reading the ICDRR. - (RW)

Table 4-1315. ICSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	XSMT	RW	0h	Transmit shift empty not. This bit indicates whether the transmitter has experienced underflow. Underflow occurs when the transmit shift register (ICXSR) is empty and ICDXR has not been loaded. The FSM is holding for ICDXR write access. XSMT_ is cleared when underflow has occurred. XSMT_ is set to"1" as a result of writing to ICDXR. In repeat mode if the I2C in master transmitter mode is holding transfer with XSMT_=0 (i.e. waiting for further action) and the STT or STP bit is set XSMT_ is set to"1" by hardware.
9	AAS	RW	0h	Address As Slave. This bit is set to 1 by the device when it has recognized its own slave address or an address of all (8) zeros. The AAS bit is reset by stop condition or detection of any address byte that does not match ICOAR. - (RW)
8	AD0	RW	0h	Address Zero Status: This bit is set to 1 by device if it detects the address of all (8) zeros (i.e. general call). The AD0 bit is reset to 0 (default value) when a"start" or"stop" condition is detected. - (RW)
7 - 6	NU1	RW	0h	Reserved
5	SCD	RW	0h	Stop Condition Detection bit SCD is set when the I2C sends or receives STOP condition. This bit is cleared by reading ICIVR (as 110) or writing '1' to itself.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt flag bit. ICXRDY is set to"1" is generated when the transmitted data has been copied from ICDXR to the transmit-shift register (ICXSR). ICRXDY is clear to"0" when the ICDXR is written. This bit can also be polled by the CPU to write a new transmitted data into the ICDXR. Write '1' to this bit will set it and DXR Write will clear it.
3	ICRRDY	RW	0h	Receive Data Ready interrupt flag bit. ICRRDY is set to"1" when the received data has been copied from ICRSR into the ICDRR. ICRRDY is cleared to"0" when the ICDRR is read. This bit can also be polled by the CPU to read the received data in the ICDRR. Write '1' or DRR Read will clear it.
2	ARDY	RW	0h	Register-access-ready interrupt flag bit. ARDY is generated by the hardware if the I2C is in the master mode when the previously programmed data and command has been performed and status bit has been updated. This flag is used by the CPU to let it knows that the I2C registers are ready to be accessed again. When RM=0 ARDY is set when the internal data count is passed 0 if STP register bit has not been set. When RM=1 ARDY is set at each byte end. If the I2C is in FDF mode(FDF=1) ARDY is set just after Start condition. This bit is automatically cleared by hardware when writing data to ICDXR in transmit mode reading data from ICDRR in receive mode or setting STT or STP bit. Write '1' will clear it.
1	NACK	RW	0h	No-Acknowledgement interrupt flag bit. The No Acknowledge flag bit is set when the hardware in "master" mode detects no acknowledge has been received. This bit is NOT set by no-acknowledgement after Start byte Write '1' or Read the ICIVR (as 010) will clear it.
0	AL	RW	0h	Arbitration-Lost interrupt flag bit. The Arbitration Lost flag bit is set to 1 when the device in the "master" mode senses it has lost an arbitration when two or more transmitters start a transmission almost simultaneously or when the I2C attempts to start a transfer while BB (bus busy) is 1. When this is set to 1 due to arbitration lost the MST/STT/STP bits are clear the I2C becomes a slave. Write '1' or Read the ICIVR (as 001) will clear it.

4.12.4 I2C0_ICCLKL Register (Offset = Ch) [reset = h]

Short Description: I2C Clock Divider Low register

Long Description:

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Table 4-1316. Instance Table

Instance Name	Physical Address
I2C0	5250 000Ch
I2C1	5250 100Ch
I2C2	5250 200Ch
I2C3	5250 300Ch

Figure 4-628. I2C0_ICCLKL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICCL15_ICCL0															
RW															
0															

Access Types Legend

Table 4-1317. ICCLKL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCL15_ICCL0	RW	0h	Low time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL low time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

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4.12.5 I2C0_ICCLKH Register (Offset = 10h) [reset = h]

Short Description: I2C Clock Divider High register

Long Description:

Return to Summary Table

Table 4-1318. Instance Table

Instance Name	Physical Address
I2C0	5250 0010h
I2C1	5250 1010h
I2C2	5250 2010h
I2C3	5250 3010h

Figure 4-629. I2C0_ICCLKH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICCH15_ICCLH0															
RW															
0															

Access Types Legend

Table 4-1319. ICCLKH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCH15_ICCLH0	RW	0h	High time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL high time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

4.12.6 I2C0_ICCNT Register (Offset = 14h) [reset = h]

Short Description: I2C Data Count register

Long Description:

Return to Summary Table

Table 4-1320. Instance Table

Instance Name	Physical Address
I2C0	5250 0014h
I2C1	5250 1014h
I2C2	5250 2014h
I2C3	5250 3014h

Figure 4-630. I2C0_ICCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICDC15_ICDC0															
RW															
0															

Access Types Legend

Table 4-1321. ICCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICDC15_ICDC0	RW	0h	Data count. This data count register is used to generate a Stop condition if a Stop condition is specified (STP=1). . ICCNT=1 data count is 1 :: :: ICCNT=0FFFFh data count is 65535 ICCNT=0data counter is 65536 Note that ICCNT is a don"t care when RM is set to 1.

4.12.7 I2C0_ICDRR Register (Offset = 18h) [reset = h]

Short Description: I2C Data Receive register

Long Description:

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Table 4-1322. Instance Table

Instance Name	Physical Address
I2C0	5250 0018h
I2C1	5250 1018h
I2C2	5250 2018h
I2C3	5250 3018h

Figure 4-631. I2C0_ICDRR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								D7_D0							
RW								RW							
0								0							

Access Types Legend

Table 4-1323. ICDRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Receive data

4.12.8 I2C0_ICSAR Register (Offset = 1Ch) [reset = h]

Short Description: I2C Slave Address register

Long Description:

Return to Summary Table

Table 4-1324. Instance Table

Instance Name	Physical Address
I2C0	5250 001Ch
I2C1	5250 101Ch
I2C2	5250 201Ch
I2C3	5250 301Ch

Figure 4-632. I2C0_ICSAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						A9_A0									
RW						RW									
0						0									

Access Types Legend

Table 4-1325. ICSAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Slave address. Use in both 7- and 10-bit address mode.

4.12.9 I2C0_ICDXR Register (Offset = 20h) [reset = h]

Short Description: I2C Data Transmit register

Long Description:

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Table 4-1326. Instance Table

Instance Name	Physical Address
I2C0	5250 0020h
I2C1	5250 1020h
I2C2	5250 2020h
I2C3	5250 3020h

Figure 4-633. I2C0_ICDXR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								D7_D0							
RW								RW							
0								0							

Access Types Legend

Table 4-1327. ICDXR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Transmit data

4.12.10 I2C0_ICMDR Register (Offset = 24h) [reset = h]

Short Description: I2C Mode register

Long Description:

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Table 4-1328. Instance Table

Instance Name	Physical Address
I2C0	5250 0024h
I2C1	5250 1024h
I2C2	5250 2024h
I2C3	5250 3024h

Figure 4-634. I2C0_ICMDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NACK MOD	FREE	STT	NU1	STP	MST	TRX	XA	RM	DLB	IRS	STB	FDF	BC2_BC1_BC0		
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Access Types Legend

Table 4-1329. ICMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU2	RW	0h	Reserved
15	NACKMOD	RW	0h	No Acknowledge (NACK) mode. This bit is used to send an Acknowledge (ACK) or a No Acknowledge (NACK) to the transmitter. This bit is only applicable when the I2C is in receiver mode. In master receiver mode when the internal data count counter decrements to zero the I2C sends a NACK. The master receiver I2C finishes a transfer when it sends a NACK. The I2C ignores ICCNT when NACKMOD is '1'. The NACKMOD bit should be set before the rising edge of the last data bit (bit 8) if a NACK must be sent and this bit is cleared once a NACK has been sent. NACKMOD=0 the I2C sends an ACK to the transmitter during the acknowledge cycle. NACKMOD=1 the I2C sends a NACK to the transmitter during the acknowledge cycle.
14	FREE	RW	0h	Free Running. This bit is used to determine the state of the I2C when a breakpoint is encountered in the HLL debugger. FREE=0: (default) Stops immediately if SCL is low and keep driving SCL low whether I2C is master transmitter/receiver. If SCL is high I2C waits until SCL becomes low and then stops. If the I2C is a slave it will stop when the transmission/receiving completes. FREE=1: The I2C runs free.

Table 4-1329. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	STT	RW	0h	Start Condition (Master only mode). This bit can be set to a"1" by the CPU to generate a Start condition. In master mode when setting Start to"1" generates a Start condition. It is reset to "0" by the hardware after the Start condition has been generated. The Start/ Stop bits can be configured to generate different transfer formats. Note that the STT and STP can be used to terminate the repeat mode. ST T___STP____Conditions_____Bus Activities _1_____0_____Start_____S-A-D _0_____1_____Stop_____P _1_____1_____Start-Stop (ICCNT= n)_____S-A-D..(n)..D-P _1_____0_____Start (ICCNT= n)_____S-A-D..(n)..D
12	NU1	RW	0h	Reserved for IDLEEN (IDLE Enable on 5509). - (RW)
11	STP	RW	0h	Stop Condition (Master mode only). This bit can be set to a"1" by the CPU to generate a Stop condition. It is reset to "0" by the hardware after the Stop condition has been generated. The Stop condition is generated when ICCNT passes 0 when the I2C is in non-repeat mode(RM=0).
10	MST	RW	0h	Master. MST=0: The I 2 C peripheral is in the"slave" mode and clock is received from the"master" device. MST=1: The I 2 C peripheral is in the"master" mode and it generates the clock. This bit is clear when the transfer completed.
9	TRX	RW	0h	Transmitter. TRX=0: The I 2 C is in the"receiver" mode and data on data line SDA is shifted into the data register ICDRR. TRX=1: The I 2 C is in the"transmitter" mode and the data in ICDXR is shifted out on data line SDA. The operating modes (not in FDF mode) are defined as follows. In FDF mode TRX must be configured even if the I2C is in slave mode because there is no address/direction byte in FDF mode. MST___TRX___Operating Modes _0_____x_____"slave receiver" _0_____x_____"slave transmitter" _1_____0_____"master receiver" _1_____1_____"master transmitter"
8	XA	RW	0h	Expanded Address. XA=0: (default) 7-bit address mode (normal address mode). XA=1: 10-bit address mode (expanded address mode) Please note that XA needs to be configured even if the I2C is in slave mode.
7	RM	RW	0h	Repeat Mode. This bit is set to a"1" by the CPU to put the I2C in the repeat mode. In this mode data is continuously transmitted out of the ICDXR until the STP bit is set to"1" regardless of ICCNT value. This bit is don"t care if the I2C is configured in slave mode. __RM___STT___STP___Conditions_____Bus Activities_____Mode _0_____0_____0_____Idle_____None_____NA _0_____0_____1_____Stop_____P_____NA _0_____1_____0_____(Re)Start_____S-A-D..(n)..D____Repeat n _0_____1_____1_____(Re)Start-Stop___S-A-D..(n)..D-P__Repeat n _1_____0_____0_____Idle_____none_____NA _1_____0_____1_____Stop_____P _____NA _1_____1_____0_____(Re)Start_____S-A-D-D-D..____Continuous _1_____1_____1_____Reserved_____None_____NA
6	DLB	RW	0h	Digital Loop Back (in master transmit mode only). This bit is set to a"1" by the CPU to put the I2C in the loop back mode. In this mode data transmitted out of the ICDXR will be received in the ICDRR after ((CPU freq/I2C freq)8) CPU cycles via an internal path. The address of the ICOAR is output on SDA.

Table 4-1329. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	IRS	RW	0h	I2C Reset Not. This can be set to a"0" by the CPU to put the I2C in reset or to a"1" to take the I2C out of reset. When this bit is reset to 0 all status bits in ICSTR and ICIVR are set to default values. Note that if this bit is reset during a transfer it can cause the I2C bus hang (SDA and SCL are tri-stated).
4	STB	RW	0h	Start Byte (Master only mode). The Start Byte mode bit is set to 1 by the CPU to configure the I2C in Start byte mode the I2C sends "00000001"? regardless ICSAR value. Refer to the Philip I2C spec for more details.
3	FDF	RW	0h	Free Data Format. This bit can be set to"1" by the CPU to configure the I2C in Free Data Format mode. FDF___MST___TRX_____Operating mode _0_____0_____ x____Slave in non FDF mode _0_____1_____0____Master receive in non FDF mode _0_____1_____1____Master transmit in non FDF mode _1_____0_____0____Slave receiver in FDF mode _1_____0_____1____Slave transmitter in FDF mode _1_____1_____0____Master receiver in FDF mode _1_____1_____1____Master transmitter in FDF mode
2 - 0	BC2_BC1_BC0	RW	0h	Bit Count : Bit Count 2, Bit Count 1 and Bit Count 0 define the number of bits starting from the lsb (excluding the acknowledge bit) of the next byte which are yet to be received or transmitted. BC2_BC1_BC0 __Bits/byte in FDF__Bits/byte w/ ACK _0___0___1_____NA (reserved)____ NA (reserved) _0___1___0_____2_____3_____ _0___1___1_____3_____4_____ _1___0___0_____4_____5_____ _1___0___1_____5_____6_____ _1___1___0_____6_____7_____ _1___1___1_____7_____8_____ _0___0___0_____8_____9_____

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4.12.11 I2C0_ICIVR Register (Offset = 28h) [reset = h]

Short Description: I2C Interrupt Vector register

Long Description:

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Table 4-1330. Instance Table

Instance Name	Physical Address
I2C0	5250 0028h
I2C1	5250 1028h
I2C2	5250 2028h
I2C3	5250 3028h

Figure 4-635. I2C0_ICIVR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2				TESTMD				NU1					INTCODE		
RW				RW				RW					RW		
0				0				0					0		

Access Types Legend

Table 4-1331. ICIVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RW	0h	Reserved.
11 - 8	TESTMD	RW	0h	Reserved for internal testing.
7 - 3	NU1	RW	0h	Reserved.
2 - 0	INTCODE	RW	0h	Interrupt code. The binary-coded-interrupt vector indicates which interrupt has occurred. Reading the ICIVR clears the interrupt code except ARDY(011) RRDY(100) and XRDY(101). Interrupt code for ARDY RRDY and XRDY is cleared when ARDY ICRRDY and ICXRDY bits in the ICSTR is cleared to default value respectively. If other interrupts are pending a new interrupt is generated. If there are more than one interrupt flag reading the ICIVR clears the highest priority interrupt code. Reading the ICIVR also clears corresponding status bit in the ICSTR except ARDY ICRRDY ICXRDY and AAS. Note that users must read (clear) the ICIVR before doing another start otherwise the ICIVR could contain incorrect (old interrupt flags) value. Interrupt Code Interrupt Occurred 000_(default) None _001_(highest priority) Arbitration Lost interrupt _010 No Acknowledgement interrupt _011 Register Access Ready interrupt _100 Receive Data Ready interrupt _101 Transmit Data Ready interrupt _110 Stop Condition Detection _111_(lowest priority) Address As Slave - (RW)

4.12.12 I2C0_ICEMDR Register (Offset = 2Ch) [reset = h]

Short Description: I2C Extended Mode register

Long Description:

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Table 4-1332. Instance Table

Instance Name	Physical Address
I2C0	5250 002Ch
I2C1	5250 102Ch
I2C2	5250 202Ch
I2C3	5250 302Ch

Figure 4-636. I2C0_ICEMDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														IGNACK	BCM
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1333. ICEMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	IGNACK	RW	0h	Ignore NACK mode IGNACK=0 The master transmitter will operate normally discontinue the data transfer and set the ARDY and NACK status bits when a NACK signal is received from the slave. IGNACK=1 The master transmitter will ignore a NACK received from the slave.
0	BCM	RW	0h	Backward Compatibility Mode. This bit affects the I2C interrupt behavior. Refer to appendix A for details.

4.12.13 I2C0_ICPSC Register (Offset = 30h) [reset = h]

Short Description: I2C Prescaler register

Long Description:

Return to Summary Table

Table 4-1334. Instance Table

Instance Name	Physical Address
I2C0	5250 0030h
I2C1	5250 1030h
I2C2	5250 2030h
I2C3	5250 3030h

Figure 4-637. I2C0_ICPSC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								IPSC7_IPSC0							
RW								RW							
0								0							

Access Types Legend

Table 4-1335. ICPSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	IPSC7_IPSC0	RW	0h	8-bit prescaler to divide the system clock down to 4/8/12Mhz clock and used by the I2C module. This register must be initialized while the I2C is still in reset (IRS_=0). The value takes effect on the rising edge of IRS_.

4.12.14 I2C0_ICPID1 Register (Offset = 34h) [reset = h]

Short Description: I2C Peripheral ID register 1

Long Description:

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Table 4-1336. Instance Table

Instance Name	Physical Address
I2C0	5250 0034h
I2C1	5250 1034h
I2C2	5250 2034h
I2C3	5250 3034h

Figure 4-638. I2C0_ICPID1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLASS								REVISION							
RW								RW							
0								0							

Access Types Legend

Table 4-1337. ICPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved.
15 - 8	CLASS	RW	0h	Identifies the class of peripheral. This value should be 0x01 - (RW)
7 - 0	REVISION	RW	0h	Identifies the revision level of the I2C. This value should be incremented each time the design is revised. - (RW)

4.12.15 I2C0_ICPID2 Register (Offset = 38h) [reset = h]

Short Description: I2C Peripheral ID register 2

Long Description:

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Table 4-1338. Instance Table

Instance Name	Physical Address
I2C0	5250 0038h
I2C1	5250 1038h
I2C2	5250 2038h
I2C3	5250 3038h

Figure 4-639. I2C0_ICPID2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								TYPE							
RW								RW							
0								0							

Access Types Legend

Table 4-1339. ICPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	TYPE	RW	0h	Identifies the type of peripheral. This value should be 0x05 - (RW)

4.12.16 I2C0_ICDMAC Register (Offset = 3Ch) [reset = h]

Short Description: I2C DMA Control Register

Long Description:

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Table 4-1340. Instance Table

Instance Name	Physical Address
I2C0	5250 003Ch
I2C1	5250 103Ch
I2C2	5250 203Ch
I2C3	5250 303Ch

Figure 4-640. I2C0_ICDMAC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														TXDMAEN	RXDMAEN
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1341. ICDMAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	TXDMAEN	RW	0h	Transmit DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICTEVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICTEVT_POR pin is never asserted. RXDMAEN=0: DMA transmit event is disabled. RXDMAEN=1: DMA transmit event is enabled. (Default)
0	RXDMAEN	RW	0h	Receive DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICREVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICREVT_POR pin is never asserted. RXDMAEN=0: DMA receive event is disabled. RXDMAEN=1: DMA receive event is enabled. (Default)

4.12.17 I2C0_I2C_RESERVED1 Register (Offset = 40h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-1342. Instance Table

Instance Name	Physical Address
I2C0	5250 0040h
I2C1	5250 1040h
I2C2	5250 2040h
I2C3	5250 3040h

Figure 4-641. I2C0_I2C_RESERVED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU															
RW															
0															

Access Types Legend

Table 4-1343. I2C_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

4.12.18 I2C0_I2C_RESERVED2 Register (Offset = 44h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-1344. Instance Table

Instance Name	Physical Address
I2C0	5250 0044h
I2C1	5250 1044h
I2C2	5250 2044h
I2C3	5250 3044h

Figure 4-642. I2C0_I2C_RESERVED2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU															
RW															
0															

Access Types Legend

Table 4-1345. I2C_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

4.12.19 I2C0_ICPFUNC Register (Offset = 48h) [reset = h]

Short Description: I2C Pin Function register

Long Description:

Return to Summary Table

Table 4-1346. Instance Table

Instance Name	Physical Address
I2C0	5250 0048h
I2C1	5250 1048h
I2C2	5250 2048h
I2C3	5250 3048h

Figure 4-643. I2C0_ICPFUNC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU															PFUNC0
RW															RW
0															0

Access Types Legend

Table 4-1347. ICPFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU	RW	0h	Reserved.
0	PFUNC0	RW	0h	Controls the function of the I2C SCL and SDA pins. 0 = Pins function as SCL and SDA 1 = Pins functions as GPIO Note: No hardware protection is required to disable I2C function when the PFUNC[0] and IRS_ bits are both set to one. When PFUNC[0] is"1" (GPIO mode) the sub-module which controls the I2C function receives the value"1" for SCL and SDA. IRS_ can be set to"1" regardless of PFUNC[0] and the I2C function works whenever the IRS_ bit is"1". The user is expected to hold I2C in reset via IRS_ bit when changing to/from GPIO mode via the PFUNC[0] bit.

4.12.20 I2C0_ICPDIR Register (Offset = 4Ch) [reset = h]

Short Description: I2C Pin Direction register

Long Description:

Return to Summary Table

Table 4-1348. Instance Table

Instance Name	Physical Address
I2C0	5250 004Ch
I2C1	5250 104Ch
I2C2	5250 204Ch
I2C3	5250 304Ch

Figure 4-644. I2C0_ICPDIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDIR1	PDIR0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1349. ICPDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIR1	RW	0h	Controls the direction of the I2C SDA pin when configured as GPIO. 0 = SDA pin functions as input 1 = SDA pin functions as output
0	PDIR0	RW	0h	Controls the direction of the I2C SCL pin when configured as GPIO. 0 = SCL pin functions as input 1 = SCL pin functions as output

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4.12.21 I2C0_ICPDIN Register (Offset = 50h) [reset = h]

Short Description: I2C Pin Data In register

Long Description:

Return to Summary Table

Table 4-1350. Instance Table

Instance Name	Physical Address
I2C0	5250 0050h
I2C1	5250 1050h
I2C2	5250 2050h
I2C3	5250 3050h

Figure 4-645. I2C0_ICPDIN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDIN1	PDIN0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1351. ICPDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIN1	RW	0h	Indicates the logic level present on the SDA pin. Reads: 0 = Logic low present at SDA pin regardless of PFUNC setting. 1 = Logic high present at SDA pin regardless of PFUNC setting. Writes: Writes have no effect. - (RW)
0	PDIN0	RW	0h	Indicates the logic level present on the SCL pin. Reads: 0 = Logic low present at SCL pin regardless of PFUNC setting. 1 = Logic high present at SCL pin regardless of PFUNC setting. Writes: Writes have no effect - (RW)

4.12.22 I2C0_ICPDOUT Register (Offset = 54h) [reset = h]

Short Description: I2C Pin Data Out register

Long Description:

Return to Summary Table

Table 4-1352. Instance Table

Instance Name	Physical Address
I2C0	5250 0054h
I2C1	5250 1054h
I2C2	5250 2054h
I2C3	5250 3054h

Figure 4-646. I2C0_ICPDOUT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDOUT1	PDOUT0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1353. ICPDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDOUT1	RW	0h	Controls the level driven on the SDA pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SDA pin driven low 1 = SDA pin driven high. Note: If SDA is connected to an open-drain buffer at the chiplevel the I2C cannot drive SDA to high.
0	PDOUT0	RW	0h	Controls the level driven on the SCL pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SCL pin driven low 1 = SCL pin driven high Note: If SCL is connected to an open-drain buffer at the chiplevel the I2C cannot drive SCL to high.

4.12.23 I2C0_ICPDSET Register (Offset = 58h) [reset = h]

Short Description: I2C Pin Data Set register

Long Description:

Return to Summary Table

Table 4-1354. Instance Table

Instance Name	Physical Address
I2C0	5250 0058h
I2C1	5250 1058h
I2C2	5250 2058h
I2C3	5250 3058h

Figure 4-647. I2C0_ICPDSET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDSET1	PDSET0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1355. ICPDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDSET1	RW	0h	Used to set PDOUT[1] bit which corresponds to the SDA GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is set to logic high.
0	PDSET0	RW	0h	Used to set PDOUT[0] bit which corresponds to the SCL GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is set to logic high.

4.12.24 I2C0_ICPDCLR Register (Offset = 5Ch) [reset = h]

Short Description: I2C Pin Data Clear register

Long Description:

Return to Summary Table

Table 4-1356. Instance Table

Instance Name	Physical Address
I2C0	5250 005Ch
I2C1	5250 105Ch
I2C2	5250 205Ch
I2C3	5250 305Ch

Figure 4-648. I2C0_ICPDCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDCLR1	PDCLR0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1357. ICPDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDCLR1	RW	0h	Used to clear PDOUT[1] bit which corresponds to the SDA pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is cleared to logic low.
0	PDCLR0	RW	0h	Used to clear PDOUT[0] bit which corresponds to the SCL pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is cleared to logic low.

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4.12.25 I2C0_ICPDRV Register (Offset = 60h) [reset = h]

Short Description: I2C Pin Driver Mode Register

Long Description:

Return to Summary Table

Table 4-1358. Instance Table

Instance Name	Physical Address
I2C0	5250 0060h
I2C1	5250 1060h
I2C2	5250 2060h
I2C3	5250 3060h

Figure 4-649. I2C0_ICPDRV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														PDRV1	PDRV0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-1359. ICPDRV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDRV1	RW	0h	Used to select driver mode of output buffer for SDA pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SDA_POR port. Actual function depends on I/O buffer and chip implementation.
0	PDRV0	RW	0h	Used to select driver mode of output buffer for SCL pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SCL_POR port. Actual function depends on I/O buffer and chip implementation.

Table 4-1360. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.13 MSS_L2 Registers

Table 4-1361. L2OCRAM, L2OCRAM_L2OCRAM Registers, Base Address=7000 0000H, Length=2

Offset	Length	Acronym	Register Name	L2OCRAM Physical Address
0h	32	L2OCRAM_START	RW	7000 0000h
1FFFFCh	32	L2OCRAM_END	RW	701F FFFCh

4.13.1 L2OCRAM_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-1362. Instance Table

Instance Name	Physical Address
L2OCRAM	7000 0000h

Figure 4-650. L2OCRAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1363. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	L2 Memory start address

4.13.2 L2OCRAM_END Register (Offset = 1FFFFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1364. Instance Table

Instance Name	Physical Address
L2OCRAM	701F FFFCh

Figure 4-651. L2OCRAM_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-1365. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	L2 Memory end address

Table 4-1366. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.14 MSS_LIN Registers

Table 4-1367. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2

Offset	Length	Acronym	Register Name	LIN0 Physical Address	LIN1 Physical Address	LIN2 Physical Address
0h	32	LIN0_SCIGCR0	The SCIGCR0 register defines the module reset.	5240 0000h	5240 1000h	5240 2000h
4h	32	LIN0_SCIGCR1	The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.	5240 0004h	5240 1004h	5240 2004h
8h	32	LIN0_SCIGCR2	The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.	5240 0008h	5240 1008h	5240 2008h
Ch	32	LIN0_SCISETINT	The SCISETINT register is used to enable the various interrupts available in the LIN module.	5240 000Ch	5240 100Ch	5240 200Ch
10h	32	LIN0_SCICLEARINT	The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.	5240 0010h	5240 1010h	5240 2010h
14h	32	LIN0_SCISETINTLVL	The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.	5240 0014h	5240 1014h	5240 2014h
18h	32	LIN0_SCICLEARINTLVL	The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.	5240 0018h	5240 1018h	5240 2018h
1Ch	32	LIN0_SCIFLR	The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.	5240 001Ch	5240 101Ch	5240 201Ch
20h	32	LIN0_SCIINTVECT0	The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.	5240 0020h	5240 1020h	5240 2020h
24h	32	LIN0_SCIINTVECT1	The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.	5240 0024h	5240 1024h	5240 2024h

Table 4-1367. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	LIN0 Physical Address	LIN1 Physical Address	LIN2 Physical Address
28h	32	LIN0_SCIFORMAT	The SCIFORMAT register is used to set up the character and frame lengths.	5240 0028h	5240 1028h	5240 2028h
2Ch	32	LIN0_BRSR	The BRSR register is used to configure the baud rate of the LIN module.	5240 002Ch	5240 102Ch	5240 202Ch
30h	32	LIN0_SCIED	The SCIED register is a duplicate copy of SCIRD register that has no affect on the RXRDY flag for use with an emulator.	5240 0030h	5240 1030h	5240 2030h
34h	32	LIN0_SCIRD	The SCIRD register is where received data is stored and can be read from.	5240 0034h	5240 1034h	5240 2034h
38h	32	LIN0_SCITD	The SCITD register is where data to be transmitted is written to by application software.	5240 0038h	5240 1038h	5240 2038h
3Ch	32	LIN0_SCIPIO0	The SCIPIO0 register is used to enable the LINTX and LINRX pins.	5240 003Ch	5240 103Ch	5240 203Ch
40h	32	LIN0_SCIPIO1	Pin control Register 1	5240 0040h	5240 1040h	5240 2040h
44h	32	LIN0_SCIPIO2	The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.	5240 0044h	5240 1044h	5240 2044h
48h	32	LIN0_SCIPIO3	Pin control Register 3	5240 0048h	5240 1048h	5240 2048h
4Ch	32	LIN0_SCIPIO4	Pin control Register 4	5240 004Ch	5240 104Ch	5240 204Ch
50h	32	LIN0_SCIPIO5	Pin control Register 5	5240 0050h	5240 1050h	5240 2050h
54h	32	LIN0_SCIPIO6	Pin control Register 6	5240 0054h	5240 1054h	5240 2054h
58h	32	LIN0_SCIPIO7	Pin control Register 7	5240 0058h	5240 1058h	5240 2058h
5Ch	32	LIN0_SCIPIO8	Pin control Register 8	5240 005Ch	5240 105Ch	5240 205Ch
60h	32	LIN0_LINCOMP	The LINCOMPARE register is used to configure the sync delimeter and sync break extension.	5240 0060h	5240 1060h	5240 2060h
64h	32	LIN0_LINRD0	The LINRD0 register contains the lower 4 bytes of the received LIN frame data.	5240 0064h	5240 1064h	5240 2064h
68h	32	LIN0_LINRD1	The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.	5240 0068h	5240 1068h	5240 2068h
6Ch	32	LIN0_LINMASK	The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.	5240 006Ch	5240 106Ch	5240 206Ch

Table 4-1367. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	LIN0 Physical Address	LIN1 Physical Address	LIN2 Physical Address
70h	32	LIN0_LINID	The LINID register contains the identification fields for LIN communication. [[br]]NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.	5240 0070h	5240 1070h	5240 2070h
74h	32	LIN0_LINTD0	The LINTD0 register contains the lower 4 bytes of the data to be transmitted. [[br]]NOTE: TD	5240 0074h	5240 1074h	5240 2074h
78h	32	LIN0_LINTD1	The LINTD1 register contains the upper 4 bytes of the data to be transmitted. [[br]]NOTE: TD	5240 0078h	5240 1078h	5240 2078h
7Ch	32	LIN0_MBRSR	The MBRSR register is used to configure the expected maximum baud rate of the LIN network.	5240 007Ch	5240 107Ch	5240 207Ch
80h	32	LIN0_RESERVED_1	RW	5240 0080h	5240 1080h	5240 2080h
90h	32	LIN0_IODFTCTRL	The IODFTCTRL register is used to emulate various error and test conditions.	5240 0090h	5240 1090h	5240 2090h
94h	32	LIN0_RESERVED_2	RW	5240 0094h	5240 1094h	5240 2094h
E0h	32	LIN0_LIN_GLB_INT_EN	The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.	5240 00E0h	5240 10E0h	5240 20E0h

Table 4-1368. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2

Offset	Length	Acronym	Register Name	LIN3 Physical Address	LIN4 Physical Address
0h	32	LIN0_SCIGCR0	The SCIGCR0 register defines the module reset.	5240 3000h	5240 4000h
4h	32	LIN0_SCIGCR1	The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.	5240 3004h	5240 4004h
8h	32	LIN0_SCIGCR2	The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.	5240 3008h	5240 4008h

Table 4-1368. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	LIN3 Physical Address	LIN4 Physical Address
Ch	32	LIN0_SCISETINT	The SCISETINT register is used to enable the various interrupts available in the LIN module.	5240 300Ch	5240 400Ch
10h	32	LIN0_SCICLEARINT	The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.	5240 3010h	5240 4010h
14h	32	LIN0_SCISETINTLVL	The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.	5240 3014h	5240 4014h
18h	32	LIN0_SCICLEARINTLVL	The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.	5240 3018h	5240 4018h
1Ch	32	LIN0_SCIFLR	The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.	5240 301Ch	5240 401Ch
20h	32	LIN0_SCIINTVECT0	The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.	5240 3020h	5240 4020h
24h	32	LIN0_SCIINTVECT1	The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.	5240 3024h	5240 4024h
28h	32	LIN0_SCIFORMAT	The SCIFORMAT register is used to set up the character and frame lengths.	5240 3028h	5240 4028h
2Ch	32	LIN0_BRSR	The BRSR register is used to configure the baud rate of the LIN module.	5240 302Ch	5240 402Ch
30h	32	LIN0_SCIED	The SCIED register is a duplicate copy of SCIRD register that has no affect on the RXRDY flag for use with an emulator.	5240 3030h	5240 4030h
34h	32	LIN0_SCIRD	The SCIRD register is where received data is stored and can be read from.	5240 3034h	5240 4034h
38h	32	LIN0_SCITD	The SCITD register is where data to be transmitted is written to by application software.	5240 3038h	5240 4038h
3Ch	32	LIN0_SCIPIO0	The SCIPIO0 register is used to enable the LINTX and LINRX pins.	5240 303Ch	5240 403Ch
40h	32	LIN0_SCIPIO1	Pin control Register 1	5240 3040h	5240 4040h
44h	32	LIN0_SCIPIO2	The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.	5240 3044h	5240 4044h
48h	32	LIN0_SCIPIO3	Pin control Register 3	5240 3048h	5240 4048h
4Ch	32	LIN0_SCIPIO4	Pin control Register 4	5240 304Ch	5240 404Ch
50h	32	LIN0_SCIPIO5	Pin control Register 5	5240 3050h	5240 4050h
54h	32	LIN0_SCIPIO6	Pin control Register 6	5240 3054h	5240 4054h

Table 4-1368. LIN0, LIN0_LIN Registers, Base Address=5240 0000H, Length=2 (continued)

Offset	Length	Acronym	Register Name	LIN3 Physical Address	LIN4 Physical Address
58h	32	LIN0_SCIPIO7	Pin control Register 7	5240 3058h	5240 4058h
5Ch	32	LIN0_SCIPIO8	Pin control Register 8	5240 305Ch	5240 405Ch
60h	32	LIN0_LINCOMP	The LINCOMPARE register is used to configure the sync delimeter and sync break extension.	5240 3060h	5240 4060h
64h	32	LIN0_LINRD0	The LINRD0 register contains the lower 4 bytes of the received LIN frame data.	5240 3064h	5240 4064h
68h	32	LIN0_LINRD1	The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.	5240 3068h	5240 4068h
6Ch	32	LIN0_LINMASK	The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.	5240 306Ch	5240 406Ch
70h	32	LIN0_LINID	The LINID register contains the identification fields for LIN communication. [[br]]NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.	5240 3070h	5240 4070h
74h	32	LIN0_LINTD0	The LINTD0 register contains the lower 4 bytes of the data to be transmitted.[[br]]NOTE: TD	5240 3074h	5240 4074h
78h	32	LIN0_LINTD1	The LINTD1 register contains the upper 4 bytes of the data to be transmitted.[[br]]NOTE: TD	5240 3078h	5240 4078h
7Ch	32	LIN0_MBRSR	The MBRSR register is used to configure the expected maximum baud rate of the LIN network.	5240 307Ch	5240 407Ch
80h	32	LIN0_RESERVED_1	RW	5240 3080h	5240 4080h
90h	32	LIN0_IODFTCTRL	The IODFTCTRL register is used to emulate various error and test conditions.	5240 3090h	5240 4090h
94h	32	LIN0_RESERVED_2	RW	5240 3094h	5240 4094h
E0h	32	LIN0_LIN_GLB_INT_EN	The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.	5240 30E0h	5240 40E0h

4.14.1 LIN0_SCIGCR0 Register (Offset = 0h) [reset = h]

Short Description: The SCIGCR0 register defines the module reset.

Long Description:

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Table 4-1369. Instance Table

Instance Name	Physical Address
LIN0	5240 0000h
LIN1	5240 1000h
LIN2	5240 2000h
LIN3	5240 3000h
LIN4	5240 4000h

Figure 4-652. LIN0_SCIGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1															RESET
RO															RW
0															0

Access Types Legend

Table 4-1370. SCIGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 1	RESERVED_1	RO	0h	Reserved
0	RESET	RW	0h	This bit resets the SCI/LIN module. [[br]]This bit is effective in LIN or SCI-compatible mode.. This bit affects the reset state of the SCI/LIN module. 0 | RESET_ONSCI/LIN module is in held in reset. 1 | RESET_OFFSCI/LIN module is out of reset.

4.14.2 LIN0_SCIGCR1 Register (Offset = 4h) [reset = h]

Short Description: The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.

Long Description:

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Table 4-1371. Instance Table

Instance Name	Physical Address
LIN0	5240 0004h
LIN1	5240 1004h
LIN2	5240 2004h
LIN3	5240 3004h
LIN4	5240 4004h

Figure 4-653. LIN0_SCIGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3						TXENA	RXENA	RESERVED_2						CONT	LOOPBACK
RO						RW	RW	RO						RW	RW
0						0	0	0						0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1		STOPEXTFRAME	HGENCTRL	CTYPE	MBUFMODE	ADAPT	SLEEP	SWNRST	LINMODE	CLK_MASTER	STOP	PARITY	PARITYENA	TIMINGMODE	COMMMODE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1372. SCIGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RESERVED_3	RO	0h	Reserved
25	TXENA	RW	0h	Transmit enable.[[br]]This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy (with y=0, 1,...7) buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set.[[br]] [[br]]Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not[[br]]transmitted. If TXENA is cleared while transmission is ongoing, the data previously[[br]]written to SCITD is sent (including the checksum byte in LIN mode). 0 | TXENA_DISABLEDisable transfers from SCITD or TDy to SCITXSHF 1 | TXENA_ENABLEEnable transfers of data from SCITD or TDy to SCITXSHF

Table 4-1372. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	RXENA	RW	0h	Receive enable.[[br]]This bit is effective in LIN or SCI-compatible mode. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers.[[br]] [[br]]Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags (see Table 7) from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA.[[br]] [[br]]Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer.[[br]] [[br]]Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flagscorrectly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame 0 | RXENA_SUSPENDPrevents the receiver from transferring data from the shift buffer to the receive buffer or multi-buffers 1 | RXENA_RUNAllows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers
23 - 18	RESERVED_2	RO	0h	Reserved
17	CONT	RW	0h	Continue on suspend.[[br]]This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/LIN operates when the program is suspended. This bit affects the LIN counters. When this bit is set, the counters are not stopped during debug. When this bit is cleared, the counters are stopped during debug. 0 | CONT_SUSPENDWhen debug mode is entered, the SCI/LIN state machine is frozen. Transmissions and LIN counters are halted and resume when debug mode is exited. 1 | CONT_RUNWhen debug mode is entered, the SCI/LIN continues to operate until the current transmit and receive functions are complete.
16	LOOPBACK	RW	0h	Loopback bit.[[br]]This bit is effective in LIN or SCI-compatible mode. The self-checking option for the SCI/LIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/LIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/LIN is transmitting or receiving data, errors may result. 0 | LOOPBACK_DISABLELoopback mode is disabled. 1 | LOOPBACK_ENABLELoopback mode is enabled.
15 - 14	RESERVED_1	RO	0h	Reserved
13	STOPEXTFRAME	RW	0h	Stop extended frame communication.[[br]]This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically. 0 | STOPEXTFRAME_NO_EFFECTNo effect 1 | STOPEXTFRAME_EFFECTExtended frame communication will be stopped, once current frame transmission/reception is completed.
12	HGENCTRL	RW	0h	HGEN control bit.[[br]]This bit is effective in LIN mode only. This bit controls the type of mask filtering comparison. 0 | HGENCTRL_IDBYTEID filtering using ID-Byte. [[br]]RECEIVEDID and IDBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in NO match. 1 | HGENCTRL_IDSLAVEID filtering using ID-SlaveTask byte (Recommended). [[br]]RECEIVEDID and IDSLAVETASKBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in ALWAYS match

Table 4-1372. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CTYPE	RW	0h	Checksum type.[[br]]This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced. 0 | CTYPE_CLASSICClassic checksum is used. [[br]]This checksum is compatible with LIN 1.3 slave nodes. The classic checksum contains the modulo-256 sum with carry over all data bytes. Frames sent with Identifier 60 (0x3C) to 63 (0x3F) must allways use the classic checksum. 1 | CTYPE_ENHANCEDEnhanced checksum is used. [[br]]The enhanced checksum is compatible with LIN 2.0 and newer slave nodes. The enhanced checksum contains the modulo-256 sum with carry over all data bytes AND the protected Identifier.
10	MBUFMODE	RW	0h	Multibuffer mode.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit controls receive/transmit buffer usage, that is, whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used. 0 | MBUFMODE_DISABLEDThe multi-buffer mode is disabled. 1 | MBUFMODE_ENABLEDThe multi-buffer mode is enabled.
9	ADAPT	RW	0h	Adapt mode enable.[[br]]This mode is effective in LIN mode only. This bit has an effect during the detection of the Sync Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a LIN slave node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register.[[br]] [[br]]This field is writable in LIN mode only. 0 | ADAPT_DISABLEAutomatic baudrate adjustment is disabled. 1 | ADAPT_ENABLEAutomatic baudrate adjustment is enabled.
8	SLEEP	RW	0h	SCI sleep.[[br]]SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode.[[br]] [[br]]The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected.[[br]] [[br]]This field is writable in SCI mode only. 0 | SLEEP_DISABLESleep mode is disabled. 1 | SLEEP_ENABLESleep mode is enabled.
7	SWNRST	RW	0h	Software reset (active low).[[br]]This bit is effective in LIN or SCI-compatible mode. The SCI/LIN should only be configured while SWnRST = 0.[[br]] [[br]]Only the following configuration bits can be changed in runtime (i.e.,[[br]]while SWnRESET = 1):[[br]]- STOP EXT Frame (SCIGCR1[13])[[br]]- CC bit (SCIGCR2[17])[[br]]- SC bit (SCIGCR2[16]) 0 | SWNRST_RESETThe SCI/LIN is in its reset state; no data will be transmitted or received. Writing a 0 to this bit intializes the SCI/LIN state machines and operating flags. All affected logic is held in the reset state until a 1 is written to this bit. 1 | SWNRST_READYThe SCI/LIN is in its ready state; transmission and reception can occur. After this bit is set to 1, the configuration of the module should not change.
6	LINMODE	RW	0h	LIN mode[[br]]This bit controls the mode of operation of the module. 0 | LINMODE_DISABLELIN mode is disabled; SCI compatibility mode is enabled. 1 | LINMODE_ENABLELIN mode is enabled; SCI compatibility mode is disabled.

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Table 4-1372. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_MASTER	RW	0h	SCI internal clock enable or LIN Master/Slave configuration.[[br]]In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a slave or master. 0 | CLK_MASTER_OFFSCI-compatible mode: Reserved.[[br]]LIN mode: The module is in slave mode. 1 | CLK_MASTER_ONSCI-compatible mode: Enable clock to the SCI module.[[br]]LIN mode: The node is in master mode.
4	STOP	RW	0h	SCI number of stop bits.[[br]]This bit is effective in SCI-compatible mode only.[[br]] [[br]]Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit (if STOP = 1) to begin checking for an idle period. [[br]] [[br]]This field is writable in SCI mode only. 0 | STOP_ONEOne stop bit is used. 1 | STOP_TWOTwo stop bits are used.
3	PARITY	RW	0h	SCI parity odd/even selection.[[br]]This bit is effective in SCI-compatible mode only. If the PARITY ENA bit (SCIGCR1.2) is set, PARITY designates odd or even parity. The parity bit is calculated based on the data bits in each frame and the address bit (in address-bit mode). The start and stop fields in the frame are not included in the parity calculation.[[br]] [[br]]This field is writable in SCI mode only. 0 | PARITY_ODDOdd parity is used. The SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1. 1 | PARITY_EVENEven parity is used. The SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITYENA	RW	0h	Parity enable.[[br]]Enables or disables the parity function. 0 | PARITYENA_DISABLESCI-compatible mode: Parity disabled; no parity bit is generated during transmission or is expected during reception.[[br]]LIN mode: ID-parity verification is disabled. 1 | PARITYENA_ENABLESCI compatible mode: Parity enabled. A parity bit is generated during transmission and is expected during reception.[[br]]LIN mode: ID-parity verification is enabled.
1	TIMINGMODE	RW	0h	SCI timing mode bit.[[br]]This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. This bit configures the SCI for asynchronous operation. 0 | TIMINGMODE_RSVDReserved. 1 | TIMINGMODE_SETMust be set to 1 when module is configured for SCI operation
0	COMMMODE	RW	0h	SCI/LIN communication mode bit.[[br]]In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5. 0 | COMMMODE_UNUSESCI-compatible mode: Idle-line mode is used. [[br]]LIN mode: ID4 and ID5 are not used for length control. 1 | COMMMODE_USESCI-compatible mode: Address-bit mode is used. [[br]]LIN mode: ID4 and ID5 are used for length control.

4.14.3 LIN0_SCIGCR2 Register (Offset = 8h) [reset = h]

Short Description: The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

Long Description:

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Table 4-1373. Instance Table

Instance Name	Physical Address
LIN0	5240 0008h
LIN1	5240 1008h
LIN2	5240 2008h
LIN3	5240 3008h
LIN4	5240 4008h

Figure 4-654. LIN0_SCIGCR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3														CC	SC
RO														RW	RW
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2							GENWU	RESERVED_1							POWERDOWN
RO							RW	RO							RW
0							0	0							0

Access Types Legend

Table 4-1374. SCIGCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED_3	RO	0h	Reserved
17	CC	RW	0h	Compare Checksum.[[br]]This mode is effective in LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by writing a one to this bit.[[br]]In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte.[[br]]During Multi-buffer mode, following are the scenarios associated with the CC bit :[[br]]- If CC bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte.[[br]]- If CC bit is set during the IDLE period (i.e. during inter-frame space), then the next immediate byte will be treated as a checksum byte.[[br]] [[br]]A CE will immediatly be flagged if there is a checksum error. This bit is automatically cleared once the checksum is successfully compared. 0 | CC_NO_EFFECTNo effect 1 | CC_EFFECTCompare checksum on expected checkbyte
16	SC	RW	0h	Send Checksum[[br]]This mode is effective in LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16]). [[br]] [[br]]This field is writable in LIN mode only. 0 | SC_NO_CHECKNo checkbyte will be sent. 1 | SC_CHECKA checkbyte will be sent. This bit will automatically get cleared after the checkbyte is transmitted. The checksum will not be sent if this bit is set before transmitting the very first byte, that is, during interframe space.
15 - 9	RESERVED_2	RO	0h	Reserved

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Table 4-1374. SCIGCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	GENWU	RW	0h	Generate wakeup signal.[[br]]This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid sync break. 0 | GENWU_NO_EFFECTNo effect 1 | GENWU_EFFECTTransmit TDO for wakeup. This bit will be cleared on a SWnRST (SCIGCR1.7)
7 - 1	RESERVED_1	RO	0h	Reserved
0	POWERDOWN	RW	0h	Power down.[[br]]This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/LIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/LIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection (more than 4 seconds, i.e. 80,000 cycles at 20kHz) 0 | POWERDOWN_RUNNormal operation 1 | POWERDOWN_LOWRequest local low-power mode

4.14.4 LIN0_SCISETINT Register (Offset = Ch) [reset = h]

Short Description: The SCISETINT register is used to enable the various interrupts available in the LIN module.

Long Description:

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Table 4-1375. Instance Table

Instance Name	Physical Address
LIN0	5240 000Ch
LIN1	5240 100Ch
LIN2	5240 200Ch
LIN3	5240 300Ch
LIN4	5240 400Ch

Figure 4-655. LIN0_SCISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINT	SETPBEINT	SETCEINT	SETISFEINT	SETNREINT	SETFEINT	SETOEINT	SETPEINT	RESERVED_5					SET_RX_DMA_ALL	SET_RX_DMA	SET_TX_DMA
RW	RW	RW	RW	RW	RW	RW	RW	RO					RW	RW	RW
0	0	0	0	0	0	0	0	0					0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINT	RESERVED_3			SETRXINT	SETTXINT	SETTOA3WUSINT	SETTOAWUSINT	RESERVED_2	SETTIMEOUTINT	RESERVED_1		SETWAKEUPINT	SETBRKDTINT
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1376. SCISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINT	RW	0h	Set bit error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a bit error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETBEINT_ENABLEInterrupt is enabled.
30	SETPBEINT	RW	0h	Set physical bus error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a physical bus error occurs.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETPBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETPBEINT_ENABLEInterrupt is enabled.
29	SETCEINT	RW	0h	Set checksum-error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a checksum error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETCEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETCEINT_DEABLEInterrupt is enabled.
28	SETISFEINT	RW	0h	Set inconsistent-sync-field-error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is an inconsistent sync field error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETISFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETISFEINT_ENABLEInterrupt is enabled.

Table 4-1376. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	SETNREINT	RW	0h	Set no-response-error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a no-response error occurs.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETNREINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETNREINT_ENABLEInterrupt is enabled.
26	SETFEINT	RW	0h	Set framing-error interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a framing error occurs. 0 | SETFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETFEINT_ENABLEInterrupt is enabled.
25	SETOEINT	RW	0h	Set overrun-error interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when an overrun error occurs. 0 | SETOEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETOEINT_ENABLEInterrupt is enabled.
24	SETPEINT	RW	0h	Set parity interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a parity error occurs. 0 | SETPEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETPEINT_ENABLEInterrupt is enabled.
23 - 19	RESERVED_5	RO	0h	Reserved
18	SET_RX_DMA_ALL	RW	0h	Set receiver DMA for Address & Data frames.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable RX DMA request for address and data frames this bit must be set. If it is cleared, RX interrupt request is generated for address frames and DMA requests are generated for data frames. 0 | SERXDMAALL_DISABLEReceiver DMA request is disabled for address frames (RX interrupt request is enabled for address frames). Writing a 0 to this bit has no effect. 1 | SERXDMAALL_ENABLEReceiver DMA request is enabled for address and data frames
17	SET_RX_DMA	RW	0h	Set receiver DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the receiver this bit must be set. If it is cleared, interrupt requests are generated depending on SETRXINT. 0 | SERXDMA_DISABLEReceiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 | SERXDMA_ENABLEReceiver DMA request is enabled.
16	SET_TX_DMA	RW	0h	Set transmit DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SETTXINT. 0 | SETXDMA_DISABLETransmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 | SETXDMA_ENABLETransmit DMA request is enabled
15 - 14	RESERVED_4	RO	0h	Reserved
13	SETIDINT	RW	0h	Set Identification interrupt.[[br]]This bit is effective in LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received. 0 | SETIDINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETIDINT_ENABLEInterrupt is enabled.
12 - 10	RESERVED_3	RO	0h	Reserved
9	SETRXINT	RW	0h	Set Receiver interrupt.[[br]]Setting this bit enables the SCI/LIN to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD. 0 | SETRXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETRXINT_ENABLEInterrupt is enabled.
8	SETTXINT	RW	0h	Set Transmitter interrupt.[[br]]Setting this bit enables the SCI/LIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set. 0 | SETTXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTXINT_ENABLEInterrupt is enabled.

Table 4-1376. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SETTOA3WUSINT	RW	0h	Set Timeout After 3 Wakeup Signals interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOA3WUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTOA3WUSINT_ENABLEInterrupt is enabled.
6	SETTOAWUSINT	RW	0h	Set Timeout After Wakeup Signal interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after one wakeup signal has been sent.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOAWUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTOAWUSINT_ENABLEInterrupt is enabled.
5	RESERVED_2	RO	0h	Reserved
4	SETTIMEOUTINT	RW	0h	Set timeout interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when no LIN bus activity (bus idle) occurs for at least 4 seconds.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTIMEOUTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTIMEOUTINT_ENABLEInterrupt is enabled.
3 - 2	RESERVED_1	RO	0h	Reserved
1	SETWAKEUPINT	RW	0h	Set wake-up interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN to generate a wake-up interrupt and thereby exit low-power mode. The wake-up interrupt is asserted on falling edge of the wake-up pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during low-power mode. Wake-up interrupt is not asserted upon a wakeup pulse if the module is not in power down mode. 0 | SETWAKEUPINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETWAKEUPINT_ENABLEInterrupt is enabled.
0	SETBRKDTINT	RW	0h	Set break-detect interrupt.[[br]]This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/LIN to generate an interrupt if a break condition is detected on the LINRX pin.[[br]] [[br]]This field is writable in SCI mode only. 0 | SETBRKDTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETBRKDTINT_ENABLEInterrupt is enabled.

4.14.5 LIN0_SCICLEARINT Register (Offset = 10h) [reset = h]

Short Description: The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.

Long Description:

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Table 4-1377. Instance Table

Instance Name	Physical Address
LIN0	5240 0010h
LIN1	5240 1010h
LIN2	5240 2010h
LIN3	5240 3010h
LIN4	5240 4010h

Figure 4-656. LIN0_SCICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINT	CLRPBEINT	CLRCEINT	CLRISFEINT	CLRNREINT	CLRFEINT	CLROEINT	CLRPEINT	RESERVED_6					RESERVED_5	SETRXDMA	CLRTXDMA
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RW	RW
0	0	0	0	0	0	0	0	0					0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINT	RESERVED_3			CLRRXINT	CLRTXINT	CLRTOA3WUSINT	CLRTOAWUSINT	RESERVED_2	CLRTIMEOUTINT	RESERVED_1		CLRWAKEUPINT	CLRBRKDTINT
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1378. SCICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINT	RW	0h	Clear Bit Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the bit error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRBEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
30	CLRPBEINT	RW	0h	Clear Physical Bus Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the physical-bus error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRPBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRPBEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
29	CLRCEINT	RW	0h	Clear checksum-error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the checksum-error interrupt. [[br]] [[br]]This field is writable in LIN mode only. 0 | CLRCEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRCEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
28	CLRISFEINT	RW	0h	Clear Inconsistent-Sync-Field-Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the ISFE interrupt. [[br]] [[br]]This field is writable in LIN mode only. 0 | CLRISFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRISFEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

Table 4-1378. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CLRNREINT	RW	0h	Clear No-Reponse-Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the no-response error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRNREINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRNREINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
26	CLRFEINT	RW	0h	Clear Framing-Error Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables framing-error interrupt. 0 | CLRFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRFEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
25	CLROEINT	RW	0h	Clear Overrun-Error Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the overrun interrupt. 0 | CLROEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLROEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
24	CLRPEINT	RW	0h	Clear Parity Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the parity error interrupt. 0 | CLRPEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRPEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
23 - 19	RESERVED_6	RO	0h	Reserved
18	RESERVED_5	RO	0h	Reserved
17	SETRXDMA	RW	0h	Clear receiver DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receive DMA request. 0 | CLRRXDMA_DISABLEReceiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 | CLRRXDMA_ENABLEReceiver DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
16	CLRTXDMA	RW	0h	Clear transmit DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmit DMA request. 0 | CLRTXDMA_DISABLETransmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 | CLRTXDMA_ENABLETransmit DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
15 - 14	RESERVED_4	RO	0h	Reserved
13	CLRIDINT	RW	0h	Clear Identifier interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the ID interrupt. 0 | CLRIDINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRIDINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
12 - 10	RESERVED_3	RO	0h	Reserved
9	CLRRXINT	RW	0h	Clear Receiver interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receiver interrupt. 0 | CLRRXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRRXINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
8	CLRTXINT	RW	0h	Clear Transmitter interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmitter interrupt. 0 | CLRTXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTXINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
7	CLRTOA3WUSINT	RW	0h	Clear Timeout After 3 Wakeup Signals interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOA3WUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTOA3WUSINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

Table 4-1378. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CLRTOAWUSINT	RW	0h	Clear Timeout After Wakeup Signal interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOAWUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTOAWUSINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
5	RESERVED_2	RO	0h	Reserved
4	CLRTIMEOUTINT	RW	0h	Clear Timeout interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout (LIN bus idle) interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTIMEOUTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTIMEOUTINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
3 - 2	RESERVED_1	RO	0h	Reserved
1	CLRWAKEUPINT	RW	0h	Clear Wake-up interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the wake-up interrupt. 0 | CLRWAKEUPINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRWAKEUPINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
0	CLRBRKDTINT	RW	0h	Clear Break-detect interrupt.[[br]]This bit is effective in SCI-compatible mode only. Setting this bit disables the Break-detect interrupt.[[br]] [[br]]This field is writable in SCI mode only. 0 | CLRBRKDTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRBRKDTINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

4.14.6 LIN0_SCISETINTLVL Register (Offset = 14h) [reset = h]

Short Description: The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.

Long Description:

Return to Summary Table

Table 4-1379. Instance Table

Instance Name	Physical Address
LIN0	5240 0014h
LIN1	5240 1014h
LIN2	5240 2014h
LIN3	5240 3014h
LIN4	5240 4014h

Figure 4-657. LIN0_SCISETINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINTLVL	SETPBEINTLVL	SETCEINTLVL	SETISFEINTLVL	SETNREINTLVL	SETFEINTLVL	SETOEINTLVL	SETPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RO	
0	0	0	0	0	0	0	0	0					0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINTLVL	RESERVED_3			SETRXINTOVO	SETTXINTLVL	SETTOA3WUSINTLVL	SETTOAWUSINTLVL	RESERVED_2	SETTIMEOUTINTLVL	RESERVED_1		SETWAKEUPINTLVL	SETBRKDTINTLVL
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1380. SCISETINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINTLVL	RW	0h	Set Bit Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETBEINTLVL_INT1Interrupt level mapped to INT1 line.
30	SETPBEINTLVL	RW	0h	Set Physical Bus Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETPBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETPBEINTLVL_INT1Interrupt level mapped to INT1 line.
29	SETCEINTLVL	RW	0h	Set Checksum-error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETCEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETCEINTLVL_INT1Interrupt level mapped to INT1 line.
28	SETISFEINTLVL	RW	0h	Set Inconsistent-Sync-Field-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETISFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETISFEINTLVL_INT1Interrupt level mapped to INT1 line.

Table 4-1380. SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	SETNREINTLVL	RW	0h	Set No-Reponse-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETNREINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETNREINTLVL_INT1Interrupt level mapped to INT1 line.
26	SETFEINTLVL	RW	0h	Set Framing-Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT1 line. 0 | SETFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETFEINTLVL_INT1Interrupt level mapped to INT1 line.
25	SETOEINTLVL	RW	0h	Set Overrun-Error Interrupt Level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT1 line. 0 | SETOEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETOEINTLVL_INT1Interrupt level mapped to INT1 line.
24	SETPEINTLVL	RW	0h	Set Parity Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity error interrupt level to the INT1 line. 0 | SETPEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETPEINTLVL_INT1Interrupt level mapped to INT1 line.
23 - 19	RESERVED_7	RO	0h	Reserved
18	RESERVED_6	RO	0h	Reserved
17 - 16	RESERVED_5	RO	0h	Reserved
15 - 14	RESERVED_4	RO	0h	Reserved
13	SETIDINTLVL	RW	0h	Set ID interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETIDINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETIDINTLVL_INT1Interrupt level mapped to INT1 line.
12 - 10	RESERVED_3	RO	0h	Reserved
9	SETRXINTOVO	RW	0h	Set Receiver interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT1 line. 0 | SETRXINTOVO_INT0Interrupt level mapped to INT0 line. 1 | SETRXINTOVO_INT1Interrupt level mapped to INT1 line.
8	SETTXINTLVL	RW	0h	Set Transmitter interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT1 line. 0 | SETTXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTXINTLVL_INT1Interrupt level mapped to INT1 line.
7	SETTOA3WUSINTLVL	RW	0h	Set Timeout After 3 Wakeup Signals interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOA3WUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTOA3WUSINTLVL_INT1Interrupt level mapped to INT1 line.
6	SETTOAWUSINTLVL	RW	0h	Set Timeout After Wakeup Signal interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOAWUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTOAWUSINTLVL_INT1Interrupt level mapped to INT1 line.
5	RESERVED_2	RO	0h	Reserved
4	SETTIMEOUTINTLVL	RW	0h	Set Timeout interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTIMEOUTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTIMEOUTINTLVL_INT1Interrupt level mapped to INT1 line.
3 - 2	RESERVED_1	RO	0h	Reserved

Table 4-1380. SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETWAKEUPINTLVL	RW	0h	Set Wake-up interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT1 line. 0 | SETWAKEUPINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETWAKEUPINTLVL_INT1Interrupt level mapped to INT1 line.
0	SETBRKDTINTLVL	RW	0h	Set Break-detect interrupt level.[[br]]This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT1 line.[[br]] [[br]]This field is writable in SCI mode only. 0 | SETBRKDTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETBRKDTINTLVL_INT1Interrupt level mapped to INT1 line.

4.14.7 LIN0_SCICLEARINTLVL Register (Offset = 18h) [reset = h]

Short Description: The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.

Long Description:

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Table 4-1381. Instance Table

Instance Name	Physical Address
LIN0	5240 0018h
LIN1	5240 1018h
LIN2	5240 2018h
LIN3	5240 3018h
LIN4	5240 4018h

Figure 4-658. LIN0_SCICLEARINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINTLVL	CLRPBEINTLVL	CLRCEINTLVL	CLRISFEINTLVL	CLRNREINTLVL	CLRFEINTLVL	CLROEINTLVL	CLRPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RO	
0	0	0	0	0	0	0	0	0					0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINTLVL	RESERVED_3			CLRRXINTLVL	CLRTXINTLVL	CLRTOA3WUSINTLVL	CLRTOAWUSINTLVL	RESERVED_2	CLRTIMEOUTINTLVL	RESERVED_1		CLRWAKEUPINTLVL	CLRBRKDTINTLVL
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1382. SCICLEARINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINTLVL	RW	0h	Clear Bit Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRBEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
30	CLRPBEINTLVL	RW	0h	Clear Physical Bus Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRPBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRPBEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
29	CLRCEINTLVL	RW	0h	Clear Checksum-error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRCEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRCEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
28	CLRISFEINTLVL	RW	0h	Clear Inconsistent-Sync-Field-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRISFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRISFEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

Table 4-1382. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CLRNREINTLVL	RW	0h	Clear No-Reponse-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRNREINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRNREINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
26	CLRFEINTLVL	RW	0h	Clear Framing-Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT0 line. 0 | CLRFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRFEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
25	CLROEINTLVL	RW	0h	Clear Overrun-Error Interrupt Level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT0 line. 0 | CLROEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLROEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
24	CLRPEINTLVL	RW	0h	Clear Parity Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity Error interrupt level to the INT0 line. 0 | CLRPEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRPEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
23 - 19	RESERVED_7	RO	0h	Reserved
18	RESERVED_6	RO	0h	Reserved
17 - 16	RESERVED_5	RO	0h	Reserved
15 - 14	RESERVED_4	RO	0h	Reserved
13	CLRIDINTLVL	RW	0h	Clear ID interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRIDINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRIDINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
12 - 10	RESERVED_3	RO	0h	Reserved
9	CLRRXINTLVL	RW	0h	Clear Receiver interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT0 line. 0 | CLRRXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRRXINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
8	CLRTXINTLVL	RW	0h	Clear Transmitter interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT0 line. 0 | CLRTXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTXINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
7	CLRTOA3WUSINTLVL	RW	0h	Clear Timeout After 3 Wakeup Signals interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOA3WUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTOA3WUSINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
6	CLRTOAWUSINTLVL	RW	0h	Clear Timeout After Wakeup Signal interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOAWUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTOAWUSINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

Table 4-1382. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED_2	RO	0h	Reserved
4	CLRTIMEOUTINTLVL	RW	0h	Clear Timeout interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTIMEOUTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTIMEOUTINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
3 - 2	RESERVED_1	RO	0h	Reserved
1	CLRWAKEUPINTLVL	RW	0h	Clear Wake-up interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT0 line. 0 | CLRWAKEUPINTLVL_INT0Interrupt level mapped to INT0 line. Writing a 0 to this bit has no effect. 1 | CLRWAKEUPINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
0	CLRBRKDTINTLVL	RW	0h	Clear Break-detect interrupt level.[[br]]This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT0 line.[[br]] [[br]]This field is writable in SCI mode only. 0 | CLRBRKDTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRBRKDTINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

4.14.8 LIN0_SCIFLR Register (Offset = 1Ch) [reset = h]

Short Description: The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.

Long Description:

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Table 4-1383. Instance Table

Instance Name	Physical Address
LIN0	5240 001Ch
LIN1	5240 101Ch
LIN2	5240 201Ch
LIN3	5240 301Ch
LIN4	5240 401Ch

Figure 4-659. LIN0_SCIFLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BE	PBE	CE	ISFE	NRE	FE	OE	PE	RESERVED_3							
RW	RW	RW	RW	RW	RW	RW	RW	RO							
0	0	0	0	0	0	0	0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2	IDRXFLAG	IDTXFLAG	RXWAKE	TXEMPTY	TXWAKE	RXRDY	TXRDY	TOA3WUS	TOAWUS	RESERVED_1	TIMEOUT	BUSY	IDLE	WAKEUP	BRKDT
RO	RW	RW	RO	RO	RW	RW	RO	RW	RW	RO	RW	RO	RO	RW	RW
0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0

Access Types Legend

Table 4-1384. SCIFLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BE	RW	0h	Bit Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been a bit error. This is detected by the bit monitor in the internal bit monitor. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | BE_NO_EFFECTNo bit error detected. 1 | BE_EFFECTBit error detected.
30	PBE	RW	0h	Physical Bus Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]Note: thie PBE will ony be flagged if no sync break can be generated. (because of a bus shortage to VBAT) or if no sync break delimeter can be generated (because of a bus shortage to GND).[[br]] [[br]]This field is writable in LIN mode only. 0 | PBE_NO_EFFECTNo physiscal bus error detected. 1 | PBE_EFFECTPhysical bus error detected.

Table 4-1384. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	CE	RW	0h	Checksum Error Flag. [[br]]This bit is effective in LIN mode only. This bit is set when there is checksum error detected by a receiving node. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | CE_NO_EFFECTNo Checksum error detected. 1 | CE_EFFECTChecksum error detected.
28	ISFE	RW	0h	Inconsistent Sync Field Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been an inconsistent Sync Field error detected by the synchronizer during header reception. See the "Header Reception and Adaptive Baudrate" section for more information. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | ISFE_NO_EFFECTNo Inconsistent Sync Field error detected. 1 | ISFE_EFFECTInconsistent Sync Field error detected.
27	NRE	RW	0h	No-Response Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there is no response to a master's header completed within TFRAME_MAX. This timeout period is applied for message frames of unknown length (identifiers 0 to 61). This error is detected by the synchronizer of the module. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | NRE_NO_EFFECTNo No-Response error detected. 1 | NRE_EFFECTNo-Response error detected.
26	FE	RW	0h	Framing error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new character (SCI-compatible mode), or frame (LIN mode)[[br]]In multibuffer mode the frame is defined in the SCIFORMAT register. 0 | FE_NO_EFFECTNo framing error detected. 1 | FE_EFFECTFraming error detected.
25	OE	RW	0h	Overrun error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit 0 | OE_NO_EFFECTNo overrun error detected. 1 | OE_EFFECTOverrun error detected.

Table 4-1384. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	PE	RW	0h	Parity error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In SCI address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see the "SCI Global Control Register (SCIGCR1)" description. If the parity function is disabled (that is, SCIGCR1.2 = 0), the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit = 1. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Reception of a new charcter (SCI-compatible mode) orframe (LIN mode)[[br]]- Writing a 1 to this bit 0 | PE_NO_EFFECTNo parity error or parity disabled. 1 | PE_EFFECTParity error detected.
23 - 16	RESERVED_3	RO	0h	Reserved
15	RESERVED_2	RO	0h	Reserved
14	IDRXFLAG	RW	0h	Identifier On Receive Flag.[[br]]This bit is effective in LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Reading the LINID register[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | IDRXFLAG_NO_EFFECTNo valid ID received. 1 | IDRXFLAG_EFFECTValid ID RX received in LINID[23:16] on RX match.
13	IDTXFLAG	RW	0h	Identifier On Transmit Flag.[[br]]This bit is effective in LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by: [[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting SWnRESET[[br]]- System reset[[br]]- Reading the LINID register[[br]]- Writing a 1 to this bit [[br]] [[br]]This field is writable in LIN mode only. 0 | IDTXFLAG_NO_EFFECTNo valid ID received. 1 | IDTXFLAG_EFFECTValid ID received in LINID[23:16] on TX match.
12	RXWAKE	RO	0h	Receiver wakeup detect flag.[[br]]This bit is effective in SCI-compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. This bit is cleared by: [[br]]- RESET bit[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- System reset[[br]]- Receipt of a data frame[[br]] [[br]]This bit is writable in SCI mode only. Read0 | RXWAKE_NO_EFFECTThe data in SCIRD is not an address. Read1 | RXWAKE_EFFECTThe data in SCIRD is an address.[[br]]See [1] Section 3.4.4, Sleep Mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.

Table 4-1384. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TXEMPTY	RO	1h	Transmitter Empty flag.[[br]]The value of this flag indicates the contents of the transmitter's buffer register(s) (SCITD/TDy) and shift register (SCITXSHF). In multibuffer mode, this flag indicates the value of the TDx registers and shift register (SCITXSHF). In non multibuffer mode, this flag indicates the value of LINTD0 (byte) and shift register (SCITXSHF). This bit is set by: [[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- System reset. [[br]] [[br]]Note: This bit does not cause an interrupt request. Read0 | TXEMPTY_NO_EFFECTCompatible mode or LIN with no multibuffer:[[br]]Transmitter buffer or shift register (or both) are loaded with data.[[br]]In LIN mode using multibuffer mode: [[br]]Multibuffer or shift register (or all) are loaded with data. Read1 | TXEMPTY_EFFECTCompatible mode or LIN with no multibuffer: [[br]]Transmitter buffer and shift registers are both empty.[[br]]In LIN mode using multibuffer mode:[[br]]Multibuffer and shift registers are all empty.
10	TXWAKE	RW	0h	SCI transmitter wakeup method select.[[br]]This bit is effective in SCI-compatible mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SWnRESET bit (SCIGCR1.7). 0 | TXWAKE_ADDR0Address-bit mode: Frame to be transmitted will be data (address bit = 0).[[br]]Idle-line mode: Frame to be transmitted will be data. 1 | TXWAKE_ADDR1Address-bit mode:[[br]]Frame to be transmitted will be an address (address bit=1).[[br]]Idle-line mode: [[br]]Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).
9	RXRDY	RW	0h	Receiver ready flag. [[br]]In SCI compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/LIN generates a receive interrupt when RXRDY flag bit is set[[br]]if the interrupt-enable bit is set (SCISETINT.9). RXRDY is cleared by:[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reading SCIRD in while in SCI compatibility mode[[br]]- Reading last data byte RDy of the response in LIN mode [[br]] [[br]]Note: The RXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. 0 | RXRDY_NO_EFFECTNo new data in SCIRD/RDy. 1 | RXRDY_EFFECTNew data ready to be read from SCIRD.
8	TXRDY	RO	1h	Transmitter buffer register ready flag.[[br]]When set, this bit indicates that the transmit buffer(s) register (SCITD in compatibility mode and LINTD0, LINTD1 in MBUF mode) is/are ready to get another character from a CPU write. [[br]]In SCI compatibility mode, writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 (TD0) is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit DMA event if the DMA enable bit is set. This bit is set to 1 by:[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET (SCIGCR1.7)[[br]]- System reset[[br]] [[br]]Note: The TXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]] [[br]]Note: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disaLINg the corresponding interrupt via theSCICLEARINT register or by disaLINg the transmitter via the TXENA bit (SCIGCR1.25=0). Read0 | TXRDY_FULLCompatible mode: SCITD is full.[[br]]LIN mode: The multibuffers are full. Read1 | TXRDY_EMPTYCompatible mode: SCITD is ready to receive the next character.[[br]]LIN mode: The multibuffers are ready to receive the next character(s).

Table 4-1384. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TOA3WUS	RW	0h	Timeout After 3 Wakeup Signals flag.[[br]]This bit is effective in LIN mode only. This flag is set if there is no Sync Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TOA3WUS_NO_EFFECTNo timeout after 3 wakeup signals. 1 | TOA3WUS_EFFECTTimeout after 3 wakeup signals and 1.5s time.
6	TOAWUS	RW	0h	Timeout After Wakeup Signal flag.[[br]]This bit is effective in LIN mode only. This bit is set if there is no Sync Break received after a wakeup signal has been sent. A minimum of 150 ms expiration time is used before issuing another wakeup signal. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TOAWUS_NO_EFFECTNo timeout after one wakeup signal (150 ms). 1 | TOAWUS_EFFECTTimeout after one wakeup signal.
5	RESERVED_1	RO	0h	Reserved
4	TIMEOUT	RW	0h	LIN Bus IDLE timeout flag.[[br]]This bit is effective in LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TIMEOUT_NO_EFFECTNo bus idle detected. 1 | TIMEOUT_EFFECTLIN bus idle detected.
3	BUSY	RO	0h	Bus BUSY flag.[[br]]This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/LIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but can be cleared by:[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset. Read0 | BUSY_NO_EFFECTReceiver is not currently receiving a frame. Read1 | BUSY_EFFECTReceiver is currently receiving a frame.
2	IDLE	RO	1h	SCI receiver in idle state.[[br]]This bit is effective in SCI-compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state:[[br]]- After a system reset[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- After coming out of power down[[br]] [[br]]This bit is writable in SCI mode only. Read0 | IDLE_NO_EFFECTIdle period detected, the SCI is ready to receive. Read1 | IDLE_EFFECTIdle period not detected, the SCI will not receive any data.
1	WAKEUP	RW	0h	Wake-up flag.[[br]]This bit is effective in LIN mode only. This bit is set by the SCI/LIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit (SCISETINT.1) is set. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit.[[br]] [[br]]This field is writable in LIN mode only. 0 | WAKEUP_NO_EFFECTDo not wake up from power-down mode. 1 | WAKEUP_EFFECTWake up from power-down mode.

Table 4-1384. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BRKDT	RW	0h	SCI break-detect flag.[[br]]This bit is effective in SCI-compatible mode only. This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- By writing a 1 to this bit.[[br]] [[br]]This bit is writable in SCI mode only. 0 | BRKDT_NO_EFFECTNo break condition detected. 1 | BRKDT_EFFECTBreak condition detected.

4.14.9 LIN0_SCIINTVECT0 Register (Offset = 20h) [reset = h]

Short Description: The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.

Long Description:

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Table 4-1385. Instance Table

Instance Name	Physical Address
LIN0	5240 0020h
LIN1	5240 1020h
LIN2	5240 2020h
LIN3	5240 3020h
LIN4	5240 4020h

Figure 4-660. LIN0_SCIINTVECT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT0				
RO											RO				
0											0				

Access Types Legend

Table 4-1386. SCIINTVECT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 5	RESERVED_1	RO	0h	Reserved
4 - 0	INTVECT0	RO	0h	Interrupt vector offset for INT0.[[br]]This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.[[br]] [[br]]Note: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

4.14.10 LIN0_SCIINTVECT1 Register (Offset = 24h) [reset = h]

Short Description: The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.

Long Description:

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Table 4-1387. Instance Table

Instance Name	Physical Address
LIN0	5240 0024h
LIN1	5240 1024h
LIN2	5240 2024h
LIN3	5240 3024h
LIN4	5240 4024h

Figure 4-661. LIN0_SCIINTVECT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT1				
RO											RO				
0											0				

Access Types Legend

Table 4-1388. SCIINTVECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 5	RESERVED_1	RO	0h	Reserved
4 - 0	INTVECT1	RO	0h	Interrupt vector offset for INT1.[[br]]This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.[[br]] [[br]]Note: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

4.14.11 LIN0_SCIFORMAT Register (Offset = 28h) [reset = h]

Short Description: The SCIFORMAT register is used to set up the character and frame lengths.

Long Description:

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Table 4-1389. Instance Table

Instance Name	Physical Address
LIN0	5240 0028h
LIN1	5240 1028h
LIN2	5240 2028h
LIN3	5240 3028h
LIN4	5240 4028h

Figure 4-662. LIN0_SCIFORMAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2													LENGTH		
RO													RW		
0													0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													CHAR		
RO													RW		
0													0		

Access Types Legend

Table 4-1390. SCIFORMAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED_2	RO	0h	Reserved
18 - 16	LENGTH	RW	0h	Frame length control bits.[[br]]In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length (SCIGCR1[0] = 1), then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each. 0x0 | FIELD_1The response field has 1 bytes/characters. 0x1 | FIELD_2The response field has 2 bytes/characters. 0x2 | FIELD_3The response field has 3 bytes/characters. 0x3 | FIELD_4The response field has 4 bytes/characters. 0x4 | FIELD_5The response field has 5 bytes/characters. 0x5 | FIELD_6The response field has 6 bytes/characters. 0x6 | FIELD_7The response field has 7 bytes/characters. 0x7 | FIELD_8The response field has 8 bytes/characters.
15 - 3	RESERVED_1	RO	0h	Reserved

Table 4-1390. SCIFORMAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	CHAR	RW	0h	Character length control bits.[[br]]These bits are effective in SCI compatible mode only. These bits set the SCI character length from 1 to 8 bits.[[br]] [[br]]Note: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified.[[br]] [[br]]Note: Data written to the SCITD should be right justified but does not need to be padded with leading zeros.[[br]] [[br]]These bits are witable in SCI mode only. 0x0 | CHAR_1The character is 1 bits long. 0x1 | CHAR_2The character is 2 bits long. 0x2 | CHAR_3The character is 3 bits long. 0x3 | CHAR_4The character is 4 bits long. 0x4 | CHAR_5The character is 5 bits long. 0x5 | CHAR_6The character is 6 bits long. 0x6 | CHAR_7The character is 7 bits long. 0x7 | CHAR_8The character is 8 bits long.

4.14.12 LIN0_BRSR Register (Offset = 2Ch) [reset = h]

Short Description: The BRSR register is used to configure the baud rate of the LIN module.

Long Description:

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Table 4-1391. Instance Table

Instance Name	Physical Address
LIN0	5240 002Ch
LIN1	5240 102Ch
LIN2	5240 202Ch
LIN3	5240 302Ch
LIN4	5240 402Ch

Figure 4-663. LIN0_BRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1	U			M				SCI_LIN_PSH							
RO	RW			RW				RW							
0	0			0				0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI_LIN_PSL															
RW															
0															

Access Types Legend

Table 4-1392. BRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	RO	0h	Reserved
30 - 28	U	RW	0h	Superfractional Divider Selection. (U)[[br]]These bits are an additional fractional part for the baudrate specification. These bits allow a super fine tuning of the fractional baudrate with 7 more intermediate values for each of the M fractional divider values. See the Superfractional Divider section for more details.
27 - 24	M	RW	0h	SCI/LIN 4-bit Fractional Divider Selection. (M)[[br]]These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/LIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values.
23 - 16	SCI_LIN_PSH	RW	0h	PRESCALER P (High Bits).[[br]]SCI/LIN 24-bit Integer Prescaler Selection.[[br]]These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.
15 - 0	SCI_LIN_PSL	RW	0h	PRESCALER P (Low Bits).[[br]]SCI/LIN 24-bit Integer Prescaler Selection.[[br]]These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

4.14.13 LIN0_SCIED Register (Offset = 30h) [reset = h]

Short Description: The SCIED register is a duplicate copy of SCIRD register that has no affect on the RXRDY flag for use with an emulator.

Long Description:

Return to Summary Table

Table 4-1393. Instance Table

Instance Name	Physical Address
LIN0	5240 0030h
LIN1	5240 1030h
LIN2	5240 2030h
LIN3	5240 3030h
LIN4	5240 4030h

Figure 4-664. LIN0_SCIED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								ED							
RO								RO							
0								0							

Access Types Legend

Table 4-1394. SCIED Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	ED	RO	0h	Receiver Emulation Data.[[br]]This bit is effective in SCI-compatible mode only. Reading SCIED(7-0) does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag.

ADVANCE INFORMATION

4.14.14 LIN0_SCIRD Register (Offset = 34h) [reset = h]

Short Description: The SCIRD register is where received data is stored and can be read from.

Long Description:

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Table 4-1395. Instance Table

Instance Name	Physical Address
LIN0	5240 0034h
LIN1	5240 1034h
LIN2	5240 2034h
LIN3	5240 3034h
LIN4	5240 4034h

Figure 4-665. LIN0_SCIRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								RD							
RO								RO							
0								0							

Access Types Legend

Table 4-1396. SCIRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	RD	RO	0h	Received Data.[[br]]This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA (SCISETINT0.9) is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared.[[br]] [[br]]When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left justified format padded with trailing zeros. Therefore, your software should perform a logical shift on the data by the correct number of positions to make it right justified.

4.14.15 LIN0_SCITD Register (Offset = 38h) [reset = h]

Short Description: The SCITD register is where data to be transmitted is written to by application software.

Long Description:

Return to Summary Table

Table 4-1397. Instance Table

Instance Name	Physical Address
LIN0	5240 0038h
LIN1	5240 1038h
LIN2	5240 2038h
LIN3	5240 3038h
LIN4	5240 4038h

Figure 4-666. LIN0_SCITD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TD							
RO								RW							
0								0							

Access Types Legend

Table 4-1398. SCITD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	TD	RW	0h	Transmit data[[br]]This bit is effective in SCI-compatible mode only. Data to be transmitted is written to this register. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag (SCIFLR.23), which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA (SCISETINT.8) is set, this data transfer also causes an interrupt.[[br]] [[br]]Note: Data written to the SCIRD register that is fewer than eight bits long must be right justified, but it does not need to be padded with leading zeros.

4.14.16 LIN0_SCIPIO0 Register (Offset = 3Ch) [reset = h]

Short Description: The SCIPIO0 register is used to enable the LINTX and LINRX pins.

Long Description:

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Table 4-1399. Instance Table

Instance Name	Physical Address
LIN0	5240 003Ch
LIN1	5240 103Ch
LIN2	5240 203Ch
LIN3	5240 303Ch
LIN4	5240 403Ch

Figure 4-667. LIN0_SCIPIO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXFUNC	RXFUNC	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1400. SCIPIO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXFUNC	RW	0h	Transmit pin function.[[br]]This bit is effective in LIN or SCI mode. This bit defines the function of LINTX pin. 0 | LINTX_DISABLEDLINTX pin is disabled. 1 | LINTX_ENABLEDLINTX pin is enabled.
1	RXFUNC	RW	0h	Receive pin function.[[br]]This bit is effective in LIN or SCI mode. This bit defines the function of the LINRX pin. 0 | LINRX_DISABLEDLINRX pin is disabled. 1 | LINRX_ENABLEDLINRX pin is enabled.
0	RESERVED_1	RO	0h	Reserved

4.14.17 LIN0_SCIPIO1 Register (Offset = 40h) [reset = h]

Short Description: Pin control Register 1

Long Description:

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Table 4-1401. Instance Table

Instance Name	Physical Address
LIN0	5240 0040h
LIN1	5240 1040h
LIN2	5240 2040h
LIN3	5240 3040h
LIN4	5240 4040h

Figure 4-668. LIN0_SCIPIO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXDIR	RXDIR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1402. SCIPIO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXDIR	RW	0h	Transmit pin direction.[[br]]This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINTX pin if it is configured with general-purpose I/O functionality (TX FUNC = 0). 0: general purpose input pin. 1: general-purpose output pin
1	RXDIR	RW	0h	Receive pin direction.[[br]]This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINRX pin if it is configured with general-purpose I/O functionality (RX FUNC = 0). 0: general purpose input pin. 1: general-purpose output pin
0	RESERVED_1	RO	0h	Reserved

4.14.18 LIN0_SCIPIO2 Register (Offset = 44h) [reset = h]

Short Description: The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.

Long Description:

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Table 4-1403. Instance Table

Instance Name	Physical Address
LIN0	5240 0044h
LIN1	5240 1044h
LIN2	5240 2044h
LIN3	5240 3044h
LIN4	5240 4044h

Figure 4-669. LIN0_SCIPIO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXIN	RXIN	RESERVED_1
RO													RO	RO	RO
0													0	0	0

Access Types Legend

Table 4-1404. SCIPIO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXIN	RO	0h	Transmit data in.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINTX pin.
1	RXIN	RO	0h	Receive data in.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINRX pin.
0	RESERVED_1	RO	0h	Reserved

4.14.19 LIN0_SCIPIO3 Register (Offset = 48h) [reset = h]

Short Description: Pin control Register 3

Long Description:

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Table 4-1405. Instance Table

Instance Name	Physical Address
LIN0	5240 0048h
LIN1	5240 1048h
LIN2	5240 2048h
LIN3	5240 3048h
LIN4	5240 4048h

Figure 4-670. LIN0_SCIPIO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXOUT	RXOUT	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1406. SCIPIO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXOUT	RW	0h	Transmit pin out.[[br]]This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINTX.
1	RXOUT	RW	0h	Receive pin out.[[br]]This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

4.14.20 LIN0_SCIPIO4 Register (Offset = 4Ch) [reset = h]

Short Description: Pin control Register 4

Long Description:

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Table 4-1407. Instance Table

Instance Name	Physical Address
LIN0	5240 004Ch
LIN1	5240 104Ch
LIN2	5240 204Ch
LIN3	5240 304Ch
LIN4	5240 404Ch

Figure 4-671. LIN0_SCIPIO4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXSET	RXSET	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1408. SCIPIO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXSET	RW	0h	Transmit pin set.[[br]]This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINTX.
1	RXSET	RW	0h	Receive pin set.[[br]]This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

4.14.21 LIN0_SCIPIO5 Register (Offset = 50h) [reset = h]

Short Description: Pin control Register 5

Long Description:

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Table 4-1409. Instance Table

Instance Name	Physical Address
LIN0	5240 0050h
LIN1	5240 1050h
LIN2	5240 2050h
LIN3	5240 3050h
LIN4	5240 4050h

Figure 4-672. LIN0_SCIPIO5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXCLR	RXCLR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1410. SCIPIO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXCLR	RW	0h	Transmit pin clear.[[br]]This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINTX.
1	RXCLR	RW	0h	Receive pin clear.[[br]]This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

4.14.22 LIN0_SCIPIO6 Register (Offset = 54h) [reset = h]

Short Description: Pin control Register 6

Long Description:

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Table 4-1411. Instance Table

Instance Name	Physical Address
LIN0	5240 0054h
LIN1	5240 1054h
LIN2	5240 2054h
LIN3	5240 3054h
LIN4	5240 4054h

Figure 4-673. LIN0_SCIPIO6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPDR	RXPDR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1412. SCIPIO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPDR	RW	0h	Transmit pin open drain enable.[[br]]This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINTX.
1	RXPDR	RW	0h	Receive pin open drain enable.[[br]]This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINRX.
0	RESERVED_1	RO	0h	Reserved

4.14.23 LIN0_SCIPIO7 Register (Offset = 58h) [reset = h]

Short Description: Pin control Register 7

Long Description:

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Table 4-1413. Instance Table

Instance Name	Physical Address
LIN0	5240 0058h
LIN1	5240 1058h
LIN2	5240 2058h
LIN3	5240 3058h
LIN4	5240 4058h

Figure 4-674. LIN0_SCIPIO7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPD	RXPD	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1414. SCIPIO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPD	RW	0h	Transmit pin pull control disable.[[br]]This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINTX.
1	RXPD	RW	0h	Receive pin pull control disable.[[br]]This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINRX.
0	RESERVED_1	RO	0h	Reserved

4.14.24 LIN0_SCIPIO8 Register (Offset = 5Ch) [reset = h]

Short Description: Pin control Register 8

Long Description:

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Table 4-1415. Instance Table

Instance Name	Physical Address
LIN0	5240 005Ch
LIN1	5240 105Ch
LIN2	5240 205Ch
LIN3	5240 305Ch
LIN4	5240 405Ch

Figure 4-675. LIN0_SCIPIO8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPSL	RXPSL	RESERVED_1
RO													RW	RW	RO
0													1	1	1

Access Types Legend

Table 4-1416. SCIPIO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPSL	RW	1h	TX pin pull select.[[br]]This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINTX.
1	RXPSL	RW	1h	RX pin pull select.[[br]]This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINRX.
0	RESERVED_1	RO	1h	Reserved

4.14.25 LIN0_LINCOMP Register (Offset = 60h) [reset = h]

Short Description: The LINCOMPARE register is used to configure the sync delimeter and sync break extension.

Long Description:

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Table 4-1417. Instance Table

Instance Name	Physical Address
LIN0	5240 0060h
LIN1	5240 1060h
LIN2	5240 2060h
LIN3	5240 3060h
LIN4	5240 4060h

Figure 4-676. LIN0_LINCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2						SDEL		RESERVED_1					SBREAK		
RO						RW		RO					RW		
0						0		0					0		

Access Types Legend

Table 4-1418. LINCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 10	RESERVED_2	RO	0h	Reserved
9 - 8	SDEL	RW	0h	2-bit Sync Delimiter compare.[[br]]These bits are effective in LIN mode only. These bits are used to configure the number of Tbit for the sync delimiter in the sync field.[[br]]The time delay calculation for the synchronization delimiter is:[[br]]TSDEL = (SDEL + 1)Tbit[[br]] [[br]]These bits are writable in LIN mode only. 0x0 | SDEL_1The sync delimiter has 1 Tbit. 0x1 | SDEL_2The sync delimiter has 2 Tbit. 0x2 | SDEL_3The sync delimiter has 3 Tbit. 0x3 | SDEL_4The sync delimiter has 4 Tbit.
7 - 3	RESERVED_1	RO	0h	Reserved
2 - 0	SBREAK	RW	0h	3-bit Sync Break extend.[[br]]LIN mode only. These bits are used to configure the number of Tbits for the sync break to extend the minimum 13 Tbit in the Sync Field to a maximum of 20 Tbit.[[br]]The time delay calculation for the sync break is:[[br]]TSYNBRK = 13Tbit + SBREAK x Tbit[[br]] [[br]]These bits are writable in LIN mode only. 0x0 | SBREAK_0The sync break has no additional Tbit. 0x1 | SBREAK_1The sync break has 1 additional Tbit. 0x2 | SBREAK_2The sync break has 2 additional Tbit. 0x3 | SBREAK_3The sync break has 3 additional Tbit. 0x4 | SBREAK_4The sync break has 4 additional Tbit. 0x5 | SBREAK_5The sync break has 5 additional Tbit. 0x6 | SBREAK_6The sync break has 6 additional Tbit. 0x7 | SBREAK_7The sync break has 7 additional Tbit.

4.14.26 LIN0_LINRD0 Register (Offset = 64h) [reset = h]

Short Description: The LINRD0 register contains the lower 4 bytes of the received LIN frame data.

Long Description:

Return to Summary Table

Table 4-1419. Instance Table

Instance Name	Physical Address
LIN0	5240 0064h
LIN1	5240 1064h
LIN2	5240 2064h
LIN3	5240 3064h
LIN4	5240 4064h

Figure 4-677. LIN0_LINRD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD0								RD1							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD2								RD3							
RO								RO							
0								0							

Access Types Legend

Table 4-1420. LINRD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RD0	RO	0h	8-bit Receive Buffer 0[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.[[br]]A read of this byte clears the RXDY byte.[[br]]Note: RD
23 - 16	RD1	RO	0h	8-bit Receive Buffer 1.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15 - 8	RD2	RO	0h	8-bit Receive Buffer 2.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7 - 0	RD3	RO	0h	8-bit Receive Buffer 3.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

4.14.27 LIN0_LINRD1 Register (Offset = 68h) [reset = h]

Short Description: The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.

Long Description:

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Table 4-1421. Instance Table

Instance Name	Physical Address
LIN0	5240 0068h
LIN1	5240 1068h
LIN2	5240 2068h
LIN3	5240 3068h
LIN4	5240 4068h

Figure 4-678. LIN0_LINRD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD4								RD5							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD6								RD7							
RO								RO							
0								0							

Access Types Legend

Table 4-1422. LINRD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RD4	RO	0h	8-bit Receive Buffer 4 [[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
23 - 16	RD5	RO	0h	8-bit Receive Buffer 5.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15 - 8	RD6	RO	0h	8-bit Receive Buffer 6.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7 - 0	RD7	RO	0h	8-bit Receive Buffer 7.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

4.14.28 LIN0_LINMASK Register (Offset = 6Ch) [reset = h]

Short Description: The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.

Long Description:

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Table 4-1423. Instance Table

Instance Name	Physical Address
LIN0	5240 006Ch
LIN1	5240 106Ch
LIN2	5240 206Ch
LIN3	5240 306Ch
LIN4	5240 406Ch

Figure 4-679. LIN0_LINMASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2								RXIDMASK							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TXIDMASK							
RO								RW							
0								0							

Access Types Legend

Table 4-1424. LINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED_2	RO	0h	Reserved
23 - 16	RXIDMASK	RW	0h	Receive ID mask.[[br]]This field is effective in LIN mode only.This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID witht the RX ID mask will set the ID RX flag and trigger and ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare.[[br]] [[br]]When HGENCTRL is set to 1, this field must be set to 0xFF.
15 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	TXIDMASK	RW	0h	Transmit ID mask.[[br]]This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare.[[br]] [[br]]When HGENCTRL is set to 1, this field must be set to 0xFF.

4.14.29 LIN0_LINID Register (Offset = 70h) [reset = h]

Short Description: The LINID register contains the identification fields for LIN communication.[[br]]NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.

Long Description:

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Table 4-1425. Instance Table

Instance Name	Physical Address
LIN0	5240 0070h
LIN1	5240 1070h
LIN2	5240 2070h
LIN3	5240 3070h
LIN4	5240 4070h

Figure 4-680. LIN0_LINID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1								RECEIVEDID							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDSLAVETASKBYTE								IDBYTE							
RW								RW							
0								0							

Access Types Legend

Table 4-1426. LINID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED_1	RO	0h	Reserved
23 - 16	RECEIVEDID	RO	0h	Received ID.[[br]]This bit is effective in LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match.[[br]]Note: If a framing error (FE) is detected during ID reception, the received ID will also not be copied to the LINID register.
15 - 8	IDSLAVETASKBYTE	RW	0h	ID Slave Task byte.[[br]]This field is effective in LIN mode only. This byte contains the identifier to which the received ID of an incoming header will be compared in order to decide whether a RX response, a TX response, or no action needs to be done by the LIN node. [[br]] [[br]]These bits are writable in LIN mode only.
7 - 0	IDBYTE	RW	0h	ID byte.[[br]]This field is effective in LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a slave task, this byte is used for message filtering when HGENCTRL (SCIGCR1.12) is '0'.[[br]] [[br]]These bits are writable in LIN mode only.

4.14.30 LIN0_LINTD0 Register (Offset = 74h) [reset = h]

Short Description: The LINTD0 register contains the lower 4 bytes of the data to be transmitted.[[br]]NOTE: TD

Long Description:

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Table 4-1427. Instance Table

Instance Name	Physical Address
LIN0	5240 0074h
LIN1	5240 1074h
LIN2	5240 2074h
LIN3	5240 3074h
LIN4	5240 4074h

Figure 4-681. LIN0_LINTD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD0								TD1							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD2								TD3							
RW								RW							
0								0							

Access Types Legend

Table 4-1428. LINTD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TD0	RW	0h	8-bit Transmit Buffer 0.[[br]]Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated.
23 - 16	TD1	RW	0h	8-bit Transmit Buffer 3.[[br]]Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15 - 8	TD2	RW	0h	8-bit Transmit Buffer 2.[[br]]Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7 - 0	TD3	RW	0h	8-bit Transmit Buffer 3.[[br]]Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

4.14.31 LIN0_LINTD1 Register (Offset = 78h) [reset = h]

Short Description: The LINTD1 register contains the upper 4 bytes of the data to be transmitted.[[br]]NOTE: TD

Long Description:

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Table 4-1429. Instance Table

Instance Name	Physical Address
LIN0	5240 0078h
LIN1	5240 1078h
LIN2	5240 2078h
LIN3	5240 3078h
LIN4	5240 4078h

Figure 4-682. LIN0_LINTD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD4								TD5							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD6								TD7							
RW								RW							
0								0							

Access Types Legend

Table 4-1430. LINTD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TD4	RW	0h	8-bit Transmit Buffer 4.[[br]]Byte4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
23 - 16	TD5	RW	0h	8-bit Transmit Buffer 5.[[br]]Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15 - 8	TD6	RW	0h	8-bit Transmit Buffer 6.[[br]]Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7 - 0	TD7	RW	0h	8-bit Transmit Buffer 7.[[br]]Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

4.14.32 LIN0_MBRSR Register (Offset = 7Ch) [reset = h]

Short Description: The MBRSR register is used to configure the expected maximum baud rate of the LIN network.

Long Description:

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Table 4-1431. Instance Table

Instance Name	Physical Address
LIN0	5240 007Ch
LIN1	5240 107Ch
LIN2	5240 207Ch
LIN3	5240 307Ch
LIN4	5240 407Ch

Figure 4-683. LIN0_MBRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1			MBR												
RO			RW												
0			110110101100												

Access Types Legend

Table 4-1432. MBRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RESERVED_1	RO	0h	Reserved
12 - 0	MBR	RW	19A312CE6Ch	Maximum Baud Rate Prescaler.[[br]]This field is effective in LIN mode only. This 13-bit prescaler is used during the synchronization phase (see the "Header Reception and Adaptive Baudrate" section) of a slave module if the ADAPT bit is set. In this way, a SCI/LIN slave using an automatic or select bit rate modes detects any LIN bus legal rate automatically.[[br]] [[br]]The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could mistakenly be detected as sync break. [[br]]The default value is for a 70MHz LINCLK (0xDAC).[[br]]This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate.

4.14.33 LIN0_RESERVED_1 Register (Offset = 80h) [reset = h]

Short Description: RW

Long Description:

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Table 4-1433. Instance Table

Instance Name	Physical Address
LIN0	5240 0080h
LIN1	5240 1080h
LIN2	5240 2080h
LIN3	5240 3080h
LIN4	5240 4080h

Figure 4-684. LIN0_RESERVED_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BERRENA	PBERRENA	CERRENA	ISFERRENA	RESERVED_4	FERRENA	PERRENA	BRKDTERRENA	RESERVED_3			PINSAMPLEMASK		TXSHIFT		
RW	RW	RW	RW	RO	RW	RW	RW	RW			RW		RW		
0	0	0	0	0	0	0	0	0			0		0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2				IODFTENA				RESERVED_1						LPBENA	RXPENA
RO				RW				RO						RW	RW
0				101				0						0	0

Access Types Legend

Table 4-1434. RESERVED_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BERRENA	RW	0h	Bit Errror Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.
30	PBERRENA	RW	0h	Physical Bus Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Sync Break field transmission is ORed with 1 and passed to the Bit monitor circuitry
29	CERRENA	RW	0h	Checksum Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE (checksum type) in the receive checksum calculator is changed so that a checksum error is generated.
28	ISFERRENA	RW	0h	Inconsistent Sync Field Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create an ISF error. When this bit is set, the bit widths in the sync field are varied so that the ISF check fails and the error flag is set.
27	RESERVED_4	RO	0h	Reserved
26	FERRENA	RW	0h	This bit is used to create a Frame Error.[[br]]This bit is effective in SCI-compatible mode only. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.
25	PERRENA	RW	0h	Compatible Mode only[[br]]This bit is effective in SCI-compatible mode only. This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.

Table 4-1434. RESERVED_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	BRKDTERRENA	RW	0h	Compatible Mode only[[br]]This bit is effective in SCI-compatible mode only. This bit is used to create BRKDT error (SCI mode only). When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 Tbits so that a BRKDT error occurs.
23 - 21	RESERVED_3	RW	0h	Reserved
20 - 19	PINSAMPLEMASK	RW	0h	Pin sample mask.[[br]]These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry.[[br]]Note: During IODFT mode testing for the pin sample mask, the prescalar P must be programmed to be greater than 2. 0x0 | PINSAMPLEMASK_NONo Mask 0x1 | PINSAMPLEMASK_TBITInvert the TX Pin value at TBIT_CENTER 0x2 | PINSAMPLEMASK_SCLKInvert the TX Pin value at TBIT_CENTER + SCLK 0x3 | PINSAMPLEMASK_2SCLKInvert the TX Pin value at TBIT_CENTER + 2 SCLK
18 - 16	TXSHIFT	RW	0h	Transmit shift.[[br]]These bits define the delay by which the value on LINTX is delayed so that the value on LINRX is asynchronous. (Not applicable to Start Bit) 0x0 | TXSHIFT_DELAY_0No Delay 0x1 | TXSHIFT_DELAY_1Delay by 1 SCLK 0x2 | TXSHIFT_DELAY_2Delay by 2 SCLK 0x3 | TXSHIFT_DELAY_3Delay by 3 SCLK 0x4 | TXSHIFT_DELAY_4Delay by 4 SCLK 0x5 | TXSHIFT_DELAY_5Delay by 5 SCLK 0x6 | TXSHIFT_DELAY_6Delay by 6 SCLK 0x7 | TXSHIFT_DELAY_7Delay by 7 SCLK
15 - 12	RESERVED_2	RO	0h	Reserved
11 - 8	IODFTENA	RW	65h	IO DFT Enable Key[[br]]This field is used to enable the IODFT mode of the SCI/LIN module for testing. 0x0 | IODFTENA_DISABLE_0IODFT is disabled 0x1 | IODFTENA_DISABLE_1IODFT is disabled 0x2 | IODFTENA_DISABLE_2IODFT is disabled 0x3 | IODFTENA_DISABLE_3IODFT is disabled 0x4 | IODFTENA_DISABLE_4IODFT is disabled 0x5 | IODFTENA_DISABLE_5IODFT is disabled 0x6 | IODFTENA_DISABLE_6IODFT is disabled 0x7 | IODFTENA_DISABLE_7IODFT is disabled 0x8 | IODFTENA_DISABLE_8IODFT is disabled 0x9 | IODFTENA_DISABLE_9IODFT is disabled 0xA | IODFTENA_DISABLE_10IODFT is enabled 0xB | IODFTENA_DISABLE_11IODFT is disabled 0xC | IODFTENA_DISABLE_12IODFT is disabled 0xD | IODFTENA_DISABLE_13IODFT is disabled 0xE | IODFTENA_DISABLE_14IODFT is disabled 0xF | IODFTENA_DISABLE_15IODFT is disabled
7 - 2	RESERVED_1	RO	0h	Reserved
1	LPBENA	RW	0h	Module loopback enable.[[br]]In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path. 0 | LPBENA_DIGITALDigital loopback is enabled. 1 | LPBENA_ANALOGAnalog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)
0	RXPENA	RW	0h	Module Analog loopback through receive pin enable.[[br]]This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path in analog loopback mode only. 0 | RXPENA_TRANSMITAnalog loopback through the transmit pin is enabled. 1 | RXPENA_RECEIVEAnalog loopback through the receive pin is enabled.

4.14.34 LIN0_IODFTCTRL Register (Offset = 90h) [reset = h]

Short Description: The IODFTCTRL register is used to emulate various error and test conditions.

Long Description:

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Table 4-1435. Instance Table

Instance Name	Physical Address
LIN0	5240 0090h
LIN1	5240 1090h
LIN2	5240 2090h
LIN3	5240 3090h
LIN4	5240 4090h

Figure 4-685. LIN0_IODFTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														GLBINT1_EN	GLBINT0_EN
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1436. IODFTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	GLBINT1_EN	RW	0h	Global Interrupt Enable for LIN INT1.[[br]]This bit determines whether the INT1 interrupt line generates an interrupt to the PIE or not 0 | GLBINT1_DISABLEDLIN INT1 line does not generate an interrupt to the PIE. 1 | GLBINT1_ENABLEDLIN INT1 line generates an interrupt to the PIE if an enabled interrupt condition occurs.
0	GLBINT0_EN	RW	0h	Global Interrupt Enable for LIN INT0.[[br]]This bit determines whether the INT0 interrupt line generates an interrupt to the PIE or not. 0 | GLBINT0_DISABLEDLIN INT0 line does not generate an interrupt to the PIE. 1 | GLBINT0_ENABLEDLIN INT0 line generates an interrupt to the PIE if an enabled interrupt condition occurs.

4.14.35 LIN0_RESERVED_2 Register (Offset = 94h) [reset = h]

Short Description: RW

Long Description:

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Table 4-1437. Instance Table

Instance Name	Physical Address
LIN0	5240 0094h
LIN1	5240 1094h
LIN2	5240 2094h
LIN3	5240 3094h
LIN4	5240 4094h

Figure 4-686. LIN0_RESERVED_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG	INT0_FLG
RO														RO	RO
0														0	0

Access Types Legend

Table 4-1438. RESERVED_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	INT1_FLG	RO	0h	Global Interrupt Flag for LIN INT1.[[br]]This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT1 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.[[br]]This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. Read0 | INT1_FLG_NOT_GENERATEDNo interrupt is active on the INT1 line. Read1 | INT1_FLG_GENERATEDAn interrupt was generated due to an enabled interrupt on the INT1 interrupt line.
0	INT0_FLG	RO	0h	Global Interrupt Flag for LIN INT0.[[br]]This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT0 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.[[br]]This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. Read0 | INT0_FLG_NOT_GENERATEDNo interrupt is active on the INT0 line. Read1 | INT0_FLG_GENERATEDAn interrupt was generated due to an enabled interrupt on the INT0 interrupt line.

4.14.36 LIN0_LIN_GLB_INT_EN Register (Offset = E0h) [reset = h]

Short Description: The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.

Long Description:

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Table 4-1439. Instance Table

Instance Name	Physical Address
LIN0	5240 00E0h
LIN1	5240 10E0h
LIN2	5240 20E0h
LIN3	5240 30E0h
LIN4	5240 40E0h

Figure 4-687. LIN0_LIN_GLB_INT_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG_CLR	INT0_FLG_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1440. LIN_GLB_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	INT1_FLG_CLR	RW	0h	Global Interrupt flag clear for LIN INT1.[[br]]This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT1_FLG bit. Writing 0 has no effect.
0	INT0_FLG_CLR	RW	0h	Global Interrupt flag clear for LIN INT0.[[br]]This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT0_FLG bit. Writing 0 has no effect.

Table 4-1441. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.15 MSS_MBOX Registers

Table 4-1442. MBOX_SRAM, MBOX_SRAM_MBOX_SRAM Registers, Base Address=7200 0000H, Length=1

Offset	Length	Acronym	Register Name	MBOX_SRAM Physical Address
0h	32	MBOX_SRAM_START	RW	7200 0000h
3FFCh	32	MBOX_SRAM_END	RW	7200 3FFCh

4.15.1 MBOX_SRAM_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-1443. Instance Table

Instance Name	Physical Address
MBOX_SRAM	7200 0000h

Figure 4-688. MBOX_SRAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1444. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	L2 Memory start address

4.15.2 MBOX_SRAM_END Register (Offset = 3FFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1445. Instance Table

Instance Name	Physical Address
MBOX_SRAM	7200 3FFCh

Figure 4-689. MBOX_SRAM_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-1446. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	L2 Memory end address

Table 4-1447. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.16 MSS_MCAN_CFG Registers

Table 4-1448. MCAN0_CFG, MCAN0_CFG_MCAN0_CFG Registers, Base Address=5260 8000H, Length=7

Offset	Length	Acronym	Register Name	MCAN0_CFG Physical Address
0h	32	MCAN0_CFG_SS_PID	SS_PID	5260 8000h
4h	32	MCAN0_CFG_SS_CTRL	SS_CTRL	5260 8004h
8h	32	MCAN0_CFG_SS_STAT	SS_STAT	5260 8008h
Ch	32	MCAN0_CFG_SS_ICS	SS_ICS	5260 800Ch
10h	32	MCAN0_CFG_SS_IRS	SS_IRS	5260 8010h
14h	32	MCAN0_CFG_SS_IECS	SS_IECS	5260 8014h
18h	32	MCAN0_CFG_SS_IE	SS_IE	5260 8018h
1Ch	32	MCAN0_CFG_SS_IES	SS_IES	5260 801Ch
20h	32	MCAN0_CFG_SS_EOI	SS_EOI	5260 8020h
24h	32	MCAN0_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS	5260 8024h
28h	32	MCAN0_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC	5260 8028h
200h	32	MCAN0_CFG_CREL	CREL	5260 8200h
204h	32	MCAN0_CFG_ENDN	ENDN	5260 8204h
208h	32	MCAN0_CFG_CUST	CUST	5260 8208h
20Ch	32	MCAN0_CFG_DBTP	DBTP	5260 820Ch
210h	32	MCAN0_CFG_TEST	TEST	5260 8210h
214h	32	MCAN0_CFG_RWD	RWD	5260 8214h
218h	32	MCAN0_CFG_CCCR	CCCR	5260 8218h
21Ch	32	MCAN0_CFG_NBTP	NBTP	5260 821Ch
220h	32	MCAN0_CFG_TSCC	TSCC	5260 8220h
224h	32	MCAN0_CFG_TSCV	TSCV	5260 8224h
228h	32	MCAN0_CFG_TOCC	TOCC	5260 8228h
22Ch	32	MCAN0_CFG_TOCV	TOCV	5260 822Ch
230h	32	MCAN0_CFG_RES00	RES00	5260 8230h
234h	32	MCAN0_CFG_RES01	RES01	5260 8234h
238h	32	MCAN0_CFG_RES02	RES02	5260 8238h
23Ch	32	MCAN0_CFG_RES03	RES03	5260 823Ch
240h	32	MCAN0_CFG_ECR	ECR	5260 8240h
244h	32	MCAN0_CFG_PSR	PSR	5260 8244h
248h	32	MCAN0_CFG_TDCR	TDCR	5260 8248h
24Ch	32	MCAN0_CFG_RES04	RES04	5260 824Ch
250h	32	MCAN0_CFG_IR	IR	5260 8250h
254h	32	MCAN0_CFG_IE	IE	5260 8254h
258h	32	MCAN0_CFG_ILS	ILS	5260 8258h
25Ch	32	MCAN0_CFG_ILE	ILE	5260 825Ch
260h	32	MCAN0_CFG_RES05	RES05	5260 8260h
264h	32	MCAN0_CFG_RES06	RES06	5260 8264h
268h	32	MCAN0_CFG_RES07	RES07	5260 8268h
26Ch	32	MCAN0_CFG_RES08	RES08	5260 826Ch
270h	32	MCAN0_CFG_RES09	RES09	5260 8270h
274h	32	MCAN0_CFG_RES10	RES10	5260 8274h

Table 4-1448. MCAN0_CFG, MCAN0_CFG_MCAN0_CFG Registers, Base Address=5260 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN0_CFG Physical Address
278h	32	MCAN0_CFG_RES11	RES11	5260 8278h
27Ch	32	MCAN0_CFG_RES12	RES12	5260 827Ch
280h	32	MCAN0_CFG_GFC	GFC	5260 8280h
284h	32	MCAN0_CFG_SIDFC	SIDFC	5260 8284h
288h	32	MCAN0_CFG_XIDFC	XIDFC	5260 8288h
28Ch	32	MCAN0_CFG_RES13	RES13	5260 828Ch
290h	32	MCAN0_CFG_XIDAM	XIDAM	5260 8290h
294h	32	MCAN0_CFG_HPMS	HPMS	5260 8294h
298h	32	MCAN0_CFG_NDAT1	NDAT1	5260 8298h
29Ch	32	MCAN0_CFG_NDAT2	NDAT2	5260 829Ch
2A0h	32	MCAN0_CFG_RXF0C	RXF0C	5260 82A0h
2A4h	32	MCAN0_CFG_RXF0S	RXF0S	5260 82A4h
2A8h	32	MCAN0_CFG_RXF0A	RXF0A	5260 82A8h
2ACh	32	MCAN0_CFG_RXBC	RXBC	5260 82ACh
2B0h	32	MCAN0_CFG_RXF1C	RXF1C	5260 82B0h
2B4h	32	MCAN0_CFG_RXF1S	RXF1S	5260 82B4h
2B8h	32	MCAN0_CFG_RXF1A	RXF1A	5260 82B8h
2BCh	32	MCAN0_CFG_RXESC	RXESC	5260 82BCh
2C0h	32	MCAN0_CFG_TXBC	TXBC	5260 82C0h
2C4h	32	MCAN0_CFG_TXFQS	TXFQS	5260 82C4h
2C8h	32	MCAN0_CFG_TXESC	TXESC	5260 82C8h
2CCh	32	MCAN0_CFG_TXBRP	TXBRP	5260 82CCh
2D0h	32	MCAN0_CFG_TXBAR	TXBAR	5260 82D0h
2D4h	32	MCAN0_CFG_TXBCR	TXBCR	5260 82D4h
2D8h	32	MCAN0_CFG_TXBTO	TXBTO	5260 82D8h
2DCh	32	MCAN0_CFG_TXBCF	TXBCF	5260 82DCh
2E0h	32	MCAN0_CFG_TXBTIE	TXBTIE	5260 82E0h
2E4h	32	MCAN0_CFG_TXBCIE	TXBCIE	5260 82E4h
2E8h	32	MCAN0_CFG_RES14	RES14	5260 82E8h
2ECh	32	MCAN0_CFG_RES15	RES15	5260 82ECh
2F0h	32	MCAN0_CFG_TXEFC	TXEFC	5260 82F0h
2F4h	32	MCAN0_CFG_TXEFS	TXEFS	5260 82F4h
2F8h	32	MCAN0_CFG_TXEFA	TXEFA	5260 82F8h
2FCh	32	MCAN0_CFG_RES16	RES16	5260 82FCh

Table 4-1449. MCAN0_CFG, MCAN0_CFG_MCAN0_CFG Registers, Base Address=5260 8000H, Length=7

Offset	Length	Acronym	Register Name
0h	32	MCAN0_CFG_SS_PID	SS_PID
4h	32	MCAN0_CFG_SS_CTRL	SS_CTRL
8h	32	MCAN0_CFG_SS_STAT	SS_STAT
Ch	32	MCAN0_CFG_SS_ICS	SS_ICS
10h	32	MCAN0_CFG_SS_IRS	SS_IRS
14h	32	MCAN0_CFG_SS_IECS	SS_IECS
18h	32	MCAN0_CFG_SS_IE	SS_IE
1Ch	32	MCAN0_CFG_SS_IES	SS_IES

Table 4-1449. MCAN0_CFG, MCAN0_CFG_MCAN0_CFG Registers, Base Address=5260 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
20h	32	MCAN0_CFG_SS_EOI	SS_EOI
24h	32	MCAN0_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS
28h	32	MCAN0_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC
200h	32	MCAN0_CFG_CREL	CREL
204h	32	MCAN0_CFG_ENDN	ENDN
208h	32	MCAN0_CFG_CUST	CUST
20Ch	32	MCAN0_CFG_DBTP	DBTP
210h	32	MCAN0_CFG_TEST	TEST
214h	32	MCAN0_CFG_RWD	RWD
218h	32	MCAN0_CFG_CCCR	CCCR
21Ch	32	MCAN0_CFG_NBTP	NBTP
220h	32	MCAN0_CFG_TSCC	TSCC
224h	32	MCAN0_CFG_TSCV	TSCV
228h	32	MCAN0_CFG_TOCC	TOCC
22Ch	32	MCAN0_CFG_TOCV	TOCV
230h	32	MCAN0_CFG_RES00	RES00
234h	32	MCAN0_CFG_RES01	RES01
238h	32	MCAN0_CFG_RES02	RES02
23Ch	32	MCAN0_CFG_RES03	RES03
240h	32	MCAN0_CFG_ECR	ECR
244h	32	MCAN0_CFG_PSR	PSR
248h	32	MCAN0_CFG_TDCR	TDCR
24Ch	32	MCAN0_CFG_RES04	RES04
250h	32	MCAN0_CFG_IR	IR
254h	32	MCAN0_CFG_IE	IE
258h	32	MCAN0_CFG_ILS	ILS
25Ch	32	MCAN0_CFG_ILE	ILE
260h	32	MCAN0_CFG_RES05	RES05
264h	32	MCAN0_CFG_RES06	RES06
268h	32	MCAN0_CFG_RES07	RES07
26Ch	32	MCAN0_CFG_RES08	RES08
270h	32	MCAN0_CFG_RES09	RES09
274h	32	MCAN0_CFG_RES10	RES10
278h	32	MCAN0_CFG_RES11	RES11
27Ch	32	MCAN0_CFG_RES12	RES12
280h	32	MCAN0_CFG_GFC	GFC
284h	32	MCAN0_CFG_SIDFC	SIDFC
288h	32	MCAN0_CFG_XIDFC	XIDFC
28Ch	32	MCAN0_CFG_RES13	RES13
290h	32	MCAN0_CFG_XIDAM	XIDAM
294h	32	MCAN0_CFG_HPMS	HPMS
298h	32	MCAN0_CFG_NDAT1	NDAT1
29Ch	32	MCAN0_CFG_NDAT2	NDAT2
2A0h	32	MCAN0_CFG_RXF0C	RXF0C
2A4h	32	MCAN0_CFG_RXF0S	RXF0S
2A8h	32	MCAN0_CFG_RXF0A	RXF0A

Table 4-1449. MCAN0_CFG, MCAN0_CFG_MCAN0_CFG Registers, Base Address=5260 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
2ACh	32	MCAN0_CFG_RXBC	RXBC
2B0h	32	MCAN0_CFG_RXF1C	RXF1C
2B4h	32	MCAN0_CFG_RXF1S	RXF1S
2B8h	32	MCAN0_CFG_RXF1A	RXF1A
2BCh	32	MCAN0_CFG_RXESC	RXESC
2C0h	32	MCAN0_CFG_TXBC	TXBC
2C4h	32	MCAN0_CFG_TXFQS	TXFQS
2C8h	32	MCAN0_CFG_TXESC	TXESC
2CCh	32	MCAN0_CFG_TXBRP	TXBRP
2D0h	32	MCAN0_CFG_TXBAR	TXBAR
2D4h	32	MCAN0_CFG_TXBCR	TXBCR
2D8h	32	MCAN0_CFG_TXBTO	TXBTO
2DCh	32	MCAN0_CFG_TXBCF	TXBCF
2E0h	32	MCAN0_CFG_TXBTIE	TXBTIE
2E4h	32	MCAN0_CFG_TXBCIE	TXBCIE
2E8h	32	MCAN0_CFG_RES14	RES14
2ECh	32	MCAN0_CFG_RES15	RES15
2F0h	32	MCAN0_CFG_TXEFC	TXEFC
2F4h	32	MCAN0_CFG_TXEFS	TXEFS
2F8h	32	MCAN0_CFG_TXEFA	TXEFA
2FCh	32	MCAN0_CFG_RES16	RES16

Table 4-1450. MCAN1_MSG_RAM, MCAN1_MSG_RAM_MCAN1_MSG_RAM Registers, Base Address=5261 0000H, Length=3

Offset	Length	Acronym	Register Name	MCAN1_MSG_RAM Physical Address
0h	32	MCAN1_MSG_RAM_START	START	5261 0000h

Table 4-1451. MCAN1_MSG_RAM, MCAN1_MSG_RAM_MCAN1_MSG_RAM Registers, Base Address=5261 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	MCAN1_MSG_RAM_START	START

Table 4-1452. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7

Offset	Length	Acronym	Register Name	MCAN1_CFG Physical Address
0h	32	MCAN1_CFG_SS_PID	SS_PID	5261 8000h
4h	32	MCAN1_CFG_SS_CTRL	SS_CTRL	5261 8004h
8h	32	MCAN1_CFG_SS_STAT	SS_STAT	5261 8008h
Ch	32	MCAN1_CFG_SS_ICS	SS_ICS	5261 800Ch
10h	32	MCAN1_CFG_SS_IRS	SS_IRS	5261 8010h
14h	32	MCAN1_CFG_SS_IECS	SS_IECS	5261 8014h
18h	32	MCAN1_CFG_SS_IE	SS_IE	5261 8018h
1Ch	32	MCAN1_CFG_SS_IES	SS_IES	5261 801Ch
20h	32	MCAN1_CFG_SS_EOI	SS_EOI	5261 8020h
24h	32	MCAN1_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS	5261 8024h

Table 4-1452. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN1_CFG Physical Address
28h	32	MCAN1_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC	5261 8028h
200h	32	MCAN1_CFG_CREL	CREL	5261 8200h
204h	32	MCAN1_CFG_ENDN	ENDN	5261 8204h
208h	32	MCAN1_CFG_CUST	CUST	5261 8208h
20Ch	32	MCAN1_CFG_DBTP	DBTP	5261 820Ch
210h	32	MCAN1_CFG_TEST	TEST	5261 8210h
214h	32	MCAN1_CFG_RWD	RWD	5261 8214h
218h	32	MCAN1_CFG_CCCR	CCCR	5261 8218h
21Ch	32	MCAN1_CFG_NBTP	NBTP	5261 821Ch
220h	32	MCAN1_CFG_TSCC	TSCC	5261 8220h
224h	32	MCAN1_CFG_TSCV	TSCV	5261 8224h
228h	32	MCAN1_CFG_TOCC	TOCC	5261 8228h
22Ch	32	MCAN1_CFG_TOCV	TOCV	5261 822Ch
230h	32	MCAN1_CFG_RES00	RES00	5261 8230h
234h	32	MCAN1_CFG_RES01	RES01	5261 8234h
238h	32	MCAN1_CFG_RES02	RES02	5261 8238h
23Ch	32	MCAN1_CFG_RES03	RES03	5261 823Ch
240h	32	MCAN1_CFG_ECR	ECR	5261 8240h
244h	32	MCAN1_CFG_PSR	PSR	5261 8244h
248h	32	MCAN1_CFG_TDCR	TDCR	5261 8248h
24Ch	32	MCAN1_CFG_RES04	RES04	5261 824Ch
250h	32	MCAN1_CFG_IR	IR	5261 8250h
254h	32	MCAN1_CFG_IE	IE	5261 8254h
258h	32	MCAN1_CFG_ILS	ILS	5261 8258h
25Ch	32	MCAN1_CFG_ILE	ILE	5261 825Ch
260h	32	MCAN1_CFG_RES05	RES05	5261 8260h
264h	32	MCAN1_CFG_RES06	RES06	5261 8264h
268h	32	MCAN1_CFG_RES07	RES07	5261 8268h
26Ch	32	MCAN1_CFG_RES08	RES08	5261 826Ch
270h	32	MCAN1_CFG_RES09	RES09	5261 8270h
274h	32	MCAN1_CFG_RES10	RES10	5261 8274h
278h	32	MCAN1_CFG_RES11	RES11	5261 8278h
27Ch	32	MCAN1_CFG_RES12	RES12	5261 827Ch
280h	32	MCAN1_CFG_GFC	GFC	5261 8280h
284h	32	MCAN1_CFG_SIDFC	SIDFC	5261 8284h
288h	32	MCAN1_CFG_XIDFC	XIDFC	5261 8288h
28Ch	32	MCAN1_CFG_RES13	RES13	5261 828Ch
290h	32	MCAN1_CFG_XIDAM	XIDAM	5261 8290h
294h	32	MCAN1_CFG_HPMS	HPMS	5261 8294h
298h	32	MCAN1_CFG_NDAT1	NDAT1	5261 8298h
29Ch	32	MCAN1_CFG_NDAT2	NDAT2	5261 829Ch
2A0h	32	MCAN1_CFG_RXF0C	RXF0C	5261 82A0h
2A4h	32	MCAN1_CFG_RXF0S	RXF0S	5261 82A4h
2A8h	32	MCAN1_CFG_RXF0A	RXF0A	5261 82A8h
2ACh	32	MCAN1_CFG_RXBC	RXBC	5261 82ACh
2B0h	32	MCAN1_CFG_RXF1C	RXF1C	5261 82B0h

Table 4-1452. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN1_CFG Physical Address
2B4h	32	MCAN1_CFG_RXF1S	RXF1S	5261 82B4h
2B8h	32	MCAN1_CFG_RXF1A	RXF1A	5261 82B8h
2BCh	32	MCAN1_CFG_RXESC	RXESC	5261 82BCh
2C0h	32	MCAN1_CFG_TXBC	TXBC	5261 82C0h
2C4h	32	MCAN1_CFG_TXFQS	TXFQS	5261 82C4h
2C8h	32	MCAN1_CFG_TXESC	TXESC	5261 82C8h
2CCh	32	MCAN1_CFG_TXBRP	TXBRP	5261 82CCh
2D0h	32	MCAN1_CFG_TXBAR	TXBAR	5261 82D0h
2D4h	32	MCAN1_CFG_TXBCR	TXBCR	5261 82D4h
2D8h	32	MCAN1_CFG_TXBTO	TXBTO	5261 82D8h
2DCh	32	MCAN1_CFG_TXBCF	TXBCF	5261 82DCh
2E0h	32	MCAN1_CFG_TXBTIE	TXBTIE	5261 82E0h
2E4h	32	MCAN1_CFG_TXBCIE	TXBCIE	5261 82E4h
2E8h	32	MCAN1_CFG_RES14	RES14	5261 82E8h
2ECh	32	MCAN1_CFG_RES15	RES15	5261 82ECh
2F0h	32	MCAN1_CFG_TXEFC	TXEFC	5261 82F0h
2F4h	32	MCAN1_CFG_TXEFS	TXEFS	5261 82F4h
2F8h	32	MCAN1_CFG_TXEFA	TXEFA	5261 82F8h
2FCh	32	MCAN1_CFG_RES16	RES16	5261 82FCh

Table 4-1453. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7

Offset	Length	Acronym	Register Name
0h	32	MCAN1_CFG_SS_PID	SS_PID
4h	32	MCAN1_CFG_SS_CTRL	SS_CTRL
8h	32	MCAN1_CFG_SS_STAT	SS_STAT
Ch	32	MCAN1_CFG_SS_ICS	SS_ICS
10h	32	MCAN1_CFG_SS_IRS	SS_IRS
14h	32	MCAN1_CFG_SS_IECS	SS_IECS
18h	32	MCAN1_CFG_SS_IE	SS_IE
1Ch	32	MCAN1_CFG_SS_IES	SS_IES
20h	32	MCAN1_CFG_SS_EOI	SS_EOI
24h	32	MCAN1_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS
28h	32	MCAN1_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC
200h	32	MCAN1_CFG_CREL	CREL
204h	32	MCAN1_CFG_ENDN	ENDN
208h	32	MCAN1_CFG_CUST	CUST
20Ch	32	MCAN1_CFG_DBTP	DBTP
210h	32	MCAN1_CFG_TEST	TEST
214h	32	MCAN1_CFG_RWD	RWD
218h	32	MCAN1_CFG_CCCR	CCCR
21Ch	32	MCAN1_CFG_NBTP	NBTP
220h	32	MCAN1_CFG_TSCC	TSCC
224h	32	MCAN1_CFG_TSCV	TSCV
228h	32	MCAN1_CFG_TOCC	TOCC
22Ch	32	MCAN1_CFG_TOCV	TOCV

Table 4-1453. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
230h	32	MCAN1_CFG_RES00	RES00
234h	32	MCAN1_CFG_RES01	RES01
238h	32	MCAN1_CFG_RES02	RES02
23Ch	32	MCAN1_CFG_RES03	RES03
240h	32	MCAN1_CFG_ECR	ECR
244h	32	MCAN1_CFG_PSR	PSR
248h	32	MCAN1_CFG_TDCR	TDCR
24Ch	32	MCAN1_CFG_RES04	RES04
250h	32	MCAN1_CFG_IR	IR
254h	32	MCAN1_CFG_IE	IE
258h	32	MCAN1_CFG_ILS	ILS
25Ch	32	MCAN1_CFG_ILE	ILE
260h	32	MCAN1_CFG_RES05	RES05
264h	32	MCAN1_CFG_RES06	RES06
268h	32	MCAN1_CFG_RES07	RES07
26Ch	32	MCAN1_CFG_RES08	RES08
270h	32	MCAN1_CFG_RES09	RES09
274h	32	MCAN1_CFG_RES10	RES10
278h	32	MCAN1_CFG_RES11	RES11
27Ch	32	MCAN1_CFG_RES12	RES12
280h	32	MCAN1_CFG_GFC	GFC
284h	32	MCAN1_CFG_SIDFC	SIDFC
288h	32	MCAN1_CFG_XIDFC	XIDFC
28Ch	32	MCAN1_CFG_RES13	RES13
290h	32	MCAN1_CFG_XIDAM	XIDAM
294h	32	MCAN1_CFG_HPMS	HPMS
298h	32	MCAN1_CFG_NDAT1	NDAT1
29Ch	32	MCAN1_CFG_NDAT2	NDAT2
2A0h	32	MCAN1_CFG_RXF0C	RXF0C
2A4h	32	MCAN1_CFG_RXF0S	RXF0S
2A8h	32	MCAN1_CFG_RXF0A	RXF0A
2ACh	32	MCAN1_CFG_RXBC	RXBC
2B0h	32	MCAN1_CFG_RXF1C	RXF1C
2B4h	32	MCAN1_CFG_RXF1S	RXF1S
2B8h	32	MCAN1_CFG_RXF1A	RXF1A
2BCh	32	MCAN1_CFG_RXESC	RXESC
2C0h	32	MCAN1_CFG_TXBC	TXBC
2C4h	32	MCAN1_CFG_TXFQS	TXFQS
2C8h	32	MCAN1_CFG_TXESC	TXESC
2CCh	32	MCAN1_CFG_TXBRP	TXBRP
2D0h	32	MCAN1_CFG_TXBAR	TXBAR
2D4h	32	MCAN1_CFG_TXBCR	TXBCR
2D8h	32	MCAN1_CFG_TXBTO	TXBTO
2DCh	32	MCAN1_CFG_TXBCF	TXBCF
2E0h	32	MCAN1_CFG_TXBTIE	TXBTIE
2E4h	32	MCAN1_CFG_TXBCIE	TXBCIE

Table 4-1453. MCAN1_CFG, MCAN1_CFG_MCAN1_CFG Registers, Base Address=5261 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
2E8h	32	MCAN1_CFG_RES14	RES14
2ECh	32	MCAN1_CFG_RES15	RES15
2F0h	32	MCAN1_CFG_TXEFC	TXEFC
2F4h	32	MCAN1_CFG_TXEFS	TXEFS
2F8h	32	MCAN1_CFG_TXEFA	TXEFA
2FCh	32	MCAN1_CFG_RES16	RES16

Table 4-1454. MCAN2_MSG_RAM, MCAN2_MSG_RAM_MCAN2_MSG_RAM Registers, Base Address=5262 0000H, Length=3

Offset	Length	Acronym	Register Name	MCAN2_MSG_RAM Physical Address
0h	32	MCAN2_MSG_RAM_START	START	5262 0000h

Table 4-1455. MCAN2_MSG_RAM, MCAN2_MSG_RAM_MCAN2_MSG_RAM Registers, Base Address=5262 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	MCAN2_MSG_RAM_START	START

Table 4-1456. MCAN2_CFG, MCAN2_CFG_MCAN2_CFG Registers, Base Address=5262 8000H, Length=7

Offset	Length	Acronym	Register Name	MCAN2_CFG Physical Address
0h	32	MCAN2_CFG_SS_PID	SS_PID	5262 8000h
4h	32	MCAN2_CFG_SS_CTRL	SS_CTRL	5262 8004h
8h	32	MCAN2_CFG_SS_STAT	SS_STAT	5262 8008h
Ch	32	MCAN2_CFG_SS_ICS	SS_ICS	5262 800Ch
10h	32	MCAN2_CFG_SS_IRS	SS_IRS	5262 8010h
14h	32	MCAN2_CFG_SS_IECS	SS_IECS	5262 8014h
18h	32	MCAN2_CFG_SS_IE	SS_IE	5262 8018h
1Ch	32	MCAN2_CFG_SS_IES	SS_IES	5262 801Ch
20h	32	MCAN2_CFG_SS_EOI	SS_EOI	5262 8020h
24h	32	MCAN2_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS	5262 8024h
28h	32	MCAN2_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC	5262 8028h
200h	32	MCAN2_CFG_CREL	CREL	5262 8200h
204h	32	MCAN2_CFG_ENDN	ENDN	5262 8204h
208h	32	MCAN2_CFG_CUST	CUST	5262 8208h
20Ch	32	MCAN2_CFG_DBTP	DBTP	5262 820Ch
210h	32	MCAN2_CFG_TEST	TEST	5262 8210h
214h	32	MCAN2_CFG_RWD	RWD	5262 8214h
218h	32	MCAN2_CFG_CCCR	CCCR	5262 8218h
21Ch	32	MCAN2_CFG_NBTP	NBTP	5262 821Ch
220h	32	MCAN2_CFG_TSCC	TSCC	5262 8220h
224h	32	MCAN2_CFG_TSCV	TSCV	5262 8224h
228h	32	MCAN2_CFG_TOCC	TOCC	5262 8228h
22Ch	32	MCAN2_CFG_TOCV	TOCV	5262 822Ch
230h	32	MCAN2_CFG_RES00	RES00	5262 8230h
234h	32	MCAN2_CFG_RES01	RES01	5262 8234h

Table 4-1456. MCAN2_CFG, MCAN2_CFG_MCAN2_CFG Registers, Base Address=5262 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN2_CFG Physical Address
238h	32	MCAN2_CFG_RES02	RES02	5262 8238h
23Ch	32	MCAN2_CFG_RES03	RES03	5262 823Ch
240h	32	MCAN2_CFG_ECR	ECR	5262 8240h
244h	32	MCAN2_CFG_PSR	PSR	5262 8244h
248h	32	MCAN2_CFG_TDCR	TDCR	5262 8248h
24Ch	32	MCAN2_CFG_RES04	RES04	5262 824Ch
250h	32	MCAN2_CFG_IR	IR	5262 8250h
254h	32	MCAN2_CFG_IE	IE	5262 8254h
258h	32	MCAN2_CFG_ILS	ILS	5262 8258h
25Ch	32	MCAN2_CFG_ILE	ILE	5262 825Ch
260h	32	MCAN2_CFG_RES05	RES05	5262 8260h
264h	32	MCAN2_CFG_RES06	RES06	5262 8264h
268h	32	MCAN2_CFG_RES07	RES07	5262 8268h
26Ch	32	MCAN2_CFG_RES08	RES08	5262 826Ch
270h	32	MCAN2_CFG_RES09	RES09	5262 8270h
274h	32	MCAN2_CFG_RES10	RES10	5262 8274h
278h	32	MCAN2_CFG_RES11	RES11	5262 8278h
27Ch	32	MCAN2_CFG_RES12	RES12	5262 827Ch
280h	32	MCAN2_CFG_GFC	GFC	5262 8280h
284h	32	MCAN2_CFG_SIDFC	SIDFC	5262 8284h
288h	32	MCAN2_CFG_XIDFC	XIDFC	5262 8288h
28Ch	32	MCAN2_CFG_RES13	RES13	5262 828Ch
290h	32	MCAN2_CFG_XIDAM	XIDAM	5262 8290h
294h	32	MCAN2_CFG_HPMS	HPMS	5262 8294h
298h	32	MCAN2_CFG_NDAT1	NDAT1	5262 8298h
29Ch	32	MCAN2_CFG_NDAT2	NDAT2	5262 829Ch
2A0h	32	MCAN2_CFG_RXF0C	RXF0C	5262 82A0h
2A4h	32	MCAN2_CFG_RXF0S	RXF0S	5262 82A4h
2A8h	32	MCAN2_CFG_RXF0A	RXF0A	5262 82A8h
2ACh	32	MCAN2_CFG_RXBC	RXBC	5262 82ACh
2B0h	32	MCAN2_CFG_RXF1C	RXF1C	5262 82B0h
2B4h	32	MCAN2_CFG_RXF1S	RXF1S	5262 82B4h
2B8h	32	MCAN2_CFG_RXF1A	RXF1A	5262 82B8h
2BCh	32	MCAN2_CFG_RXESC	RXESC	5262 82BCh
2C0h	32	MCAN2_CFG_TXBC	TXBC	5262 82C0h
2C4h	32	MCAN2_CFG_TXFQS	TXFQS	5262 82C4h
2C8h	32	MCAN2_CFG_TXESC	TXESC	5262 82C8h
2CCh	32	MCAN2_CFG_TXBRP	TXBRP	5262 82CCh
2D0h	32	MCAN2_CFG_TXBAR	TXBAR	5262 82D0h
2D4h	32	MCAN2_CFG_TXBCR	TXBCR	5262 82D4h
2D8h	32	MCAN2_CFG_TXBTO	TXBTO	5262 82D8h
2DCh	32	MCAN2_CFG_TXBCF	TXBCF	5262 82DCh
2E0h	32	MCAN2_CFG_TXBTIE	TXBTIE	5262 82E0h
2E4h	32	MCAN2_CFG_TXBCIE	TXBCIE	5262 82E4h
2E8h	32	MCAN2_CFG_RES14	RES14	5262 82E8h
2ECh	32	MCAN2_CFG_RES15	RES15	5262 82ECh

Table 4-1456. MCAN2_CFG, MCAN2_CFG_MCAN2_CFG Registers, Base Address=5262 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN2_CFG Physical Address
2F0h	32	MCAN2_CFG_TXEFC	TXEFC	5262 82F0h
2F4h	32	MCAN2_CFG_TXEFS	TXEFS	5262 82F4h
2F8h	32	MCAN2_CFG_TXEFA	TXEFA	5262 82F8h
2FCh	32	MCAN2_CFG_RES16	RES16	5262 82FCh

Table 4-1457. MCAN2_CFG, MCAN2_CFG_MCAN2_CFG Registers, Base Address=5262 8000H, Length=7

Offset	Length	Acronym	Register Name
0h	32	MCAN2_CFG_SS_PID	SS_PID
4h	32	MCAN2_CFG_SS_CTRL	SS_CTRL
8h	32	MCAN2_CFG_SS_STAT	SS_STAT
Ch	32	MCAN2_CFG_SS_ICS	SS_ICS
10h	32	MCAN2_CFG_SS_IRS	SS_IRS
14h	32	MCAN2_CFG_SS_IECS	SS_IECS
18h	32	MCAN2_CFG_SS_IE	SS_IE
1Ch	32	MCAN2_CFG_SS_IES	SS_IES
20h	32	MCAN2_CFG_SS_EOI	SS_EOI
24h	32	MCAN2_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS
28h	32	MCAN2_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC
200h	32	MCAN2_CFG_CREL	CREL
204h	32	MCAN2_CFG_ENDN	ENDN
208h	32	MCAN2_CFG_CUST	CUST
20Ch	32	MCAN2_CFG_DBTP	DBTP
210h	32	MCAN2_CFG_TEST	TEST
214h	32	MCAN2_CFG_RWD	RWD
218h	32	MCAN2_CFG_CCCR	CCCR
21Ch	32	MCAN2_CFG_NBTP	NBTP
220h	32	MCAN2_CFG_TSCC	TSCC
224h	32	MCAN2_CFG_TSCV	TSCV
228h	32	MCAN2_CFG_TOCC	TOCC
22Ch	32	MCAN2_CFG_TOCV	TOCV
230h	32	MCAN2_CFG_RES00	RES00
234h	32	MCAN2_CFG_RES01	RES01
238h	32	MCAN2_CFG_RES02	RES02
23Ch	32	MCAN2_CFG_RES03	RES03
240h	32	MCAN2_CFG_ECR	ECR
244h	32	MCAN2_CFG_PSR	PSR
248h	32	MCAN2_CFG_TDCR	TDCR
24Ch	32	MCAN2_CFG_RES04	RES04
250h	32	MCAN2_CFG_IR	IR
254h	32	MCAN2_CFG_IE	IE
258h	32	MCAN2_CFG_ILS	ILS
25Ch	32	MCAN2_CFG_ILE	ILE
260h	32	MCAN2_CFG_RES05	RES05
264h	32	MCAN2_CFG_RES06	RES06
268h	32	MCAN2_CFG_RES07	RES07

Table 4-1457. MCAN2_CFG, MCAN2_CFG_MCAN2_CFG Registers, Base Address=5262 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
26Ch	32	MCAN2_CFG_RES08	RES08
270h	32	MCAN2_CFG_RES09	RES09
274h	32	MCAN2_CFG_RES10	RES10
278h	32	MCAN2_CFG_RES11	RES11
27Ch	32	MCAN2_CFG_RES12	RES12
280h	32	MCAN2_CFG_GFC	GFC
284h	32	MCAN2_CFG_SIDFC	SIDFC
288h	32	MCAN2_CFG_XIDFC	XIDFC
28Ch	32	MCAN2_CFG_RES13	RES13
290h	32	MCAN2_CFG_XIDAM	XIDAM
294h	32	MCAN2_CFG_HPMS	HPMS
298h	32	MCAN2_CFG_NDAT1	NDAT1
29Ch	32	MCAN2_CFG_NDAT2	NDAT2
2A0h	32	MCAN2_CFG_RXF0C	RXF0C
2A4h	32	MCAN2_CFG_RXF0S	RXF0S
2A8h	32	MCAN2_CFG_RXF0A	RXF0A
2ACh	32	MCAN2_CFG_RXBC	RXBC
2B0h	32	MCAN2_CFG_RXF1C	RXF1C
2B4h	32	MCAN2_CFG_RXF1S	RXF1S
2B8h	32	MCAN2_CFG_RXF1A	RXF1A
2BCh	32	MCAN2_CFG_RXESC	RXESC
2C0h	32	MCAN2_CFG_TXBC	TXBC
2C4h	32	MCAN2_CFG_TXFQS	TXFQS
2C8h	32	MCAN2_CFG_TXESC	TXESC
2CCh	32	MCAN2_CFG_TXBRP	TXBRP
2D0h	32	MCAN2_CFG_TXBAR	TXBAR
2D4h	32	MCAN2_CFG_TXBCR	TXBCR
2D8h	32	MCAN2_CFG_TXBTO	TXBTO
2DCh	32	MCAN2_CFG_TXBCF	TXBCF
2E0h	32	MCAN2_CFG_TXBTIE	TXBTIE
2E4h	32	MCAN2_CFG_TXBCIE	TXBCIE
2E8h	32	MCAN2_CFG_RES14	RES14
2ECh	32	MCAN2_CFG_RES15	RES15
2F0h	32	MCAN2_CFG_TXEFC	TXEFC
2F4h	32	MCAN2_CFG_TXEFS	TXEFS
2F8h	32	MCAN2_CFG_TXEFA	TXEFA
2FCh	32	MCAN2_CFG_RES16	RES16

Table 4-1458. MCAN3_MSG_RAM, MCAN3_MSG_RAM_MCAN3_MSG_RAM Registers, Base Address=5263 0000H, Length=3

Offset	Length	Acronym	Register Name	MCAN3_MSG_RAM Physical Address
0h	32	MCAN3_MSG_RAM_START	START	5263 0000h

Table 4-1459. MCAN3_MSG_RAM, MCAN3_MSG_RAM_MCAN3_MSG_RAM Registers, Base Address=5263 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	MCAN3_MSG_RAM_START	START

Table 4-1460. MCAN3_CFG, MCAN3_CFG_MCAN3_CFG Registers, Base Address=5263 8000H, Length=7

Offset	Length	Acronym	Register Name	MCAN3_CFG Physical Address
0h	32	MCAN3_CFG_SS_PID	SS_PID	5263 8000h
4h	32	MCAN3_CFG_SS_CTRL	SS_CTRL	5263 8004h
8h	32	MCAN3_CFG_SS_STAT	SS_STAT	5263 8008h
Ch	32	MCAN3_CFG_SS_ICS	SS_ICS	5263 800Ch
10h	32	MCAN3_CFG_SS_IRS	SS_IRS	5263 8010h
14h	32	MCAN3_CFG_SS_IECS	SS_IECS	5263 8014h
18h	32	MCAN3_CFG_SS_IE	SS_IE	5263 8018h
1Ch	32	MCAN3_CFG_SS_IES	SS_IES	5263 801Ch
20h	32	MCAN3_CFG_SS_EOI	SS_EOI	5263 8020h
24h	32	MCAN3_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS	5263 8024h
28h	32	MCAN3_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC	5263 8028h
200h	32	MCAN3_CFG_CREL	CREL	5263 8200h
204h	32	MCAN3_CFG_ENDN	ENDN	5263 8204h
208h	32	MCAN3_CFG_CUST	CUST	5263 8208h
20Ch	32	MCAN3_CFG_DBTP	DBTP	5263 820Ch
210h	32	MCAN3_CFG_TEST	TEST	5263 8210h
214h	32	MCAN3_CFG_RWD	RWD	5263 8214h
218h	32	MCAN3_CFG_CCCR	CCCR	5263 8218h
21Ch	32	MCAN3_CFG_NBTP	NBTP	5263 821Ch
220h	32	MCAN3_CFG_TSCC	TSCC	5263 8220h
224h	32	MCAN3_CFG_TSCV	TSCV	5263 8224h
228h	32	MCAN3_CFG_TOCC	TOCC	5263 8228h
22Ch	32	MCAN3_CFG_TOCV	TOCV	5263 822Ch
230h	32	MCAN3_CFG_RES00	RES00	5263 8230h
234h	32	MCAN3_CFG_RES01	RES01	5263 8234h
238h	32	MCAN3_CFG_RES02	RES02	5263 8238h
23Ch	32	MCAN3_CFG_RES03	RES03	5263 823Ch
240h	32	MCAN3_CFG_ECR	ECR	5263 8240h
244h	32	MCAN3_CFG_PSR	PSR	5263 8244h
248h	32	MCAN3_CFG_TDCR	TDCR	5263 8248h
24Ch	32	MCAN3_CFG_RES04	RES04	5263 824Ch
250h	32	MCAN3_CFG_IR	IR	5263 8250h
254h	32	MCAN3_CFG_IE	IE	5263 8254h
258h	32	MCAN3_CFG_ILS	ILS	5263 8258h
25Ch	32	MCAN3_CFG_ILE	ILE	5263 825Ch
260h	32	MCAN3_CFG_RES05	RES05	5263 8260h
264h	32	MCAN3_CFG_RES06	RES06	5263 8264h
268h	32	MCAN3_CFG_RES07	RES07	5263 8268h
26Ch	32	MCAN3_CFG_RES08	RES08	5263 826Ch
270h	32	MCAN3_CFG_RES09	RES09	5263 8270h
274h	32	MCAN3_CFG_RES10	RES10	5263 8274h
278h	32	MCAN3_CFG_RES11	RES11	5263 8278h

Table 4-1460. MCAN3_CFG, MCAN3_CFG_MCAN3_CFG Registers, Base Address=5263 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name	MCAN3_CFG Physical Address
27Ch	32	MCAN3_CFG_RES12	RES12	5263 827Ch
280h	32	MCAN3_CFG_GFC	GFC	5263 8280h
284h	32	MCAN3_CFG_SIDFC	SIDFC	5263 8284h
288h	32	MCAN3_CFG_XIDFC	XIDFC	5263 8288h
28Ch	32	MCAN3_CFG_RES13	RES13	5263 828Ch
290h	32	MCAN3_CFG_XIDAM	XIDAM	5263 8290h
294h	32	MCAN3_CFG_HPMS	HPMS	5263 8294h
298h	32	MCAN3_CFG_NDAT1	NDAT1	5263 8298h
29Ch	32	MCAN3_CFG_NDAT2	NDAT2	5263 829Ch
2A0h	32	MCAN3_CFG_RXF0C	RXF0C	5263 82A0h
2A4h	32	MCAN3_CFG_RXF0S	RXF0S	5263 82A4h
2A8h	32	MCAN3_CFG_RXF0A	RXF0A	5263 82A8h
2ACh	32	MCAN3_CFG_RXBC	RXBC	5263 82ACh
2B0h	32	MCAN3_CFG_RXF1C	RXF1C	5263 82B0h
2B4h	32	MCAN3_CFG_RXF1S	RXF1S	5263 82B4h
2B8h	32	MCAN3_CFG_RXF1A	RXF1A	5263 82B8h
2BCh	32	MCAN3_CFG_RXESC	RXESC	5263 82BCh
2C0h	32	MCAN3_CFG_TXBC	TXBC	5263 82C0h
2C4h	32	MCAN3_CFG_TXFQS	TXFQS	5263 82C4h
2C8h	32	MCAN3_CFG_TXESC	TXESC	5263 82C8h
2CCh	32	MCAN3_CFG_TXBRP	TXBRP	5263 82CCh
2D0h	32	MCAN3_CFG_TXBAR	TXBAR	5263 82D0h
2D4h	32	MCAN3_CFG_TXBCR	TXBCR	5263 82D4h
2D8h	32	MCAN3_CFG_TXBTO	TXBTO	5263 82D8h
2DCh	32	MCAN3_CFG_TXBCF	TXBCF	5263 82DCh
2E0h	32	MCAN3_CFG_TXBTIE	TXBTIE	5263 82E0h
2E4h	32	MCAN3_CFG_TXBCIE	TXBCIE	5263 82E4h
2E8h	32	MCAN3_CFG_RES14	RES14	5263 82E8h
2ECh	32	MCAN3_CFG_RES15	RES15	5263 82ECh
2F0h	32	MCAN3_CFG_TXEFC	TXEFC	5263 82F0h
2F4h	32	MCAN3_CFG_TXEFS	TXEFS	5263 82F4h
2F8h	32	MCAN3_CFG_TXEFA	TXEFA	5263 82F8h
2FCh	32	MCAN3_CFG_RES16	RES16	5263 82FCh

Table 4-1461. MCAN3_CFG, MCAN3_CFG_MCAN3_CFG Registers, Base Address=5263 8000H, Length=7

Offset	Length	Acronym	Register Name
0h	32	MCAN3_CFG_SS_PID	SS_PID
4h	32	MCAN3_CFG_SS_CTRL	SS_CTRL
8h	32	MCAN3_CFG_SS_STAT	SS_STAT
Ch	32	MCAN3_CFG_SS_ICS	SS_ICS
10h	32	MCAN3_CFG_SS_IRS	SS_IRS
14h	32	MCAN3_CFG_SS_IECS	SS_IECS
18h	32	MCAN3_CFG_SS_IE	SS_IE
1Ch	32	MCAN3_CFG_SS_IES	SS_IES
20h	32	MCAN3_CFG_SS_EOI	SS_EOI

Table 4-1461. MCAN3_CFG, MCAN3_CFG_MCAN3_CFG Registers, Base Address=5263 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
24h	32	MCAN3_CFG_SS_EXT_TS_PS	SS_EXT_TS_PS
28h	32	MCAN3_CFG_SS_EXT_TS_USIC	SS_EXT_TS_USIC
200h	32	MCAN3_CFG_CREL	CREL
204h	32	MCAN3_CFG_ENDN	ENDN
208h	32	MCAN3_CFG_CUST	CUST
20Ch	32	MCAN3_CFG_DBTP	DBTP
210h	32	MCAN3_CFG_TEST	TEST
214h	32	MCAN3_CFG_RWD	RWD
218h	32	MCAN3_CFG_CCCR	CCCR
21Ch	32	MCAN3_CFG_NBTP	NBTP
220h	32	MCAN3_CFG_TSCC	TSCC
224h	32	MCAN3_CFG_TSCV	TSCV
228h	32	MCAN3_CFG_TOCC	TOCC
22Ch	32	MCAN3_CFG_TOCV	TOCV
230h	32	MCAN3_CFG_RES00	RES00
234h	32	MCAN3_CFG_RES01	RES01
238h	32	MCAN3_CFG_RES02	RES02
23Ch	32	MCAN3_CFG_RES03	RES03
240h	32	MCAN3_CFG_ECR	ECR
244h	32	MCAN3_CFG_PSR	PSR
248h	32	MCAN3_CFG_TDCR	TDCR
24Ch	32	MCAN3_CFG_RES04	RES04
250h	32	MCAN3_CFG_IR	IR
254h	32	MCAN3_CFG_IE	IE
258h	32	MCAN3_CFG_ILS	ILS
25Ch	32	MCAN3_CFG_ILE	ILE
260h	32	MCAN3_CFG_RES05	RES05
264h	32	MCAN3_CFG_RES06	RES06
268h	32	MCAN3_CFG_RES07	RES07
26Ch	32	MCAN3_CFG_RES08	RES08
270h	32	MCAN3_CFG_RES09	RES09
274h	32	MCAN3_CFG_RES10	RES10
278h	32	MCAN3_CFG_RES11	RES11
27Ch	32	MCAN3_CFG_RES12	RES12
280h	32	MCAN3_CFG_GFC	GFC
284h	32	MCAN3_CFG_SIDFC	SIDFC
288h	32	MCAN3_CFG_XIDFC	XIDFC
28Ch	32	MCAN3_CFG_RES13	RES13
290h	32	MCAN3_CFG_XIDAM	XIDAM
294h	32	MCAN3_CFG_HPMS	HPMS
298h	32	MCAN3_CFG_NDAT1	NDAT1
29Ch	32	MCAN3_CFG_NDAT2	NDAT2
2A0h	32	MCAN3_CFG_RXF0C	RXF0C
2A4h	32	MCAN3_CFG_RXF0S	RXF0S
2A8h	32	MCAN3_CFG_RXF0A	RXF0A
2ACh	32	MCAN3_CFG_RXBC	RXBC

Table 4-1461. MCAN3_CFG, MCAN3_CFG_MCAN3_CFG Registers, Base Address=5263 8000H, Length=7 (continued)

Offset	Length	Acronym	Register Name
2B0h	32	MCAN3_CFG_RXF1C	RXF1C
2B4h	32	MCAN3_CFG_RXF1S	RXF1S
2B8h	32	MCAN3_CFG_RXF1A	RXF1A
2BCh	32	MCAN3_CFG_RXESC	RXESC
2C0h	32	MCAN3_CFG_TXBC	TXBC
2C4h	32	MCAN3_CFG_TXFQS	TXFQS
2C8h	32	MCAN3_CFG_TXESC	TXESC
2CCh	32	MCAN3_CFG_TXBRP	TXBRP
2D0h	32	MCAN3_CFG_TXBAR	TXBAR
2D4h	32	MCAN3_CFG_TXBCR	TXBCR
2D8h	32	MCAN3_CFG_TXBTO	TXBTO
2DCh	32	MCAN3_CFG_TXBCF	TXBCF
2E0h	32	MCAN3_CFG_TXBTIE	TXBTIE
2E4h	32	MCAN3_CFG_TXBCIE	TXBCIE
2E8h	32	MCAN3_CFG_RES14	RES14
2ECh	32	MCAN3_CFG_RES15	RES15
2F0h	32	MCAN3_CFG_TXEFC	TXEFC
2F4h	32	MCAN3_CFG_TXEFS	TXEFS
2F8h	32	MCAN3_CFG_TXEFA	TXEFA
2FCh	32	MCAN3_CFG_RES16	RES16

4.16.1 MCAN0_CFG_SS_PID Register (Offset = 0h) [reset = h]

Short Description: SS_PID

Long Description:

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Table 4-1462. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8000h

Figure 4-690. MCAN0_CFG_SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		100011100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1011					1			0		1					

Access Types Legend

Table 4-1463. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	MODULE_ID	RO	1749204760h	Module ID
15 - 11	RTL	RO	3F3h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.16.2 MCAN0_CFG_SS_CTRL Register (Offset = 4h) [reset = h]

Short Description: SS_CTRL

Long Description:

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Table 4-1464. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8004h

Figure 4-691. MCAN0_CFG_SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
RO									RW	RW	RW	RW	RO		
0									0	0	0	1	0		

Access Types Legend

Table 4-1465. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU0	RO	0h	Reserved
6	EXT_TS_CNTR_EN	RW	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	RW	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	RW	0h	Wakeup Request Enable
3	DBGSUSP_FREE	RW	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2 - 0	NU	RO	0h	Reserved

4.16.3 MCAN0_CFG_SS_STAT Register (Offset = 8h) [reset = h]

Short Description: SS_STAT

Long Description:

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Table 4-1466. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8008h

Figure 4-692. MCAN0_CFG_SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
RO													RO	RO	RO
0													1	1	0

Access Types Legend

Table 4-1467. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU1	RO	0h	Reserved
2	EN_FDOE	RO	1h	Reflects the value of mcanss_enable_fdoe configuration portx=mcanss_enable_fdoe
1	MMI_DONE	RO	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	RO	0h	Reserved

4.16.4 MCAN0_CFG_SS_ICS Register (Offset = Ch) [reset = h]

Short Description: SS_ICS

Long Description:

Return to Summary Table

Table 4-1468. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 800Ch

Figure 4-693. MCAN0_CFG_SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
RO															WO
0															0

Access Types Legend

Table 4-1469. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU2	RO	0h	Reserved
0	ICS	WO	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. (ICS - Interrupt Clear Shadow Register)

4.16.5 MCAN0_CFG_SS_IRS Register (Offset = 10h) [reset = h]

Short Description: SS_IRS

Long Description:

Return to Summary Table

Table 4-1470. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8010h

Figure 4-694. MCAN0_CFG_SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
RO															RO
0															0

Access Types Legend

Table 4-1471. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU3	RO	0h	Reserved
0	IRS	RO	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. (IRS - Interrupt Raw Status Register)

4.16.6 MCAN0_CFG_SS_IECS Register (Offset = 14h) [reset = h]

Short Description: SS_IECS

Long Description:

Return to Summary Table

Table 4-1472. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8014h

Figure 4-695. MCAN0_CFG_SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
RO															WO
0															0

Access Types Legend

Table 4-1473. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU4	RO	0h	Reserved
0	IECS	WO	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. (IECS - Interrupt Enable Clear Shadow Register)

4.16.7 MCAN0_CFG_SS_IE Register (Offset = 18h) [reset = h]

Short Description: SS_IE

Long Description:

Return to Summary Table

Table 4-1474. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8018h

Figure 4-696. MCAN0_CFG_SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
RO															RW
0															0

Access Types Legend

Table 4-1475. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU5	RO	0h	Reserved
0	IE	RW	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. (IE - Interrupt Enable Register)

4.16.8 MCAN0_CFG_SS_IES Register (Offset = 1Ch) [reset = h]

Short Description: SS_IES

Long Description:

Return to Summary Table

Table 4-1476. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 801Ch

Figure 4-697. MCAN0_CFG_SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
RO															RO
0															0

Access Types Legend

Table 4-1477. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU6	RO	0h	Reserved
0	IES	RO	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. (IES - Interrupt Enable Status)

4.16.9 MCAN0_CFG_SS_EOI Register (Offset = 20h) [reset = h]

Short Description: SS_EOI

Long Description:

Return to Summary Table

Table 4-1478. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8020h

Figure 4-698. MCAN0_CFG_SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
RO								WO							
0								0							

Access Types Legend

Table 4-1479. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU7	RO	0h	Reserved
7 - 0	EOI	WO	0h	Write with bit position of targeted interrupt. (E.g. Ext TS is bit 0).Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi(0): EOI value for External TS interrupt mcan_0_eoi(1): EOI value for mcan[0] interrupt mcan_1_eoi(2): EOI value for mcan[1] interrupt(EOI - End Of Interrupt)

4.16.10 MCAN0_CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = h]

Short Description: SS_EXT_TS_PS

Long Description:

Return to Summary Table

Table 4-1480. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8024h

Figure 4-699. MCAN0_CFG_SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
RW															
0															

Access Types Legend

Table 4-1481. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU8	RO	0h	Reserved
23 - 0	PRESCALE	RW	0h	External Timestamp Prescaler reload value.External Timestamp count rate is host clock rate divided by this valuewith one exception: a value of 0 has the same effect as 1 .

4.16.11 MCAN0_CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = h]

Short Description: SS_EXT_TS_USIC

Long Description:

Return to Summary Table

Table 4-1482. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8028h

Figure 4-700. MCAN0_CFG_SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
RO											RO				
0											0				

Access Types Legend

Table 4-1483. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU9	RO	0h	Reserved
4 - 0	EXT_TS_INTR_CNTR	RO	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt (EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter)

4.16.12 MCAN0_CFG_CREL Register (Offset = 200h) [reset = h]

Short Description: CREL

Long Description:

Return to Summary Table

Table 4-1484. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8200h

Figure 4-701. MCAN0_CFG_CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
RO				RO				RO				RO			
11				10				11				1000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
RO								RO							
110								1000							

Access Types Legend

Table 4-1485. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	REL	RO	Bh	Core Release
27 - 24	STEP	RO	Ah	Step of Core Release
23 - 20	SUBSTEP	RO	Bh	Sub-Step of Core Release
19 - 16	YEAR	RO	3E8h	Time Stamp Year
15 - 8	MON	RO	6Eh	Time Stamp Month
7 - 0	DAY	RO	3E8h	Time Stamp Day

4.16.13 MCAN0_CFG_ENDN Register (Offset = 204h) [reset = h]

Short Description: ENDN

Long Description:

Return to Summary Table

Table 4-1486. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8204h

Figure 4-702. MCAN0_CFG_ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
RO															
10000111011001010100001100100001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
RO															
10000111011001010100001100100001															

Access Types Legend

Table 4-1487. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ETV	RO	7E3819F3A 12CEB3649 491171A1h	Endianess test value

4.16.14 MCAN0_CFG_CUST Register (Offset = 208h) [reset = h]

Short Description: CUST

Long Description:

Return to Summary Table

Table 4-1488. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8208h

Figure 4-703. MCAN0_CFG_CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
RO															
0															

Access Types Legend

Table 4-1489. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUST	RO	0h	Custom

4.16.15 MCAN0_CFG_DBTP Register (Offset = 20Ch) [reset = h]

Short Description: DBTP

Long Description:

Return to Summary Table

Table 4-1490. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 820Ch

Figure 4-704. MCAN0_CFG_DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
RO								RW	RO		RW				
0								0	0		0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2				DSJW			
RO			RW					RW				RW			
0			1010					11				11			

Access Types Legend

Table 4-1491. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU13	RO	0h	Reserved
23	TDC	RW	0h	Transmitter Delay Compensation
22 - 21	NU12	RO	0h	Reserved
20 - 16	DBRP	RW	0h	Data Baud Rate Prescaler
15 - 13	NU11	RO	0h	Reserved
12 - 8	DTSEG1	RW	3F2h	Data time segment before smaple point
7 - 4	DTSEG2	RW	Bh	Data time segment after sample point
3 - 0	DSJW	RW	Bh	Data resynchronization Jump Width

4.16.16 MCAN0_CFG_TEST Register (Offset = 210h) [reset = h]

Short Description: TEST

Long Description:

Return to Summary Table

Table 4-1492. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8210h

Figure 4-705. MCAN0_CFG_TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
RO								RO	RW		RW	RO			
0								0	0		0	0			

Access Types Legend

Table 4-1493. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU15	RO	0h	Reserved
7	RX	RO	0h	Receive Pin
6 - 5	TX	RW	0h	Control of Transmit Pin
4	LBCK	RW	0h	Loop Back Mode
3 - 0	NU14	RO	0h	Reserved

4.16.17 MCAN0_CFG_RWD Register (Offset = 214h) [reset = h]

Short Description: RWD

Long Description:

Return to Summary Table

Table 4-1494. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8214h

Figure 4-706. MCAN0_CFG_RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
RO								RW							
0								0							

Access Types Legend

Table 4-1495. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU16	RO	0h	Reserved
15 - 8	WDV	RO	0h	Watchdog Value
7 - 0	WDC	RW	0h	Watchdog Counter Value

4.16.18 MCAN0_CFG_CCCR Register (Offset = 218h) [reset = h]

Short Description: CCCR

Long Description:

Return to Summary Table

Table 4-1496. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8218h

Figure 4-707. MCAN0_CFG_CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
RW	RW	RW	RW	RO		RW	RW	RW	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0		0	0	0	0	0	0	0	0	0	1

Access Types Legend

Table 4-1497. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU18	RW	0h	Reserved
14	TXP	RW	0h	Transmit Pause
13	EFBI	RW	0h	Edge Filtering durign Bus Integration
12	PXHD	RW	0h	Protocol Exception Handling Disable
11 - 10	NU17	RO	0h	Reserved
9	BRSE	RW	0h	Bit Rate Switch Enable
8	FDOE	RW	0h	FD Operation Enable
7	TEST	RW	0h	Test Mode enable
6	DAR	RW	0h	Disable Automatic Regransmission
5	MON	RW	0h	Bus Monitoring Mode
4	CSR	RW	0h	Clock Stop Request
3	CSA	RO	0h	Clock Stop Acknowledge
2	ASM	RW	0h	Restriced Operation Mode
1	CCE	RW	0h	Configuration Change Enable
0	INIT	RW	1h	Initialization

4.16.19 MCAN0_CFG_NBTP Register (Offset = 21Ch) [reset = h]

Short Description: NBTP

Long Description:

Return to Summary Table

Table 4-1498. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 821Ch

Figure 4-708. MCAN0_CFG_NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW								NBRP							
RW								RW							
11								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
RW								RO	RW						
1010								0	11						

Access Types Legend

Table 4-1499. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NSJW	RW	Bh	Nominal Resynchronization Jump Width
24 - 16	NBRP	RW	0h	Nominal Baud Rate Prescaler
15 - 8	NTSEG1	RW	3F2h	Nominal Time segment before sample point
7	NU19	RO	0h	Reserved
6 - 0	NTSEG2	RW	Bh	Nominal Time segment after sample point

4.16.20 MCAN0_CFG_TSCC Register (Offset = 220h) [reset = h]

Short Description: TSCC

Long Description:

Return to Summary Table

Table 4-1500. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8220h

Figure 4-709. MCAN0_CFG_TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
RO														RW	
0														0	

Access Types Legend

Table 4-1501. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU21	RO	0h	Reserved
19 - 16	TCP	RW	0h	Timestamp Counter Prescaler
15 - 2	NU20	RO	0h	Reserved
1 - 0	TSS	RW	0h	Timestamp Select

4.16.21 MCAN0_CFG_TSCV Register (Offset = 224h) [reset = h]

Short Description: TSCV

Long Description:

Return to Summary Table

Table 4-1502. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8224h

Figure 4-710. MCAN0_CFG_TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
RW															
0															

Access Types Legend

Table 4-1503. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU22	RO	0h	Reserved
15 - 0	TSC	RW	0h	Timestamp Counter

4.16.22 MCAN0_CFG_TOCC Register (Offset = 228h) [reset = h]

Short Description: TOCC

Long Description:

Return to Summary Table

Table 4-1504. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8228h

Figure 4-711. MCAN0_CFG_TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
RO													RW		RW
0													0		0

Access Types Legend

Table 4-1505. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TOP	RW	3F28CB715 71C7h	Timeout Period
15 - 3	NU23	RO	0h	Reserved
2 - 1	TOS	RW	0h	Timeout Select
0	ETOC	RW	0h	Enable Timeout Counter

4.16.23 MCAN0_CFG_TOCV Register (Offset = 22Ch) [reset = h]

Short Description: TOCV

Long Description:

Return to Summary Table

Table 4-1506. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 822Ch

Figure 4-712. MCAN0_CFG_TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
RW															
1111111111111111															

Access Types Legend

Table 4-1507. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU24	RO	0h	Reserved
15 - 0	TOC	RW	3F28CB715 71C7h	Timeout Counter

4.16.24 MCAN0_CFG_RES00 Register (Offset = 230h) [reset = h]

Short Description: RES00

Long Description:

Return to Summary Table

Table 4-1508. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8230h

Figure 4-713. MCAN0_CFG_RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
RO															
0															

Access Types Legend

Table 4-1509. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES00	RO	0h	Reserved

4.16.25 MCAN0_CFG_RES01 Register (Offset = 234h) [reset = h]

Short Description: RES01

Long Description:

Return to Summary Table

Table 4-1510. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8234h

Figure 4-714. MCAN0_CFG_RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
RO															
0															

Access Types Legend

Table 4-1511. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES01	RO	0h	Reserved

4.16.26 MCAN0_CFG_RES02 Register (Offset = 238h) [reset = h]

Short Description: RES02

Long Description:

Return to Summary Table

Table 4-1512. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8238h

Figure 4-715. MCAN0_CFG_RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
RO															
0															

Access Types Legend

Table 4-1513. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES02	RO	0h	Reserved

4.16.27 MCAN0_CFG_RES03 Register (Offset = 23Ch) [reset = h]

Short Description: RES03

Long Description:

Return to Summary Table

Table 4-1514. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 823Ch

Figure 4-716. MCAN0_CFG_RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
RO															
0															

Access Types Legend

Table 4-1515. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES03	RO	0h	Reserved

4.16.28 MCAN0_CFG_ECR Register (Offset = 240h) [reset = h]

Short Description: ECR

Long Description:

Return to Summary Table

Table 4-1516. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8240h

Figure 4-717. MCAN0_CFG_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
RO	RO							RO							
0	0							0							

Access Types Legend

Table 4-1517. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU25	RO	0h	Reserved
23 - 16	CEL	RO	0h	CAN Error Logging
15	RP	RO	0h	Recieve Error Passive
14 - 8	REC	RO	0h	Recieve Error Counter
7 - 0	TEC	RO	0h	Transmit Error Counter

4.16.29 MCAN0_CFG_PSR Register (Offset = 244h) [reset = h]

Short Description: PSR

Long Description:

Return to Summary Table

Table 4-1518. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8244h

Figure 4-718. MCAN0_CFG_PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
RO									RO						
0									0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
RO	RO	RO	RO	RO	RO			RO	RO	RO	RO		RO		
0	0	0	0	0	111			0	0	0	0		111		

Access Types Legend

Table 4-1519. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 23	NU27	RO	0h	Reserved
22 - 16	TDCV	RO	0h	Transmitter Delay Compensation Value
15	NU26	RO	0h	Reserved
14	PXE	RO	0h	Protocol Exception Event
13	RFDF	RO	0h	Recieved a CAN FD Message
12	RBRS	RO	0h	BRS flag of last recieved CAN FD Message
11	RESI	RO	0h	ESI flag of last recieved CAN FD Message
10 - 8	DLEC	RO	6Fh	Data Phase Last Error Code
7	BO	RO	0h	Bus_Off status
6	EW	RO	0h	Warning Status
5	EP	RO	0h	Error Passive
4 - 3	ACT	RO	0h	Activity
2 - 0	LEC	RO	6Fh	Last Error Code

4.16.30 MCAN0_CFG_TDCR Register (Offset = 248h) [reset = h]

Short Description: TDCR

Long Description:

Return to Summary Table

Table 4-1520. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8248h

Figure 4-719. MCAN0_CFG_TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29	TDCO							NU28	TDCF						
RO	RW							RO	RW						
0	0							0	0						

Access Types Legend

Table 4-1521. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU29	RO	0h	Reserved
14 - 8	TDCO	RW	0h	Transmitter Delay Compensation Offset
7	NU28	RO	0h	Reserved
6 - 0	TDCF	RW	0h	Transmitter Delay Compensation Filter Window Length

4.16.31 MCAN0_CFG_RES04 Register (Offset = 24Ch) [reset = h]

Short Description: RES04

Long Description:

Return to Summary Table

Table 4-1522. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 824Ch

Figure 4-720. MCAN0_CFG_RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
RO															
0															

Access Types Legend

Table 4-1523. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES04	RO	0h	Reserved

4.16.32 MCAN0_CFG_IR Register (Offset = 250h) [reset = h]

Short Description: IR

Long Description:

Return to Summary Table

Table 4-1524. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8250h

Figure 4-721. MCAN0_CFG_IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1525. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU30	RO	0h	Reserved
29	ARA	RW	0h	Access to Reserved Address
28	PED	RW	0h	Protocol Error in data Phase
27	PEA	RW	0h	Protocol Error in Arbitration Phase
26	WDI	RW	0h	Watchdog Interrupt
25	BO	RW	0h	Bus_Off Status
24	EW	RW	0h	Warning Status
23	EP	RW	0h	Error Passive
22	ELO	RW	0h	Error Logging Overflow
21	BEU	RW	0h	Bit Error Uncorrected
20	BEC	RW	0h	Bit Error Corrected
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer
18	TOO	RW	0h	Timeout Occurred
17	MRAF	RW	0h	Message RAM Access Failure
16	TSW	RW	0h	Timestamp Wraparound
15	TEFL	RW	0h	Tx Event FIFO Element Lost
14	TEFF	RW	0h	Tx Event FIFO Full
13	TEFW	RW	0h	Tx Event FIFO Watermark Reached
12	TEFN	RW	0h	Tx Event FIFO New Entry
11	TFE	RW	0h	Tx FIFO Empty
10	TCF	RW	0h	Transmission Cancellation Finished
9	TC	RW	0h	Transmission Complete
8	HPM	RW	0h	High Priority Message
7	RF1L	RW	0h	Rx FIFO 1 Message Lost
6	RF1F	RW	0h	Rx FIFO 1 Full
5	RF1W	RW	0h	Rx FIFO 1 Watermark Reached
4	RF1N	RW	0h	Rx FIFO 1 New Message

Table 4-1525. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0L	RW	0h	Rx FIFO 0 Message Lost
2	RF0F	RW	0h	Rx FIFO 0 Full
1	RF0W	RW	0h	Rx FIFO 0 Watermark Reached
0	RF0N	RW	0h	Rx FIFO 0 New Message

4.16.33 MCAN0_CFG_IE Register (Offset = 254h) [reset = h]

Short Description: IE

Long Description:

Return to Summary Table

Table 4-1526. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8254h

Figure 4-722. MCAN0_CFG_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1527. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU31	RO	0h	Reserved
29	ARAE	RW	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	RW	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	RW	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	RW	0h	Watchdog Interrupt Enable
25	BOE	RW	0h	Bus_Off Status Interrupt Enable
24	EWE	RW	0h	Warning Status Interrupt Enable
23	EPE	RW	0h	Error Passive Interrupt Enable
22	ELOE	RW	0h	Error Logging Overflow Interrupt Enable
21	BEUE	RW	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	RW	0h	Bit Error Corrected Interrupt Enable
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	RW	0h	Timeout Occurred Interrupt Enable
17	MRAFE	RW	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	RW	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	RW	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	RW	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	RW	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	RW	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	RW	0h	Tx FIFO Empty Interrupt Enable
10	TCFE	RW	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	RW	0h	Transmission Completed Interrupt Enable
8	HPME	RW	0h	High Priority message Interrupt Enable
7	RF1LE	RW	0h	rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	RW	0h	Rx FIFO 1 Full Interrupt Enable

Table 4-1527. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WE	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	RW	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	RW	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	RW	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	RW	0h	Rx FIFO 0 New Message Interrupt Enable

4.16.34 MCAN0_CFG_ILS Register (Offset = 258h) [reset = h]

Short Description: ILS

Long Description:

Return to Summary Table

Table 4-1528. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8258h

Figure 4-723. MCAN0_CFG_ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1529. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU32	RO	0h	Reserved
29	ARAL	RW	0h	Accees to Reserve Address Interrupt Line
28	PEDL	RW	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	RW	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	RW	0h	Watchdog Interrupt Line
25	BOL	RW	0h	Bus_Off Status Interrupt Line
24	EWL	RW	0h	Warning Status Interrupt Line
23	EPL	RW	0h	Error Passive Interrupt Line
22	ELOL	RW	0h	Error Logging Overflow Interrupt Line
21	BEUL	RW	0h	Bit Error Uncorrected Interrupt Line
20	BECL	RW	0h	Bit Error Corrected Interrupt Line
19	DRXL	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	RW	0h	Timeout Occurred Interrupt Line
17	MRAFL	RW	0h	Message RAM Access Failure Interrupt Line
16	TSWL	RW	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	RW	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	RW	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	RW	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	RW	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	RW	0h	Tx FIFO Empty Interrupt Line
10	TCFL	RW	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	RW	0h	Transmission Completed Interrupt Line
8	HPML	RW	0h	High Priority message Interrupt Line
7	RF1LL	RW	0h	rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	RW	0h	Rx FIFO 1 Full Interrupt Line

Table 4-1529. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WL	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	RW	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	RW	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	RW	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	RW	0h	Rx FIFO 0 New Message Interrupt Line

4.16.35 MCAN0_CFG_ILE Register (Offset = 25Ch) [reset = h]

Short Description: ILE

Long Description:

Return to Summary Table

Table 4-1530. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 825Ch

Figure 4-724. MCAN0_CFG_ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1531. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU33	RO	0h	Reserved
1	EINT1	RW	0h	Enable Interrupt Line 1
0	EINT0	RW	0h	Enable Interrupt Line 0

4.16.36 MCAN0_CFG_RES05 Register (Offset = 260h) [reset = h]

Short Description: RES05

Long Description:

Return to Summary Table

Table 4-1532. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8260h

Figure 4-725. MCAN0_CFG_RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
RO															
0															

Access Types Legend

Table 4-1533. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES05	RO	0h	Reserved

4.16.37 MCAN0_CFG_RES06 Register (Offset = 264h) [reset = h]

Short Description: RES06

Long Description:

Return to Summary Table

Table 4-1534. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8264h

Figure 4-726. MCAN0_CFG_RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
RO															
0															

Access Types Legend

Table 4-1535. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES06	RO	0h	Reserved

4.16.38 MCAN0_CFG_RES07 Register (Offset = 268h) [reset = h]

Short Description: RES07

Long Description:

Return to Summary Table

Table 4-1536. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8268h

Figure 4-727. MCAN0_CFG_RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
RO															
0															

Access Types Legend

Table 4-1537. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES07	RO	0h	Reserved

4.16.39 MCAN0_CFG_RES08 Register (Offset = 26Ch) [reset = h]

Short Description: RES08

Long Description:

Return to Summary Table

Table 4-1538. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 826Ch

Figure 4-728. MCAN0_CFG_RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
RO															
0															

Access Types Legend

Table 4-1539. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES08	RO	0h	Reserved

4.16.40 MCAN0_CFG_RES09 Register (Offset = 270h) [reset = h]

Short Description: RES09

Long Description:

Return to Summary Table

Table 4-1540. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8270h

Figure 4-729. MCAN0_CFG_RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
RO															
0															

Access Types Legend

Table 4-1541. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES09	RO	0h	Reserved

4.16.41 MCAN0_CFG_RES10 Register (Offset = 274h) [reset = h]

Short Description: RES10

Long Description:

Return to Summary Table

Table 4-1542. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8274h

Figure 4-730. MCAN0_CFG_RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
RO															
0															

Access Types Legend

Table 4-1543. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES10	RO	0h	Reserved

4.16.42 MCAN0_CFG_RES11 Register (Offset = 278h) [reset = h]

Short Description: RES11

Long Description:

Return to Summary Table

Table 4-1544. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8278h

Figure 4-731. MCAN0_CFG_RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
RO															
0															

Access Types Legend

Table 4-1545. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES11	RO	0h	Reserved

4.16.43 MCAN0_CFG_RES12 Register (Offset = 27Ch) [reset = h]

Short Description: RES12

Long Description:

Return to Summary Table

Table 4-1546. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 827Ch

Figure 4-732. MCAN0_CFG_RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
RO															
0															

Access Types Legend

Table 4-1547. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES12	RO	0h	Reserved

4.16.44 MCAN0_CFG_GFC Register (Offset = 280h) [reset = h]

Short Description: GFC

Long Description:

Return to Summary Table

Table 4-1548. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8280h

Figure 4-733. MCAN0_CFG_GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
RO										RW		RW		RW	RW
0										0		0		0	0

Access Types Legend

Table 4-1549. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU34	RO	0h	Reserved
5 - 4	ANFS	RW	0h	Accept Non-matching Frames Standard
3 - 2	ANFE	RW	0h	Accept Non-matching Frames Extended
1	RRFS	RW	0h	reject Remote Frames Standard
0	RRFE	RW	0h	reject Remote Frames Extended

4.16.45 MCAN0_CFG_SIDFC Register (Offset = 284h) [reset = h]

Short Description: SIDFC

Long Description:

Return to Summary Table

Table 4-1550. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8284h

Figure 4-734. MCAN0_CFG_SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
RW														RO	
0														0	

Access Types Legend

Table 4-1551. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU36	RO	0h	Reserved
23 - 16	LSS_S	RW	0h	List Size Standard
15 - 2	FLSSA_S	RW	0h	Filter List Standard Start Address
1 - 0	NU35	RO	0h	Reserved

4.16.46 MCAN0_CFG_XIDFC Register (Offset = 288h) [reset = h]

Short Description: XIDFC

Long Description:

Return to Summary Table

Table 4-1552. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8288h

Figure 4-735. MCAN0_CFG_XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
RW														RO	
0														0	

Access Types Legend

Table 4-1553. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU38	RO	0h	Reserved
23 - 16	LSS_X	RW	0h	List Size Standard
15 - 2	FLSSA_X	RW	0h	Filter List Standard Start Address
1 - 0	NU37	RO	0h	Reserved

4.16.47 MCAN0_CFG_RES13 Register (Offset = 28Ch) [reset = h]

Short Description: RES13

Long Description:

Return to Summary Table

Table 4-1554. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 828Ch

Figure 4-736. MCAN0_CFG_RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
RO															
0															

Access Types Legend

Table 4-1555. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES13	RO	0h	Reserved

4.16.48 MCAN0_CFG_XIDAM Register (Offset = 290h) [reset = h]

Short Description: XIDAM

Long Description:

Return to Summary Table

Table 4-1556. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8290h

Figure 4-737. MCAN0_CFG_XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
RO			RW												
0			11111111111111111111111111111												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
RW															
11111111111111111111111111111															

Access Types Legend

Table 4-1557. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	NU39	RO	0h	Reserved
28 - 0	EIDM	RW	23E6E54C4 50CAD4F67 1C71C7h	Extended ID Mask

4.16.49 MCAN0_CFG_HPMS Register (Offset = 294h) [reset = h]

Short Description: HPMS

Long Description:

Return to Summary Table

Table 4-1558. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8294h

Figure 4-738. MCAN0_CFG_HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
RO	RO							RO		RO					
0	0							0		0					

Access Types Legend

Table 4-1559. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU40	RO	0h	Reserved
15	FLST	RO	0h	Filter List
14 - 8	FIDX	RO	0h	Filter Index
7 - 6	MSI	RO	0h	Message Storeage Indicator
5 - 0	BIDX	RO	0h	Buffer Index

4.16.50 MCAN0_CFG_NDAT1 Register (Offset = 298h) [reset = h]

Short Description: NDAT1

Long Description:

Return to Summary Table

Table 4-1560. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8298h

Figure 4-739. MCAN0_CFG_NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
RW															
0															

Access Types Legend

Table 4-1561. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND0_31	RW	0h	New Data 0-31

4.16.51 MCAN0_CFG_NDAT2 Register (Offset = 29Ch) [reset = h]

Short Description: NDAT2

Long Description:

Return to Summary Table

Table 4-1562. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 829Ch

Figure 4-740. MCAN0_CFG_NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
RW															
0															

Access Types Legend

Table 4-1563. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND32_63	RW	0h	New Data 32-63

4.16.52 MCAN0_CFG_RXF0C Register (Offset = 2A0h) [reset = h]

Short Description: RXF0C

Long Description:

Return to Summary Table

Table 4-1564. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A0h

Figure 4-741. MCAN0_CFG_RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1565. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F0WM	RW	0h	Rx FIFO 0 Watermark
23	NU42_1	RO	0h	Reserved
22 - 16	F0S	RW	0h	Rx FIFO 0 Size
15	NU42	RO	0h	Reserved
14 - 2	F0SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU41	RO	0h	Reserved

4.16.53 MCAN0_CFG_RXF0S Register (Offset = 2A4h) [reset = h]

Short Description: RXF0S

Long Description:

Return to Summary Table

Table 4-1566. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A4h

Figure 4-742. MCAN0_CFG_RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1567. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU46	RO	0h	Reserved
25	RF0L	RO	0h	Rx FIFO 0 Message Lost
24	F0F	RO	0h	Rx FIFO 0 Full
23 - 22	NU45	RO	0h	Reserved
21 - 16	F0PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU44	RO	0h	Reserved
13 - 8	F0GI	RO	0h	Rx FIFO 0 Get Index
7	NU43	RO	0h	Reserved
6 - 0	F0FL	RO	0h	Rx FIFO 0 Fill Level

4.16.54 MCAN0_CFG_RXF0A Register (Offset = 2A8h) [reset = h]

Short Description: RXF0A

Long Description:

Return to Summary Table

Table 4-1568. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A8h

Figure 4-743. MCAN0_CFG_RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1569. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU47	RO	0h	Reserved
5 - 0	F0AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.55 MCAN0_CFG_RXBC Register (Offset = 2ACh) [reset = h]

Short Description: RXBC

Long Description:

Return to Summary Table

Table 4-1570. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82ACh

Figure 4-744. MCAN0_CFG_RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
RW														RO	
0														0	

Access Types Legend

Table 4-1571. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU49	RO	0h	Reserved
15 - 2	RBSA	RW	0h	Rx Buffer Start Address
1 - 0	NU48	RO	0h	Reserved

4.16.56 MCAN0_CFG_RXF1C Register (Offset = 2B0h) [reset = h]

Short Description: RXF1C

Long Description:

Return to Summary Table

Table 4-1572. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B0h

Figure 4-745. MCAN0_CFG_RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1573. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F1WM	RW	0h	Rx FIFO 0 Watermark
23	NU50_1	RO	0h	Reserved
22 - 16	F1S	RW	0h	Rx FIFO 0 Size
15	NU50	RO	0h	Reserved
14 - 2	F1SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU499	RO	0h	Reserved

4.16.57 MCAN0_CFG_RXF1S Register (Offset = 2B4h) [reset = h]

Short Description: RXF1S

Long Description:

Return to Summary Table

Table 4-1574. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B4h

Figure 4-746. MCAN0_CFG_RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1575. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU54	RO	0h	Reserved
25	RF1L	RO	0h	Rx FIFO 0 Message Lost
24	F1F	RO	0h	Rx FIFO 0 Full
23 - 22	NU53	RO	0h	Reserved
21 - 16	F1PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU52	RO	0h	Reserved
13 - 8	F1GI	RO	0h	Rx FIFO 0 Get Index
7	NU51	RO	0h	Reserved
6 - 0	F1FL	RO	0h	Rx FIFO 0 Fill Level

4.16.58 MCAN0_CFG_RXF1A Register (Offset = 2B8h) [reset = h]

Short Description: RXF1A

Long Description:

Return to Summary Table

Table 4-1576. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B8h

Figure 4-747. MCAN0_CFG_RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1577. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU55	RO	0h	Reserved
5 - 0	F1AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.59 MCAN0_CFG_RXESC Register (Offset = 2BCh) [reset = h]

Short Description: RXESC

Long Description:

Return to Summary Table

Table 4-1578. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82BCh

Figure 4-748. MCAN0_CFG_RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
RO					RW			RO	RW			RO	RW		
0					0			0	0			0	0		

Access Types Legend

Table 4-1579. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU58	RO	0h	Reserved
10 - 8	RBDS	RW	0h	Rx Buffer data Field Size
7	NU57	RO	0h	Reserved
6 - 4	F1DS	RW	0h	Rx FIFO 1 Data Field Size
3	NU56	RO	0h	Reserved
2 - 0	F0DS	RW	0h	Rx FIFO 0 Data Field Size

4.16.60 MCAN0_CFG_TXBC Register (Offset = 2C0h) [reset = h]

Short Description: TXBC

Long Description:

Return to Summary Table

Table 4-1580. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C0h

Figure 4-749. MCAN0_CFG_TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
RO	RO	RO						RO		RO					
0	0	0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
RO														RO	
0														0	

Access Types Legend

Table 4-1581. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	RO	0h	Reserved
30	TFQM	RO	0h	Tx FIFO/Queue Mode
29 - 24	TFQS	RO	0h	Transmit FIFO/Queue Size
23 - 22	NU60	RO	0h	Reserved
21 - 16	NDTB	RO	0h	Number of Dedicated Transmit Buffers
15 - 2	TBSA	RO	0h	Tx Buffers Start Address
1 - 0	NU59	RO	0h	Reserved

4.16.61 MCAN0_CFG_TXFQS Register (Offset = 2C4h) [reset = h]

Short Description: TXFQS

Long Description:

Return to Summary Table

Table 4-1582. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C4h

Figure 4-750. MCAN0_CFG_TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
RO										RO	RO				
0										0	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1583. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 22	NU64	RO	0h	Reserved
21	TFQF	RO	0h	Tx FIFO/Queue Full
20 - 16	TFQPI	RO	0h	Tx FIFO/Queue Put Index
15 - 13	NU63	RO	0h	Reserved
12 - 8	TFGI	RO	0h	Tx Queue Get Index
7 - 6	NU62	RO	0h	Reserved
5 - 0	TFFL	RO	0h	Tx FIFO Free Level

4.16.62 MCAN0_CFG_TXESC Register (Offset = 2C8h) [reset = h]

Short Description: TXESC

Long Description:

Return to Summary Table

Table 4-1584. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C8h

Figure 4-751. MCAN0_CFG_TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
RO													RW		
0													0		

Access Types Legend

Table 4-1585. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU65	RO	0h	Reserved
2 - 0	TBDS	RW	0h	Tx Buffer Data Field Size

4.16.63 MCAN0_CFG_TXBRP Register (Offset = 2CCh) [reset = h]

Short Description: TXBRP

Long Description:

Return to Summary Table

Table 4-1586. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82CCh

Figure 4-752. MCAN0_CFG_TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
RO															
0															

Access Types Legend

Table 4-1587. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TRP	RO	0h	Transmission Request Pending

4.16.64 MCAN0_CFG_TXBAR Register (Offset = 2D0h) [reset = h]

Short Description: TXBAR

Long Description:

Return to Summary Table

Table 4-1588. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D0h

Figure 4-753. MCAN0_CFG_TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1589. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AR	RW W0TOCLR	0h	Add request

4.16.65 MCAN0_CFG_TXBCR Register (Offset = 2D4h) [reset = h]

Short Description: TXBCR

Long Description:

Return to Summary Table

Table 4-1590. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D4h

Figure 4-754. MCAN0_CFG_TXBCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1591. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CR	RW W0TOCLR	0h	Cancellation Request

4.16.66 MCAN0_CFG_TXBTO Register (Offset = 2D8h) [reset = h]

Short Description: TXBTO

Long Description:

Return to Summary Table

Table 4-1592. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D8h

Figure 4-755. MCAN0_CFG_TXBTO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO															
RO															
0															

Access Types Legend

Table 4-1593. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO	RO	0h	Transmission Occurred

4.16.67 MCAN0_CFG_TXBCF Register (Offset = 2DCh) [reset = h]

Short Description: TXBCF

Long Description:

Return to Summary Table

Table 4-1594. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82DCh

Figure 4-756. MCAN0_CFG_TXBCF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF															
RO															
0															

Access Types Legend

Table 4-1595. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CF	RO	0h	Cancellation Finished

4.16.68 MCAN0_CFG_TXBTIE Register (Offset = 2E0h) [reset = h]

Short Description: TXBTIE

Long Description:

Return to Summary Table

Table 4-1596. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E0h

Figure 4-757. MCAN0_CFG_TXBTIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE															
RW															
0															

Access Types Legend

Table 4-1597. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIE	RW	0h	Transmission Interrupt Enable

4.16.69 MCAN0_CFG_TXBCIE Register (Offset = 2E4h) [reset = h]

Short Description: TXBCIE

Long Description:

Return to Summary Table

Table 4-1598. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E4h

Figure 4-758. MCAN0_CFG_TXBCIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE															
RW															
0															

Access Types Legend

Table 4-1599. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CFIE	RW	0h	Cancellation Finished Interrupt Enable

4.16.70 MCAN0_CFG_RES14 Register (Offset = 2E8h) [reset = h]

Short Description: RES14

Long Description:

Return to Summary Table

Table 4-1600. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E8h

Figure 4-759. MCAN0_CFG_RES14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES14															
RO															
0															

Access Types Legend

Table 4-1601. RES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES14	RO	0h	Reserved

4.16.71 MCAN0_CFG_RES15 Register (Offset = 2ECh) [reset = h]

Short Description: RES15

Long Description:

Return to Summary Table

Table 4-1602. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82ECh

Figure 4-760. MCAN0_CFG_RES15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15															
RO															
0															

Access Types Legend

Table 4-1603. RES15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES15	RO	0h	Reserved

4.16.72 MCAN0_CFG_TXEFC Register (Offset = 2F0h) [reset = h]

Short Description: TXEFC

Long Description:

Return to Summary Table

Table 4-1604. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F0h

Figure 4-761. MCAN0_CFG_TXEFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68		EFWM						NU67		EFS					
RW		RW						RW		RW					
0		0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFSA														NU66	
RW														RW	
0														0	

Access Types Legend

Table 4-1605. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU68	RW	0h	Reserved
29 - 24	EFWM	RW	0h	Event FIFO Watermark
23 - 22	NU67	RW	0h	Reserved
21 - 16	EFS	RW	0h	Event FIFO Size
15 - 2	EFSA	RW	0h	Event FIFO Start Address
1 - 0	NU66	RW	0h	Reserved

4.16.73 MCAN0_CFG_TXEFS Register (Offset = 2F4h) [reset = h]

Short Description: TXEFS

Long Description:

Return to Summary Table

Table 4-1606. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F4h

Figure 4-762. MCAN0_CFG_TXEFS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU72						TEFL	EFF	NU71			EFPI				
RO						RO	RO	RO			RO				
0						0	0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU70			EFGI					NU69		EFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1607. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU72	RO	0h	Reserved
25	TEFL	RO	0h	Tx Event FIFO Element Lost
24	EFF	RO	0h	Event FIFO Full
23 - 21	NU71	RO	0h	Reserved
20 - 16	EFPI	RO	0h	Event FIFO Put Index
15 - 13	NU70	RO	0h	Reserved
12 - 8	EFGI	RO	0h	Event FIFO Get Index
7 - 6	NU69	RO	0h	Reserved
5 - 0	EFFL	RO	0h	Event FIFO FIll Level

4.16.74 MCAN0_CFG_TXEFA Register (Offset = 2F8h) [reset = h]

Short Description: TXEFA

Long Description:

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Table 4-1608. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F8h

Figure 4-763. MCAN0_CFG_TXEFA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU73											EFAI				
RO											RO				
0											0				

Access Types Legend

Table 4-1609. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU73	RO	0h	Reserved
4 - 0	EFAI	RO	0h	Event FIFO Acknowledge Index

4.16.75 MCAN0_CFG_RES16 Register (Offset = 2FCh) [reset = h]

Short Description: RES16

Long Description:

Return to Summary Table

Table 4-1610. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82FCh

Figure 4-764. MCAN0_CFG_RES16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES16															
RO															
0															

Access Types Legend

Table 4-1611. RES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES16	RO	0h	Reserved

4.16.76 MCAN1_MSG_RAM_START Register (Offset = 0h) [reset = h]

Short Description: START

Long Description:

Return to Summary Table

Table 4-1612. Instance Table

Instance Name	Physical Address
MCAN1_MSG_RAM	5261 0000h

Figure 4-765. MCAN1_MSG_RAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1613. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	MCAN message mem Start address

4.16.77 MCAN1_CFG_SS_PID Register (Offset = 0h) [reset = h]

Short Description: SS_PID

Long Description:

Return to Summary Table

Table 4-1614. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8000h

Figure 4-766. MCAN1_CFG_SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		100011100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1011					1			0		1					

Access Types Legend

Table 4-1615. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	MODULE_ID	RO	1749204760h	Module ID
15 - 11	RTL	RO	3F3h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.16.78 MCAN1_CFG_SS_CTRL Register (Offset = 4h) [reset = h]

Short Description: SS_CTRL

Long Description:

Return to Summary Table

Table 4-1616. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8004h

Figure 4-767. MCAN1_CFG_SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
RO									RW	RW	RW	RW	RO		
0									0	0	0	1	0		

Access Types Legend

Table 4-1617. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU0	RO	0h	Reserved
6	EXT_TS_CNTR_EN	RW	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	RW	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	RW	0h	Wakeup Request Enable
3	DBGSUSP_FREE	RW	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2 - 0	NU	RO	0h	Reserved

4.16.79 MCAN1_CFG_SS_STAT Register (Offset = 8h) [reset = h]

Short Description: SS_STAT

Long Description:

Return to Summary Table

Table 4-1618. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8008h

Figure 4-768. MCAN1_CFG_SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
RO													RO	RO	RO
0													1	1	0

Access Types Legend

Table 4-1619. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU1	RO	0h	Reserved
2	EN_FDOE	RO	1h	Reflects the value of mcanss_enable_fdoe configuration portx=mcanss_enable_fdoe
1	MMI_DONE	RO	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	RO	0h	Reserved

4.16.80 MCAN1_CFG_SS_ICS Register (Offset = Ch) [reset = h]

Short Description: SS_ICS

Long Description:

Return to Summary Table

Table 4-1620. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 800Ch

Figure 4-769. MCAN1_CFG_SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
RO															WO
0															0

Access Types Legend

Table 4-1621. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU2	RO	0h	Reserved
0	ICS	WO	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. (ICS - Interrupt Clear Shadow Register)

4.16.81 MCAN1_CFG_SS_IRS Register (Offset = 10h) [reset = h]

Short Description: SS_IRS

Long Description:

Return to Summary Table

Table 4-1622. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8010h

Figure 4-770. MCAN1_CFG_SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
RO															RO
0															0

Access Types Legend

Table 4-1623. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU3	RO	0h	Reserved
0	IRS	RO	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. (IRS - Interrupt Raw Status Register)

4.16.82 MCAN1_CFG_SS_IECS Register (Offset = 14h) [reset = h]

Short Description: SS_IECS

Long Description:

Return to Summary Table

Table 4-1624. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8014h

Figure 4-771. MCAN1_CFG_SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
RO															WO
0															0

Access Types Legend

Table 4-1625. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU4	RO	0h	Reserved
0	IECS	WO	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. (IECS - Interrupt Enable Clear Shadow Register)

4.16.83 MCAN1_CFG_SS_IE Register (Offset = 18h) [reset = h]

Short Description: SS_IE

Long Description:

Return to Summary Table

Table 4-1626. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8018h

Figure 4-772. MCAN1_CFG_SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
RO															RW
0															0

Access Types Legend

Table 4-1627. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU5	RO	0h	Reserved
0	IE	RW	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. (IE - Interrupt Enable Register)

4.16.84 MCAN1_CFG_SS_IES Register (Offset = 1Ch) [reset = h]

Short Description: SS_IES

Long Description:

Return to Summary Table

Table 4-1628. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 801Ch

Figure 4-773. MCAN1_CFG_SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
RO															RO
0															0

Access Types Legend

Table 4-1629. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU6	RO	0h	Reserved
0	IES	RO	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. (IES - Interrupt Enable Status)

4.16.85 MCAN1_CFG_SS_EOI Register (Offset = 20h) [reset = h]

Short Description: SS_EOI

Long Description:

Return to Summary Table

Table 4-1630. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8020h

Figure 4-774. MCAN1_CFG_SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
RO								WO							
0								0							

Access Types Legend

Table 4-1631. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU7	RO	0h	Reserved
7 - 0	EOI	WO	0h	Write with bit position of targeted interrupt. (E.g. Ext TS is bit 0).Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi(0): EOI value for External TS interrupt mcan_0_eoi(1): EOI value for mcan[0] interrupt mcan_1_eoi(2): EOI value for mcan[1] interrupt(EOI - End Of Interrupt)

4.16.86 MCAN1_CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = h]

Short Description: SS_EXT_TS_PS

Long Description:

Return to Summary Table

Table 4-1632. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8024h

Figure 4-775. MCAN1_CFG_SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
RW															
0															

Access Types Legend

Table 4-1633. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU8	RO	0h	Reserved
23 - 0	PRESCALE	RW	0h	External Timestamp Prescaler reload value.External Timestamp count rate is host clock rate divided by this valuewith one exception: a value of 0 has the same effect as 1 .

4.16.87 MCAN1_CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = h]

Short Description: SS_EXT_TS_USIC

Long Description:

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Table 4-1634. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8028h

Figure 4-776. MCAN1_CFG_SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
RO											RO				
0											0				

Access Types Legend

Table 4-1635. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU9	RO	0h	Reserved
4 - 0	EXT_TS_INTR_CNTR	RO	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt (EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter)

4.16.88 MCAN1_CFG_CREL Register (Offset = 200h) [reset = h]

Short Description: CREL

Long Description:

Return to Summary Table

Table 4-1636. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8200h

Figure 4-777. MCAN1_CFG_CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
RO				RO				RO				RO			
11				10				11				1000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
RO								RO							
110								1000							

Access Types Legend

Table 4-1637. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	REL	RO	Bh	Core Release
27 - 24	STEP	RO	Ah	Step of Core Release
23 - 20	SUBSTEP	RO	Bh	Sub-Step of Core Release
19 - 16	YEAR	RO	3E8h	Time Stamp Year
15 - 8	MON	RO	6Eh	Time Stamp Month
7 - 0	DAY	RO	3E8h	Time Stamp Day

4.16.89 MCAN1_CFG_ENDN Register (Offset = 204h) [reset = h]

Short Description: ENDN

Long Description:

Return to Summary Table

Table 4-1638. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8204h

Figure 4-778. MCAN1_CFG_ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
RO															
10000111011001010100001100100001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
RO															
10000111011001010100001100100001															

Access Types Legend

Table 4-1639. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ETV	RO	7E3819F3A 12CEB3649 491171A1h	Endianess test value

4.16.90 MCAN1_CFG_CUST Register (Offset = 208h) [reset = h]

Short Description: CUST

Long Description:

Return to Summary Table

Table 4-1640. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8208h

Figure 4-779. MCAN1_CFG_CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
RO															
0															

Access Types Legend

Table 4-1641. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUST	RO	0h	Custom

4.16.91 MCAN1_CFG_DBTP Register (Offset = 20Ch) [reset = h]

Short Description: DBTP

Long Description:

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Table 4-1642. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 820Ch

Figure 4-780. MCAN1_CFG_DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
RO								RW	RO		RW				
0								0	0		0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2				DSJW			
RO			RW					RW				RW			
0			1010					11				11			

Access Types Legend

Table 4-1643. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU13	RO	0h	Reserved
23	TDC	RW	0h	Transmitter Delay Compensation
22 - 21	NU12	RO	0h	Reserved
20 - 16	DBRP	RW	0h	Data Baud Rate Prescaler
15 - 13	NU11	RO	0h	Reserved
12 - 8	DTSEG1	RW	3F2h	Data time segment before smaple point
7 - 4	DTSEG2	RW	Bh	Data time segment after sample point
3 - 0	DSJW	RW	Bh	Data resynchronization Jump Width

4.16.92 MCAN1_CFG_TEST Register (Offset = 210h) [reset = h]

Short Description: TEST

Long Description:

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Table 4-1644. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8210h

Figure 4-781. MCAN1_CFG_TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
RO								RO	RW		RW	RO			
0								0	0		0	0			

Access Types Legend

Table 4-1645. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU15	RO	0h	Reserved
7	RX	RO	0h	Receive Pin
6 - 5	TX	RW	0h	Control of Transmit Pin
4	LBCK	RW	0h	Loop Back Mode
3 - 0	NU14	RO	0h	Reserved

4.16.93 MCAN1_CFG_RWD Register (Offset = 214h) [reset = h]

Short Description: RWD

Long Description:

Return to Summary Table

Table 4-1646. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8214h

Figure 4-782. MCAN1_CFG_RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
RO								RW							
0								0							

Access Types Legend

Table 4-1647. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU16	RO	0h	Reserved
15 - 8	WDV	RO	0h	Watchdog Value
7 - 0	WDC	RW	0h	Watchdog Counter Value

4.16.94 MCAN1_CFG_CCCR Register (Offset = 218h) [reset = h]

Short Description: CCCR

Long Description:

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Table 4-1648. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8218h

Figure 4-783. MCAN1_CFG_CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
RW	RW	RW	RW	RO		RW	RW	RW	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0		0	0	0	0	0	0	0	0	0	1

Access Types Legend

Table 4-1649. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU18	RW	0h	Reserved
14	TXP	RW	0h	Transmit Pause
13	EFBI	RW	0h	Edge Filtering durign Bus Integration
12	PXHD	RW	0h	Protocol Exception Handling Disable
11 - 10	NU17	RO	0h	Reserved
9	BRSE	RW	0h	Bit Rate Switch Enable
8	FDOE	RW	0h	FD Operation Enable
7	TEST	RW	0h	Test Mode enable
6	DAR	RW	0h	Disable Automatic Regransmission
5	MON	RW	0h	Bus Monitoring Mode
4	CSR	RW	0h	Clock Stop Request
3	CSA	RO	0h	Clock Stop Acknowledge
2	ASM	RW	0h	Restriced Operation Mode
1	CCE	RW	0h	Configuration Change Enable
0	INIT	RW	1h	Initialization

4.16.95 MCAN1_CFG_NBTP Register (Offset = 21Ch) [reset = h]

Short Description: NBTP

Long Description:

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Table 4-1650. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 821Ch

Figure 4-784. MCAN1_CFG_NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW								NBRP							
RW								RW							
11								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
RW								RO	RW						
1010								0	11						

Access Types Legend

Table 4-1651. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NSJW	RW	Bh	Nominal Resynchronization Jump Width
24 - 16	NBRP	RW	0h	Nominal Baud Rate Prescaler
15 - 8	NTSEG1	RW	3F2h	Nominal Time segment before sample point
7	NU19	RO	0h	Reserved
6 - 0	NTSEG2	RW	Bh	Nominal Time segment after sample point

4.16.96 MCAN1_CFG_TSCC Register (Offset = 220h) [reset = h]

Short Description: TSCC

Long Description:

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Table 4-1652. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8220h

Figure 4-785. MCAN1_CFG_TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
RO														RW	
0														0	

Access Types Legend

Table 4-1653. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU21	RO	0h	Reserved
19 - 16	TCP	RW	0h	Timestamp Counter Prescaler
15 - 2	NU20	RO	0h	Reserved
1 - 0	TSS	RW	0h	Timestamp Select

4.16.97 MCAN1_CFG_TSCV Register (Offset = 224h) [reset = h]

Short Description: TSCV

Long Description:

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Table 4-1654. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8224h

Figure 4-786. MCAN1_CFG_TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
RW															
0															

Access Types Legend

Table 4-1655. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU22	RO	0h	Reserved
15 - 0	TSC	RW	0h	Timestamp Counter

4.16.98 MCAN1_CFG_TOCC Register (Offset = 228h) [reset = h]

Short Description: TOCC

Long Description:

Return to Summary Table

Table 4-1656. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8228h

Figure 4-787. MCAN1_CFG_TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
RO													RW		RW
0													0		0

Access Types Legend

Table 4-1657. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TOP	RW	3F28CB715 71C7h	Timeout Period
15 - 3	NU23	RO	0h	Reserved
2 - 1	TOS	RW	0h	Timeout Select
0	ETOC	RW	0h	Enable Timeout Counter

4.16.99 MCAN1_CFG_TOCV Register (Offset = 22Ch) [reset = h]

Short Description: TOCV

Long Description:

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Table 4-1658. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 822Ch

Figure 4-788. MCAN1_CFG_TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
RW															
1111111111111111															

Access Types Legend

Table 4-1659. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU24	RO	0h	Reserved
15 - 0	TOC	RW	3F28CB715 71C7h	Timeout Counter

4.16.100 MCAN1_CFG_RES00 Register (Offset = 230h) [reset = h]

Short Description: RES00

Long Description:

Return to Summary Table

Table 4-1660. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8230h

Figure 4-789. MCAN1_CFG_RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
RO															
0															

Access Types Legend

Table 4-1661. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES00	RO	0h	Reserved

4.16.101 MCAN1_CFG_RES01 Register (Offset = 234h) [reset = h]

Short Description: RES01

Long Description:

Return to Summary Table

Table 4-1662. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8234h

Figure 4-790. MCAN1_CFG_RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
RO															
0															

Access Types Legend

Table 4-1663. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES01	RO	0h	Reserved

4.16.102 MCAN1_CFG_RES02 Register (Offset = 238h) [reset = h]

Short Description: RES02

Long Description:

Return to Summary Table

Table 4-1664. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8238h

Figure 4-791. MCAN1_CFG_RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
RO															
0															

Access Types Legend

Table 4-1665. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES02	RO	0h	Reserved

4.16.103 MCAN1_CFG_RES03 Register (Offset = 23Ch) [reset = h]

Short Description: RES03

Long Description:

Return to Summary Table

Table 4-1666. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 823Ch

Figure 4-792. MCAN1_CFG_RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
RO															
0															

Access Types Legend

Table 4-1667. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES03	RO	0h	Reserved

4.16.104 MCAN1_CFG_ECR Register (Offset = 240h) [reset = h]

Short Description: ECR

Long Description:

Return to Summary Table

Table 4-1668. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8240h

Figure 4-793. MCAN1_CFG_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
RO	RO							RO							
0	0							0							

Access Types Legend

Table 4-1669. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU25	RO	0h	Reserved
23 - 16	CEL	RO	0h	CAN Error Logging
15	RP	RO	0h	Recieve Error Passive
14 - 8	REC	RO	0h	Recieve Error Counter
7 - 0	TEC	RO	0h	Transmit Error Counter

4.16.105 MCAN1_CFG_PSR Register (Offset = 244h) [reset = h]

Short Description: PSR

Long Description:

Return to Summary Table

Table 4-1670. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8244h

Figure 4-794. MCAN1_CFG_PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
RO									RO						
0									0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
RO	RO	RO	RO	RO	RO			RO	RO	RO	RO		RO		
0	0	0	0	0	111			0	0	0	0		111		

Access Types Legend

Table 4-1671. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 23	NU27	RO	0h	Reserved
22 - 16	TDCV	RO	0h	Transmitter Delay Compensation Value
15	NU26	RO	0h	Reserved
14	PXE	RO	0h	Protocol Exception Event
13	RFDF	RO	0h	Recieved a CAN FD Message
12	RBRS	RO	0h	BRS flag of last recieved CAN FD Message
11	RESI	RO	0h	ESI flag of last recieved CAN FD Message
10 - 8	DLEC	RO	6Fh	Data Phase Last Error Code
7	BO	RO	0h	Bus_Off status
6	EW	RO	0h	Warning Status
5	EP	RO	0h	Error Passive
4 - 3	ACT	RO	0h	Activity
2 - 0	LEC	RO	6Fh	Last Error Code

4.16.106 MCAN1_CFG_TDCR Register (Offset = 248h) [reset = h]

Short Description: TDCR

Long Description:

Return to Summary Table

Table 4-1672. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8248h

Figure 4-795. MCAN1_CFG_TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29	TDCO							NU28	TDCF						
RO	RW							RO	RW						
0	0							0	0						

Access Types Legend

Table 4-1673. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU29	RO	0h	Reserved
14 - 8	TDCO	RW	0h	Transmitter Delay Compensation Offset
7	NU28	RO	0h	Reserved
6 - 0	TDCF	RW	0h	Transmitter Delay Compensation Filter Window Length

4.16.107 MCAN1_CFG_RES04 Register (Offset = 24Ch) [reset = h]

Short Description: RES04

Long Description:

Return to Summary Table

Table 4-1674. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 824Ch

Figure 4-796. MCAN1_CFG_RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
RO															
0															

Access Types Legend

Table 4-1675. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES04	RO	0h	Reserved

4.16.108 MCAN1_CFG_IR Register (Offset = 250h) [reset = h]

Short Description: IR

Long Description:

Return to Summary Table

Table 4-1676. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8250h

Figure 4-797. MCAN1_CFG_IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1677. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU30	RO	0h	Reserved
29	ARA	RW	0h	Access to Reserved Address
28	PED	RW	0h	Protocol Error in data Phase
27	PEA	RW	0h	Protocol Error in Arbitration Phase
26	WDI	RW	0h	Watchdog Interrupt
25	BO	RW	0h	Bus_Off Status
24	EW	RW	0h	Warning Status
23	EP	RW	0h	Error Passive
22	ELO	RW	0h	Error Logging Overflow
21	BEU	RW	0h	Bit Error Uncorrected
20	BEC	RW	0h	Bit Error Corrected
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer
18	TOO	RW	0h	Timeout Occurred
17	MRAF	RW	0h	Message RAM Access Failure
16	TSW	RW	0h	Timestamp Wraparound
15	TEFL	RW	0h	Tx Event FIFO Element Lost
14	TEFF	RW	0h	Tx Event FIFO Full
13	TEFW	RW	0h	Tx Event FIFO Watermark Reached
12	TEFN	RW	0h	Tx Event FIFO New Entry
11	TFE	RW	0h	Tx FIFO Empty
10	TCF	RW	0h	Transmission Cancellation Finished
9	TC	RW	0h	Transmission Complete
8	HPM	RW	0h	High Priority Message
7	RF1L	RW	0h	Rx FIFO 1 Message Lost
6	RF1F	RW	0h	Rx FIFO 1 Full
5	RF1W	RW	0h	Rx FIFO 1 Watermark Reached
4	RF1N	RW	0h	Rx FIFO 1 New Message

Table 4-1677. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0L	RW	0h	Rx FIFO 0 Message Lost
2	RF0F	RW	0h	Rx FIFO 0 Full
1	RF0W	RW	0h	Rx FIFO 0 Watermark Reached
0	RF0N	RW	0h	Rx FIFO 0 New Message

4.16.109 MCAN1_CFG_IE Register (Offset = 254h) [reset = h]

Short Description: IE

Long Description:

Return to Summary Table

Table 4-1678. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8254h

Figure 4-798. MCAN1_CFG_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1679. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU31	RO	0h	Reserved
29	ARAE	RW	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	RW	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	RW	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	RW	0h	Watchdog Interrupt Enable
25	BOE	RW	0h	Bus_Off Status Interrupt Enable
24	EWE	RW	0h	Warning Status Interrupt Enable
23	EPE	RW	0h	Error Passive Interrupt Enable
22	ELOE	RW	0h	Error Logging Overflow Interrupt Enable
21	BEUE	RW	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	RW	0h	Bit Error Corrected Interrupt Enable
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	RW	0h	Timeout Occurred Interrupt Enable
17	MRAFE	RW	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	RW	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	RW	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	RW	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	RW	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	RW	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	RW	0h	Tx FIFO Empty Interrupt Enable
10	TCFE	RW	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	RW	0h	Transmission Completed Interrupt Enable
8	HPME	RW	0h	High Priority message Interrupt Enable
7	RF1LE	RW	0h	rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	RW	0h	Rx FIFO 1 Full Interrupt Enable

Table 4-1679. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WE	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	RW	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	RW	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	RW	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	RW	0h	Rx FIFO 0 New Message Interrupt Enable

4.16.110 MCAN1_CFG_ILS Register (Offset = 258h) [reset = h]

Short Description: ILS

Long Description:

Return to Summary Table

Table 4-1680. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8258h

Figure 4-799. MCAN1_CFG_ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1681. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU32	RO	0h	Reserved
29	ARAL	RW	0h	Accees to Reserve Address Interrupt Line
28	PEDL	RW	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	RW	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	RW	0h	Watchdog Interrupt Line
25	BOL	RW	0h	Bus_Off Status Interrupt Line
24	EWL	RW	0h	Warning Status Interrupt Line
23	EPL	RW	0h	Error Passive Interrupt Line
22	ELOL	RW	0h	Error Logging Overflow Interrupt Line
21	BEUL	RW	0h	Bit Error Uncorrected Interrupt Line
20	BECL	RW	0h	Bit Error Corrected Interrupt Line
19	DRXL	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	RW	0h	Timeout Occurred Interrupt Line
17	MRAFL	RW	0h	Message RAM Access Failure Interrupt Line
16	TSWL	RW	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	RW	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	RW	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	RW	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	RW	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	RW	0h	Tx FIFO Empty Interrupt Line
10	TCFL	RW	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	RW	0h	Transmission Completed Interrupt Line
8	HPML	RW	0h	High Priority message Interrupt Line
7	RF1LL	RW	0h	rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	RW	0h	Rx FIFO 1 Full Interrupt Line

Table 4-1681. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WL	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	RW	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	RW	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	RW	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	RW	0h	Rx FIFO 0 New Message Interrupt Line

4.16.111 MCAN1_CFG_ILE Register (Offset = 25Ch) [reset = h]

Short Description: ILE

Long Description:

Return to Summary Table

Table 4-1682. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 825Ch

Figure 4-800. MCAN1_CFG_ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1683. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU33	RO	0h	Reserved
1	EINT1	RW	0h	Enable Interrupt Line 1
0	EINT0	RW	0h	Enable Interrupt Line 0

4.16.112 MCAN1_CFG_RES05 Register (Offset = 260h) [reset = h]

Short Description: RES05

Long Description:

Return to Summary Table

Table 4-1684. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8260h

Figure 4-801. MCAN1_CFG_RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
RO															
0															

Access Types Legend

Table 4-1685. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES05	RO	0h	Reserved

4.16.113 MCAN1_CFG_RES06 Register (Offset = 264h) [reset = h]

Short Description: RES06

Long Description:

Return to Summary Table

Table 4-1686. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8264h

Figure 4-802. MCAN1_CFG_RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
RO															
0															

Access Types Legend

Table 4-1687. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES06	RO	0h	Reserved

4.16.114 MCAN1_CFG_RES07 Register (Offset = 268h) [reset = h]

Short Description: RES07

Long Description:

Return to Summary Table

Table 4-1688. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8268h

Figure 4-803. MCAN1_CFG_RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
RO															
0															

Access Types Legend

Table 4-1689. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES07	RO	0h	Reserved

4.16.115 MCAN1_CFG_RES08 Register (Offset = 26Ch) [reset = h]

Short Description: RES08

Long Description:

Return to Summary Table

Table 4-1690. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 826Ch

Figure 4-804. MCAN1_CFG_RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
RO															
0															

Access Types Legend

Table 4-1691. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES08	RO	0h	Reserved

4.16.116 MCAN1_CFG_RES09 Register (Offset = 270h) [reset = h]

Short Description: RES09

Long Description:

Return to Summary Table

Table 4-1692. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8270h

Figure 4-805. MCAN1_CFG_RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
RO															
0															

Access Types Legend

Table 4-1693. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES09	RO	0h	Reserved

4.16.117 MCAN1_CFG_RES10 Register (Offset = 274h) [reset = h]

Short Description: RES10

Long Description:

Return to Summary Table

Table 4-1694. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8274h

Figure 4-806. MCAN1_CFG_RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
RO															
0															

Access Types Legend

Table 4-1695. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES10	RO	0h	Reserved

4.16.118 MCAN1_CFG_RES11 Register (Offset = 278h) [reset = h]

Short Description: RES11

Long Description:

Return to Summary Table

Table 4-1696. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8278h

Figure 4-807. MCAN1_CFG_RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
RO															
0															

Access Types Legend

Table 4-1697. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES11	RO	0h	Reserved

4.16.119 MCAN1_CFG_RES12 Register (Offset = 27Ch) [reset = h]

Short Description: RES12

Long Description:

Return to Summary Table

Table 4-1698. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 827Ch

Figure 4-808. MCAN1_CFG_RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
RO															
0															

Access Types Legend

Table 4-1699. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES12	RO	0h	Reserved

4.16.120 MCAN1_CFG_GFC Register (Offset = 280h) [reset = h]

Short Description: GFC

Long Description:

Return to Summary Table

Table 4-1700. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8280h

Figure 4-809. MCAN1_CFG_GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
RO										RW		RW		RW	RW
0										0		0		0	0

Access Types Legend

Table 4-1701. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU34	RO	0h	Reserved
5 - 4	ANFS	RW	0h	Accept Non-matching Frames Standard
3 - 2	ANFE	RW	0h	Accept Non-matching Frames Extended
1	RRFS	RW	0h	reject Remote Frames Standard
0	RRFE	RW	0h	reject Remote Frames Extended

4.16.121 MCAN1_CFG_SIDFC Register (Offset = 284h) [reset = h]

Short Description: SIDFC

Long Description:

Return to Summary Table

Table 4-1702. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8284h

Figure 4-810. MCAN1_CFG_SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
RW														RO	
0														0	

Access Types Legend

Table 4-1703. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU36	RO	0h	Reserved
23 - 16	LSS_S	RW	0h	List Size Standard
15 - 2	FLSSA_S	RW	0h	Filter List Standard Start Address
1 - 0	NU35	RO	0h	Reserved

4.16.122 MCAN1_CFG_XIDFC Register (Offset = 288h) [reset = h]

Short Description: XIDFC

Long Description:

Return to Summary Table

Table 4-1704. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8288h

Figure 4-811. MCAN1_CFG_XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
RW														RO	
0														0	

Access Types Legend

Table 4-1705. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU38	RO	0h	Reserved
23 - 16	LSS_X	RW	0h	List Size Standard
15 - 2	FLSSA_X	RW	0h	Filter List Standard Start Address
1 - 0	NU37	RO	0h	Reserved

4.16.123 MCAN1_CFG_RES13 Register (Offset = 28Ch) [reset = h]

Short Description: RES13

Long Description:

Return to Summary Table

Table 4-1706. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 828Ch

Figure 4-812. MCAN1_CFG_RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
RO															
0															

Access Types Legend

Table 4-1707. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES13	RO	0h	Reserved

4.16.124 MCAN1_CFG_XIDAM Register (Offset = 290h) [reset = h]

Short Description: XIDAM

Long Description:

Return to Summary Table

Table 4-1708. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8290h

Figure 4-813. MCAN1_CFG_XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
RO			RW												
0			11111111111111111111111111111												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
RW															
11111111111111111111111111111															

Access Types Legend

Table 4-1709. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	NU39	RO	0h	Reserved
28 - 0	EIDM	RW	23E6E54C4 50CAD4F67 1C71C7h	Extended ID Mask

4.16.125 MCAN1_CFG_HPMS Register (Offset = 294h) [reset = h]

Short Description: HPMS

Long Description:

Return to Summary Table

Table 4-1710. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8294h

Figure 4-814. MCAN1_CFG_HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
RO	RO							RO		RO					
0	0							0		0					

Access Types Legend

Table 4-1711. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU40	RO	0h	Reserved
15	FLST	RO	0h	Filter List
14 - 8	FIDX	RO	0h	Filter Index
7 - 6	MSI	RO	0h	Message Storeage Indicator
5 - 0	BIDX	RO	0h	Buffer Index

4.16.126 MCAN1_CFG_NDAT1 Register (Offset = 298h) [reset = h]

Short Description: NDAT1

Long Description:

Return to Summary Table

Table 4-1712. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 8298h

Figure 4-815. MCAN1_CFG_NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
RW															
0															

Access Types Legend

Table 4-1713. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND0_31	RW	0h	New Data 0-31

4.16.127 MCAN1_CFG_NDAT2 Register (Offset = 29Ch) [reset = h]

Short Description: NDAT2

Long Description:

Return to Summary Table

Table 4-1714. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 829Ch

Figure 4-816. MCAN1_CFG_NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
RW															
0															

Access Types Legend

Table 4-1715. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND32_63	RW	0h	New Data 32-63

4.16.128 MCAN1_CFG_RXF0C Register (Offset = 2A0h) [reset = h]

Short Description: RXF0C

Long Description:

Return to Summary Table

Table 4-1716. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82A0h

Figure 4-817. MCAN1_CFG_RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1717. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F0WM	RW	0h	Rx FIFO 0 Watermark
23	NU42_1	RO	0h	Reserved
22 - 16	F0S	RW	0h	Rx FIFO 0 Size
15	NU42	RO	0h	Reserved
14 - 2	F0SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU41	RO	0h	Reserved

4.16.129 MCAN1_CFG_RXF0S Register (Offset = 2A4h) [reset = h]

Short Description: RXF0S

Long Description:

Return to Summary Table

Table 4-1718. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82A4h

Figure 4-818. MCAN1_CFG_RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1719. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU46	RO	0h	Reserved
25	RF0L	RO	0h	Rx FIFO 0 Message Lost
24	F0F	RO	0h	Rx FIFO 0 Full
23 - 22	NU45	RO	0h	Reserved
21 - 16	F0PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU44	RO	0h	Reserved
13 - 8	F0GI	RO	0h	Rx FIFO 0 Get Index
7	NU43	RO	0h	Reserved
6 - 0	F0FL	RO	0h	Rx FIFO 0 Fill Level

4.16.130 MCAN1_CFG_RXF0A Register (Offset = 2A8h) [reset = h]

Short Description: RXF0A

Long Description:

Return to Summary Table

Table 4-1720. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82A8h

Figure 4-819. MCAN1_CFG_RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1721. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU47	RO	0h	Reserved
5 - 0	F0AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.131 MCAN1_CFG_RXBC Register (Offset = 2ACh) [reset = h]

Short Description: RXBC

Long Description:

Return to Summary Table

Table 4-1722. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82ACh

Figure 4-820. MCAN1_CFG_RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
RW														RO	
0														0	

Access Types Legend

Table 4-1723. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU49	RO	0h	Reserved
15 - 2	RBSA	RW	0h	Rx Buffer Start Address
1 - 0	NU48	RO	0h	Reserved

4.16.132 MCAN1_CFG_RXF1C Register (Offset = 2B0h) [reset = h]

Short Description: RXF1C

Long Description:

Return to Summary Table

Table 4-1724. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82B0h

Figure 4-821. MCAN1_CFG_RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1725. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F1WM	RW	0h	Rx FIFO 0 Watermark
23	NU50_1	RO	0h	Reserved
22 - 16	F1S	RW	0h	Rx FIFO 0 Size
15	NU50	RO	0h	Reserved
14 - 2	F1SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU499	RO	0h	Reserved

4.16.133 MCAN1_CFG_RXF1S Register (Offset = 2B4h) [reset = h]

Short Description: RXF1S

Long Description:

Return to Summary Table

Table 4-1726. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82B4h

Figure 4-822. MCAN1_CFG_RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1727. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU54	RO	0h	Reserved
25	RF1L	RO	0h	Rx FIFO 0 Message Lost
24	F1F	RO	0h	Rx FIFO 0 Full
23 - 22	NU53	RO	0h	Reserved
21 - 16	F1PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU52	RO	0h	Reserved
13 - 8	F1GI	RO	0h	Rx FIFO 0 Get Index
7	NU51	RO	0h	Reserved
6 - 0	F1FL	RO	0h	Rx FIFO 0 Fill Level

4.16.134 MCAN1_CFG_RXF1A Register (Offset = 2B8h) [reset = h]

Short Description: RXF1A

Long Description:

Return to Summary Table

Table 4-1728. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82B8h

Figure 4-823. MCAN1_CFG_RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1729. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU55	RO	0h	Reserved
5 - 0	F1AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.135 MCAN1_CFG_RXESC Register (Offset = 2BCh) [reset = h]

Short Description: RXESC

Long Description:

Return to Summary Table

Table 4-1730. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82BCh

Figure 4-824. MCAN1_CFG_RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
RO					RW			RO	RW			RO	RW		
0					0			0	0			0	0		

Access Types Legend

Table 4-1731. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU58	RO	0h	Reserved
10 - 8	RBDS	RW	0h	Rx Buffer data Field Size
7	NU57	RO	0h	Reserved
6 - 4	F1DS	RW	0h	Rx FIFO 1 Data Field Size
3	NU56	RO	0h	Reserved
2 - 0	F0DS	RW	0h	Rx FIFO 0 Data Field Size

4.16.136 MCAN1_CFG_TXBC Register (Offset = 2C0h) [reset = h]

Short Description: TXBC

Long Description:

Return to Summary Table

Table 4-1732. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82C0h

Figure 4-825. MCAN1_CFG_TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
RO	RO	RO						RO		RO					
0	0	0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
RO														RO	
0														0	

Access Types Legend

Table 4-1733. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	RO	0h	Reserved
30	TFQM	RO	0h	Tx FIFO/Queue Mode
29 - 24	TFQS	RO	0h	Transmit FIFO/Queue Size
23 - 22	NU60	RO	0h	Reserved
21 - 16	NDTB	RO	0h	Number of Dedicated Transmit Buffers
15 - 2	TBSA	RO	0h	Tx Buffers Start Address
1 - 0	NU59	RO	0h	Reserved

4.16.137 MCAN1_CFG_TXFQS Register (Offset = 2C4h) [reset = h]

Short Description: TXFQS

Long Description:

Return to Summary Table

Table 4-1734. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82C4h

Figure 4-826. MCAN1_CFG_TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
RO										RO	RO				
0										0	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1735. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 22	NU64	RO	0h	Reserved
21	TFQF	RO	0h	Tx FIFO/Queue Full
20 - 16	TFQPI	RO	0h	Tx FIFO/Queue Put Index
15 - 13	NU63	RO	0h	Reserved
12 - 8	TFGI	RO	0h	Tx Queue Get Index
7 - 6	NU62	RO	0h	Reserved
5 - 0	TFFL	RO	0h	Tx FIFO Free Level

4.16.138 MCAN1_CFG_TXESC Register (Offset = 2C8h) [reset = h]

Short Description: TXESC

Long Description:

Return to Summary Table

Table 4-1736. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82C8h

Figure 4-827. MCAN1_CFG_TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
RO													RW		
0													0		

Access Types Legend

Table 4-1737. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU65	RO	0h	Reserved
2 - 0	TBDS	RW	0h	Tx Buffer Data Field Size

4.16.139 MCAN1_CFG_TXBRP Register (Offset = 2CCh) [reset = h]

Short Description: TXBRP

Long Description:

Return to Summary Table

Table 4-1738. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82CCh

Figure 4-828. MCAN1_CFG_TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
RO															
0															

Access Types Legend

Table 4-1739. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TRP	RO	0h	Transmission Request Pending

4.16.140 MCAN1_CFG_TXBAR Register (Offset = 2D0h) [reset = h]

Short Description: TXBAR

Long Description:

Return to Summary Table

Table 4-1740. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82D0h

Figure 4-829. MCAN1_CFG_TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1741. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AR	RW W0TOCLR	0h	Add request

4.16.141 MCAN1_CFG_TXBCR Register (Offset = 2D4h) [reset = h]

Short Description: TXBCR

Long Description:

Return to Summary Table

Table 4-1742. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82D4h

Figure 4-830. MCAN1_CFG_TXBCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1743. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CR	RW W0TOCLR	0h	Cancellation Request

4.16.142 MCAN1_CFG_TXBTO Register (Offset = 2D8h) [reset = h]

Short Description: TXBTO

Long Description:

Return to Summary Table

Table 4-1744. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82D8h

Figure 4-831. MCAN1_CFG_TXBTO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO															
RO															
0															

Access Types Legend

Table 4-1745. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO	RO	0h	Transmission Occurred

4.16.143 MCAN1_CFG_TXBCF Register (Offset = 2DCh) [reset = h]

Short Description: TXBCF

Long Description:

Return to Summary Table

Table 4-1746. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82DCh

Figure 4-832. MCAN1_CFG_TXBCF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF															
RO															
0															

Access Types Legend

Table 4-1747. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CF	RO	0h	Cancellation Finished

4.16.144 MCAN1_CFG_TXBTIE Register (Offset = 2E0h) [reset = h]

Short Description: TXBTIE

Long Description:

Return to Summary Table

Table 4-1748. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82E0h

Figure 4-833. MCAN1_CFG_TXBTIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE															
RW															
0															

Access Types Legend

Table 4-1749. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIE	RW	0h	Transmission Interrupt Enable

4.16.145 MCAN1_CFG_TXBCIE Register (Offset = 2E4h) [reset = h]

Short Description: TXBCIE

Long Description:

Return to Summary Table

Table 4-1750. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82E4h

Figure 4-834. MCAN1_CFG_TXBCIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE															
RW															
0															

Access Types Legend

Table 4-1751. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CFIE	RW	0h	Cancellation Finished Interrupt Enable

4.16.146 MCAN1_CFG_RES14 Register (Offset = 2E8h) [reset = h]

Short Description: RES14

Long Description:

Return to Summary Table

Table 4-1752. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82E8h

Figure 4-835. MCAN1_CFG_RES14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES14															
RO															
0															

Access Types Legend

Table 4-1753. RES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES14	RO	0h	Reserved

4.16.147 MCAN1_CFG_RES15 Register (Offset = 2ECh) [reset = h]

Short Description: RES15

Long Description:

Return to Summary Table

Table 4-1754. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82ECh

Figure 4-836. MCAN1_CFG_RES15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15															
RO															
0															

Access Types Legend

Table 4-1755. RES15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES15	RO	0h	Reserved

4.16.148 MCAN1_CFG_TXEFC Register (Offset = 2F0h) [reset = h]

Short Description: TXEFC

Long Description:

Return to Summary Table

Table 4-1756. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82F0h

Figure 4-837. MCAN1_CFG_TXEFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68		EFWM						NU67		EFS					
RW		RW						RW		RW					
0		0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFSA														NU66	
RW														RW	
0														0	

Access Types Legend

Table 4-1757. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU68	RW	0h	Reserved
29 - 24	EFWM	RW	0h	Event FIFO Watermark
23 - 22	NU67	RW	0h	Reserved
21 - 16	EFS	RW	0h	Event FIFO Size
15 - 2	EFSA	RW	0h	Event FIFO Start Address
1 - 0	NU66	RW	0h	Reserved

4.16.149 MCAN1_CFG_TXEFS Register (Offset = 2F4h) [reset = h]

Short Description: TXEFS

Long Description:

Return to Summary Table

Table 4-1758. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82F4h

Figure 4-838. MCAN1_CFG_TXEFS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU72						TEFL	EFF	NU71			EFPI				
RO						RO	RO	RO			RO				
0						0	0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU70			EFGI					NU69		EFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1759. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU72	RO	0h	Reserved
25	TEFL	RO	0h	Tx Event FIFO Element Lost
24	EFF	RO	0h	Event FIFO Full
23 - 21	NU71	RO	0h	Reserved
20 - 16	EFPI	RO	0h	Event FIFO Put Index
15 - 13	NU70	RO	0h	Reserved
12 - 8	EFGI	RO	0h	Event FIFO Get Index
7 - 6	NU69	RO	0h	Reserved
5 - 0	EFFL	RO	0h	Event FIFO FIll Level

4.16.150 MCAN1_CFG_TXEFA Register (Offset = 2F8h) [reset = h]

Short Description: TXEFA

Long Description:

Return to Summary Table

Table 4-1760. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82F8h

Figure 4-839. MCAN1_CFG_TXEFA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU73											EFAI				
RO											RO				
0											0				

Access Types Legend

Table 4-1761. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU73	RO	0h	Reserved
4 - 0	EFAI	RO	0h	Event FIFO Acknowledge Index

4.16.151 MCAN1_CFG_RES16 Register (Offset = 2FCh) [reset = h]

Short Description: RES16

Long Description:

Return to Summary Table

Table 4-1762. Instance Table

Instance Name	Physical Address
MCAN1_CFG	5261 82FCh

Figure 4-840. MCAN1_CFG_RES16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES16															
RO															
0															

Access Types Legend

Table 4-1763. RES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES16	RO	0h	Reserved

4.16.152 MCAN2_MSG_RAM_START Register (Offset = 0h) [reset = h]

Short Description: START

Long Description:

Return to Summary Table

Table 4-1764. Instance Table

Instance Name	Physical Address
MCAN2_MSG_RAM	5262 0000h

Figure 4-841. MCAN2_MSG_RAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1765. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	MCAN message mem Start address

4.16.153 MCAN2_CFG_SS_PID Register (Offset = 0h) [reset = h]

Short Description: SS_PID

Long Description:

Return to Summary Table

Table 4-1766. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8000h

Figure 4-842. MCAN2_CFG_SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		100011100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1011					1			0		1					

Access Types Legend

Table 4-1767. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	MODULE_ID	RO	1749204760h	Module ID
15 - 11	RTL	RO	3F3h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.16.154 MCAN2_CFG_SS_CTRL Register (Offset = 4h) [reset = h]

Short Description: SS_CTRL

Long Description:

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Table 4-1768. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8004h

Figure 4-843. MCAN2_CFG_SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
RO									RW	RW	RW	RW	RO		
0									0	0	0	1	0		

Access Types Legend

Table 4-1769. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU0	RO	0h	Reserved
6	EXT_TS_CNTR_EN	RW	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	RW	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	RW	0h	Wakeup Request Enable
3	DBGSUSP_FREE	RW	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2 - 0	NU	RO	0h	Reserved

4.16.155 MCAN2_CFG_SS_STAT Register (Offset = 8h) [reset = h]

Short Description: SS_STAT

Long Description:

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Table 4-1770. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8008h

Figure 4-844. MCAN2_CFG_SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
RO													RO	RO	RO
0													1	1	0

Access Types Legend

Table 4-1771. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU1	RO	0h	Reserved
2	EN_FDOE	RO	1h	Reflects the value of mcanss_enable_fdoe configuration portx=mcanss_enable_fdoe
1	MMI_DONE	RO	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	RO	0h	Reserved

4.16.156 MCAN2_CFG_SS_ICS Register (Offset = Ch) [reset = h]

Short Description: SS_ICS

Long Description:

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Table 4-1772. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 800Ch

Figure 4-845. MCAN2_CFG_SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
RO															WO
0															0

Access Types Legend

Table 4-1773. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU2	RO	0h	Reserved
0	ICS	WO	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. (ICS - Interrupt Clear Shadow Register)

4.16.157 MCAN2_CFG_SS_IRS Register (Offset = 10h) [reset = h]

Short Description: SS_IRS

Long Description:

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Table 4-1774. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8010h

Figure 4-846. MCAN2_CFG_SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
RO															RO
0															0

Access Types Legend

Table 4-1775. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU3	RO	0h	Reserved
0	IRS	RO	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. (IRS - Interrupt Raw Status Register)

4.16.158 MCAN2_CFG_SS_IECS Register (Offset = 14h) [reset = h]

Short Description: SS_IECS

Long Description:

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Table 4-1776. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8014h

Figure 4-847. MCAN2_CFG_SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
RO															WO
0															0

Access Types Legend

Table 4-1777. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU4	RO	0h	Reserved
0	IECS	WO	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. (IECS - Interrupt Enable Clear Shadow Register)

4.16.159 MCAN2_CFG_SS_IE Register (Offset = 18h) [reset = h]

Short Description: SS_IE

Long Description:

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Table 4-1778. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8018h

Figure 4-848. MCAN2_CFG_SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
RO															RW
0															0

Access Types Legend

Table 4-1779. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU5	RO	0h	Reserved
0	IE	RW	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. (IE - Interrupt Enable Register)

4.16.160 MCAN2_CFG_SS_IES Register (Offset = 1Ch) [reset = h]

Short Description: SS_IES

Long Description:

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Table 4-1780. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 801Ch

Figure 4-849. MCAN2_CFG_SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
RO															RO
0															0

Access Types Legend

Table 4-1781. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU6	RO	0h	Reserved
0	IES	RO	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. (IES - Interrupt Enable Status)

4.16.161 MCAN2_CFG_SS_EOI Register (Offset = 20h) [reset = h]

Short Description: SS_EOI

Long Description:

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Table 4-1782. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8020h

Figure 4-850. MCAN2_CFG_SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
RO								WO							
0								0							

Access Types Legend

Table 4-1783. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU7	RO	0h	Reserved
7 - 0	EOI	WO	0h	Write with bit position of targeted interrupt. (E.g. Ext TS is bit 0).Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi(0): EOI value for External TS interrupt mcan_0_eoi(1): EOI value for mcan[0] interrupt mcan_1_eoi(2): EOI value for mcan[1] interrupt(EOI - End Of Interrupt)

4.16.162 MCAN2_CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = h]

Short Description: SS_EXT_TS_PS

Long Description:

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Table 4-1784. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8024h

Figure 4-851. MCAN2_CFG_SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
RW															
0															

Access Types Legend

Table 4-1785. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU8	RO	0h	Reserved
23 - 0	PRESCALE	RW	0h	External Timestamp Prescaler reload value.External Timestamp count rate is host clock rate divided by this valuewith one exception: a value of 0 has the same effect as 1 .

4.16.163 MCAN2_CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = h]

Short Description: SS_EXT_TS_USIC

Long Description:

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Table 4-1786. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8028h

Figure 4-852. MCAN2_CFG_SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
RO											RO				
0											0				

Access Types Legend

Table 4-1787. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU9	RO	0h	Reserved
4 - 0	EXT_TS_INTR_CNTR	RO	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt (EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter)

4.16.164 MCAN2_CFG_CREL Register (Offset = 200h) [reset = h]

Short Description: CREL

Long Description:

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Table 4-1788. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8200h

Figure 4-853. MCAN2_CFG_CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
RO				RO				RO				RO			
11				10				11				1000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
RO								RO							
110								1000							

Access Types Legend

Table 4-1789. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	REL	RO	Bh	Core Release
27 - 24	STEP	RO	Ah	Step of Core Release
23 - 20	SUBSTEP	RO	Bh	Sub-Step of Core Release
19 - 16	YEAR	RO	3E8h	Time Stamp Year
15 - 8	MON	RO	6Eh	Time Stamp Month
7 - 0	DAY	RO	3E8h	Time Stamp Day

4.16.165 MCAN2_CFG_ENDN Register (Offset = 204h) [reset = h]

Short Description: ENDN

Long Description:

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Table 4-1790. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8204h

Figure 4-854. MCAN2_CFG_ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
RO															
10000111011001010100001100100001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
RO															
10000111011001010100001100100001															

Access Types Legend

Table 4-1791. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ETV	RO	7E3819F3A 12CEB3649 491171A1h	Endianess test value

4.16.166 MCAN2_CFG_CUST Register (Offset = 208h) [reset = h]

Short Description: CUST

Long Description:

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Table 4-1792. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8208h

Figure 4-855. MCAN2_CFG_CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
RO															
0															

Access Types Legend

Table 4-1793. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUST	RO	0h	Custom

4.16.167 MCAN2_CFG_DBTP Register (Offset = 20Ch) [reset = h]

Short Description: DBTP

Long Description:

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Table 4-1794. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 820Ch

Figure 4-856. MCAN2_CFG_DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
RO								RW	RO		RW				
0								0	0		0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2				DSJW			
RO			RW					RW				RW			
0			1010					11				11			

Access Types Legend

Table 4-1795. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU13	RO	0h	Reserved
23	TDC	RW	0h	Transmitter Delay Compensation
22 - 21	NU12	RO	0h	Reserved
20 - 16	DBRP	RW	0h	Data Baud Rate Prescaler
15 - 13	NU11	RO	0h	Reserved
12 - 8	DTSEG1	RW	3F2h	Data time segment before smaple point
7 - 4	DTSEG2	RW	Bh	Data time segment after sample point
3 - 0	DSJW	RW	Bh	Data resynchronization Jump Width

4.16.168 MCAN2_CFG_TEST Register (Offset = 210h) [reset = h]

Short Description: TEST

Long Description:

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Table 4-1796. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8210h

Figure 4-857. MCAN2_CFG_TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
RO								RO	RW		RW	RO			
0								0	0		0	0			

Access Types Legend

Table 4-1797. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU15	RO	0h	Reserved
7	RX	RO	0h	Receive Pin
6 - 5	TX	RW	0h	Control of Transmit Pin
4	LBCK	RW	0h	Loop Back Mode
3 - 0	NU14	RO	0h	Reserved

4.16.169 MCAN2_CFG_RWD Register (Offset = 214h) [reset = h]

Short Description: RWD

Long Description:

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Table 4-1798. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8214h

Figure 4-858. MCAN2_CFG_RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
RO								RW							
0								0							

Access Types Legend

Table 4-1799. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU16	RO	0h	Reserved
15 - 8	WDV	RO	0h	Watchdog Value
7 - 0	WDC	RW	0h	Watchdog Counter Value

4.16.170 MCAN2_CFG_CCCR Register (Offset = 218h) [reset = h]

Short Description: CCCR

Long Description:

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Table 4-1800. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8218h

Figure 4-859. MCAN2_CFG_CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
RW	RW	RW	RW	RO		RW	RW	RW	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0		0	0	0	0	0	0	0	0	0	1

Access Types Legend

Table 4-1801. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU18	RW	0h	Reserved
14	TXP	RW	0h	Transmit Pause
13	EFBI	RW	0h	Edge Filtering durign Bus Integration
12	PXHD	RW	0h	Protocol Exception Handling Disable
11 - 10	NU17	RO	0h	Reserved
9	BRSE	RW	0h	Bit Rate Switch Enable
8	FDOE	RW	0h	FD Operation Enable
7	TEST	RW	0h	Test Mode enable
6	DAR	RW	0h	Disable Automatic Regransmission
5	MON	RW	0h	Bus Monitoring Mode
4	CSR	RW	0h	Clock Stop Request
3	CSA	RO	0h	Clock Stop Acknowledge
2	ASM	RW	0h	Restriced Operation Mode
1	CCE	RW	0h	Configuration Change Enable
0	INIT	RW	1h	Initialization

4.16.171 MCAN2_CFG_NBTP Register (Offset = 21Ch) [reset = h]

Short Description: NBTP

Long Description:

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Table 4-1802. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 821Ch

Figure 4-860. MCAN2_CFG_NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW								NBRP							
RW								RW							
11								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
RW								RO	RW						
1010								0	11						

Access Types Legend

Table 4-1803. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NSJW	RW	Bh	Nominal Resynchronization Jump Width
24 - 16	NBRP	RW	0h	Nominal Baud Rate Prescaler
15 - 8	NTSEG1	RW	3F2h	Nominal Time segment before sample point
7	NU19	RO	0h	Reserved
6 - 0	NTSEG2	RW	Bh	Nominal Time segment after sample point

4.16.172 MCAN2_CFG_TSCC Register (Offset = 220h) [reset = h]

Short Description: TSCC

Long Description:

Return to Summary Table

Table 4-1804. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8220h

Figure 4-861. MCAN2_CFG_TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
RO														RW	
0														0	

Access Types Legend

Table 4-1805. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU21	RO	0h	Reserved
19 - 16	TCP	RW	0h	Timestamp Counter Prescaler
15 - 2	NU20	RO	0h	Reserved
1 - 0	TSS	RW	0h	Timestamp Select

4.16.173 MCAN2_CFG_TSCV Register (Offset = 224h) [reset = h]

Short Description: TSCV

Long Description:

Return to Summary Table

Table 4-1806. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8224h

Figure 4-862. MCAN2_CFG_TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
RW															
0															

Access Types Legend

Table 4-1807. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU22	RO	0h	Reserved
15 - 0	TSC	RW	0h	Timestamp Counter

4.16.174 MCAN2_CFG_TOCC Register (Offset = 228h) [reset = h]

Short Description: TOCC

Long Description:

Return to Summary Table

Table 4-1808. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8228h

Figure 4-863. MCAN2_CFG_TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
RO													RW		RW
0													0		0

Access Types Legend

Table 4-1809. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TOP	RW	3F28CB715 71C7h	Timeout Period
15 - 3	NU23	RO	0h	Reserved
2 - 1	TOS	RW	0h	Timeout Select
0	ETOC	RW	0h	Enable Timeout Counter

4.16.175 MCAN2_CFG_TOCV Register (Offset = 22Ch) [reset = h]

Short Description: TOCV

Long Description:

Return to Summary Table

Table 4-1810. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 822Ch

Figure 4-864. MCAN2_CFG_TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
RW															
1111111111111111															

Access Types Legend

Table 4-1811. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU24	RO	0h	Reserved
15 - 0	TOC	RW	3F28CB715 71C7h	Timeout Counter

4.16.176 MCAN2_CFG_RES00 Register (Offset = 230h) [reset = h]

Short Description: RES00

Long Description:

Return to Summary Table

Table 4-1812. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8230h

Figure 4-865. MCAN2_CFG_RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
RO															
0															

Access Types Legend

Table 4-1813. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES00	RO	0h	Reserved

4.16.177 MCAN2_CFG_RES01 Register (Offset = 234h) [reset = h]

Short Description: RES01

Long Description:

Return to Summary Table

Table 4-1814. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8234h

Figure 4-866. MCAN2_CFG_RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
RO															
0															

Access Types Legend

Table 4-1815. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES01	RO	0h	Reserved

4.16.178 MCAN2_CFG_RES02 Register (Offset = 238h) [reset = h]

Short Description: RES02

Long Description:

Return to Summary Table

Table 4-1816. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8238h

Figure 4-867. MCAN2_CFG_RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
RO															
0															

Access Types Legend

Table 4-1817. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES02	RO	0h	Reserved

4.16.179 MCAN2_CFG_RES03 Register (Offset = 23Ch) [reset = h]

Short Description: RES03

Long Description:

Return to Summary Table

Table 4-1818. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 823Ch

Figure 4-868. MCAN2_CFG_RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
RO															
0															

Access Types Legend

Table 4-1819. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES03	RO	0h	Reserved

4.16.180 MCAN2_CFG_ECR Register (Offset = 240h) [reset = h]

Short Description: ECR

Long Description:

Return to Summary Table

Table 4-1820. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8240h

Figure 4-869. MCAN2_CFG_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
RO	RO							RO							
0	0							0							

Access Types Legend

Table 4-1821. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU25	RO	0h	Reserved
23 - 16	CEL	RO	0h	CAN Error Logging
15	RP	RO	0h	Recieve Error Passive
14 - 8	REC	RO	0h	Recieve Error Counter
7 - 0	TEC	RO	0h	Transmit Error Counter

4.16.181 MCAN2_CFG_PSR Register (Offset = 244h) [reset = h]

Short Description: PSR

Long Description:

Return to Summary Table

Table 4-1822. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8244h

Figure 4-870. MCAN2_CFG_PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
RO									RO						
0									0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
RO	RO	RO	RO	RO	RO			RO	RO	RO	RO		RO		
0	0	0	0	0	111			0	0	0	0		111		

Access Types Legend

Table 4-1823. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 23	NU27	RO	0h	Reserved
22 - 16	TDCV	RO	0h	Transmitter Delay Compensation Value
15	NU26	RO	0h	Reserved
14	PXE	RO	0h	Protocol Exception Event
13	RFDF	RO	0h	Recieved a CAN FD Message
12	RBRS	RO	0h	BRS flag of last recieved CAN FD Message
11	RESI	RO	0h	ESI flag of last recieved CAN FD Message
10 - 8	DLEC	RO	6Fh	Data Phase Last Error Code
7	BO	RO	0h	Bus_Off status
6	EW	RO	0h	Warning Status
5	EP	RO	0h	Error Passive
4 - 3	ACT	RO	0h	Activity
2 - 0	LEC	RO	6Fh	Last Error Code

4.16.182 MCAN2_CFG_TDCR Register (Offset = 248h) [reset = h]

Short Description: TDCR

Long Description:

Return to Summary Table

Table 4-1824. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8248h

Figure 4-871. MCAN2_CFG_TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29	TDCO							NU28	TDCF						
RO	RW							RO	RW						
0	0							0	0						

Access Types Legend

Table 4-1825. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU29	RO	0h	Reserved
14 - 8	TDCO	RW	0h	Transmitter Delay Compensation Offset
7	NU28	RO	0h	Reserved
6 - 0	TDCF	RW	0h	Transmitter Delay Compensation Filter Window Length

4.16.183 MCAN2_CFG_RES04 Register (Offset = 24Ch) [reset = h]

Short Description: RES04

Long Description:

Return to Summary Table

Table 4-1826. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 824Ch

Figure 4-872. MCAN2_CFG_RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
RO															
0															

Access Types Legend

Table 4-1827. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES04	RO	0h	Reserved

4.16.184 MCAN2_CFG_IR Register (Offset = 250h) [reset = h]

Short Description: IR

Long Description:

Return to Summary Table

Table 4-1828. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8250h

Figure 4-873. MCAN2_CFG_IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1829. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU30	RO	0h	Reserved
29	ARA	RW	0h	Access to Reserved Address
28	PED	RW	0h	Protocol Error in data Phase
27	PEA	RW	0h	Protocol Error in Arbitration Phase
26	WDI	RW	0h	Watchdog Interrupt
25	BO	RW	0h	Bus_Off Status
24	EW	RW	0h	Warning Status
23	EP	RW	0h	Error Passive
22	ELO	RW	0h	Error Logging Overflow
21	BEU	RW	0h	Bit Error Uncorrected
20	BEC	RW	0h	Bit Error Corrected
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer
18	TOO	RW	0h	Timeout Occurred
17	MRAF	RW	0h	Message RAM Access Failure
16	TSW	RW	0h	Timestamp Wraparound
15	TEFL	RW	0h	Tx Event FIFO Element Lost
14	TEFF	RW	0h	Tx Event FIFO Full
13	TEFW	RW	0h	Tx Event FIFO Watermark Reached
12	TEFN	RW	0h	Tx Event FIFO New Entry
11	TFE	RW	0h	Tx FIFO Empty
10	TCF	RW	0h	Transmission Cancellation Finished
9	TC	RW	0h	Transmission Complete
8	HPM	RW	0h	High Priority Message
7	RF1L	RW	0h	Rx FIFO 1 Message Lost
6	RF1F	RW	0h	Rx FIFO 1 Full
5	RF1W	RW	0h	Rx FIFO 1 Watermark Reached
4	RF1N	RW	0h	Rx FIFO 1 New Message

Table 4-1829. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0L	RW	0h	Rx FIFO 0 Message Lost
2	RF0F	RW	0h	Rx FIFO 0 Full
1	RF0W	RW	0h	Rx FIFO 0 Watermark Reached
0	RF0N	RW	0h	Rx FIFO 0 New Message

4.16.185 MCAN2_CFG_IE Register (Offset = 254h) [reset = h]

Short Description: IE

Long Description:

Return to Summary Table

Table 4-1830. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8254h

Figure 4-874. MCAN2_CFG_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1831. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU31	RO	0h	Reserved
29	ARAE	RW	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	RW	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	RW	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	RW	0h	Watchdog Interrupt Enable
25	BOE	RW	0h	Bus_Off Status Interrupt Enable
24	EWE	RW	0h	Warning Status Interrupt Enable
23	EPE	RW	0h	Error Passive Interrupt Enable
22	ELOE	RW	0h	Error Logging Overflow Interrupt Enable
21	BEUE	RW	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	RW	0h	Bit Error Corrected Interrupt Enable
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	RW	0h	Timeout Occurred Interrupt Enable
17	MRAFE	RW	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	RW	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	RW	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	RW	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	RW	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	RW	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	RW	0h	Tx FIFO Empty Interrupt Enable
10	TCFE	RW	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	RW	0h	Transmission Completed Interrupt Enable
8	HPME	RW	0h	High Priority message Interrupt Enable
7	RF1LE	RW	0h	rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	RW	0h	Rx FIFO 1 Full Interrupt Enable

Table 4-1831. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WE	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	RW	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	RW	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	RW	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	RW	0h	Rx FIFO 0 New Message Interrupt Enable

4.16.186 MCAN2_CFG_ILS Register (Offset = 258h) [reset = h]

Short Description: ILS

Long Description:

Return to Summary Table

Table 4-1832. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8258h

Figure 4-875. MCAN2_CFG_ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1833. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU32	RO	0h	Reserved
29	ARAL	RW	0h	Accees to Reserve Address Interrupt Line
28	PEDL	RW	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	RW	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	RW	0h	Watchdog Interrupt Line
25	BOL	RW	0h	Bus_Off Status Interrupt Line
24	EWL	RW	0h	Warning Status Interrupt Line
23	EPL	RW	0h	Error Passive Interrupt Line
22	ELOL	RW	0h	Error Logging Overflow Interrupt Line
21	BEUL	RW	0h	Bit Error Uncorrected Interrupt Line
20	BECL	RW	0h	Bit Error Corrected Interrupt Line
19	DRXL	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	RW	0h	Timeout Occurred Interrupt Line
17	MRAFL	RW	0h	Message RAM Access Failure Interrupt Line
16	TSWL	RW	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	RW	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	RW	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	RW	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	RW	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	RW	0h	Tx FIFO Empty Interrupt Line
10	TCFL	RW	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	RW	0h	Transmission Completed Interrupt Line
8	HPML	RW	0h	High Priority message Interrupt Line
7	RF1LL	RW	0h	rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	RW	0h	Rx FIFO 1 Full Interrupt Line

Table 4-1833. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WL	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	RW	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	RW	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	RW	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	RW	0h	Rx FIFO 0 New Message Interrupt Line

4.16.187 MCAN2_CFG_ILE Register (Offset = 25Ch) [reset = h]

Short Description: ILE

Long Description:

Return to Summary Table

Table 4-1834. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 825Ch

Figure 4-876. MCAN2_CFG_ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1835. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU33	RO	0h	Reserved
1	EINT1	RW	0h	Enable Interrupt Line 1
0	EINT0	RW	0h	Enable Interrupt Line 0

4.16.188 MCAN2_CFG_RES05 Register (Offset = 260h) [reset = h]

Short Description: RES05

Long Description:

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Table 4-1836. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8260h

Figure 4-877. MCAN2_CFG_RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
RO															
0															

Access Types Legend

Table 4-1837. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES05	RO	0h	Reserved

4.16.189 MCAN2_CFG_RES06 Register (Offset = 264h) [reset = h]

Short Description: RES06

Long Description:

Return to Summary Table

Table 4-1838. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8264h

Figure 4-878. MCAN2_CFG_RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
RO															
0															

Access Types Legend

Table 4-1839. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES06	RO	0h	Reserved

4.16.190 MCAN2_CFG_RES07 Register (Offset = 268h) [reset = h]

Short Description: RES07

Long Description:

Return to Summary Table

Table 4-1840. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8268h

Figure 4-879. MCAN2_CFG_RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
RO															
0															

Access Types Legend

Table 4-1841. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES07	RO	0h	Reserved

4.16.191 MCAN2_CFG_RES08 Register (Offset = 26Ch) [reset = h]

Short Description: RES08

Long Description:

Return to Summary Table

Table 4-1842. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 826Ch

Figure 4-880. MCAN2_CFG_RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
RO															
0															

Access Types Legend

Table 4-1843. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES08	RO	0h	Reserved

4.16.192 MCAN2_CFG_RES09 Register (Offset = 270h) [reset = h]

Short Description: RES09

Long Description:

Return to Summary Table

Table 4-1844. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8270h

Figure 4-881. MCAN2_CFG_RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
RO															
0															

Access Types Legend

Table 4-1845. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES09	RO	0h	Reserved

4.16.193 MCAN2_CFG_RES10 Register (Offset = 274h) [reset = h]

Short Description: RES10

Long Description:

Return to Summary Table

Table 4-1846. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8274h

Figure 4-882. MCAN2_CFG_RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
RO															
0															

Access Types Legend

Table 4-1847. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES10	RO	0h	Reserved

4.16.194 MCAN2_CFG_RES11 Register (Offset = 278h) [reset = h]

Short Description: RES11

Long Description:

Return to Summary Table

Table 4-1848. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8278h

Figure 4-883. MCAN2_CFG_RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
RO															
0															

Access Types Legend

Table 4-1849. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES11	RO	0h	Reserved

4.16.195 MCAN2_CFG_RES12 Register (Offset = 27Ch) [reset = h]

Short Description: RES12

Long Description:

Return to Summary Table

Table 4-1850. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 827Ch

Figure 4-884. MCAN2_CFG_RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
RO															
0															

Access Types Legend

Table 4-1851. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES12	RO	0h	Reserved

4.16.196 MCAN2_CFG_GFC Register (Offset = 280h) [reset = h]

Short Description: GFC

Long Description:

Return to Summary Table

Table 4-1852. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8280h

Figure 4-885. MCAN2_CFG_GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
RO										RW		RW		RW	RW
0										0		0		0	0

Access Types Legend

Table 4-1853. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU34	RO	0h	Reserved
5 - 4	ANFS	RW	0h	Accept Non-matching Frames Standard
3 - 2	ANFE	RW	0h	Accept Non-matching Frames Extended
1	RRFS	RW	0h	reject Remote Frames Standard
0	RRFE	RW	0h	reject Remote Frames Extended

4.16.197 MCAN2_CFG_SIDFC Register (Offset = 284h) [reset = h]

Short Description: SIDFC

Long Description:

Return to Summary Table

Table 4-1854. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8284h

Figure 4-886. MCAN2_CFG_SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
RW														RO	
0														0	

Access Types Legend

Table 4-1855. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU36	RO	0h	Reserved
23 - 16	LSS_S	RW	0h	List Size Standard
15 - 2	FLSSA_S	RW	0h	Filter List Standard Start Address
1 - 0	NU35	RO	0h	Reserved

4.16.198 MCAN2_CFG_XIDFC Register (Offset = 288h) [reset = h]

Short Description: XIDFC

Long Description:

Return to Summary Table

Table 4-1856. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8288h

Figure 4-887. MCAN2_CFG_XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
RW														RO	
0														0	

Access Types Legend

Table 4-1857. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU38	RO	0h	Reserved
23 - 16	LSS_X	RW	0h	List Size Standard
15 - 2	FLSSA_X	RW	0h	Filter List Standard Start Address
1 - 0	NU37	RO	0h	Reserved

4.16.199 MCAN2_CFG_RES13 Register (Offset = 28Ch) [reset = h]

Short Description: RES13

Long Description:

Return to Summary Table

Table 4-1858. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 828Ch

Figure 4-888. MCAN2_CFG_RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
RO															
0															

Access Types Legend

Table 4-1859. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES13	RO	0h	Reserved

4.16.200 MCAN2_CFG_XIDAM Register (Offset = 290h) [reset = h]

Short Description: XIDAM

Long Description:

Return to Summary Table

Table 4-1860. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8290h

Figure 4-889. MCAN2_CFG_XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
RO			RW												
0			11111111111111111111111111111												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
RW															
11111111111111111111111111111															

Access Types Legend

Table 4-1861. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	NU39	RO	0h	Reserved
28 - 0	EIDM	RW	23E6E54C4 50CAD4F67 1C71C7h	Extended ID Mask

4.16.201 MCAN2_CFG_HPMS Register (Offset = 294h) [reset = h]

Short Description: HPMS

Long Description:

Return to Summary Table

Table 4-1862. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8294h

Figure 4-890. MCAN2_CFG_HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
RO	RO							RO		RO					
0	0							0		0					

Access Types Legend

Table 4-1863. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU40	RO	0h	Reserved
15	FLST	RO	0h	Filter List
14 - 8	FIDX	RO	0h	Filter Index
7 - 6	MSI	RO	0h	Message Storeage Indicator
5 - 0	BIDX	RO	0h	Buffer Index

4.16.202 MCAN2_CFG_NDAT1 Register (Offset = 298h) [reset = h]

Short Description: NDAT1

Long Description:

Return to Summary Table

Table 4-1864. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 8298h

Figure 4-891. MCAN2_CFG_NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
RW															
0															

Access Types Legend

Table 4-1865. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND0_31	RW	0h	New Data 0-31

4.16.203 MCAN2_CFG_NDAT2 Register (Offset = 29Ch) [reset = h]

Short Description: NDAT2

Long Description:

Return to Summary Table

Table 4-1866. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 829Ch

Figure 4-892. MCAN2_CFG_NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
RW															
0															

Access Types Legend

Table 4-1867. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND32_63	RW	0h	New Data 32-63

4.16.204 MCAN2_CFG_RXF0C Register (Offset = 2A0h) [reset = h]

Short Description: RXF0C

Long Description:

Return to Summary Table

Table 4-1868. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82A0h

Figure 4-893. MCAN2_CFG_RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1869. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F0WM	RW	0h	Rx FIFO 0 Watermark
23	NU42_1	RO	0h	Reserved
22 - 16	F0S	RW	0h	Rx FIFO 0 Size
15	NU42	RO	0h	Reserved
14 - 2	F0SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU41	RO	0h	Reserved

4.16.205 MCAN2_CFG_RXF0S Register (Offset = 2A4h) [reset = h]

Short Description: RXF0S

Long Description:

Return to Summary Table

Table 4-1870. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82A4h

Figure 4-894. MCAN2_CFG_RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1871. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU46	RO	0h	Reserved
25	RF0L	RO	0h	Rx FIFO 0 Message Lost
24	F0F	RO	0h	Rx FIFO 0 Full
23 - 22	NU45	RO	0h	Reserved
21 - 16	F0PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU44	RO	0h	Reserved
13 - 8	F0GI	RO	0h	Rx FIFO 0 Get Index
7	NU43	RO	0h	Reserved
6 - 0	F0FL	RO	0h	Rx FIFO 0 Fill Level

4.16.206 MCAN2_CFG_RXF0A Register (Offset = 2A8h) [reset = h]

Short Description: RXF0A

Long Description:

Return to Summary Table

Table 4-1872. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82A8h

Figure 4-895. MCAN2_CFG_RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1873. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU47	RO	0h	Reserved
5 - 0	F0AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.207 MCAN2_CFG_RXBC Register (Offset = 2ACh) [reset = h]

Short Description: RXBC

Long Description:

Return to Summary Table

Table 4-1874. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82ACh

Figure 4-896. MCAN2_CFG_RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
RW														RO	
0														0	

Access Types Legend

Table 4-1875. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU49	RO	0h	Reserved
15 - 2	RBSA	RW	0h	Rx Buffer Start Address
1 - 0	NU48	RO	0h	Reserved

4.16.208 MCAN2_CFG_RXF1C Register (Offset = 2B0h) [reset = h]

Short Description: RXF1C

Long Description:

Return to Summary Table

Table 4-1876. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82B0h

Figure 4-897. MCAN2_CFG_RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-1877. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F1WM	RW	0h	Rx FIFO 0 Watermark
23	NU50_1	RO	0h	Reserved
22 - 16	F1S	RW	0h	Rx FIFO 0 Size
15	NU50	RO	0h	Reserved
14 - 2	F1SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU499	RO	0h	Reserved

4.16.209 MCAN2_CFG_RXF1S Register (Offset = 2B4h) [reset = h]

Short Description: RXF1S

Long Description:

Return to Summary Table

Table 4-1878. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82B4h

Figure 4-898. MCAN2_CFG_RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-1879. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU54	RO	0h	Reserved
25	RF1L	RO	0h	Rx FIFO 0 Message Lost
24	F1F	RO	0h	Rx FIFO 0 Full
23 - 22	NU53	RO	0h	Reserved
21 - 16	F1PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU52	RO	0h	Reserved
13 - 8	F1GI	RO	0h	Rx FIFO 0 Get Index
7	NU51	RO	0h	Reserved
6 - 0	F1FL	RO	0h	Rx FIFO 0 Fill Level

4.16.210 MCAN2_CFG_RXF1A Register (Offset = 2B8h) [reset = h]

Short Description: RXF1A

Long Description:

Return to Summary Table

Table 4-1880. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82B8h

Figure 4-899. MCAN2_CFG_RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
RO										RW					
0										0					

Access Types Legend

Table 4-1881. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU55	RO	0h	Reserved
5 - 0	F1AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.211 MCAN2_CFG_RXESC Register (Offset = 2BCh) [reset = h]

Short Description: RXESC

Long Description:

Return to Summary Table

Table 4-1882. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82BCh

Figure 4-900. MCAN2_CFG_RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
RO					RW			RO	RW			RO	RW		
0					0			0	0			0	0		

Access Types Legend

Table 4-1883. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU58	RO	0h	Reserved
10 - 8	RBDS	RW	0h	Rx Buffer data Field Size
7	NU57	RO	0h	Reserved
6 - 4	F1DS	RW	0h	Rx FIFO 1 Data Field Size
3	NU56	RO	0h	Reserved
2 - 0	F0DS	RW	0h	Rx FIFO 0 Data Field Size

4.16.212 MCAN2_CFG_TXBC Register (Offset = 2C0h) [reset = h]

Short Description: TXBC

Long Description:

Return to Summary Table

Table 4-1884. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82C0h

Figure 4-901. MCAN2_CFG_TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
RO	RO	RO						RO		RO					
0	0	0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
RO														RO	
0														0	

Access Types Legend

Table 4-1885. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	RO	0h	Reserved
30	TFQM	RO	0h	Tx FIFO/Queue Mode
29 - 24	TFQS	RO	0h	Transmit FIFO/Queue Size
23 - 22	NU60	RO	0h	Reserved
21 - 16	NDTB	RO	0h	Number of Dedicated Transmit Buffers
15 - 2	TBSA	RO	0h	Tx Buffers Start Address
1 - 0	NU59	RO	0h	Reserved

4.16.213 MCAN2_CFG_TXFQS Register (Offset = 2C4h) [reset = h]

Short Description: TXFQS

Long Description:

Return to Summary Table

Table 4-1886. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82C4h

Figure 4-902. MCAN2_CFG_TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
RO										RO	RO				
0										0	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1887. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 22	NU64	RO	0h	Reserved
21	TFQF	RO	0h	Tx FIFO/Queue Full
20 - 16	TFQPI	RO	0h	Tx FIFO/Queue Put Index
15 - 13	NU63	RO	0h	Reserved
12 - 8	TFGI	RO	0h	Tx Queue Get Index
7 - 6	NU62	RO	0h	Reserved
5 - 0	TFFL	RO	0h	Tx FIFO Free Level

4.16.214 MCAN2_CFG_TXESC Register (Offset = 2C8h) [reset = h]

Short Description: TXESC

Long Description:

Return to Summary Table

Table 4-1888. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82C8h

Figure 4-903. MCAN2_CFG_TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
RO													RW		
0													0		

Access Types Legend

Table 4-1889. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU65	RO	0h	Reserved
2 - 0	TBDS	RW	0h	Tx Buffer Data Field Size

4.16.215 MCAN2_CFG_TXBRP Register (Offset = 2CCh) [reset = h]

Short Description: TXBRP

Long Description:

Return to Summary Table

Table 4-1890. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82CCh

Figure 4-904. MCAN2_CFG_TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
RO															
0															

Access Types Legend

Table 4-1891. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TRP	RO	0h	Transmission Request Pending

4.16.216 MCAN2_CFG_TXBAR Register (Offset = 2D0h) [reset = h]

Short Description: TXBAR

Long Description:

Return to Summary Table

Table 4-1892. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82D0h

Figure 4-905. MCAN2_CFG_TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1893. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AR	RW W0TOCLR	0h	Add request

4.16.217 MCAN2_CFG_TXBCR Register (Offset = 2D4h) [reset = h]

Short Description: TXBCR

Long Description:

Return to Summary Table

Table 4-1894. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82D4h

Figure 4-906. MCAN2_CFG_TXBCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-1895. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CR	RW W0TOCLR	0h	Cancellation Request

4.16.218 MCAN2_CFG_TXBTO Register (Offset = 2D8h) [reset = h]

Short Description: TXBTO

Long Description:

Return to Summary Table

Table 4-1896. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82D8h

Figure 4-907. MCAN2_CFG_TXBTO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO															
RO															
0															

Access Types Legend

Table 4-1897. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO	RO	0h	Transmission Occurred

4.16.219 MCAN2_CFG_TXBCF Register (Offset = 2DCh) [reset = h]

Short Description: TXBCF

Long Description:

Return to Summary Table

Table 4-1898. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82DCh

Figure 4-908. MCAN2_CFG_TXBCF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF															
RO															
0															

Access Types Legend

Table 4-1899. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CF	RO	0h	Cancellation Finished

4.16.220 MCAN2_CFG_TXBTIE Register (Offset = 2E0h) [reset = h]

Short Description: TXBTIE

Long Description:

Return to Summary Table

Table 4-1900. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82E0h

Figure 4-909. MCAN2_CFG_TXBTIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE															
RW															
0															

Access Types Legend

Table 4-1901. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIE	RW	0h	Transmission Interrupt Enable

4.16.221 MCAN2_CFG_TXBCIE Register (Offset = 2E4h) [reset = h]

Short Description: TXBCIE

Long Description:

Return to Summary Table

Table 4-1902. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82E4h

Figure 4-910. MCAN2_CFG_TXBCIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE															
RW															
0															

Access Types Legend

Table 4-1903. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CFIE	RW	0h	Cancellation Finished Interrupt Enable

4.16.222 MCAN2_CFG_RES14 Register (Offset = 2E8h) [reset = h]

Short Description: RES14

Long Description:

Return to Summary Table

Table 4-1904. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82E8h

Figure 4-911. MCAN2_CFG_RES14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES14															
RO															
0															

Access Types Legend

Table 4-1905. RES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES14	RO	0h	Reserved

4.16.223 MCAN2_CFG_RES15 Register (Offset = 2ECh) [reset = h]

Short Description: RES15

Long Description:

Return to Summary Table

Table 4-1906. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82ECh

Figure 4-912. MCAN2_CFG_RES15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15															
RO															
0															

Access Types Legend

Table 4-1907. RES15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES15	RO	0h	Reserved

4.16.224 MCAN2_CFG_TXEFC Register (Offset = 2F0h) [reset = h]

Short Description: TXEFC

Long Description:

Return to Summary Table

Table 4-1908. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82F0h

Figure 4-913. MCAN2_CFG_TXEFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68		EFWM						NU67		EFS					
RW		RW						RW		RW					
0		0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFSA														NU66	
RW														RW	
0														0	

Access Types Legend

Table 4-1909. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU68	RW	0h	Reserved
29 - 24	EFWM	RW	0h	Event FIFO Watermark
23 - 22	NU67	RW	0h	Reserved
21 - 16	EFS	RW	0h	Event FIFO Size
15 - 2	EFSA	RW	0h	Event FIFO Start Address
1 - 0	NU66	RW	0h	Reserved

4.16.225 MCAN2_CFG_TXEFS Register (Offset = 2F4h) [reset = h]

Short Description: TXEFS

Long Description:

Return to Summary Table

Table 4-1910. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82F4h

Figure 4-914. MCAN2_CFG_TXEFS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU72						TEFL	EFF	NU71			EFPI				
RO						RO	RO	RO			RO				
0						0	0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU70			EFGI					NU69		EFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-1911. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU72	RO	0h	Reserved
25	TEFL	RO	0h	Tx Event FIFO Element Lost
24	EFF	RO	0h	Event FIFO Full
23 - 21	NU71	RO	0h	Reserved
20 - 16	EFPI	RO	0h	Event FIFO Put Index
15 - 13	NU70	RO	0h	Reserved
12 - 8	EFGI	RO	0h	Event FIFO Get Index
7 - 6	NU69	RO	0h	Reserved
5 - 0	EFFL	RO	0h	Event FIFO FIll Level

4.16.226 MCAN2_CFG_TXEFA Register (Offset = 2F8h) [reset = h]

Short Description: TXEFA

Long Description:

Return to Summary Table

Table 4-1912. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82F8h

Figure 4-915. MCAN2_CFG_TXEFA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU73											EFAI				
RO											RO				
0											0				

Access Types Legend

Table 4-1913. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU73	RO	0h	Reserved
4 - 0	EFAI	RO	0h	Event FIFO Acknowledge Index

4.16.227 MCAN2_CFG_RES16 Register (Offset = 2FCh) [reset = h]

Short Description: RES16

Long Description:

Return to Summary Table

Table 4-1914. Instance Table

Instance Name	Physical Address
MCAN2_CFG	5262 82FCh

Figure 4-916. MCAN2_CFG_RES16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES16															
RO															
0															

Access Types Legend

Table 4-1915. RES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES16	RO	0h	Reserved

4.16.228 MCAN3_MSG_RAM_START Register (Offset = 0h) [reset = h]

Short Description: START

Long Description:

Return to Summary Table

Table 4-1916. Instance Table

Instance Name	Physical Address
MCAN3_MSG_RAM	5263 0000h

Figure 4-917. MCAN3_MSG_RAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1917. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	MCAN message mem Start address

4.16.229 MCAN3_CFG_SS_PID Register (Offset = 0h) [reset = h]

Short Description: SS_PID

Long Description:

Return to Summary Table

Table 4-1918. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8000h

Figure 4-918. MCAN3_CFG_SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		100011100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1011					1			0		1					

Access Types Legend

Table 4-1919. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	MODULE_ID	RO	1749204760h	Module ID
15 - 11	RTL	RO	3F3h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.16.230 MCAN3_CFG_SS_CTRL Register (Offset = 4h) [reset = h]

Short Description: SS_CTRL

Long Description:

Return to Summary Table

Table 4-1920. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8004h

Figure 4-919. MCAN3_CFG_SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
RO									RW	RW	RW	RW	RO		
0									0	0	0	1	0		

Access Types Legend

Table 4-1921. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU0	RO	0h	Reserved
6	EXT_TS_CNTR_EN	RW	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	RW	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	RW	0h	Wakeup Request Enable
3	DBGSUSP_FREE	RW	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2 - 0	NU	RO	0h	Reserved

4.16.231 MCAN3_CFG_SS_STAT Register (Offset = 8h) [reset = h]

Short Description: SS_STAT

Long Description:

Return to Summary Table

Table 4-1922. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8008h

Figure 4-920. MCAN3_CFG_SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
RO													RO	RO	RO
0													1	1	0

Access Types Legend

Table 4-1923. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU1	RO	0h	Reserved
2	EN_FDOE	RO	1h	Reflects the value of mcanss_enable_fdoe configuration portx=mcanss_enable_fdoe
1	MMI_DONE	RO	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	RO	0h	Reserved

4.16.232 MCAN3_CFG_SS_ICS Register (Offset = Ch) [reset = h]

Short Description: SS_ICS

Long Description:

Return to Summary Table

Table 4-1924. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 800Ch

Figure 4-921. MCAN3_CFG_SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
RO															WO
0															0

Access Types Legend

Table 4-1925. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU2	RO	0h	Reserved
0	ICS	WO	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. (ICS - Interrupt Clear Shadow Register)

4.16.233 MCAN3_CFG_SS_IRS Register (Offset = 10h) [reset = h]

Short Description: SS_IRS

Long Description:

Return to Summary Table

Table 4-1926. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8010h

Figure 4-922. MCAN3_CFG_SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
RO															RO
0															0

Access Types Legend

Table 4-1927. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU3	RO	0h	Reserved
0	IRS	RO	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. (IRS - Interrupt Raw Status Register)

4.16.234 MCAN3_CFG_SS_IECS Register (Offset = 14h) [reset = h]

Short Description: SS_IECS

Long Description:

Return to Summary Table

Table 4-1928. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8014h

Figure 4-923. MCAN3_CFG_SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
RO															WO
0															0

Access Types Legend

Table 4-1929. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU4	RO	0h	Reserved
0	IECS	WO	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. (IECS - Interrupt Enable Clear Shadow Register)

4.16.235 MCAN3_CFG_SS_IE Register (Offset = 18h) [reset = h]

Short Description: SS_IE

Long Description:

Return to Summary Table

Table 4-1930. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8018h

Figure 4-924. MCAN3_CFG_SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
RO															RW
0															0

Access Types Legend

Table 4-1931. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU5	RO	0h	Reserved
0	IE	RW	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. (IE - Interrupt Enable Register)

4.16.236 MCAN3_CFG_SS_IES Register (Offset = 1Ch) [reset = h]

Short Description: SS_IES

Long Description:

Return to Summary Table

Table 4-1932. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 801Ch

Figure 4-925. MCAN3_CFG_SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
RO															RO
0															0

Access Types Legend

Table 4-1933. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU6	RO	0h	Reserved
0	IES	RO	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. (IES - Interrupt Enable Status)

4.16.237 MCAN3_CFG_SS_EOI Register (Offset = 20h) [reset = h]

Short Description: SS_EOI

Long Description:

Return to Summary Table

Table 4-1934. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8020h

Figure 4-926. MCAN3_CFG_SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
RO								WO							
0								0							

Access Types Legend

Table 4-1935. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU7	RO	0h	Reserved
7 - 0	EOI	WO	0h	Write with bit position of targeted interrupt. (E.g. Ext TS is bit 0).Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi(0): EOI value for External TS interrupt mcan_0_eoi(1): EOI value for mcan[0] interrupt mcan_1_eoi(2): EOI value for mcan[1] interrupt(EOI - End Of Interrupt)

4.16.238 MCAN3_CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = h]

Short Description: SS_EXT_TS_PS

Long Description:

Return to Summary Table

Table 4-1936. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8024h

Figure 4-927. MCAN3_CFG_SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
RW															
0															

Access Types Legend

Table 4-1937. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU8	RO	0h	Reserved
23 - 0	PRESCALE	RW	0h	External Timestamp Prescaler reload value.External Timestamp count rate is host clock rate divided by this valuewith one exception: a value of 0 has the same effect as 1 .

4.16.239 MCAN3_CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = h]

Short Description: SS_EXT_TS_USIC

Long Description:

Return to Summary Table

Table 4-1938. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8028h

Figure 4-928. MCAN3_CFG_SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
RO											RO				
0											0				

Access Types Legend

Table 4-1939. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU9	RO	0h	Reserved
4 - 0	EXT_TS_INTR_CNTR	RO	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt (EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter)

4.16.240 MCAN3_CFG_CREL Register (Offset = 200h) [reset = h]

Short Description: CREL

Long Description:

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Table 4-1940. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8200h

Figure 4-929. MCAN3_CFG_CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
RO				RO				RO				RO			
11				10				11				1000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
RO								RO							
110								1000							

Access Types Legend

Table 4-1941. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	REL	RO	Bh	Core Release
27 - 24	STEP	RO	Ah	Step of Core Release
23 - 20	SUBSTEP	RO	Bh	Sub-Step of Core Release
19 - 16	YEAR	RO	3E8h	Time Stamp Year
15 - 8	MON	RO	6Eh	Time Stamp Month
7 - 0	DAY	RO	3E8h	Time Stamp Day

4.16.241 MCAN3_CFG_ENDN Register (Offset = 204h) [reset = h]

Short Description: ENDN

Long Description:

Return to Summary Table

Table 4-1942. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8204h

Figure 4-930. MCAN3_CFG_ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
RO															
10000111011001010100001100100001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
RO															
10000111011001010100001100100001															

Access Types Legend

Table 4-1943. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ETV	RO	7E3819F3A 12CEB3649 491171A1h	Endianess test value

4.16.242 MCAN3_CFG_CUST Register (Offset = 208h) [reset = h]

Short Description: CUST

Long Description:

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Table 4-1944. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8208h

Figure 4-931. MCAN3_CFG_CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
RO															
0															

Access Types Legend

Table 4-1945. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUST	RO	0h	Custom

4.16.243 MCAN3_CFG_DBTP Register (Offset = 20Ch) [reset = h]

Short Description: DBTP

Long Description:

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Table 4-1946. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 820Ch

Figure 4-932. MCAN3_CFG_DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
RO								RW	RO		RW				
0								0	0		0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2				DSJW			
RO			RW					RW				RW			
0			1010					11				11			

Access Types Legend

Table 4-1947. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU13	RO	0h	Reserved
23	TDC	RW	0h	Transmitter Delay Compensation
22 - 21	NU12	RO	0h	Reserved
20 - 16	DBRP	RW	0h	Data Baud Rate Prescaler
15 - 13	NU11	RO	0h	Reserved
12 - 8	DTSEG1	RW	3F2h	Data time segment before smaple point
7 - 4	DTSEG2	RW	Bh	Data time segment after sample point
3 - 0	DSJW	RW	Bh	Data resynchronization Jump Width

4.16.244 MCAN3_CFG_TEST Register (Offset = 210h) [reset = h]

Short Description: TEST

Long Description:

Return to Summary Table

Table 4-1948. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8210h

Figure 4-933. MCAN3_CFG_TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
RO								RO	RW		RW	RO			
0								0	0		0	0			

Access Types Legend

Table 4-1949. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU15	RO	0h	Reserved
7	RX	RO	0h	Receive Pin
6 - 5	TX	RW	0h	Control of Transmit Pin
4	LBCK	RW	0h	Loop Back Mode
3 - 0	NU14	RO	0h	Reserved

4.16.245 MCAN3_CFG_RWD Register (Offset = 214h) [reset = h]

Short Description: RWD

Long Description:

Return to Summary Table

Table 4-1950. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8214h

Figure 4-934. MCAN3_CFG_RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
RO								RW							
0								0							

Access Types Legend

Table 4-1951. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU16	RO	0h	Reserved
15 - 8	WDV	RO	0h	Watchdog Value
7 - 0	WDC	RW	0h	Watchdog Counter Value

4.16.246 MCAN3_CFG_CCCR Register (Offset = 218h) [reset = h]

Short Description: CCCR

Long Description:

Return to Summary Table

Table 4-1952. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8218h

Figure 4-935. MCAN3_CFG_CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
RW	RW	RW	RW	RO		RW	RW	RW	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0		0	0	0	0	0	0	0	0	0	1

Access Types Legend

Table 4-1953. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU18	RW	0h	Reserved
14	TXP	RW	0h	Transmit Pause
13	EFBI	RW	0h	Edge Filtering durign Bus Integration
12	PXHD	RW	0h	Protocol Exception Handling Disable
11 - 10	NU17	RO	0h	Reserved
9	BRSE	RW	0h	Bit Rate Switch Enable
8	FDOE	RW	0h	FD Operation Enable
7	TEST	RW	0h	Test Mode enable
6	DAR	RW	0h	Disable Automatic Regransmission
5	MON	RW	0h	Bus Monitoring Mode
4	CSR	RW	0h	Clock Stop Request
3	CSA	RO	0h	Clock Stop Acknowledge
2	ASM	RW	0h	Restriced Operation Mode
1	CCE	RW	0h	Configuration Change Enable
0	INIT	RW	1h	Initialization

4.16.247 MCAN3_CFG_NBTP Register (Offset = 21Ch) [reset = h]

Short Description: NBTP

Long Description:

Return to Summary Table

Table 4-1954. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 821Ch

Figure 4-936. MCAN3_CFG_NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW								NBRP							
RW								RW							
11								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
RW								RO	RW						
1010								0	11						

Access Types Legend

Table 4-1955. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NSJW	RW	Bh	Nominal Resynchronization Jump Width
24 - 16	NBRP	RW	0h	Nominal Baud Rate Prescaler
15 - 8	NTSEG1	RW	3F2h	Nominal Time segment before sample point
7	NU19	RO	0h	Reserved
6 - 0	NTSEG2	RW	Bh	Nominal Time segment after sample point

4.16.248 MCAN3_CFG_TSCC Register (Offset = 220h) [reset = h]

Short Description: TSCC

Long Description:

Return to Summary Table

Table 4-1956. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8220h

Figure 4-937. MCAN3_CFG_TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
RO														RW	
0														0	

Access Types Legend

Table 4-1957. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU21	RO	0h	Reserved
19 - 16	TCP	RW	0h	Timestamp Counter Prescaler
15 - 2	NU20	RO	0h	Reserved
1 - 0	TSS	RW	0h	Timestamp Select

4.16.249 MCAN3_CFG_TSCV Register (Offset = 224h) [reset = h]

Short Description: TSCV

Long Description:

Return to Summary Table

Table 4-1958. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8224h

Figure 4-938. MCAN3_CFG_TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
RW															
0															

Access Types Legend

Table 4-1959. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU22	RO	0h	Reserved
15 - 0	TSC	RW	0h	Timestamp Counter

4.16.250 MCAN3_CFG_TOCC Register (Offset = 228h) [reset = h]

Short Description: TOCC

Long Description:

Return to Summary Table

Table 4-1960. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8228h

Figure 4-939. MCAN3_CFG_TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
RO													RW		RW
0													0		0

Access Types Legend

Table 4-1961. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TOP	RW	3F28CB715 71C7h	Timeout Period
15 - 3	NU23	RO	0h	Reserved
2 - 1	TOS	RW	0h	Timeout Select
0	ETOC	RW	0h	Enable Timeout Counter

4.16.251 MCAN3_CFG_TOCV Register (Offset = 22Ch) [reset = h]

Short Description: TOCV

Long Description:

Return to Summary Table

Table 4-1962. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 822Ch

Figure 4-940. MCAN3_CFG_TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
RW															
1111111111111111															

Access Types Legend

Table 4-1963. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU24	RO	0h	Reserved
15 - 0	TOC	RW	3F28CB715 71C7h	Timeout Counter

4.16.252 MCAN3_CFG_RES00 Register (Offset = 230h) [reset = h]

Short Description: RES00

Long Description:

Return to Summary Table

Table 4-1964. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8230h

Figure 4-941. MCAN3_CFG_RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
RO															
0															

Access Types Legend

Table 4-1965. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES00	RO	0h	Reserved

4.16.253 MCAN3_CFG_RES01 Register (Offset = 234h) [reset = h]

Short Description: RES01

Long Description:

Return to Summary Table

Table 4-1966. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8234h

Figure 4-942. MCAN3_CFG_RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
RO															
0															

Access Types Legend

Table 4-1967. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES01	RO	0h	Reserved

4.16.254 MCAN3_CFG_RES02 Register (Offset = 238h) [reset = h]

Short Description: RES02

Long Description:

Return to Summary Table

Table 4-1968. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8238h

Figure 4-943. MCAN3_CFG_RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
RO															
0															

Access Types Legend

Table 4-1969. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES02	RO	0h	Reserved

4.16.255 MCAN3_CFG_RES03 Register (Offset = 23Ch) [reset = h]

Short Description: RES03

Long Description:

Return to Summary Table

Table 4-1970. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 823Ch

Figure 4-944. MCAN3_CFG_RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
RO															
0															

Access Types Legend

Table 4-1971. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES03	RO	0h	Reserved

4.16.256 MCAN3_CFG_ECR Register (Offset = 240h) [reset = h]

Short Description: ECR

Long Description:

Return to Summary Table

Table 4-1972. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8240h

Figure 4-945. MCAN3_CFG_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
RO	RO							RO							
0	0							0							

Access Types Legend

Table 4-1973. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU25	RO	0h	Reserved
23 - 16	CEL	RO	0h	CAN Error Logging
15	RP	RO	0h	Recieve Error Passive
14 - 8	REC	RO	0h	Recieve Error Counter
7 - 0	TEC	RO	0h	Transmit Error Counter

4.16.257 MCAN3_CFG_PSR Register (Offset = 244h) [reset = h]

Short Description: PSR

Long Description:

Return to Summary Table

Table 4-1974. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8244h

Figure 4-946. MCAN3_CFG_PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
RO									RO						
0									0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
RO	RO	RO	RO	RO	RO			RO	RO	RO	RO		RO		
0	0	0	0	0	111			0	0	0	0		111		

Access Types Legend

Table 4-1975. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 23	NU27	RO	0h	Reserved
22 - 16	TDCV	RO	0h	Transmitter Delay Compensation Value
15	NU26	RO	0h	Reserved
14	PXE	RO	0h	Protocol Exception Event
13	RFDF	RO	0h	Recieved a CAN FD Message
12	RBRS	RO	0h	BRS flag of last recieved CAN FD Message
11	RESI	RO	0h	ESI flag of last recieved CAN FD Message
10 - 8	DLEC	RO	6Fh	Data Phase Last Error Code
7	BO	RO	0h	Bus_Off status
6	EW	RO	0h	Warning Status
5	EP	RO	0h	Error Passive
4 - 3	ACT	RO	0h	Activity
2 - 0	LEC	RO	6Fh	Last Error Code

4.16.258 MCAN3_CFG_TDCR Register (Offset = 248h) [reset = h]

Short Description: TDCR

Long Description:

Return to Summary Table

Table 4-1976. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8248h

Figure 4-947. MCAN3_CFG_TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29				TDCO				NU28				TDCF			
RO				RW				RO				RW			
0				0				0				0			

Access Types Legend

Table 4-1977. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU29	RO	0h	Reserved
14 - 8	TDCO	RW	0h	Transmitter Delay Compensation Offset
7	NU28	RO	0h	Reserved
6 - 0	TDCF	RW	0h	Transmitter Delay Compensation Filter Window Length

4.16.259 MCAN3_CFG_RES04 Register (Offset = 24Ch) [reset = h]

Short Description: RES04

Long Description:

Return to Summary Table

Table 4-1978. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 824Ch

Figure 4-948. MCAN3_CFG_RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
RO															
0															

Access Types Legend

Table 4-1979. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES04	RO	0h	Reserved

4.16.260 MCAN3_CFG_IR Register (Offset = 250h) [reset = h]

Short Description: IR

Long Description:

Return to Summary Table

Table 4-1980. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8250h

Figure 4-949. MCAN3_CFG_IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1981. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU30	RO	0h	Reserved
29	ARA	RW	0h	Access to Reserved Address
28	PED	RW	0h	Protocol Error in data Phase
27	PEA	RW	0h	Protocol Error in Arbitration Phase
26	WDI	RW	0h	Watchdog Interrupt
25	BO	RW	0h	Bus_Off Status
24	EW	RW	0h	Warning Status
23	EP	RW	0h	Error Passive
22	ELO	RW	0h	Error Logging Overflow
21	BEU	RW	0h	Bit Error Uncorrected
20	BEC	RW	0h	Bit Error Corrected
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer
18	TOO	RW	0h	Timeout Occurred
17	MRAF	RW	0h	Message RAM Access Failure
16	TSW	RW	0h	Timestamp Wraparound
15	TEFL	RW	0h	Tx Event FIFO Element Lost
14	TEFF	RW	0h	Tx Event FIFO Full
13	TEFW	RW	0h	Tx Event FIFO Watermark Reached
12	TEFN	RW	0h	Tx Event FIFO New Entry
11	TFE	RW	0h	Tx FIFO Empty
10	TCF	RW	0h	Transmission Cancellation Finished
9	TC	RW	0h	Transmission Complete
8	HPM	RW	0h	High Priority Message
7	RF1L	RW	0h	Rx FIFO 1 Message Lost
6	RF1F	RW	0h	Rx FIFO 1 Full
5	RF1W	RW	0h	Rx FIFO 1 Watermark Reached
4	RF1N	RW	0h	Rx FIFO 1 New Message

Table 4-1981. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RF0L	RW	0h	Rx FIFO 0 Message Lost
2	RF0F	RW	0h	Rx FIFO 0 Full
1	RF0W	RW	0h	Rx FIFO 0 Watermark Reached
0	RF0N	RW	0h	Rx FIFO 0 New Message

4.16.261 MCAN3_CFG_IE Register (Offset = 254h) [reset = h]

Short Description: IE

Long Description:

Return to Summary Table

Table 4-1982. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8254h

Figure 4-950. MCAN3_CFG_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1983. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU31	RO	0h	Reserved
29	ARAE	RW	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	RW	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	RW	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	RW	0h	Watchdog Interrupt Enable
25	BOE	RW	0h	Bus_Off Status Interrupt Enable
24	EWE	RW	0h	Warning Status Interrupt Enable
23	EPE	RW	0h	Error Passive Interrupt Enable
22	ELOE	RW	0h	Error Logging Overflow Interrupt Enable
21	BEUE	RW	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	RW	0h	Bit Error Corrected Interrupt Enable
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	RW	0h	Timeout Occurred Interrupt Enable
17	MRAFE	RW	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	RW	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	RW	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	RW	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	RW	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	RW	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	RW	0h	Tx FIFO Empty Interrupt Enable
10	TCFE	RW	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	RW	0h	Transmission Completed Interrupt Enable
8	HPME	RW	0h	High Priority message Interrupt Enable
7	RF1LE	RW	0h	rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	RW	0h	Rx FIFO 1 Full Interrupt Enable

Table 4-1983. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WE	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	RW	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	RW	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	RW	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	RW	0h	Rx FIFO 0 New Message Interrupt Enable

4.16.262 MCAN3_CFG_ILS Register (Offset = 258h) [reset = h]

Short Description: ILS

Long Description:

Return to Summary Table

Table 4-1984. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8258h

Figure 4-951. MCAN3_CFG_ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1985. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU32	RO	0h	Reserved
29	ARAL	RW	0h	Accees to Reserve Address Interrupt Line
28	PEDL	RW	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	RW	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	RW	0h	Watchdog Interrupt Line
25	BOL	RW	0h	Bus_Off Status Interrupt Line
24	EWL	RW	0h	Warning Status Interrupt Line
23	EPL	RW	0h	Error Passive Interrupt Line
22	ELOL	RW	0h	Error Logging Overflow Interrupt Line
21	BEUL	RW	0h	Bit Error Uncorrected Interrupt Line
20	BECL	RW	0h	Bit Error Corrected Interrupt Line
19	DRXL	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	RW	0h	Timeout Occurred Interrupt Line
17	MRAFL	RW	0h	Message RAM Access Failure Interrupt Line
16	TSWL	RW	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	RW	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	RW	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	RW	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	RW	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	RW	0h	Tx FIFO Empty Interrupt Line
10	TCFL	RW	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	RW	0h	Transmission Completed Interrupt Line
8	HPML	RW	0h	High Priority message Interrupt Line
7	RF1LL	RW	0h	rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	RW	0h	Rx FIFO 1 Full Interrupt Line

Table 4-1985. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1WL	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	RW	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	RW	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	RW	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	RW	0h	Rx FIFO 0 New Message Interrupt Line

4.16.263 MCAN3_CFG_ILE Register (Offset = 25Ch) [reset = h]

Short Description: ILE

Long Description:

Return to Summary Table

Table 4-1986. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 825Ch

Figure 4-952. MCAN3_CFG_ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1987. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU33	RO	0h	Reserved
1	EINT1	RW	0h	Enable Interrupt Line 1
0	EINT0	RW	0h	Enable Interrupt Line 0

4.16.264 MCAN3_CFG_RES05 Register (Offset = 260h) [reset = h]

Short Description: RES05

Long Description:

Return to Summary Table

Table 4-1988. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8260h

Figure 4-953. MCAN3_CFG_RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
RO															
0															

Access Types Legend

Table 4-1989. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES05	RO	0h	Reserved

4.16.265 MCAN3_CFG_RES06 Register (Offset = 264h) [reset = h]

Short Description: RES06

Long Description:

Return to Summary Table

Table 4-1990. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8264h

Figure 4-954. MCAN3_CFG_RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
RO															
0															

Access Types Legend

Table 4-1991. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES06	RO	0h	Reserved

4.16.266 MCAN3_CFG_RES07 Register (Offset = 268h) [reset = h]

Short Description: RES07

Long Description:

Return to Summary Table

Table 4-1992. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8268h

Figure 4-955. MCAN3_CFG_RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
RO															
0															

Access Types Legend

Table 4-1993. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES07	RO	0h	Reserved

4.16.267 MCAN3_CFG_RES08 Register (Offset = 26Ch) [reset = h]

Short Description: RES08

Long Description:

Return to Summary Table

Table 4-1994. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 826Ch

Figure 4-956. MCAN3_CFG_RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
RO															
0															

Access Types Legend

Table 4-1995. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES08	RO	0h	Reserved

4.16.268 MCAN3_CFG_RES09 Register (Offset = 270h) [reset = h]

Short Description: RES09

Long Description:

Return to Summary Table

Table 4-1996. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8270h

Figure 4-957. MCAN3_CFG_RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
RO															
0															

Access Types Legend

Table 4-1997. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES09	RO	0h	Reserved

4.16.269 MCAN3_CFG_RES10 Register (Offset = 274h) [reset = h]

Short Description: RES10

Long Description:

Return to Summary Table

Table 4-1998. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8274h

Figure 4-958. MCAN3_CFG_RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
RO															
0															

Access Types Legend

Table 4-1999. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES10	RO	0h	Reserved

4.16.270 MCAN3_CFG_RES11 Register (Offset = 278h) [reset = h]

Short Description: RES11

Long Description:

Return to Summary Table

Table 4-2000. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8278h

Figure 4-959. MCAN3_CFG_RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
RO															
0															

Access Types Legend

Table 4-2001. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES11	RO	0h	Reserved

4.16.271 MCAN3_CFG_RES12 Register (Offset = 27Ch) [reset = h]

Short Description: RES12

Long Description:

Return to Summary Table

Table 4-2002. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 827Ch

Figure 4-960. MCAN3_CFG_RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
RO															
0															

Access Types Legend

Table 4-2003. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES12	RO	0h	Reserved

4.16.272 MCAN3_CFG_GFC Register (Offset = 280h) [reset = h]

Short Description: GFC

Long Description:

Return to Summary Table

Table 4-2004. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8280h

Figure 4-961. MCAN3_CFG_GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
RO										RW		RW		RW	RW
0										0		0		0	0

Access Types Legend

Table 4-2005. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU34	RO	0h	Reserved
5 - 4	ANFS	RW	0h	Accept Non-matching Frames Standard
3 - 2	ANFE	RW	0h	Accept Non-matching Frames Extended
1	RRFS	RW	0h	reject Remote Frames Standard
0	RRFE	RW	0h	reject Remote Frames Extended

4.16.273 MCAN3_CFG_SIDFC Register (Offset = 284h) [reset = h]

Short Description: SIDFC

Long Description:

Return to Summary Table

Table 4-2006. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8284h

Figure 4-962. MCAN3_CFG_SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
RW														RO	
0														0	

Access Types Legend

Table 4-2007. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU36	RO	0h	Reserved
23 - 16	LSS_S	RW	0h	List Size Standard
15 - 2	FLSSA_S	RW	0h	Filter List Standard Start Address
1 - 0	NU35	RO	0h	Reserved

4.16.274 MCAN3_CFG_XIDFC Register (Offset = 288h) [reset = h]

Short Description: XIDFC

Long Description:

Return to Summary Table

Table 4-2008. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8288h

Figure 4-963. MCAN3_CFG_XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
RW														RO	
0														0	

Access Types Legend

Table 4-2009. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU38	RO	0h	Reserved
23 - 16	LSS_X	RW	0h	List Size Standard
15 - 2	FLSSA_X	RW	0h	Filter List Standard Start Address
1 - 0	NU37	RO	0h	Reserved

4.16.275 MCAN3_CFG_RES13 Register (Offset = 28Ch) [reset = h]

Short Description: RES13

Long Description:

Return to Summary Table

Table 4-2010. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 828Ch

Figure 4-964. MCAN3_CFG_RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
RO															
0															

Access Types Legend

Table 4-2011. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES13	RO	0h	Reserved

4.16.276 MCAN3_CFG_XIDAM Register (Offset = 290h) [reset = h]

Short Description: XIDAM

Long Description:

Return to Summary Table

Table 4-2012. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8290h

Figure 4-965. MCAN3_CFG_XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
RO			RW												
0			11111111111111111111111111111												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
RW															
11111111111111111111111111111															

Access Types Legend

Table 4-2013. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	NU39	RO	0h	Reserved
28 - 0	EIDM	RW	23E6E54C4 50CAD4F67 1C71C7h	Extended ID Mask

4.16.277 MCAN3_CFG_HPMS Register (Offset = 294h) [reset = h]

Short Description: HPMS

Long Description:

Return to Summary Table

Table 4-2014. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8294h

Figure 4-966. MCAN3_CFG_HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
RO	RO							RO		RO					
0	0							0		0					

Access Types Legend

Table 4-2015. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU40	RO	0h	Reserved
15	FLST	RO	0h	Filter List
14 - 8	FIDX	RO	0h	Filter Index
7 - 6	MSI	RO	0h	Message Storeage Indicator
5 - 0	BIDX	RO	0h	Buffer Index

4.16.278 MCAN3_CFG_NDAT1 Register (Offset = 298h) [reset = h]

Short Description: NDAT1

Long Description:

Return to Summary Table

Table 4-2016. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 8298h

Figure 4-967. MCAN3_CFG_NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
RW															
0															

Access Types Legend

Table 4-2017. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND0_31	RW	0h	New Data 0-31

4.16.279 MCAN3_CFG_NDAT2 Register (Offset = 29Ch) [reset = h]

Short Description: NDAT2

Long Description:

Return to Summary Table

Table 4-2018. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 829Ch

Figure 4-968. MCAN3_CFG_NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
RW															
0															

Access Types Legend

Table 4-2019. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND32_63	RW	0h	New Data 32-63

ADVANCE INFORMATION

4.16.280 MCAN3_CFG_RXF0C Register (Offset = 2A0h) [reset = h]

Short Description: RXF0C

Long Description:

Return to Summary Table

Table 4-2020. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82A0h

Figure 4-969. MCAN3_CFG_RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-2021. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F0WM	RW	0h	Rx FIFO 0 Watermark
23	NU42_1	RO	0h	Reserved
22 - 16	F0S	RW	0h	Rx FIFO 0 Size
15	NU42	RO	0h	Reserved
14 - 2	F0SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU41	RO	0h	Reserved

4.16.281 MCAN3_CFG_RXF0S Register (Offset = 2A4h) [reset = h]

Short Description: RXF0S

Long Description:

Return to Summary Table

Table 4-2022. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82A4h

Figure 4-970. MCAN3_CFG_RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-2023. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU46	RO	0h	Reserved
25	RF0L	RO	0h	Rx FIFO 0 Message Lost
24	F0F	RO	0h	Rx FIFO 0 Full
23 - 22	NU45	RO	0h	Reserved
21 - 16	F0PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU44	RO	0h	Reserved
13 - 8	F0GI	RO	0h	Rx FIFO 0 Get Index
7	NU43	RO	0h	Reserved
6 - 0	F0FL	RO	0h	Rx FIFO 0 Fill Level

4.16.282 MCAN3_CFG_RXF0A Register (Offset = 2A8h) [reset = h]

Short Description: RXF0A

Long Description:

Return to Summary Table

Table 4-2024. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82A8h

Figure 4-971. MCAN3_CFG_RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
RO										RW					
0										0					

Access Types Legend

Table 4-2025. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU47	RO	0h	Reserved
5 - 0	F0AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.283 MCAN3_CFG_RXBC Register (Offset = 2ACh) [reset = h]

Short Description: RXBC

Long Description:

Return to Summary Table

Table 4-2026. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82ACh

Figure 4-972. MCAN3_CFG_RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
RW														RO	
0														0	

Access Types Legend

Table 4-2027. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU49	RO	0h	Reserved
15 - 2	RBSA	RW	0h	Rx Buffer Start Address
1 - 0	NU48	RO	0h	Reserved

4.16.284 MCAN3_CFG_RXF1C Register (Offset = 2B0h) [reset = h]

Short Description: RXF1C

Long Description:

Return to Summary Table

Table 4-2028. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82B0h

Figure 4-973. MCAN3_CFG_RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-2029. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F1WM	RW	0h	Rx FIFO 0 Watermark
23	NU50_1	RO	0h	Reserved
22 - 16	F1S	RW	0h	Rx FIFO 0 Size
15	NU50	RO	0h	Reserved
14 - 2	F1SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU499	RO	0h	Reserved

4.16.285 MCAN3_CFG_RXF1S Register (Offset = 2B4h) [reset = h]

Short Description: RXF1S

Long Description:

Return to Summary Table

Table 4-2030. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82B4h

Figure 4-974. MCAN3_CFG_RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-2031. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU54	RO	0h	Reserved
25	RF1L	RO	0h	Rx FIFO 0 Message Lost
24	F1F	RO	0h	Rx FIFO 0 Full
23 - 22	NU53	RO	0h	Reserved
21 - 16	F1PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU52	RO	0h	Reserved
13 - 8	F1GI	RO	0h	Rx FIFO 0 Get Index
7	NU51	RO	0h	Reserved
6 - 0	F1FL	RO	0h	Rx FIFO 0 Fill Level

4.16.286 MCAN3_CFG_RXF1A Register (Offset = 2B8h) [reset = h]

Short Description: RXF1A

Long Description:

Return to Summary Table

Table 4-2032. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82B8h

Figure 4-975. MCAN3_CFG_RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
RO										RW					
0										0					

Access Types Legend

Table 4-2033. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU55	RO	0h	Reserved
5 - 0	F1AI	RW	0h	Rx FIFO 0 Acknowledge Index

4.16.287 MCAN3_CFG_RXESC Register (Offset = 2BCh) [reset = h]

Short Description: RXESC

Long Description:

Return to Summary Table

Table 4-2034. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82BCh

Figure 4-976. MCAN3_CFG_RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
RO					RW			RO	RW			RO	RW		
0					0			0	0			0	0		

Access Types Legend

Table 4-2035. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU58	RO	0h	Reserved
10 - 8	RBDS	RW	0h	Rx Buffer data Field Size
7	NU57	RO	0h	Reserved
6 - 4	F1DS	RW	0h	Rx FIFO 1 Data Field Size
3	NU56	RO	0h	Reserved
2 - 0	F0DS	RW	0h	Rx FIFO 0 Data Field Size

4.16.288 MCAN3_CFG_TXBC Register (Offset = 2C0h) [reset = h]

Short Description: TXBC

Long Description:

Return to Summary Table

Table 4-2036. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82C0h

Figure 4-977. MCAN3_CFG_TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
RO	RO	RO						RO		RO					
0	0	0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
RO														RO	
0														0	

Access Types Legend

Table 4-2037. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	RO	0h	Reserved
30	TFQM	RO	0h	Tx FIFO/Queue Mode
29 - 24	TFQS	RO	0h	Transmit FIFO/Queue Size
23 - 22	NU60	RO	0h	Reserved
21 - 16	NDTB	RO	0h	Number of Dedicated Transmit Buffers
15 - 2	TBSA	RO	0h	Tx Buffers Start Address
1 - 0	NU59	RO	0h	Reserved

4.16.289 MCAN3_CFG_TXFQS Register (Offset = 2C4h) [reset = h]

Short Description: TXFQS

Long Description:

Return to Summary Table

Table 4-2038. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82C4h

Figure 4-978. MCAN3_CFG_TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
RO										RO	RO				
0										0	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-2039. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 22	NU64	RO	0h	Reserved
21	TFQF	RO	0h	Tx FIFO/Queue Full
20 - 16	TFQPI	RO	0h	Tx FIFO/Queue Put Index
15 - 13	NU63	RO	0h	Reserved
12 - 8	TFGI	RO	0h	Tx Queue Get Index
7 - 6	NU62	RO	0h	Reserved
5 - 0	TFFL	RO	0h	Tx FIFO Free Level

4.16.290 MCAN3_CFG_TXESC Register (Offset = 2C8h) [reset = h]

Short Description: TXESC

Long Description:

Return to Summary Table

Table 4-2040. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82C8h

Figure 4-979. MCAN3_CFG_TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
RO													RW		
0													0		

Access Types Legend

Table 4-2041. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU65	RO	0h	Reserved
2 - 0	TBDS	RW	0h	Tx Buffer Data Field Size

4.16.291 MCAN3_CFG_TXBRP Register (Offset = 2CCh) [reset = h]

Short Description: TXBRP

Long Description:

Return to Summary Table

Table 4-2042. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82CCh

Figure 4-980. MCAN3_CFG_TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
RO															
0															

Access Types Legend

Table 4-2043. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TRP	RO	0h	Transmission Request Pending

4.16.292 MCAN3_CFG_TXBAR Register (Offset = 2D0h) [reset = h]

Short Description: TXBAR

Long Description:

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Table 4-2044. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82D0h

Figure 4-981. MCAN3_CFG_TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-2045. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AR	RW W0TOCLR	0h	Add request

4.16.293 MCAN3_CFG_TXBCR Register (Offset = 2D4h) [reset = h]

Short Description: TXBCR

Long Description:

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Table 4-2046. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82D4h

Figure 4-982. MCAN3_CFG_TXBCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-2047. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CR	RW W0TOCLR	0h	Cancellation Request

4.16.294 MCAN3_CFG_TXBTO Register (Offset = 2D8h) [reset = h]

Short Description: TXBTO

Long Description:

Return to Summary Table

Table 4-2048. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82D8h

Figure 4-983. MCAN3_CFG_TXBTO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO															
RO															
0															

Access Types Legend

Table 4-2049. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO	RO	0h	Transmission Occurred

4.16.295 MCAN3_CFG_TXBCF Register (Offset = 2DCh) [reset = h]

Short Description: TXBCF

Long Description:

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Table 4-2050. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82DCh

Figure 4-984. MCAN3_CFG_TXBCF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF															
RO															
0															

Access Types Legend

Table 4-2051. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CF	RO	0h	Cancellation Finished

4.16.296 MCAN3_CFG_TXBTIE Register (Offset = 2E0h) [reset = h]

Short Description: TXBTIE

Long Description:

Return to Summary Table

Table 4-2052. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82E0h

Figure 4-985. MCAN3_CFG_TXBTIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE															
RW															
0															

Access Types Legend

Table 4-2053. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIE	RW	0h	Transmission Interrupt Enable

4.16.297 MCAN3_CFG_TXBCIE Register (Offset = 2E4h) [reset = h]

Short Description: TXBCIE

Long Description:

Return to Summary Table

Table 4-2054. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82E4h

Figure 4-986. MCAN3_CFG_TXBCIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE															
RW															
0															

Access Types Legend

Table 4-2055. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CFIE	RW	0h	Cancellation Finished Interrupt Enable

4.16.298 MCAN3_CFG_RES14 Register (Offset = 2E8h) [reset = h]

Short Description: RES14

Long Description:

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Table 4-2056. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82E8h

Figure 4-987. MCAN3_CFG_RES14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES14															
RO															
0															

Access Types Legend

Table 4-2057. RES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES14	RO	0h	Reserved

4.16.299 MCAN3_CFG_RES15 Register (Offset = 2ECh) [reset = h]

Short Description: RES15

Long Description:

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Table 4-2058. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82ECh

Figure 4-988. MCAN3_CFG_RES15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15															
RO															
0															

Access Types Legend

Table 4-2059. RES15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES15	RO	0h	Reserved

4.16.300 MCAN3_CFG_TXEFC Register (Offset = 2F0h) [reset = h]

Short Description: TXEFC

Long Description:

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Table 4-2060. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82F0h

Figure 4-989. MCAN3_CFG_TXEFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68		EFWM						NU67		EFS					
RW		RW						RW		RW					
0		0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFSA														NU66	
RW														RW	
0														0	

Access Types Legend

Table 4-2061. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU68	RW	0h	Reserved
29 - 24	EFWM	RW	0h	Event FIFO Watermark
23 - 22	NU67	RW	0h	Reserved
21 - 16	EFS	RW	0h	Event FIFO Size
15 - 2	EFSA	RW	0h	Event FIFO Start Address
1 - 0	NU66	RW	0h	Reserved

4.16.301 MCAN3_CFG_TXEFS Register (Offset = 2F4h) [reset = h]

Short Description: TXEFS

Long Description:

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Table 4-2062. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82F4h

Figure 4-990. MCAN3_CFG_TXEFS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU72						TEFL	EFF	NU71			EFPI				
RO						RO	RO	RO			RO				
0						0	0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU70			EFGI					NU69		EFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-2063. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU72	RO	0h	Reserved
25	TEFL	RO	0h	Tx Event FIFO Element Lost
24	EFF	RO	0h	Event FIFO Full
23 - 21	NU71	RO	0h	Reserved
20 - 16	EFPI	RO	0h	Event FIFO Put Index
15 - 13	NU70	RO	0h	Reserved
12 - 8	EFGI	RO	0h	Event FIFO Get Index
7 - 6	NU69	RO	0h	Reserved
5 - 0	EFFL	RO	0h	Event FIFO FIll Level

4.16.302 MCAN3_CFG_TXEFA Register (Offset = 2F8h) [reset = h]

Short Description: TXEFA

Long Description:

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Table 4-2064. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82F8h

Figure 4-991. MCAN3_CFG_TXEFA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU73											EFAI				
RO											RO				
0											0				

Access Types Legend

Table 4-2065. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU73	RO	0h	Reserved
4 - 0	EFAI	RO	0h	Event FIFO Acknowledge Index

4.16.303 MCAN3_CFG_RES16 Register (Offset = 2FCh) [reset = h]

Short Description: RES16

Long Description:

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Table 4-2066. Instance Table

Instance Name	Physical Address
MCAN3_CFG	5263 82FCh

Figure 4-992. MCAN3_CFG_RES16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES16															
RO															
0															

Access Types Legend

Table 4-2067. RES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES16	RO	0h	Reserved

Table 4-2068. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined
RW W0TOCLR	RW W0TOCLR	Undefined

4.17 MSS_MCAN_ECC Registers

Table 4-2069. MCAN0_ECC, MCAN0_ECC_MCAN0_ECC Registers, Base Address=5270 0000H, Length=5

Offset	Length	Acronym	Register Name	MCAN0_ECC Physical Address
0h	32	MCAN0_ECC_REV	Aggregator Revision Register	5270 0000h
8h	32	MCAN0_ECC_VECTOR	ECC Vector Register	5270 0008h
Ch	32	MCAN0_ECC_STAT	Misc Status	5270 000Ch
14h	32	MCAN0_ECC_CTRL	CTRL	5270 0014h
18h	32	MCAN0_ECC_ERR_CTRL1	ERR_CTRL1	5270 0018h
1Ch	32	MCAN0_ECC_ERR_CTRL2	ERR_CTRL2	5270 001Ch
20h	32	MCAN0_ECC_ERR_STAT1	ERR_STAT1	5270 0020h
24h	32	MCAN0_ECC_ERR_STAT2	ERR_STAT2	5270 0024h
28h	32	MCAN0_ECC_ERR_STAT3	ERR_STAT3	5270 0028h
3Ch	32	MCAN0_ECC_SEC_EOI_REG	EOI Register	5270 003Ch
40h	32	MCAN0_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	5270 0040h
80h	32	MCAN0_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 0080h
C0h	32	MCAN0_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 00C0h
13Ch	32	MCAN0_ECC_DED_EOI_REG	EOI Register	5270 013Ch
140h	32	MCAN0_ECC_DED_STATUS_REG0	Interrupt Status Register 0	5270 0140h
180h	32	MCAN0_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 0180h
1C0h	32	MCAN0_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 01C0h
200h	32	MCAN0_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5270 0200h
204h	32	MCAN0_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5270 0204h
208h	32	MCAN0_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	5270 0208h
20Ch	32	MCAN0_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5270 020Ch

Table 4-2070. MCAN1_ECC, MCAN1_ECC_MCAN1_ECC Registers, Base Address=5270 1000H, Length=5

Offset	Length	Acronym	Register Name	MCAN1_ECC Physical Address
0h	32	MCAN1_ECC_REV	Aggregator Revision Register	5270 1000h
8h	32	MCAN1_ECC_VECTOR	ECC Vector Register	5270 1008h
Ch	32	MCAN1_ECC_STAT	Misc Status	5270 100Ch
14h	32	MCAN1_ECC_CTRL	CTRL	5270 1014h
18h	32	MCAN1_ECC_ERR_CTRL1	ERR_CTRL1	5270 1018h
1Ch	32	MCAN1_ECC_ERR_CTRL2	ERR_CTRL2	5270 101Ch
20h	32	MCAN1_ECC_ERR_STAT1	ERR_STAT1	5270 1020h
24h	32	MCAN1_ECC_ERR_STAT2	ERR_STAT2	5270 1024h
28h	32	MCAN1_ECC_ERR_STAT3	ERR_STAT3	5270 1028h
3Ch	32	MCAN1_ECC_SEC_EOI_REG	EOI Register	5270 103Ch
40h	32	MCAN1_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	5270 1040h

Table 4-2070. MCAN1_ECC, MCAN1_ECC_MCAN1_ECC Registers, Base Address=5270 1000H, Length=5 (continued)

Offset	Length	Acronym	Register Name	MCAN1_ECC Physical Address
80h	32	MCAN1_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 1080h
C0h	32	MCAN1_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 10C0h
13Ch	32	MCAN1_ECC_DED_EOI_REG	EOI Register	5270 113Ch
140h	32	MCAN1_ECC_DED_STATUS_REG0	Interrupt Status Register 0	5270 1140h
180h	32	MCAN1_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 1180h
1C0h	32	MCAN1_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 11C0h
200h	32	MCAN1_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5270 1200h
204h	32	MCAN1_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5270 1204h
208h	32	MCAN1_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	5270 1208h
20Ch	32	MCAN1_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5270 120Ch

Table 4-2071. MCAN2_ECC, MCAN2_ECC_MCAN2_ECC Registers, Base Address=5270 2000H, Length=5

Offset	Length	Acronym	Register Name	MCAN2_ECC Physical Address
0h	32	MCAN2_ECC_REV	Aggregator Revision Register	5270 2000h
8h	32	MCAN2_ECC_VECTOR	ECC Vector Register	5270 2008h
Ch	32	MCAN2_ECC_STAT	Misc Status	5270 200Ch
14h	32	MCAN2_ECC_CTRL	CTRL	5270 2014h
18h	32	MCAN2_ECC_ERR_CTRL1	ERR_CTRL1	5270 2018h
1Ch	32	MCAN2_ECC_ERR_CTRL2	ERR_CTRL2	5270 201Ch
20h	32	MCAN2_ECC_ERR_STAT1	ERR_STAT1	5270 2020h
24h	32	MCAN2_ECC_ERR_STAT2	ERR_STAT2	5270 2024h
28h	32	MCAN2_ECC_ERR_STAT3	ERR_STAT3	5270 2028h
3Ch	32	MCAN2_ECC_SEC_EOI_REG	EOI Register	5270 203Ch
40h	32	MCAN2_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	5270 2040h
80h	32	MCAN2_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 2080h
C0h	32	MCAN2_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 20C0h
13Ch	32	MCAN2_ECC_DED_EOI_REG	EOI Register	5270 213Ch
140h	32	MCAN2_ECC_DED_STATUS_REG0	Interrupt Status Register 0	5270 2140h
180h	32	MCAN2_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 2180h
1C0h	32	MCAN2_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 21C0h
200h	32	MCAN2_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5270 2200h
204h	32	MCAN2_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5270 2204h
208h	32	MCAN2_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	5270 2208h
20Ch	32	MCAN2_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5270 220Ch

Table 4-2072. MCAN3_ECC, MCAN3_ECC_MCAN3_ECC Registers, Base Address=5270 3000H, Length=5

Offset	Length	Acronym	Register Name	MCAN3_ECC Physical Address
0h	32	MCAN3_ECC_REV	Aggregator Revision Register	5270 3000h
8h	32	MCAN3_ECC_VECTOR	ECC Vector Register	5270 3008h
Ch	32	MCAN3_ECC_STAT	Misc Status	5270 300Ch

Table 4-2072. MCAN3_ECC, MCAN3_ECC_MCAN3_ECC Registers, Base Address=5270 3000H, Length=5 (continued)

Offset	Length	Acronym	Register Name	MCAN3_ECC Physical Address
14h	32	MCAN3_ECC_CTRL	CTRL	5270 3014h
18h	32	MCAN3_ECC_ERR_CTRL1	ERR_CTRL1	5270 3018h
1Ch	32	MCAN3_ECC_ERR_CTRL2	ERR_CTRL2	5270 301Ch
20h	32	MCAN3_ECC_ERR_STAT1	ERR_STAT1	5270 3020h
24h	32	MCAN3_ECC_ERR_STAT2	ERR_STAT2	5270 3024h
28h	32	MCAN3_ECC_ERR_STAT3	ERR_STAT3	5270 3028h
3Ch	32	MCAN3_ECC_SEC_EOI_REG	EOI Register	5270 303Ch
40h	32	MCAN3_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	5270 3040h
80h	32	MCAN3_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 3080h
C0h	32	MCAN3_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 30C0h
13Ch	32	MCAN3_ECC_DED_EOI_REG	EOI Register	5270 313Ch
140h	32	MCAN3_ECC_DED_STATUS_REG0	Interrupt Status Register 0	5270 3140h
180h	32	MCAN3_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	5270 3180h
1C0h	32	MCAN3_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	5270 31C0h
200h	32	MCAN3_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	5270 3200h
204h	32	MCAN3_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	5270 3204h
208h	32	MCAN3_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	5270 3208h
20Ch	32	MCAN3_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	5270 320Ch

4.17.1 MCAN0_ECC_REV Register (Offset = 0h) [reset = h]

Short Description: Aggregator Revision Register

Long Description:

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Table 4-2073. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0000h

Figure 4-993. MCAN0_ECC_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
RO				RO				RO		RO					
11101				10				0		0					

Access Types Legend

Table 4-2074. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.17.2 MCAN0_ECC_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-2075. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0008h

Figure 4-994. MCAN0_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
RO							RW	RW							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
RW	RO				RW										
0	0				0										

Access Types Legend

Table 4-2076. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NU1	RO	0h	Reserved
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23 - 16	RD_SVBUS_ADDR	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14 - 11	NU0	RO	0h	Reserved
10 - 0	ECC_VEC	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.17.3 MCAN0_ECC_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

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Table 4-2077. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 000Ch

Figure 4-995. MCAN0_ECC_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
RO					RO										
0					10										

Access Types Legend

Table 4-2078. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU2	RO	0h	Reserved
10 - 0	NUM_RAMS	RO	Ah	Indicates the number of RAMS serviced by the ECC aggregator

4.17.4 MCAN0_ECC_CTRL Register (Offset = 14h) [reset = h]

Short Description: CTRL

Long Description:

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Table 4-2079. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0014h

Figure 4-996. MCAN0_ECC_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
RO							WO	WO	WO	WO	WO	WO	WO	WO	WO
0							1	1	0	0	0	0	1	1	1

Access Types Legend

Table 4-2080. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	NU3	RO	0h	TI Internal : Reserved
8	CHECK_TIMEOUT	WO	1h	TI Internal : Check timeout
7	CHECK_PARITY	WO	1h	TI Internal : Check Parity
6	ERROR_ONCE	WO	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	WO	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	WO	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	WO	0h	TI Internal : Force Single Bit Error
2	EN_RMW	WO	1h	TI Internal : Enable rmw
1	ECC_CHK	WO	1h	TI Internal : Enable ECC check
0	ECC_EN	WO	1h	TI Internal : Enable ECC

4.17.5 MCAN0_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ERR_CTRL1

Long Description:

Return to Summary Table

Table 4-2081. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0018h

Figure 4-997. MCAN0_ECC_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-2082. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.17.6 MCAN0_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ERR_CTRL2

Long Description:

Return to Summary Table

Table 4-2083. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 001Ch

Figure 4-998. MCAN0_ECC_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-2084. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

4.17.7 MCAN0_ECC_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ERR_STAT1

Long Description:

Return to Summary Table

Table 4-2085. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0020h

Figure 4-999. MCAN0_ECC_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
WO	WO		WO	WO		WO		WO	WO		WO	WO		WO	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-2086. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1_STS	RO	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	WO	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14 - 13	CLR_ECC_PAR	WO	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	WO	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11 - 10	CLR_ECC_DED	WO	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9 - 8	CLR_ECC_SEC	WO	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	WO	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.
6 - 5	ECC_PAR	WO	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	WO	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3 - 2	ECC_DED	WO	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1 - 0	ECC_SEC	WO	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

4.17.8 MCAN0_ECC_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ERR_STAT2

Long Description:

Return to Summary Table

Table 4-2087. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0024h

Figure 4-1000. MCAN0_ECC_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-2088. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	TI Internal : Row address where the single or double-bit error has occurred

4.17.9 MCAN0_ECC_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ERR_STAT3

Long Description:

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Table 4-2089. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0028h

Figure 4-1001. MCAN0_ECC_ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND	NU5							TIMEOUT_PEND	NU4
RO						WO	RO							WO	RO
0						0	0							0	0

Access Types Legend

Table 4-2090. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU6	RO	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	WO	0h	TI Internal : Clear timeout pending
8 - 2	NU5	RO	0h	TI Internal : Reserved
1	TIMEOUT_PEND	WO	0h	TI Internal : Timeout pending
0	NU4	RO	0h	TI Internal : Reserved

4.17.10 MCAN0_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2091. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 003Ch

Figure 4-1002. MCAN0_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2092. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU7	RO	0h	Reserved
0	SEC_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.11 MCAN0_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2093. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0040h

Figure 4-1003. MCAN0_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2094. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU8	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.12 MCAN0_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2095. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0080h

Figure 4-1004. MCAN0_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2096. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU9	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.13 MCAN0_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2097. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 00C0h

Figure 4-1005. MCAN0_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2098. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU10	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.14 MCAN0_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2099. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 013Ch

Figure 4-1006. MCAN0_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2100. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU11	RO	0h	Reserved
0	DED_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.15 MCAN0_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2101. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0140h

Figure 4-1007. MCAN0_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2102. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.16 MCAN0_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2103. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0180h

Figure 4-1008. MCAN0_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2104. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU13	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.17 MCAN0_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2105. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 01C0h

Figure 4-1009. MCAN0_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2106. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU14	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.18 MCAN0_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-2107. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0200h

Figure 4-1010. MCAN0_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2108. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU15	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	RW	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.19 MCAN0_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-2109. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0204h

Figure 4-1011. MCAN0_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2110. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU16	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	RW	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.20 MCAN0_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-2111. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0208h

Figure 4-1012. MCAN0_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2112. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU17	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.

4.17.21 MCAN0_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-2113. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 020Ch

Figure 4-1013. MCAN0_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2114. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU18	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.

4.17.22 MCAN1_ECC_REV Register (Offset = 0h) [reset = h]

Short Description: Aggregator Revision Register

Long Description:

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Table 4-2115. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1000h

Figure 4-1014. MCAN1_ECC_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11101					10			0		0					

Access Types Legend

Table 4-2116. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.17.23 MCAN1_ECC_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-2117. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1008h

Figure 4-1015. MCAN1_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
RO							RW	RW							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
RW	RO				RW										
0	0				0										

Access Types Legend

Table 4-2118. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NU1	RO	0h	Reserved
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23 - 16	RD_SVBUS_ADDR	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14 - 11	NU0	RO	0h	Reserved
10 - 0	ECC_VEC	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.17.24 MCAN1_ECC_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-2119. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 100Ch

Figure 4-1016. MCAN1_ECC_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
RO					RO										
0					10										

Access Types Legend

Table 4-2120. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU2	RO	0h	Reserved
10 - 0	NUM_RAMS	RO	Ah	Indicates the number of RAMS serviced by the ECC aggregator

4.17.25 MCAN1_ECC_CTRL Register (Offset = 14h) [reset = h]

Short Description: CTRL

Long Description:

Return to Summary Table

Table 4-2121. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1014h

Figure 4-1017. MCAN1_ECC_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
RO							WO	WO	WO	WO	WO	WO	WO	WO	WO
0							1	1	0	0	0	0	1	1	1

Access Types Legend

Table 4-2122. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	NU3	RO	0h	TI Internal : Reserved
8	CHECK_TIMEOUT	WO	1h	TI Internal : Check timeout
7	CHECK_PARITY	WO	1h	TI Internal : Check Parity
6	ERROR_ONCE	WO	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	WO	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	WO	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	WO	0h	TI Internal : Force Single Bit Error
2	EN_RMW	WO	1h	TI Internal : Enable rmw
1	ECC_CHK	WO	1h	TI Internal : Enable ECC check
0	ECC_EN	WO	1h	TI Internal : Enable ECC

4.17.26 MCAN1_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ERR_CTRL1

Long Description:

Return to Summary Table

Table 4-2123. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1018h

Figure 4-1018. MCAN1_ECC_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-2124. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.17.27 MCAN1_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ERR_CTRL2

Long Description:

Return to Summary Table

Table 4-2125. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 101Ch

Figure 4-1019. MCAN1_ECC_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-2126. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

4.17.28 MCAN1_ECC_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ERR_STAT1

Long Description:

Return to Summary Table

Table 4-2127. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1020h

Figure 4-1020. MCAN1_ECC_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
WO	WO		WO	WO		WO		WO	WO		WO	WO		WO	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-2128. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1_STS	RO	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	WO	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14 - 13	CLR_ECC_PAR	WO	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	WO	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11 - 10	CLR_ECC_DED	WO	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9 - 8	CLR_ECC_SEC	WO	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	WO	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.
6 - 5	ECC_PAR	WO	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	WO	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3 - 2	ECC_DED	WO	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1 - 0	ECC_SEC	WO	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

4.17.29 MCAN1_ECC_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ERR_STAT2

Long Description:

Return to Summary Table

Table 4-2129. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1024h

Figure 4-1021. MCAN1_ECC_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-2130. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	TI Internal : Row address where the single or double-bit error has occurred

4.17.30 MCAN1_ECC_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ERR_STAT3

Long Description:

Return to Summary Table

Table 4-2131. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1028h

Figure 4-1022. MCAN1_ECC_ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND	NU5							TIMEOUT_PEND	NU4
RO						WO	RO							WO	RO
0						0	0							0	0

Access Types Legend

Table 4-2132. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU6	RO	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	WO	0h	TI Internal : Clear timeout pending
8 - 2	NU5	RO	0h	TI Internal : Reserved
1	TIMEOUT_PEND	WO	0h	TI Internal : Timeout pending
0	NU4	RO	0h	TI Internal : Reserved

4.17.31 MCAN1_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2133. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 103Ch

Figure 4-1023. MCAN1_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2134. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU7	RO	0h	Reserved
0	SEC_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.32 MCAN1_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2135. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1040h

Figure 4-1024. MCAN1_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2136. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU8	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.33 MCAN1_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2137. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1080h

Figure 4-1025. MCAN1_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2138. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU9	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.34 MCAN1_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2139. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 10C0h

Figure 4-1026. MCAN1_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2140. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU10	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.35 MCAN1_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2141. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 113Ch

Figure 4-1027. MCAN1_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2142. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU11	RO	0h	Reserved
0	DED_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.36 MCAN1_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2143. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1140h

Figure 4-1028. MCAN1_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2144. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.37 MCAN1_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2145. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1180h

Figure 4-1029. MCAN1_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2146. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU13	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.38 MCAN1_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2147. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 11C0h

Figure 4-1030. MCAN1_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2148. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU14	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.39 MCAN1_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-2149. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1200h

Figure 4-1031. MCAN1_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2150. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU15	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	RW	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.40 MCAN1_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-2151. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1204h

Figure 4-1032. MCAN1_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2152. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU16	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	RW	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.41 MCAN1_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-2153. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 1208h

Figure 4-1033. MCAN1_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2154. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU17	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.

4.17.42 MCAN1_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-2155. Instance Table

Instance Name	Physical Address
MCAN1_ECC	5270 120Ch

Figure 4-1034. MCAN1_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2156. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU18	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.

4.17.43 MCAN2_ECC_REV Register (Offset = 0h) [reset = h]

Short Description: Aggregator Revision Register

Long Description:

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Table 4-2157. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2000h

Figure 4-1035. MCAN2_ECC_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11101					10			0		0					

Access Types Legend

Table 4-2158. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.17.44 MCAN2_ECC_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-2159. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2008h

Figure 4-1036. MCAN2_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
RO							RW	RW							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
RW	RO				RW										
0	0				0										

Access Types Legend

Table 4-2160. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NU1	RO	0h	Reserved
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23 - 16	RD_SVBUS_ADDR	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14 - 11	NU0	RO	0h	Reserved
10 - 0	ECC_VEC	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.17.45 MCAN2_ECC_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-2161. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 200Ch

Figure 4-1037. MCAN2_ECC_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
RO					RO										
0					10										

Access Types Legend

Table 4-2162. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU2	RO	0h	Reserved
10 - 0	NUM_RAMS	RO	Ah	Indicates the number of RAMS serviced by the ECC aggregator

4.17.46 MCAN2_ECC_CTRL Register (Offset = 14h) [reset = h]

Short Description: CTRL

Long Description:

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Table 4-2163. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2014h

Figure 4-1038. MCAN2_ECC_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
RO							WO	WO	WO	WO	WO	WO	WO	WO	WO
0							1	1	0	0	0	0	1	1	1

Access Types Legend

Table 4-2164. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	NU3	RO	0h	TI Internal : Reserved
8	CHECK_TIMEOUT	WO	1h	TI Internal : Check timeout
7	CHECK_PARITY	WO	1h	TI Internal : Check Parity
6	ERROR_ONCE	WO	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	WO	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	WO	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	WO	0h	TI Internal : Force Single Bit Error
2	EN_RMW	WO	1h	TI Internal : Enable rmw
1	ECC_CHK	WO	1h	TI Internal : Enable ECC check
0	ECC_EN	WO	1h	TI Internal : Enable ECC

4.17.47 MCAN2_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ERR_CTRL1

Long Description:

Return to Summary Table

Table 4-2165. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2018h

Figure 4-1039. MCAN2_ECC_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-2166. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.17.48 MCAN2_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ERR_CTRL2

Long Description:

Return to Summary Table

Table 4-2167. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 201Ch

Figure 4-1040. MCAN2_ECC_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-2168. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

4.17.49 MCAN2_ECC_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ERR_STAT1

Long Description:

Return to Summary Table

Table 4-2169. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2020h

Figure 4-1041. MCAN2_ECC_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
WO	WO		WO	WO		WO		WO	WO		WO	WO		WO	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-2170. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1_STS	RO	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	WO	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14 - 13	CLR_ECC_PAR	WO	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	WO	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11 - 10	CLR_ECC_DED	WO	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9 - 8	CLR_ECC_SEC	WO	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	WO	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.
6 - 5	ECC_PAR	WO	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	WO	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3 - 2	ECC_DED	WO	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1 - 0	ECC_SEC	WO	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

4.17.50 MCAN2_ECC_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ERR_STAT2

Long Description:

Return to Summary Table

Table 4-2171. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2024h

Figure 4-1042. MCAN2_ECC_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-2172. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	TI Internal : Row address where the single or double-bit error has occurred

4.17.51 MCAN2_ECC_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ERR_STAT3

Long Description:

Return to Summary Table

Table 4-2173. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2028h

Figure 4-1043. MCAN2_ECC_ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND	NU5							TIMEOUT_PEND	NU4
RO						WO	RO							WO	RO
0						0	0							0	0

Access Types Legend

Table 4-2174. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU6	RO	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	WO	0h	TI Internal : Clear timeout pending
8 - 2	NU5	RO	0h	TI Internal : Reserved
1	TIMEOUT_PEND	WO	0h	TI Internal : Timeout pending
0	NU4	RO	0h	TI Internal : Reserved

4.17.52 MCAN2_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2175. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 203Ch

Figure 4-1044. MCAN2_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2176. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU7	RO	0h	Reserved
0	SEC_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.53 MCAN2_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2177. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2040h

Figure 4-1045. MCAN2_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2178. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU8	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.54 MCAN2_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2179. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2080h

Figure 4-1046. MCAN2_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2180. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU9	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.55 MCAN2_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2181. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 20C0h

Figure 4-1047. MCAN2_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2182. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU10	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.56 MCAN2_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2183. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 213Ch

Figure 4-1048. MCAN2_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2184. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU11	RO	0h	Reserved
0	DED_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.57 MCAN2_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2185. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2140h

Figure 4-1049. MCAN2_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2186. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.58 MCAN2_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2187. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2180h

Figure 4-1050. MCAN2_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2188. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU13	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.59 MCAN2_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2189. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 21C0h

Figure 4-1051. MCAN2_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2190. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU14	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.60 MCAN2_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-2191. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2200h

Figure 4-1052. MCAN2_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2192. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU15	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	RW	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.61 MCAN2_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-2193. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2204h

Figure 4-1053. MCAN2_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2194. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU16	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	RW	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.62 MCAN2_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-2195. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 2208h

Figure 4-1054. MCAN2_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2196. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU17	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.

4.17.63 MCAN2_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-2197. Instance Table

Instance Name	Physical Address
MCAN2_ECC	5270 220Ch

Figure 4-1055. MCAN2_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2198. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU18	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.

4.17.64 MCAN3_ECC_REV Register (Offset = 0h) [reset = h]

Short Description: Aggregator Revision Register

Long Description:

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Table 4-2199. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3000h

Figure 4-1056. MCAN3_ECC_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11101					10			0		0					

Access Types Legend

Table 4-2200. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

4.17.65 MCAN3_ECC_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

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Table 4-2201. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3008h

Figure 4-1057. MCAN3_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
RO							RW	RW							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
RW	RO				RW										
0	0				0										

Access Types Legend

Table 4-2202. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NU1	RO	0h	Reserved
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23 - 16	RD_SVBUS_ADDR	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14 - 11	NU0	RO	0h	Reserved
10 - 0	ECC_VEC	RW	0h	Value written to select the corresponding ECC RAM for control or status

4.17.66 MCAN3_ECC_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-2203. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 300Ch

Figure 4-1058. MCAN3_ECC_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
RO					RO										
0					10										

Access Types Legend

Table 4-2204. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU2	RO	0h	Reserved
10 - 0	NUM_RAMS	RO	Ah	Indicates the number of RAMS serviced by the ECC aggregator

4.17.67 MCAN3_ECC_CTRL Register (Offset = 14h) [reset = h]

Short Description: CTRL

Long Description:

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Table 4-2205. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3014h

Figure 4-1059. MCAN3_ECC_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
RO							WO	WO	WO	WO	WO	WO	WO	WO	WO
0							1	1	0	0	0	0	1	1	1

Access Types Legend

Table 4-2206. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	NU3	RO	0h	TI Internal : Reserved
8	CHECK_TIMEOUT	WO	1h	TI Internal : Check timeout
7	CHECK_PARITY	WO	1h	TI Internal : Check Parity
6	ERROR_ONCE	WO	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	WO	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	WO	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	WO	0h	TI Internal : Force Single Bit Error
2	EN_RMW	WO	1h	TI Internal : Enable rmw
1	ECC_CHK	WO	1h	TI Internal : Enable ECC check
0	ECC_EN	WO	1h	TI Internal : Enable ECC

4.17.68 MCAN3_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ERR_CTRL1

Long Description:

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Table 4-2207. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3018h

Figure 4-1060. MCAN3_ECC_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-2208. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

4.17.69 MCAN3_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ERR_CTRL2

Long Description:

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Table 4-2209. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 301Ch

Figure 4-1061. MCAN3_ECC_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-2210. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

4.17.70 MCAN3_ECC_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ERR_STAT1

Long Description:

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Table 4-2211. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3020h

Figure 4-1062. MCAN3_ECC_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
WO	WO		WO	WO		WO		WO	WO		WO	WO		WO	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-2212. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1_STS	RO	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	WO	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14 - 13	CLR_ECC_PAR	WO	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	WO	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11 - 10	CLR_ECC_DED	WO	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9 - 8	CLR_ECC_SEC	WO	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	WO	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.
6 - 5	ECC_PAR	WO	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	WO	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3 - 2	ECC_DED	WO	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1 - 0	ECC_SEC	WO	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

4.17.71 MCAN3_ECC_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ERR_STAT2

Long Description:

Return to Summary Table

Table 4-2213. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3024h

Figure 4-1063. MCAN3_ECC_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-2214. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	TI Internal : Row address where the single or double-bit error has occurred

4.17.72 MCAN3_ECC_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ERR_STAT3

Long Description:

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Table 4-2215. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3028h

Figure 4-1064. MCAN3_ECC_ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND	NU5							TIMEOUT_PEND	NU4
RO						WO	RO							WO	RO
0						0	0							0	0

Access Types Legend

Table 4-2216. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU6	RO	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	WO	0h	TI Internal : Clear timeout pending
8 - 2	NU5	RO	0h	TI Internal : Reserved
1	TIMEOUT_PEND	WO	0h	TI Internal : Timeout pending
0	NU4	RO	0h	TI Internal : Reserved

4.17.73 MCAN3_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-2217. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 303Ch

Figure 4-1065. MCAN3_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2218. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU7	RO	0h	Reserved
0	SEC_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.74 MCAN3_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

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Table 4-2219. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3040h

Figure 4-1066. MCAN3_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2220. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU8	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.75 MCAN3_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2221. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3080h

Figure 4-1067. MCAN3_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2222. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU9	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.76 MCAN3_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2223. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 30C0h

Figure 4-1068. MCAN3_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2224. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU10	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.77 MCAN3_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2225. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 313Ch

Figure 4-1069. MCAN3_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2226. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU11	RO	0h	Reserved
0	DED_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

4.17.78 MCAN3_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2227. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3140h

Figure 4-1070. MCAN3_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2228. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

4.17.79 MCAN3_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2229. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3180h

Figure 4-1071. MCAN3_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2230. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU13	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.80 MCAN3_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

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Table 4-2231. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 31C0h

Figure 4-1072. MCAN3_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2232. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU14	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.81 MCAN3_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

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Table 4-2233. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3200h

Figure 4-1073. MCAN3_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2234. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU15	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	RW	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

4.17.82 MCAN3_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

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Table 4-2235. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3204h

Figure 4-1074. MCAN3_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2236. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU16	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	RW	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

4.17.83 MCAN3_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

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Table 4-2237. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 3208h

Figure 4-1075. MCAN3_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2238. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU17	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.

4.17.84 MCAN3_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

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Table 4-2239. Instance Table

Instance Name	Physical Address
MCAN3_ECC	5270 320Ch

Figure 4-1076. MCAN3_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2240. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU18	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.

Table 4-2241. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

4.18 MSS_MCAN_MSG_RAM Registers

Table 4-2242. MCAN0_MSG_RAM, MCAN0_MSG_RAM_MCAN0_MSG_RAM Registers, Base Address=5260 0000H, Length=3

Offset	Length	Acronym	Register Name	MCAN0_MSG_RAM Physical Address
0h	32	MCAN0_MSG_RAM_START	START	5260 0000h

4.18.1 MCAN0_MSG_RAM_START Register (Offset = 0h) [reset = h]

Short Description: START

Long Description:

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Table 4-2243. Instance Table

Instance Name	Physical Address
MCAN0_MSG_RAM	5260 0000h

Figure 4-1077. MCAN0_MSG_RAM_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2244. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	MCAN message mem Start address

Table 4-2245. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.19 MSS_MCRC Registers

Table 4-2246. MCRC0, MCRC0_MCRC Registers, Base Address=3500 0000H, Length=3

Offset	Length	Acronym	Register Name	MCRC0 Physical Address
0h	32	MCRC0_CRC_CTRL0	Contains sw reset control bit to reset PSA	3500 0000h
8h	32	MCRC0_CRC_CTRL1	Contains power down control bit	3500 0008h
10h	32	MCRC0_CRC_CTRL2	Contains channel mode, data trace enable control bits	3500 0010h
18h	32	MCRC0_CRC_INTS	Write one to a bit to enable a interrupt	3500 0018h
20h	32	MCRC0_CRC_INTR	Write one to a bit to disable a interrupt	3500 0020h
28h	32	MCRC0_CRC_STATUS_REG	Contains interrupt flags for different types of interrupt	3500 0028h
30h	32	MCRC0_CRC_INT_OFFSET_REG	Contains the interrupt offset vector address	3500 0030h
38h	32	MCRC0_CRC_BUSY	Contains the busy flag for each channel	3500 0038h
40h	32	MCRC0_CRC_PCOUNT_REG1	Channel 1 preload register for the pattern count	3500 0040h
44h	32	MCRC0_CRC_SCOUNT_REG1	Channel 1 preload register for the sector count	3500 0044h
48h	32	MCRC0_CRC_CURSEC_REG1	Channel 1 current sector register contains the sector number which causes CRC failure	3500 0048h
4Ch	32	MCRC0_CRC_WDTOPLD1	Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer	3500 004Ch
50h	32	MCRC0_CRC_BCTOPLD1	Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time	3500 0050h
60h	32	MCRC0_PSA_SIGREGL1	Channel 1 PSA signature low register	3500 0060h
64h	32	MCRC0_PSA_SIGREGH1	Channel 1 PSA signature high register	3500 0064h
68h	32	MCRC0_CRC_REGL1	Channel 1 CRC value low register	3500 0068h
6Ch	32	MCRC0_CRC_REGH1	Channel 1 CRC value high register	3500 006Ch
70h	32	MCRC0_PSA_SECSIGREGL1	Channel 1 PSA sector signature low regis-ter	3500 0070h
74h	32	MCRC0_PSA_SECSIGREGH1	Channel 1 PSA sector signature high regis-ter	3500 0074h
78h	32	MCRC0_RAW_DATAREGL1	Channel 1 un-compressed raw data low register	3500 0078h
7Ch	32	MCRC0_RAW_DATAREGH1	Channel 1 un-compressed raw data high register	3500 007Ch
80h	32	MCRC0_CRC_PCOUNT_REG2	Channel 2 preload register for the pattern count	3500 0080h
84h	32	MCRC0_CRC_SCOUNT_REG2	Channel 2 preload register for the sector count	3500 0084h

Table 4-2246. MCRC0, MCRC0_MCRC Registers, Base Address=3500 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	MCRC0 Physical Address
88h	32	MCRC0_CRC_CURSEC_REG2	Channel 2 current sector register contains the sector number which causes CRC fail-ure	3500 0088h
8Ch	32	MCRC0_CRC_WDTOPLD2	Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer	3500 008Ch
90h	32	MCRC0_CRC_BCTOPLD2	Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time	3500 0090h
A0h	32	MCRC0_PSA_SIGREGL2	Channel 2 PSA signature low register	3500 00A0h
A4h	32	MCRC0_PSA_SIGREGH2	Channel 2 PSA signature high register	3500 00A4h
A8h	32	MCRC0_CRC_REGL2	Channel 2 CRC value low register	3500 00A8h
ACh	32	MCRC0_CRC_REGH2	Channel 2 CRC value high register	3500 00ACh
B0h	32	MCRC0_PSA_SECSIGREGL2	Channel 2 PSA sector signature low regis-ter	3500 00B0h
B4h	32	MCRC0_PSA_SECSIGREGH2	Channel 2 PSA sector signature high regis-ter	3500 00B4h
B8h	32	MCRC0_RAW_DATAREGL2	Channel 2 un-compressed raw data low register	3500 00B8h
BCh	32	MCRC0_RAW_DATAREGH2	Channel 2 un-compressed raw data high Register	3500 00BCh
C0h	32	MCRC0_CRC_PCOUNT_REG3	Channel 3 preload register for the pattern count	3500 00C0h
C4h	32	MCRC0_CRC_SCOUNT_REG3	Channel 3 preload register for the sector count	3500 00C4h
C8h	32	MCRC0_CRC_CURSEC_REG3	Channel 3 current sector register contains the sector number which causes CRC fail-ure	3500 00C8h
CCh	32	MCRC0_CRC_WDTOPLD3	Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer	3500 00CCh
D0h	32	MCRC0_CRC_BCTOPLD3	Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time	3500 00D0h
E0h	32	MCRC0_PSA_SIGREGL3	Channel 3 PSA signature low register	3500 00E0h
E4h	32	MCRC0_PSA_SIGREGH3	Channel 3 PSA signature high register	3500 00E4h
E8h	32	MCRC0_CRC_REGL3	Channel 3 CRC value low register	3500 00E8h
ECh	32	MCRC0_CRC_REGH3	Channel 3 CRC value high register	3500 00ECh
F0h	32	MCRC0_PSA_SECSIGREGL3	Channel 3 PSA sector signature low regis-ter	3500 00F0h
F4h	32	MCRC0_PSA_SECSIGREGH3	Channel 3 PSA sector signature high regis-ter	3500 00F4h
F8h	32	MCRC0_RAW_DATAREGL3	Channel 3 un-compressed raw data low register	3500 00F8h
FCh	32	MCRC0_RAW_DATAREGH3	Channel 3 un-compressed raw data high Register	3500 00FCh
100h	32	MCRC0_CRC_PCOUNT_REG4	Channel 4 preload register for the pattern count	3500 0100h
104h	32	MCRC0_CRC_SCOUNT_REG4	Channel 4 preload register for the sector count	3500 0104h

Table 4-2246. MCRC0, MCRC0_MCRC Registers, Base Address=3500 0000H, Length=3 (continued)

Offset	Length	Acronym	Register Name	MCRC0 Physical Address
108h	32	MCRC0_CRC_CURSEC_REG4	Channel 4 current sector register contains the sector number which causes CRC fail-ure	3500 0108h
10Ch	32	MCRC0_CRC_WDTOPLD4	Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer	3500 010Ch
110h	32	MCRC0_CRC_BCTOPLD4	Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time	3500 0110h
120h	32	MCRC0_PSA_SIGREGL4	Channel 4 PSA signature low register	3500 0120h
124h	32	MCRC0_PSA_SIGREGH4	Channel 4 PSA signature high register	3500 0124h
128h	32	MCRC0_CRC_REGL4	Channel 4 CRC value low register	3500 0128h
12Ch	32	MCRC0_CRC_REGH4	Channel 4 CRC value high register	3500 012Ch
130h	32	MCRC0_PSA_SECSIGREGL4	Channel 4 PSA sector signature low regis-ter	3500 0130h
134h	32	MCRC0_PSA_SECSIGREGH4	Channel 4 PSA sector signature high regis-ter	3500 0134h
138h	32	MCRC0_RAW_DATAREGL4	Channel 4 un-compressed raw data low register	3500 0138h
13Ch	32	MCRC0_RAW_DATAREGH4	Channel 4 un-compressed raw data high Register	3500 013Ch
140h	32	MCRC0_MCRC_BUS_SEL	Disables either or all tracing of data buses	3500 0140h
144h	32	MCRC0_MCRC_RESERVED	0x144 to 0x1FF is reserved area.	3500 0144h

4.19.1 MCRC0_CRC_CTRL0 Register (Offset = 0h) [reset = h]

Short Description: Contains sw reset control bit to reset PSA

Long Description:

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Table 4-2247. Instance Table

Instance Name	Physical Address
MCRC0	3500 0000h

Figure 4-1078. MCRC0_CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12	NU11	NU10	NU9		NU8		NU7	NU6	NU5	NU4	NU3		NU2		NU1
RO	RO	RO	RO		RO		RO	RO	RO	RO	RO		RO		RO
0	0	0	0		0		0	0	0	0	0		0		0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH2_CRC_SEL2	CH2_BYTE_SWAP	CH2_BIT_SWAP	CH2_CRC_SEL		CH2_DW_SEL		CH2_PSA_SWREST	CH1_CRC_SEL2	CH1_BYTE_SWAP	CH1_BIT_SWAP	CH1_CRC_SEL		CH1_DW_SEL		CH1_PSA_SWREST
RW	RW	RW	RW		RW		RW	RW	RW	RW	RW		RW		RW
0	0	0	0		0		0	0	0	0	0		0		0

Access Types Legend

Table 4-2248. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU12	RO	0h	Reserved
30	NU11	RO	0h	Reserved
29	NU10	RO	0h	Reserved
28 - 27	NU9	RO	0h	Reserved
26 - 25	NU8	RO	0h	Reserved
24	NU7	RO	0h	Reserved
23	NU6	RO	0h	Reserved
22	NU5	RO	0h	Reserved
21	NU4	RO	0h	Reserved
20 - 19	NU3	RO	0h	Reserved
18 - 17	NU2	RO	0h	Reserved
16	NU1	RO	0h	Reserved
15	CH2_CRC_SEL2	RW	0h	Refer "CH2_DW_SEL" field description
14	CH2_BYTE_SWAP	RW	0h	BYTE SWAP Enable across Data Size0 ? Byte Swap Disabled1 ? Byte Swap enabled.
13	CH2_BIT_SWAP	RW	0h	msb/lsb SWAPPING 0 ? msb (most significant bit First)1 ? lsb (least significant bit First)
12 - 11	CH2_CRC_SEL	RW	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}000 ? CRC-64001 - CRC-16010 ? CRC-32100 - VDA CAN, SAE-J1850 CRC-8101 - H2F, Autosar 4.0110 - CASTAGNOLI, iSCSI111 / 011 - E2E Profile 4
10 - 9	CH2_DW_SEL	RW	0h	CRC Data Size select.000 ? 64 bit Data Size001 - 16 bit Data Size010 ? 32 Bit Data Size
8	CH2_PSA_SWREST	RW	0h	Channel 2 PSA Software Reset. When set, the PSA SignatureRegister is reset to all zero. Software reset does not reset softwarereset bit itself. Therefore, CPU is required to clear this bit by writinga ?0?.0 = PSA Signature Register not reset1 = PSA Signature Register reset

Table 4-2248. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CH1_CRC_SEL2	RW	0h	Refer "CH1_DW_SEL" field description
6	CH1_BYTE_SWAP	RW	0h	BYTE SWAP Enable across Data Size0 ? Byte Swap Disabled1 ? Byte Swap enabled.
5	CH1_BIT_SWAP	RW	0h	msb/lsb SWAPPING 0 ? msb (most significant bit First)1 ? lsb (least significant bit First)
4 - 3	CH1_CRC_SEL	RW	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}000 ? CRC-64001 - CRC-16010 ? CRC-32100 - VDA CAN, SAE-J1850 CRC-8101 - H2F, Autosar 4.0110 - CASTAGNOLI, iSCSI111 / 011 - E2E Profile 4
2 - 1	CH1_DW_SEL	RW	0h	CRC Data Size select.000 ? 64 bit Data Size001 - 16 bit Data Size010 ? 32 Bit Data Size
0	CH1_PSA_SWREST	RW	0h	Channel 1 PSA Software Reset. When set, the PSA SignatureRegister is reset to all zero. Software reset does not reset softwarereset bit itself. Therefore, CPU is required to clear this bit by writinga ?0?.0 = PSA Signature Register not reset1 = PSA Signature Register reset

4.19.2 MCRC0_CRC_CTRL1 Register (Offset = 8h) [reset = h]

Short Description: Contains power down control bit

Long Description:

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Table 4-2249. Instance Table

Instance Name	Physical Address
MCRC0	3500 0008h

Figure 4-1079. MCRC0_CRC_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1															PWDN
RO															RW
0															0

Access Types Legend

Table 4-2250. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED1	RO	0h	Not Defined
0	PWDN	RW	0h	Power Down. When set, MCRC moduleMCRC Module is put inpower down mode.0 = MCRC is not in power down mode1 = MCRC is in power down mode

4.19.3 MCRC0_CRC_CTRL2 Register (Offset = 10h) [reset = h]

Short Description: Contains channel mode, data trace enable control bits

Long Description:

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Table 4-2251. Instance Table

Instance Name	Physical Address
MCRC0	3500 0010h

Figure 4-1080. MCRC0_CRC_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5						NU14		RESERVED4						NU13	
RO						RO		RO						RO	
0						0		0						0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3						CH2_MODE		RESERVED2			CH1_TRACEEN	RESERVED1		CH1_MODE	
RO						RW		RO			RW	RO		RW	
0						0		0			0	0		0	

Access Types Legend

Table 4-2252. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RESERVED5	RO	0h	Not Defined
25 - 24	NU14	RO	0h	Reserved
23 - 18	RESERVED4	RO	0h	Not Defined
17 - 16	NU13	RO	0h	Reserved
15 - 10	RESERVED3	RO	0h	Not Defined
9 - 8	CH2_MODE	RW	0h	Channel 2 Mode:0 0 = Data Capture mode. In this mode, the PSA Signature Registerdoes not compress data when it is written. Any datawritten to PSA Signature Register is simply captured byPSA Signature Register without any compression. Thismode can be used to plant seed value into the PSA register0 1 = AUTO mode1 0 = reserved1 1 = Full-CPU mode
7 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TRACEEN	RW	0h	Channel 1 Data Trace Enable. When set, the channel is put intodata trace mode. The channel snoops on the CPU VBUSM,ITCM, DTCM buses for any read transaction. Any read data onthese buses is compressed by the PSA Signature Register. Whensuspend is on, the PSA Signature Register does not compress anyread data on these buses.0 = Data Trace disable1 = Data Trace enable
3 - 2	RESERVED1	RO	0h	Not Defined
1 - 0	CH1_MODE	RW	0h	Channel 1 Mode:0 0 = Data Capture mode. In this mode, the PSA Signature Registerdoes not compress data when it is written. Any datawritten to PSA Signature Register is simply captured byPSA Signature Register without any compression. Thismode can be used to plant seed value into the PSA register0 1 = AUTO mode1 0 = reserved1 1 = Full-CPU mode

4.19.4 MCRC0_CRC_INTS Register (Offset = 18h) [reset = h]

Short Description: Write one to a bit to enable a interrupt

Long Description:

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Table 4-2253. Instance Table

Instance Name	Physical Address
MCRC0	3500 0018h

Figure 4-1081. MCRC0_CRC_INTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU22	NU21	NU20	NU19	RESERVED4				NU18	NU17	NU16	NU15	RESERVED3
RO			RO	RO	RO	RO	RO				RO	RO	RO	RO	RO
0			0	0	0	0	0				0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUTENS	CH2_UNDERENS	CH2_OVERENS	CH2_CRCFAILENS	RESERVED2				CH1_TIMEOUTENS	CH1_UNDERENS	CH1_OVERENS	CH1_CRCFAILENS	RESERVED1
RO			RW	RW	RW	RW	RO				RW	RW	RW	RW	RO
0			0	0	0	0	0				0	0	0	0	0

Access Types Legend

Table 4-2254. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU22	RO	0h	Reserved
27	NU21	RO	0h	Reserved
26	NU20	RO	0h	Reserved
25	NU19	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU18	RO	0h	Reserved
19	NU17	RO	0h	Reserved
18	NU16	RO	0h	Reserved
17	NU15	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUTENS	RW	0h	Channel 2 Timeout Interrupt Enable Bit. Writing a one to thisbit enable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt enable
11	CH2_UNDERENS	RW	0h	Channel 2 Underrun Interrupt Enable Bit. Writing a one tothis bit enable the underrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt enable
10	CH2_OVERENS	RW	0h	Channel 2 Overrun Interrupt Enable Bit. Writing a one to thisbit enable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt enable

Table 4-2254. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CH2_CRCFAILENS	RW	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to thisbit enable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt enable
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUTENS	RW	0h	Channel 1 Timeout Interrupt Enable Bit. Writing a one to thisbit enable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt enable
3	CH1_UNDERENS	RW	0h	Channel 1 Underrun Interrupt Enable Bit. Writing a one tothis bit enable the underrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt enable
2	CH1_OVERENS	RW	0h	Channel 1 Overrun Interrupt Enable Bit. Writing a one to thisbit enable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt enable
1	CH1_CRCFAILENS	RW	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to thisbit enable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt enable
0	RESERVED1	RO	0h	Not Defined

4.19.5 MCRC0_CRC_INTR Register (Offset = 20h) [reset = h]

Short Description: Write one to a bit to disable a interrupt

Long Description:

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Table 4-2255. Instance Table

Instance Name	Physical Address
MCRC0	3500 0020h

Figure 4-1082. MCRC0_CRC_INTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU30	NU29	NU28	NU27	RESERVED4				NU26	NU25	NU24	NU23	RESERVED3
RO			RO	RO	RO	RO	RO				RO	RO	RO	RO	RO
0			0	0	0	0	0				0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUTENR	CH2_UNDERENR	CH2_OVERENR	CH2_CRCFAILENR	RESERVED2				CH1_TIMEOUTENR	CH1_UNDERENR	CH1_OVERENR	CH1_CRCFAILENR	RESERVED1
RO			RW	RW	RW	RW	RO				RW	RW	RW	RW	RO
0			0	0	0	0	0				0	0	0	0	0

Access Types Legend

Table 4-2256. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU30	RO	0h	Reserved
27	NU29	RO	0h	Reserved
26	NU28	RO	0h	Reserved
25	NU27	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU26	RO	0h	Reserved
19	NU25	RO	0h	Reserved
18	NU24	RO	0h	Reserved
17	NU23	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUTENR	RW	0h	Channel 2 Timeout Interrupt Disable Bit. Writing a one to thisbit disable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt disable
11	CH2_UNDERENR	RW	0h	Channel 2 Underrun Interrupt Disable Bit. Writing a one tothis bit disable the underrun interrupt. Writing a zero has noeffect. Reading from this bit gives the status (interrupt enable/dis-able).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt disable
10	CH2_OVERENR	RW	0h	Channel 2 Overrun Interrupt Disable Bit. Writing a one to thisbit disable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt disable

Table 4-2256. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CH2_CRCFAILENR	RW	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to thisbit disable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt disable
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUTENR	RW	0h	Channel 1 Timeout Interrupt Disable Bit. Writing a one to thisbit disable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt disable
3	CH1_UNDERENR	RW	0h	Channel 1 Underrun Interrupt Disable Bit. Writing a one tothis bit disable the underrun interrupt. Writing a zero has noeffect. Reading from this bit gives the status (interrupt enable/dis-able).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt disable
2	CH1_OVERENR	RW	0h	Channel 1 Overrun Interrupt Disable Bit. Writing a one to thisbit disable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt disable
1	CH1_CRCFAILENR	RW	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to thisbit disable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt disable
0	RESERVED1	RO	0h	Not Defined

4.19.6 MCRC0_CRC_STATUS_REG Register (Offset = 28h) [reset = h]

Short Description: Contains interrupt flags for different types of interrupt

Long Description:

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Table 4-2257. Instance Table

Instance Name	Physical Address
MCRC0	3500 0028h

Figure 4-1083. MCRC0_CRC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED5			NU38	NU37	NU36	NU35	RESERVED4				NU34	NU33	NU32	NU31	RESERVED3
RO			RO	RO	RO	RO	RO				RO	RO	RO	RO	RO
0			0	0	0	0	0				0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3			CH2_TIMEOUT	CH2_UNDER	CH2_OVER	CH2_CRCFAIL	RESERVED2				CH1_TIMEOUT	CH1_UNDER	CH1_OVER	CH1_CRCFAIL	RESERVED1
RO			RW	RW	RW	RW	RO				RW	RW	RW	RW	RO
0			0	0	0	0	0				0	0	0	0	0

Access Types Legend

Table 4-2258. CRC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU38	RO	0h	Reserved
27	NU37	RO	0h	Reserved
26	NU36	RO	0h	Reserved
25	NU35	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU34	RO	0h	Reserved
19	NU33	RO	0h	Reserved
18	NU32	RO	0h	Reserved
17	NU31	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUT	RW	0h	Channel 2 CRC Timeout Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode.0 = No timeout interrupt is active1 = Timeout interrupt is active
11	CH2_UNDER	RW	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode only0 = No underrun interrupt is active1 = Underrun interrupt is active
10	CH2_OVER	RW	0h	Channel 2 CRC Overrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode0 = No overrun interrupt is active1 = Overrun interrupt is active
9	CH2_CRCFAIL	RW	0h	Channel 2 CRC Compare Fail Status Flag. This bit is clearedby writing a ?1? to it only. Writing ?0? has no effect. This bit is setin AUTO mode only.0 = No CRC compare fail interrupt is active1 = CRC compare fail interrupt is active
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUT	RW	0h	Channel 1 CRC Timeout Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode.0 = No timeout interrupt is active1 = Timeout interrupt is active

Table 4-2258. CRC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1_UNDER	RW	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode only0 = No underrun interrupt is active1 = Underrun interrupt is active
2	CH1_OVER	RW	0h	Channel 1 CRC Overrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode0 = No overrun interrupt is active1 = Overrun interrupt is active
1	CH1_CRCFAIL	RW	0h	Channel 1 CRC Compare Fail Status Flag. This bit is clearedby writing a ?1? to it only. Writing ?0? has no effect. This bit is setin AUTO mode only.0 = No CRC compare fail interrupt is active1 = CRC compare fail interrupt is active
0	RESERVED1	RO	0h	Not Defined

4.19.7 MCRC0_CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = h]

Short Description: Contains the interrupt offset vector address

Long Description:

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Table 4-2259. Instance Table

Instance Name	Physical Address
MCRC0	3500 0030h

Figure 4-1084. MCRC0_CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								OFSTREG							
RO								RW							
0								0							

Access Types Legend

Table 4-2260. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7 - 0	OFSTREG	RW	0h	CRC Interrupt Offset. This register indicates the highest prioritypending interrupt vector address. Reading the offset register auto-matically clear the respective interrupt flag. Please referenceTable 1?3. for details.

4.19.8 MCRC0_CRC_BUSY Register (Offset = 38h) [reset = h]

Short Description: Contains the busy flag for each channel

Long Description:

Return to Summary Table

Table 4-2261. Instance Table

Instance Name	Physical Address
MCRC0	3500 0038h

Figure 4-1085. MCRC0_CRC_BUSY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4							NU40	RESERVED3							NU39
RO							RO	RO							RO
0							0	0							0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2							CH2_BUSY	RESERVED1							CH1_BUSY
RO							RO	RO							RO
0							0	0							0

Access Types Legend

Table 4-2262. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED4	RO	0h	Not Defined
24	NU40	RO	0h	Reserved
23 - 17	RESERVED3	RO	0h	Not Defined
16	NU39	RO	0h	Reserved
15 - 9	RESERVED2	RO	0h	Not Defined
8	CH2_BUSY	RO	0h	Ch2_BUSY. During AUTO mode, the busy flag is set when thefirst data pattern of the block is compressed and remains set untilthe the last data pattern of the block is compressed. The flag iscleared when the last data pattern of the block is compressed.
7 - 1	RESERVED1	RO	0h	Not Defined
0	CH1_BUSY	RO	0h	CH1_BUSY. During AUTO mode, the busy flag is set when thefirst data pattern of the block is compressed and remains set untilthe the last data pattern of the block is compressed. The flag iscleared when the last data pattern of the block is compressed.

4.19.9 MCRC0_CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = h]

Short Description: Channel 1 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2263. Instance Table

Instance Name	Physical Address
MCRC0	3500 0040h

Figure 4-1086. MCRC0_CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												CRC_PAT_COUNT1			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_PAT_COUNT1															
RW															
0															

Access Types Legend

Table 4-2264. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	CRC_PAT_COUNT1	RW	0h	Channel 1 Pattern Counter Preload Register. This register con-tains the number of data patterns in one sector to be compressedbefore a CRC is performed.

4.19.10 MCRC0_CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = h]

Short Description: Channel 1 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2265. Instance Table

Instance Name	Physical Address
MCRC0	3500 0044h

Figure 4-1087. MCRC0_CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_SEC_COUNT1															
RW															
0															

Access Types Legend

Table 4-2266. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_SEC_COUNT1	RW	0h	Channel 1 Sector Counter Preload Register. This register con-tains the number of sectors in one block of memory.

4.19.11 MCRC0_CRC_CURSEC_REG1 Register (Offset = 48h) [reset = h]

Short Description: Channel 1 current sector register contains the sector number which causes CRC failure

Long Description:

Return to Summary Table

Table 4-2267. Instance Table

Instance Name	Physical Address
MCRC0	3500 0048h

Figure 4-1088. MCRC0_CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_CURSEC1															
RW															
0															

Access Types Legend

Table 4-2268. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_CURSEC1	RW	0h	Channel 1 Current Sector ID Register. In AUTO mode, thisregister contains the current sector number of which the signatureverification fails. The sector counter is a free running up counter.When a sector fails, the erroneous sector number is logged intocurrent sector ID register and the CRC fail interrupt is generatedThe sector ID register is frozen until it is read and the CRC failstatus bit is cleared by CPU. While it is frozen, it does not captureanother erroneous sector number. When this condition happens,an overrun interrupt is generated instead. Once the register is readand the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

4.19.12 MCRC0_CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = h]

Short Description: Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2269. Instance Table

Instance Name	Physical Address
MCRC0	3500 004Ch

Figure 4-1089. MCRC0_CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_WDTOPLD1							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_WDTOPLD1															
RW															
0															

Access Types Legend

Table 4-2270. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_WDTOPLD1	RW	0h	Channel 1 Watchdog Timeout Counter Preload Register. Thisregister contains the number of clock cycles within which theDMA must transfer the next block of data patterns.

4.19.13 MCRC0_CRC_BCTOPLD1 Register (Offset = 50h) [reset = h]

Short Description: Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2271. Instance Table

Instance Name	Physical Address
MCRC0	3500 0050h

Figure 4-1090. MCRC0_CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_BCTOPLD1							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_BCTOPLD1															
RW															
0															

Access Types Legend

Table 4-2272. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_BCTOPLD1	RW	0h	Channel 1 Block Complete Timeout Counter Preload Regis-ter. This register contains the number of clock cycles withinwhich the CRC for an entire block needs to complete before atimeout interrupt is generated.

4.19.14 MCRC0_PSA_SIGREGL1 Register (Offset = 60h) [reset = h]

Short Description: Channel 1 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2273. Instance Table

Instance Name	Physical Address
MCRC0	3500 0060h

Figure 4-1091. MCRC0_PSA_SIGREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASIG1_31_0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASIG1_31_0															
RW															
0															

Access Types Legend

Table 4-2274. PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASIG1_31_0	RW	0h	Channel 1 PSA Signature Low Register. This register containsthe value stored at PSASIG1[31:0] register.

4.19.15 MCRC0_PSA_SIGREGH1 Register (Offset = 64h) [reset = h]

Short Description: Channel 1 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2275. Instance Table

Instance Name	Physical Address
MCRC0	3500 0064h

Figure 4-1092. MCRC0_PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSA_SIG1_63_32															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSA_SIG1_63_32															
RW															
0															

Access Types Legend

Table 4-2276. PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSA_SIG1_63_32	RW	0h	Channel 1 PSA Signature High Register. This register containsthe value stored at PSASIG1[63:32] register.

4.19.16 MCRC0_CRC_REGL1 Register (Offset = 68h) [reset = h]

Short Description: Channel 1 CRC value low register

Long Description:

Return to Summary Table

Table 4-2277. Instance Table

Instance Name	Physical Address
MCRC0	3500 0068h

Figure 4-1093. MCRC0_CRC_REGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC1_31_0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC1_31_0															
RW															
0															

Access Types Legend

Table 4-2278. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC1_31_0	RW	0h	Channel 1 CRC Value Low Register. This register contains thecurrent known good signature value stored at CRC1[31:0] register.

4.19.17 MCRC0_CRC_REGH1 Register (Offset = 6Ch) [reset = h]

Short Description: Channel 1 CRC value high register

Long Description:

Return to Summary Table

Table 4-2279. Instance Table

Instance Name	Physical Address
MCRC0	3500 006Ch

Figure 4-1094. MCRC0_CRC_REGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC1_63_32															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC1_63_32															
RW															
0															

Access Types Legend

Table 4-2280. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC1_63_32	RW	0h	Channel 1 CRC Value High Register. This register contains thecurrent known good signature value stored at CRC1[63:32] register.

4.19.18 MCRC0_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = h]

Short Description: Channel 1 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2281. Instance Table

Instance Name	Physical Address
MCRC0	3500 0070h

Figure 4-1095. MCRC0_PSA_SECSIGREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG1_31_0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG1_31_0															
RO															
0															

Access Types Legend

Table 4-2282. PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG1_31_0	RO	0h	Channel 1 PSA Sector Signature Low Register. This registercontains the value stored at PSASECSIG1[31:0] register.

4.19.19 MCRC0_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = h]

Short Description: Channel 1 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2283. Instance Table

Instance Name	Physical Address
MCRC0	3500 0074h

Figure 4-1096. MCRC0_PSA_SECSIGREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG1_63_32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG1_63_32															
RO															
0															

Access Types Legend

Table 4-2284. PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG1_63_32	RO	0h	Channel 1 PSA Sector Signature High Register. This registercontains the value stored at PSASECSIG1[63:32] register.

4.19.20 MCRC0_RAW_DATAREGL1 Register (Offset = 78h) [reset = h]

Short Description: Channel 1 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2285. Instance Table

Instance Name	Physical Address
MCRC0	3500 0078h

Figure 4-1097. MCRC0_RAW_DATAREGL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA1_31_0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA1_31_0															
RO															
0															

Access Types Legend

Table 4-2286. RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA1_31_0	RO	0h	Channel 1 Raw Data Low Register. This register contains bit31:0 of the un-compressed raw data.

4.19.21 MCRC0_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = h]

Short Description: Channel 1 un-compressed raw data high register

Long Description:

Return to Summary Table

Table 4-2287. Instance Table

Instance Name	Physical Address
MCRC0	3500 007Ch

Figure 4-1098. MCRC0_RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA1_63_32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA1_63_32															
RO															
0															

Access Types Legend

Table 4-2288. RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA1_63_32	RO	0h	Channel 1 Raw Data High Register. This register contains bit63:32 of the un-compressed raw data.

4.19.22 MCRC0_CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = h]

Short Description: Channel 2 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2289. Instance Table

Instance Name	Physical Address
MCRC0	3500 0080h

Figure 4-1099. MCRC0_CRC_PCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												CRC_PAT_COUNT2			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_PAT_COUNT2															
RW															
0															

Access Types Legend

Table 4-2290. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	CRC_PAT_COUNT2	RW	0h	Channel 2 Pattern Counter Preload Register. This register con-tains the number of data patterns in one sector to be compressedbefore a CRC is performed.

4.19.23 MCRC0_CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = h]

Short Description: Channel 2 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2291. Instance Table

Instance Name	Physical Address
MCRC0	3500 0084h

Figure 4-1100. MCRC0_CRC_SCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_SEC_COUNT2															
RW															
0															

Access Types Legend

Table 4-2292. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_SEC_COUNT2	RW	0h	Channel 2 Sector Counter Preload Register. This register con-tains the number of sectors in one block of memory.

4.19.24 MCRC0_CRC_CURSEC_REG2 Register (Offset = 88h) [reset = h]

Short Description: Channel 2 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2293. Instance Table

Instance Name	Physical Address
MCRC0	3500 0088h

Figure 4-1101. MCRC0_CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_CURSEC2															
RW															
0															

Access Types Legend

Table 4-2294. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_CURSEC2	RW	0h	Channel 2 Current Sector ID Register. In AUTO mode, thisregister contains the current sector number of which the signatureverification fails. The sector counter is a free running up counter.When a sector fails, the erroneous sector number is logged intocurrent sector ID register and the CRC fail interrupt is generatedThe sector ID register is frozen until it is read and the CRC failstatus bit is cleared by CPU. While it is frozen, it does not captureanother erroneous sector number. When this condition happens,an overrun interrupt is generated instead. Once the register is readand the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

4.19.25 MCRC0_CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = h]

Short Description: Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2295. Instance Table

Instance Name	Physical Address
MCRC0	3500 008Ch

Figure 4-1102. MCRC0_CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_WDTOPLD2							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_WDTOPLD2															
RW															
0															

Access Types Legend

Table 4-2296. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_WDTOPLD2	RW	0h	Channel 2 Watchdog Timeout Counter Preload Register. Thisregister contains the number of clock cycles within which theDMA must transfer the next block of data patterns.

4.19.26 MCRC0_CRC_BCTOPLD2 Register (Offset = 90h) [reset = h]

Short Description: Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2297. Instance Table

Instance Name	Physical Address
MCRC0	3500 0090h

Figure 4-1103. MCRC0_CRC_BCTOPLD2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								CRC_BCTOPLD2							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC_BCTOPLD2															
RW															
0															

Access Types Legend

Table 4-2298. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_BCTOPLD2	RW	0h	Channel 2 Block Complete Timeout Counter Preload Regis-ter. This register contains the number of clock cycles withinwhich the CRC for an entire block needs to complete before atimeout interrupt is generated.

4.19.27 MCRC0_PSA_SIGREGL2 Register (Offset = A0h) [reset = h]

Short Description: Channel 2 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2299. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A0h

Figure 4-1104. MCRC0_PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASIG2_31_0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASIG2_31_0															
RW															
0															

Access Types Legend

Table 4-2300. PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASIG2_31_0	RW	0h	Channel 2 PSA Signature Low Register. This register containsthe value stored at PSASIG2[31:0] register.

4.19.28 MCRC0_PSA_SIGREGH2 Register (Offset = A4h) [reset = h]

Short Description: Channel 2 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2301. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A4h

Figure 4-1105. MCRC0_PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSA_SIG2_63_32															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSA_SIG2_63_32															
RW															
0															

Access Types Legend

Table 4-2302. PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSA_SIG2_63_32	RW	0h	Channel 2 PSA Signature High Register. This register containsthe value stored at PSASIG2[63:32] register.

4.19.29 MCRC0_CRC_REGL2 Register (Offset = A8h) [reset = h]

Short Description: Channel 2 CRC value low register

Long Description:

Return to Summary Table

Table 4-2303. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A8h

Figure 4-1106. MCRC0_CRC_REGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC2_31_0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC2_31_0															
RW															
0															

Access Types Legend

Table 4-2304. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC2_31_0	RW	0h	Channel 2 CRC Value Low Register. This register contains thecurrent known good signature value stored at CRC2[31:0] register.

4.19.30 MCRC0_CRC_REGH2 Register (Offset = ACh) [reset = h]

Short Description: Channel 2 CRC value high register

Long Description:

Return to Summary Table

Table 4-2305. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ACh

Figure 4-1107. MCRC0_CRC_REGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC2_63_32															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC2_63_32															
RW															
0															

Access Types Legend

Table 4-2306. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC2_63_32	RW	0h	Channel 2 CRC Value High Register. This register contains thecurrent known good signature value stored at CRC2[63:32] register.

4.19.31 MCRC0_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = h]

Short Description: Channel 2 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2307. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B0h

Figure 4-1108. MCRC0_PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG2_31_0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG2_31_0															
RO															
0															

Access Types Legend

Table 4-2308. PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG2_31_0	RO	0h	Channel 2 PSA Sector Signature Low Register. This registercontains the value stored at PSASECSIG2[31:0] register.

4.19.32 MCRC0_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = h]

Short Description: Channel 2 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2309. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B4h

Figure 4-1109. MCRC0_PSA_SECSIGREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSASECSIG2_63_32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSASECSIG2_63_32															
RO															
0															

Access Types Legend

Table 4-2310. PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG2_63_32	RO	0h	Channel 2 PSA Sector Signature High Register. This registercontains the value stored at PSASECSIG2[63:32] register.

4.19.33 MCRC0_RAW_DATAREGL2 Register (Offset = B8h) [reset = h]

Short Description: Channel 2 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2311. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B8h

Figure 4-1110. MCRC0_RAW_DATAREGL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA2_31_0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA2_31_0															
RO															
0															

Access Types Legend

Table 4-2312. RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA2_31_0	RO	0h	Channel 2 Raw Data Low Register. This register contains bit31:0 of the un-compressed raw data.

4.19.34 MCRC0_RAW_DATAREGH2 Register (Offset = BCh) [reset = h]

Short Description: Channel 2 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2313. Instance Table

Instance Name	Physical Address
MCRC0	3500 00BCh

Figure 4-1111. MCRC0_RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAW_DATA2_63_32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_DATA2_63_32															
RO															
0															

Access Types Legend

Table 4-2314. RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA2_63_32	RO	0h	Channel 2 Raw Data High Register. This register contains bit63:32 of the un-compressed raw data.

4.19.35 MCRC0_CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = h]

Short Description: Channel 3 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2315. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C0h

Figure 4-1112. MCRC0_CRC_PCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												NU41			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU41															
RO															
0															

Access Types Legend

Table 4-2316. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	NU41	RO	0h	Reserved

4.19.36 MCRC0_CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = h]

Short Description: Channel 3 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2317. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C4h

Figure 4-1113. MCRC0_CRC_SCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42															
RO															
0															

Access Types Legend

Table 4-2318. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU42	RO	0h	Reserved

4.19.37 MCRC0_CRC_CURSEC_REG3 Register (Offset = C8h) [reset = h]

Short Description: Channel 3 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2319. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C8h

Figure 4-1114. MCRC0_CRC_CURSEC_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU43															
RO															
0															

Access Types Legend

Table 4-2320. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU43	RO	0h	Reserved

4.19.38 MCRC0_CRC_WDTOPLD3 Register (Offset = CCh) [reset = h]

Short Description: Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2321. Instance Table

Instance Name	Physical Address
MCRC0	3500 00CCh

Figure 4-1115. MCRC0_CRC_WDTOPLD3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU44							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44															
RO															
0															

Access Types Legend

Table 4-2322. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU44	RO	0h	Reserved

4.19.39 MCRC0_CRC_BCTOPLD3 Register (Offset = D0h) [reset = h]

Short Description: Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2323. Instance Table

Instance Name	Physical Address
MCRC0	3500 00D0h

Figure 4-1116. MCRC0_CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU45							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU45															
RO															
0															

Access Types Legend

Table 4-2324. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU45	RO	0h	Reserved

4.19.40 MCRC0_PSA_SIGREGL3 Register (Offset = E0h) [reset = h]

Short Description: Channel 3 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2325. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E0h

Figure 4-1117. MCRC0_PSA_SIGREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU46															
RO															
0															

Access Types Legend

Table 4-2326. PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU46	RO	0h	Reserved

4.19.41 MCRC0_PSA_SIGREGH3 Register (Offset = E4h) [reset = h]

Short Description: Channel 3 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2327. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E4h

Figure 4-1118. MCRC0_PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47															
RO															
0															

Access Types Legend

Table 4-2328. PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU47	RO	0h	Reserved

4.19.42 MCRC0_CRC_REGL3 Register (Offset = E8h) [reset = h]

Short Description: Channel 3 CRC value low register

Long Description:

Return to Summary Table

Table 4-2329. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E8h

Figure 4-1119. MCRC0_CRC_REGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU48															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU48															
RO															
0															

Access Types Legend

Table 4-2330. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU48	RO	0h	Reserved

4.19.43 MCRC0_CRC_REGH3 Register (Offset = ECh) [reset = h]

Short Description: Channel 3 CRC value high register

Long Description:

Return to Summary Table

Table 4-2331. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ECh

Figure 4-1120. MCRC0_CRC_REGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU49															
RO															
0															

Access Types Legend

Table 4-2332. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU49	RO	0h	Reserved

4.19.44 MCRC0_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = h]

Short Description: Channel 3 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2333. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F0h

Figure 4-1121. MCRC0_PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU50															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50															
RO															
0															

Access Types Legend

Table 4-2334. PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU50	RO	0h	Reserved

4.19.45 MCRC0_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = h]

Short Description: Channel 3 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2335. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F4h

Figure 4-1122. MCRC0_PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU51															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU51															
RO															
0															

Access Types Legend

Table 4-2336. PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU51	RO	0h	Reserved

4.19.46 MCRC0_RAW_DATAREGL3 Register (Offset = F8h) [reset = h]

Short Description: Channel 3 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2337. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F8h

Figure 4-1123. MCRC0_RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU52															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52															
RO															
0															

Access Types Legend

Table 4-2338. RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU52	RO	0h	Reserved

4.19.47 MCRC0_RAW_DATAREGH3 Register (Offset = FCh) [reset = h]

Short Description: Channel 3 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2339. Instance Table

Instance Name	Physical Address
MCRC0	3500 00FCh

Figure 4-1124. MCRC0_RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU53															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU53															
RO															
0															

Access Types Legend

Table 4-2340. RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU53	RO	0h	Reserved

4.19.48 MCRC0_CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = h]

Short Description: Channel 4 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2341. Instance Table

Instance Name	Physical Address
MCRC0	3500 0100h

Figure 4-1125. MCRC0_CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1												NU54			
RO												RO			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU54															
RO															
0															

Access Types Legend

Table 4-2342. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	NU54	RO	0h	Reserved

4.19.49 MCRC0_CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = h]

Short Description: Channel 4 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2343. Instance Table

Instance Name	Physical Address
MCRC0	3500 0104h

Figure 4-1126. MCRC0_CRC_SCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55															
RO															
0															

Access Types Legend

Table 4-2344. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU55	RO	0h	Reserved

4.19.50 MCRC0_CRC_CURSEC_REG4 Register (Offset = 108h) [reset = h]

Short Description: Channel 4 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2345. Instance Table

Instance Name	Physical Address
MCRC0	3500 0108h

Figure 4-1127. MCRC0_CRC_CURSEC_REG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU56															
RO															
0															

Access Types Legend

Table 4-2346. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU56	RO	0h	Reserved

4.19.51 MCRC0_CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = h]

Short Description: Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2347. Instance Table

Instance Name	Physical Address
MCRC0	3500 010Ch

Figure 4-1128. MCRC0_CRC_WDTOPLD4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU57							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU57															
RO															
0															

Access Types Legend

Table 4-2348. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU57	RO	0h	Reserved

4.19.52 MCRC0_CRC_BCTOPLD4 Register (Offset = 110h) [reset = h]

Short Description: Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2349. Instance Table

Instance Name	Physical Address
MCRC0	3500 0110h

Figure 4-1129. MCRC0_CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1								NU58							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58															
RO															
0															

Access Types Legend

Table 4-2350. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU58	RO	0h	Reserved

4.19.53 MCRC0_PSA_SIGREGL4 Register (Offset = 120h) [reset = h]

Short Description: Channel 4 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2351. Instance Table

Instance Name	Physical Address
MCRC0	3500 0120h

Figure 4-1130. MCRC0_PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU59															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU59															
RO															
0															

Access Types Legend

Table 4-2352. PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU59	RO	0h	Reserved

4.19.54 MCRC0_PSA_SIGREGH4 Register (Offset = 124h) [reset = h]

Short Description: Channel 4 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2353. Instance Table

Instance Name	Physical Address
MCRC0	3500 0124h

Figure 4-1131. MCRC0_PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU60															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU60															
RO															
0															

Access Types Legend

Table 4-2354. PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU60	RO	0h	Reserved

4.19.55 MCRC0_CRC_REGL4 Register (Offset = 128h) [reset = h]

Short Description: Channel 4 CRC value low register

Long Description:

Return to Summary Table

Table 4-2355. Instance Table

Instance Name	Physical Address
MCRC0	3500 0128h

Figure 4-1132. MCRC0_CRC_REGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU61															
RO															
0															

Access Types Legend

Table 4-2356. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU61	RO	0h	Reserved

4.19.56 MCRC0_CRC_REGH4 Register (Offset = 12Ch) [reset = h]

Short Description: Channel 4 CRC value high register

Long Description:

Return to Summary Table

Table 4-2357. Instance Table

Instance Name	Physical Address
MCRC0	3500 012Ch

Figure 4-1133. MCRC0_CRC_REGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU62															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU62															
RO															
0															

Access Types Legend

Table 4-2358. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU62	RO	0h	Reserved

4.19.57 MCRC0_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = h]

Short Description: Channel 4 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2359. Instance Table

Instance Name	Physical Address
MCRC0	3500 0130h

Figure 4-1134. MCRC0_PSA_SECSIGREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU63															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63															
RO															
0															

Access Types Legend

Table 4-2360. PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU63	RO	0h	Reserved

4.19.58 MCRC0_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = h]

Short Description: Channel 4 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2361. Instance Table

Instance Name	Physical Address
MCRC0	3500 0134h

Figure 4-1135. MCRC0_PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU64															
RO															
0															

Access Types Legend

Table 4-2362. PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU64	RO	0h	Reserved

4.19.59 MCRC0_RAW_DATAREGL4 Register (Offset = 138h) [reset = h]

Short Description: Channel 4 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2363. Instance Table

Instance Name	Physical Address
MCRC0	3500 0138h

Figure 4-1136. MCRC0_RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65															
RO															
0															

Access Types Legend

Table 4-2364. RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU65	RO	0h	Reserved

4.19.60 MCRC0_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = h]

Short Description: Channel 4 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2365. Instance Table

Instance Name	Physical Address
MCRC0	3500 013Ch

Figure 4-1137. MCRC0_RAW_DATAREGH4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU66															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU66															
RO															
0															

Access Types Legend

Table 4-2366. RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU66	RO	0h	Reserved

4.19.61 MCRC0_MCRC_BUS_SEL Register (Offset = 140h) [reset = h]

Short Description: Disables either or all tracing of data buses

Long Description:

Return to Summary Table

Table 4-2367. Instance Table

Instance Name	Physical Address
MCRC0	3500 0140h

Figure 4-1138. MCRC0_MCRC_BUS_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU67															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU67													MEN	DTCMEN	ITCMEN
RO													RW	RW	RW
0													1	1	1

Access Types Legend

Table 4-2368. MCRC_BUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU67	RO	0h	Reserved
2	MEN	RW	1h	MEn. Enable/disables the tracing of VBUSM 0: Tracing of VBUSM master bus has been disabled 1: Tracing of VBUSM master bus has been enabled
1	DTCMEN	RW	1h	DTCMEn. Enable/disables the tracing of data TCM0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITCMEN	RW	1h	ITCMEn. Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled

4.19.62 MCRC0_MCRC_RESERVED Register (Offset = 144h) [reset = h]

Short Description: 0x144 to 0x1FF is reserved area.

Long Description:

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Table 4-2369. Instance Table

Instance Name	Physical Address
MCRC0	3500 0144h

Figure 4-1139. MCRC0_MCRC_RESERVED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU68															
RO															
0															

Access Types Legend

Table 4-2370. MCRC_RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU68	RO	0h	0x144 to 0x1FF is reserved area.

Table 4-2371. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.20 MSS_QSPI Registers

Table 4-2372. QSPI0, QSPI0_QSPI Registers, Base Address=4820 0000H, Length=1

Offset	Length	Acronym	Register Name	QSPI0 Physical Address
0h	32	QSPI0_PID	PID	4820 0000h
4h	32	QSPI0_MSS_QSPI_RESERVED1	Reserved	4820 0004h
8h	32	QSPI0_MSS_QSPI_RESERVED2	Reserved	4820 0008h
Ch	32	QSPI0_MSS_QSPI_RESERVED3	Reserved	4820 000Ch
10h	32	QSPI0_SYSCONFIG	SYSCONFIG	4820 0010h
14h	32	QSPI0_MSS_QSPI_RESERVED4	Reserved	4820 0014h
18h	32	QSPI0_MSS_QSPI_RESERVED5	Reserved	4820 0018h
1Ch	32	QSPI0_MSS_QSPI_RESERVED6	Reserved	4820 001Ch
20h	32	QSPI0_INTR_STATUS_RAW_SET	INTR Interrupt Status Raw/Set Register	4820 0020h
24h	32	QSPI0_INTR_STATUS_ENABLED_CLEAR	INTR Interrupt Status Enabled/ Clear Register	4820 0024h
28h	32	QSPI0_INTR_ENABLE_SET	INTR Interrupt Enable/Set Register	4820 0028h
2Ch	32	QSPI0_INTR_ENABLE_CLEAR	INTR Interrupt Enable/Clear Register	4820 002Ch
30h	32	QSPI0_INTC_EOI	EOI Register	4820 0030h
34h	32	QSPI0_MSS_QSPI_RESERVED7	Reserved	4820 0034h
38h	32	QSPI0_MSS_QSPI_RESERVED8	Reserved	4820 0038h
3Ch	32	QSPI0_MSS_QSPI_RESERVED9	Reserved	4820 003Ch
40h	32	QSPI0_SPI_CLOCK_CNTRL	SPI Clock Control Register (SPICC)	4820 0040h
44h	32	QSPI0_SPI_DC	SPI Data Control Register (SPIDC)	4820 0044h
48h	32	QSPI0_SPI_CMD	SPI Command Register (SPICR)	4820 0048h
4Ch	32	QSPI0_SPI_STATUS	SPI Status Register (SPISR)	4820 004Ch
50h	32	QSPI0_SPI_DATA	SPI Data Register (SPIDR)	4820 0050h
54h	32	QSPI0_SPI_SETUP0	Memory Mapped SPI Setup0 Register	4820 0054h
58h	32	QSPI0_SPI_SETUP1	Memory Mapped SPI Setup1 Register	4820 0058h
5Ch	32	QSPI0_SPI_SETUP2	Memory Mapped SPI Setup2 Register	4820 005Ch
60h	32	QSPI0_SPI_SETUP3	Memory Mapped SPI Setup3 Register	4820 0060h
64h	32	QSPI0_SPI_SWITCH	Memory Mapped SPI Switch Register	4820 0064h
68h	32	QSPI0_SPI_DATA1	SPI Data Register (SPIDR1)	4820 0068h
6Ch	32	QSPI0_SPI_DATA2	SPI Data Register (SPIDR2)	4820 006Ch
70h	32	QSPI0_SPI_DATA3	SPI Data Register (SPIDR3)	4820 0070h

4.20.1 QSPI0_PID Register (Offset = 0h) [reset = h]

Short Description: PID

Long Description:

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Table 4-2373. Instance Table

Instance Name	Physical Address
QSPI0	4820 0000h

Figure 4-1140. QSPI0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		RO		RO											
1		0		111101000000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
0					0			0		0					

Access Types Legend

Table 4-2374. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	The scheme of the register used. This indicates the PDR3.5 Method
29 - 28	RESERVED	RO		Always read as 0
27 - 16	FUNC	RO	19DE22B940h	The function of the module being used
15 - 11	RTL	RO	0h	RTL Release Version The PDR release number of this IP
10 - 8	MAJOR	RO	0h	Major Release Number
7 - 6	CUSTOM	RO	0h	Custom IP
5 - 0	MINOR	RO	0h	Minor Release Number

4.20.2 QSPI0_MSS_QSPI_RESERVED1 Register (Offset = 4h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2375. Instance Table

Instance Name	Physical Address
QSPI0	4820 0004h

Figure 4-1141. QSPI0_MSS_QSPI_RESERVED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1															
RO															
0															

Access Types Legend

Table 4-2376. MSS_QSPI_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_1	RO	0h	Reserved

4.20.3 QSPI0_MSS_QSPI_RESERVED2 Register (Offset = 8h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2377. Instance Table

Instance Name	Physical Address
QSPI0	4820 0008h

Figure 4-1142. QSPI0_MSS_QSPI_RESERVED2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2															
RO															
0															

Access Types Legend

Table 4-2378. MSS_QSPI_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_2	RO	0h	Reserved

4.20.4 QSPI0_MSS_QSPI_RESERVED3 Register (Offset = Ch) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2379. Instance Table

Instance Name	Physical Address
QSPI0	4820 000Ch

Figure 4-1143. QSPI0_MSS_QSPI_RESERVED3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_3															
RO															
0															

Access Types Legend

Table 4-2380. MSS_QSPI_RESERVED3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_3	RO	0h	Reserved

4.20.5 QSPI0_SYSCONFIG Register (Offset = 10h) [reset = h]

Short Description: SYSCONFIG

Long Description:

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Table 4-2381. Instance Table

Instance Name	Physical Address
QSPI0	4820 0010h

Figure 4-1144. QSPI0_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3										RESERVED2		IDLEMODE		RESERVED1	
RO										RO		RW		RO	
0										0		10		0	

Access Types Legend

Table 4-2382. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED3	RO	0h	Always read as 0
5 - 4	RESERVED2	RO	0h	Always read as 0
3 - 2	IDLEMODE	RW	Ah	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state0x0 : Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only0x1 : No-idle mode: local target never enters idle state. Backup mode, for debug only0x2 : Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events0x3 : Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented
1 - 0	RESERVED1	RO	0h	Always read as 0

4.20.6 QSPI0_MSS_QSPI_RESERVED4 Register (Offset = 14h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2383. Instance Table

Instance Name	Physical Address
QSPI0	4820 0014h

Figure 4-1145. QSPI0_MSS_QSPI_RESERVED4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4															
RO															
0															

Access Types Legend

Table 4-2384. MSS_QSPI_RESERVED4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_4	RO	0h	Reserved

4.20.7 QSPI0_MSS_QSPI_RESERVED5 Register (Offset = 18h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2385. Instance Table

Instance Name	Physical Address
QSPI0	4820 0018h

Figure 4-1146. QSPI0_MSS_QSPI_RESERVED5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_5															
RO															
0															

Access Types Legend

Table 4-2386. MSS_QSPI_RESERVED5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_5	RO	0h	Reserved

4.20.8 QSPI0_MSS_QSPI_RESERVED6 Register (Offset = 1Ch) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2387. Instance Table

Instance Name	Physical Address
QSPI0	4820 001Ch

Figure 4-1147. QSPI0_MSS_QSPI_RESERVED6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_6															
RO															
0															

Access Types Legend

Table 4-2388. MSS_QSPI_RESERVED6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_6	RO	0h	Reserved

4.20.9 QSPI0_INTR_STATUS_RAW_SET Register (Offset = 20h) [reset = h]

Short Description: INTR Interrupt Status Raw/Set Register

Long Description:

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Table 4-2389. Instance Table

Instance Name	Physical Address
QSPI0	4820 0020h

Figure 4-1148. QSPI0_INTR_STATUS_RAW_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_RAW	FIRQ_RAW
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2390. INTR_STATUS_RAW_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_RAW	RW	0h	Word Interrupt Status Read indicates raw status0 = inactive1 = activeWriting 1 will set statusWriting 0 has no effect
0	FIRQ_RAW	RW	0h	Frame Interrupt StatusRead indicates raw status0 = inactive1 = activeWriting 1 will set statusWriting 0 has no effect

4.20.10 QSPI0_INTR_STATUS_ENABLED_CLEAR Register (Offset = 24h) [reset = h]

Short Description: INTR Interrupt Status Enabled/Clear Register

Long Description:

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Table 4-2391. Instance Table

Instance Name	Physical Address
QSPI0	4820 0024h

Figure 4-1149. QSPI0_INTR_STATUS_ENABLED_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA	FIRQ_ENA
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2392. INTR_STATUS_ENABLED_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA	RW	0h	Word Interrupt Enabled StatusRead indicates enabled status0 = inactive1 = activeWriting 1 will clear interruptWriting 0 has no effect
0	FIRQ_ENA	RW	0h	Frame Interrupt Enabled StatusRead indicates enabled status0 = inactive1 = activeWriting 1 will clear interruptWriting 0 has no effect

4.20.11 QSPI0_INTR_ENABLE_SET Register (Offset = 28h) [reset = h]

Short Description: INTR Interrupt Enable/Set Register

Long Description:

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Table 4-2393. Instance Table

Instance Name	Physical Address
QSPI0	4820 0028h

Figure 4-1150. QSPI0_INTR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA_SET	FIRQ_ENA_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2394. INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA_SET	RW	0h	Word Interrupt Enable/SetRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will set interrupt enabledWriting 0 has no effect
0	FIRQ_ENA_SET	RW	0h	Frame Interrupt Enable/SetRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will set interrupt enabledWriting 0 has no effect

4.20.12 QSPI0_INTR_ENABLE_CLEAR Register (Offset = 2Ch) [reset = h]

Short Description: INTR Interrupt Enable/Clear Register

Long Description:

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Table 4-2395. Instance Table

Instance Name	Physical Address
QSPI0	4820 002Ch

Figure 4-1151. QSPI0_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WIRQ_ENA_CLR	FIRQ_ENA_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2396. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA_CLR	RW	0h	Word Interrupt Enable/ClearRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will clear interrupt enabledWriting 0 has no effect
0	FIRQ_ENA_CLR	RW	0h	Frame Interrupt Enable/ClearRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will clear interrupt enabledWriting 0 has no effect

4.20.13 QSPI0_INTC_EOI Register (Offset = 30h) [reset = h]

Short Description: EOI Register

Long Description:

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Table 4-2397. Instance Table

Instance Name	Physical Address
QSPI0	4820 0030h

Figure 4-1152. QSPI0_INTC_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOI_VECTOR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOI_VECTOR															
RW															
0															

Access Types Legend

Table 4-2398. INTC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	EOI_VECTOR	RW	0h	Number associated with the ipgenericirq for intr output. There are 1 interrupt outputsWrite 0x0 : Write to intr IP GenericAny other write value is ignored.

4.20.14 QSPI0_MSS_QSPI_RESERVED7 Register (Offset = 34h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2399. Instance Table

Instance Name	Physical Address
QSPI0	4820 0034h

Figure 4-1153. QSPI0_MSS_QSPI_RESERVED7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_7															
RO															
0															

Access Types Legend

Table 4-2400. MSS_QSPI_RESERVED7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_7	RO	0h	Reserved

4.20.15 QSPI0_MSS_QSPI_RESERVED8 Register (Offset = 38h) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2401. Instance Table

Instance Name	Physical Address
QSPI0	4820 0038h

Figure 4-1154. QSPI0_MSS_QSPI_RESERVED8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_8															
RO															
0															

Access Types Legend

Table 4-2402. MSS_QSPI_RESERVED8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_8	RO	0h	Reserved

4.20.16 QSPI0_MSS_QSPI_RESERVED9 Register (Offset = 3Ch) [reset = h]

Short Description: Reserved

Long Description:

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Table 4-2403. Instance Table

Instance Name	Physical Address
QSPI0	4820 003Ch

Figure 4-1155. QSPI0_MSS_QSPI_RESERVED9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_9															
RO															
0															

Access Types Legend

Table 4-2404. MSS_QSPI_RESERVED9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_9	RO	0h	Reserved

4.20.17 QSPI0_SPI_CLOCK_CNTRL Register (Offset = 40h) [reset = h]

Short Description: SPI Clock Control Register (SPICC)

Long Description:

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Table 4-2405. Instance Table

Instance Name	Physical Address
QSPI0	4820 0040h

Figure 4-1156. QSPI0_SPI_CLOCK_CNTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLKEN	RESERVED														
RW	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCLK_DIV															
RW															
0															

Access Types Legend

Table 4-2406. SPI_CLOCK_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKEN	RW	0h	Clock Enable. 0- Data clock is turned off1- Data clock is enabled
30 - 16	RESERVED	RO		Always read as 0
15 - 0	DCLK_DIV	RW	0h	Serial data clock divide by ratio

4.20.18 QSPI0_SPI_DC Register (Offset = 44h) [reset = h]

Short Description: SPI Data Control Register (SPIDC)

Long Description:

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Table 4-2407. Instance Table

Instance Name	Physical Address
QSPI0	4820 0044h

Figure 4-1157. QSPI0_SPI_DC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4			DD3		CKPH3	CSP3	CKP3	RESERVED3			DD2		CKPH2	CSP2	CKP2
RO			RW		RW	RW	RW	RO			RW		RW	RW	RW
0			0		0	0	0	0			0		0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2			DD1		CKPH1	CSP1	CKP1	RESERVED1			DD0		CKPH0	CSP0	CKP0
RO			RW		RW	RW	RW	RO			RW		RW	RW	RW
0			0		0	0	0	0			0		0	0	0

Access Types Legend

Table 4-2408. SPI_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED4	RO	0h	Always read as 0
28 - 27	DD3	RW	0h	Data delay for chip select 300- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
26	CKPH3	RW	0h	Clock phase for chip select 3 If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
25	CSP3	RW	0h	Chip select polarity for chip select 30- Active low1- Active high
24	CKP3	RW	0h	Clock polarity for chip select 30- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1
23 - 21	RESERVED3	RO	0h	Always read as 0
20 - 19	DD2	RW	0h	Data delay for chip select 200- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
18	CKPH2	RW	0h	Clock phase for chip select 2. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
17	CSP2	RW	0h	Chip select polarity for chip select 20- Active low1- Active high
16	CKP2	RW	0h	Clock polarity for chip select 20- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1
15 - 13	RESERVED2	RO	0h	Always read as 0
12 - 11	DD1	RW	0h	Data delay for chip select 100- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active

Table 4-2408. SPI_DC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CKPH1	RW	0h	Clock phase for chip select 1. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
9	CSP1	RW	0h	Chip select polarity for chip select 10- Active low1- Active high
8	CKP1	RW	0h	Clock polarity for chip select 10- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1
7 - 5	RESERVED1	RO	0h	Always read as 0
4 - 3	DD0	RW	0h	Data delay for chip select 000- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
2	CKPH0	RW	0h	Clock phase for chip select 0. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
1	CSP0	RW	0h	Chip select polarity for chip select 00- Active low1- Active high
0	CKP0	RW	0h	Clock polarity for chip select 00- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1

4.20.19 QSPI0_SPI_CMD Register (Offset = 48h) [reset = h]

Short Description: SPI Command Register (SPICR)

Long Description:

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Table 4-2409. Instance Table

Instance Name	Physical Address
QSPI0	4820 0048h

Figure 4-1158. QSPI0_SPI_CMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3		CSNUM		RESERVED2		WLEN							CMD		
RO		RW		RO		RW							RW		
0		0		0		0							0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRQ	WIRQ	RESERVED1		FLEN											
RW	RW	RO		RW											
0	0	0		0											

Access Types Legend

Table 4-2410. SPI_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED3	RO	0h	Always read as 0
29 - 28	CSNUM	RW	0h	Device select. Sets the active chip select for the transfer00- Chip Select 0 active01- Chip Select 1 active10- Chip Select 2 active11- Chip Select 3 active
27 - 26	RESERVED2	RO	0h	Always read as 0
25 - 19	WLEN	RW	0h	Word length. Sets the size of the individual transfers from 1 ? 128 bits0- 1 bit1- 2 bits?127 ? 128 bits
18 - 16	CMD	RW	0h	Transfer command000- Reserved001- 4 pin Read Single 010- 4 pin Write Single011- 4 pin Read Dual100 ? Reserved101 ? 3 pin Read Single110 ? 3 pin Write Single 111 ? 6 pin Read Quad
15	FIRQ	RW	0h	Frame count interrupt enable
14	WIRQ	RW	0h	Word count interrupt enable
13 - 12	RESERVED1	RO	0h	Always read as 0
11 - 0	FLEN	RW	0h	Frame Length0- 1 word1- 2 words?4095 ? 4096 words

4.20.20 QSPI0_SPI_STATUS Register (Offset = 4Ch) [reset = h]

Short Description: SPI Status Register (SPISR)

Long Description:

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Table 4-2411. Instance Table

Instance Name	Physical Address
QSPI0	4820 004Ch

Figure 4-1159. QSPI0_SPI_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2				WDCNT											
RO				RO											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1													FC	WC	BUSY
RO													RO	RO	RO
0													0	0	0

Access Types Legend

Table 4-2412. SPI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	RESERVED2	RO	0h	Always read as 0
27 - 16	WDCNT	RO	0h	Word count. This field will reflect the 1-4096 words transferred
15 - 3	RESERVED1	RO	0h	Always read as 0
2	FC	RO	0h	Frame complete. This bit is set after all of the requested words have been transmitted.0- Transfer is not complete1- Transfer is completeThis bit is reset when the SPI Status Register is read
1	WC	RO	0h	Word complete. This bit is set after each word transfer is completed.0- Word transfer is not complete1- Word transfer is completeThis bit is reset when the SPI Status Register is read
0	BUSY	RO	0h	Busy bit. Active transfer in progress. This bit is only set during an active word transfer. Between words, the bit will clear to signal that it is ok to read/write the data registers.0- Idle1- Busy

4.20.21 QSPI0_SPI_DATA Register (Offset = 50h) [reset = h]

Short Description: SPI Data Register (SPIDR)

Long Description:

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Table 4-2413. Instance Table

Instance Name	Physical Address
QSPI0	4820 0050h

Figure 4-1160. QSPI0_SPI_DATA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
RW															
0															

Access Types Legend

Table 4-2414. SPI_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

4.20.22 QSPI0_SPI_SETUP0 Register (Offset = 54h) [reset = h]

Short Description: Memory Mapped SPI Setup0 Register

Long Description:

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Table 4-2415. Instance Table

Instance Name	Physical Address
QSPI0	4820 0054h

Figure 4-1161. QSPI0_SPI_SETUP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
RO			RW					RW							
0			0					10							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
RO		RW		RW		RW		RW							
0		0		0		10		11							

Access Types Legend

Table 4-2416. SPI_SETUP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

4.20.23 QSPI0_SPI_SETUP1 Register (Offset = 58h) [reset = h]

Short Description: Memory Mapped SPI Setup1 Register

Long Description:

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Table 4-2417. Instance Table

Instance Name	Physical Address
QSPI0	4820 0058h

Figure 4-1162. QSPI0_SPI_SETUP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
RO			RW					RW							
0			0					10							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
RO		RW		RW		RW		RW							
0		0		0		10		11							

Access Types Legend

Table 4-2418. SPI_SETUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

4.20.24 QSPI0_SPI_SETUP2 Register (Offset = 5Ch) [reset = h]

Short Description: Memory Mapped SPI Setup2 Register

Long Description:

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Table 4-2419. Instance Table

Instance Name	Physical Address
QSPI0	4820 005Ch

Figure 4-1163. QSPI0_SPI_SETUP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
RO			RW					RW							
0			0					10							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
RO		RW		RW		RW		RW							
0		0		0		10		11							

Access Types Legend

Table 4-2420. SPI_SETUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

4.20.25 QSPI0_SPI_SETUP3 Register (Offset = 60h) [reset = h]

Short Description: Memory Mapped SPI Setup3 Register

Long Description:

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Table 4-2421. Instance Table

Instance Name	Physical Address
QSPI0	4820 0060h

Figure 4-1164. QSPI0_SPI_SETUP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2			NUM_D_BITS					WCMD							
RO			RW					RW							
0			0					10							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1		READ_TYPE		NUM_D_BYTES		NUM_A_BYTES		RCMD							
RO		RW		RW		RW		RW							
0		0		0		10		11							

Access Types Legend

Table 4-2422. SPI_SETUP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

4.20.26 QSPI0_SPI_SWITCH Register (Offset = 64h) [reset = h]

Short Description: Memory Mapped SPI Switch Register

Long Description:

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Table 4-2423. Instance Table

Instance Name	Physical Address
QSPI0	4820 0064h

Figure 4-1165. QSPI0_SPI_SWITCH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MM_INT_EN	MMPT_S
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2424. SPI_SWITCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	MM_INT_EN	RW	0h	Memory Mapped mode interrupt enable.0 ? Interrupts are disabled during memory mapped operations1 ? Word Count interrupt is enabled for memory mapped operations
0	MMPT_S	RW	0h	MMPT select. If 0 (default) config port has is selected to control config of core SPI module. If 1, Memory Mapped Protocol Translator is selected to control config port of core SPI module.

4.20.27 QSPI0_SPI_DATA1 Register (Offset = 68h) [reset = h]

Short Description: SPI Data Register (SPIDR1)

Long Description:

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Table 4-2425. Instance Table

Instance Name	Physical Address
QSPI0	4820 0068h

Figure 4-1166. QSPI0_SPI_DATA1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
RW															
0															

Access Types Legend

Table 4-2426. SPI_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

4.20.28 QSPI0_SPI_DATA2 Register (Offset = 6Ch) [reset = h]

Short Description: SPI Data Register (SPIDR2)

Long Description:

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Table 4-2427. Instance Table

Instance Name	Physical Address
QSPI0	4820 006Ch

Figure 4-1167. QSPI0_SPI_DATA2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
RW															
0															

Access Types Legend

Table 4-2428. SPI_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

4.20.29 QSPI0_SPI_DATA3 Register (Offset = 70h) [reset = h]

Short Description: SPI Data Register (SPIDR3)

Long Description:

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Table 4-2429. Instance Table

Instance Name	Physical Address
QSPI0	4820 0070h

Figure 4-1168. QSPI0_SPI_DATA3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
RW															
0															

Access Types Legend

Table 4-2430. SPI_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

Table 4-2431. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.21 MSS_RTI Registers

Table 4-2432. HSM_RTI0, HSM_RTI0_HSM_RTI Registers, Base Address=47F7 8C00H, Length=1

Offset	Length	Acronym	Register Name	HSM_RTI0 Physical Address
0h	32	HSM_RTI0_RTIGCTRL	Global Control Register starts / stops the counters	47F7 8C00h
4h	32	HSM_RTI0_RTITBCTRL	Timebase Control selection which source triggers free running counter 0	47F7 8C04h
8h	32	HSM_RTI0_RTICAPCTRL	Capture Control controls the capture source for the counters	47F7 8C08h
Ch	32	HSM_RTI0_RTICOMPCTRL	Compare Control controls the source for the compare registers	47F7 8C0Ch
10h	32	HSM_RTI0_RTIFRC0	Free Running Counter 0 current value of free running counter 0	47F7 8C10h
14h	32	HSM_RTI0_RTIUC0	Up Counter 0 current value of prescale counter 0	47F7 8C14h
18h	32	HSM_RTI0_RTICPUC0	Compare Up Counter 0 compare value compared with prescale counter 0	47F7 8C18h
20h	32	HSM_RTI0_RTICAFRC0	Capture Free Running Counter 0 current value of free running counter 0 on external event	47F7 8C20h
24h	32	HSM_RTI0_RTICAUC0	Capture Up Counter 0 current value of prescale counter 0 on external event	47F7 8C24h
30h	32	HSM_RTI0_RTIFRC1	Free Running Counter 1 current value of free running counter 1	47F7 8C30h
34h	32	HSM_RTI0_RTIUC1	Up Counter 1 current value of prescale counter 1	47F7 8C34h
38h	32	HSM_RTI0_RTICPUC1	Compare Up Counter 1 compare value compared with prescale counter 1	47F7 8C38h
40h	32	HSM_RTI0_RTICAFRC1	Capture Free Running Counter 1 current value of free running counter 1 on external event	47F7 8C40h
44h	32	HSM_RTI0_RTICAUC1	Capture Up Counter 1 current value of prescale counter 1 on external event	47F7 8C44h
50h	32	HSM_RTI0_RTICOMP0	Compare 0 compare value to be compared with the counters	47F7 8C50h
54h	32	HSM_RTI0_RTIUDCP0	Update Compare 0 value to be added to the compare register 0 value on compare match	47F7 8C54h
58h	32	HSM_RTI0_RTICOMP1	Compare 1 compare value to be compared with the counters	47F7 8C58h
5Ch	32	HSM_RTI0_RTIUDCP1	Update Compare 1 value to be added to the compare register 1 value on compare match	47F7 8C5Ch
60h	32	HSM_RTI0_RTICOMP2	Compare 2 compare value to be compared with the counters	47F7 8C60h

Table 4-2432. HSM_RTI0, HSM_RTI0_HSM_RTI Registers, Base Address=47F7 8C00H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_RTI0 Physical Address
64h	32	HSM_RTI0_RTIUDCP2	Update Compare 2 value to be added to the compare register 2 value on compare match	47F7 8C64h
68h	32	HSM_RTI0_RTICOMP3	Compare 3 compare value to be compared with the counters	47F7 8C68h
6Ch	32	HSM_RTI0_RTIUDCP3	Update Compare 3 value to be added to the compare register 3 value on compare match	47F7 8C6Ch
70h	32	HSM_RTI0_RTITBLCOMP	Timebase Low Compare compare value to activate edge detection circuit	47F7 8C70h
74h	32	HSM_RTI0_RTITBHCOMP	Timebase High Compare compare value to deactivate edge detection circuit	47F7 8C74h
80h	32	HSM_RTI0_RTISETINT	Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation	47F7 8C80h
84h	32	HSM_RTI0_RTICLEARINT	Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation	47F7 8C84h
88h	32	HSM_RTI0_RTIINTFLAG	Interrupt Flags interrupt pending bits	47F7 8C88h
90h	32	HSM_RTI0_RTIDWDCTRL	Digital Watchdog Control Enables the Digital Watchdog	47F7 8C90h
94h	32	HSM_RTI0_RTIDWDPRLD	Digital Watchdog Preload sets the experation time of the Digital Watchdog	47F7 8C94h
98h	32	HSM_RTI0_RTIWDSTATUS	Watchdog Status reflects the status of Analog and Digital Watchdog	47F7 8C98h
9Ch	32	HSM_RTI0_RTIWDKEY	Watchdog Key correct written key values discharge the external capacitor	47F7 8C9Ch
A0h	32	HSM_RTI0_RTIDWDCNTR	Digital Watchdog Down Counter current value of DWD down counter	47F7 8CA0h
A4h	32	HSM_RTI0_RTIWWDRXNCTRL	Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset	47F7 8CA4h
A8h	32	HSM_RTI0_RTIWWDSIZECTRL	Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog	47F7 8CA8h
ACh	32	HSM_RTI0_RTIINTCLRENABLE	RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts	47F7 8CACh
B0h	32	HSM_RTI0_RTICOMP0CLR	Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line	47F7 8CB0h

Table 4-2432. HSM_RTI0, HSM_RTI0_HSM_RTI Registers, Base Address=47F7 8C00H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_RTI0 Physical Address
B4h	32	HSM_RTI0_RTICOMP1CLR	Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line	47F7 8CB4h
B8h	32	HSM_RTI0_RTICOMP2CLR	Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line	47F7 8CB8h
BCh	32	HSM_RTI0_RTICOMP3CLR	Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line	47F7 8CBCh

Table 4-2433. HSM_WDT0, HSM_WDT0_HSM_WDT Registers, Base Address=47F7 8D00H, Length=1

Offset	Length	Acronym	Register Name	HSM_WDT0 Physical Address
0h	32	HSM_WDT0_RTIGCTRL	Global Control Register starts / stops the counters	47F7 8D00h
4h	32	HSM_WDT0_RTITBCTRL	Timebase Control selection which source triggers free running counter 0	47F7 8D04h
8h	32	HSM_WDT0_RTICAPCTRL	Capture Control controls the capture source for the counters	47F7 8D08h
Ch	32	HSM_WDT0_RTICOMPCTRL	Compare Control controls the source for the compare registers	47F7 8D0Ch
10h	32	HSM_WDT0_RTIFRC0	Free Running Counter 0 current value of free running counter 0	47F7 8D10h
14h	32	HSM_WDT0_RTIUC0	Up Counter 0 current value of prescale counter 0	47F7 8D14h
18h	32	HSM_WDT0_RTICPUC0	Compare Up Counter 0 compare value compared with prescale counter 0	47F7 8D18h
20h	32	HSM_WDT0_RTICAFRC0	Capture Free Running Counter 0 current value of free running counter 0 on external event	47F7 8D20h
24h	32	HSM_WDT0_RTICAUC0	Capture Up Counter 0 current value of prescale counter 0 on external event	47F7 8D24h
30h	32	HSM_WDT0_RTIFRC1	Free Running Counter 1 current value of free running counter 1	47F7 8D30h
34h	32	HSM_WDT0_RTIUC1	Up Counter 1 current value of prescale counter 1	47F7 8D34h
38h	32	HSM_WDT0_RTICPUC1	Compare Up Counter 1 compare value compared with prescale counter 1	47F7 8D38h
40h	32	HSM_WDT0_RTICAFRC1	Capture Free Running Counter 1 current value of free running counter 1 on external event	47F7 8D40h
44h	32	HSM_WDT0_RTICAUC1	Capture Up Counter 1 current value of prescale counter 1 on external event	47F7 8D44h
50h	32	HSM_WDT0_RTICOMP0	Compare 0 compare value to be compared with the counters	47F7 8D50h
54h	32	HSM_WDT0_RTIUDCP0	Update Compare 0 value to be added to the compare register 0 value on compare match	47F7 8D54h

Table 4-2433. HSM_WDT0, HSM_WDT0_HSM_WDT Registers, Base Address=47F7 8D00H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_WDT0 Physical Address
58h	32	HSM_WDT0_RTICOMP1	Compare 1 compare value to be compared with the counters	47F7 8D58h
5Ch	32	HSM_WDT0_RTIUDCP1	Update Compare 1 value to be added to the compare register 1 value on compare match	47F7 8D5Ch
60h	32	HSM_WDT0_RTICOMP2	Compare 2 compare value to be compared with the counters	47F7 8D60h
64h	32	HSM_WDT0_RTIUDCP2	Update Compare 2 value to be added to the compare register 2 value on compare match	47F7 8D64h
68h	32	HSM_WDT0_RTICOMP3	Compare 3 compare value to be compared with the counters	47F7 8D68h
6Ch	32	HSM_WDT0_RTIUDCP3	Update Compare 3 value to be added to the compare register 3 value on compare match	47F7 8D6Ch
70h	32	HSM_WDT0_RTITBLCOMP	Timebase Low Compare compare value to activate edge detection circuit	47F7 8D70h
74h	32	HSM_WDT0_RTITBHCOMP	Timebase High Compare compare value to deactivate edge detection circuit	47F7 8D74h
80h	32	HSM_WDT0_RTISETINT	Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation	47F7 8D80h
84h	32	HSM_WDT0_RTICLEARINT	Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation	47F7 8D84h
88h	32	HSM_WDT0_RTIINTFLAG	Interrupt Flags interrupt pending bits	47F7 8D88h
90h	32	HSM_WDT0_RTIDWDCTRL	Digital Watchdog Control Enables the Digital Watchdog	47F7 8D90h
94h	32	HSM_WDT0_RTIDWDPRLD	Digital Watchdog Preload sets the experation time of the Digital Watchdog	47F7 8D94h
98h	32	HSM_WDT0_RTIWDSTATUS	Watchdog Status reflects the status of Analog and Digital Watchdog	47F7 8D98h
9Ch	32	HSM_WDT0_RTIWDKEY	Watchdog Key correct written key values discharge the external capacitor	47F7 8D9Ch
A0h	32	HSM_WDT0_RTIDWDCNTR	Digital Watchdog Down Counter current value of DWD down counter	47F7 8DA0h
A4h	32	HSM_WDT0_RTIWWDRXNCTRL	Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset	47F7 8DA4h
A8h	32	HSM_WDT0_RTIWWDSIZECTRL	Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog	47F7 8DA8h

Table 4-2433. HSM_WDT0, HSM_WDT0_HSM_WDT Registers, Base Address=47F7 8D00H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_WDT0 Physical Address
ACh	32	HSM_WDT0_RTIINTCLRENABLE	RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts	47F7 8DACh
B0h	32	HSM_WDT0_RTICOMP0CLR	Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line	47F7 8DB0h
B4h	32	HSM_WDT0_RTICOMP1CLR	Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line	47F7 8DB4h
B8h	32	HSM_WDT0_RTICOMP2CLR	Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line	47F7 8DB8h
BCh	32	HSM_WDT0_RTICOMP3CLR	Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line	47F7 8DBCh

4.21.1 HSM_RTI0_RTIGCTRL Register (Offset = 0h) [reset = h]

Short Description: Global Control Register starts / stops the counters

Long Description:

Return to Summary Table

Table 4-2434. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C00h

Figure 4-1169. HSM_RTI0_RTIGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2												NTUSEL			
RW												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS	RESERVED1													CNT1EN	CNT0EN
RW	RW													RW	RW
0	0													0	0

Access Types Legend

Table 4-2435. RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED2	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	NTUSEL	RW	0h	NTUSEL: Select NTU signal.These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL.User and privilege mode (read):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0? Privilege mode (write):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0?
15	COS	RW	0h	COS: Continue On Suspend.This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.User and privilege mode (read):0 = counters are stopped while in debug mode1 = counters are running while in debug modePrivilege mode (write):0 = stop counters in debug mode1 = continue counting in debug mode
14 - 2	RESERVED1	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CNT1EN	RW	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bit destination address (physical).
0	CNT0EN	RW	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bits source address (physical).

4.21.2 HSM_RTI0_RTITBCTRL Register (Offset = 4h) [reset = h]

Short Description: Timebase Control selection which source triggers free running counter 0

Long Description:

Return to Summary Table

Table 4-2436. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C04h

Figure 4-1170. HSM_RTI0_RTITBCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3														INC	TBEXT
RW														RW	RW
0														0	0

Access Types Legend

Table 4-2437. RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED3	RW	0h	Reserved
1	INC	RW	0h	INC: Increment Free Running Counter 0.This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.User and privilege mode (read):0 = FRC0 will not be incremented1 = FRC0 will be incrementedPrivilege mode (write):0 = Do not increment FRC0 on failing external clock1 = Increment FRC0 on failing external clock
0	TBEXT	RW	0h	TBEXT: Timebase External.The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx.When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset.The selection if the external signal should be used, can only be done by software.User and privilege mode (read):0 = UC0 clocks FRC01 = NTUx clocks FRC0Privilege mode (write):0 = MUX is switched to internal UC0 clocking scheme1 = MUX is switched to external NTUx clocking scheme

4.21.3 HSM_RTI0_RTICAPCTRL Register (Offset = 8h) [reset = h]

Short Description: Capture Control controls the capture source for the counters

Long Description:

Return to Summary Table

Table 4-2438. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C08h

Figure 4-1171. HSM_RTI0_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED4														CAPCNTR1	CAPCNTR0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-2439. RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED4	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CAPCNTR1	RW	0h	CAPCNTR1: Capture Counter 1.This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 1
0	CAPCNTR0	RW	0h	CAPCNTR0: Capture Counter 0.This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 111 indexed10 reserved01 post-increment00 constant

4.21.4 HSM_RTI0_RTICOMPCTRL Register (Offset = Ch) [reset = h]

Short Description: Compare Control controls the source for the compare registers

Long Description:

Return to Summary Table

Table 4-2440. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C0Ch

Figure 4-1172. HSM_RTI0_RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED8															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED8			COMP 3SEL	RESERVED7			COMP 2SEL	RESERVED6			COMP 1SEL	RESERVED5			COMP 0SEL
RW			RW	RW			RW	RW			RW	RW			RW
0			0	0			0	0			0	0			0

Access Types Legend

Table 4-2441. RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RESERVED8	RW	0h	Reserved.Reads return 0 and writes have no effect
12	COMP3SEL	RW	0h	COMPSEL3: Compare Select 3.This bit determines the counter with which the compare value hold in compare register 3 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
11 - 9	RESERVED7	RW	0h	Reserved.Reads return 0 and writes have no effect
8	COMP2SEL	RW	0h	COMPSEL2: Compare Select 2.This bit determines the counter with which the compare value hold in compare register 2 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
7 - 5	RESERVED6	RW	0h	Reserved.Reads return 0 and writes have no effect
4	COMP1SEL	RW	0h	COMPSEL1: Compare Select 1.This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
3 - 1	RESERVED5	RW	0h	Reserved.Reads return 0 and writes have no effect
0	COMP0SEL	RW	0h	COMPSEL0: Compare Select 0.This bit determines the counter with which the compare value hold in compare register 0 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1

4.21.5 HSM_RTI0_RTIFRC0 Register (Offset = 10h) [reset = h]

Short Description: Free Running Counter 0 current value of free running counter 0

Long Description:

Return to Summary Table

Table 4-2442. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C10h

Figure 4-1173. HSM_RTI0_RTIFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC0															
RW															
0															

Access Types Legend

Table 4-2443. RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC0	RW	0h	FRC0: Free Running Counter 0.This registers holds the current value of the Free Running Counter 0 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

4.21.6 HSM_RTI0_RTIUC0 Register (Offset = 14h) [reset = h]

Short Description: Up Counter 0 current value of prescale counter 0

Long Description:

Return to Summary Table

Table 4-2444. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C14h

Figure 4-1174. HSM_RTI0_RTIUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC0															
RW															
0															

Access Types Legend

Table 4-2445. RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC0	RW	0h	UC0: Up Counter 0.This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.User and privilege mode (read):value of the counter when the Free Running Counter 0 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

4.21.7 HSM_RTI0_RTICPUC0 Register (Offset = 18h) [reset = h]

Short Description: Compare Up Counter 0 compare value compared with prescale counter 0

Long Description:

Return to Summary Table

Table 4-2446. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C18h

Figure 4-1175. HSM_RTI0_RTICPUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC0															
RW															
0															

Access Types Legend

Table 4-2447. RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC0	RW	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock.If CPUC0 = 0: then, frequency = RTICLK/ (2^32)If CPUC0 ? 0: then , frequency = RTICLK/(CPUC0 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

4.21.8 HSM_RTI0_RTICAFRC0 Register (Offset = 20h) [reset = h]

Short Description: Capture Free Running Counter 0 current value of free running counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2448. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C20h

Figure 4-1176. HSM_RTI0_RTICAFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC0															
RW															
0															

Access Types Legend

Table 4-2449. RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC0	RW	0h	CAFRC0: Capture Free Running Counter 0.This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 0 on a capture event

4.21.9 HSM_RTI0_RTICAUC0 Register (Offset = 24h) [reset = h]

Short Description: Capture Up Counter 0 current value of prescale counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2450. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C24h

Figure 4-1177. HSM_RTI0_RTICAUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC0															
RW															
0															

Access Types Legend

Table 4-2451. RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC0	RW	0h	CAUC0: Capture Up Counter 0.This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 0 on a capture event

4.21.10 HSM_RTI0_RTIFRC1 Register (Offset = 30h) [reset = h]

Short Description: Free Running Counter 1 current value of free running counter 1

Long Description:

Return to Summary Table

Table 4-2452. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C30h

Figure 4-1178. HSM_RTI0_RTIFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC1															
RW															
0															

Access Types Legend

Table 4-2453. RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC1	RW	0h	FRC1: Free Running Counter 1.This registers holds the current value of the Free Running Counter 1 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

4.21.11 HSM_RTI0_RTIUC1 Register (Offset = 34h) [reset = h]

Short Description: Up Counter 1 current value of prescale counter 1

Long Description:

Return to Summary Table

Table 4-2454. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C34h

Figure 4-1179. HSM_RTI0_RTIUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC1															
RW															
0															

Access Types Legend

Table 4-2455. RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC1	RW	0h	UC1: Up Counter 1.This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.User and privilege mode (read):value of the counter when the Free Running Counter 1 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

4.21.12 HSM_RTI0_RTICPUC1 Register (Offset = 38h) [reset = h]

Short Description: Compare Up Counter 1 compare value compared with prescale counter 1

Long Description:

Return to Summary Table

Table 4-2456. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C38h

Figure 4-1180. HSM_RTI0_RTICPUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC1															
RW															
0															

Access Types Legend

Table 4-2457. RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC1	RW	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock.If CPUC1 = 0: then, frequency = RTICLK/ (2^32)If CPUC1 ? 0: then , frequency = RTICLK/(CPUC1 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

4.21.13 HSM_RTI0_RTICAFRC1 Register (Offset = 40h) [reset = h]

Short Description: Capture Free Running Counter 1 current value of free running counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2458. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C40h

Figure 4-1181. HSM_RTI0_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC1															
RW															
0															

Access Types Legend

Table 4-2459. RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC1	RW	0h	CAFRC1: Capture Free Running Counter 1.This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 1 on a capture event

4.21.14 HSM_RTI0_RTICAUC1 Register (Offset = 44h) [reset = h]

Short Description: Capture Up Counter 1 current value of prescale counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2460. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C44h

Figure 4-1182. HSM_RTI0_RTICAUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC1															
RW															
0															

Access Types Legend

Table 4-2461. RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC1	RW	0h	CAUC1: Capture Up Counter 1.This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 1 on a capture event

4.21.15 HSM_RTI0_RTICOMP0 Register (Offset = 50h) [reset = h]

Short Description: Compare 0 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2462. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C50h

Figure 4-1183. HSM_RTI0_RTICOMP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0															
RW															
0															

Access Types Legend

Table 4-2463. RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0	RW	0h	COMP0: Compare 0.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.16 HSM_RTI0_RTIUDCP0 Register (Offset = 54h) [reset = h]

Short Description: Update Compare 0 value to be added to the compare register 0 value on compare match

Long Description:

Return to Summary Table

Table 4-2464. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C54h

Figure 4-1184. HSM_RTI0_RTIUDCP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP0															
RW															
0															

Access Types Legend

Table 4-2465. RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP0	RW	0h	UDCP0: Update Compare 0 Register.This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 0 register on the next compare matchPrivilege mode (write):new update value

4.21.17 HSM_RTI0_RTICOMP1 Register (Offset = 58h) [reset = h]

Short Description: Compare 1 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2466. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C58h

Figure 4-1185. HSM_RTI0_RTICOMP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1															
RW															
0															

Access Types Legend

Table 4-2467. RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1	RW	0h	COMP1: compare1.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.18 HSM_RTI0_RTIUDCP1 Register (Offset = 5Ch) [reset = h]

Short Description: Update Compare 1 value to be added to the compare register 1 value on compare match

Long Description:

Return to Summary Table

Table 4-2468. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C5Ch

Figure 4-1186. HSM_RTI0_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP1															
RW															
0															

Access Types Legend

Table 4-2469. RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP1	RW	0h	UDCP1: Update compare1 Register.This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare1 register on the next compare matchPrivilege mode (write):new update value

4.21.19 HSM_RTI0_RTICOMP2 Register (Offset = 60h) [reset = h]

Short Description: Compare 2 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2470. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C60h

Figure 4-1187. HSM_RTI0_RTICOMP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2															
RW															
0															

Access Types Legend

Table 4-2471. RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2	RW	0h	COMP2: compare 2.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.20 HSM_RTI0_RTIUDCP2 Register (Offset = 64h) [reset = h]

Short Description: Update Compare 2 value to be added to the compare register 2 value on compare match

Long Description:

Return to Summary Table

Table 4-2472. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C64h

Figure 4-1188. HSM_RTI0_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP2															
RW															
0															

Access Types Legend

Table 4-2473. RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP2	RW	0h	UDCP2: Update compare 2 Register.This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 2 register on the next compare matchPrivilege mode (write):new update value

4.21.21 HSM_RTI0_RTICOMP3 Register (Offset = 68h) [reset = h]

Short Description: Compare 3 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2474. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C68h

Figure 4-1189. HSM_RTI0_RTICOMP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3															
RW															
0															

Access Types Legend

Table 4-2475. RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3	RW	0h	COMP3: compare 3.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.22 HSM_RTI0_RTIUDCP3 Register (Offset = 6Ch) [reset = h]

Short Description: Update Compare 3 value to be added to the compare register 3 value on compare match

Long Description:

Return to Summary Table

Table 4-2476. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C6Ch

Figure 4-1190. HSM_RTI0_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP3															
RW															
0															

Access Types Legend

Table 4-2477. RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP3	RW	0h	UDCP3: Update compare 3 Register.This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 3 register on the next compare matchPrivilege mode (write):new update value

4.21.23 HSM_RTI0_RTITBLCOMP Register (Offset = 70h) [reset = h]

Short Description: Timebase Low Compare compare value to activate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2478. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C70h

Figure 4-1191. HSM_RTI0_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBLCOMP															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLCOMP															
RW															
0															

Access Types Legend

Table 4-2479. RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBLCOMP	RW	0h	TBLCOMP: Timebase Low Compare Value.This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0.User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

4.21.24 HSM_RTI0_RTITBHCOMP Register (Offset = 74h) [reset = h]

Short Description: Timebase High Compare compare value to deactivate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2480. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C74h

Figure 4-1192. HSM_RTI0_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBHCOMP															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBHCOMP															
RW															
0															

Access Types Legend

Table 4-2481. RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBHCOMP	RW	0h	TBHCOMP: Timebase High Compare Value.This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0.RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached.Example:The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0.RTICPUC0 = 0x00000050RTITBLCOMP = 0x000046RTITBHCOMP = 0x00000009User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

4.21.25 HSM_RTI0_RTISETINT Register (Offset = 80h) [reset = h]

Short Description: Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2482. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C80h

Figure 4-1193. HSM_RTI0_RTISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED11													SETOVL1INT	SETOVL0INT	SETTBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0	RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
RW				RW	RW	RW	RW	RW				RW	RW	RW	RW
0				0	0	0	0	0				0	0	0	0

Access Types Legend

Table 4-2483. RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED11	RW	0h	Reserved.Reads return 0 and writes have no effect
18	SETOVL1INT	RW	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
17	SETOVL0INT	RW	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
16	SETTBINT	RW	0h	SETTBINT: Set Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
15 - 12	RESERVED10	RW	0h	Reserved.Reads return 0 and writes have no effect
11	SETDMA3	RW	0h	SETDMA3: Set Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
10	SETDMA2	RW	0h	SETDMA2: Set Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
9	SETDMA1	RW	0h	SETDMA1: Set Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
8	SETDMA0	RW	0h	SETDMA0: Set Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
7 - 4	RESERVED9	RW	0h	Reserved.Reads return 0 and writes have no effect

Table 4-2483. RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SETINT3	RW	0h	SETINT3: Set Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged
2	SETINT2	RW	0h	SETINT2: Set Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
1	SETINT1	RW	0h	SETINT1: Set Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
0	SETINT0	RW	0h	SETINT0: Set Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt

4.21.26 HSM_RTI0_RTICLEARINT Register (Offset = 84h) [reset = h]

Short Description: Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2484. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C84h

Figure 4-1194. HSM_RTI0_RTICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED14													CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0	RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
RW				RW	RW	RW	RW	RW				RW	RW	RW	RW
0				0	0	0	0	0				0	0	0	0

Access Types Legend

Table 4-2485. RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED14	RW	0h	Reserved.Reads return 0 and writes have no effect
18	CLEAROVL1INT	RW	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
17	CLEAROVL0INT	RW	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
16	CLEARTBINT	RW	0h	CLEARTBINT: CLEAR Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
15 - 12	RESERVED13	RW	0h	Reserved.Reads return 0 and writes have no effect
11	CLEARDMA3	RW	0h	CLEARDMA3: CLEAR Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
10	CLEARDMA2	RW	0h	CLEARDMA2: CLEAR Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
9	CLEARDMA1	RW	0h	CLEARDMA1: CLEAR Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
8	CLEARDMA0	RW	0h	CLEARDMA0: CLEAR Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request

Table 4-2485. RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 4	RESERVED12	RW	0h	Reserved.Reads return 0 and writes have no effect
3	CLEARINT3	RW	0h	CLEARINT3: CLEAR Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
2	CLEARINT2	RW	0h	CLEARINT2: CLEAR Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
1	CLEARINT1	RW	0h	CLEARINT1: CLEAR Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
0	CLEARINT0	RW	0h	CLEARINT0: CLEAR Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt

4.21.27 HSM_RTI0_RTIINTFLAG Register (Offset = 88h) [reset = h]

Short Description: Interrupt Flags interrupt pending bits

Long Description:

Return to Summary Table

Table 4-2486. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C88h

Figure 4-1195. HSM_RTI0_RTIINTFLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED16													OVL1INT	OVL0INT	TBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED15												INT3	INT2	INT1	INT0
RW												RW	RW	RW	RW
0												0	0	0	0

Access Types Legend

Table 4-2487. RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED16	RW	0h	Reserved.Reads return 0 and writes have no effect
18	OVL1INT	RW	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
17	OVL0INT	RW	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
16	TBINT	RW	0h	User and privilege mode (read):this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software.determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
15 - 4	RESERVED15	RW	0h	Reserved.Reads return 0 and writes have no effect
3	INT3	RW	0h	INT3: Interrupt Flag 3.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
2	INT2	RW	0h	INT2: Interrupt Flag 2.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
1	INT1	RW	0h	INT1: Interrupt Flag 1.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
0	INT0	RW	0h	INT0: Interrupt Flag 0.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0

4.21.28 HSM_RTI0_RTIDWDCTRL Register (Offset = 90h) [reset = h]

Short Description: Digital Watchdog Control Enables the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2488. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C90h

Figure 4-1196. HSM_RTI0_RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DWDCTRL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCTRL															
RW															
0															

Access Types Legend

Table 4-2489. RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DWDCTRL	RW	0h	DWDCTRL: Digital Watchdog Control.User and priviledge mode (read):0x5312ACED = DWD counter is disabled. This is the default value.0xA98559DA = DWD counter is enabledAny other value = DWD counter state is unchanged (enabled or disabled)Priviledge mode (write):0xA98559DA = DWD counter is enabledAny other value = State of DWD counter is unchanged (stays enabled or disabled)Note: One-Write Functionality of DWDCTRL RegisterThe RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

4.21.29 HSM_RTI0_RTIDWDPRLD Register (Offset = 94h) [reset = h]

Short Description: Digital Watchdog Preload sets the experation time of the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2490. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C94h

Figure 4-1197. HSM_RTI0_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED17															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED17				DWDPRLD											
RW				RW											
0				0											

Access Types Legend

Table 4-2491. RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED17	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 0	DWDPRLD	RW	0h	DWDPRLD: Digital Watchdog Preload Value.User and priviledge mode (read):A read from this register in any CPU mode returns the current preload value.Priviledge mode (write):If the DWD is always enabled after reset is released:The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires.When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value.If the DWD is implemented such that the down counter is enabled by software:The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.The expiration time of the DWD Down Counter can be determined with following equation:texp = (RTIDWDPRLD+1) x 2 ^ 13 / RTICLK1where: RTIDWDPRLD = 0...4095

4.21.30 HSM_RTI0_RTIWDSTATUS Register (Offset = 98h) [reset = h]

Short Description: Watchdog Status reflects the status of Analog and Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2492. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C98h

Figure 4-1198. HSM_RTI0_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED18										DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
RW										RW	RW	RW	RW	RW	RW
0										0	0	0	0	0	0

Access Types Legend

Table 4-2493. RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED18	RW	0h	Reserved.Reads return 0 and writes have no effect
5	DWWD_ST	RW	0h	DWWD ST: Windowed Watchdog Status.This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.User and priviledge mode (read):0 = no time-window violation has occurred.1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.
4	ENDTIMEVIOL	RW	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status.This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.User and priviledge mode (read):0 = no end-time window violation has occurred.1 = the end-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
3	STARTTIMEVIOL	RW	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.User and priviledge mode (read):0 = no start-time window violation has occurred.1 = the start-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
2	KEYST	RW	0h	KEYST: Watchdog KeyStatus.This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register.User and priviledge mode (read):0 = no wrong key or key-sequence written1 = wrong key or key-sequence written to RTIWDKEY registerPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

Table 4-2493. RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DWDST	RW	0h	DWDST: Digital Watchdog Status.This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons.User and priviledge mode (read):0 = DWD timeout period not expired1 = DWD timeout period has expiredPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0
0	AWDST	RW	0h	AWDST: Analog Watchdog Status.User and priviledge mode (read):0 = AWD pin 0 ?> 1 threshold not exceeded1 = AWD pin 0 ?> 1 threshold exceededPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

4.21.31 HSM_RTI0_RTIWDKEY Register (Offset = 9Ch) [reset = h]

Short Description: Watchdog Key correct written key values discharge the external capacitor

Long Description:

Return to Summary Table

Table 4-2494. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8C9Ch

Figure 4-1199. HSM_RTI0_RTIWDKEY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED19															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDKEY															
RW															
0															

Access Types Legend

Table 4-2495. RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED19	RW	0h	Reserved.Reads return 0 and writes have no effect
15 - 0	WDKEY	RW	0h	WDKEY: Watchdog Key.User and privilege mode reads are indeterminate.Privilege mode (write):A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1?s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3.Note: Register write access time precautionThe user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

4.21.32 HSM_RTI0_RTIDWDCNTR Register (Offset = A0h) [reset = h]

Short Description: Digital Watchdog Down Counter current value of DWD down counter

Long Description:

Return to Summary Table

Table 4-2496. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CA0h

Figure 4-1200. HSM_RTI0_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED20							DWDCNTR								
RW							RW								
0							0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCNTR															
RW															
0															

Access Types Legend

Table 4-2497. RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED20	RW	0h	Reserved.Reads return 0 and writes have no effect
24 - 0	DWDCNTR	RW	0h	DWDCNTR: Digital Watchdog Down Counter.The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second.User and privilege mode (read):Reads return the current counter value.Privilege mode (write):Writes don?t have an effect.

4.21.33 HSM_RTI0_RTIWWDRXNCTRL Register (Offset = A4h) [reset = h]

Short Description: Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset

Long Description:

Return to Summary Table

Table 4-2498. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CA4h

Figure 4-1201. HSM_RTI0_RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED21															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED21												WWDRXN			
RW												RW			
0												0			

Access Types Legend

Table 4-2499. RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RESERVED21	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	WWDRXN	RW	0h	WWDRXN: Digital Windowed Watchdog Reaction.User and privilege mode (read), privileged mode (write):0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Note: Configuration of DWWD ReactionThe DWWD reaction can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

4.21.34 HSM_RTI0_RTIWWDSIZECTRL Register (Offset = A8h) [reset = h]

Short Description: Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog

Long Description:

Return to Summary Table

Table 4-2500. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CA8h

Figure 4-1202. HSM_RTI0_RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WWDSIZE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WWDSIZE															
RW															
0															

Access Types Legend

Table 4-2501. RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	WWDSIZE	RW	0h	WWDSIZE: Digital Windowed Watchdog Window Size.User and privilege mode (read), privileged mode (write):Value written to WWDSIZE Window Size0x00000005 100% (Functionality same as the time-out digital watchdog.)0x00000050 50%0x00000500 25%0x00005000 12.5%0x00050000 6.25%0x00500000 3.125%Any other value 3.125%Note: Incorrect value being written to watchdog window size control registerIf an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.Note: Configuration of DWWD Window SizeThe DWWD window size can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDSIZE is made when the watchdog service window is already open, then

4.21.35 HSM_RTI0_RTIINTCLRENABLE Register (Offset = ACh) [reset = h]

Short Description: RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts

Long Description:

Return to Summary Table

Table 4-2502. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CACh

Figure 4-1203. HSM_RTI0_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED25				INTCLRENABLE3				RESERVED24				INTCLRENABLE2			
RW				RW				RW				RW			
0				0				0				0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED23				INTCLRENABLE1				RESERVED22				INTCLRENABLE0			
RW				RW				RW				RW			
0				0				0				0			

Access Types Legend

Table 4-2503. RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	RESERVED25	RW	0h	Reserved.Reads return 0 and writes have no effect
27 - 24	INTCLRENABLE3	RW	0h	INTCLRENABLE3.Enables the auto-clear functionality on the compare 3 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 3 interrupt is disabled.Any other value = Auto-clear for compare 3 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 3 interrupt.Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23 - 20	RESERVED24	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	INTCLRENABLE2	RW	0h	INTCLRENABLE2.Enables the auto-clear functionality on the compare 2 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 2 interrupt is disabled.Any other value = Auto-clear for compare 2 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 2 interrupt.Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15 - 12	RESERVED23	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 8	INTCLRENABLE1	RW	0h	INTCLRENABLE1.Enables the auto-clear functionality on the compare 1 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 1 interrupt is disabled.Any other value = Auto-clear for compare 1 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 1 interrupt.Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7 - 4	RESERVED22	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	INTCLRENABLE0	RW	0h	INTCLRENABLE0.Enables the auto-clear functionality on the compare 0 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 0 interrupt is disabled.Any other value = Auto-clear for compare 0 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 0 interrupt.Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

4.21.36 HSM_RTI0_RTICOMP0CLR Register (Offset = B0h) [reset = h]

Short Description: Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line

Long Description:

Return to Summary Table

Table 4-2504. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CB0h

Figure 4-1204. HSM_RTI0_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0CLR															
RW															
0															

Access Types Legend

Table 4-2505. RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0CLR	RW	0h	COMP0CLR: Compare 0 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.37 HSM_RTI0_RTICOMP1CLR Register (Offset = B4h) [reset = h]

Short Description: Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line

Long Description:

Return to Summary Table

Table 4-2506. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CB4h

Figure 4-1205. HSM_RTI0_RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1CLR															
RW															
0															

Access Types Legend

Table 4-2507. RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1CLR	RW	0h	COMP1CLR: Compare 1 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.38 HSM_RTI0_RTICOMP2CLR Register (Offset = B8h) [reset = h]

Short Description: Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line

Long Description:

Return to Summary Table

Table 4-2508. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CB8h

Figure 4-1206. HSM_RTI0_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2CLR															
RW															
0															

Access Types Legend

Table 4-2509. RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2CLR	RW	0h	COMP2CLR: Compare 2 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.39 HSM_RTI0_RTICOMP3CLR Register (Offset = BCh) [reset = h]

Short Description: Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line

Long Description:

Return to Summary Table

Table 4-2510. Instance Table

Instance Name	Physical Address
HSM_RTI0	47F7 8CBCh

Figure 4-1207. HSM_RTI0_RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3CLR															
RW															
0															

Access Types Legend

Table 4-2511. RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3CLR	RW	0h	COMP3CLR: Compare 3 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.40 HSM_WDT0_RTIGCTRL Register (Offset = 0h) [reset = h]

Short Description: Global Control Register starts / stops the counters

Long Description:

Return to Summary Table

Table 4-2512. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D00h

Figure 4-1208. HSM_WDT0_RTIGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2												NTUSEL			
RW												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS	RESERVED1													CNT1EN	CNT0EN
RW	RW													RW	RW
0	0													0	0

Access Types Legend

Table 4-2513. RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED2	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	NTUSEL	RW	0h	NTUSEL: Select NTU signal.These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL.User and privilege mode (read):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0? Privilege mode (write):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0?
15	COS	RW	0h	COS: Continue On Suspend.This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.User and privilege mode (read):0 = counters are stopped while in debug mode1 = counters are running while in debug modePrivilege mode (write):0 = stop counters in debug mode1 = continue counting in debug mode
14 - 2	RESERVED1	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CNT1EN	RW	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bit destination address (physical).
0	CNT0EN	RW	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bits source address (physical).

4.21.41 HSM_WDT0_RTITBCTRL Register (Offset = 4h) [reset = h]

Short Description: Timebase Control selection which source triggers free running counter 0

Long Description:

Return to Summary Table

Table 4-2514. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D04h

Figure 4-1209. HSM_WDT0_RTITBCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED3														INC	TBEXT
RW														RW	RW
0														0	0

Access Types Legend

Table 4-2515. RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED3	RW	0h	Reserved
1	INC	RW	0h	INC: Increment Free Running Counter 0.This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.User and privilege mode (read):0 = FRC0 will not be incremented1 = FRC0 will be incrementedPrivilege mode (write):0 = Do not increment FRC0 on failing external clock1 = Increment FRC0 on failing external clock
0	TBEXT	RW	0h	TBEXT: Timebase External.The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx.When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset.The selection if the external signal should be used, can only be done by software.User and privilege mode (read):0 = UC0 clocks FRC01 = NTUx clocks FRC0Privilege mode (write):0 = MUX is switched to internal UC0 clocking scheme1 = MUX is switched to external NTUx clocking scheme

4.21.42 HSM_WDT0_RTICAPCTRL Register (Offset = 8h) [reset = h]

Short Description: Capture Control controls the capture source for the counters

Long Description:

Return to Summary Table

Table 4-2516. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D08h

Figure 4-1210. HSM_WDT0_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED4															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED4														CAPCNTR1	CAPCNTR0
RW														RW	RW
0														0	0

Access Types Legend

Table 4-2517. RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED4	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CAPCNTR1	RW	0h	CAPCNTR1: Capture Counter 1.This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 1
0	CAPCNTR0	RW	0h	CAPCNTR0: Capture Counter 0.This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 111 indexed10 reserved01 post-increment00 constant

4.21.43 HSM_WDT0_RTICOMPCTRL Register (Offset = Ch) [reset = h]

Short Description: Compare Control controls the source for the compare registers

Long Description:

Return to Summary Table

Table 4-2518. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D0Ch

Figure 4-1211. HSM_WDT0_RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED8															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED8			COMP 3SEL	RESERVED7			COMP 2SEL	RESERVED6			COMP 1SEL	RESERVED5			COMP 0SEL
RW			RW	RW			RW	RW			RW	RW			RW
0			0	0			0	0			0	0			0

Access Types Legend

Table 4-2519. RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RESERVED8	RW	0h	Reserved.Reads return 0 and writes have no effect
12	COMP3SEL	RW	0h	COMPSEL3: Compare Select 3.This bit determines the counter with which the compare value hold in compare register 3 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
11 - 9	RESERVED7	RW	0h	Reserved.Reads return 0 and writes have no effect
8	COMP2SEL	RW	0h	COMPSEL2: Compare Select 2.This bit determines the counter with which the compare value hold in compare register 2 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
7 - 5	RESERVED6	RW	0h	Reserved.Reads return 0 and writes have no effect
4	COMP1SEL	RW	0h	COMPSEL1: Compare Select 1.This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
3 - 1	RESERVED5	RW	0h	Reserved.Reads return 0 and writes have no effect
0	COMP0SEL	RW	0h	COMPSEL0: Compare Select 0.This bit determines the counter with which the compare value hold in compare register 0 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1

4.21.44 HSM_WDT0_RTIFRC0 Register (Offset = 10h) [reset = h]

Short Description: Free Running Counter 0 current value of free running counter 0

Long Description:

Return to Summary Table

Table 4-2520. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D10h

Figure 4-1212. HSM_WDT0_RTIFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC0															
RW															
0															

Access Types Legend

Table 4-2521. RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC0	RW	0h	FRC0: Free Running Counter 0.This registers holds the current value of the Free Running Counter 0 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

4.21.45 HSM_WDT0_RTIUC0 Register (Offset = 14h) [reset = h]

Short Description: Up Counter 0 current value of prescale counter 0

Long Description:

Return to Summary Table

Table 4-2522. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D14h

Figure 4-1213. HSM_WDT0_RTIUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC0															
RW															
0															

Access Types Legend

Table 4-2523. RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC0	RW	0h	UC0: Up Counter 0.This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.User and privilege mode (read):value of the counter when the Free Running Counter 0 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

4.21.46 HSM_WDT0_RTICPUC0 Register (Offset = 18h) [reset = h]

Short Description: Compare Up Counter 0 compare value compared with prescale counter 0

Long Description:

Return to Summary Table

Table 4-2524. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D18h

Figure 4-1214. HSM_WDT0_RTICPUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC0															
RW															
0															

Access Types Legend

Table 4-2525. RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC0	RW	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock.If CPUC0 = 0: then, frequency = RTICLK/ (2^32)If CPUC0 ? 0: then , frequency = RTICLK/(CPUC0 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

4.21.47 HSM_WDT0_RTICAFRC0 Register (Offset = 20h) [reset = h]

Short Description: Capture Free Running Counter 0 current value of free running counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2526. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D20h

Figure 4-1215. HSM_WDT0_RTICAFRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC0															
RW															
0															

Access Types Legend

Table 4-2527. RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC0	RW	0h	CAFRC0: Capture Free Running Counter 0.This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 0 on a capture event

4.21.48 HSM_WDT0_RTICAUC0 Register (Offset = 24h) [reset = h]

Short Description: Capture Up Counter 0 current value of prescale counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2528. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D24h

Figure 4-1216. HSM_WDT0_RTICAUC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC0															
RW															
0															

Access Types Legend

Table 4-2529. RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC0	RW	0h	CAUC0: Capture Up Counter 0.This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 0 on a capture event

4.21.49 HSM_WDT0_RTIFRC1 Register (Offset = 30h) [reset = h]

Short Description: Free Running Counter 1 current value of free running counter 1

Long Description:

Return to Summary Table

Table 4-2530. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D30h

Figure 4-1217. HSM_WDT0_RTIFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRC1															
RW															
0															

Access Types Legend

Table 4-2531. RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC1	RW	0h	FRC1: Free Running Counter 1.This registers holds the current value of the Free Running Counter 1 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

4.21.50 HSM_WDT0_RTIUC1 Register (Offset = 34h) [reset = h]

Short Description: Up Counter 1 current value of prescale counter 1

Long Description:

Return to Summary Table

Table 4-2532. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D34h

Figure 4-1218. HSM_WDT0_RTIUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC1															
RW															
0															

Access Types Legend

Table 4-2533. RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC1	RW	0h	UC1: Up Counter 1.This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.User and privilege mode (read):value of the counter when the Free Running Counter 1 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

4.21.51 HSM_WDT0_RTICPUC1 Register (Offset = 38h) [reset = h]

Short Description: Compare Up Counter 1 compare value compared with prescale counter 1

Long Description:

Return to Summary Table

Table 4-2534. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D38h

Figure 4-1219. HSM_WDT0_RTICPUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPUC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUC1															
RW															
0															

Access Types Legend

Table 4-2535. RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC1	RW	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock.If CPUC1 = 0: then, frequency = RTICLK/ (2^32)If CPUC1 ? 0: then , frequency = RTICLK/(CPUC1 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

4.21.52 HSM_WDT0_RTICAFRC1 Register (Offset = 40h) [reset = h]

Short Description: Capture Free Running Counter 1 current value of free running counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2536. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D40h

Figure 4-1220. HSM_WDT0_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAFRC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAFRC1															
RW															
0															

Access Types Legend

Table 4-2537. RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC1	RW	0h	CAFRC1: Capture Free Running Counter 1.This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 1 on a capture event

4.21.53 HSM_WDT0_RTICAUC1 Register (Offset = 44h) [reset = h]

Short Description: Capture Up Counter 1 current value of prescale counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2538. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D44h

Figure 4-1221. HSM_WDT0_RTICAUC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAUC1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAUC1															
RW															
0															

Access Types Legend

Table 4-2539. RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC1	RW	0h	CAUC1: Capture Up Counter 1.This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 1 on a capture event

4.21.54 HSM_WDT0_RTICOMP0 Register (Offset = 50h) [reset = h]

Short Description: Compare 0 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2540. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D50h

Figure 4-1222. HSM_WDT0_RTICOMP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0															
RW															
0															

Access Types Legend

Table 4-2541. RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0	RW	0h	COMP0: Compare 0.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.55 HSM_WDT0_RTIUDCP0 Register (Offset = 54h) [reset = h]

Short Description: Update Compare 0 value to be added to the compare register 0 value on compare match

Long Description:

Return to Summary Table

Table 4-2542. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D54h

Figure 4-1223. HSM_WDT0_RTIUDCP0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP0															
RW															
0															

Access Types Legend

Table 4-2543. RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP0	RW	0h	UDCP0: Update Compare 0 Register.This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 0 register on the next compare matchPrivilege mode (write):new update value

4.21.56 HSM_WDT0_RTICOMP1 Register (Offset = 58h) [reset = h]

Short Description: Compare 1 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2544. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D58h

Figure 4-1224. HSM_WDT0_RTICOMP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1															
RW															
0															

Access Types Legend

Table 4-2545. RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1	RW	0h	COMP1: compare1.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.57 HSM_WDT0_RTIUDCP1 Register (Offset = 5Ch) [reset = h]

Short Description: Update Compare 1 value to be added to the compare register 1 value on compare match

Long Description:

Return to Summary Table

Table 4-2546. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D5Ch

Figure 4-1225. HSM_WDT0_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP1															
RW															
0															

Access Types Legend

Table 4-2547. RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP1	RW	0h	UDCP1: Update compare1 Register.This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare1 register on the next compare matchPrivilege mode (write):new update value

4.21.58 HSM_WDT0_RTICOMP2 Register (Offset = 60h) [reset = h]

Short Description: Compare 2 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2548. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D60h

Figure 4-1226. HSM_WDT0_RTICOMP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2															
RW															
0															

Access Types Legend

Table 4-2549. RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2	RW	0h	COMP2: compare 2.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.59 HSM_WDT0_RTIUDCP2 Register (Offset = 64h) [reset = h]

Short Description: Update Compare 2 value to be added to the compare register 2 value on compare match

Long Description:

Return to Summary Table

Table 4-2550. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D64h

Figure 4-1227. HSM_WDT0_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP2															
RW															
0															

Access Types Legend

Table 4-2551. RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP2	RW	0h	UDCP2: Update compare 2 Register.This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 2 register on the next compare matchPrivilege mode (write):new update value

4.21.60 HSM_WDT0_RTICOMP3 Register (Offset = 68h) [reset = h]

Short Description: Compare 3 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2552. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D68h

Figure 4-1228. HSM_WDT0_RTICOMP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3															
RW															
0															

Access Types Legend

Table 4-2553. RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3	RW	0h	COMP3: compare 3.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.61 HSM_WDT0_RTIUDCP3 Register (Offset = 6Ch) [reset = h]

Short Description: Update Compare 3 value to be added to the compare register 3 value on compare match

Long Description:

Return to Summary Table

Table 4-2554. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D6Ch

Figure 4-1229. HSM_WDT0_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDCP3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UDCP3															
RW															
0															

Access Types Legend

Table 4-2555. RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP3	RW	0h	UDCP3: Update compare 3 Register.This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 3 register on the next compare matchPrivilege mode (write):new update value

4.21.62 HSM_WDT0_RTITBLCOMP Register (Offset = 70h) [reset = h]

Short Description: Timebase Low Compare compare value to activate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2556. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D70h

Figure 4-1230. HSM_WDT0_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBLCOMP															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLCOMP															
RW															
0															

Access Types Legend

Table 4-2557. RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBLCOMP	RW	0h	TBLCOMP: Timebase Low Compare Value.This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0.User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

4.21.63 HSM_WDT0_RTITBHCOMP Register (Offset = 74h) [reset = h]

Short Description: Timebase High Compare compare value to deactivate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2558. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D74h

Figure 4-1231. HSM_WDT0_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBHCOMP															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBHCOMP															
RW															
0															

Access Types Legend

Table 4-2559. RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBHCOMP	RW	0h	TBHCOMP: Timebase High Compare Value.This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0.RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached.Example:The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0.RTICPUC0 = 0x00000050RTITBLCOMP = 0x000046RTITBHCOMP = 0x00000009User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

4.21.64 HSM_WDT0_RTISETINT Register (Offset = 80h) [reset = h]

Short Description: Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2560. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D80h

Figure 4-1232. HSM_WDT0_RTISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED11													SETOVL1INT	SETOVL0INT	SETTBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0	RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
RW				RW	RW	RW	RW	RW				RW	RW	RW	RW
0				0	0	0	0	0				0	0	0	0

Access Types Legend

Table 4-2561. RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED11	RW	0h	Reserved.Reads return 0 and writes have no effect
18	SETOVL1INT	RW	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
17	SETOVL0INT	RW	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
16	SETTBINT	RW	0h	SETTBINT: Set Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
15 - 12	RESERVED10	RW	0h	Reserved.Reads return 0 and writes have no effect
11	SETDMA3	RW	0h	SETDMA3: Set Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
10	SETDMA2	RW	0h	SETDMA2: Set Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
9	SETDMA1	RW	0h	SETDMA1: Set Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
8	SETDMA0	RW	0h	SETDMA0: Set Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
7 - 4	RESERVED9	RW	0h	Reserved.Reads return 0 and writes have no effect

Table 4-2561. RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SETINT3	RW	0h	SETINT3: Set Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged
2	SETINT2	RW	0h	SETINT2: Set Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
1	SETINT1	RW	0h	SETINT1: Set Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
0	SETINT0	RW	0h	SETINT0: Set Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt

4.21.65 HSM_WDT0_RTICLEARINT Register (Offset = 84h) [reset = h]

Short Description: Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2562. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D84h

Figure 4-1233. HSM_WDT0_RTICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED14													CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0	RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
RW				RW	RW	RW	RW	RW				RW	RW	RW	RW
0				0	0	0	0	0				0	0	0	0

Access Types Legend

Table 4-2563. RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED14	RW	0h	Reserved.Reads return 0 and writes have no effect
18	CLEAROVL1INT	RW	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
17	CLEAROVL0INT	RW	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
16	CLEARTBINT	RW	0h	CLEARTBINT: CLEAR Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
15 - 12	RESERVED13	RW	0h	Reserved.Reads return 0 and writes have no effect
11	CLEARDMA3	RW	0h	CLEARDMA3: CLEAR Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
10	CLEARDMA2	RW	0h	CLEARDMA2: CLEAR Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
9	CLEARDMA1	RW	0h	CLEARDMA1: CLEAR Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
8	CLEARDMA0	RW	0h	CLEARDMA0: CLEAR Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request

Table 4-2563. RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 4	RESERVED12	RW	0h	Reserved.Reads return 0 and writes have no effect
3	CLEARINT3	RW	0h	CLEARINT3: CLEAR Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
2	CLEARINT2	RW	0h	CLEARINT2: CLEAR Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
1	CLEARINT1	RW	0h	CLEARINT1: CLEAR Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
0	CLEARINT0	RW	0h	CLEARINT0: CLEAR Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt

4.21.66 HSM_WDT0_RTIINTFLAG Register (Offset = 88h) [reset = h]

Short Description: Interrupt Flags interrupt pending bits

Long Description:

Return to Summary Table

Table 4-2564. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D88h

Figure 4-1234. HSM_WDT0_RTIINTFLAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED16													OVL1INT	OVL0INT	TBINT
RW													RW	RW	RW
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED15												INT3	INT2	INT1	INT0
RW												RW	RW	RW	RW
0												0	0	0	0

Access Types Legend

Table 4-2565. RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED16	RW	0h	Reserved.Reads return 0 and writes have no effect
18	OVL1INT	RW	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
17	OVL0INT	RW	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
16	TBINT	RW	0h	User and privilege mode (read):this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software.determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
15 - 4	RESERVED15	RW	0h	Reserved.Reads return 0 and writes have no effect
3	INT3	RW	0h	INT3: Interrupt Flag 3.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
2	INT2	RW	0h	INT2: Interrupt Flag 2.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
1	INT1	RW	0h	INT1: Interrupt Flag 1.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
0	INT0	RW	0h	INT0: Interrupt Flag 0.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0

4.21.67 HSM_WDT0_RTIDWDCTRL Register (Offset = 90h) [reset = h]

Short Description: Digital Watchdog Control Enables the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2566. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D90h

Figure 4-1235. HSM_WDT0_RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DWDCTRL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCTRL															
RW															
0															

Access Types Legend

Table 4-2567. RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DWDCTRL	RW	0h	DWDCTRL: Digital Watchdog Control.User and priviledge mode (read):0x5312ACED = DWD counter is disabled. This is the default value.0xA98559DA = DWD counter is enabledAny other value = DWD counter state is unchanged (enabled or disabled)Priviledge mode (write):0xA98559DA = DWD counter is enabledAny other value = State of DWD counter is unchanged (stays enabled or disabled)Note: One-Write Functionality of DWDCTRL RegisterThe RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

4.21.68 HSM_WDT0_RTIDWDPRLD Register (Offset = 94h) [reset = h]

Short Description: Digital Watchdog Preload sets the experation time of the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2568. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D94h

Figure 4-1236. HSM_WDT0_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED17															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED17				DWDPRLD											
RW				RW											
0				0											

Access Types Legend

Table 4-2569. RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED17	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 0	DWDPRLD	RW	0h	DWDPRLD: Digital Watchdog Preload Value.User and priviledge mode (read):A read from this register in any CPU mode returns the current preload value.Priviledge mode (write):If the DWD is always enabled after reset is released:The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires.When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value.If the DWD is implemented such that the down counter is enabled by software:The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.The expiration time of the DWD Down Counter can be determined with following equation:texp = (RTIDWDPRLD+1) x 2 ^ 13 / RTICLK1where: RTIDWDPRLD = 0...4095

4.21.69 HSM_WDT0_RTIWDSTATUS Register (Offset = 98h) [reset = h]

Short Description: Watchdog Status reflects the status of Analog and Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2570. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D98h

Figure 4-1237. HSM_WDT0_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED18										DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
RW										RW	RW	RW	RW	RW	RW
0										0	0	0	0	0	0

Access Types Legend

Table 4-2571. RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED18	RW	0h	Reserved.Reads return 0 and writes have no effect
5	DWWD_ST	RW	0h	DWWD ST: Windowed Watchdog Status.This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.User and priviledge mode (read):0 = no time-window violation has occurred.1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.
4	ENDTIMEVIOL	RW	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status.This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.User and priviledge mode (read):0 = no end-time window violation has occurred.1 = the end-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
3	STARTTIMEVIOL	RW	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.User and priviledge mode (read):0 = no start-time window violation has occurred.1 = the start-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
2	KEYST	RW	0h	KEYST: Watchdog KeyStatus.This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register.User and priviledge mode (read):0 = no wrong key or key-sequence written1 = wrong key or key-sequence written to RTIWDKEY registerPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

Table 4-2571. RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DWDST	RW	0h	DWDST: Digital Watchdog Status.This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons.User and priviledge mode (read):0 = DWD timeout period not expired1 = DWD timeout period has expiredPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0
0	AWDST	RW	0h	AWDST: Analog Watchdog Status.User and priviledge mode (read):0 = AWD pin 0 ?> 1 threshold not exceeded1 = AWD pin 0 ?> 1 threshold exceededPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

4.21.70 HSM_WDT0_RTIWDKEY Register (Offset = 9Ch) [reset = h]

Short Description: Watchdog Key correct written key values discharge the external capacitor

Long Description:

Return to Summary Table

Table 4-2572. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8D9Ch

Figure 4-1238. HSM_WDT0_RTIWDKEY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED19															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDKEY															
RW															
0															

Access Types Legend

Table 4-2573. RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED19	RW	0h	Reserved.Reads return 0 and writes have no effect
15 - 0	WDKEY	RW	0h	WDKEY: Watchdog Key.User and privilege mode reads are indeterminate.Privilege mode (write):A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1?s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3.Note: Register write access time precautionThe user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

4.21.71 HSM_WDT0_RTIDWDCNTR Register (Offset = A0h) [reset = h]

Short Description: Digital Watchdog Down Counter current value of DWD down counter

Long Description:

Return to Summary Table

Table 4-2574. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DA0h

Figure 4-1239. HSM_WDT0_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED20							DWDCNTR								
RW							RW								
0							0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWDCNTR															
RW															
0															

Access Types Legend

Table 4-2575. RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED20	RW	0h	Reserved.Reads return 0 and writes have no effect
24 - 0	DWDCNTR	RW	0h	DWDCNTR: Digital Watchdog Down Counter.The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second.User and privilege mode (read):Reads return the current counter value.Privilege mode (write):Writes don?t have an effect.

4.21.72 HSM_WDT0_RTIWWDRXNCTRL Register (Offset = A4h) [reset = h]

Short Description: Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset

Long Description:

Return to Summary Table

Table 4-2576. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DA4h

Figure 4-1240. HSM_WDT0_RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED21															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED21												WWDRXN			
RW												RW			
0												0			

Access Types Legend

Table 4-2577. RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RESERVED21	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	WWDRXN	RW	0h	WWDRXN: Digital Windowed Watchdog Reaction.User and privilege mode (read), privileged mode (write):0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Note: Configuration of DWWD ReactionThe DWWD reaction can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

4.21.73 HSM_WDT0_RTIWWDSIZECTRL Register (Offset = A8h) [reset = h]

Short Description: Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog

Long Description:

Return to Summary Table

Table 4-2578. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DA8h

Figure 4-1241. HSM_WDT0_RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WWDSIZE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WWDSIZE															
RW															
0															

Access Types Legend

Table 4-2579. RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	WWDSIZE	RW	0h	WWDSIZE: Digital Windowed Watchdog Window Size.User and privilege mode (read), privileged mode (write):Value written to WWDSIZE Window Size0x00000005 100% (Functionality same as the time-out digital watchdog.)0x00000050 50%0x00000500 25%0x00005000 12.5%0x00050000 6.25%0x00500000 3.125%Any other value 3.125%Note: Incorrect value being written to watchdog window size control registerIf an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.Note: Configuration of DWWD Window SizeThe DWWD window size can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDSIZE is made when the watchdog service window is already open, then

4.21.74 HSM_WDT0_RTIINTCLRENABLE Register (Offset = ACh) [reset = h]

Short Description: RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts

Long Description:

Return to Summary Table

Table 4-2580. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DACh

Figure 4-1242. HSM_WDT0_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED25				INTCLRENABLE3				RESERVED24				INTCLRENABLE2			
RW				RW				RW				RW			
0				0				0				0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED23				INTCLRENABLE1				RESERVED22				INTCLRENABLE0			
RW				RW				RW				RW			
0				0				0				0			

Access Types Legend

Table 4-2581. RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	RESERVED25	RW	0h	Reserved.Reads return 0 and writes have no effect
27 - 24	INTCLRENABLE3	RW	0h	INTCLRENABLE3.Enables the auto-clear functionality on the compare 3 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 3 interrupt is disabled.Any other value = Auto-clear for compare 3 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 3 interrupt.Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23 - 20	RESERVED24	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	INTCLRENABLE2	RW	0h	INTCLRENABLE2.Enables the auto-clear functionality on the compare 2 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 2 interrupt is disabled.Any other value = Auto-clear for compare 2 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 2 interrupt.Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15 - 12	RESERVED23	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 8	INTCLRENABLE1	RW	0h	INTCLRENABLE1.Enables the auto-clear functionality on the compare 1 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 1 interrupt is disabled.Any other value = Auto-clear for compare 1 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 1 interrupt.Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7 - 4	RESERVED22	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	INTCLRENABLE0	RW	0h	INTCLRENABLE0.Enables the auto-clear functionality on the compare 0 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 0 interrupt is disabled.Any other value = Auto-clear for compare 0 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 0 interrupt.Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

4.21.75 HSM_WDT0_RTICOMP0CLR Register (Offset = B0h) [reset = h]

Short Description: Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line

Long Description:

Return to Summary Table

Table 4-2582. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DB0h

Figure 4-1243. HSM_WDT0_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP0CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP0CLR															
RW															
0															

Access Types Legend

Table 4-2583. RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0CLR	RW	0h	COMP0CLR: Compare 0 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.76 HSM_WDT0_RTICOMP1CLR Register (Offset = B4h) [reset = h]

Short Description: Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line

Long Description:

Return to Summary Table

Table 4-2584. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DB4h

Figure 4-1244. HSM_WDT0_RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP1CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP1CLR															
RW															
0															

Access Types Legend

Table 4-2585. RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1CLR	RW	0h	COMP1CLR: Compare 1 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.77 HSM_WDT0_RTICOMP2CLR Register (Offset = B8h) [reset = h]

Short Description: Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line

Long Description:

Return to Summary Table

Table 4-2586. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DB8h

Figure 4-1245. HSM_WDT0_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP2CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP2CLR															
RW															
0															

Access Types Legend

Table 4-2587. RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2CLR	RW	0h	COMP2CLR: Compare 2 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.21.78 HSM_WDT0_RTICOMP3CLR Register (Offset = BCh) [reset = h]

Short Description: Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line

Long Description:

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Table 4-2588. Instance Table

Instance Name	Physical Address
HSM_WDT0	47F7 8DBCh

Figure 4-1246. HSM_WDT0_RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP3CLR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP3CLR															
RW															
0															

Access Types Legend

Table 4-2589. RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3CLR	RW	0h	COMP3CLR: Compare 3 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

Table 4-2590. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.22 MSS_SPI Registers

Table 4-2591. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4

Offset	Length	Acronym	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	MCSPI0_HL_REV	IP Revision Identifier (X.Y.R)Used by software to track features, bugs, and compatibility	5220 0000h	5220 1000h	5220 2000h
4h	32	MCSPI0_HL_HWINFO	Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any).Actual field format and encoding is up to the module's designer to decide.	5220 0004h	5220 1004h	5220 2004h
10h	32	MCSPI0_HL_SYSCONFIG	Clock management configuration	5220 0010h	5220 1010h	5220 2010h
100h	32	MCSPI0_REVISION	This register contains the hard coded RTL revision number.	5220 0100h	5220 1100h	5220 2100h
110h	32	MCSPI0_SYSCONFIG	This register allows controlling various parameters of the OCP interface.	5220 0110h	5220 1110h	5220 2110h
114h	32	MCSPI0_SYSSTATUS	This register provides status information about the module excluding the interrupt status information	5220 0114h	5220 1114h	5220 2114h
118h	32	MCSPI0_IRQSTATUS	The interrupt status regroups all the status of the module internal events that can generate an interrupt	5220 0118h	5220 1118h	5220 2118h
11Ch	32	MCSPI0_IRQENABLE	This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.	5220 011Ch	5220 111Ch	5220 211Ch
120h	32	MCSPI0_WAKEUPENABLE	The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.	5220 0120h	5220 1120h	5220 2120h

Table 4-2591. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
124h	32	MCSPI0_SYST	This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.	5220 0124h	5220 1124h	5220 2124h
128h	32	MCSPI0_MODULCTRL	This register is dedicated to the configuration of the serial port interface.	5220 0128h	5220 1128h	5220 2128h
12Ch	32	MCSPI0_CH0CONF	This register is dedicated to the configuration of the channel 0	5220 012Ch	5220 112Ch	5220 212Ch
130h	32	MCSPI0_CH0STAT	This register provides status information about transmitter and receiver registers of channel 0	5220 0130h	5220 1130h	5220 2130h
134h	32	MCSPI0_CH0CTRL	This register is dedicated to enable the channel 0	5220 0134h	5220 1134h	5220 2134h
138h	32	MCSPI0_TX0	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 0138h	5220 1138h	5220 2138h
13Ch	32	MCSPI0_RX0	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 013Ch	5220 113Ch	5220 213Ch
140h	32	MCSPI0_CH1CONF	This register is dedicated to the configuration of the channel.	5220 0140h	5220 1140h	5220 2140h
144h	32	MCSPI0_CH1STAT	This register provides status information about transmitter and receiver registers of channel 1	5220 0144h	5220 1144h	5220 2144h
148h	32	MCSPI0_CH1CTRL	This register is dedicated to enable the channel 1	5220 0148h	5220 1148h	5220 2148h
14Ch	32	MCSPI0_TX1	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 014Ch	5220 114Ch	5220 214Ch
150h	32	MCSPI0_RX1	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 0150h	5220 1150h	5220 2150h

Table 4-2591. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
154h	32	MCSPI0_CH2CONF	This register is dedicated to the configuration of the channel 2	5220 0154h	5220 1154h	5220 2154h
158h	32	MCSPI0_CH2STAT	This register provides status information about transmitter and receiver registers of channel 2	5220 0158h	5220 1158h	5220 2158h
15Ch	32	MCSPI0_CH2CTRL	This register is dedicated to enable the channel 2	5220 015Ch	5220 115Ch	5220 215Ch
160h	32	MCSPI0_TX2	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 0160h	5220 1160h	5220 2160h
164h	32	MCSPI0_RX2	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 0164h	5220 1164h	5220 2164h
168h	32	MCSPI0_CH3CONF	This register is dedicated to the configuration of the channel 3	5220 0168h	5220 1168h	5220 2168h
16Ch	32	MCSPI0_CH3STAT	This register provides status information about transmitter and receiver registers of channel 3	5220 016Ch	5220 116Ch	5220 216Ch
170h	32	MCSPI0_CH3CTRL	This register is dedicated to enable the channel 3	5220 0170h	5220 1170h	5220 2170h
174h	32	MCSPI0_TX3	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 0174h	5220 1174h	5220 2174h
178h	32	MCSPI0_RX3	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 0178h	5220 1178h	5220 2178h
17Ch	32	MCSPI0_XFERLEVEL	This register provides transfer levels needed while using FIFO buffer during transfer.	5220 017Ch	5220 117Ch	5220 217Ch
180h	32	MCSPI0_DAFTX	This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.	5220 0180h	5220 1180h	5220 2180h

Table 4-2591. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
1A0h	32	MCSPI0_DAFRX	This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.	5220 01A0h	5220 11A0h	5220 21A0h

Table 4-2592. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4

Offset	Length	Acronym	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
0h	32	MCSPI0_HL_REV	IP Revision Identifier (X.Y.R)Used by software to track features, bugs, and compatibility	5220 3000h	5220 4000h
4h	32	MCSPI0_HL_HWINFO	Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any).Actual field format and encoding is up to the module's designer to decide.	5220 3004h	5220 4004h
10h	32	MCSPI0_HL_SYSCONFIG	Clock management configuration	5220 3010h	5220 4010h
100h	32	MCSPI0_REVISION	This register contains the hard coded RTL revision number.	5220 3100h	5220 4100h
110h	32	MCSPI0_SYSCONFIG	This register allows controlling various parameters of the OCP interface.	5220 3110h	5220 4110h
114h	32	MCSPI0_SYSSTATUS	This register provides status information about the module excluding the interrupt status information	5220 3114h	5220 4114h
118h	32	MCSPI0_IRQSTATUS	The interrupt status regroups all the status of the module internal events that can generate an interrupt	5220 3118h	5220 4118h
11Ch	32	MCSPI0_IRQENABLE	This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.	5220 311Ch	5220 411Ch
120h	32	MCSPI0_WAKEUPENABLE	The wakeup enable register allows to enable/ disable the module internal sources of wakeup on event-by-event basis.	5220 3120h	5220 4120h

Table 4-2592. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
124h	32	MCSPI0_SYST	This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.	5220 3124h	5220 4124h
128h	32	MCSPI0_MODULCTRL	This register is dedicated to the configuration of the serial port interface.	5220 3128h	5220 4128h
12Ch	32	MCSPI0_CH0CONF	This register is dedicated to the configuration of the channel 0	5220 312Ch	5220 412Ch
130h	32	MCSPI0_CH0STAT	This register provides status information about transmitter and receiver registers of channel 0	5220 3130h	5220 4130h
134h	32	MCSPI0_CH0CTRL	This register is dedicated to enable the channel 0	5220 3134h	5220 4134h
138h	32	MCSPI0_TX0	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 3138h	5220 4138h
13Ch	32	MCSPI0_RX0	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 313Ch	5220 413Ch
140h	32	MCSPI0_CH1CONF	This register is dedicated to the configuration of the channel.	5220 3140h	5220 4140h
144h	32	MCSPI0_CH1STAT	This register provides status information about transmitter and receiver registers of channel 1	5220 3144h	5220 4144h
148h	32	MCSPI0_CH1CTRL	This register is dedicated to enable the channel 1	5220 3148h	5220 4148h
14Ch	32	MCSPI0_TX1	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 314Ch	5220 414Ch
150h	32	MCSPI0_RX1	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 3150h	5220 4150h
154h	32	MCSPI0_CH2CONF	This register is dedicated to the configuration of the channel 2	5220 3154h	5220 4154h
158h	32	MCSPI0_CH2STAT	This register provides status information about transmitter and receiver registers of channel 2	5220 3158h	5220 4158h
15Ch	32	MCSPI0_CH2CTRL	This register is dedicated to enable the channel 2	5220 315Ch	5220 415Ch

Table 4-2592. MCSPI0, MCSPI0_MCSPI Registers, Base Address=5220 0000H, Length=4 (continued)

Offset	Length	Acronym	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address
160h	32	MCSPI0_TX2	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 3160h	5220 4160h
164h	32	MCSPI0_RX2	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 3164h	5220 4164h
168h	32	MCSPI0_CH3CONF	This register is dedicated to the configuration of the channel 3	5220 3168h	5220 4168h
16Ch	32	MCSPI0_CH3STAT	This register provides status information about transmitter and receiver registers of channel 3	5220 316Ch	5220 416Ch
170h	32	MCSPI0_CH3CTRL	This register is dedicated to enable the channel 3	5220 3170h	5220 4170h
174h	32	MCSPI0_TX3	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.	5220 3174h	5220 4174h
178h	32	MCSPI0_RX3	This register contains a single SPI word received through the serial link, what ever SPI word length is.	5220 3178h	5220 4178h
17Ch	32	MCSPI0_XFERLEVEL	This register provides transfer levels needed while using FIFO buffer during transfer.	5220 317Ch	5220 417Ch
180h	32	MCSPI0_DAFTX	This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.	5220 3180h	5220 4180h
1A0h	32	MCSPI0_DAFRX	This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.	5220 31A0h	5220 41A0h

4.22.1 MCSPI0_HL_REV Register (Offset = 0h) [reset = h]

Short Description: IP Revision Identifier (X.Y.R)Used by software to track features, bugs, and compatibility

Long Description:

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Table 4-2593. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0000h
MCSPI1	5220 1000h
MCSPI2	5220 2000h
MCSPI3	5220 3000h
MCSPI4	5220 4000h

Figure 4-1247. MCSPI0_HL_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RSVD		FUNC											
RO		RO		RO											
1		0		110000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_RTL				X_MAJOR				CUSTOM		Y_MINOR					
RO				RO				RO		RO					
11				10				0		1011					

Access Types Legend

Table 4-2594. HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Used to distinguish between old scheme and current
29 - 28	RSVD	RO	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27 - 16	FUNC	RO	1ADB0h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15 - 11	R_RTL	RO	Bh	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments
10 - 8	X_MAJOR	RO	Ah	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Master Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7 - 6	CUSTOM	RO	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers

Table 4-2594. HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 0	Y_MINOR	RO	3F3h	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

4.22.2 MCSPI0_HL_HWINFO Register (Offset = 4h) [reset = h]

Short Description: Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any).Actual field format and encoding is up to the module's designer to decide.

Long Description:

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Table 4-2595. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0004h
MCSPI1	5220 1004h
MCSPI2	5220 2004h
MCSPI3	5220 3004h
MCSPI4	5220 4004h

Figure 4-1248. MCSPI0_HL_HWINFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RETMODE	FFNBYTE					USEFIFO
RO									RO	RO					RO
0									0	100					1

Access Types Legend

Table 4-2596. HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RSVD	RO	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	RO	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET
5 - 1	FFNBYTE	RO	64h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account
0	USEFIFO	RO	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management

4.22.3 MCSPI0_HL_SYSCONFIG Register (Offset = 10h) [reset = h]

Short Description: Clock management configuration

Long Description:

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Table 4-2597. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0010h
MCSPI1	5220 1010h
MCSPI2	5220 2010h
MCSPI3	5220 3010h
MCSPI4	5220 4010h

Figure 4-1249. MCSPI0_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												IDLEMODE		FREEEMU	SOFTRESET
RO												RW		RW	RW
0												10		0	0

Access Types Legend

Table 4-2598. HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RSVD	RO	0h	Reserved
3 - 2	IDLEMODE	RW	Ah	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state
1	FREEEMU	RW	0h	Sensitivity to emulation [debug] suspend input signal
0	SOFTRESET	RW	0h	Software reset [Optional]

ADVANCE INFORMATION

4.22.4 MCSPI0_REVISION Register (Offset = 100h) [reset = h]

Short Description: This register contains the hard coded RTL revision number.

Long Description:

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Table 4-2599. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0100h
MCSPI1	5220 1100h
MCSPI2	5220 2100h
MCSPI3	5220 3100h
MCSPI4	5220 4100h

Figure 4-1250. MCSPI0_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_13								REV							
RO								RO							
0								101011							

Access Types Legend

Table 4-2600. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_13	RO	0h	Reads returns 0
7 - 0	REV	RO	18A93h	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

4.22.5 MCSPI0_SYSCONFIG Register (Offset = 110h) [reset = h]

Short Description: This register allows controlling various parameters of the OCP interface.

Long Description:

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Table 4-2601. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0110h
MCSPI1	5220 1110h
MCSPI2	5220 2110h
MCSPI3	5220 3110h
MCSPI4	5220 4110h

Figure 4-1251. MCSPI0_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_14						CLOCKACTIVITY		RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
RO						RW		RO			RW		RW	RW	RW
0						0		0			10		1	0	1

Access Types Legend

Table 4-2602. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	RESERVED_14	RO	0h	Reads returns 0
9 - 8	CLOCKACTIVITY	RW	0h	Clocks activity during wake up mode period
7 - 5	RESERVED_15	RO	0h	Reads returns 0
4 - 3	SIDLEMODE	RW	Ah	Power management
2	ENAWAKEUP	RW	1h	WakeUp feature control
1	SOFTRESET	RW	0h	Software reset During reads it always returns 0
0	AUTOIDLE	RW	1h	Internal OCP Clock gating strategy

4.22.6 MCSPI0_SYSSTATUS Register (Offset = 114h) [reset = h]

Short Description: This register provides status information about the module excluding the interrupt status information

Long Description:

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Table 4-2603. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0114h
MCSPI1	5220 1114h
MCSPI2	5220 2114h
MCSPI3	5220 3114h
MCSPI4	5220 4114h

Figure 4-1252. MCSPI0_SYSSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_16															RESET DONE
RO															RO
0															1

Access Types Legend

Table 4-2604. SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED_16	RO	0h	Reserved for module specific status information Read returns 0
0	RESETDONE	RO	1h	Internal Reset Monitoring

4.22.7 MCSPI0_IRQSTATUS Register (Offset = 118h) [reset = h]

Short Description: The interrupt status regroups all the status of the module internal events that can generate an interrupt

Long Description:

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Table 4-2605. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0118h
MCSPI1	5220 1118h
MCSPI2	5220 2118h
MCSPI3	5220 3118h
MCSPI4	5220 4118h

Figure 4-1253. MCSPI0_IRQSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_8														EOW	WKS
RO														RW	RW
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_7	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED_9	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY	RESERVED_10	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
RO	RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2606. IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED_8	RO	0h	Reads returns 0
17	EOW	RW	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]
16	WKS	RW	0h	Wake Up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED_7	RO	0h	Reads returns 0
14	RX3_FULL	RW	0h	Receiver register is full or almost full Only when Channel 3 is enabled
13	TX3_UNDERFLOW	RW	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled
12	TX3_EMPTY	RW	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event
11	RESERVED_9	RO	0h	Reads returns 0
10	RX2_FULL	RW	0h	Receiver register full or almost full Channel 2
9	TX2_UNDERFLOW	RW	0h	Transmitter register underflow Channel 2
8	TX2_EMPTY	RW	0h	Transmitter register empty or almost empty Channel 2
7	RESERVED_10	RO	0h	Reads returns 0
6	RX1_FULL	RW	0h	Receiver register full or almost full Channel 1
5	TX1_UNDERFLOW	RW	0h	Transmitter register underflow Channel 1

Table 4-2606. IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TX1_EMPTY	RW	0h	Transmitter register empty or almost empty Channel 1
3	RX0_OVERFLOW	RW	0h	Receiver register overflow [slave mode only] Channel 0
2	RX0_FULL	RW	0h	Receiver register full or almost full Channel 0
1	TX0_UNDERFLOW	RW	0h	Transmitter register underflow Channel 0
0	TX0_EMPTY	RW	0h	Transmitter register empty or almost empty Channel 0

4.22.8 MCSPI0_IRQENABLE Register (Offset = 11Ch) [reset = h]

Short Description: This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

Long Description:

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Table 4-2607. Instance Table

Instance Name	Physical Address
MCSPI0	5220 011Ch
MCSPI1	5220 111Ch
MCSPI2	5220 211Ch
MCSPI3	5220 311Ch
MCSPI4	5220 411Ch

Figure 4-1254. MCSPI0_IRQENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_5														EOW_ENABLE	WKE
RO														RW	RW
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED_6	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE	RESERVED_3	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
RO	RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2608. IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED_5	RO	0h	Reads return 0
17	EOW_ENABLE	RW	0h	End of Word count Interrupt Enable
16	WKE	RW	0h	Wake Up event interrupt Enable in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED_4	RO	0h	Reads returns 0
14	RX3_FULL_ENABLE	RW	0h	Receiver register Full Interrupt Enable Ch 3
13	TX3_UNDERFLOW_ENABLE	RW	0h	Transmitter register Underflow Interrupt Enable Ch 3
12	TX3_EMPTY_ENABLE	RW	0h	Transmitter register Empty Interrupt Enable Ch3
11	RESERVED_6	RO	0h	Reads return 0
10	RX2_FULL_ENABLE	RW	0h	Receiver register Full Interrupt Enable Ch 2
9	TX2_UNDERFLOW_ENABLE	RW	0h	Transmitter register Underflow Interrupt Enable Ch 2
8	TX2_EMPTY_ENABLE	RW	0h	Transmitter register Empty Interrupt Enable Ch 2
7	RESERVED_3	RO	0h	Reads return 0
6	RX1_FULL_ENABLE	RW	0h	Receiver register Full Interrupt Enable Ch 1
5	TX1_UNDERFLOW_ENABLE	RW	0h	Transmitter register Underflow Interrupt Enable Ch 1

Table 4-2608. IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TX1_EMPTY_ENABLE	RW	0h	Transmitter register Empty Interrupt Enable Ch 1
3	RX0_OVERFLOW_ENABLE	RW	0h	Receiver register Overflow Interrupt Enable Ch 0
2	RX0_FULL_ENABLE	RW	0h	Receiver register Full Interrupt Enable Ch 0
1	TX0_UNDERFLOW_ENABLE	RW	0h	Transmitter register Underflow Interrupt Enable Ch 0
0	TX0_EMPTY_ENABLE	RW	0h	Transmitter register Empty Interrupt Enable Ch 0

4.22.9 MCSPI0_WAKEUPENABLE Register (Offset = 120h) [reset = h]

Short Description: The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

Long Description:

Return to Summary Table

Table 4-2609. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0120h
MCSPI1	5220 1120h
MCSPI2	5220 2120h
MCSPI3	5220 3120h
MCSPI4	5220 4120h

Figure 4-1255. MCSPI0_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_18															WKEN
RO															RW
0															0

Access Types Legend

Table 4-2610. WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED_18	RO	0h	Reads returns 0
0	WKEN	RW	0h	WakeUp functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]

4.22.10 MCSPI0_SYST Register (Offset = 124h) [reset = h]

Short Description: This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

Long Description:

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Table 4-2611. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0124h
MCSPI1	5220 1124h
MCSPI2	5220 2124h
MCSPI3	5220 3124h
MCSPI4	5220 4124h

Figure 4-1256. MCSPI0_SYST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_17				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0	WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
RO				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0				0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2612. SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED_17	RO	0h	Reads returns 0
11	SSB	RW	0h	Set status bit
10	SPIENDIR	RW	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line
9	SPIDATDIR1	RW	0h	Set the direction of the SPIDAT[1]
8	SPIDATDIR0	RW	0h	Set the direction of the SPIDAT[0]
7	WAKD	RW	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit
6	SPICLK	RW	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	RW	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect
4	SPIDAT_0	RW	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect

Table 4-2612. SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SPIEN_3	RW	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	RW	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	RW	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	RW	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

4.22.11 MCSPI0_MODULCTRL Register (Offset = 128h) [reset = h]

Short Description: This register is dedicated to the configuration of the serial port interface.

Long Description:

Return to Summary Table

Table 4-2613. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0128h
MCSPI1	5220 1128h
MCSPI2	5220 2128h
MCSPI3	5220 3128h
MCSPI4	5220 4128h

Figure 4-1257. MCSPI0_MODULCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_11							FDAA	MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
RO							RW	RW	RW			RW	RW	RW	RW
0							0	0	0			0	1	0	0

Access Types Legend

Table 4-2614. MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED_11	RO	0h	Reads returns 0
8	FDAA	RW	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers
7	MOA	RW	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16
6 - 4	INITDLY	RW	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE master mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period
3	SYSTEM_TEST	RW	0h	Enables the system test mode
2	MS	RW	1h	Master/ Slave
1	PIN34	RW	0h	Pin mode selection: This register is used to configure the SPI pin mode, in master or slave mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers
0	SINGLE	RW	0h	Single channel / Multi Channel [master mode only]

4.22.12 MCSPI0_CH0CONF Register (Offset = 12Ch) [reset = h]

Short Description: This register is dedicated to the configuration of the channel 0

Long Description:

Return to Summary Table

Table 4-2615. Instance Table

Instance Name	Physical Address
MCSPI0	5220 012Ch
MCSPI1	5220 112Ch
MCSPI2	5220 212Ch
MCSPI3	5220 312Ch
MCSPI4	5220 412Ch

Figure 4-1258. MCSPI0_CH0CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0		CLKG	FFER	FFEW	TCS0		SBPOL	SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
RO		RW	RW	RW	RW		RW	RW	RW		RW	RW	RW	RW	RW
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
RW	RW	RW		RW					RW	RW				RW	RW
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2616. CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED_0	RO	0h	read returns 0
29	CLKG	RW	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	RW	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	RW	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS0	RW	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	RW	0h	Start bit polarity
23	SBE	RW	0h	Start bit enable for SPI transfer
22 - 21	SPIENSLV	RW	0h	Channel 0 only and slave mode only: SPI slave select signal detection Reserved bits for other cases
20	FORCE	RW	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	RW	0h	Turbo mode
18	IS	RW	1h	Input Select
17	DPE1	RW	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	RW	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

Table 4-2616. CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	RW	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	RW	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	RW	0h	Transmit/Receive modes
11 - 7	WL	RW	0h	SPI word length
6	EPOL	RW	0h	SPIEN polarity
5 - 2	CLKD	RW	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	RW	0h	SPICLK polarity
0	PHA	RW	0h	SPICLK phase

4.22.13 MCSPI0_CH0STAT Register (Offset = 130h) [reset = h]

Short Description: This register provides status information about transmitter and receiver registers of channel 0

Long Description:

Return to Summary Table

Table 4-2617. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0130h
MCSPI1	5220 1130h
MCSPI2	5220 2130h
MCSPI3	5220 3130h
MCSPI4	5220 4130h

Figure 4-1259. MCSPI0_CH0STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
RO									RO	RO	RO	RO	RO	RO	RO
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2618. CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED_2	RO	0h	Read returns 0
6	RXFFF	RO	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	RO	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	RO	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	RO	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	RO	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	RO	0h	Channel "i" Transmitter Register Status
0	RXS	RO	0h	Channel "i" Receiver Register Status

4.22.14 MCSPI0_CH0CTRL Register (Offset = 134h) [reset = h]

Short Description: This register is dedicated to enable the channel 0

Long Description:

Return to Summary Table

Table 4-2619. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0134h
MCSPI1	5220 1134h
MCSPI2	5220 2134h
MCSPI3	5220 3134h
MCSPI4	5220 4134h

Figure 4-1260. MCSPI0_CH0CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED_1							EN
RW								RO							RW
0								0							0

Access Types Legend

Table 4-2620. CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Read returns 0
15 - 8	EXTCLK	RW	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED_1	RO	0h	Read returns 0
0	EN	RW	0h	Channel Enable

4.22.15 MCSPI0_TX0 Register (Offset = 138h) [reset = h]

Short Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2621. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0138h
MCSPI1	5220 1138h
MCSPI2	5220 2138h
MCSPI3	5220 3138h
MCSPI4	5220 4138h

Figure 4-1261. MCSPI0_TX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
RW															
0															

Access Types Legend

Table 4-2622. TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	RW	0h	Channel 0 Data to transmit

4.22.16 MCSPI0_RX0 Register (Offset = 13Ch) [reset = h]

Short Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2623. Instance Table

Instance Name	Physical Address
MCSPI0	5220 013Ch
MCSPI1	5220 113Ch
MCSPI2	5220 213Ch
MCSPI3	5220 313Ch
MCSPI4	5220 413Ch

Figure 4-1262. MCSPI0_RX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
RO															
0															

Access Types Legend

Table 4-2624. RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	RO	0h	Channel 0 Received Data

4.22.17 MCSPI0_CH1CONF Register (Offset = 140h) [reset = h]

Short Description: This register is dedicated to the configuration of the channel.

Long Description:

Return to Summary Table

Table 4-2625. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0140h
MCSPI1	5220 1140h
MCSPI2	5220 2140h
MCSPI3	5220 3140h
MCSPI4	5220 4140h

Figure 4-1263. MCSPI0_CH1CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0		CLKG	FFER	FFEW	TCS1		SBPOL	SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
RO		RW	RW	RW	RW		RW	RW	RO		RW	RW	RW	RW	RW
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
RW	RW	RW		RW					RW	RW				RW	RW
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2626. CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED_0	RO	0h	read returns 0
29	CLKG	RW	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	RW	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	RW	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS1	RW	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	RW	0h	Start bit polarity
23	SBE	RW	0h	Start bit enable for SPI transfer
22 - 21	RESERVED_1	RO	0h	read returns 0
20	FORCE	RW	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	RW	0h	Turbo mode
18	IS	RW	1h	Input Select
17	DPE1	RW	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	RW	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]
15	DMAR	RW	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel

Table 4-2626. CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	RW	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	RW	0h	Transmit/Receive modes
11 - 7	WL	RW	0h	SPI word length
6	EPOL	RW	0h	SPIEN polarity
5 - 2	CLKD	RW	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	RW	0h	SPICLK polarity
0	PHA	RW	0h	SPICLK phase

4.22.18 MCSPI0_CH1STAT Register (Offset = 144h) [reset = h]

Short Description: This register provides status information about transmitter and receiver registers of channel 1

Long Description:

Return to Summary Table

Table 4-2627. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0144h
MCSPI1	5220 1144h
MCSPI2	5220 2144h
MCSPI3	5220 3144h
MCSPI4	5220 4144h

Figure 4-1264. MCSPI0_CH1STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
RO									RO	RO	RO	RO	RO	RO	RO
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2628. CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED_2	RO	0h	Read returns 0
6	RXFFF	RO	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	RO	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	RO	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	RO	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	RO	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	RO	0h	Channel "i" Transmitter Register Status
0	RXS	RO	0h	Channel "i" Receiver Register Status

4.22.19 MCSPI0_CH1CTRL Register (Offset = 148h) [reset = h]

Short Description: This register is dedicated to enable the channel 1

Long Description:

Return to Summary Table

Table 4-2629. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0148h
MCSPI1	5220 1148h
MCSPI2	5220 2148h
MCSPI3	5220 3148h
MCSPI4	5220 4148h

Figure 4-1265. MCSPI0_CH1CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED_1							EN
RW								RO							RW
0								0							0

Access Types Legend

Table 4-2630. CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Read returns 0
15 - 8	EXTCLK	RW	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED_1	RO	0h	Read returns 0
0	EN	RW	0h	Channel Enable

4.22.20 MCSPI0_TX1 Register (Offset = 14Ch) [reset = h]

Short Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2631. Instance Table

Instance Name	Physical Address
MCSPI0	5220 014Ch
MCSPI1	5220 114Ch
MCSPI2	5220 214Ch
MCSPI3	5220 314Ch
MCSPI4	5220 414Ch

Figure 4-1266. MCSPI0_TX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
RW															
0															

Access Types Legend

Table 4-2632. TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	RW	0h	Channel 1 Data to transmit

4.22.21 MCSPI0_RX1 Register (Offset = 150h) [reset = h]

Short Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2633. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0150h
MCSPI1	5220 1150h
MCSPI2	5220 2150h
MCSPI3	5220 3150h
MCSPI4	5220 4150h

Figure 4-1267. MCSPI0_RX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
RO															
0															

Access Types Legend

Table 4-2634. RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	RO	0h	Channel 1 Received Data

4.22.22 MCSPI0_CH2CONF Register (Offset = 154h) [reset = h]

Short Description: This register is dedicated to the configuration of the channel 2

Long Description:

Return to Summary Table

Table 4-2635. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0154h
MCSPI1	5220 1154h
MCSPI2	5220 2154h
MCSPI3	5220 3154h
MCSPI4	5220 4154h

Figure 4-1268. MCSPI0_CH2CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0		CLKG	FFER	FFEW	TCS2		SBPOL	SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
RO		RW	RW	RW	RW		RW	RW	RO		RW	RW	RW	RW	RW
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
RW	RW	RW		RW					RW	RW				RW	RW
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2636. CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED_0	RO	0h	read returns 0
29	CLKG	RW	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	RW	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	RW	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS2	RW	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	RW	0h	Start bit polarity
23	SBE	RW	0h	Start bit enable for SPI transfer
22 - 21	RESERVED_1	RO	0h	read returns 0
20	FORCE	RW	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	RW	0h	Turbo mode
18	IS	RW	1h	Input Select
17	DPE1	RW	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	RW	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]
15	DMAR	RW	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel

Table 4-2636. CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	RW	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	RW	0h	Transmit/Receive modes
11 - 7	WL	RW	0h	SPI word length
6	EPOL	RW	0h	SPIEN polarity
5 - 2	CLKD	RW	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	RW	0h	SPICLK polarity
0	PHA	RW	0h	SPICLK phase

4.22.23 MCSPI0_CH2STAT Register (Offset = 158h) [reset = h]

Short Description: This register provides status information about transmitter and receiver registers of channel 2

Long Description:

Return to Summary Table

Table 4-2637. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0158h
MCSPI1	5220 1158h
MCSPI2	5220 2158h
MCSPI3	5220 3158h
MCSPI4	5220 4158h

Figure 4-1269. MCSPI0_CH2STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
RO									RO	RO	RO	RO	RO	RO	RO
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2638. CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED_2	RO	0h	Read returns 0
6	RXFFF	RO	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	RO	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	RO	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	RO	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	RO	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	RO	0h	Channel "i" Transmitter Register Status
0	RXS	RO	0h	Channel "i" Receiver Register Status

4.22.24 MCSPI0_CH2CTRL Register (Offset = 15Ch) [reset = h]

Short Description: This register is dedicated to enable the channel 2

Long Description:

Return to Summary Table

Table 4-2639. Instance Table

Instance Name	Physical Address
MCSPI0	5220 015Ch
MCSPI1	5220 115Ch
MCSPI2	5220 215Ch
MCSPI3	5220 315Ch
MCSPI4	5220 415Ch

Figure 4-1270. MCSPI0_CH2CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED_1							EN
RW								RO							RW
0								0							0

Access Types Legend

Table 4-2640. CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Read returns 0
15 - 8	EXTCLK	RW	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED_1	RO	0h	Read returns 0
0	EN	RW	0h	Channel Enable

4.22.25 MCSPI0_TX2 Register (Offset = 160h) [reset = h]

Short Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2641. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0160h
MCSPI1	5220 1160h
MCSPI2	5220 2160h
MCSPI3	5220 3160h
MCSPI4	5220 4160h

Figure 4-1271. MCSPI0_TX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
RW															
0															

Access Types Legend

Table 4-2642. TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	RW	0h	Channel 2 Data to transmit

4.22.26 MCSPI0_RX2 Register (Offset = 164h) [reset = h]

Short Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2643. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0164h
MCSPI1	5220 1164h
MCSPI2	5220 2164h
MCSPI3	5220 3164h
MCSPI4	5220 4164h

Figure 4-1272. MCSPI0_RX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
RO															
0															

Access Types Legend

Table 4-2644. RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	RO	0h	Channel 2 Received Data

4.22.27 MCSPI0_CH3CONF Register (Offset = 168h) [reset = h]

Short Description: This register is dedicated to the configuration of the channel 3

Long Description:

Return to Summary Table

Table 4-2645. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0168h
MCSPI1	5220 1168h
MCSPI2	5220 2168h
MCSPI3	5220 3168h
MCSPI4	5220 4168h

Figure 4-1273. MCSPI0_CH3CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_0		CLKG	FFER	FFEW	TCS3		SBPOL	SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
RO		RW	RW	RW	RW		RW	RW	RO		RW	RW	RW	RW	RW
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
RW	RW	RW		RW					RW	RW				RW	RW
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2646. CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED_0	RO	0h	read returns 0
29	CLKG	RW	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	RW	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	RW	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS3	RW	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	RW	0h	Start bit polarity
23	SBE	RW	0h	Start bit enable for SPI transfer
22 - 21	RESERVED_1	RO	0h	read returns 0
20	FORCE	RW	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	RW	0h	Turbo mode
18	IS	RW	1h	Input Select
17	DPE1	RW	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	RW	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]
15	DMAR	RW	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel

Table 4-2646. CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	RW	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	RW	0h	Transmit/Receive modes
11 - 7	WL	RW	0h	SPI word length
6	EPOL	RW	0h	SPIEN polarity
5 - 2	CLKD	RW	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	RW	0h	SPICLK polarity
0	PHA	RW	0h	SPICLK phase

4.22.28 MCSPI0_CH3STAT Register (Offset = 16Ch) [reset = h]

Short Description: This register provides status information about transmitter and receiver registers of channel 3

Long Description:

Return to Summary Table

Table 4-2647. Instance Table

Instance Name	Physical Address
MCSPI0	5220 016Ch
MCSPI1	5220 116Ch
MCSPI2	5220 216Ch
MCSPI3	5220 316Ch
MCSPI4	5220 416Ch

Figure 4-1274. MCSPI0_CH3STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
RO									RO	RO	RO	RO	RO	RO	RO
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2648. CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED_2	RO	0h	Read returns 0
6	RXFFF	RO	0h	Channel "i" FIFO Receive Buffer Full Status
5	RXFFE	RO	0h	Channel "i" FIFO Receive Buffer Empty Status
4	TXFFF	RO	0h	Channel "i" FIFO Transmit Buffer Full Status
3	TXFFE	RO	0h	Channel "i" FIFO Transmit Buffer Empty Status
2	EOT	RO	0h	Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	RO	0h	Channel "i" Transmitter Register Status
0	RXS	RO	0h	Channel "i" Receiver Register Status

4.22.29 MCSPI0_CH3CTRL Register (Offset = 170h) [reset = h]

Short Description: This register is dedicated to enable the channel 3

Long Description:

Return to Summary Table

Table 4-2649. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0170h
MCSPI1	5220 1170h
MCSPI2	5220 2170h
MCSPI3	5220 3170h
MCSPI4	5220 4170h

Figure 4-1275. MCSPI0_CH3CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED_1							EN
RW								RO							RW
0								0							0

Access Types Legend

Table 4-2650. CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Read returns 0
15 - 8	EXTCLK	RW	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED_1	RO	0h	Read returns 0
0	EN	RW	0h	Channel Enable

4.22.30 MCSPI0_TX3 Register (Offset = 174h) [reset = h]

Short Description: This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2651. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0174h
MCSPI1	5220 1174h
MCSPI2	5220 2174h
MCSPI3	5220 3174h
MCSPI4	5220 4174h

Figure 4-1276. MCSPI0_TX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
RW															
0															

Access Types Legend

Table 4-2652. TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	RW	0h	Channel 3 Data to transmit

4.22.31 MCSPI0_RX3 Register (Offset = 178h) [reset = h]

Short Description: This register contains a single SPI word received through the serial link, what ever SPI word length is.

Long Description:

Return to Summary Table

Table 4-2653. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0178h
MCSPI1	5220 1178h
MCSPI2	5220 2178h
MCSPI3	5220 3178h
MCSPI4	5220 4178h

Figure 4-1277. MCSPI0_RX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
RO															
0															

Access Types Legend

Table 4-2654. RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	RO	0h	Channel 3 Received Data

4.22.32 MCSPI0_XFERLEVEL Register (Offset = 17Ch) [reset = h]

Short Description: This register provides transfer levels needed while using FIFO buffer during transfer.

Long Description:

Return to Summary Table

Table 4-2655. Instance Table

Instance Name	Physical Address
MCSPI0	5220 017Ch
MCSPI1	5220 117Ch
MCSPI2	5220 217Ch
MCSPI3	5220 317Ch
MCSPI4	5220 417Ch

Figure 4-1278. MCSPI0_XFERLEVEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFL								AEL							
RW								RW							
0								0							

Access Types Legend

Table 4-2656. XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	WCNT	RW	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index
15 - 8	AFL	RW	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE
7 - 0	AEL	RW	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1

4.22.33 MCSPI0_DAFTX Register (Offset = 180h) [reset = h]

Short Description: This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

Long Description:

Return to Summary Table

Table 4-2657. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0180h
MCSPI1	5220 1180h
MCSPI2	5220 2180h
MCSPI3	5220 3180h
MCSPI4	5220 4180h

Figure 4-1279. MCSPI0_DAFTX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFTDATA															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFTDATA															
RW															
0															

Access Types Legend

Table 4-2658. DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DAFTDATA	RW	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

4.22.34 MCSPI0_DAFRX Register (Offset = 1A0h) [reset = h]

Short Description: This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

Long Description:

Return to Summary Table

Table 4-2659. Instance Table

Instance Name	Physical Address
MCSPI0	5220 01A0h
MCSPI1	5220 11A0h
MCSPI2	5220 21A0h
MCSPI3	5220 31A0h
MCSPI4	5220 41A0h

Figure 4-1280. MCSPI0_DAFRX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFRDATA															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFRDATA															
RO															
0															

Access Types Legend

Table 4-2660. DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DAFRDATA	RO	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

Table 4-2661. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.23 MSS_SPINLOCK Registers

Table 4-2662. SPINLOCK0, SPINLOCK0_SPINLOCK Registers, Base Address=50E0 0000H, Length=3

Offset	Length	Acronym	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK0_REVISION	This is the standard TI peripheral ID register that exists at address 0 in the peripheral space	50E0 0000h
10h	8	SPINLOCK0_SYSCONFIG	Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock	50E0 0010h
14h	32	SPINLOCK0_SYSTATUS	Provides information about the Spinlock module	50E0 0014h
800h	0	SPINLOCK0_LOCK_REG	The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'	50E0 0800h

4.23.1 SPINLOCK0_REVISION Register (Offset = 0h) [reset = h]

Short Description: This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Long Description:

Return to Summary Table

Table 4-2663. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0000h

Figure 4-1281. SPINLOCK0_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
RO		RO		RO											
1		10		11011111010											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_RTL				X_MAJOR				CUSTOM		Y_MINOR					
RO				RO				RO		RO					
1100				1				0		0					

Access Types Legend

Table 4-2664. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Used to distinguish which ID numbering scheme is used.
29 - 28	BU	RO	Ah	BU identifier
27 - 16	FUNC	RO	290503862h	Module family.
15 - 11	R_RTL	RO	44Ch	RTL version. R of X.Y.R.Z
10 - 8	X_MAJOR	RO	1h	Major revision. X of X.Y.R.Z
7 - 6	CUSTOM	RO	0h	Special version number
5 - 0	Y_MINOR	RO	0h	Minor revision. Y of X.Y.R.Z

4.23.2 SPINLOCK0_SYSCONFIG Register (Offset = 10h) [reset = h]

Short Description: Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

Long Description:

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Table 4-2665. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0010h

Figure 4-1282. SPINLOCK0_SYSCONFIG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SOFTRESET	RESERVED
NONE						RW	NONE
0						0	0

Access Types Legend

Table 4-2666. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFTRESET	RW	0h	Module Software ResetThe bit is automatically reset by the hardware. During reads, it always returns 0It has the same effect as the hardware resetWriting a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks
	RESERVED	NONE		Reserved

4.23.3 SPINLOCK0_SYSTATUS Register (Offset = 14h) [reset = h]

Short Description: Provides information about the Spinlock module

Long Description:

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Table 4-2667. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0014h

Figure 4-1283. SPINLOCK0_SYSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUMLOCKS								RESERVED							
RO								NONE							
1000								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IU7	IU6	IU5	IU4	IU3	IU2	IU1	IU0
NONE								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2668. SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NUMLOCKS	RO	3E8h	Module configuration parameter n, the total number of spinlocks divided by 32.e.g. For 256 spin locks, this will return the number 0x08
	RESERVED	NONE		Reserved
7	IU7	RO	0h	In-Use flag 7 covering lock registers 224 - 255.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 224 - 255 are in the Not Taken stateRead 1 : At least one of the lock registers 224 - 255 are in the Taken state
6	IU6	RO	0h	In-Use flag 6 covering lock registers 192 - 223.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 192 - 223 are in the Not Taken stateRead 1 : At least one of the lock registers 192 - 223 are in the Taken state
5	IU5	RO	0h	In-Use flag 5 covering lock registers 160 - 191.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 160 - 191 are in the Not Taken stateRead 1 : At least one of the lock registers 160 - 191 are in the Taken state
4	IU4	RO	0h	In-Use flag 4 covering lock registers 128 - 159.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 128 - 159 are in the Not Taken stateRead 1 : At least one of the lock registers 128 - 159 are in the Taken state
3	IU3	RO	0h	In-Use flag 3 covering lock registers 96 - 127.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 96 - 127 are in the Not Taken stateRead 1 : At least one of the lock registers 96 - 127 are in the Taken state
2	IU2	RO	0h	In-Use flag 2 covering lock registers 64 - 95.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 64 - 95 are in the Not Taken stateRead 1 : At least one of the lock registers 64 - 95 are in the Taken state
1	IU1	RO	0h	In-Use flag 1 covering lock registers 32 - 63.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 32 - 63 are in the Not Taken stateRead 1 : At least one of the lock registers 32 - 63 are in the Taken state

Table 4-2668. SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IU0	RO	0h	In-Use flag 0 covering lock registers 0 - 31.If no lock registers are implemented in this range, then this flag always reads as 0Read 0 : All lock registers 0 - 31 are in the Not Taken stateRead 1 : At least one of the lock registers 0 - 31 are in the Taken state

4.23.4 SPINLOCK0_LOCK_REG Register (Offset = 800h) [reset = h]

Short Description: The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'

Long Description:

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Table 4-2669. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0800h

Figure 4-1284. SPINLOCK0_LOCK_REG Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
TAKEN							
RW							
0							

Access Types Legend

Table 4-2670. LOCK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TAKEN	RW	0h	Lock StatusRead 0 : Lock was previously free. The reader now has been granted the lock.Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry.Write 0 : Free the lock by setting TAKEN to zero.Write 1 : No effect

Table 4-2671. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.24 MSS_TCM Registers

Table 4-2672. R5SS0_CORE0_TCMA_RAM, R5SS0_CORE0_TCMA_RAM_R5SS0_CORE0_TCMA_RAM Registers, Base Address=0002 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS0_CORE0_TCMA_RAM Physical Address
0h	32	R5SS0_CORE0_TCMA_RAM_RAM_START_TCMA	RW	0002 0000h
7FFCh	32	R5SS0_CORE0_TCMA_RAM_RAM_END_TCMA	RW	0002 7FFCh

Table 4-2673. R5SS0_CORE0_TCMB_RAM, R5SS0_CORE0_TCMB_RAM_R5SS0_CORE0_TCMB_RAM Registers, Base Address=0008 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS0_CORE0_TCMB_RAM Physical Address
0h	32	R5SS0_CORE0_TCMB_RAM_RAM_START_TCMA	RW	0008 0000h
7FFCh	32	R5SS0_CORE0_TCMB_RAM_RAM_END_TCMA	RW	0008 7FFCh

4.24.1 R5SS0_CORE0_TCMA_RAM_RAM_START_TCMA Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2674. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA_RAM	0002 0000h

Figure 4-1285. R5SS0_CORE0_TCMA_RAM_RAM_START_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_START															
RW															
0															

Access Types Legend

Table 4-2675. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_START	RW	0h	RAM start address of master sub system tcma

4.24.2 R5SS0_CORE0_TCMA_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2676. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA_RAM	0002 7FFCh

Figure 4-1286. R5SS0_CORE0_TCMA_RAM_RAM_END_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_END															
RW															
0															

Access Types Legend

Table 4-2677. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_END	RW	0h	RAM end address of master sub system tcma

4.24.3 R5SS0_CORE0_TCMB_RAM_RAM_START_TCMA Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2678. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB_RAM	0008 0000h

Figure 4-1287. R5SS0_CORE0_TCMB_RAM_RAM_START_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_START															
RW															
0															

Access Types Legend

Table 4-2679. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_START	RW	0h	RAM start address of master sub system tcma

4.24.4 R5SS0_CORE0_TCMB_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2680. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB_RAM	0008 7FFCh

Figure 4-1288. R5SS0_CORE0_TCMB_RAM_RAM_END_TCMA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RAM_END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_END															
RW															
0															

Access Types Legend

Table 4-2681. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_END	RW	0h	RAM end address of master sub system tcma

Table 4-2682. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.25 MSS_TCMA_CR5B Registers

Table 4-2683. R5SS0_CORE1_TCMA, R5SS0_CORE1_TCMA_R5SS0_CORE1_TCMA Registers, Base Address=7820 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS0_CORE1_TCMA Physical Address
0h	32	R5SS0_CORE1_TCMA_START	RW	7820 0000h
7FFCh	32	R5SS0_CORE1_TCMA_END	RW	7820 7FFCh

4.25.1 R5SS0_CORE1_TCMA_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2684. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMA	7820 0000h

Figure 4-1289. R5SS0_CORE1_TCMA_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2685. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMA start address

4.25.2 R5SS0_CORE1_TCMA_END Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2686. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMA	7820 7FFCh

Figure 4-1290. R5SS0_CORE1_TCMA_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2687. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMA end address

Table 4-2688. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.26 MSS_TCMA1_CR5A Registers

Table 4-2689. R5SS0_CORE0_TCMA, R5SS0_CORE0_TCMA_R5SS0_CORE0_TCMA Registers, Base Address=7800 0000H, Length=6

Offset	Length	Acronym	Register Name	R5SS0_CORE0_TCMA Physical Address
0h	32	R5SS0_CORE0_TCMA_START	RW	7800 0000h
FFFCh	32	R5SS0_CORE0_TCMA_END	RW	7800 FFFCh

4.26.1 R5SS0_CORE0_TCMA_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2690. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA	7800 0000h

Figure 4-1291. R5SS0_CORE0_TCMA_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2691. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMA start address

4.26.2 R5SS0_CORE0_TCMA_END Register (Offset = FFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2692. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA	7800 FFFCh

Figure 4-1292. R5SS0_CORE0_TCMA_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2693. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMA end address

Table 4-2694. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.27 MSS_TCMB_CR5A Registers

Table 4-2695. R5SS0_CORE0_TCMB, R5SS0_CORE0_TCMB_R5SS0_CORE0_TCMB Registers, Base Address=7810 0000H, Length=6

Offset	Length	Acronym	Register Name	R5SS0_CORE0_TCMB Physical Address
0h	32	R5SS0_CORE0_TCMB_START	RW	7810 0000h
FFFCh	32	R5SS0_CORE0_TCMB_END	RW	7810 FFFCh

4.27.1 R5SS0_CORE0_TCMB_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2696. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB	7810 0000h

Figure 4-1293. R5SS0_CORE0_TCMB_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2697. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMB start address

4.27.2 R5SS0_CORE0_TCMB_END Register (Offset = FFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2698. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB	7810 FFFCh

Figure 4-1294. R5SS0_CORE0_TCMB_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2699. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMB end address

Table 4-2700. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.28 MSS_TCMB_CR5B Registers

Table 4-2701. R5SS0_CORE1_TCMB, R5SS0_CORE1_TCMB_R5SS0_CORE1_TCMB Registers, Base Address=7830 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS0_CORE1_TCMB Physical Address
0h	32	R5SS0_CORE1_TCMB_START	RW	7830 0000h
7FFCh	32	R5SS0_CORE1_TCMB_END	RW	7830 7FFCh

Table 4-2702. R5SS0_CORE1_TCMB, R5SS0_CORE1_TCMB_R5SS0_CORE1_TCMB Registers, Base Address=7830 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	R5SS0_CORE1_TCMB_START	RW
7FFCh	32	R5SS0_CORE1_TCMB_END	RW

Table 4-2703. R5SS1_CORE0_TCMA, R5SS1_CORE0_TCMA_R5SS1_CORE0_TCMA Registers, Base Address=7840 0000H, Length=6

Offset	Length	Acronym	Register Name	R5SS1_CORE0_TCMA Physical Address
0h	32	R5SS1_CORE0_TCMA_START	RW	7840 0000h
FFFCh	32	R5SS1_CORE0_TCMA_END	RW	7840 FFFCh

Table 4-2704. R5SS1_CORE0_TCMA, R5SS1_CORE0_TCMA_R5SS1_CORE0_TCMA Registers, Base Address=7840 0000H, Length=6

Offset	Length	Acronym	Register Name
0h	32	R5SS1_CORE0_TCMA_START	RW
FFFCh	32	R5SS1_CORE0_TCMA_END	RW

Table 4-2705. R5SS1_CORE0_TCMB, R5SS1_CORE0_TCMB_R5SS1_CORE0_TCMB Registers, Base Address=7850 0000H, Length=6

Offset	Length	Acronym	Register Name	R5SS1_CORE0_TCMB Physical Address
0h	32	R5SS1_CORE0_TCMB_START	RW	7850 0000h
FFFCh	32	R5SS1_CORE0_TCMB_END	RW	7850 FFFCh

Table 4-2706. R5SS1_CORE0_TCMB, R5SS1_CORE0_TCMB_R5SS1_CORE0_TCMB Registers, Base Address=7850 0000H, Length=6

Offset	Length	Acronym	Register Name
0h	32	R5SS1_CORE0_TCMB_START	RW
FFFCh	32	R5SS1_CORE0_TCMB_END	RW

Table 4-2707. R5SS1_CORE1_TCMA, R5SS1_CORE1_TCMA_R5SS1_CORE1_TCMA Registers, Base Address=7860 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS1_CORE1_TCMA Physical Address
0h	32	R5SS1_CORE1_TCMA_START	RW	7860 0000h
7FFCh	32	R5SS1_CORE1_TCMA_END	RW	7860 7FFCh

Table 4-2708. R5SS1_CORE1_TCMA, R5SS1_CORE1_TCMA_R5SS1_CORE1_TCMA Registers, Base Address=7860 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	R5SS1_CORE1_TCMA_START	RW
7FFCh	32	R5SS1_CORE1_TCMA_END	RW

Table 4-2709. R5SS1_CORE1_TCMB, R5SS1_CORE1_TCMB_R5SS1_CORE1_TCMB Registers, Base Address=7870 0000H, Length=3

Offset	Length	Acronym	Register Name	R5SS1_CORE1_TCMB Physical Address
0h	32	R5SS1_CORE1_TCMB_START	RW	7870 0000h
7FFCh	32	R5SS1_CORE1_TCMB_END	RW	7870 7FFCh

Table 4-2710. R5SS1_CORE1_TCMB, R5SS1_CORE1_TCMB_R5SS1_CORE1_TCMB Registers, Base Address=7870 0000H, Length=3

Offset	Length	Acronym	Register Name
0h	32	R5SS1_CORE1_TCMB_START	RW
7FFCh	32	R5SS1_CORE1_TCMB_END	RW

4.28.1 R5SS0_CORE1_TCMB_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2711. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMB	7830 0000h

Figure 4-1295. R5SS0_CORE1_TCMB_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2712. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMB start address

4.28.2 R5SS0_CORE1_TCMB_END Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2713. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMB	7830 7FFCh

Figure 4-1296. R5SS0_CORE1_TCMB_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2714. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMB end address

4.28.3 R5SS1_CORE0_TCMA_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2715. Instance Table

Instance Name	Physical Address
R5SS1_CORE0_TCMA	7840 0000h

Figure 4-1297. R5SS1_CORE0_TCMA_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2716. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMA start address

4.28.4 R5SS1_CORE0_TCMA_END Register (Offset = FFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2717. Instance Table

Instance Name	Physical Address
R5SS1_CORE0_TCMA	7840 FFFCh

Figure 4-1298. R5SS1_CORE0_TCMA_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2718. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMA end address

4.28.5 R5SS1_CORE0_TCMB_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2719. Instance Table

Instance Name	Physical Address
R5SS1_CORE0_TCMB	7850 0000h

Figure 4-1299. R5SS1_CORE0_TCMB_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2720. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMB start address

4.28.6 R5SS1_CORE0_TCMB_END Register (Offset = FFFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2721. Instance Table

Instance Name	Physical Address
R5SS1_CORE0_TCMB	7850 FFFCh

Figure 4-1300. R5SS1_CORE0_TCMB_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2722. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMB end address

4.28.7 R5SS1_CORE1_TCMA_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2723. Instance Table

Instance Name	Physical Address
R5SS1_CORE1_TCMA	7860 0000h

Figure 4-1301. R5SS1_CORE1_TCMA_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2724. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMA start address

4.28.8 R5SS1_CORE1_TCMA_END Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2725. Instance Table

Instance Name	Physical Address
R5SS1_CORE1_TCMA	7860 7FFCh

Figure 4-1302. R5SS1_CORE1_TCMA_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2726. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMA end address

4.28.9 R5SS1_CORE1_TCMB_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

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Table 4-2727. Instance Table

Instance Name	Physical Address
R5SS1_CORE1_TCMB	7870 0000h

Figure 4-1303. R5SS1_CORE1_TCMB_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-2728. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMB start address

4.28.10 R5SS1_CORE1_TCMB_END Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

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Table 4-2729. Instance Table

Instance Name	Physical Address
R5SS1_CORE1_TCMB	7870 7FFCh

Figure 4-1304. R5SS1_CORE1_TCMB_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-2730. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	TCMB end address

Table 4-2731. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined

4.29 MSS_UART Registers

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART0_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART0_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h
0h	32	UART0_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART0_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	8	UART0_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART0_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	32	UART0_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART0_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART0_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
8h	8	UART0_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART0_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART0_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART0_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART0_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h
10h	32	UART0_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART0_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART0_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART0_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART0_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART0_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART0_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART0_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART0_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART0_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
1Ch	32	UART0_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART0_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h
24h	32	UART0_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
28h	32	UART0_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART0_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h
2Ch	32	UART0_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART0_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch

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Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART0_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h
30h	32	UART0_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART0_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h
34h	32	UART0_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART0_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
38h	32	UART0_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART0_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART0_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h
44h	32	UART0_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
48h	32	UART0_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART0_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART0_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART0_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART0_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART0_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART0_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART0_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART0_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART0_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART0_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART0_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART0_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART0_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART0_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART0_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART0_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART0_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART0_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2732. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART0_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART0_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART0_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART0_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART0_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART0_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART0_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART0_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART0_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART0_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART0_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART0_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART0_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART0_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART0_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART0_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART0_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART0_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART0_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART0_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART0_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART0_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART0_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART0_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART0_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART0_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART0_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART0_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART0_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART0_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART0_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART0_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART0_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART0_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART0_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART0_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART0_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART0_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART0_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART0_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART0_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART0_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART0_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART0_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART0_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART0_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART0_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART0_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART0_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART0_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART0_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART0_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART0_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART0_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART0_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART0_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART0_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART0_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART0_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART0_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART0_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART0_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART0_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART0_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART0_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART0_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART0_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2733. UART0, UART0_UART Registers, Base Address=5230 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART0_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART0_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART0_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART0_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART0_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART0_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART0_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART0_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART1_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART1_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART1_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART1_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h
4h	8	UART1_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART1_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	32	UART1_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART1_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART1_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h
8h	8	UART1_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART1_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART1_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART1_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART1_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
10h	32	UART1_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART1_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART1_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART1_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART1_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART1_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART1_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART1_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART1_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART1_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART1_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART1_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	32	UART1_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h
28h	32	UART1_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART1_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
2Ch	32	UART1_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART1_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART1_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART1_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h
34h	32	UART1_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART1_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART1_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h
38h	32	UART1_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART1_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART1_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART1_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h
48h	32	UART1_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART1_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART1_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART1_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART1_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART1_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART1_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART1_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART1_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART1_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART1_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART1_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART1_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART1_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART1_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART1_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART1_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART1_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART1_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2734. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART1_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART1_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART1_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART1_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART1_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART1_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART1_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART1_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART1_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART1_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART1_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART1_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART1_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART1_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART1_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART1_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART1_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART1_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART1_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART1_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART1_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART1_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART1_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART1_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART1_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART1_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART1_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART1_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART1_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART1_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART1_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART1_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART1_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART1_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART1_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART1_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART1_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART1_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART1_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART1_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART1_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART1_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART1_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART1_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART1_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART1_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART1_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART1_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART1_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART1_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART1_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART1_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART1_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART1_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART1_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART1_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART1_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART1_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART1_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART1_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART1_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART1_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART1_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART1_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART1_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART1_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART1_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2735. UART1, UART1_UART Registers, Base Address=5230 1000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART1_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART1_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART1_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART1_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART1_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART1_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART1_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART1_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART2_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART2_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART2_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART2_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h
4h	8	UART2_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART2_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	32	UART2_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART2_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART2_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h
8h	8	UART2_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART2_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART2_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART2_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART2_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
10h	32	UART2_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART2_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART2_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART2_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART2_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART2_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART2_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART2_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART2_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART2_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART2_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART2_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	32	UART2_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h
28h	32	UART2_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART2_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
2Ch	32	UART2_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART2_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART2_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART2_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h
34h	32	UART2_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART2_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART2_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h
38h	32	UART2_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART2_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART2_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART2_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h
48h	32	UART2_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART2_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART2_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART2_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART2_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART2_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART2_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART2_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART2_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART2_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART2_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART2_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART2_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART2_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART2_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART2_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART2_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART2_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART2_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2736. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART2_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART2_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART2_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART2_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART2_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART2_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART2_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART2_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART2_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART2_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART2_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART2_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART2_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART2_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART2_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART2_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART2_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART2_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART2_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART2_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART2_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART2_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART2_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART2_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART2_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART2_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART2_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART2_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART2_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART2_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART2_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART2_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART2_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART2_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART2_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART2_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART2_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART2_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART2_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART2_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART2_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART2_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART2_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART2_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART2_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART2_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART2_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART2_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART2_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART2_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART2_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART2_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART2_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART2_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART2_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART2_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART2_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART2_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART2_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART2_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART2_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART2_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART2_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART2_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART2_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART2_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART2_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2737. UART2, UART2_UART Registers, Base Address=5230 2000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART2_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART2_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART2_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART2_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART2_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART2_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART2_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART2_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART3_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART3_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART3_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART3_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h
4h	8	UART3_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART3_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	32	UART3_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART3_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART3_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h
8h	8	UART3_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART3_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART3_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART3_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART3_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
10h	32	UART3_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART3_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART3_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART3_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART3_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART3_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART3_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART3_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART3_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART3_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART3_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART3_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	32	UART3_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h
28h	32	UART3_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART3_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
2Ch	32	UART3_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART3_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART3_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART3_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h
34h	32	UART3_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART3_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART3_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h
38h	32	UART3_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART3_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART3_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART3_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h
48h	32	UART3_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART3_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART3_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART3_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART3_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART3_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART3_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART3_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART3_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART3_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART3_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART3_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART3_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART3_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART3_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART3_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART3_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART3_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART3_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2738. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART3_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART3_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART3_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART3_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART3_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART3_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART3_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART3_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART3_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART3_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART3_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART3_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART3_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART3_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART3_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART3_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART3_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART3_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART3_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART3_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART3_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART3_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART3_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART3_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART3_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART3_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART3_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART3_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART3_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART3_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART3_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART3_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART3_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART3_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART3_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART3_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART3_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART3_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART3_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART3_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART3_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART3_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART3_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART3_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART3_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART3_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART3_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART3_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART3_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART3_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART3_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART3_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART3_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART3_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART3_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART3_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART3_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART3_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART3_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART3_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART3_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART3_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART3_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART3_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART3_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART3_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART3_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2739. UART3, UART3_UART Registers, Base Address=5230 3000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART3_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART3_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART3_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART3_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART3_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART3_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART3_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART3_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART4_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART4_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART4_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART4_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h
4h	8	UART4_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART4_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	32	UART4_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART4_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART4_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h
8h	8	UART4_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART4_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART4_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART4_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART4_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
10h	32	UART4_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART4_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART4_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART4_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART4_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART4_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART4_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART4_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART4_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART4_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART4_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART4_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	32	UART4_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h
28h	32	UART4_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART4_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
2Ch	32	UART4_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART4_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART4_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART4_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h
34h	32	UART4_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART4_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART4_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h
38h	32	UART4_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART4_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART4_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART4_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h
48h	32	UART4_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART4_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART4_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART4_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART4_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART4_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART4_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART4_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART4_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART4_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART4_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART4_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART4_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART4_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART4_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART4_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART4_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART4_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART4_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2740. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART4_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART4_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART4_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART4_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART4_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART4_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART4_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART4_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART4_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART4_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART4_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART4_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART4_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART4_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART4_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART4_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART4_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART4_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART4_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART4_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART4_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART4_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART4_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART4_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART4_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART4_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART4_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART4_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART4_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART4_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART4_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART4_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART4_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART4_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART4_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART4_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART4_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART4_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART4_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART4_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART4_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART4_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART4_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART4_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART4_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART4_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART4_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART4_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART4_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART4_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART4_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART4_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART4_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART4_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART4_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART4_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART4_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART4_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART4_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART4_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART4_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART4_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART4_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART4_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART4_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART4_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART4_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2741. UART4, UART4_UART Registers, Base Address=5230 4000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART4_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART4_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART4_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART4_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART4_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART4_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART4_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART4_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	8	UART5_DLL	Divisor Latches Low Register	5230 0000h	5230 1000h	5230 2000h
0h	32	UART5_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 0000h	5230 1000h	5230 2000h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART5_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 0000h	5230 1000h	5230 2000h
4h	8	UART5_DLH	Divisor Latches High Register	5230 0004h	5230 1004h	5230 2004h
4h	8	UART5_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 0004h	5230 1004h	5230 2004h
4h	8	UART5_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 0004h	5230 1004h	5230 2004h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
4h	32	UART5_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 0004h	5230 1004h	5230 2004h
8h	8	UART5_EFR	Enhanced Feature Register	5230 0008h	5230 1008h	5230 2008h
8h	32	UART5_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 0008h	5230 1008h	5230 2008h
8h	8	UART5_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	8	UART5_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
8h	32	UART5_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART5_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 000Ch	5230 100Ch	5230 200Ch
10h	8	UART5_XON1_ADDR1	XON1/ADDR1 Register	5230 0010h	5230 1010h	5230 2010h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
10h	32	UART5_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 0010h	5230 1010h	5230 2010h
14h	8	UART5_XON2_ADDR2	XON2/ADDR2 Register	5230 0014h	5230 1014h	5230 2014h
14h	8	UART5_LSR_CIR	RO	5230 0014h	5230 1014h	5230 2014h
14h	8	UART5_LSR_IRDA	RO	5230 0014h	5230 1014h	5230 2014h
14h	32	UART5_LSR_UART	RO	5230 0014h	5230 1014h	5230 2014h
18h	8	UART5_TCR	Transmission Control Register	5230 0018h	5230 1018h	5230 2018h
18h	8	UART5_XOFF1	XOFF1 Register	5230 0018h	5230 1018h	5230 2018h
18h	32	UART5_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 0018h	5230 1018h	5230 2018h
1Ch	8	UART5_TLR	Trigger Level Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	8	UART5_XOFF2	XOFF2 Register	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART5_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART5_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 0020h	5230 1020h	5230 2020h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	32	UART5_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 0024h	5230 1024h	5230 2024h
28h	32	UART5_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 0028h	5230 1028h	5230 2028h
28h	32	UART5_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 0028h	5230 1028h	5230 2028h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
2Ch	32	UART5_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART5_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART5_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0030h	5230 1030h	5230 2030h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
30h	32	UART5_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0030h	5230 1030h	5230 2030h
34h	32	UART5_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 0034h	5230 1034h	5230 2034h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
34h	32	UART5_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 0034h	5230 1034h	5230 2034h
38h	8	UART5_UASR	UART Autobauding Status Register	5230 0038h	5230 1038h	5230 2038h
38h	32	UART5_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART5_ACREG	IR-IrDA and IR-CIR modes only.	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART5_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 0040h	5230 1040h	5230 2040h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART5_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 0044h	5230 1044h	5230 2044h
48h	32	UART5_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 0048h	5230 1048h	5230 2048h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
50h	32	UART5_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 0050h	5230 1050h	5230 2050h
54h	32	UART5_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 0054h	5230 1054h	5230 2054h
58h	32	UART5_SYSS	RO	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART5_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 005Ch	5230 105Ch	5230 205Ch

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
60h	32	UART5_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 0060h	5230 1060h	5230 2060h
64h	32	UART5_RXFIFO_LVL	Level of the RX FIFO	5230 0064h	5230 1064h	5230 2064h
68h	32	UART5_TXFIFO_LVL	Level of the TX FIFO	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART5_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART5_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 0070h	5230 1070h	5230 2070h
74h	32	UART5_FREQ_SEL	Sample per bit value selector	5230 0074h	5230 1074h	5230 2074h
78h	32	UART5_ABAUD_1ST_CHAR	Unused	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART5_BAUD_2ND_CHAR	Unused	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART5_MDR3	Mode definition register 3.	5230 0080h	5230 1080h	5230 2080h
84h	32	UART5_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 0084h	5230 1084h	5230 2084h
88h	32	UART5_MDR4	Mode definition register 4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART5_EFR2	Enhanced Features Register 2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART5_ECR	Enhanced Control register	5230 0090h	5230 1090h	5230 2090h
94h	32	UART5_TIMEGUARD	Timeguard	5230 0094h	5230 1094h	5230 2094h

Table 4-2742. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
98h	32	UART5_TIMEOUTL	Timeout lower byte	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART5_TIMEOUTH	Timeout higher byte	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART5_SCCR	Smartcard (ISO7816) mode Control Register	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART5_ETHR	Extended Transmit Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART5_ERHR	Extended Receive Holding Register	5230 00A4h	5230 10A4h	5230 20A4h
A8h	8	UART5_MAR	Multidrop Address Register	5230 00A8h	5230 10A8h	5230 20A8h
ACh	8	UART5_MMR	Multidrop Mask Register	5230 00ACh	5230 10ACh	5230 20ACh
B0h	8	UART5_MBR	Multidrop Broadcast Address Register	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	8	UART5_DLL	Divisor Latches Low Register	5230 3000h	5230 4000h	5230 5000h
0h	32	UART5_RHR	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.	5230 3000h	5230 4000h	5230 5000h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART5_THR	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.	5230 3000h	5230 4000h	5230 5000h
4h	8	UART5_DLH	Divisor Latches High Register	5230 3004h	5230 4004h	5230 5004h
4h	8	UART5_IER_CIR	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually.	5230 3004h	5230 4004h	5230 5004h
4h	8	UART5_IER_IRDA	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.	5230 3004h	5230 4004h	5230 5004h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
4h	32	UART5_IER_UART	The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/ RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.	5230 3004h	5230 4004h	5230 5004h
8h	8	UART5_EFR	Enhanced Feature Register	5230 3008h	5230 4008h	5230 5008h
8h	32	UART5_FCR	Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1	5230 3008h	5230 4008h	5230 5008h
8h	8	UART5_IIR_CIR	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	8	UART5_IIR_IRDA	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
8h	32	UART5_IIR_UART	The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART5_LCR	LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.	5230 300Ch	5230 400Ch	5230 500Ch
10h	8	UART5_XON1_ADDR1	XON1/ADDR1 Register	5230 3010h	5230 4010h	5230 5010h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART5_MCR	MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.	5230 3010h	5230 4010h	5230 5010h
14h	8	UART5_XON2_ADDR2	XON2/ADDR2 Register	5230 3014h	5230 4014h	5230 5014h
14h	8	UART5_LSR_CIR	RO	5230 3014h	5230 4014h	5230 5014h
14h	8	UART5_LSR_IRDA	RO	5230 3014h	5230 4014h	5230 5014h
14h	32	UART5_LSR_UART	RO	5230 3014h	5230 4014h	5230 5014h
18h	8	UART5_TCR	Transmission Control Register	5230 3018h	5230 4018h	5230 5018h
18h	8	UART5_XOFF1	XOFF1 Register	5230 3018h	5230 4018h	5230 5018h
18h	32	UART5_MSR	This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.	5230 3018h	5230 4018h	5230 5018h
1Ch	8	UART5_TLR	Trigger Level Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	8	UART5_XOFF2	XOFF2 Register	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART5_SPR	This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART5_MDR1	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to	5230 3020h	5230 4020h	5230 5020h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
24h	32	UART5_MDR2	IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.	5230 3024h	5230 4024h	5230 5024h
28h	32	UART5_TXFLL	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 3028h	5230 4028h	5230 5028h
28h	32	UART5_SFLSR	IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).	5230 3028h	5230 4028h	5230 5028h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
2Ch	32	UART5_TXFLH	IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART5_RESUME	IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/ reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART5_RXFLL	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3030h	5230 4030h	5230 5030h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
30h	32	UART5_SFREGL	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3030h	5230 4030h	5230 5030h
34h	32	UART5_RXFLH	IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).	5230 3034h	5230 4034h	5230 5034h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
34h	32	UART5_SFREGH	IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.	5230 3034h	5230 4034h	5230 5034h
38h	8	UART5_UASR	UART Autobauding Status Register	5230 3038h	5230 4038h	5230 5038h
38h	32	UART5_BLR	IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART5_ACREG	IR-IrDA and IR-CIR modes only.	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART5_SCR	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.	5230 3040h	5230 4040h	5230 5040h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
44h	32	UART5_SSR	Note: Bit 1 is reset only when SCR[4] is reset to 0.	5230 3044h	5230 4044h	5230 5044h
48h	32	UART5_EBLR	IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to	5230 3048h	5230 4048h	5230 5048h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
50h	32	UART5_MVR	The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8	5230 3050h	5230 4050h	5230 5050h
54h	32	UART5_SYSC	The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.	5230 3054h	5230 4054h	5230 5054h
58h	32	UART5_SYSS	RO	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART5_WER	The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.	5230 305Ch	5230 405Ch	5230 505Ch

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
60h	32	UART5_CFPS	Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.	5230 3060h	5230 4060h	5230 5060h
64h	32	UART5_RXFIFO_LVL	Level of the RX FIFO	5230 3064h	5230 4064h	5230 5064h
68h	32	UART5_TXFIFO_LVL	Level of the TX FIFO	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART5_IER2	Enables RX/TX FIFOs empty corresponding interrupts.	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART5_ISR2	Status of RX/TX FIFOs empty corresponding interrupts.	5230 3070h	5230 4070h	5230 5070h
74h	32	UART5_FREQ_SEL	Sample per bit value selector	5230 3074h	5230 4074h	5230 5074h
78h	32	UART5_ABAUD_1ST_CHAR	Unused	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART5_BAUD_2ND_CHAR	Unused	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART5_MDR3	Mode definition register 3.	5230 3080h	5230 4080h	5230 5080h
84h	32	UART5_TX_DMA_THRESHOLD	Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.	5230 3084h	5230 4084h	5230 5084h
88h	32	UART5_MDR4	Mode definition register 4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART5_EFR2	Enhanced Features Register 2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART5_ECR	Enhanced Control register	5230 3090h	5230 4090h	5230 5090h
94h	32	UART5_TIMEGUARD	Timeguard	5230 3094h	5230 4094h	5230 5094h

Table 4-2743. UART5, UART5_UART Registers, Base Address=5230 5000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
98h	32	UART5_TIMEOUTL	Timeout lower byte	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART5_TIMEOUTH	Timeout higher byte	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART5_SCCR	Smartcard (ISO7816) mode Control Register	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART5_ETHR	Extended Transmit Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART5_ERHR	Extended Receive Holding Register	5230 30A4h	5230 40A4h	5230 50A4h
A8h	8	UART5_MAR	Multidrop Address Register	5230 30A8h	5230 40A8h	5230 50A8h
ACh	8	UART5_MMR	Multidrop Mask Register	5230 30ACh	5230 40ACh	5230 50ACh
B0h	8	UART5_MBR	Multidrop Broadcast Address Register	5230 30B0h	5230 40B0h	5230 50B0h

4.29.1 UART0_DLL Register (Offset = 0h) [reset = h]

Short Description: Divisor Latches Low Register

Long Description:

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Table 4-2744. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1305. UART0_DLL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CLOCK_LSB							
RW							
0							

Access Types Legend

Table 4-2745. DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	CLOCK_LSB	RW	0h	Used to store the 8-bit LSB divisor value

4.29.2 UART0_RHR Register (Offset = 0h) [reset = h]

Short Description: The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character. Note: If an overflow occurs the data in the RHR is not overwritten.

Long Description:

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Table 4-2746. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1306. UART0_RHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RHR							
RO								RO							
0								0							

Access Types Legend

Table 4-2747. RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	RHR	RO	0h	Receive holding register

4.29.3 UART0_THR Register (Offset = 0h) [reset = h]

Short Description: The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

Long Description:

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Table 4-2748. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-1307. UART0_THR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								THR							
RO								WO							
0								0							

Access Types Legend

Table 4-2749. THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	THR	WO	0h	TRANSMIT HOLDING REGISTER

4.29.4 UART0_DLH Register (Offset = 4h) [reset = h]

Short Description: Divisor Latches High Register

Long Description:

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Table 4-2750. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1308. UART0_DLH Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
CLOCK_MSB							
RW							
0							

Access Types Legend

Table 4-2751. DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	CLOCK_MSB	RW	0h	Used to store the 8-bit MSB divisor value

4.29.5 UART0_IER_CIR Register (Offset = 4h) [reset = h]

Short Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

Long Description:

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Table 4-2752. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1309. UART0_IER_CIR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
RW		RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0

Access Types Legend

Table 4-2753. IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 6	NOT_USED2	RW	0h	Not Defined
5	TX_STATUS_IT	RW	0h	Not Defined 0 | TX_STATUS_IT_VALUE_0Disables the TX status interrupt. 1 | TX_STATUS_IT_VALUE_1Enables the TX status interrupt.
4	NOT_USED1	RW	0h	Not Defined
3	RX_OVERRUN_IT	RW	0h	Not Defined 0 | RX_OVERRUN_IT_VALUE_0Disables the RX overrun interrupt. 1 | RX_OVERRUN_IT_VALUE_1Enables the RX overrun interrupt.
2	RX_STOP_IT	RW	0h	Not Defined 0 | RX_STOP_IT_VALUE_0Disables the receive stop interrupt. 1 | RX_STOP_IT_VALUE_1Enables the receive stop interrupt.
1	THR_IT	RW	0h	Not Defined 0 | THR_IT_VALUE_0Disables the THR interrupt. 1 | THR_IT_VALUE_1Enables the THR interrupt.
0	RHR_IT	RW	0h	Not Defined 0 | RHR_IT_VALUE_0Disables the RHR interrupt. 1 | RHR_IT_VALUE_1Enables the RHR interrupt.

4.29.6 UART0_IER_IRDA Register (Offset = 4h) [reset = h]

Short Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

Long Description:

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Table 4-2754. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1310. UART0_IER_IRDA Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2755. IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EOF_IT	RW	0h	Not Defined 0 | EOF_IT_VALUE_0Disables the received EOF interrupt. 1 | EOF_IT_VALUE_1Enables the received EOF interrupt.
6	LINE_STS_IT	RW	0h	Not Defined 0 | LINE_STS_IT_VALUE_0Disables the receiver line status interrupt. 1 | LINE_STS_IT_VALUE_1Enables the receiver line status interrupt.
5	TX_STATUS_IT	RW	0h	Not Defined 0 | TX_STATUS_IT_VALUE_0Disables the TX status interrupt. 1 | TX_STATUS_IT_VALUE_1Enables the TX status interrupt.
4	STS_FIFO_TRIG_IT	RW	0h	Not Defined 0 | STS_FIFO_TRIG_IT_VALUE_0Disables the status FIFO trigger level interrupt. 1 | STS_FIFO_TRIG_IT_VALUE_1Enables the status FIFO trigger level interrupt.
3	RX_OVERRUN_IT	RW	0h	Not Defined 0 | RX_OVERRUN_IT_VALUE_0Disables the RX overrun interrupt. 1 | RX_OVERRUN_IT_VALUE_1Enables the RX overrun interrupt.
2	LAST_RX_BYTE_IT	RW	0h	Not Defined 0 | LAST_RX_BYTE_IT_VALUE_0Disables the last byte of frame in RX FIFO interrupt. 1 | LAST_RX_BYTE_IT_VALUE_1Enables the last byte of frame in RX FIFO interrupt.
1	THR_IT	RW	0h	Not Defined 0 | THR_IT_VALUE_0Disables the THR interrupt. 1 | THR_IT_VALUE_1Enables the THR interrupt.
0	RHR_IT	RW	0h	Not Defined 0 | RHR_IT_VALUE_0Disables the RHR interrupt. 1 | RHR_IT_VALUE_1Enables the RHR interrupt.

4.29.7 UART0_IER_UART Register (Offset = 4h) [reset = h]

Short Description: The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

Long Description:

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Table 4-2756. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-1311. UART0_IER_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2757. IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	RO		Not Defined
7	CTS_IT	RW	0h	Not Defined 0 | CTS_IT_VALUE_0Disables the CTS* interrupt 1 | CTS_IT_VALUE_1Enables the CTS* interrupt
6	RTS_IT	RW	0h	Not Defined 0 | RTS_IT_VALUE_0Disables the RTS* interrupt 1 | RTS_IT_VALUE_1Enables the RTS* interrupt
5	XOFF_IT	RW	0h	Not Defined 0 | XOFF_IT_VALUE_0Disables the XOFF interrupt 1 | XOFF_IT_VALUE_1Enables the XOFF interrupt
4	SLEEP_MODE	RW	0h	Not Defined 0 | SLEEP_MODE_VALUE_0Disables sleep mode 1 | SLEEP_MODE_VALUE_1Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	RW	0h	Not Defined 0 | MODEM_STS_IT_VALUE_0Disables the modem status register interrupt 1 | MODEM_STS_IT_VALUE_1Enables the modem status register interrupt
2	LINE_STS_IT	RW	0h	Not Defined 0 | LINE_STS_IT_U_VALUE_0Disables the receiver line status interrupt 1 | LINE_STS_IT_U_VALUE_1Enables the receiver line status interrupt
1	THR_IT	RW	0h	Not Defined 0 | THR_IT_VALUE_0Disables the THR interrupt 1 | THR_IT_VALUE_1Enables the THR interrupt
0	RHR_IT	RW	0h	Not Defined 0 | RHR_IT_VALUE_0Disables the RHR interrupt and time out interrupt. 1 | RHR_IT_VALUE_1Enables the RHR interrupt and time out interrupt.

4.29.8 UART0_EFR Register (Offset = 8h) [reset = h]

Short Description: Enhanced Feature Register

Long Description:

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Table 4-2758. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1312. UART0_EFR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
RW	RW	RW	RW	RW			
0	0	0	0	0			

Access Types Legend

Table 4-2759. EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUTO_CTS_EN	RW	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive).
6	AUTO_RTS_EN	RW	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached.
5	SPECIAL_CHAR_DETECT	RW	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected.
4	ENHANCED_EN	RW	0h	Enhanced functions write enable bit. 0: Disables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7.
3 - 0	SW_FLOW_CONTROL	RW	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options

4.29.9 UART0_FCR Register (Offset = 8h) [reset = h]

Short Description: Notes: Bits 4 and 5 can only be written to when EFR[4] = 1 Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0) See Table 31 for FCR[5:4] setting restriction when SCR[6]=1 See Table 32 for FCR[7:6] setting restriction when SCR[7]=1

Long Description:

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Table 4-2760. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1313. UART0_FCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
RO								WO		WO		WO	WO	WO	WO
0								0		0		0	0	0	0

Access Types Legend

Table 4-2761. FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 6	RX_FIFO_TRIG	WO	0h	Sets the trigger level for the RX FIFO:If SCR[7] = 0 and TLR[7:4] = 0000:00: 8 characters01: 16 characters10: 56 characters11: 60 charactersIf SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered.If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1.
5 - 4	TX_FIFO_TRIG	WO	0h	Sets the trigger level for the TX FIFO:If SCR[6] = 0 and TLR[3:0] = 0000:00: 8 spaces01: 16 spaces10: 32 spaces11: 56 spacesIf SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered.If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1
3	DMA_MODE	WO	0h	This register is considered if SCR[0] = 0. Write0 | DMA_MODE_VALUE_0DMA_MODE 0 (No DMA) Write1 | DMA_MODE_VALUE_1DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	WO	0h	Not Defined Write0 | TX_FIFO_CLEAR_VALUE_0No change Write1 | TX_FIFO_CLEAR_VALUE_1Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	WO	0h	Not Defined Write0 | RX_FIFO_CLEAR_VALUE_0No change Write1 | RX_FIFO_CLEAR_VALUE_1Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.

Table 4-2761. FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FIFO_EN	WO	0h	Not Defined Write0 | FIFO_EN_VALUE_0Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs. Write1 | FIFO_EN_VALUE_1: Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

4.29.10 UART0_IIR_CIR Register (Offset = 8h) [reset = h]

Short Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Long Description:

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Table 4-2762. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1314. UART0_IIR_CIR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE		RO	NONE	RO	RO	RO	RO
0		0	0	0	0	0	0

Access Types Legend

Table 4-2763. IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	TX_STATUS_IT	RO	0h	Not Defined Read0 | TX_STATUS_IT_VALUE_0TX status interrupt inactive Read1 | TX_STATUS_IT_VALUE_1TX status interrupt active
	RESERVED	NONE		Reserved
3	RX_OE_IT	RO	0h	Not Defined Read0 | RX_OE_IT_VALUE_0RX overrun interrupt inactive Read1 | RX_OE_IT_VALUE_1RX overrun interrupt active
2	RX_STOP_IT	RO	0h	Not Defined Read0 | RX_STOP_IT_VALUE_0Receive stop interrupt inactive Read1 | RX_STOP_IT_VALUE_1Receive stop interrupt active
1	THR_IT	RO	0h	Not Defined Read0 | THR_IT_VALUE_0THR interrupt inactive Read1 | THR_IT_VALUE_1THR interrupt active
0	RHR_IT	RO	0h	Not Defined Read0 | RHR_IT_VALUE_0RHR interrupt inactive Read1 | RHR_IT_VALUE_1RHR interrupt active

4.29.11 UART0_IIR_IRDA Register (Offset = 8h) [reset = h]

Short Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Long Description:

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Table 4-2764. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1315. UART0_IIR_IRDA Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2765. IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EOF_IT	RO	0h	Not Defined Read0 | EOF_IT_VALUE_0Received EOF interrupt inactive Read1 | EOF_IT_VALUE_1Received EOF interrupt active
6	LINE_STS_IT	RO	0h	Not Defined Read0 | LINE_STS_IT_VALUE_0Receiver line status interrupt inactive Read1 | LINE_STS_IT_VALUE_1Receiver line status interrupt active
5	TX_STATUS_IT	RO	0h	Not Defined Read0 | TX_STATUS_IT_VALUE_0TX status interrupt inactive Read1 | TX_STATUS_IT_VALUE_1TX status interrupt active
4	STS_FIFO_IT	RO	0h	Not Defined Read0 | STS_FIFO_IT_VALUE_0Status FIFO trigger level interrupt inactive Read1 | STS_FIFO_IT_VALUE_1Status FIFO trigger level interrupt active
3	RX_OE_IT	RO	0h	Not Defined Read0 | RX_OE_IT_VALUE_0RX overrun interrupt inactive Read1 | RX_OE_IT_VALUE_1RX overrun interrupt active
2	RX_FIFO_LAST_BYTE_IT	RO	0h	Not Defined Read0 | RX_FIFO_LAST_BYTE_IT_VALUE_0Last byte of frame in RX FIFO interrupt inactive Read1 | RX_FIFO_LAST_BYTE_IT_VALUE_1Last byte of frame in RX FIFO interrupt active
1	THR_IT	RO	0h	Not Defined Read0 | THR_IT_VALUE_0THR interrupt inactive Read1 | THR_IT_VALUE_1THR interrupt active
0	RHR_IT	RO	0h	Not Defined Read0 | RHR_IT_VALUE_0RHR interrupt inactive Read1 | RHR_IT_VALUE_1RHR interrupt active

4.29.12 UART0_IIR_UART Register (Offset = 8h) [reset = h]

Short Description: The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Long Description:

Return to Summary Table

Table 4-2766. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-1316. UART0_IIR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FCR_MIRROR		IT_TYPE					IT_PENDING
RO								RO		RO					RO
0								0		0					1

Access Types Legend

Table 4-2767. IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 6	FCR_MIRROR	RO	0h	Mirror the contents of FCR[0] on both bits.
5 - 1	IT_TYPE	RO	0h	Not Defined Read0x00 | IT_TYPE_VALUE_0Modem Interrupt. Priority=4 Read0x01 | IT_TYPE_VALUE_1THR interrupt. Priority=3 Read0x02 | IT_TYPE_VALUE_2RHR interrupt. Priority=2 Read0x03 | IT_TYPE_VALUE_3Receiver line status error. Priority=3 Read0x06 | IT_TYPE_VALUE_6Rx timeout. Priority=2 Read0x08 | IT_TYPE_VALUE_8Xoff/Special character. Priority=5 Read0x10 | IT_TYPE_VALUE_10CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6
0	IT_PENDING	RO	1h	Not Defined Read0 | IT_PENDING_VALUE_0An interrupt is pending Read1 | IT_PENDING_VALUE_1No interrupt is pending

4.29.13 UART0_LCR Register (Offset = Ch) [reset = h]

Short Description: LCR[6:0] define parameters of the transmission and reception.Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

Long Description:

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Table 4-2768. Instance Table

Instance Name	Physical Address
UART0	5230 000Ch
UART1	5230 100Ch
UART2	5230 200Ch
UART3	5230 300Ch
UART4	5230 400Ch
UART5	5230 500Ch

Figure 4-1317. UART0_LCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								DIV_EN	BREAK_EN	PARITY_TYPE2	PARITY_TYPE1	PARITY_EN	NB_STOP	CHAR_LENGTH	
RO								RW	RW	RW	RW	RW	RW	RW	
0								0	0	0	0	0	0	0	

Access Types Legend

Table 4-2769. LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	DIV_EN	RW	0h	Not Defined 0 | DIV_EN_VALUE_0Normal operating condition 1 | DIV_EN_VALUE_1Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)
6	BREAK_EN	RW	0h	Break control bit. 0 | BREAK_EN_VALUE_0Normal operating condition. 1 | BREAK_EN_VALUE_1Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	RW	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.
4	PARITY_TYPE1	RW	0h	Not Defined 0 | PARITY_TYPE1_VALUE_0Odd parity is generated (if LCR[3] = 1) 1 | PARITY_TYPE1_VALUE_1Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	RW	0h	Not Defined 0 | PARITY_EN_VALUE_0No parity 1 | PARITY_EN_VALUE_1A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	RW	0h	Specifies the number of stop bits: 0 | NB_STOP_VALUE_01 stop bits (word length = 5, 6, 7, 8) 1 | NB_STOP_VALUE_11.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1 - 0	CHAR_LENGTH	RW	0h	Specifies the word length to be transmitted or received. 0x0 | CHAR_LENGTH_VALUE_05 bits 0x1 | CHAR_LENGTH_VALUE_16 bits 0x2 | CHAR_LENGTH_VALUE_27 bits 0x3 | CHAR_LENGTH_VALUE_38 bits

4.29.14 UART0_XON1_ADDR1 Register (Offset = 10h) [reset = h]

Short Description: XON1/ADDR1 Register

Long Description:

Return to Summary Table

Table 4-2770. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-1318. UART0_XON1_ADDR1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
XON_WORD1							
RW							
0							

Access Types Legend

Table 4-2771. XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	XON_WORD1	RW	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes.

4.29.15 UART0_MCR Register (Offset = 10h) [reset = h]

Short Description: MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

Long Description:

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Table 4-2772. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-1319. UART0_MCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
RO								RO	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2773. MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	RESERVED	RO		Not Defined
6	TCR_TLR	RW	0h	Not Defined 0 | TCR_TLR_VALUE_0No action 1 | TCR_TLR_VALUE_1Enables access to the TCR and TLR registers.
5	XON_EN	RW	0h	Not Defined 0 | XON_EN_VALUE_0Disable 'XON any' function 1 | XON_EN_VALUE_1Enable 'XON any' function
4	LOOPBACK_EN	RW	0h	Not Defined 0 | LOOPBACK_EN_VALUE_0Normal operating mode 1 | LOOPBACK_EN_VALUE_1Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally
3	CD_STS_CH	RW	0h	Not Defined 0 | CD_STS_CH_VALUE_0In loopback forces DCD* input high and IRQ outputs to inactive state. 1 | CD_STS_CH_VALUE_1In loopback forces DCD* input low and IRQ outputs to inactive state.
2	RI_STS_CH	RW	0h	Not Defined 0 | RI_STS_CH_VALUE_0In loopback forces RI* input high. 1 | RI_STS_CH_VALUE_1In loopback forces RI* input low.
1	RTS	RW	0h	In loop back controls MSR[4].If auto-RTS is enabled the RTS* output is controlled by hardware flow control. 0 | RTS_VALUE_0Force RTS* output to inactive (high). 1 | RTS_VALUE_1Force RTS* output to active (low).
0	DTR	RW	0h	Not Defined 0 | DTR_VALUE_0Force DTR* output to inactive (high). 1 | DTR_VALUE_1Force DTR* output to active (low).

4.29.16 UART0_XON2_ADDR2 Register (Offset = 14h) [reset = h]

Short Description: XON2/ADDR2 Register

Long Description:

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Table 4-2774. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1320. UART0_XON2_ADDR2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
XON_WORD2							
RW							
0							

Access Types Legend

Table 4-2775. XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	XON_WORD2	RW	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes.

4.29.17 UART0_LSR_CIR Register (Offset = 14h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 4-2776. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1321. UART0_LSR_CIR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
RO	RO	RO	NONE				RO
1	0	0	0				1

Access Types Legend

Table 4-2777. LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THR_EMPTY	RO	1h	Not Defined Read0 | THR_EMPTY_VALUE_0Transmit holding register (TX FIFO) is not empty Read1 | THR_EMPTY_VALUE_1Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	RESERVED	RO		Not Defined
5	RX_STOP	RO	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register Read0 | RX_STOP_VALUE_0Reception is on going or waiting for a new frame Read1 | RX_STOP_VALUE_1Reception is completed
	RESERVED	NONE		Reserved
0	RX_FIFO_E	RO	1h	Not Defined Read0 | RX_FIFO_E_VALUE_0No data in the receive FIFO Read1 | RX_FIFO_E_VALUE_1At least one data character in the RX FIFO

4.29.18 UART0_LSR_IRDA Register (Offset = 14h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 4-2778. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1322. UART0_LSR_IRDA Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
RO	RO	RO	RO	RO	RO	RO	RO
1	0	0	0	0	0	1	1

Access Types Legend

Table 4-2779. LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THR_EMPTY	RO	1h	Not Defined Read0 | THR_EMPTY_VALUE_0Transmit holding register (TX FIFO) is not empty Read1 | THR_EMPTY_VALUE_1Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	RO	0h	Not Defined Read0 | STS_FIFO_FULL_VALUE_0Status FIFO not full Read1 | STS_FIFO_FULL_VALUE_1Status FIFO full
5	RX_LAST_BYTE	RO	0h	Not Defined Read0 | RX_LAST_BYTE_VALUE_0The RX FIFO (RHR) does not contain the last byte of the frame to be read Read1 | RX_LAST_BYTE_VALUE_1The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register
4	FRAME_TOO_LONG	RO	0h	Not Defined Read0 | FRAME_TOO_LONG_VALUE_0No frame-too-long error in frame Read1 | FRAME_TOO_LONG_VALUE_1Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	RO	0h	Not Defined Read0 | ABORT_VALUE_0No abort pattern error in frame Read1 | ABORT_VALUE_1Abort pattern is received. SIR , MIR: Abort pattern. FIR: Illegal symbol
2	CRC	RO	0h	Not Defined Read0 | CRC_VALUE_0No CRC error in frame Read1 | CRC_VALUE_1CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	RO	1h	Not Defined Read0 | STS_FIFO_E_VALUE_0Status FIFO not empty Read1 | STS_FIFO_E_VALUE_1Status FIFO empty
0	RX_FIFO_E	RO	1h	Not Defined Read0 | RX_FIFO_E_VALUE_0No data in the receive FIFO Read1 | RX_FIFO_E_VALUE_1At least one data character in the RX FIFO

4.29.19 UART0_LSR_UART Register (Offset = 14h) [reset = h]

Short Description: RO

Long Description:

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Table 4-2780. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-1323. UART0_LSR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	1	1	0	0	0	0	0

Access Types Legend

Table 4-2781. LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	RX_FIFO_STS	RO	0h	Not Defined Read0 | RX_FIFO_STS_VALUE_0Normal operation Read1 | RX_FIFO_STS_VALUE_1At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	RO	1h	Not Defined Read0 | TX_SR_E_VALUE_0Transmitter hold (TX FIFO) and shift registers are not empty. Read1 | TX_SR_E_VALUE_1Transmitter hold (TX FIFO) and shift registers are empty
5	TX_FIFO_E	RO	1h	Not Defined Read0 | TX_FIFO_E_VALUE_0Transmit hold register (TX FIFO) is not empty Read1 | TX_FIFO_E_VALUE_1Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.
4	RX_BI	RO	0h	Not Defined Read0 | RX_BI_VALUE_0No break condition Read1 | RX_BI_VALUE_1A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	RO	0h	Not Defined Read0 | RX_FE_VALUE_0No framing error in data being read from RX FIFO. Read1 | RX_FE_VALUE_1Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	RO	0h	Not Defined Read0 | RX_PE_VALUE_0No parity error in data being read from RX FIFO. Read1 | RX_PE_VALUE_1Parity error in data being read from RX FIFO

Table 4-2781. LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_OE	RO	0h	Not Defined Read0 | RX_OE_VALUE_0No overrun error Read1 | RX_OE_VALUE_1Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.
0	RX_FIFO_E	RO	0h	Not Defined Read0 | RX_FIFO_E_VALUE_0No data in the receive FIFO Read1 | RX_FIFO_E_VALUE_1At least one data character in the RX FIFO

4.29.20 UART0_TCR Register (Offset = 18h) [reset = h]

Short Description: Transmission Control Register

Long Description:

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Table 4-2782. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1324. UART0_TCR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
RW				RW			
0				1111			

Access Types Legend

Table 4-2783. TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	RX_FIFO_TRIG_START	RW	0h	RX FIFO trigger level to RESTORE transmission (0 - 60)
3 - 0	RX_FIFO_TRIG_HALT	RW	457h	RX FIFO trigger level to HALT transmission (0 - 60)

4.29.21 UART0_XOFF1 Register (Offset = 18h) [reset = h]

Short Description: XOFF1 Register

Long Description:

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Table 4-2784. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1325. UART0_XOFF1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
XOFF_WORD1							
RW							
0							

Access Types Legend

Table 4-2785. XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	XOFF_WORD1	RW	0h	Used to store the 8-bit XOFF1 character in used in UART modes.

4.29.22 UART0_MSR Register (Offset = 18h) [reset = h]

Short Description: This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

Long Description:

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Table 4-2786. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-1326. UART0_MSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2787. MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	NCD_STS	RO	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3]
6	NRI_STS	RO	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2]
5	NDSR_STS	RO	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0]
4	NCTS_STS	RO	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1]
3	DCD_STS	RO	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read.
2	RI_STS	RO	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read.
1	DSR_STS	RO	0h	Not Defined Read1 | DSR_STS_VALUE_1Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read
0	CTS_STS	RO	0h	Not Defined Read1 | CTS_STS_VALUE_1Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.

4.29.23 UART0_TLR Register (Offset = 1Ch) [reset = h]

Short Description: Trigger Level Register

Long Description:

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Table 4-2788. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1327. UART0_TLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
RW				RW			
0				0			

Access Types Legend

Table 4-2789. TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	RX_FIFO_TRIG_DMA	RW	0h	Receive FIFO trigger level
3 - 0	TX_FIFO_TRIG_DMA	RW	0h	Transmit FIFO trigger level

4.29.24 UART0_XOFF2 Register (Offset = 1Ch) [reset = h]

Short Description: XOFF2 Register

Long Description:

Return to Summary Table

Table 4-2790. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1328. UART0_XOFF2 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
XOFF_WORD2							
RW							
0							

Access Types Legend

Table 4-2791. XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	XOFF_WORD2	RW	0h	Used to store the 8-bit XOFF2 character in used in UART modes.

4.29.25 UART0_SPR Register (Offset = 1Ch) [reset = h]

Short Description: This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

Long Description:

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Table 4-2792. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-1329. UART0_SPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SPR_WORD							
RO								RW							
0								0							

Access Types Legend

Table 4-2793. SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	SPR_WORD	RW	0h	Scratchpad register

4.29.26 UART0_MDR1 Register (Offset = 20h) [reset = h]

Short Description: The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to

Long Description:

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Table 4-2794. Instance Table

Instance Name	Physical Address
UART0	5230 0020h
UART1	5230 1020h
UART2	5230 2020h
UART3	5230 3020h
UART4	5230 4020h
UART5	5230 5020h

Figure 4-1330. UART0_MDR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
RO								RW	RW	RW	RW	RW	RW		
0								0	0	0	0	0	111		

Access Types Legend

Table 4-2795. MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	FRAME_END_MODE	RW	0h	IrDA mode only. 0 | FRAME_END_MODE_VALUE_0Frame-length method 1 | FRAME_END_MODE_VALUE_1Set EOT bit method
6	SIP_MODE	RW	0h	MIR/FIR modes only. 0 | SIP_MODE_VALUE_0Manual SIP mode: SIP is generated with the control of ACREG[3] 1 | SIP_MODE_VALUE_1Automatic SIP mode: SIP is generated after each transmission.
5	SCT	RW	0h	Store and control the transmission 0 | SCT_VALUE_0Starts the Infrared transmission as soon as a value is written to THR 1 | SCT_VALUE_1Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	RW	0h	Used to configure the infrared transceiver. 0 | SET_TXIR_VALUE_0No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1 1 | SET_TXIR_VALUE_1TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	RW	0h	Not Defined 0 | IR_SLEEP_VALUE_0IrDA/CIR sleep mode disabled 1 | IR_SLEEP_VALUE_1IrDA/CIR sleep mode enabled

Table 4-2795. MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	MODE_SELECT	RW	6Fh	Not Defined 0x0 | MODE_SELECT_VALUE_0UART 16x mode 0x1 | MODE_SELECT_VALUE_1SIR mode 0x2 | MODE_SELECT_VALUE_2UART 16x auto-baud 0x3 | MODE_SELECT_VALUE_3UART 13x mode 0x4 | MODE_SELECT_VALUE_4MIR mode 0x5 | MODE_SELECT_VALUE_5FIR mode 0x6 | MODE_SELECT_VALUE_6CIR mode 0x7 | MODE_SELECT_VALUE_7Disable (default state)

4.29.27 UART0_MDR2 Register (Offset = 24h) [reset = h]

Short Description: IR-IrDA and IR-CIR modes only.MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

Long Description:

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Table 4-2796. Instance Table

Instance Name	Physical Address
UART0	5230 0024h
UART1	5230 1024h
UART2	5230 2024h
UART3	5230 3024h
UART4	5230 4024h
UART5	5230 5024h

Figure 4-1331. UART0_MDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
RO								RW	RW	RW		RW	RW		RO
0								0	0	0		0	0		0

Access Types Legend

Table 4-2797. MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	SET_TXIR_ALT	RW	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] 0 | SET_TXIR_ALT_VALUE_0Normal mode 1 | SET_TXIR_ALT_VALUE_1Alternate mode for SET_TXIR
6	IRRXINVERT	RW	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. 0 | IRRXINVERT_VALUE_0inversion is performed 1 | IRRXINVERT_VALUE_1No inversion is performed
5 - 4	CIR_PULSE_MODE	RW	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: 0x0 | CIR_PULSE_MODE_VALUE_0Pulse width of 3 from 12 cycles 0x1 | CIR_PULSE_MODE_VALUE_1Pulse width of 4 from 12 cycles 0x2 | CIR_PULSE_MODE_VALUE_2Pulse width of 5 from 12 cycles 0x3 | CIR_PULSE_MODE_VALUE_3Pulse width of 6 from 12 cycles
3	UART_PULSE	RW	0h	UART mode only. Used to allow pulse shaping in UART mode. 0 | UART_PULSE_VALUE_0normal UART mode 1 | UART_PULSE_VALUE_1UART mode with a pulse shaping

Table 4-2797. MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 1	STS_FIFO_TRIG	RW	0h	Only for IR-IRDA mode.Frame Status FIFO Threshold select: 0x0 | STS_FIFO_TRIG_VALUE_01 entry 0x1 | STS_FIFO_TRIG_VALUE_14 entries 0x2 | STS_FIFO_TRIG_VALUE_27 entries 0x3 | STS_FIFO_TRIG_VALUE_38 entries
0	IRTX_UNDERRUN	RO	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : Read0 | IRTX_UNDERRUN_VALUE_0the last bit of the frame has been transmitted successfully without error. Read1 | IRTX_UNDERRUN_VALUE_1an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.

4.29.28 UART0_TXFLL Register (Offset = 28h) [reset = h]

Short Description: IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

Long Description:

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Table 4-2798. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-1332. UART0_TXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								TXFLL							
RO								WO							
0								0							

Access Types Legend

Table 4-2799. TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	TXFLL	WO	0h	LSB register used to specify the frame length

4.29.29 UART0_SFLSR Register (Offset = 28h) [reset = h]

Short Description: IrDA modes only.Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

Long Description:

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Table 4-2800. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-1333. UART0_SFLSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
RO								RO			RO	RO	RO	RO	RO
0								0			0	0	0	0	0

Access Types Legend

Table 4-2801. SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 5	RESERVED5	RO	0h	Not Defined
4	OE_ERROR	RO	0h	Not Defined Read1 | OE_ERROR_VALUE_1Overrun error in RX FIFO when frame at top of RX FIFO was received.
3	FRAME_TOO_LONG_ERROR	RO	0h	Not Defined Read1 | FRAME_TOO_LONG_ERROR_VALUE_1Frame-length too long error in frame at top of RX FIFO.
2	ABORT_DETECT	RO	0h	Not Defined Read1 | ABORT_DETECT_VALUE_1Abort pattern detected in frame at top of RX FIFO
1	CRC_ERROR	RO	0h	Not Defined Read1 | CRC_ERROR_VALUE_1CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO
0	RESERVED0	RO	0h	Not Defined

4.29.30 UART0_TXFLH Register (Offset = 2Ch) [reset = h]

Short Description: IrDA modes only.The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

Long Description:

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Table 4-2802. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-1334. UART0_TXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			TXFLH				
RO								RO			WO				
0								0			0				

Access Types Legend

Table 4-2803. TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 5	RESERVED	RO		Not Defined
4 - 0	TXFLH	WO	0h	MSB register used to specify the frame length

4.29.31 UART0_RESUME Register (Offset = 2Ch) [reset = h]

Short Description: IR-IrDA and IR-CIR modes only.This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

Long Description:

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Table 4-2804. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-1335. UART0_RESUME Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESUME							
RO								RO							
0								0							

Access Types Legend

Table 4-2805. RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	RESUME	RO	0h	Dummy read to restart the TX or RX

4.29.32 UART0_RXFLL Register (Offset = 30h) [reset = h]

Short Description: IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

Long Description:

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Table 4-2806. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-1336. UART0_RXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RXFLL							
RO								WO							
0								0							

Access Types Legend

Table 4-2807. RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	RXFLL	WO	0h	LSB register used to specify the frame length in reception

4.29.33 UART0_SFREGL Register (Offset = 30h) [reset = h]

Short Description: IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

Long Description:

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Table 4-2808. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-1337. UART0_SFREGL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SFREGL							
RO								RO							
0								0							

Access Types Legend

Table 4-2809. SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	SFREGL	RO	0h	LSB part of the frame length

4.29.34 UART0_RXFLH Register (Offset = 34h) [reset = h]

Short Description: IrDA modes only.The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

Long Description:

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Table 4-2810. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-1338. UART0_RXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				RXFLH			
RO								RO				WO			
0								0				0			

Access Types Legend

Table 4-2811. RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 4	RESERVED	RO		Not Defined
3 - 0	RXFLH	WO	0h	MSB register used to specify the frame length in reception

4.29.35 UART0_SFREGH Register (Offset = 34h) [reset = h]

Short Description: IrDA modes only.The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

Long Description:

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Table 4-2812. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-1339. UART0_SFREGH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				SFREGH			
RO								RO				RO			
0								0				0			

Access Types Legend

Table 4-2813. SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 4	RESERVED	RO		Not Defined
3 - 0	SFREGH	RO	0h	MSB part of the frame length

4.29.36 UART0_UASR Register (Offset = 38h) [reset = h]

Short Description: UART Autobauding Status Register

Long Description:

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Table 4-2814. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-1340. UART0_UASR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PARITY_TYPE		BIT_BY_CHAR	SPEED				
RO		RO	RO				
0		0	0				

Access Types Legend

Table 4-2815. UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 6	PARITY_TYPE	RO	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity
5	BIT_BY_CHAR	RO	0h	0 => 7 bits character identified. 1 => 8 bits character identified
4 - 0	SPEED	RO	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds

4.29.37 UART0_BLR Register (Offset = 38h) [reset = h]

Short Description: IrDA modes only.Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

Long Description:

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Table 4-2816. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-1341. UART0_BLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								STS_FIFO_RESET	XBOF_TYPE	RESERVED					
RO								RW	RW	RO					
0								0	1	0					

Access Types Legend

Table 4-2817. BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	STS_FIFO_RESET	RW	0h	Status FIFO reset. This bit is self-clearing
6	XBOF_TYPE	RW	1h	SIR xBOF select. 0 | XBOF_TYPE_VALUE_00xFF 1 | XBOF_TYPE_VALUE_10xC0
5 - 0	RESERVED	RO		Not Defined

4.29.38 UART0_ACREG Register (Offset = 3Ch) [reset = h]

Short Description: IR-IrDA and IR-CIR modes only.

Long Description:

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Table 4-2818. Instance Table

Instance Name	Physical Address
UART0	5230 003Ch
UART1	5230 103Ch
UART2	5230 203Ch
UART3	5230 303Ch
UART4	5230 403Ch
UART5	5230 503Ch

Figure 4-1342. UART0_ACREG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2819. ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	PULSE_TYPE	RW	0h	SIR pulse width select: 0 | PULSE_TYPE_VALUE_03/16 of baud-rate pulse width 1 | PULSE_TYPE_VALUE_11.6us
6	SD_MOD	RW	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. 0 | SD_MOD_VALUE_0SD pin is set to high 1 | SD_MOD_VALUE_1SD pin is set to low
5	DIS_IR_RX	RW	0h	Not Defined 0 | DIS_IR_RX_VALUE_0Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation). 1 | DIS_IR_RX_VALUE_1Disables RX input (permanent state - independent of transmit).
4	DIS_TX_UNDERRUN	RW	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. 0 | DIS_TX_UNDERRUN_VALUE_0Long stop bits cannot be transmitted, TX underrun is enabled 1 | DIS_TX_UNDERRUN_VALUE_1Long stop bits can be transmitted, TX underrun is disabled
3	SEND_SIP	RW	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP]If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. 0 | SEND_SIP_VALUE_0No action 1 | SEND_SIP_VALUE_1Send SIP pulse.
2	SCTX_EN	RW	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing.

Table 4-2819. ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ABORT_EN	RW	0h	Frame Abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame.
0	EOT_EN	RW	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO].

4.29.39 UART0_SCR Register (Offset = 40h) [reset = h]

Short Description: Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

Long Description:

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Table 4-2820. Instance Table

Instance Name	Physical Address
UART0	5230 0040h
UART1	5230 1040h
UART2	5230 2040h
UART3	5230 3040h
UART4	5230 4040h
UART5	5230 5040h

Figure 4-1343. UART0_SCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
RO								RW	RW	RW	RW	RW	RW		RW
0								0	0	0	0	0	0		0

Access Types Legend

Table 4-2821. SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	RX_TRIG_GRANU1	RW	0h	Not Defined 0 | RX_TRIG_GRANU1_VALUE_0DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. 1 | RX_TRIG_GRANU1_VALUE_1ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.
6	TX_TRIG_GRANU1	RW	0h	Not Defined 0 | TX_TRIG_GRANU1_VALUE_0DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL. 1 | TX_TRIG_GRANU1_VALUE_1Enables the granularity of 1 for trigger TX level.
5	DSR_IT	RW	0h	Not Defined 0 | DSR_IT_VALUE_0DISABLES DSR* INTERRUPT. 1 | DSR_IT_VALUE_1ENABLES DSR* INTERRUPT.
4	RX_CTS_DSR_WAKE_UP_ENABLE	RW	0h	Not Defined 0 | RX_CTS_DSR_WAKE_UP_ENABLE_VALUE_0DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1]. 1 | RX_CTS_DSR_WAKE_UP_ENABLE_VALUE_1Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	RW	0h	Not Defined 0 | TX_EMPTY_CTL_IT_VALUE_0Normal mode for THR interrupt (See UART mode interrupts table). 1 | TX_EMPTY_CTL_IT_VALUE_1THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.

Table 4-2821. SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 1	DMA_MODE_2	RW	0h	Used to specify the DMA mode valid if SCR[0] = 1 0x0 | DMA_MODE_2_VALUE_0DMA mode 0 (no DMA) 0x1 | DMA_MODE_2_VALUE_1DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 0x2 | DMA_MODE_2_VALUE_2DMA mode 2 (UART_nDMA_REQ[0] in RX) 0x3 | DMA_MODE_2_VALUE_3DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	RW	0h	Not Defined 0 | DMA_MODE_CTL_VALUE_0The DMA_MODE is set with FCR[3] 1 | DMA_MODE_CTL_VALUE_1The DMA_MODE is set with SCR[2:1]

4.29.40 UART0_SSR Register (Offset = 44h) [reset = h]

Short Description: Note: Bit 1 is reset only when SCR[4] is reset to 0.

Long Description:

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Table 4-2822. Instance Table

Instance Name	Physical Address
UART0	5230 0044h
UART1	5230 1044h
UART2	5230 2044h
UART3	5230 3044h
UART4	5230 4044h
UART5	5230 5044h

Figure 4-1344. UART0_SSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
RO								RO					RW	RO	RO
0								0					1	0	0

Access Types Legend

Table 4-2823. SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 3	RESERVED	RO		Not Defined
2	DMA_COUNTER_RST	RW	1h	Not Defined 0 | DMA_COUNTER_RST_VALUE_0The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2]) 1 | DMA_COUNTER_RST_VALUE_1The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])
1	RX_CTS_DSR_WAKE_UP_STS	RO	0h	Not Defined Read0 | RX_CTS_DSR_WAKE_UP_STS_VALUE_0No falling edge event on RX, CTS* and DSR* Read1 | RX_CTS_DSR_WAKE_UP_STS_VALUE_1A falling edge occurred on RX, CTS* or DSR*
0	TX_FIFO_FULL	RO	0h	Not Defined Read0 | TX_FIFO_FULL_VALUE_0TX FIFO is not full Read1 | TX_FIFO_FULL_VALUE_1TX FIFO is full.

4.29.41 UART0_EBLR Register (Offset = 48h) [reset = h]

Short Description: IR-IrDA and IR-CIR modes only.In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to

Long Description:

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Table 4-2824. Instance Table

Instance Name	Physical Address
UART0	5230 0048h
UART1	5230 1048h
UART2	5230 2048h
UART3	5230 3048h
UART4	5230 4048h
UART5	5230 5048h

Figure 4-1345. UART0_EBLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EBLR							
RO								RW							
0								0							

Access Types Legend

Table 4-2825. EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	EBLR	RW	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification.IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]].0x00: feature disabled.0x01: generate RX_STOP interrupt after receiving one zero bit....0xFF: generate RX_STOP interrupt after receiving 255 zero bits.

4.29.42 UART0_MVR Register (Offset = 50h) [reset = h]

Short Description: The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returnedNotes: UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification). UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification). UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

Long Description:

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Table 4-2826. Instance Table

Instance Name	Physical Address
UART0	5230 0050h
UART1	5230 1050h
UART2	5230 2050h
UART3	5230 3050h
UART4	5230 4050h
UART5	5230 5050h

Figure 4-1346. UART0_MVR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		RO		RO											
1		0		11101000010											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
1000				110				0		11					

Access Types Legend

Table 4-2827. MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme revision number of module
29 - 28	RESERVED	RO		Not Defined
27 - 16	FUNC	RO	295ABD14Ah	Function revision number of module
15 - 11	RTL	RO	3E8h	Rtl revision number of module
10 - 8	MAJOR	RO	6Eh	Major revision number of the module.
7 - 6	CUSTOM	RO	0h	Custom revision number of the module.
5 - 0	MINOR	RO	Bh	Minor revision number of the module.

4.29.43 UART0_SYSC Register (Offset = 54h) [reset = h]

Short Description: The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

Long Description:

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Table 4-2828. Instance Table

Instance Name	Physical Address
UART0	5230 0054h
UART1	5230 1054h
UART2	5230 2054h
UART3	5230 3054h
UART4	5230 4054h
UART5	5230 5054h

Figure 4-1347. UART0_SYSC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
RO								RO			RW		RW	WO	RW
0								0			0		0	0	0

Access Types Legend

Table 4-2829. SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 5	RESERVED	RO		Not Defined
4 - 3	IDLEMODE	RW	0h	POWER MANAGEMENT REQ/ACK CONTROLREF: OCP DESIGN GUIDELINES VERSION 1.1 0x0 | IDLEMODE_VALUE_0Force idle. An idle request is acknowledged unconditionally 0x1 | IDLEMODE_VALUE_1No-idle. An idle request is never acknowledged. 0x2 | IDLEMODE_VALUE_2Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module. 0x3 | IDLEMODE_VALUE_3reserved
2	ENAWAKEUP	RW	0h	WAKE UP FEATURE CONTROL 0 | ENAWAKEUP_VALUE_0Wake up is disabled 1 | ENAWAKEUP_VALUE_1Wake up capability is enabled
1	SOFTRESET	WO	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. Write0 | SOFTRESET_VALUE_0Normal mode Write1 | SOFTRESET_VALUE_1The module is reset
0	AUTOIDLE	RW	0h	Internal OCP clock gating strategy 0 | AUTOIDLE_VALUE_0Clock is running 1 | AUTOIDLE_VALUE_1Automatic OCP clock gating strategy is applied, based on the OCP interface activity

4.29.44 UART0_SYSS Register (Offset = 58h) [reset = h]

Short Description: RO

Long Description:

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Table 4-2830. Instance Table

Instance Name	Physical Address
UART0	5230 0058h
UART1	5230 1058h
UART2	5230 2058h
UART3	5230 3058h
UART4	5230 4058h
UART5	5230 5058h

Figure 4-1348. UART0_SYSS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED							RESETDONE
RO								RO							RO
0								0							0

Access Types Legend

Table 4-2831. SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 1	RESERVED	RO		Not Defined
0	RESETDONE	RO	0h	Internal Reset Monitoring Read0 | RESETDONE_VALUE_0Internal Module Reset is ongoing Read1 | RESETDONE_VALUE_1Reset completed

4.29.45 UART0_WER Register (Offset = 5Ch) [reset = h]

Short Description: The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

Long Description:

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Table 4-2832. Instance Table

Instance Name	Physical Address
UART0	5230 005Ch
UART1	5230 105Ch
UART2	5230 205Ch
UART3	5230 305Ch
UART4	5230 405Ch
UART5	5230 505Ch

Figure 4-1349. UART0_WER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								1	1	1	1	1	1	1	1

Access Types Legend

Table 4-2833. WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7	EVENT_7_TX_WAKEUP_EN	RW	1h	Not Defined 0 | EVENT_7_TX_WAKEUP_EN_VALUE_0Event is not allowed to wake up the system 1 | EVENT_7_TX_WAKEUP_EN_VALUE_1EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	RW	1h	Not Defined 0 | EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT_VALUE_0Event is not allowed to wake up the system 1 | EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT_VALUE_1Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	RW	1h	Not Defined 0 | EVENT_5_RHR_INTERRUPT_VALUE_0Event is not allowed to wake up the system 1 | EVENT_5_RHR_INTERRUPT_VALUE_1Event can wake up the system
4	EVENT_4_RX_ACTIVITY	RW	1h	Not Defined 0 | EVENT_4_RX_ACTIVITY_VALUE_0Event is not allowed to wake up the system 1 | EVENT_4_RX_ACTIVITY_VALUE_1Event can wake up the system

Table 4-2833. WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EVENT_3_DCD_CD_ACTIVITY	RW	1h	Not Defined 0 | EVENT_3_DCD_CD_ACTIVITY_VALUE_0Event is not allowed to wake up the system 1 | EVENT_3_DCD_CD_ACTIVITY_VALUE_1Event can wake up the system
2	EVENT_2_RI_ACTIVITY	RW	1h	Not Defined 0 | EVENT_2_RI_ACTIVITY_VALUE_0Event is not allowed to wake up the system 1 | EVENT_2_RI_ACTIVITY_VALUE_1Event can wake up the system
1	EVENT_1_DSR_ACTIVITY	RW	1h	Not Defined 0 | EVENT_1_DSR_ACTIVITY_VALUE_0Event is not allowed to wake up the system 1 | EVENT_1_DSR_ACTIVITY_VALUE_1Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	RW	1h	Not Defined 0 | EVENT_0_CTS_ACTIVITY_VALUE_0Event is not allowed to wake up the system 1 | EVENT_0_CTS_ACTIVITY_VALUE_1Event can wake up the system

4.29.46 UART0_CFPS Register (Offset = 60h) [reset = h]

Short Description: Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

Long Description:

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Table 4-2834. Instance Table

Instance Name	Physical Address
UART0	5230 0060h
UART1	5230 1060h
UART2	5230 2060h
UART3	5230 3060h
UART4	5230 4060h
UART5	5230 5060h

Figure 4-1350. UART0_CFPS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								CFPS							
RO								RW							
0								1101001							

Access Types Legend

Table 4-2835. CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	RO	0h	Not Defined
7 - 0	CFPS	RW	10CCC9h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below.Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14* configured at reset to this valueNote: CFPS = 0 is not supported.

4.29.47 UART0_RXFIFO_LVL Register (Offset = 64h) [reset = h]

Short Description: Level of the RX FIFO

Long Description:

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Table 4-2836. Instance Table

Instance Name	Physical Address
UART0	5230 0064h
UART1	5230 1064h
UART2	5230 2064h
UART3	5230 3064h
UART4	5230 4064h
UART5	5230 5064h

Figure 4-1351. UART0_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								RXFIFO_LVL							
RO								RO							
0								0							

Access Types Legend

Table 4-2837. RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED24	RO	0h	Not Defined
7 - 0	RXFIFO_LVL	RO	0h	Not Defined

4.29.48 UART0_TXFIFO_LVL Register (Offset = 68h) [reset = h]

Short Description: Level of the TX FIFO

Long Description:

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Table 4-2838. Instance Table

Instance Name	Physical Address
UART0	5230 0068h
UART1	5230 1068h
UART2	5230 2068h
UART3	5230 3068h
UART4	5230 4068h
UART5	5230 5068h

Figure 4-1352. UART0_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								TXFIFO_LVL							
RO								RO							
0								0							

Access Types Legend

Table 4-2839. TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED24	RO	0h	Not Defined
7 - 0	TXFIFO_LVL	RO	0h	Not Defined

4.29.49 UART0_IER2 Register (Offset = 6Ch) [reset = h]

Short Description: Enables RX/TX FIFOs empty corresponding interrupts.

Long Description:

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Table 4-2840. Instance Table

Instance Name	Physical Address
UART0	5230 006Ch
UART1	5230 106Ch
UART2	5230 206Ch
UART3	5230 306Ch
UART4	5230 406Ch
UART5	5230 506Ch

Figure 4-1353. UART0_IER2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
RO								RO					RW	RW	RW
0								0					0	0	0

Access Types Legend

Table 4-2841. IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7 - 3	RESERVED	RO		Not Defined
2	RHR_IT_DIS	RW	0h	Not Defined 0 | RHR_IT_DIS_VALUE_0Enables the RHR interrupt. 1 | RHR_IT_DIS_VALUE_1Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	RW	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt.
0	EN_RXFIFO_EMPTY	RW	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt.

4.29.50 UART0_ISR2 Register (Offset = 70h) [reset = h]

Short Description: Status of RX/TX FIFOs empty corresponding interrupts.

Long Description:

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Table 4-2842. Instance Table

Instance Name	Physical Address
UART0	5230 0070h
UART1	5230 1070h
UART2	5230 2070h
UART3	5230 3070h
UART4	5230 4070h
UART5	5230 5070h

Figure 4-1354. UART0_ISR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
RO								RO						RW	RW
0								0						1	1

Access Types Legend

Table 4-2843. ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7 - 2	RESERVED	RO		Not Defined
1	TXFIFO_EMPTY_STS	RW	1h	TXFIFO interrupt pending 0 | TXFIFO_EMPTY_STS_VALUE_0TXFIFO_EMPTY interrupt not pending. 1 | TXFIFO_EMPTY_STS_VALUE_1TXFIFO_EMPTY interrupt pending.
0	RXFIFO_EMPTY_STS	RW	1h	RXFIFO interrupt pending 0 | RXFIFO_EMPTY_STS_VALUE_0RXFIFO_EMPTY interrupt not pending. 1 | RXFIFO_EMPTY_STS_VALUE_1RXFIFO_EMPTY interrupt pending.

4.29.51 UART0_FREQ_SEL Register (Offset = 74h) [reset = h]

Short Description: Sample per bit value selector

Long Description:

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Table 4-2844. Instance Table

Instance Name	Physical Address
UART0	5230 0074h
UART1	5230 1074h
UART2	5230 2074h
UART3	5230 3074h
UART4	5230 4074h
UART5	5230 5074h

Figure 4-1355. UART0_FREQ_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								FREQ_SEL							
RO								RW							
0								11010							

Access Types Legend

Table 4-2845. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED2	RO	0h	RESERVED
7 - 0	FREQ_SEL	RW	2B02h	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6.

4.29.52 UART0_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = h]

Short Description: Unused

Long Description:

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Table 4-2846. Instance Table

Instance Name	Physical Address
UART0	5230 0078h
UART1	5230 1078h
UART2	5230 2078h
UART3	5230 3078h
UART4	5230 4078h
UART5	5230 5078h

Figure 4-1356. UART0_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
RO															
0															

Access Types Legend

Table 4-2847. ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED	RO		Not Defined

4.29.53 UART0_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = h]

Short Description: Unused

Long Description:

Return to Summary Table

Table 4-2848. Instance Table

Instance Name	Physical Address
UART0	5230 007Ch
UART1	5230 107Ch
UART2	5230 207Ch
UART3	5230 307Ch
UART4	5230 407Ch
UART5	5230 507Ch

Figure 4-1357. UART0_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
RO															
0															

Access Types Legend

Table 4-2849. BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED	RO		Not Defined

4.29.54 UART0_MDR3 Register (Offset = 80h) [reset = h]

Short Description: Mode definition register 3.

Long Description:

Return to Summary Table

Table 4-2850. Instance Table

Instance Name	Physical Address
UART0	5230 0080h
UART1	5230 1080h
UART2	5230 2080h
UART3	5230 3080h
UART4	5230 4080h
UART5	5230 5080h

Figure 4-1358. UART0_MDR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
RO								RO			RW	RW	RW	RW	RW
0								0			0	0	0	0	0

Access Types Legend

Table 4-2851. MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED2	RO	0h	Not Defined
7 - 5	RESERVED1	RO	0h	Reserved
4	DIR_EN	RW	0h	RS-485 External Transceiver Direction Enable
3	DIR_POL	RW	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0
2	SET_DMA_TX_THRESHOLD	RW	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD]
1	NONDEFAULT_FREQ	RW	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies
0	DISABLE_CIR_RX_DEMOD	RW	0h	Disables[1]/Enables[0] CIR RX demodulation 0 | DISABLE_CIR_RX_DEMOD_VALUE_0Enables CIR RX demodulation 1 | DISABLE_CIR_RX_DEMOD_VALUE_1Disables CIR RX demodulation

4.29.55 UART0_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = h]

Short Description: Use to manually set the TX DMA threshold level.MDR3[2] SET_TX_DMA_THRESHOLD must be one and must be value + tx_trigger_level <= 64 (TX FIFO size).If not, 64-tx_trigger_level will be used w/o modifying the value of this register.

Long Description:

Return to Summary Table

Table 4-2852. Instance Table

Instance Name	Physical Address
UART0	5230 0084h
UART1	5230 1084h
UART2	5230 2084h
UART3	5230 3084h
UART4	5230 4084h
UART5	5230 5084h

Figure 4-1359. UART0_TX_DMA_THRESHOLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		TX_DMA_THRESHOLD					
RO								RO		RW					
0								0		0					

Access Types Legend

Table 4-2853. TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	RESERVED
7 - 6	RESERVED	RO		Reserved
5 - 0	TX_DMA_THRESHOLD	RW	0h	Use to manually set the TX DMA threshold level.

4.29.56 UART0_MDR4 Register (Offset = 88h) [reset = h]

Short Description: Mode definition register 4

Long Description:

Return to Summary Table

Table 4-2854. Instance Table

Instance Name	Physical Address
UART0	5230 0088h
UART1	5230 1088h
UART2	5230 2088h
UART3	5230 3088h
UART4	5230 4088h
UART5	5230 5088h

Figure 4-1360. UART0_MDR4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED	MODE9	FREQ_SEL_H			MODE		
RO								RO	RW	RW			RW		
0								0	0	0			0		

Access Types Legend

Table 4-2855. MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7	RESERVED	RO		Not Defined
6	MODE9	RW	0h	9-bit character length. When '1', overrides character length setting in LCR
5 - 3	FREQ_SEL_H	RW	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode
2 - 0	MODE	RW	0h	New modes [when set, overrides MDR1 modes] 0x0 | DISABLEDdisabled (no override) 0x1 | RESERVEDreserved 0x2 | SYNCH_EXTSynchronous mode with external clock 0x3 | SYNCH_GENSynchronous mode with generated clock 0x4 | ISO7816_0ISO 7816 mode T=0 0x5 | ISO7816_1ISO 7816 mode T=1 0x6 | RESERVED1reserved 0x7 | RESERVED2reserved

4.29.57 UART0_EFR2 Register (Offset = 8Ch) [reset = h]

Short Description: Enhanced Features Register 2

Long Description:

Return to Summary Table

Table 4-2856. Instance Table

Instance Name	Physical Address
UART0	5230 008Ch
UART1	5230 108Ch
UART2	5230 208Ch
UART3	5230 308Ch
UART4	5230 408Ch
UART5	5230 508Ch

Figure 4-1361. UART0_EFR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2857. EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7	BROADCAST	RW	0h	Enables broadcast address matching in multi-drop address match mode
6	TIMEOUT_BEHAVE	RW	0h	Specifies how timeout is measured 0 | _0timeout after at least one character has been received 1 | _1periodic timeout even when no character has been received
5	C8	RW	0h	Value for ISO 7816 C8 pin for software control
4	C4	RW	0h	Value for ISO 7816 C4 pin for software control
3	C2	RW	0h	Value for ISO 7816 reset pin [software controllable]
2	MULTIDROP	RW	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1'
1	RHR_OVERRUN	RW	0h	RHR Overrun behaviour when buffer full 0 | DEFAULTdata in RHR is not overwritten (standard) 1 | ATMELdata in RHR is overwritten when buffer full (and FIFO disabled)
0	ENDIAN	RW	0h	Endianness 0 | LOW_ENDIANLittle Endian (LSB First) 1 | BIG_ENDIANBig Endian (MSB First)

4.29.58 UART0_ECR Register (Offset = 90h) [reset = h]

Short Description: Enhanced Control register

Long Description:

Return to Summary Table

Table 4-2858. Instance Table

Instance Name	Physical Address
UART0	5230 0090h
UART1	5230 1090h
UART2	5230 2090h
UART3	5230 3090h
UART4	5230 4090h
UART5	5230 5090h

Figure 4-1362. UART0_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
RO								RO		WO	RW	RW	WO	WO	WO
0								0		0	1	1	0	0	0

Access Types Legend

Table 4-2859. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7 - 6	RESERVED	RO		Not Defined
5	CLEAR_TX_PE	WO	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only]
4	TX_EN	RW	1h	Enables/Disables the transmitter 0 | DISABLEDTransmitter is shut down 1 | ENABLEDTransmitter is working
3	RX_EN	RW	1h	Enables/Disables the receiver 0 | DISABLEDReceiver is shut down 1 | ENABLEDReceiver is operating
2	TX_RST	WO	0h	Writing '1' resets the transmitter
1	RX_RST	WO	0h	Writing '1' resets the receiver
0	A_MULTIDROP	WO	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address

4.29.59 UART0_TIMEGUARD Register (Offset = 94h) [reset = h]

Short Description: Timeguard

Long Description:

Return to Summary Table

Table 4-2860. Instance Table

Instance Name	Physical Address
UART0	5230 0094h
UART1	5230 1094h
UART2	5230 2094h
UART3	5230 3094h
UART4	5230 4094h
UART5	5230 5094h

Figure 4-1363. UART0_TIMEGUARD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEGUARD							
RO								RW							
0								0							

Access Types Legend

Table 4-2861. TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	RO		Not Defined
7 - 0	TIMEGUARD	RW	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices

4.29.60 UART0_TIMEOUTL Register (Offset = 98h) [reset = h]

Short Description: Timeout lower byte

Long Description:

Return to Summary Table

Table 4-2862. Instance Table

Instance Name	Physical Address
UART0	5230 0098h
UART1	5230 1098h
UART2	5230 2098h
UART3	5230 3098h
UART4	5230 4098h
UART5	5230 5098h

Figure 4-1364. UART0_TIMEOUTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_L							
RO								RW							
0								0							

Access Types Legend

Table 4-2863. TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	RO		Not Defined
7 - 0	TIMEOUT_L	RW	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value]

4.29.61 UART0_TIMEOUTH Register (Offset = 9Ch) [reset = h]

Short Description: Timeout higher byte

Long Description:

Return to Summary Table

Table 4-2864. Instance Table

Instance Name	Physical Address
UART0	5230 009Ch
UART1	5230 109Ch
UART2	5230 209Ch
UART3	5230 309Ch
UART4	5230 409Ch
UART5	5230 509Ch

Figure 4-1365. UART0_TIMEOUTH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_H							
RO								RW							
0								0							

Access Types Legend

Table 4-2865. TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	RO		Not Defined
7 - 0	TIMEOUT_H	RW	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value]

4.29.62 UART0_SCCR Register (Offset = A0h) [reset = h]

Short Description: Smartcard (ISO7816) mode Control Register

Long Description:

Return to Summary Table

Table 4-2866. Instance Table

Instance Name	Physical Address
UART0	5230 00A0h
UART1	5230 10A0h
UART2	5230 20A0h
UART3	5230 30A0h
UART4	5230 40A0h
UART5	5230 50A0h

Figure 4-1366. UART0_SCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								DSNACK	INACK	RESERVED			MAX_ITERATION		
RO								RW	RW	RO			RW		
0								0	0	0			111		

Access Types Legend

Table 4-2867. SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7	DSNACK	RW	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when reading it.
6	INACK	RW	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when reading it.
5 - 3	RESERVED	RO		Not Defined
2 - 0	MAX_ITERATION	RW	6Fh	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared.

4.29.63 UART0_ETHR Register (Offset = A4h) [reset = h]

Short Description: Extended Transmit Holding Register

Long Description:

Return to Summary Table

Table 4-2868. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-1367. UART0_ETHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ETHR								
RO							WO								
0							0								

Access Types Legend

Table 4-2869. ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED	RO		Not Defined
8 - 0	ETHR	WO	0h	Extended Transmit Holding Register - allows writing the full 9bit RHR

4.29.64 UART0_ERHR Register (Offset = A4h) [reset = h]

Short Description: Extended Receive Holding Register

Long Description:

Return to Summary Table

Table 4-2870. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-1368. UART0_ERHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ERHR								
RO							RO								
0							0								

Access Types Legend

Table 4-2871. ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED	RO		Not Defined
8 - 0	ERHR	RO	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR

4.29.65 UART0_MAR Register (Offset = A8h) [reset = h]

Short Description: Multidrop Address Register

Long Description:

Return to Summary Table

Table 4-2872. Instance Table

Instance Name	Physical Address
UART0	5230 00A8h
UART1	5230 10A8h
UART2	5230 20A8h
UART3	5230 30A8h
UART4	5230 40A8h
UART5	5230 50A8h

Figure 4-1369. UART0_MAR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
ADDRESS							
RW							
0							

Access Types Legend

Table 4-2873. MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	ADDRESS	RW	0h	Multidrop match address value

4.29.66 UART0_MMR Register (Offset = ACh) [reset = h]

Short Description: Multidrop Mask Register

Long Description:

Return to Summary Table

Table 4-2874. Instance Table

Instance Name	Physical Address
UART0	5230 00ACh
UART1	5230 10ACh
UART2	5230 20ACh
UART3	5230 30ACh
UART4	5230 40ACh
UART5	5230 50ACh

Figure 4-1370. UART0_MMR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
MASK							
RW							
0							

Access Types Legend

Table 4-2875. MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	MASK	RW	0h	Address match masking value ? writing a 0 to a bit means that the corresponding address bit will be ignored in matching

4.29.67 UART0_MBR Register (Offset = B0h) [reset = h]

Short Description: Multidrop Broadcast Address Register

Long Description:

Return to Summary Table

Table 4-2876. Instance Table

Instance Name	Physical Address
UART0	5230 00B0h
UART1	5230 10B0h
UART2	5230 20B0h
UART3	5230 30B0h
UART4	5230 40B0h
UART5	5230 50B0h

Figure 4-1371. UART0_MBR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
BROADCAST_ADDRESS							
RW							
0							

Access Types Legend

Table 4-2877. MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	BROADCAST_ADDRESS	RW	0h	Broadcast address for address matching

Table 4-2878. Access Type Codes

Access Type	Code	Description
RW	RW	Undefined
RO	RO	Undefined
WO	WO	Undefined

4.30 MSS_VIM Registers

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9

Offset	Length	Acronym	Register Name	VIM Physical Address
0h	32	VIM_PID	The Revision Register contains the major and minor revisions for the module.	50F0 0000h
4h	32	VIM_INFO	The Info Register gives the configuration Inforrmation of this VIM.	50F0 0004h
8h	32	VIM_PRIIRQ	The Prioritized IRQ Register shows the number of the highest priority pending IRQ.	50F0 0008h
Ch	32	VIM_PRIFIQ	The Prioritized FIQ Register shows the number of the highest priority pending FIQ.	50F0 000Ch
10h	32	VIM_IRQGSTS	The IRQ Group Status Register indicates which groups have pending IRQ interrupts.	50F0 0010h
14h	32	VIM_FIQGSTS	The FIQ Group Status Register indicates which groups have pending FIQ interrupts.	50F0 0014h
18h	32	VIM_IRQVEC	The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.	50F0 0018h
1Ch	32	VIM_FIQVEC	The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.	50F0 001Ch
20h	32	VIM_ACTIRQ	The Active IRQ Register shows the number of the currently active IRQ.	50F0 0020h
24h	32	VIM_ACTFIQ	The Active FIQ Register shows the number of the currently active FIQ.	50F0 0024h
28h	32	VIM_IRQPRIMSK	The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.	50F0 0028h
2Ch	32	VIM_FIQPRIMSK	The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.	50F0 002Ch
30h	32	VIM_DEDVEC	The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.	50F0 0030h
400h	32	VIM_RAW	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0400h
404h	32	VIM_STS	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0404h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
408h	32	VIM_INTR_EN_SET	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0408h
40Ch	32	VIM_INTER_EN_CLR	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 040Ch
410h	32	VIM_IRQSTS	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0410h
414h	32	VIM_FIQSTS	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0414h
418h	32	VIM_INTMAP	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0418h
41Ch	32	VIM_INTTYPE	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 041Ch
420h	32	VIM_RAW_1	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0420h
424h	32	VIM_STS_1	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0424h
428h	32	VIM_INTR_EN_SET_1	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0428h
42Ch	32	VIM_INTER_EN_CLR_1	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 042Ch
430h	32	VIM_IRQSTS_1	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0430h
434h	32	VIM_FIQSTS_1	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0434h
438h	32	VIM_INTMAP_1	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0438h
43Ch	32	VIM_INTTYPE_1	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 043Ch
440h	32	VIM_RAW_2	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0440h
444h	32	VIM_STS_2	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0444h
448h	32	VIM_INTR_EN_SET_2	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0448h
44Ch	32	VIM_INTER_EN_CLR_2	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 044Ch
450h	32	VIM_IRQSTS_2	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0450h
454h	32	VIM_FIQSTS_2	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0454h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
458h	32	VIM_INTMAP_2	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0458h
45Ch	32	VIM_INTTYPE_2	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 045Ch
460h	32	VIM_RAW_3	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0460h
464h	32	VIM_STS_3	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0464h
468h	32	VIM_INTR_EN_SET_3	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0468h
46Ch	32	VIM_INTER_EN_CLR_3	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 046Ch
470h	32	VIM_IRQSTS_3	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0470h
474h	32	VIM_FIQSTS_3	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0474h
478h	32	VIM_INTMAP_3	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0478h
47Ch	32	VIM_INTTYPE_3	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 047Ch
480h	32	VIM_RAW_4	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 0480h
484h	32	VIM_STS_4	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 0484h
488h	32	VIM_INTR_EN_SET_4	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 0488h
48Ch	32	VIM_INTER_EN_CLR_4	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 048Ch
490h	32	VIM_IRQSTS_4	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 0490h
494h	32	VIM_FIQSTS_4	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 0494h
498h	32	VIM_INTMAP_4	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 0498h
49Ch	32	VIM_INTTYPE_4	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 049Ch
4A0h	32	VIM_RAW_5	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04A0h
4A4h	32	VIM_STS_5	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04A4h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
4A8h	32	VIM_INTR_EN_SET_5	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04A8h
4ACh	32	VIM_INTER_EN_CLR_5	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04ACh
4B0h	32	VIM_IRQSTS_5	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04B0h
4B4h	32	VIM_FIQSTS_5	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04B4h
4B8h	32	VIM_INTMAP_5	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04B8h
4BCh	32	VIM_INTTYPE_5	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04BCh
4C0h	32	VIM_RAW_6	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04C0h
4C4h	32	VIM_STS_6	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04C4h
4C8h	32	VIM_INTR_EN_SET_6	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04C8h
4CCh	32	VIM_INTER_EN_CLR_6	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04CCh
4D0h	32	VIM_IRQSTS_6	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04D0h
4D4h	32	VIM_FIQSTS_6	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04D4h
4D8h	32	VIM_INTMAP_6	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04D8h
4DCh	32	VIM_INTTYPE_6	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04DCh
4E0h	32	VIM_RAW_7	Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00	50F0 04E0h
4E4h	32	VIM_STS_7	Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04	50F0 04E4h
4E8h	32	VIM_INTR_EN_SET_7	Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08	50F0 04E8h
4ECh	32	VIM_INTER_EN_CLR_7	Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C	50F0 04ECh
4F0h	32	VIM_IRQSTS_7	Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10	50F0 04F0h
4F4h	32	VIM_FIQSTS_7	Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14	50F0 04F4h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
4F8h	32	VIM_INTMAP_7	Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18	50F0 04F8h
4FCh	32	VIM_INTTYPE_7	Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C	50F0 04FCh
1000h	32	VIM_INTPRIORITY	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h4	50F0 1000h
1004h	32	VIM_INTPRIORITY_1	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h5	50F0 1004h
1008h	32	VIM_INTPRIORITY_2	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h6	50F0 1008h
100Ch	32	VIM_INTPRIORITY_3	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h7	50F0 100Ch
1010h	32	VIM_INTPRIORITY_4	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h8	50F0 1010h
1014h	32	VIM_INTPRIORITY_5	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h9	50F0 1014h
1018h	32	VIM_INTPRIORITY_6	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h10	50F0 1018h
101Ch	32	VIM_INTPRIORITY_7	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h11	50F0 101Ch
1020h	32	VIM_INTPRIORITY_8	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h12	50F0 1020h
1024h	32	VIM_INTPRIORITY_9	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h13	50F0 1024h
1028h	32	VIM_INTPRIORITY_10	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h14	50F0 1028h
102Ch	32	VIM_INTPRIORITY_11	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h15	50F0 102Ch
1030h	32	VIM_INTPRIORITY_12	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h16	50F0 1030h
1034h	32	VIM_INTPRIORITY_13	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h17	50F0 1034h
1038h	32	VIM_INTPRIORITY_14	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h18	50F0 1038h
103Ch	32	VIM_INTPRIORITY_15	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h19	50F0 103Ch
1040h	32	VIM_INTPRIORITY_16	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h20	50F0 1040h
1044h	32	VIM_INTPRIORITY_17	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h21	50F0 1044h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
1048h	32	VIM_INTPRIORITY_18	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h22	50F0 1048h
104Ch	32	VIM_INTPRIORITY_19	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h23	50F0 104Ch
1050h	32	VIM_INTPRIORITY_20	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h24	50F0 1050h
1054h	32	VIM_INTPRIORITY_21	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h25	50F0 1054h
1058h	32	VIM_INTPRIORITY_22	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h26	50F0 1058h
105Ch	32	VIM_INTPRIORITY_23	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h27	50F0 105Ch
1060h	32	VIM_INTPRIORITY_24	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h28	50F0 1060h
1064h	32	VIM_INTPRIORITY_25	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h29	50F0 1064h
1068h	32	VIM_INTPRIORITY_26	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h30	50F0 1068h
106Ch	32	VIM_INTPRIORITY_27	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h31	50F0 106Ch
1070h	32	VIM_INTPRIORITY_28	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h32	50F0 1070h
1074h	32	VIM_INTPRIORITY_29	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h33	50F0 1074h
1078h	32	VIM_INTPRIORITY_30	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h34	50F0 1078h
107Ch	32	VIM_INTPRIORITY_31	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h35	50F0 107Ch
1080h	32	VIM_INTPRIORITY_32	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h36	50F0 1080h
1084h	32	VIM_INTPRIORITY_33	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h37	50F0 1084h
1088h	32	VIM_INTPRIORITY_34	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h38	50F0 1088h
108Ch	32	VIM_INTPRIORITY_35	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h39	50F0 108Ch
1090h	32	VIM_INTPRIORITY_36	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h40	50F0 1090h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
1094h	32	VIM_INTPRIORITY_37	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h41	50F0 1094h
1098h	32	VIM_INTPRIORITY_38	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h42	50F0 1098h
109Ch	32	VIM_INTPRIORITY_39	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h43	50F0 109Ch
10A0h	32	VIM_INTPRIORITY_40	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h44	50F0 10A0h
10A4h	32	VIM_INTPRIORITY_41	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h45	50F0 10A4h
10A8h	32	VIM_INTPRIORITY_42	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h46	50F0 10A8h
10ACh	32	VIM_INTPRIORITY_43	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h47	50F0 10ACh
10B0h	32	VIM_INTPRIORITY_44	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h48	50F0 10B0h
10B4h	32	VIM_INTPRIORITY_45	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h49	50F0 10B4h
10B8h	32	VIM_INTPRIORITY_46	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h50	50F0 10B8h
10BCh	32	VIM_INTPRIORITY_47	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h51	50F0 10BCh
10C0h	32	VIM_INTPRIORITY_48	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h52	50F0 10C0h
10C4h	32	VIM_INTPRIORITY_49	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h53	50F0 10C4h
10C8h	32	VIM_INTPRIORITY_50	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h54	50F0 10C8h
10CCh	32	VIM_INTPRIORITY_51	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h55	50F0 10CCh
10D0h	32	VIM_INTPRIORITY_52	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h56	50F0 10D0h
10D4h	32	VIM_INTPRIORITY_53	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h57	50F0 10D4h
10D8h	32	VIM_INTPRIORITY_54	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h58	50F0 10D8h
10DCh	32	VIM_INTPRIORITY_55	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h59	50F0 10DCh

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
10E0h	32	VIM_INTPRIORITY_56	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h60	50F0 10E0h
10E4h	32	VIM_INTPRIORITY_57	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h61	50F0 10E4h
10E8h	32	VIM_INTPRIORITY_58	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h62	50F0 10E8h
10ECh	32	VIM_INTPRIORITY_59	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h63	50F0 10ECh
10F0h	32	VIM_INTPRIORITY_60	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h64	50F0 10F0h
10F4h	32	VIM_INTPRIORITY_61	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h65	50F0 10F4h
10F8h	32	VIM_INTPRIORITY_62	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h66	50F0 10F8h
10FCh	32	VIM_INTPRIORITY_63	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h67	50F0 10FCh
1100h	32	VIM_INTPRIORITY_64	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h68	50F0 1100h
1104h	32	VIM_INTPRIORITY_65	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h69	50F0 1104h
1108h	32	VIM_INTPRIORITY_66	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h70	50F0 1108h
110Ch	32	VIM_INTPRIORITY_67	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h71	50F0 110Ch
1110h	32	VIM_INTPRIORITY_68	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h72	50F0 1110h
1114h	32	VIM_INTPRIORITY_69	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h73	50F0 1114h
1118h	32	VIM_INTPRIORITY_70	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h74	50F0 1118h
111Ch	32	VIM_INTPRIORITY_71	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h75	50F0 111Ch
1120h	32	VIM_INTPRIORITY_72	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h76	50F0 1120h
1124h	32	VIM_INTPRIORITY_73	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h77	50F0 1124h
1128h	32	VIM_INTPRIORITY_74	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h78	50F0 1128h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
112Ch	32	VIM_INTPRIORITY_75	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h79	50F0 112Ch
1130h	32	VIM_INTPRIORITY_76	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h80	50F0 1130h
1134h	32	VIM_INTPRIORITY_77	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h81	50F0 1134h
1138h	32	VIM_INTPRIORITY_78	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h82	50F0 1138h
113Ch	32	VIM_INTPRIORITY_79	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h83	50F0 113Ch
1140h	32	VIM_INTPRIORITY_80	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h84	50F0 1140h
1144h	32	VIM_INTPRIORITY_81	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h85	50F0 1144h
1148h	32	VIM_INTPRIORITY_82	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h86	50F0 1148h
114Ch	32	VIM_INTPRIORITY_83	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h87	50F0 114Ch
1150h	32	VIM_INTPRIORITY_84	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h88	50F0 1150h
1154h	32	VIM_INTPRIORITY_85	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h89	50F0 1154h
1158h	32	VIM_INTPRIORITY_86	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h90	50F0 1158h
115Ch	32	VIM_INTPRIORITY_87	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h91	50F0 115Ch
1160h	32	VIM_INTPRIORITY_88	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h92	50F0 1160h
1164h	32	VIM_INTPRIORITY_89	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h93	50F0 1164h
1168h	32	VIM_INTPRIORITY_90	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h94	50F0 1168h
116Ch	32	VIM_INTPRIORITY_91	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h95	50F0 116Ch
1170h	32	VIM_INTPRIORITY_92	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h96	50F0 1170h
1174h	32	VIM_INTPRIORITY_93	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h97	50F0 1174h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
1178h	32	VIM_INTPRIORITY_94	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h98	50F0 1178h
117Ch	32	VIM_INTPRIORITY_95	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h99	50F0 117Ch
1180h	32	VIM_INTPRIORITY_96	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h100	50F0 1180h
1184h	32	VIM_INTPRIORITY_97	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h101	50F0 1184h
1188h	32	VIM_INTPRIORITY_98	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h102	50F0 1188h
118Ch	32	VIM_INTPRIORITY_99	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h103	50F0 118Ch
1190h	32	VIM_INTPRIORITY_100	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h104	50F0 1190h
1194h	32	VIM_INTPRIORITY_101	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h105	50F0 1194h
1198h	32	VIM_INTPRIORITY_102	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h106	50F0 1198h
119Ch	32	VIM_INTPRIORITY_103	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h107	50F0 119Ch
11A0h	32	VIM_INTPRIORITY_104	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h108	50F0 11A0h
11A4h	32	VIM_INTPRIORITY_105	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h109	50F0 11A4h
11A8h	32	VIM_INTPRIORITY_106	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h110	50F0 11A8h
11ACh	32	VIM_INTPRIORITY_107	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h111	50F0 11ACh
11B0h	32	VIM_INTPRIORITY_108	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h112	50F0 11B0h
11B4h	32	VIM_INTPRIORITY_109	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h113	50F0 11B4h
11B8h	32	VIM_INTPRIORITY_110	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h114	50F0 11B8h
11BCh	32	VIM_INTPRIORITY_111	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h115	50F0 11BCh
11C0h	32	VIM_INTPRIORITY_112	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h116	50F0 11C0h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
11C4h	32	VIM_INTPRIORITY_113	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h117	50F0 11C4h
11C8h	32	VIM_INTPRIORITY_114	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h118	50F0 11C8h
11CCh	32	VIM_INTPRIORITY_115	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h119	50F0 11CCh
11D0h	32	VIM_INTPRIORITY_116	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h120	50F0 11D0h
11D4h	32	VIM_INTPRIORITY_117	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h121	50F0 11D4h
11D8h	32	VIM_INTPRIORITY_118	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h122	50F0 11D8h
11DCh	32	VIM_INTPRIORITY_119	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h123	50F0 11DCh
11E0h	32	VIM_INTPRIORITY_120	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h124	50F0 11E0h
11E4h	32	VIM_INTPRIORITY_121	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h125	50F0 11E4h
11E8h	32	VIM_INTPRIORITY_122	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h126	50F0 11E8h
11ECh	32	VIM_INTPRIORITY_123	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h127	50F0 11ECh
11F0h	32	VIM_INTPRIORITY_124	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h128	50F0 11F0h
11F4h	32	VIM_INTPRIORITY_125	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h129	50F0 11F4h
11F8h	32	VIM_INTPRIORITY_126	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h130	50F0 11F8h
11FCh	32	VIM_INTPRIORITY_127	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h131	50F0 11FCh
1200h	32	VIM_INTPRIORITY_128	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h132	50F0 1200h
1204h	32	VIM_INTPRIORITY_129	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h133	50F0 1204h
1208h	32	VIM_INTPRIORITY_130	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h134	50F0 1208h
120Ch	32	VIM_INTPRIORITY_131	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h135	50F0 120Ch

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
1210h	32	VIM_INTPRIORITY_132	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h136	50F0 1210h
1214h	32	VIM_INTPRIORITY_133	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h137	50F0 1214h
1218h	32	VIM_INTPRIORITY_134	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h138	50F0 1218h
121Ch	32	VIM_INTPRIORITY_135	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h139	50F0 121Ch
1220h	32	VIM_INTPRIORITY_136	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h140	50F0 1220h
1224h	32	VIM_INTPRIORITY_137	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h141	50F0 1224h
1228h	32	VIM_INTPRIORITY_138	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h142	50F0 1228h
122Ch	32	VIM_INTPRIORITY_139	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h143	50F0 122Ch
1230h	32	VIM_INTPRIORITY_140	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h144	50F0 1230h
1234h	32	VIM_INTPRIORITY_141	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h145	50F0 1234h
1238h	32	VIM_INTPRIORITY_142	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h146	50F0 1238h
123Ch	32	VIM_INTPRIORITY_143	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h147	50F0 123Ch
1240h	32	VIM_INTPRIORITY_144	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h148	50F0 1240h
1244h	32	VIM_INTPRIORITY_145	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h149	50F0 1244h
1248h	32	VIM_INTPRIORITY_146	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h150	50F0 1248h
124Ch	32	VIM_INTPRIORITY_147	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h151	50F0 124Ch
1250h	32	VIM_INTPRIORITY_148	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h152	50F0 1250h
1254h	32	VIM_INTPRIORITY_149	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h153	50F0 1254h
1258h	32	VIM_INTPRIORITY_150	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h154	50F0 1258h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
125Ch	32	VIM_INTPRIORITY_151	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h155	50F0 125Ch
1260h	32	VIM_INTPRIORITY_152	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h156	50F0 1260h
1264h	32	VIM_INTPRIORITY_153	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h157	50F0 1264h
1268h	32	VIM_INTPRIORITY_154	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h158	50F0 1268h
126Ch	32	VIM_INTPRIORITY_155	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h159	50F0 126Ch
1270h	32	VIM_INTPRIORITY_156	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h160	50F0 1270h
1274h	32	VIM_INTPRIORITY_157	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h161	50F0 1274h
1278h	32	VIM_INTPRIORITY_158	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h162	50F0 1278h
127Ch	32	VIM_INTPRIORITY_159	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h163	50F0 127Ch
1280h	32	VIM_INTPRIORITY_160	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h164	50F0 1280h
1284h	32	VIM_INTPRIORITY_161	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h165	50F0 1284h
1288h	32	VIM_INTPRIORITY_162	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h166	50F0 1288h
128Ch	32	VIM_INTPRIORITY_163	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h167	50F0 128Ch
1290h	32	VIM_INTPRIORITY_164	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h168	50F0 1290h
1294h	32	VIM_INTPRIORITY_165	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h169	50F0 1294h
1298h	32	VIM_INTPRIORITY_166	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h170	50F0 1298h
129Ch	32	VIM_INTPRIORITY_167	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h171	50F0 129Ch
12A0h	32	VIM_INTPRIORITY_168	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h172	50F0 12A0h
12A4h	32	VIM_INTPRIORITY_169	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h173	50F0 12A4h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
12A8h	32	VIM_INTPRIORITY_170	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h174	50F0 12A8h
12ACh	32	VIM_INTPRIORITY_171	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h175	50F0 12ACh
12B0h	32	VIM_INTPRIORITY_172	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h176	50F0 12B0h
12B4h	32	VIM_INTPRIORITY_173	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h177	50F0 12B4h
12B8h	32	VIM_INTPRIORITY_174	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h178	50F0 12B8h
12BCh	32	VIM_INTPRIORITY_175	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h179	50F0 12BCh
12C0h	32	VIM_INTPRIORITY_176	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h180	50F0 12C0h
12C4h	32	VIM_INTPRIORITY_177	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h181	50F0 12C4h
12C8h	32	VIM_INTPRIORITY_178	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h182	50F0 12C8h
12CCh	32	VIM_INTPRIORITY_179	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h183	50F0 12CCh
12D0h	32	VIM_INTPRIORITY_180	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h184	50F0 12D0h
12D4h	32	VIM_INTPRIORITY_181	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h185	50F0 12D4h
12D8h	32	VIM_INTPRIORITY_182	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h186	50F0 12D8h
12DCh	32	VIM_INTPRIORITY_183	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h187	50F0 12DCh
12E0h	32	VIM_INTPRIORITY_184	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h188	50F0 12E0h
12E4h	32	VIM_INTPRIORITY_185	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h189	50F0 12E4h
12E8h	32	VIM_INTPRIORITY_186	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h190	50F0 12E8h
12ECh	32	VIM_INTPRIORITY_187	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h191	50F0 12ECh
12F0h	32	VIM_INTPRIORITY_188	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h192	50F0 12F0h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
12F4h	32	VIM_INTPRIORITY_189	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h193	50F0 12F4h
12F8h	32	VIM_INTPRIORITY_190	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h194	50F0 12F8h
12FCh	32	VIM_INTPRIORITY_191	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h195	50F0 12FCh
1300h	32	VIM_INTPRIORITY_192	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h196	50F0 1300h
1304h	32	VIM_INTPRIORITY_193	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h197	50F0 1304h
1308h	32	VIM_INTPRIORITY_194	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h198	50F0 1308h
130Ch	32	VIM_INTPRIORITY_195	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h199	50F0 130Ch
1310h	32	VIM_INTPRIORITY_196	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h200	50F0 1310h
1314h	32	VIM_INTPRIORITY_197	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h201	50F0 1314h
1318h	32	VIM_INTPRIORITY_198	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h202	50F0 1318h
131Ch	32	VIM_INTPRIORITY_199	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h203	50F0 131Ch
1320h	32	VIM_INTPRIORITY_200	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h204	50F0 1320h
1324h	32	VIM_INTPRIORITY_201	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h205	50F0 1324h
1328h	32	VIM_INTPRIORITY_202	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h206	50F0 1328h
132Ch	32	VIM_INTPRIORITY_203	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h207	50F0 132Ch
1330h	32	VIM_INTPRIORITY_204	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h208	50F0 1330h
1334h	32	VIM_INTPRIORITY_205	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h209	50F0 1334h
1338h	32	VIM_INTPRIORITY_206	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h210	50F0 1338h
133Ch	32	VIM_INTPRIORITY_207	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h211	50F0 133Ch

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
1340h	32	VIM_INTPRIORITY_208	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h212	50F0 1340h
1344h	32	VIM_INTPRIORITY_209	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h213	50F0 1344h
1348h	32	VIM_INTPRIORITY_210	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h214	50F0 1348h
134Ch	32	VIM_INTPRIORITY_211	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h215	50F0 134Ch
1350h	32	VIM_INTPRIORITY_212	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h216	50F0 1350h
1354h	32	VIM_INTPRIORITY_213	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h217	50F0 1354h
1358h	32	VIM_INTPRIORITY_214	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h218	50F0 1358h
135Ch	32	VIM_INTPRIORITY_215	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h219	50F0 135Ch
1360h	32	VIM_INTPRIORITY_216	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h220	50F0 1360h
1364h	32	VIM_INTPRIORITY_217	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h221	50F0 1364h
1368h	32	VIM_INTPRIORITY_218	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h222	50F0 1368h
136Ch	32	VIM_INTPRIORITY_219	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h223	50F0 136Ch
1370h	32	VIM_INTPRIORITY_220	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h224	50F0 1370h
1374h	32	VIM_INTPRIORITY_221	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h225	50F0 1374h
1378h	32	VIM_INTPRIORITY_222	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h226	50F0 1378h
137Ch	32	VIM_INTPRIORITY_223	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h227	50F0 137Ch
1380h	32	VIM_INTPRIORITY_224	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h228	50F0 1380h
1384h	32	VIM_INTPRIORITY_225	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h229	50F0 1384h
1388h	32	VIM_INTPRIORITY_226	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h230	50F0 1388h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
138Ch	32	VIM_INTPRIORITY_227	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h231	50F0 138Ch
1390h	32	VIM_INTPRIORITY_228	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h232	50F0 1390h
1394h	32	VIM_INTPRIORITY_229	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h233	50F0 1394h
1398h	32	VIM_INTPRIORITY_230	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h234	50F0 1398h
139Ch	32	VIM_INTPRIORITY_231	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h235	50F0 139Ch
13A0h	32	VIM_INTPRIORITY_232	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h236	50F0 13A0h
13A4h	32	VIM_INTPRIORITY_233	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h237	50F0 13A4h
13A8h	32	VIM_INTPRIORITY_234	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h238	50F0 13A8h
13ACh	32	VIM_INTPRIORITY_235	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h239	50F0 13ACh
13B0h	32	VIM_INTPRIORITY_236	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h240	50F0 13B0h
13B4h	32	VIM_INTPRIORITY_237	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h241	50F0 13B4h
13B8h	32	VIM_INTPRIORITY_238	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h242	50F0 13B8h
13BCh	32	VIM_INTPRIORITY_239	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h243	50F0 13BCh
13C0h	32	VIM_INTPRIORITY_240	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h244	50F0 13C0h
13C4h	32	VIM_INTPRIORITY_241	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h245	50F0 13C4h
13C8h	32	VIM_INTPRIORITY_242	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h246	50F0 13C8h
13CCh	32	VIM_INTPRIORITY_243	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h247	50F0 13CCh
13D0h	32	VIM_INTPRIORITY_244	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h248	50F0 13D0h
13D4h	32	VIM_INTPRIORITY_245	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h249	50F0 13D4h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
13D8h	32	VIM_INTPRIORITY_246	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h250	50F0 13D8h
13DCh	32	VIM_INTPRIORITY_247	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h251	50F0 13DCh
13E0h	32	VIM_INTPRIORITY_248	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h252	50F0 13E0h
13E4h	32	VIM_INTPRIORITY_249	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h253	50F0 13E4h
13E8h	32	VIM_INTPRIORITY_250	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h254	50F0 13E8h
13ECh	32	VIM_INTPRIORITY_251	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h255	50F0 13ECh
13F0h	32	VIM_INTPRIORITY_252	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h256	50F0 13F0h
13F4h	32	VIM_INTPRIORITY_253	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h257	50F0 13F4h
13F8h	32	VIM_INTPRIORITY_254	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h258	50F0 13F8h
13FCh	32	VIM_INTPRIORITY_255	Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h259	50F0 13FCh
2000h	32	VIM_INTVECTOR	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h4	50F0 2000h
2004h	32	VIM_INTVECTOR_1	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h5	50F0 2004h
2008h	32	VIM_INTVECTOR_2	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h6	50F0 2008h
200Ch	32	VIM_INTVECTOR_3	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h7	50F0 200Ch
2010h	32	VIM_INTVECTOR_4	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h8	50F0 2010h
2014h	32	VIM_INTVECTOR_5	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h9	50F0 2014h
2018h	32	VIM_INTVECTOR_6	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h10	50F0 2018h
201Ch	32	VIM_INTVECTOR_7	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h11	50F0 201Ch
2020h	32	VIM_INTVECTOR_8	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h12	50F0 2020h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2024h	32	VIM_INTVECTOR_9	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h13	50F0 2024h
2028h	32	VIM_INTVECTOR_10	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h14	50F0 2028h
202Ch	32	VIM_INTVECTOR_11	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h15	50F0 202Ch
2030h	32	VIM_INTVECTOR_12	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h16	50F0 2030h
2034h	32	VIM_INTVECTOR_13	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h17	50F0 2034h
2038h	32	VIM_INTVECTOR_14	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h18	50F0 2038h
203Ch	32	VIM_INTVECTOR_15	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h19	50F0 203Ch
2040h	32	VIM_INTVECTOR_16	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h20	50F0 2040h
2044h	32	VIM_INTVECTOR_17	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h21	50F0 2044h
2048h	32	VIM_INTVECTOR_18	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h22	50F0 2048h
204Ch	32	VIM_INTVECTOR_19	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h23	50F0 204Ch
2050h	32	VIM_INTVECTOR_20	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h24	50F0 2050h
2054h	32	VIM_INTVECTOR_21	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h25	50F0 2054h
2058h	32	VIM_INTVECTOR_22	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h26	50F0 2058h
205Ch	32	VIM_INTVECTOR_23	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h27	50F0 205Ch
2060h	32	VIM_INTVECTOR_24	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h28	50F0 2060h
2064h	32	VIM_INTVECTOR_25	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h29	50F0 2064h
2068h	32	VIM_INTVECTOR_26	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h30	50F0 2068h
206Ch	32	VIM_INTVECTOR_27	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h31	50F0 206Ch

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2070h	32	VIM_INTVECTOR_28	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h32	50F0 2070h
2074h	32	VIM_INTVECTOR_29	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h33	50F0 2074h
2078h	32	VIM_INTVECTOR_30	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h34	50F0 2078h
207Ch	32	VIM_INTVECTOR_31	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h35	50F0 207Ch
2080h	32	VIM_INTVECTOR_32	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h36	50F0 2080h
2084h	32	VIM_INTVECTOR_33	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h37	50F0 2084h
2088h	32	VIM_INTVECTOR_34	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h38	50F0 2088h
208Ch	32	VIM_INTVECTOR_35	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h39	50F0 208Ch
2090h	32	VIM_INTVECTOR_36	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h40	50F0 2090h
2094h	32	VIM_INTVECTOR_37	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h41	50F0 2094h
2098h	32	VIM_INTVECTOR_38	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h42	50F0 2098h
209Ch	32	VIM_INTVECTOR_39	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h43	50F0 209Ch
20A0h	32	VIM_INTVECTOR_40	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h44	50F0 20A0h
20A4h	32	VIM_INTVECTOR_41	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h45	50F0 20A4h
20A8h	32	VIM_INTVECTOR_42	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h46	50F0 20A8h
20ACh	32	VIM_INTVECTOR_43	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h47	50F0 20ACh
20B0h	32	VIM_INTVECTOR_44	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h48	50F0 20B0h
20B4h	32	VIM_INTVECTOR_45	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h49	50F0 20B4h
20B8h	32	VIM_INTVECTOR_46	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h50	50F0 20B8h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
20BCh	32	VIM_INTVECTOR_47	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h51	50F0 20BCh
20C0h	32	VIM_INTVECTOR_48	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h52	50F0 20C0h
20C4h	32	VIM_INTVECTOR_49	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h53	50F0 20C4h
20C8h	32	VIM_INTVECTOR_50	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h54	50F0 20C8h
20CCh	32	VIM_INTVECTOR_51	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h55	50F0 20CCh
20D0h	32	VIM_INTVECTOR_52	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h56	50F0 20D0h
20D4h	32	VIM_INTVECTOR_53	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h57	50F0 20D4h
20D8h	32	VIM_INTVECTOR_54	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h58	50F0 20D8h
20DCh	32	VIM_INTVECTOR_55	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h59	50F0 20DCh
20E0h	32	VIM_INTVECTOR_56	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h60	50F0 20E0h
20E4h	32	VIM_INTVECTOR_57	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h61	50F0 20E4h
20E8h	32	VIM_INTVECTOR_58	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h62	50F0 20E8h
20ECh	32	VIM_INTVECTOR_59	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h63	50F0 20ECh
20F0h	32	VIM_INTVECTOR_60	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h64	50F0 20F0h
20F4h	32	VIM_INTVECTOR_61	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h65	50F0 20F4h
20F8h	32	VIM_INTVECTOR_62	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h66	50F0 20F8h
20FCh	32	VIM_INTVECTOR_63	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h67	50F0 20FCh
2100h	32	VIM_INTVECTOR_64	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h68	50F0 2100h
2104h	32	VIM_INTVECTOR_65	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h69	50F0 2104h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2108h	32	VIM_INTVECTOR_66	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h70	50F0 2108h
210Ch	32	VIM_INTVECTOR_67	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h71	50F0 210Ch
2110h	32	VIM_INTVECTOR_68	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h72	50F0 2110h
2114h	32	VIM_INTVECTOR_69	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h73	50F0 2114h
2118h	32	VIM_INTVECTOR_70	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h74	50F0 2118h
211Ch	32	VIM_INTVECTOR_71	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h75	50F0 211Ch
2120h	32	VIM_INTVECTOR_72	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h76	50F0 2120h
2124h	32	VIM_INTVECTOR_73	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h77	50F0 2124h
2128h	32	VIM_INTVECTOR_74	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h78	50F0 2128h
212Ch	32	VIM_INTVECTOR_75	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h79	50F0 212Ch
2130h	32	VIM_INTVECTOR_76	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h80	50F0 2130h
2134h	32	VIM_INTVECTOR_77	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h81	50F0 2134h
2138h	32	VIM_INTVECTOR_78	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h82	50F0 2138h
213Ch	32	VIM_INTVECTOR_79	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h83	50F0 213Ch
2140h	32	VIM_INTVECTOR_80	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h84	50F0 2140h
2144h	32	VIM_INTVECTOR_81	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h85	50F0 2144h
2148h	32	VIM_INTVECTOR_82	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h86	50F0 2148h
214Ch	32	VIM_INTVECTOR_83	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h87	50F0 214Ch
2150h	32	VIM_INTVECTOR_84	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h88	50F0 2150h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2154h	32	VIM_INTVECTOR_85	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h89	50F0 2154h
2158h	32	VIM_INTVECTOR_86	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h90	50F0 2158h
215Ch	32	VIM_INTVECTOR_87	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h91	50F0 215Ch
2160h	32	VIM_INTVECTOR_88	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h92	50F0 2160h
2164h	32	VIM_INTVECTOR_89	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h93	50F0 2164h
2168h	32	VIM_INTVECTOR_90	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h94	50F0 2168h
216Ch	32	VIM_INTVECTOR_91	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h95	50F0 216Ch
2170h	32	VIM_INTVECTOR_92	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h96	50F0 2170h
2174h	32	VIM_INTVECTOR_93	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h97	50F0 2174h
2178h	32	VIM_INTVECTOR_94	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h98	50F0 2178h
217Ch	32	VIM_INTVECTOR_95	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h99	50F0 217Ch
2180h	32	VIM_INTVECTOR_96	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h100	50F0 2180h
2184h	32	VIM_INTVECTOR_97	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h101	50F0 2184h
2188h	32	VIM_INTVECTOR_98	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h102	50F0 2188h
218Ch	32	VIM_INTVECTOR_99	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h103	50F0 218Ch
2190h	32	VIM_INTVECTOR_100	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h104	50F0 2190h
2194h	32	VIM_INTVECTOR_101	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h105	50F0 2194h
2198h	32	VIM_INTVECTOR_102	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h106	50F0 2198h
219Ch	32	VIM_INTVECTOR_103	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h107	50F0 219Ch

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
21A0h	32	VIM_INTVECTOR_104	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h108	50F0 21A0h
21A4h	32	VIM_INTVECTOR_105	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h109	50F0 21A4h
21A8h	32	VIM_INTVECTOR_106	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h110	50F0 21A8h
21ACh	32	VIM_INTVECTOR_107	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h111	50F0 21ACh
21B0h	32	VIM_INTVECTOR_108	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h112	50F0 21B0h
21B4h	32	VIM_INTVECTOR_109	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h113	50F0 21B4h
21B8h	32	VIM_INTVECTOR_110	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h114	50F0 21B8h
21BCh	32	VIM_INTVECTOR_111	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h115	50F0 21BCh
21C0h	32	VIM_INTVECTOR_112	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h116	50F0 21C0h
21C4h	32	VIM_INTVECTOR_113	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h117	50F0 21C4h
21C8h	32	VIM_INTVECTOR_114	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h118	50F0 21C8h
21CCh	32	VIM_INTVECTOR_115	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h119	50F0 21CCh
21D0h	32	VIM_INTVECTOR_116	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h120	50F0 21D0h
21D4h	32	VIM_INTVECTOR_117	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h121	50F0 21D4h
21D8h	32	VIM_INTVECTOR_118	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h122	50F0 21D8h
21DCh	32	VIM_INTVECTOR_119	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h123	50F0 21DCh
21E0h	32	VIM_INTVECTOR_120	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h124	50F0 21E0h
21E4h	32	VIM_INTVECTOR_121	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h125	50F0 21E4h
21E8h	32	VIM_INTVECTOR_122	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h126	50F0 21E8h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
21ECh	32	VIM_INTVECTOR_123	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h127	50F0 21ECh
21F0h	32	VIM_INTVECTOR_124	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h128	50F0 21F0h
21F4h	32	VIM_INTVECTOR_125	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h129	50F0 21F4h
21F8h	32	VIM_INTVECTOR_126	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h130	50F0 21F8h
21FCh	32	VIM_INTVECTOR_127	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h131	50F0 21FCh
2200h	32	VIM_INTVECTOR_128	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h132	50F0 2200h
2204h	32	VIM_INTVECTOR_129	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h133	50F0 2204h
2208h	32	VIM_INTVECTOR_130	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h134	50F0 2208h
220Ch	32	VIM_INTVECTOR_131	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h135	50F0 220Ch
2210h	32	VIM_INTVECTOR_132	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h136	50F0 2210h
2214h	32	VIM_INTVECTOR_133	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h137	50F0 2214h
2218h	32	VIM_INTVECTOR_134	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h138	50F0 2218h
221Ch	32	VIM_INTVECTOR_135	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h139	50F0 221Ch
2220h	32	VIM_INTVECTOR_136	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h140	50F0 2220h
2224h	32	VIM_INTVECTOR_137	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h141	50F0 2224h
2228h	32	VIM_INTVECTOR_138	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h142	50F0 2228h
222Ch	32	VIM_INTVECTOR_139	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h143	50F0 222Ch
2230h	32	VIM_INTVECTOR_140	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h144	50F0 2230h
2234h	32	VIM_INTVECTOR_141	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h145	50F0 2234h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2238h	32	VIM_INTVECTOR_142	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h146	50F0 2238h
223Ch	32	VIM_INTVECTOR_143	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h147	50F0 223Ch
2240h	32	VIM_INTVECTOR_144	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h148	50F0 2240h
2244h	32	VIM_INTVECTOR_145	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h149	50F0 2244h
2248h	32	VIM_INTVECTOR_146	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h150	50F0 2248h
224Ch	32	VIM_INTVECTOR_147	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h151	50F0 224Ch
2250h	32	VIM_INTVECTOR_148	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h152	50F0 2250h
2254h	32	VIM_INTVECTOR_149	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h153	50F0 2254h
2258h	32	VIM_INTVECTOR_150	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h154	50F0 2258h
225Ch	32	VIM_INTVECTOR_151	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h155	50F0 225Ch
2260h	32	VIM_INTVECTOR_152	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h156	50F0 2260h
2264h	32	VIM_INTVECTOR_153	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h157	50F0 2264h
2268h	32	VIM_INTVECTOR_154	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h158	50F0 2268h
226Ch	32	VIM_INTVECTOR_155	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h159	50F0 226Ch
2270h	32	VIM_INTVECTOR_156	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h160	50F0 2270h
2274h	32	VIM_INTVECTOR_157	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h161	50F0 2274h
2278h	32	VIM_INTVECTOR_158	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h162	50F0 2278h
227Ch	32	VIM_INTVECTOR_159	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h163	50F0 227Ch
2280h	32	VIM_INTVECTOR_160	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h164	50F0 2280h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2284h	32	VIM_INTVECTOR_161	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h165	50F0 2284h
2288h	32	VIM_INTVECTOR_162	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h166	50F0 2288h
228Ch	32	VIM_INTVECTOR_163	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h167	50F0 228Ch
2290h	32	VIM_INTVECTOR_164	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h168	50F0 2290h
2294h	32	VIM_INTVECTOR_165	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h169	50F0 2294h
2298h	32	VIM_INTVECTOR_166	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h170	50F0 2298h
229Ch	32	VIM_INTVECTOR_167	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h171	50F0 229Ch
22A0h	32	VIM_INTVECTOR_168	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h172	50F0 22A0h
22A4h	32	VIM_INTVECTOR_169	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h173	50F0 22A4h
22A8h	32	VIM_INTVECTOR_170	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h174	50F0 22A8h
22ACh	32	VIM_INTVECTOR_171	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h175	50F0 22ACh
22B0h	32	VIM_INTVECTOR_172	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h176	50F0 22B0h
22B4h	32	VIM_INTVECTOR_173	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h177	50F0 22B4h
22B8h	32	VIM_INTVECTOR_174	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h178	50F0 22B8h
22BCh	32	VIM_INTVECTOR_175	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h179	50F0 22BCh
22C0h	32	VIM_INTVECTOR_176	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h180	50F0 22C0h
22C4h	32	VIM_INTVECTOR_177	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h181	50F0 22C4h
22C8h	32	VIM_INTVECTOR_178	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h182	50F0 22C8h
22CCh	32	VIM_INTVECTOR_179	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h183	50F0 22CCh

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
22D0h	32	VIM_INTVECTOR_180	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h184	50F0 22D0h
22D4h	32	VIM_INTVECTOR_181	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h185	50F0 22D4h
22D8h	32	VIM_INTVECTOR_182	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h186	50F0 22D8h
22DCh	32	VIM_INTVECTOR_183	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h187	50F0 22DCh
22E0h	32	VIM_INTVECTOR_184	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h188	50F0 22E0h
22E4h	32	VIM_INTVECTOR_185	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h189	50F0 22E4h
22E8h	32	VIM_INTVECTOR_186	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h190	50F0 22E8h
22ECh	32	VIM_INTVECTOR_187	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h191	50F0 22ECh
22F0h	32	VIM_INTVECTOR_188	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h192	50F0 22F0h
22F4h	32	VIM_INTVECTOR_189	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h193	50F0 22F4h
22F8h	32	VIM_INTVECTOR_190	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h194	50F0 22F8h
22FCh	32	VIM_INTVECTOR_191	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h195	50F0 22FCh
2300h	32	VIM_INTVECTOR_192	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h196	50F0 2300h
2304h	32	VIM_INTVECTOR_193	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h197	50F0 2304h
2308h	32	VIM_INTVECTOR_194	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h198	50F0 2308h
230Ch	32	VIM_INTVECTOR_195	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h199	50F0 230Ch
2310h	32	VIM_INTVECTOR_196	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h200	50F0 2310h
2314h	32	VIM_INTVECTOR_197	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h201	50F0 2314h
2318h	32	VIM_INTVECTOR_198	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h202	50F0 2318h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
231Ch	32	VIM_INTVECTOR_199	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h203	50F0 231Ch
2320h	32	VIM_INTVECTOR_200	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h204	50F0 2320h
2324h	32	VIM_INTVECTOR_201	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h205	50F0 2324h
2328h	32	VIM_INTVECTOR_202	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h206	50F0 2328h
232Ch	32	VIM_INTVECTOR_203	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h207	50F0 232Ch
2330h	32	VIM_INTVECTOR_204	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h208	50F0 2330h
2334h	32	VIM_INTVECTOR_205	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h209	50F0 2334h
2338h	32	VIM_INTVECTOR_206	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h210	50F0 2338h
233Ch	32	VIM_INTVECTOR_207	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h211	50F0 233Ch
2340h	32	VIM_INTVECTOR_208	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h212	50F0 2340h
2344h	32	VIM_INTVECTOR_209	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h213	50F0 2344h
2348h	32	VIM_INTVECTOR_210	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h214	50F0 2348h
234Ch	32	VIM_INTVECTOR_211	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h215	50F0 234Ch
2350h	32	VIM_INTVECTOR_212	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h216	50F0 2350h
2354h	32	VIM_INTVECTOR_213	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h217	50F0 2354h
2358h	32	VIM_INTVECTOR_214	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h218	50F0 2358h
235Ch	32	VIM_INTVECTOR_215	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h219	50F0 235Ch
2360h	32	VIM_INTVECTOR_216	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h220	50F0 2360h
2364h	32	VIM_INTVECTOR_217	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h221	50F0 2364h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
2368h	32	VIM_INTVECTOR_218	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h222	50F0 2368h
236Ch	32	VIM_INTVECTOR_219	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h223	50F0 236Ch
2370h	32	VIM_INTVECTOR_220	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h224	50F0 2370h
2374h	32	VIM_INTVECTOR_221	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h225	50F0 2374h
2378h	32	VIM_INTVECTOR_222	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h226	50F0 2378h
237Ch	32	VIM_INTVECTOR_223	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h227	50F0 237Ch
2380h	32	VIM_INTVECTOR_224	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h228	50F0 2380h
2384h	32	VIM_INTVECTOR_225	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h229	50F0 2384h
2388h	32	VIM_INTVECTOR_226	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h230	50F0 2388h
238Ch	32	VIM_INTVECTOR_227	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h231	50F0 238Ch
2390h	32	VIM_INTVECTOR_228	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h232	50F0 2390h
2394h	32	VIM_INTVECTOR_229	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h233	50F0 2394h
2398h	32	VIM_INTVECTOR_230	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h234	50F0 2398h
239Ch	32	VIM_INTVECTOR_231	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h235	50F0 239Ch
23A0h	32	VIM_INTVECTOR_232	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h236	50F0 23A0h
23A4h	32	VIM_INTVECTOR_233	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h237	50F0 23A4h
23A8h	32	VIM_INTVECTOR_234	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h238	50F0 23A8h
23ACh	32	VIM_INTVECTOR_235	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h239	50F0 23ACh
23B0h	32	VIM_INTVECTOR_236	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h240	50F0 23B0h

Table 4-2879. VIM, VIM_VIM Registers, Base Address=50F0 0000H, Length=9 (continued)

Offset	Length	Acronym	Register Name	VIM Physical Address
23B4h	32	VIM_INTVECTOR_237	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h241	50F0 23B4h
23B8h	32	VIM_INTVECTOR_238	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h242	50F0 23B8h
23BCh	32	VIM_INTVECTOR_239	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h243	50F0 23BCh
23C0h	32	VIM_INTVECTOR_240	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h244	50F0 23C0h
23C4h	32	VIM_INTVECTOR_241	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h245	50F0 23C4h
23C8h	32	VIM_INTVECTOR_242	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h246	50F0 23C8h
23CCh	32	VIM_INTVECTOR_243	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h247	50F0 23CCh
23D0h	32	VIM_INTVECTOR_244	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h248	50F0 23D0h
23D4h	32	VIM_INTVECTOR_245	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h249	50F0 23D4h
23D8h	32	VIM_INTVECTOR_246	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h250	50F0 23D8h
23DCh	32	VIM_INTVECTOR_247	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h251	50F0 23DCh
23E0h	32	VIM_INTVECTOR_248	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h252	50F0 23E0h
23E4h	32	VIM_INTVECTOR_249	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h253	50F0 23E4h
23E8h	32	VIM_INTVECTOR_250	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h254	50F0 23E8h
23ECh	32	VIM_INTVECTOR_251	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h255	50F0 23ECh
23F0h	32	VIM_INTVECTOR_252	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h256	50F0 23F0h
23F4h	32	VIM_INTVECTOR_253	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h257	50F0 23F4h
23F8h	32	VIM_INTVECTOR_254	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h258	50F0 23F8h
23FCh	32	VIM_INTVECTOR_255	Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h259	50F0 23FCh

4.30.1 VIM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description:

Return to Summary Table

Table 4-2880. Instance Table

Instance Name	Physical Address
VIM	50F0 0000h

Figure 4-1372. VIM_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
RO		RO		RO											
1		10		10010000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
0					0			0		1					

Access Types Legend

Table 4-2881. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	FUNC	RO	98BD90h	Module ID
15 - 11	RTL	RO	0h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	0h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

4.30.2 VIM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this VIM.

Long Description:

Return to Summary Table

Table 4-2882. Instance Table

Instance Name	Physical Address
VIM	50F0 0004h

Figure 4-1373. VIM_INFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1					INTERRUPTS										
RO					RO										
0					100000000										

Access Types Legend

Table 4-2883. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	RES1	RO	0h	RESERVE FIELD
10 - 0	INTERRUPTS	RO	5F5E100h	Total number of Interrupts

4.30.3 VIM_PRIIRQ Register (Offset = 8h) [reset = h]

Short Description: The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Long Description:

Return to Summary Table

Table 4-2884. Instance Table

Instance Name	Physical Address
VIM	50F0 0008h

Figure 4-1374. VIM_PRIIRQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES2											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-2885. PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES2	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES3	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending IRQ. valid only if the valid flag is set.

4.30.4 VIM_PRIFIQ Register (Offset = Ch) [reset = h]

Short Description: The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Long Description:

Return to Summary Table

Table 4-2886. Instance Table

Instance Name	Physical Address
VIM	50F0 000Ch

Figure 4-1375. VIM_PRIFIQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES4											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES5						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-2887. PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES4	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending FIQ. valid only if the valid flag is set.
15 - 10	RES5	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending FIQ. valid only if the valid flag is set.

4.30.5 VIM_IRQGSTS Register (Offset = 10h) [reset = h]

Short Description: The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Long Description:

Return to Summary Table

Table 4-2888. Instance Table

Instance Name	Physical Address
VIM	50F0 0010h

Figure 4-1376. VIM_IRQGSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-2889. IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

4.30.6 VIM_FIQGSTS Register (Offset = 14h) [reset = h]

Short Description: The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Long Description:

Return to Summary Table

Table 4-2890. Instance Table

Instance Name	Physical Address
VIM	50F0 0014h

Figure 4-1377. VIM_FIQGSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-2891. FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

4.30.7 VIM_IRQVEC Register (Offset = 18h) [reset = h]

Short Description: The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

Long Description:

Return to Summary Table

Table 4-2892. Instance Table

Instance Name	Physical Address
VIM	50F0 0018h

Figure 4-1378. VIM_IRQVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES21	
RW														RO	
0														0	

Access Types Legend

Table 4-2893. IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true.
1 - 0	RES21	RO	0h	RESERVE FIELD

4.30.8 VIM_FIQVEC Register (Offset = 1Ch) [reset = h]

Short Description: The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

Long Description:

Return to Summary Table

Table 4-2894. Instance Table

Instance Name	Physical Address
VIM	50F0 001Ch

Figure 4-1379. VIM_FIQVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES22	
RW														RO	
0														0	

Access Types Legend

Table 4-2895. FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true.
1 - 0	RES22	RO	0h	RESERVE FIELD

4.30.9 VIM_ACTIRQ Register (Offset = 20h) [reset = h]

Short Description: The Active IRQ Register shows the number of the currently active IRQ.

Long Description:

Return to Summary Table

Table 4-2896. Instance Table

Instance Name	Physical Address
VIM	50F0 0020h

Figure 4-1380. VIM_ACTIRQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES6											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES7						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-2897. ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.
30 - 20	RES6	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES7	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set.

4.30.10 VIM_ACTFIQ Register (Offset = 24h) [reset = h]

Short Description: The Active FIQ Register shows the number of the currently active FIQ.

Long Description:

Return to Summary Table

Table 4-2898. Instance Table

Instance Name	Physical Address
VIM	50F0 0024h

Figure 4-1381. VIM_ACTFIQ Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALID	RES8											PRI			
RO	RO											RO			
0	0											0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES9						NUM									
RO						RO									
0						0									

Access Types Legend

Table 4-2899. ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.
30 - 20	RES8	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES9	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set.

4.30.11 VIM_IRQPRIMSK Register (Offset = 28h) [reset = h]

Short Description: The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Long Description:

Return to Summary Table

Table 4-2900. Instance Table

Instance Name	Physical Address
VIM	50F0 0028h

Figure 4-1382. VIM_IRQPRIMSK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK															
RW															
1111111111111111															

Access Types Legend

Table 4-2901. IRQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	3F28CB715 71C7h	Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled.

4.30.12 VIM_FIQPRIMSK Register (Offset = 2Ch) [reset = h]

Short Description: The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Long Description:

Return to Summary Table

Table 4-2902. Instance Table

Instance Name	Physical Address
VIM	50F0 002Ch

Figure 4-1383. VIM_FIQPRIMSK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSK															
RW															
1111111111111111															

Access Types Legend

Table 4-2903. FIQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	3F28CB715 71C7h	Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled.

4.30.13 VIM_DEDVEC Register (Offset = 30h) [reset = h]

Short Description: The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Long Description:

Return to Summary Table

Table 4-2904. Instance Table

Instance Name	Physical Address
VIM	50F0 0030h

Figure 4-1384. VIM_DEDVEC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES23	
RW														RO	
0														0	

Access Types Legend

Table 4-2905. DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address.
1 - 0	RES23	RO	0h	RESERVE FIELD

4.30.14 VIM_RAW Register (Offset = 400h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2906. Instance Table

Instance Name	Physical Address
VIM	50F0 0400h

Figure 4-1385. VIM_RAW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2907. RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.15 VIM_STS Register (Offset = 404h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2908. Instance Table

Instance Name	Physical Address
VIM	50F0 0404h

Figure 4-1386. VIM_STS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2909. STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.16 VIM_INTR_EN_SET Register (Offset = 408h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2910. Instance Table

Instance Name	Physical Address
VIM	50F0 0408h

Figure 4-1387. VIM_INTR_EN_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2911. INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.17 VIM_INTER_EN_CLR Register (Offset = 40Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2912. Instance Table

Instance Name	Physical Address
VIM	50F0 040Ch

Figure 4-1388. VIM_INTER_EN_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2913. INTER_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.18 VIM_IRQSTS Register (Offset = 410h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2914. Instance Table

Instance Name	Physical Address
VIM	50F0 0410h

Figure 4-1389. VIM_IRQSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2915. IRQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.19 VIM_FIQSTS Register (Offset = 414h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2916. Instance Table

Instance Name	Physical Address
VIM	50F0 0414h

Figure 4-1390. VIM_FIQSTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2917. FIQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.20 VIM_INTMAP Register (Offset = 418h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2918. Instance Table

Instance Name	Physical Address
VIM	50F0 0418h

Figure 4-1391. VIM_INTMAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2919. INTMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.21 VIM_INTTYPE Register (Offset = 41Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2920. Instance Table

Instance Name	Physical Address
VIM	50F0 041Ch

Figure 4-1392. VIM_INTTYPE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-2921. INTTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.22 VIM_RAW_1 Register (Offset = 420h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2922. Instance Table

Instance Name	Physical Address
VIM	50F0 0420h

Figure 4-1393. VIM_RAW_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2923. RAW_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.23 VIM_STS_1 Register (Offset = 424h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2924. Instance Table

Instance Name	Physical Address
VIM	50F0 0424h

Figure 4-1394. VIM_STS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2925. STS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.24 VIM_INTR_EN_SET_1 Register (Offset = 428h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2926. Instance Table

Instance Name	Physical Address
VIM	50F0 0428h

Figure 4-1395. VIM_INTR_EN_SET_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2927. INTR_EN_SET_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.25 VIM_INTER_EN_CLR_1 Register (Offset = 42Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2928. Instance Table

Instance Name	Physical Address
VIM	50F0 042Ch

Figure 4-1396. VIM_INTER_EN_CLR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2929. INTER_EN_CLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.26 VIM_IRQSTS_1 Register (Offset = 430h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2930. Instance Table

Instance Name	Physical Address
VIM	50F0 0430h

Figure 4-1397. VIM_IRQSTS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2931. IRQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.27 VIM_FIQSTS_1 Register (Offset = 434h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2932. Instance Table

Instance Name	Physical Address
VIM	50F0 0434h

Figure 4-1398. VIM_FIQSTS_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2933. FIQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.28 VIM_INTMAP_1 Register (Offset = 438h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2934. Instance Table

Instance Name	Physical Address
VIM	50F0 0438h

Figure 4-1399. VIM_INTMAP_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2935. INTMAP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.29 VIM_INTTYPE_1 Register (Offset = 43Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2936. Instance Table

Instance Name	Physical Address
VIM	50F0 043Ch

Figure 4-1400. VIM_INTTYPE_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-2937. INTTYPE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.30 VIM_RAW_2 Register (Offset = 440h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2938. Instance Table

Instance Name	Physical Address
VIM	50F0 0440h

Figure 4-1401. VIM_RAW_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2939. RAW_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.31 VIM_STS_2 Register (Offset = 444h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2940. Instance Table

Instance Name	Physical Address
VIM	50F0 0444h

Figure 4-1402. VIM_STS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2941. STS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.32 VIM_INTR_EN_SET_2 Register (Offset = 448h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2942. Instance Table

Instance Name	Physical Address
VIM	50F0 0448h

Figure 4-1403. VIM_INTR_EN_SET_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2943. INTR_EN_SET_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.33 VIM_INTER_EN_CLR_2 Register (Offset = 44Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2944. Instance Table

Instance Name	Physical Address
VIM	50F0 044Ch

Figure 4-1404. VIM_INTER_EN_CLR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2945. INTER_EN_CLR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.34 VIM_IRQSTS_2 Register (Offset = 450h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2946. Instance Table

Instance Name	Physical Address
VIM	50F0 0450h

Figure 4-1405. VIM_IRQSTS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2947. IRQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.35 VIM_FIQSTS_2 Register (Offset = 454h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2948. Instance Table

Instance Name	Physical Address
VIM	50F0 0454h

Figure 4-1406. VIM_FIQSTS_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2949. FIQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.36 VIM_INTMAP_2 Register (Offset = 458h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2950. Instance Table

Instance Name	Physical Address
VIM	50F0 0458h

Figure 4-1407. VIM_INTMAP_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2951. INTMAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.37 VIM_INTTYPE_2 Register (Offset = 45Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2952. Instance Table

Instance Name	Physical Address
VIM	50F0 045Ch

Figure 4-1408. VIM_INTTYPE_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-2953. INTTYPE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.38 VIM_RAW_3 Register (Offset = 460h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2954. Instance Table

Instance Name	Physical Address
VIM	50F0 0460h

Figure 4-1409. VIM_RAW_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2955. RAW_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.39 VIM_STS_3 Register (Offset = 464h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2956. Instance Table

Instance Name	Physical Address
VIM	50F0 0464h

Figure 4-1410. VIM_STS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2957. STS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.40 VIM_INTR_EN_SET_3 Register (Offset = 468h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2958. Instance Table

Instance Name	Physical Address
VIM	50F0 0468h

Figure 4-1411. VIM_INTR_EN_SET_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2959. INTR_EN_SET_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.41 VIM_INTER_EN_CLR_3 Register (Offset = 46Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2960. Instance Table

Instance Name	Physical Address
VIM	50F0 046Ch

Figure 4-1412. VIM_INTER_EN_CLR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2961. INTER_EN_CLR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.42 VIM_IRQSTS_3 Register (Offset = 470h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2962. Instance Table

Instance Name	Physical Address
VIM	50F0 0470h

Figure 4-1413. VIM_IRQSTS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2963. IRQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.43 VIM_FIQSTS_3 Register (Offset = 474h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2964. Instance Table

Instance Name	Physical Address
VIM	50F0 0474h

Figure 4-1414. VIM_FIQSTS_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2965. FIQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.44 VIM_INTMAP_3 Register (Offset = 478h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2966. Instance Table

Instance Name	Physical Address
VIM	50F0 0478h

Figure 4-1415. VIM_INTMAP_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2967. INTMAP_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.45 VIM_INTTYPE_3 Register (Offset = 47Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2968. Instance Table

Instance Name	Physical Address
VIM	50F0 047Ch

Figure 4-1416. VIM_INTTYPE_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-2969. INTTYPE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.46 VIM_RAW_4 Register (Offset = 480h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2970. Instance Table

Instance Name	Physical Address
VIM	50F0 0480h

Figure 4-1417. VIM_RAW_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2971. RAW_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.47 VIM_STS_4 Register (Offset = 484h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2972. Instance Table

Instance Name	Physical Address
VIM	50F0 0484h

Figure 4-1418. VIM_STS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2973. STS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.48 VIM_INTR_EN_SET_4 Register (Offset = 488h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2974. Instance Table

Instance Name	Physical Address
VIM	50F0 0488h

Figure 4-1419. VIM_INTR_EN_SET_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2975. INTR_EN_SET_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.49 VIM_INTER_EN_CLR_4 Register (Offset = 48Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2976. Instance Table

Instance Name	Physical Address
VIM	50F0 048Ch

Figure 4-1420. VIM_INTER_EN_CLR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2977. INTER_EN_CLR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.50 VIM_IRQSTS_4 Register (Offset = 490h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2978. Instance Table

Instance Name	Physical Address
VIM	50F0 0490h

Figure 4-1421. VIM_IRQSTS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2979. IRQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.51 VIM_FIQSTS_4 Register (Offset = 494h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2980. Instance Table

Instance Name	Physical Address
VIM	50F0 0494h

Figure 4-1422. VIM_FIQSTS_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2981. FIQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.52 VIM_INTMAP_4 Register (Offset = 498h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2982. Instance Table

Instance Name	Physical Address
VIM	50F0 0498h

Figure 4-1423. VIM_INTMAP_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2983. INTMAP_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.53 VIM_INTTYPE_4 Register (Offset = 49Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2984. Instance Table

Instance Name	Physical Address
VIM	50F0 049Ch

Figure 4-1424. VIM_INTTYPE_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-2985. INTTYPE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.54 VIM_RAW_5 Register (Offset = 4A0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2986. Instance Table

Instance Name	Physical Address
VIM	50F0 04A0h

Figure 4-1425. VIM_RAW_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-2987. RAW_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.55 VIM_STS_5 Register (Offset = 4A4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2988. Instance Table

Instance Name	Physical Address
VIM	50F0 04A4h

Figure 4-1426. VIM_STS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2989. STS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.56 VIM_INTR_EN_SET_5 Register (Offset = 4A8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2990. Instance Table

Instance Name	Physical Address
VIM	50F0 04A8h

Figure 4-1427. VIM_INTR_EN_SET_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2991. INTR_EN_SET_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.57 VIM_INTER_EN_CLR_5 Register (Offset = 4ACh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2992. Instance Table

Instance Name	Physical Address
VIM	50F0 04ACh

Figure 4-1428. VIM_INTER_EN_CLR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2993. INTER_EN_CLR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.58 VIM_IRQSTS_5 Register (Offset = 4B0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2994. Instance Table

Instance Name	Physical Address
VIM	50F0 04B0h

Figure 4-1429. VIM_IRQSTS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2995. IRQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.59 VIM_FIQSTS_5 Register (Offset = 4B4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2996. Instance Table

Instance Name	Physical Address
VIM	50F0 04B4h

Figure 4-1430. VIM_FIQSTS_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2997. FIQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.60 VIM_INTMAP_5 Register (Offset = 4B8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2998. Instance Table

Instance Name	Physical Address
VIM	50F0 04B8h

Figure 4-1431. VIM_INTMAP_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-2999. INTMAP_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.61 VIM_INTTYPE_5 Register (Offset = 4BCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-3000. Instance Table

Instance Name	Physical Address
VIM	50F0 04BCh

Figure 4-1432. VIM_INTTYPE_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3001. INTTYPE_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.62 VIM_RAW_6 Register (Offset = 4C0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-3002. Instance Table

Instance Name	Physical Address
VIM	50F0 04C0h

Figure 4-1433. VIM_RAW_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3003. RAW_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.63 VIM_STS_6 Register (Offset = 4C4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-3004. Instance Table

Instance Name	Physical Address
VIM	50F0 04C4h

Figure 4-1434. VIM_STS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3005. STS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.64 VIM_INTR_EN_SET_6 Register (Offset = 4C8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-3006. Instance Table

Instance Name	Physical Address
VIM	50F0 04C8h

Figure 4-1435. VIM_INTR_EN_SET_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3007. INTR_EN_SET_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.65 VIM_INTER_EN_CLR_6 Register (Offset = 4CCh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-3008. Instance Table

Instance Name	Physical Address
VIM	50F0 04CCh

Figure 4-1436. VIM_INTER_EN_CLR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3009. INTER_EN_CLR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.66 VIM_IRQSTS_6 Register (Offset = 4D0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-3010. Instance Table

Instance Name	Physical Address
VIM	50F0 04D0h

Figure 4-1437. VIM_IRQSTS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3011. IRQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.67 VIM_FIQSTS_6 Register (Offset = 4D4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-3012. Instance Table

Instance Name	Physical Address
VIM	50F0 04D4h

Figure 4-1438. VIM_FIQSTS_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3013. FIQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.68 VIM_INTMAP_6 Register (Offset = 4D8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-3014. Instance Table

Instance Name	Physical Address
VIM	50F0 04D8h

Figure 4-1439. VIM_INTMAP_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3015. INTMAP_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.69 VIM_INTTYPE_6 Register (Offset = 4DCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-3016. Instance Table

Instance Name	Physical Address
VIM	50F0 04DCh

Figure 4-1440. VIM_INTTYPE_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3017. INTTYPE_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.70 VIM_RAW_7 Register (Offset = 4E0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-3018. Instance Table

Instance Name	Physical Address
VIM	50F0 04E0h

Figure 4-1441. VIM_RAW_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RW															
0															

Access Types Legend

Table 4-3019. RAW_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

4.30.71 VIM_STS_7 Register (Offset = 4E4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-3020. Instance Table

Instance Name	Physical Address
VIM	50F0 04E4h

Figure 4-1442. VIM_STS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3021. STS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

4.30.72 VIM_INTR_EN_SET_7 Register (Offset = 4E8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-3022. Instance Table

Instance Name	Physical Address
VIM	50F0 04E8h

Figure 4-1443. VIM_INTR_EN_SET_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3023. INTR_EN_SET_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

4.30.73 VIM_INTER_EN_CLR_7 Register (Offset = 4ECh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-3024. Instance Table

Instance Name	Physical Address
VIM	50F0 04ECh

Figure 4-1444. VIM_INTER_EN_CLR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3025. INTER_EN_CLR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

4.30.74 VIM_IRQSTS_7 Register (Offset = 4F0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-3026. Instance Table

Instance Name	Physical Address
VIM	50F0 04F0h

Figure 4-1445. VIM_IRQSTS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3027. IRQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

4.30.75 VIM_FIQSTS_7 Register (Offset = 4F4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-3028. Instance Table

Instance Name	Physical Address
VIM	50F0 04F4h

Figure 4-1446. VIM_FIQSTS_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3029. FIQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

4.30.76 VIM_INTMAP_7 Register (Offset = 4F8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-3030. Instance Table

Instance Name	Physical Address
VIM	50F0 04F8h

Figure 4-1447. VIM_INTMAP_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK															
RW															
0															

Access Types Legend

Table 4-3031. INTMAP_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

4.30.77 VIM_INTTYPE_7 Register (Offset = 4FCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-3032. Instance Table

Instance Name	Physical Address
VIM	50F0 04FCh

Figure 4-1448. VIM_INTTYPE_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VAL															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL															
RW															
0															

Access Types Legend

Table 4-3033. INTTYPE_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

4.30.78 VIM_INTPRIORITY Register (Offset = 1000h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h4

Long Description:

Return to Summary Table

Table 4-3034. Instance Table

Instance Name	Physical Address
VIM	50F0 1000h

Figure 4-1449. VIM_INTPRIORITY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3035. INTPRIORITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.79 VIM_INTPRIORITY_1 Register (Offset = 1004h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h5

Long Description:

Return to Summary Table

Table 4-3036. Instance Table

Instance Name	Physical Address
VIM	50F0 1004h

Figure 4-1450. VIM_INTPRIORITY_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3037. INTPRIORITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.80 VIM_INTPRIORITY_2 Register (Offset = 1008h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h6

Long Description:

Return to Summary Table

Table 4-3038. Instance Table

Instance Name	Physical Address
VIM	50F0 1008h

Figure 4-1451. VIM_INTPRIORITY_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3039. INTPRIORITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.81 VIM_INTPRIORITY_3 Register (Offset = 100Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h7

Long Description:

Return to Summary Table

Table 4-3040. Instance Table

Instance Name	Physical Address
VIM	50F0 100Ch

Figure 4-1452. VIM_INTPRIORITY_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3041. INTPRIORITY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.82 VIM_INTPRIORITY_4 Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h8

Long Description:

Return to Summary Table

Table 4-3042. Instance Table

Instance Name	Physical Address
VIM	50F0 1010h

Figure 4-1453. VIM_INTPRIORITY_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3043. INTPRIORITY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.83 VIM_INTPRIORITY_5 Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h9

Long Description:

Return to Summary Table

Table 4-3044. Instance Table

Instance Name	Physical Address
VIM	50F0 1014h

Figure 4-1454. VIM_INTPRIORITY_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3045. INTPRIORITY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.84 VIM_INTPRIORITY_6 Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h10

Long Description:

Return to Summary Table

Table 4-3046. Instance Table

Instance Name	Physical Address
VIM	50F0 1018h

Figure 4-1455. VIM_INTPRIORITY_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3047. INTPRIORITY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.85 VIM_INTPRIORITY_7 Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h11

Long Description:

Return to Summary Table

Table 4-3048. Instance Table

Instance Name	Physical Address
VIM	50F0 101Ch

Figure 4-1456. VIM_INTPRIORITY_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3049. INTPRIORITY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.86 VIM_INTPRIORITY_8 Register (Offset = 1020h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h12

Long Description:

Return to Summary Table

Table 4-3050. Instance Table

Instance Name	Physical Address
VIM	50F0 1020h

Figure 4-1457. VIM_INTPRIORITY_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3051. INTPRIORITY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.87 VIM_INTPRIORITY_9 Register (Offset = 1024h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h13

Long Description:

Return to Summary Table

Table 4-3052. Instance Table

Instance Name	Physical Address
VIM	50F0 1024h

Figure 4-1458. VIM_INTPRIORITY_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3053. INTPRIORITY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.88 VIM_INTPRIORITY_10 Register (Offset = 1028h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h14

Long Description:

Return to Summary Table

Table 4-3054. Instance Table

Instance Name	Physical Address
VIM	50F0 1028h

Figure 4-1459. VIM_INTPRIORITY_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3055. INTPRIORITY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.89 VIM_INTPRIORITY_11 Register (Offset = 102Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h15

Long Description:

Return to Summary Table

Table 4-3056. Instance Table

Instance Name	Physical Address
VIM	50F0 102Ch

Figure 4-1460. VIM_INTPRIORITY_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3057. INTPRIORITY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.90 VIM_INTPRIORITY_12 Register (Offset = 1030h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h16

Long Description:

Return to Summary Table

Table 4-3058. Instance Table

Instance Name	Physical Address
VIM	50F0 1030h

Figure 4-1461. VIM_INTPRIORITY_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3059. INTPRIORITY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.91 VIM_INTPRIORITY_13 Register (Offset = 1034h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h17

Long Description:

Return to Summary Table

Table 4-3060. Instance Table

Instance Name	Physical Address
VIM	50F0 1034h

Figure 4-1462. VIM_INTPRIORITY_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3061. INTPRIORITY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.92 VIM_INTPRIORITY_14 Register (Offset = 1038h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h18

Long Description:

Return to Summary Table

Table 4-3062. Instance Table

Instance Name	Physical Address
VIM	50F0 1038h

Figure 4-1463. VIM_INTPRIORITY_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3063. INTPRIORITY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.93 VIM_INTPRIORITY_15 Register (Offset = 103Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h19

Long Description:

Return to Summary Table

Table 4-3064. Instance Table

Instance Name	Physical Address
VIM	50F0 103Ch

Figure 4-1464. VIM_INTPRIORITY_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3065. INTPRIORITY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.94 VIM_INTPRIORITY_16 Register (Offset = 1040h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h20

Long Description:

Return to Summary Table

Table 4-3066. Instance Table

Instance Name	Physical Address
VIM	50F0 1040h

Figure 4-1465. VIM_INTPRIORITY_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3067. INTPRIORITY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.95 VIM_INTPRIORITY_17 Register (Offset = 1044h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h21

Long Description:

Return to Summary Table

Table 4-3068. Instance Table

Instance Name	Physical Address
VIM	50F0 1044h

Figure 4-1466. VIM_INTPRIORITY_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3069. INTPRIORITY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.96 VIM_INTPRIORITY_18 Register (Offset = 1048h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h22

Long Description:

Return to Summary Table

Table 4-3070. Instance Table

Instance Name	Physical Address
VIM	50F0 1048h

Figure 4-1467. VIM_INTPRIORITY_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3071. INTPRIORITY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.97 VIM_INTPRIORITY_19 Register (Offset = 104Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h23

Long Description:

Return to Summary Table

Table 4-3072. Instance Table

Instance Name	Physical Address
VIM	50F0 104Ch

Figure 4-1468. VIM_INTPRIORITY_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3073. INTPRIORITY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.98 VIM_INTPRIORITY_20 Register (Offset = 1050h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h24

Long Description:

Return to Summary Table

Table 4-3074. Instance Table

Instance Name	Physical Address
VIM	50F0 1050h

Figure 4-1469. VIM_INTPRIORITY_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3075. INTPRIORITY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.99 VIM_INTPRIORITY_21 Register (Offset = 1054h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h25

Long Description:

Return to Summary Table

Table 4-3076. Instance Table

Instance Name	Physical Address
VIM	50F0 1054h

Figure 4-1470. VIM_INTPRIORITY_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3077. INTPRIORITY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.100 VIM_INTPRIORITY_22 Register (Offset = 1058h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h26

Long Description:

Return to Summary Table

Table 4-3078. Instance Table

Instance Name	Physical Address
VIM	50F0 1058h

Figure 4-1471. VIM_INTPRIORITY_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3079. INTPRIORITY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.101 VIM_INTPRIORITY_23 Register (Offset = 105Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h27

Long Description:

Return to Summary Table

Table 4-3080. Instance Table

Instance Name	Physical Address
VIM	50F0 105Ch

Figure 4-1472. VIM_INTPRIORITY_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3081. INTPRIORITY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.102 VIM_INTPRIORITY_24 Register (Offset = 1060h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h28

Long Description:

Return to Summary Table

Table 4-3082. Instance Table

Instance Name	Physical Address
VIM	50F0 1060h

Figure 4-1473. VIM_INTPRIORITY_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3083. INTPRIORITY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.103 VIM_INTPRIORITY_25 Register (Offset = 1064h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h29

Long Description:

Return to Summary Table

Table 4-3084. Instance Table

Instance Name	Physical Address
VIM	50F0 1064h

Figure 4-1474. VIM_INTPRIORITY_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3085. INTPRIORITY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.104 VIM_INTPRIORITY_26 Register (Offset = 1068h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h30

Long Description:

Return to Summary Table

Table 4-3086. Instance Table

Instance Name	Physical Address
VIM	50F0 1068h

Figure 4-1475. VIM_INTPRIORITY_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3087. INTPRIORITY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.105 VIM_INTPRIORITY_27 Register (Offset = 106Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h31

Long Description:

Return to Summary Table

Table 4-3088. Instance Table

Instance Name	Physical Address
VIM	50F0 106Ch

Figure 4-1476. VIM_INTPRIORITY_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3089. INTPRIORITY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.106 VIM_INTPRIORITY_28 Register (Offset = 1070h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h32

Long Description:

Return to Summary Table

Table 4-3090. Instance Table

Instance Name	Physical Address
VIM	50F0 1070h

Figure 4-1477. VIM_INTPRIORITY_28 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3091. INTPRIORITY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.107 VIM_INTPRIORITY_29 Register (Offset = 1074h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h33

Long Description:

Return to Summary Table

Table 4-3092. Instance Table

Instance Name	Physical Address
VIM	50F0 1074h

Figure 4-1478. VIM_INTPRIORITY_29 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3093. INTPRIORITY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.108 VIM_INTPRIORITY_30 Register (Offset = 1078h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h34

Long Description:

Return to Summary Table

Table 4-3094. Instance Table

Instance Name	Physical Address
VIM	50F0 1078h

Figure 4-1479. VIM_INTPRIORITY_30 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3095. INTPRIORITY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.109 VIM_INTPRIORITY_31 Register (Offset = 107Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h35

Long Description:

Return to Summary Table

Table 4-3096. Instance Table

Instance Name	Physical Address
VIM	50F0 107Ch

Figure 4-1480. VIM_INTPRIORITY_31 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3097. INTPRIORITY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.110 VIM_INTPRIORITY_32 Register (Offset = 1080h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h36

Long Description:

Return to Summary Table

Table 4-3098. Instance Table

Instance Name	Physical Address
VIM	50F0 1080h

Figure 4-1481. VIM_INTPRIORITY_32 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3099. INTPRIORITY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.111 VIM_INTPRIORITY_33 Register (Offset = 1084h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h37

Long Description:

Return to Summary Table

Table 4-3100. Instance Table

Instance Name	Physical Address
VIM	50F0 1084h

Figure 4-1482. VIM_INTPRIORITY_33 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3101. INTPRIORITY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.112 VIM_INTPRIORITY_34 Register (Offset = 1088h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h38

Long Description:

Return to Summary Table

Table 4-3102. Instance Table

Instance Name	Physical Address
VIM	50F0 1088h

Figure 4-1483. VIM_INTPRIORITY_34 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3103. INTPRIORITY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.113 VIM_INTPRIORITY_35 Register (Offset = 108Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h39

Long Description:

Return to Summary Table

Table 4-3104. Instance Table

Instance Name	Physical Address
VIM	50F0 108Ch

Figure 4-1484. VIM_INTPRIORITY_35 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3105. INTPRIORITY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.114 VIM_INTPRIORITY_36 Register (Offset = 1090h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h40

Long Description:

Return to Summary Table

Table 4-3106. Instance Table

Instance Name	Physical Address
VIM	50F0 1090h

Figure 4-1485. VIM_INTPRIORITY_36 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3107. INTPRIORITY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.115 VIM_INTPRIORITY_37 Register (Offset = 1094h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h41

Long Description:

Return to Summary Table

Table 4-3108. Instance Table

Instance Name	Physical Address
VIM	50F0 1094h

Figure 4-1486. VIM_INTPRIORITY_37 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3109. INTPRIORITY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.116 VIM_INTPRIORITY_38 Register (Offset = 1098h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h42

Long Description:

Return to Summary Table

Table 4-3110. Instance Table

Instance Name	Physical Address
VIM	50F0 1098h

Figure 4-1487. VIM_INTPRIORITY_38 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3111. INTPRIORITY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.117 VIM_INTPRIORITY_39 Register (Offset = 109Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h43

Long Description:

Return to Summary Table

Table 4-3112. Instance Table

Instance Name	Physical Address
VIM	50F0 109Ch

Figure 4-1488. VIM_INTPRIORITY_39 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3113. INTPRIORITY_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.118 VIM_INTPRIORITY_40 Register (Offset = 10A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h44

Long Description:

Return to Summary Table

Table 4-3114. Instance Table

Instance Name	Physical Address
VIM	50F0 10A0h

Figure 4-1489. VIM_INTPRIORITY_40 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3115. INTPRIORITY_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.119 VIM_INTPRIORITY_41 Register (Offset = 10A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h45

Long Description:

Return to Summary Table

Table 4-3116. Instance Table

Instance Name	Physical Address
VIM	50F0 10A4h

Figure 4-1490. VIM_INTPRIORITY_41 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3117. INTPRIORITY_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.120 VIM_INTPRIORITY_42 Register (Offset = 10A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h46

Long Description:

Return to Summary Table

Table 4-3118. Instance Table

Instance Name	Physical Address
VIM	50F0 10A8h

Figure 4-1491. VIM_INTPRIORITY_42 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3119. INTPRIORITY_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.121 VIM_INTPRIORITY_43 Register (Offset = 10ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h47

Long Description:

Return to Summary Table

Table 4-3120. Instance Table

Instance Name	Physical Address
VIM	50F0 10ACh

Figure 4-1492. VIM_INTPRIORITY_43 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3121. INTPRIORITY_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.122 VIM_INTPRIORITY_44 Register (Offset = 10B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h48

Long Description:

Return to Summary Table

Table 4-3122. Instance Table

Instance Name	Physical Address
VIM	50F0 10B0h

Figure 4-1493. VIM_INTPRIORITY_44 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3123. INTPRIORITY_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.123 VIM_INTPRIORITY_45 Register (Offset = 10B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h49

Long Description:

Return to Summary Table

Table 4-3124. Instance Table

Instance Name	Physical Address
VIM	50F0 10B4h

Figure 4-1494. VIM_INTPRIORITY_45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3125. INTPRIORITY_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.124 VIM_INTPRIORITY_46 Register (Offset = 10B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h50

Long Description:

Return to Summary Table

Table 4-3126. Instance Table

Instance Name	Physical Address
VIM	50F0 10B8h

Figure 4-1495. VIM_INTPRIORITY_46 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3127. INTPRIORITY_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.125 VIM_INTPRIORITY_47 Register (Offset = 10BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h51

Long Description:

Return to Summary Table

Table 4-3128. Instance Table

Instance Name	Physical Address
VIM	50F0 10BCh

Figure 4-1496. VIM_INTPRIORITY_47 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3129. INTPRIORITY_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.126 VIM_INTPRIORITY_48 Register (Offset = 10C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h52

Long Description:

Return to Summary Table

Table 4-3130. Instance Table

Instance Name	Physical Address
VIM	50F0 10C0h

Figure 4-1497. VIM_INTPRIORITY_48 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3131. INTPRIORITY_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.127 VIM_INTPRIORITY_49 Register (Offset = 10C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h53

Long Description:

Return to Summary Table

Table 4-3132. Instance Table

Instance Name	Physical Address
VIM	50F0 10C4h

Figure 4-1498. VIM_INTPRIORITY_49 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3133. INTPRIORITY_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.128 VIM_INTPRIORITY_50 Register (Offset = 10C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h54

Long Description:

Return to Summary Table

Table 4-3134. Instance Table

Instance Name	Physical Address
VIM	50F0 10C8h

Figure 4-1499. VIM_INTPRIORITY_50 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3135. INTPRIORITY_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.129 VIM_INTPRIORITY_51 Register (Offset = 10CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h55

Long Description:

Return to Summary Table

Table 4-3136. Instance Table

Instance Name	Physical Address
VIM	50F0 10CCh

Figure 4-1500. VIM_INTPRIORITY_51 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3137. INTPRIORITY_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.130 VIM_INTPRIORITY_52 Register (Offset = 10D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h56

Long Description:

Return to Summary Table

Table 4-3138. Instance Table

Instance Name	Physical Address
VIM	50F0 10D0h

Figure 4-1501. VIM_INTPRIORITY_52 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3139. INTPRIORITY_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.131 VIM_INTPRIORITY_53 Register (Offset = 10D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h57

Long Description:

Return to Summary Table

Table 4-3140. Instance Table

Instance Name	Physical Address
VIM	50F0 10D4h

Figure 4-1502. VIM_INTPRIORITY_53 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3141. INTPRIORITY_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.132 VIM_INTPRIORITY_54 Register (Offset = 10D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h58

Long Description:

Return to Summary Table

Table 4-3142. Instance Table

Instance Name	Physical Address
VIM	50F0 10D8h

Figure 4-1503. VIM_INTPRIORITY_54 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3143. INTPRIORITY_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.133 VIM_INTPRIORITY_55 Register (Offset = 10DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h59

Long Description:

Return to Summary Table

Table 4-3144. Instance Table

Instance Name	Physical Address
VIM	50F0 10DCh

Figure 4-1504. VIM_INTPRIORITY_55 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3145. INTPRIORITY_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.134 VIM_INTPRIORITY_56 Register (Offset = 10E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h60

Long Description:

Return to Summary Table

Table 4-3146. Instance Table

Instance Name	Physical Address
VIM	50F0 10E0h

Figure 4-1505. VIM_INTPRIORITY_56 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3147. INTPRIORITY_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.135 VIM_INTPRIORITY_57 Register (Offset = 10E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h61

Long Description:

Return to Summary Table

Table 4-3148. Instance Table

Instance Name	Physical Address
VIM	50F0 10E4h

Figure 4-1506. VIM_INTPRIORITY_57 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3149. INTPRIORITY_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.136 VIM_INTPRIORITY_58 Register (Offset = 10E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h62

Long Description:

Return to Summary Table

Table 4-3150. Instance Table

Instance Name	Physical Address
VIM	50F0 10E8h

Figure 4-1507. VIM_INTPRIORITY_58 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3151. INTPRIORITY_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.137 VIM_INTPRIORITY_59 Register (Offset = 10ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h63

Long Description:

Return to Summary Table

Table 4-3152. Instance Table

Instance Name	Physical Address
VIM	50F0 10ECh

Figure 4-1508. VIM_INTPRIORITY_59 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3153. INTPRIORITY_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.138 VIM_INTPRIORITY_60 Register (Offset = 10F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h64

Long Description:

Return to Summary Table

Table 4-3154. Instance Table

Instance Name	Physical Address
VIM	50F0 10F0h

Figure 4-1509. VIM_INTPRIORITY_60 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3155. INTPRIORITY_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.139 VIM_INTPRIORITY_61 Register (Offset = 10F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h65

Long Description:

Return to Summary Table

Table 4-3156. Instance Table

Instance Name	Physical Address
VIM	50F0 10F4h

Figure 4-1510. VIM_INTPRIORITY_61 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3157. INTPRIORITY_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.140 VIM_INTPRIORITY_62 Register (Offset = 10F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h66

Long Description:

Return to Summary Table

Table 4-3158. Instance Table

Instance Name	Physical Address
VIM	50F0 10F8h

Figure 4-1511. VIM_INTPRIORITY_62 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3159. INTPRIORITY_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.141 VIM_INTPRIORITY_63 Register (Offset = 10FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h67

Long Description:

Return to Summary Table

Table 4-3160. Instance Table

Instance Name	Physical Address
VIM	50F0 10FCh

Figure 4-1512. VIM_INTPRIORITY_63 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3161. INTPRIORITY_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.142 VIM_INTPRIORITY_64 Register (Offset = 1100h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h68

Long Description:

Return to Summary Table

Table 4-3162. Instance Table

Instance Name	Physical Address
VIM	50F0 1100h

Figure 4-1513. VIM_INTPRIORITY_64 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3163. INTPRIORITY_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.143 VIM_INTPRIORITY_65 Register (Offset = 1104h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h69

Long Description:

Return to Summary Table

Table 4-3164. Instance Table

Instance Name	Physical Address
VIM	50F0 1104h

Figure 4-1514. VIM_INTPRIORITY_65 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3165. INTPRIORITY_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.144 VIM_INTPRIORITY_66 Register (Offset = 1108h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h70

Long Description:

Return to Summary Table

Table 4-3166. Instance Table

Instance Name	Physical Address
VIM	50F0 1108h

Figure 4-1515. VIM_INTPRIORITY_66 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3167. INTPRIORITY_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.145 VIM_INTPRIORITY_67 Register (Offset = 110Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h71

Long Description:

Return to Summary Table

Table 4-3168. Instance Table

Instance Name	Physical Address
VIM	50F0 110Ch

Figure 4-1516. VIM_INTPRIORITY_67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3169. INTPRIORITY_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.146 VIM_INTPRIORITY_68 Register (Offset = 1110h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h72

Long Description:

Return to Summary Table

Table 4-3170. Instance Table

Instance Name	Physical Address
VIM	50F0 1110h

Figure 4-1517. VIM_INTPRIORITY_68 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3171. INTPRIORITY_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.147 VIM_INTPRIORITY_69 Register (Offset = 1114h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h73

Long Description:

Return to Summary Table

Table 4-3172. Instance Table

Instance Name	Physical Address
VIM	50F0 1114h

Figure 4-1518. VIM_INTPRIORITY_69 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3173. INTPRIORITY_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.148 VIM_INTPRIORITY_70 Register (Offset = 1118h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h74

Long Description:

Return to Summary Table

Table 4-3174. Instance Table

Instance Name	Physical Address
VIM	50F0 1118h

Figure 4-1519. VIM_INTPRIORITY_70 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3175. INTPRIORITY_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.149 VIM_INTPRIORITY_71 Register (Offset = 111Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h75

Long Description:

Return to Summary Table

Table 4-3176. Instance Table

Instance Name	Physical Address
VIM	50F0 111Ch

Figure 4-1520. VIM_INTPRIORITY_71 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3177. INTPRIORITY_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.150 VIM_INTPRIORITY_72 Register (Offset = 1120h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h76

Long Description:

Return to Summary Table

Table 4-3178. Instance Table

Instance Name	Physical Address
VIM	50F0 1120h

Figure 4-1521. VIM_INTPRIORITY_72 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3179. INTPRIORITY_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.151 VIM_INTPRIORITY_73 Register (Offset = 1124h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h77

Long Description:

Return to Summary Table

Table 4-3180. Instance Table

Instance Name	Physical Address
VIM	50F0 1124h

Figure 4-1522. VIM_INTPRIORITY_73 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3181. INTPRIORITY_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.152 VIM_INTPRIORITY_74 Register (Offset = 1128h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h78

Long Description:

Return to Summary Table

Table 4-3182. Instance Table

Instance Name	Physical Address
VIM	50F0 1128h

Figure 4-1523. VIM_INTPRIORITY_74 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3183. INTPRIORITY_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.153 VIM_INTPRIORITY_75 Register (Offset = 112Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h79

Long Description:

Return to Summary Table

Table 4-3184. Instance Table

Instance Name	Physical Address
VIM	50F0 112Ch

Figure 4-1524. VIM_INTPRIORITY_75 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3185. INTPRIORITY_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.154 VIM_INTPRIORITY_76 Register (Offset = 1130h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h80

Long Description:

Return to Summary Table

Table 4-3186. Instance Table

Instance Name	Physical Address
VIM	50F0 1130h

Figure 4-1525. VIM_INTPRIORITY_76 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3187. INTPRIORITY_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.155 VIM_INTPRIORITY_77 Register (Offset = 1134h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h81

Long Description:

Return to Summary Table

Table 4-3188. Instance Table

Instance Name	Physical Address
VIM	50F0 1134h

Figure 4-1526. VIM_INTPRIORITY_77 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3189. INTPRIORITY_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.156 VIM_INTPRIORITY_78 Register (Offset = 1138h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h82

Long Description:

Return to Summary Table

Table 4-3190. Instance Table

Instance Name	Physical Address
VIM	50F0 1138h

Figure 4-1527. VIM_INTPRIORITY_78 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3191. INTPRIORITY_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.157 VIM_INTPRIORITY_79 Register (Offset = 113Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h83

Long Description:

Return to Summary Table

Table 4-3192. Instance Table

Instance Name	Physical Address
VIM	50F0 113Ch

Figure 4-1528. VIM_INTPRIORITY_79 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3193. INTPRIORITY_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.158 VIM_INTPRIORITY_80 Register (Offset = 1140h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h84

Long Description:

Return to Summary Table

Table 4-3194. Instance Table

Instance Name	Physical Address
VIM	50F0 1140h

Figure 4-1529. VIM_INTPRIORITY_80 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3195. INTPRIORITY_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.159 VIM_INTPRIORITY_81 Register (Offset = 1144h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h85

Long Description:

Return to Summary Table

Table 4-3196. Instance Table

Instance Name	Physical Address
VIM	50F0 1144h

Figure 4-1530. VIM_INTPRIORITY_81 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3197. INTPRIORITY_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.160 VIM_INTPRIORITY_82 Register (Offset = 1148h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h86

Long Description:

Return to Summary Table

Table 4-3198. Instance Table

Instance Name	Physical Address
VIM	50F0 1148h

Figure 4-1531. VIM_INTPRIORITY_82 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3199. INTPRIORITY_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.161 VIM_INTPRIORITY_83 Register (Offset = 114Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h87

Long Description:

Return to Summary Table

Table 4-3200. Instance Table

Instance Name	Physical Address
VIM	50F0 114Ch

Figure 4-1532. VIM_INTPRIORITY_83 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3201. INTPRIORITY_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.162 VIM_INTPRIORITY_84 Register (Offset = 1150h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h88

Long Description:

Return to Summary Table

Table 4-3202. Instance Table

Instance Name	Physical Address
VIM	50F0 1150h

Figure 4-1533. VIM_INTPRIORITY_84 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3203. INTPRIORITY_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.163 VIM_INTPRIORITY_85 Register (Offset = 1154h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h89

Long Description:

Return to Summary Table

Table 4-3204. Instance Table

Instance Name	Physical Address
VIM	50F0 1154h

Figure 4-1534. VIM_INTPRIORITY_85 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3205. INTPRIORITY_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.164 VIM_INTPRIORITY_86 Register (Offset = 1158h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h90

Long Description:

Return to Summary Table

Table 4-3206. Instance Table

Instance Name	Physical Address
VIM	50F0 1158h

Figure 4-1535. VIM_INTPRIORITY_86 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3207. INTPRIORITY_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.165 VIM_INTPRIORITY_87 Register (Offset = 115Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h91

Long Description:

Return to Summary Table

Table 4-3208. Instance Table

Instance Name	Physical Address
VIM	50F0 115Ch

Figure 4-1536. VIM_INTPRIORITY_87 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3209. INTPRIORITY_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.166 VIM_INTPRIORITY_88 Register (Offset = 1160h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h92

Long Description:

Return to Summary Table

Table 4-3210. Instance Table

Instance Name	Physical Address
VIM	50F0 1160h

Figure 4-1537. VIM_INTPRIORITY_88 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3211. INTPRIORITY_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.167 VIM_INTPRIORITY_89 Register (Offset = 1164h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h93

Long Description:

Return to Summary Table

Table 4-3212. Instance Table

Instance Name	Physical Address
VIM	50F0 1164h

Figure 4-1538. VIM_INTPRIORITY_89 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3213. INTPRIORITY_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.168 VIM_INTPRIORITY_90 Register (Offset = 1168h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h94

Long Description:

Return to Summary Table

Table 4-3214. Instance Table

Instance Name	Physical Address
VIM	50F0 1168h

Figure 4-1539. VIM_INTPRIORITY_90 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3215. INTPRIORITY_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.169 VIM_INTPRIORITY_91 Register (Offset = 116Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h95

Long Description:

Return to Summary Table

Table 4-3216. Instance Table

Instance Name	Physical Address
VIM	50F0 116Ch

Figure 4-1540. VIM_INTPRIORITY_91 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3217. INTPRIORITY_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.170 VIM_INTPRIORITY_92 Register (Offset = 1170h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h96

Long Description:

Return to Summary Table

Table 4-3218. Instance Table

Instance Name	Physical Address
VIM	50F0 1170h

Figure 4-1541. VIM_INTPRIORITY_92 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3219. INTPRIORITY_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.171 VIM_INTPRIORITY_93 Register (Offset = 1174h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h97

Long Description:

Return to Summary Table

Table 4-3220. Instance Table

Instance Name	Physical Address
VIM	50F0 1174h

Figure 4-1542. VIM_INTPRIORITY_93 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3221. INTPRIORITY_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.172 VIM_INTPRIORITY_94 Register (Offset = 1178h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h98

Long Description:

Return to Summary Table

Table 4-3222. Instance Table

Instance Name	Physical Address
VIM	50F0 1178h

Figure 4-1543. VIM_INTPRIORITY_94 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3223. INTPRIORITY_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.173 VIM_INTPRIORITY_95 Register (Offset = 117Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h99

Long Description:

Return to Summary Table

Table 4-3224. Instance Table

Instance Name	Physical Address
VIM	50F0 117Ch

Figure 4-1544. VIM_INTPRIORITY_95 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3225. INTPRIORITY_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.174 VIM_INTPRIORITY_96 Register (Offset = 1180h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h100

Long Description:

Return to Summary Table

Table 4-3226. Instance Table

Instance Name	Physical Address
VIM	50F0 1180h

Figure 4-1545. VIM_INTPRIORITY_96 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3227. INTPRIORITY_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.175 VIM_INTPRIORITY_97 Register (Offset = 1184h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h101

Long Description:

Return to Summary Table

Table 4-3228. Instance Table

Instance Name	Physical Address
VIM	50F0 1184h

Figure 4-1546. VIM_INTPRIORITY_97 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3229. INTPRIORITY_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.176 VIM_INTPRIORITY_98 Register (Offset = 1188h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h102

Long Description:

Return to Summary Table

Table 4-3230. Instance Table

Instance Name	Physical Address
VIM	50F0 1188h

Figure 4-1547. VIM_INTPRIORITY_98 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3231. INTPRIORITY_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.177 VIM_INTPRIORITY_99 Register (Offset = 118Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h103

Long Description:

Return to Summary Table

Table 4-3232. Instance Table

Instance Name	Physical Address
VIM	50F0 118Ch

Figure 4-1548. VIM_INTPRIORITY_99 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3233. INTPRIORITY_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.178 VIM_INTPRIORITY_100 Register (Offset = 1190h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h104

Long Description:

Return to Summary Table

Table 4-3234. Instance Table

Instance Name	Physical Address
VIM	50F0 1190h

Figure 4-1549. VIM_INTPRIORITY_100 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3235. INTPRIORITY_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.179 VIM_INTPRIORITY_101 Register (Offset = 1194h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h105

Long Description:

Return to Summary Table

Table 4-3236. Instance Table

Instance Name	Physical Address
VIM	50F0 1194h

Figure 4-1550. VIM_INTPRIORITY_101 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3237. INTPRIORITY_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.180 VIM_INTPRIORITY_102 Register (Offset = 1198h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h106

Long Description:

Return to Summary Table

Table 4-3238. Instance Table

Instance Name	Physical Address
VIM	50F0 1198h

Figure 4-1551. VIM_INTPRIORITY_102 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3239. INTPRIORITY_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.181 VIM_INTPRIORITY_103 Register (Offset = 119Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h107

Long Description:

Return to Summary Table

Table 4-3240. Instance Table

Instance Name	Physical Address
VIM	50F0 119Ch

Figure 4-1552. VIM_INTPRIORITY_103 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3241. INTPRIORITY_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.182 VIM_INTPRIORITY_104 Register (Offset = 11A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h108

Long Description:

Return to Summary Table

Table 4-3242. Instance Table

Instance Name	Physical Address
VIM	50F0 11A0h

Figure 4-1553. VIM_INTPRIORITY_104 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3243. INTPRIORITY_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.183 VIM_INTPRIORITY_105 Register (Offset = 11A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h109

Long Description:

Return to Summary Table

Table 4-3244. Instance Table

Instance Name	Physical Address
VIM	50F0 11A4h

Figure 4-1554. VIM_INTPRIORITY_105 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3245. INTPRIORITY_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.184 VIM_INTPRIORITY_106 Register (Offset = 11A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h110

Long Description:

Return to Summary Table

Table 4-3246. Instance Table

Instance Name	Physical Address
VIM	50F0 11A8h

Figure 4-1555. VIM_INTPRIORITY_106 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3247. INTPRIORITY_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.185 VIM_INTPRIORITY_107 Register (Offset = 11ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h111

Long Description:

Return to Summary Table

Table 4-3248. Instance Table

Instance Name	Physical Address
VIM	50F0 11ACh

Figure 4-1556. VIM_INTPRIORITY_107 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3249. INTPRIORITY_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.186 VIM_INTPRIORITY_108 Register (Offset = 11B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h112

Long Description:

Return to Summary Table

Table 4-3250. Instance Table

Instance Name	Physical Address
VIM	50F0 11B0h

Figure 4-1557. VIM_INTPRIORITY_108 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3251. INTPRIORITY_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.187 VIM_INTPRIORITY_109 Register (Offset = 11B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h113

Long Description:

Return to Summary Table

Table 4-3252. Instance Table

Instance Name	Physical Address
VIM	50F0 11B4h

Figure 4-1558. VIM_INTPRIORITY_109 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3253. INTPRIORITY_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.188 VIM_INTPRIORITY_110 Register (Offset = 11B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h114

Long Description:

Return to Summary Table

Table 4-3254. Instance Table

Instance Name	Physical Address
VIM	50F0 11B8h

Figure 4-1559. VIM_INTPRIORITY_110 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3255. INTPRIORITY_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.189 VIM_INTPRIORITY_111 Register (Offset = 11BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h115

Long Description:

Return to Summary Table

Table 4-3256. Instance Table

Instance Name	Physical Address
VIM	50F0 11BCh

Figure 4-1560. VIM_INTPRIORITY_111 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3257. INTPRIORITY_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.190 VIM_INTPRIORITY_112 Register (Offset = 11C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h116

Long Description:

Return to Summary Table

Table 4-3258. Instance Table

Instance Name	Physical Address
VIM	50F0 11C0h

Figure 4-1561. VIM_INTPRIORITY_112 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3259. INTPRIORITY_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.191 VIM_INTPRIORITY_113 Register (Offset = 11C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h117

Long Description:

Return to Summary Table

Table 4-3260. Instance Table

Instance Name	Physical Address
VIM	50F0 11C4h

Figure 4-1562. VIM_INTPRIORITY_113 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3261. INTPRIORITY_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.192 VIM_INTPRIORITY_114 Register (Offset = 11C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h118

Long Description:

Return to Summary Table

Table 4-3262. Instance Table

Instance Name	Physical Address
VIM	50F0 11C8h

Figure 4-1563. VIM_INTPRIORITY_114 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3263. INTPRIORITY_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.193 VIM_INTPRIORITY_115 Register (Offset = 11CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h119

Long Description:

Return to Summary Table

Table 4-3264. Instance Table

Instance Name	Physical Address
VIM	50F0 11CCh

Figure 4-1564. VIM_INTPRIORITY_115 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3265. INTPRIORITY_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.194 VIM_INTPRIORITY_116 Register (Offset = 11D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h120

Long Description:

Return to Summary Table

Table 4-3266. Instance Table

Instance Name	Physical Address
VIM	50F0 11D0h

Figure 4-1565. VIM_INTPRIORITY_116 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3267. INTPRIORITY_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.195 VIM_INTPRIORITY_117 Register (Offset = 11D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h121

Long Description:

Return to Summary Table

Table 4-3268. Instance Table

Instance Name	Physical Address
VIM	50F0 11D4h

Figure 4-1566. VIM_INTPRIORITY_117 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3269. INTPRIORITY_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.196 VIM_INTPRIORITY_118 Register (Offset = 11D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h122

Long Description:

Return to Summary Table

Table 4-3270. Instance Table

Instance Name	Physical Address
VIM	50F0 11D8h

Figure 4-1567. VIM_INTPRIORITY_118 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3271. INTPRIORITY_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.197 VIM_INTPRIORITY_119 Register (Offset = 11DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h123

Long Description:

Return to Summary Table

Table 4-3272. Instance Table

Instance Name	Physical Address
VIM	50F0 11DCh

Figure 4-1568. VIM_INTPRIORITY_119 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3273. INTPRIORITY_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.198 VIM_INTPRIORITY_120 Register (Offset = 11E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h124

Long Description:

Return to Summary Table

Table 4-3274. Instance Table

Instance Name	Physical Address
VIM	50F0 11E0h

Figure 4-1569. VIM_INTPRIORITY_120 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3275. INTPRIORITY_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.199 VIM_INTPRIORITY_121 Register (Offset = 11E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h125

Long Description:

Return to Summary Table

Table 4-3276. Instance Table

Instance Name	Physical Address
VIM	50F0 11E4h

Figure 4-1570. VIM_INTPRIORITY_121 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3277. INTPRIORITY_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.200 VIM_INTPRIORITY_122 Register (Offset = 11E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h126

Long Description:

Return to Summary Table

Table 4-3278. Instance Table

Instance Name	Physical Address
VIM	50F0 11E8h

Figure 4-1571. VIM_INTPRIORITY_122 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3279. INTPRIORITY_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.201 VIM_INTPRIORITY_123 Register (Offset = 11ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h127

Long Description:

Return to Summary Table

Table 4-3280. Instance Table

Instance Name	Physical Address
VIM	50F0 11ECh

Figure 4-1572. VIM_INTPRIORITY_123 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3281. INTPRIORITY_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.202 VIM_INTPRIORITY_124 Register (Offset = 11F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h128

Long Description:

Return to Summary Table

Table 4-3282. Instance Table

Instance Name	Physical Address
VIM	50F0 11F0h

Figure 4-1573. VIM_INTPRIORITY_124 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3283. INTPRIORITY_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.203 VIM_INTPRIORITY_125 Register (Offset = 11F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h129

Long Description:

Return to Summary Table

Table 4-3284. Instance Table

Instance Name	Physical Address
VIM	50F0 11F4h

Figure 4-1574. VIM_INTPRIORITY_125 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3285. INTPRIORITY_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.204 VIM_INTPRIORITY_126 Register (Offset = 11F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h130

Long Description:

Return to Summary Table

Table 4-3286. Instance Table

Instance Name	Physical Address
VIM	50F0 11F8h

Figure 4-1575. VIM_INTPRIORITY_126 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3287. INTPRIORITY_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.205 VIM_INTPRIORITY_127 Register (Offset = 11FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h131

Long Description:

Return to Summary Table

Table 4-3288. Instance Table

Instance Name	Physical Address
VIM	50F0 11FCh

Figure 4-1576. VIM_INTPRIORITY_127 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3289. INTPRIORITY_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.206 VIM_INTPRIORITY_128 Register (Offset = 1200h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h132

Long Description:

Return to Summary Table

Table 4-3290. Instance Table

Instance Name	Physical Address
VIM	50F0 1200h

Figure 4-1577. VIM_INTPRIORITY_128 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3291. INTPRIORITY_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.207 VIM_INTPRIORITY_129 Register (Offset = 1204h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h133

Long Description:

Return to Summary Table

Table 4-3292. Instance Table

Instance Name	Physical Address
VIM	50F0 1204h

Figure 4-1578. VIM_INTPRIORITY_129 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3293. INTPRIORITY_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.208 VIM_INTPRIORITY_130 Register (Offset = 1208h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h134

Long Description:

Return to Summary Table

Table 4-3294. Instance Table

Instance Name	Physical Address
VIM	50F0 1208h

Figure 4-1579. VIM_INTPRIORITY_130 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3295. INTPRIORITY_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.209 VIM_INTPRIORITY_131 Register (Offset = 120Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h135

Long Description:

Return to Summary Table

Table 4-3296. Instance Table

Instance Name	Physical Address
VIM	50F0 120Ch

Figure 4-1580. VIM_INTPRIORITY_131 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3297. INTPRIORITY_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.210 VIM_INTPRIORITY_132 Register (Offset = 1210h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h136

Long Description:

Return to Summary Table

Table 4-3298. Instance Table

Instance Name	Physical Address
VIM	50F0 1210h

Figure 4-1581. VIM_INTPRIORITY_132 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3299. INTPRIORITY_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.211 VIM_INTPRIORITY_133 Register (Offset = 1214h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h137

Long Description:

Return to Summary Table

Table 4-3300. Instance Table

Instance Name	Physical Address
VIM	50F0 1214h

Figure 4-1582. VIM_INTPRIORITY_133 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3301. INTPRIORITY_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.212 VIM_INTPRIORITY_134 Register (Offset = 1218h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h138

Long Description:

Return to Summary Table

Table 4-3302. Instance Table

Instance Name	Physical Address
VIM	50F0 1218h

Figure 4-1583. VIM_INTPRIORITY_134 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3303. INTPRIORITY_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.213 VIM_INTPRIORITY_135 Register (Offset = 121Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h139

Long Description:

Return to Summary Table

Table 4-3304. Instance Table

Instance Name	Physical Address
VIM	50F0 121Ch

Figure 4-1584. VIM_INTPRIORITY_135 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3305. INTPRIORITY_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.214 VIM_INTPRIORITY_136 Register (Offset = 1220h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h140

Long Description:

Return to Summary Table

Table 4-3306. Instance Table

Instance Name	Physical Address
VIM	50F0 1220h

Figure 4-1585. VIM_INTPRIORITY_136 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3307. INTPRIORITY_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.215 VIM_INTPRIORITY_137 Register (Offset = 1224h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h141

Long Description:

Return to Summary Table

Table 4-3308. Instance Table

Instance Name	Physical Address
VIM	50F0 1224h

Figure 4-1586. VIM_INTPRIORITY_137 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3309. INTPRIORITY_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.216 VIM_INTPRIORITY_138 Register (Offset = 1228h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h142

Long Description:

Return to Summary Table

Table 4-3310. Instance Table

Instance Name	Physical Address
VIM	50F0 1228h

Figure 4-1587. VIM_INTPRIORITY_138 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3311. INTPRIORITY_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.217 VIM_INTPRIORITY_139 Register (Offset = 122Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h143

Long Description:

Return to Summary Table

Table 4-3312. Instance Table

Instance Name	Physical Address
VIM	50F0 122Ch

Figure 4-1588. VIM_INTPRIORITY_139 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3313. INTPRIORITY_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.218 VIM_INTPRIORITY_140 Register (Offset = 1230h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h144

Long Description:

Return to Summary Table

Table 4-3314. Instance Table

Instance Name	Physical Address
VIM	50F0 1230h

Figure 4-1589. VIM_INTPRIORITY_140 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3315. INTPRIORITY_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.219 VIM_INTPRIORITY_141 Register (Offset = 1234h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h145

Long Description:

Return to Summary Table

Table 4-3316. Instance Table

Instance Name	Physical Address
VIM	50F0 1234h

Figure 4-1590. VIM_INTPRIORITY_141 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3317. INTPRIORITY_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.220 VIM_INTPRIORITY_142 Register (Offset = 1238h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h146

Long Description:

Return to Summary Table

Table 4-3318. Instance Table

Instance Name	Physical Address
VIM	50F0 1238h

Figure 4-1591. VIM_INTPRIORITY_142 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3319. INTPRIORITY_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.221 VIM_INTPRIORITY_143 Register (Offset = 123Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h147

Long Description:

Return to Summary Table

Table 4-3320. Instance Table

Instance Name	Physical Address
VIM	50F0 123Ch

Figure 4-1592. VIM_INTPRIORITY_143 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3321. INTPRIORITY_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.222 VIM_INTPRIORITY_144 Register (Offset = 1240h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h148

Long Description:

Return to Summary Table

Table 4-3322. Instance Table

Instance Name	Physical Address
VIM	50F0 1240h

Figure 4-1593. VIM_INTPRIORITY_144 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3323. INTPRIORITY_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.223 VIM_INTPRIORITY_145 Register (Offset = 1244h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h149

Long Description:

Return to Summary Table

Table 4-3324. Instance Table

Instance Name	Physical Address
VIM	50F0 1244h

Figure 4-1594. VIM_INTPRIORITY_145 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3325. INTPRIORITY_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.224 VIM_INTPRIORITY_146 Register (Offset = 1248h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h150

Long Description:

Return to Summary Table

Table 4-3326. Instance Table

Instance Name	Physical Address
VIM	50F0 1248h

Figure 4-1595. VIM_INTPRIORITY_146 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3327. INTPRIORITY_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.225 VIM_INTPRIORITY_147 Register (Offset = 124Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h151

Long Description:

Return to Summary Table

Table 4-3328. Instance Table

Instance Name	Physical Address
VIM	50F0 124Ch

Figure 4-1596. VIM_INTPRIORITY_147 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3329. INTPRIORITY_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.226 VIM_INTPRIORITY_148 Register (Offset = 1250h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h152

Long Description:

Return to Summary Table

Table 4-3330. Instance Table

Instance Name	Physical Address
VIM	50F0 1250h

Figure 4-1597. VIM_INTPRIORITY_148 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3331. INTPRIORITY_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.227 VIM_INTPRIORITY_149 Register (Offset = 1254h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h153

Long Description:

Return to Summary Table

Table 4-3332. Instance Table

Instance Name	Physical Address
VIM	50F0 1254h

Figure 4-1598. VIM_INTPRIORITY_149 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3333. INTPRIORITY_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.228 VIM_INTPRIORITY_150 Register (Offset = 1258h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h154

Long Description:

Return to Summary Table

Table 4-3334. Instance Table

Instance Name	Physical Address
VIM	50F0 1258h

Figure 4-1599. VIM_INTPRIORITY_150 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3335. INTPRIORITY_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.229 VIM_INTPRIORITY_151 Register (Offset = 125Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h155

Long Description:

Return to Summary Table

Table 4-3336. Instance Table

Instance Name	Physical Address
VIM	50F0 125Ch

Figure 4-1600. VIM_INTPRIORITY_151 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3337. INTPRIORITY_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.230 VIM_INTPRIORITY_152 Register (Offset = 1260h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h156

Long Description:

Return to Summary Table

Table 4-3338. Instance Table

Instance Name	Physical Address
VIM	50F0 1260h

Figure 4-1601. VIM_INTPRIORITY_152 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3339. INTPRIORITY_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.231 VIM_INTPRIORITY_153 Register (Offset = 1264h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h157

Long Description:

Return to Summary Table

Table 4-3340. Instance Table

Instance Name	Physical Address
VIM	50F0 1264h

Figure 4-1602. VIM_INTPRIORITY_153 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3341. INTPRIORITY_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.232 VIM_INTPRIORITY_154 Register (Offset = 1268h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h158

Long Description:

Return to Summary Table

Table 4-3342. Instance Table

Instance Name	Physical Address
VIM	50F0 1268h

Figure 4-1603. VIM_INTPRIORITY_154 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3343. INTPRIORITY_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.233 VIM_INTPRIORITY_155 Register (Offset = 126Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h159

Long Description:

Return to Summary Table

Table 4-3344. Instance Table

Instance Name	Physical Address
VIM	50F0 126Ch

Figure 4-1604. VIM_INTPRIORITY_155 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3345. INTPRIORITY_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.234 VIM_INTPRIORITY_156 Register (Offset = 1270h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h160

Long Description:

Return to Summary Table

Table 4-3346. Instance Table

Instance Name	Physical Address
VIM	50F0 1270h

Figure 4-1605. VIM_INTPRIORITY_156 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3347. INTPRIORITY_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.235 VIM_INTPRIORITY_157 Register (Offset = 1274h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h161

Long Description:

Return to Summary Table

Table 4-3348. Instance Table

Instance Name	Physical Address
VIM	50F0 1274h

Figure 4-1606. VIM_INTPRIORITY_157 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3349. INTPRIORITY_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.236 VIM_INTPRIORITY_158 Register (Offset = 1278h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h162

Long Description:

Return to Summary Table

Table 4-3350. Instance Table

Instance Name	Physical Address
VIM	50F0 1278h

Figure 4-1607. VIM_INTPRIORITY_158 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3351. INTPRIORITY_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.237 VIM_INTPRIORITY_159 Register (Offset = 127Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h163

Long Description:

Return to Summary Table

Table 4-3352. Instance Table

Instance Name	Physical Address
VIM	50F0 127Ch

Figure 4-1608. VIM_INTPRIORITY_159 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3353. INTPRIORITY_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.238 VIM_INTPRIORITY_160 Register (Offset = 1280h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h164

Long Description:

Return to Summary Table

Table 4-3354. Instance Table

Instance Name	Physical Address
VIM	50F0 1280h

Figure 4-1609. VIM_INTPRIORITY_160 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3355. INTPRIORITY_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.239 VIM_INTPRIORITY_161 Register (Offset = 1284h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h165

Long Description:

Return to Summary Table

Table 4-3356. Instance Table

Instance Name	Physical Address
VIM	50F0 1284h

Figure 4-1610. VIM_INTPRIORITY_161 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3357. INTPRIORITY_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.240 VIM_INTPRIORITY_162 Register (Offset = 1288h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h166

Long Description:

Return to Summary Table

Table 4-3358. Instance Table

Instance Name	Physical Address
VIM	50F0 1288h

Figure 4-1611. VIM_INTPRIORITY_162 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3359. INTPRIORITY_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.241 VIM_INTPRIORITY_163 Register (Offset = 128Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h167

Long Description:

Return to Summary Table

Table 4-3360. Instance Table

Instance Name	Physical Address
VIM	50F0 128Ch

Figure 4-1612. VIM_INTPRIORITY_163 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3361. INTPRIORITY_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.242 VIM_INTPRIORITY_164 Register (Offset = 1290h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h168

Long Description:

Return to Summary Table

Table 4-3362. Instance Table

Instance Name	Physical Address
VIM	50F0 1290h

Figure 4-1613. VIM_INTPRIORITY_164 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3363. INTPRIORITY_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.243 VIM_INTPRIORITY_165 Register (Offset = 1294h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h169

Long Description:

Return to Summary Table

Table 4-3364. Instance Table

Instance Name	Physical Address
VIM	50F0 1294h

Figure 4-1614. VIM_INTPRIORITY_165 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3365. INTPRIORITY_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.244 VIM_INTPRIORITY_166 Register (Offset = 1298h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h170

Long Description:

Return to Summary Table

Table 4-3366. Instance Table

Instance Name	Physical Address
VIM	50F0 1298h

Figure 4-1615. VIM_INTPRIORITY_166 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3367. INTPRIORITY_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.245 VIM_INTPRIORITY_167 Register (Offset = 129Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h171

Long Description:

Return to Summary Table

Table 4-3368. Instance Table

Instance Name	Physical Address
VIM	50F0 129Ch

Figure 4-1616. VIM_INTPRIORITY_167 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3369. INTPRIORITY_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.246 VIM_INTPRIORITY_168 Register (Offset = 12A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h172

Long Description:

Return to Summary Table

Table 4-3370. Instance Table

Instance Name	Physical Address
VIM	50F0 12A0h

Figure 4-1617. VIM_INTPRIORITY_168 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3371. INTPRIORITY_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.247 VIM_INTPRIORITY_169 Register (Offset = 12A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h173

Long Description:

Return to Summary Table

Table 4-3372. Instance Table

Instance Name	Physical Address
VIM	50F0 12A4h

Figure 4-1618. VIM_INTPRIORITY_169 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3373. INTPRIORITY_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.248 VIM_INTPRIORITY_170 Register (Offset = 12A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h174

Long Description:

Return to Summary Table

Table 4-3374. Instance Table

Instance Name	Physical Address
VIM	50F0 12A8h

Figure 4-1619. VIM_INTPRIORITY_170 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3375. INTPRIORITY_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.249 VIM_INTPRIORITY_171 Register (Offset = 12ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h175

Long Description:

Return to Summary Table

Table 4-3376. Instance Table

Instance Name	Physical Address
VIM	50F0 12ACh

Figure 4-1620. VIM_INTPRIORITY_171 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3377. INTPRIORITY_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.250 VIM_INTPRIORITY_172 Register (Offset = 12B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h176

Long Description:

Return to Summary Table

Table 4-3378. Instance Table

Instance Name	Physical Address
VIM	50F0 12B0h

Figure 4-1621. VIM_INTPRIORITY_172 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3379. INTPRIORITY_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.251 VIM_INTPRIORITY_173 Register (Offset = 12B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h177

Long Description:

Return to Summary Table

Table 4-3380. Instance Table

Instance Name	Physical Address
VIM	50F0 12B4h

Figure 4-1622. VIM_INTPRIORITY_173 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3381. INTPRIORITY_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.252 VIM_INTPRIORITY_174 Register (Offset = 12B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h178

Long Description:

Return to Summary Table

Table 4-3382. Instance Table

Instance Name	Physical Address
VIM	50F0 12B8h

Figure 4-1623. VIM_INTPRIORITY_174 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3383. INTPRIORITY_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.253 VIM_INTPRIORITY_175 Register (Offset = 12BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h179

Long Description:

Return to Summary Table

Table 4-3384. Instance Table

Instance Name	Physical Address
VIM	50F0 12BCh

Figure 4-1624. VIM_INTPRIORITY_175 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3385. INTPRIORITY_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.254 VIM_INTPRIORITY_176 Register (Offset = 12C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h180

Long Description:

Return to Summary Table

Table 4-3386. Instance Table

Instance Name	Physical Address
VIM	50F0 12C0h

Figure 4-1625. VIM_INTPRIORITY_176 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3387. INTPRIORITY_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.255 VIM_INTPRIORITY_177 Register (Offset = 12C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h181

Long Description:

Return to Summary Table

Table 4-3388. Instance Table

Instance Name	Physical Address
VIM	50F0 12C4h

Figure 4-1626. VIM_INTPRIORITY_177 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3389. INTPRIORITY_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.256 VIM_INTPRIORITY_178 Register (Offset = 12C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h182

Long Description:

Return to Summary Table

Table 4-3390. Instance Table

Instance Name	Physical Address
VIM	50F0 12C8h

Figure 4-1627. VIM_INTPRIORITY_178 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3391. INTPRIORITY_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.257 VIM_INTPRIORITY_179 Register (Offset = 12CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h183

Long Description:

Return to Summary Table

Table 4-3392. Instance Table

Instance Name	Physical Address
VIM	50F0 12CCh

Figure 4-1628. VIM_INTPRIORITY_179 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3393. INTPRIORITY_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.258 VIM_INTPRIORITY_180 Register (Offset = 12D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h184

Long Description:

Return to Summary Table

Table 4-3394. Instance Table

Instance Name	Physical Address
VIM	50F0 12D0h

Figure 4-1629. VIM_INTPRIORITY_180 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3395. INTPRIORITY_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.259 VIM_INTPRIORITY_181 Register (Offset = 12D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h185

Long Description:

Return to Summary Table

Table 4-3396. Instance Table

Instance Name	Physical Address
VIM	50F0 12D4h

Figure 4-1630. VIM_INTPRIORITY_181 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3397. INTPRIORITY_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.260 VIM_INTPRIORITY_182 Register (Offset = 12D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h186

Long Description:

Return to Summary Table

Table 4-3398. Instance Table

Instance Name	Physical Address
VIM	50F0 12D8h

Figure 4-1631. VIM_INTPRIORITY_182 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3399. INTPRIORITY_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.261 VIM_INTPRIORITY_183 Register (Offset = 12DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h187

Long Description:

Return to Summary Table

Table 4-3400. Instance Table

Instance Name	Physical Address
VIM	50F0 12DCh

Figure 4-1632. VIM_INTPRIORITY_183 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3401. INTPRIORITY_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.262 VIM_INTPRIORITY_184 Register (Offset = 12E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h188

Long Description:

Return to Summary Table

Table 4-3402. Instance Table

Instance Name	Physical Address
VIM	50F0 12E0h

Figure 4-1633. VIM_INTPRIORITY_184 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3403. INTPRIORITY_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.263 VIM_INTPRIORITY_185 Register (Offset = 12E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h189

Long Description:

Return to Summary Table

Table 4-3404. Instance Table

Instance Name	Physical Address
VIM	50F0 12E4h

Figure 4-1634. VIM_INTPRIORITY_185 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3405. INTPRIORITY_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.264 VIM_INTPRIORITY_186 Register (Offset = 12E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h190

Long Description:

Return to Summary Table

Table 4-3406. Instance Table

Instance Name	Physical Address
VIM	50F0 12E8h

Figure 4-1635. VIM_INTPRIORITY_186 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3407. INTPRIORITY_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.265 VIM_INTPRIORITY_187 Register (Offset = 12ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h191

Long Description:

Return to Summary Table

Table 4-3408. Instance Table

Instance Name	Physical Address
VIM	50F0 12ECh

Figure 4-1636. VIM_INTPRIORITY_187 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3409. INTPRIORITY_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.266 VIM_INTPRIORITY_188 Register (Offset = 12F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h192

Long Description:

Return to Summary Table

Table 4-3410. Instance Table

Instance Name	Physical Address
VIM	50F0 12F0h

Figure 4-1637. VIM_INTPRIORITY_188 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3411. INTPRIORITY_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.267 VIM_INTPRIORITY_189 Register (Offset = 12F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h193

Long Description:

Return to Summary Table

Table 4-3412. Instance Table

Instance Name	Physical Address
VIM	50F0 12F4h

Figure 4-1638. VIM_INTPRIORITY_189 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3413. INTPRIORITY_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.268 VIM_INTPRIORITY_190 Register (Offset = 12F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h194

Long Description:

Return to Summary Table

Table 4-3414. Instance Table

Instance Name	Physical Address
VIM	50F0 12F8h

Figure 4-1639. VIM_INTPRIORITY_190 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3415. INTPRIORITY_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.269 VIM_INTPRIORITY_191 Register (Offset = 12FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h195

Long Description:

Return to Summary Table

Table 4-3416. Instance Table

Instance Name	Physical Address
VIM	50F0 12FCh

Figure 4-1640. VIM_INTPRIORITY_191 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3417. INTPRIORITY_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.270 VIM_INTPRIORITY_192 Register (Offset = 1300h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h196

Long Description:

Return to Summary Table

Table 4-3418. Instance Table

Instance Name	Physical Address
VIM	50F0 1300h

Figure 4-1641. VIM_INTPRIORITY_192 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3419. INTPRIORITY_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.271 VIM_INTPRIORITY_193 Register (Offset = 1304h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h197

Long Description:

Return to Summary Table

Table 4-3420. Instance Table

Instance Name	Physical Address
VIM	50F0 1304h

Figure 4-1642. VIM_INTPRIORITY_193 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3421. INTPRIORITY_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.272 VIM_INTPRIORITY_194 Register (Offset = 1308h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h198

Long Description:

Return to Summary Table

Table 4-3422. Instance Table

Instance Name	Physical Address
VIM	50F0 1308h

Figure 4-1643. VIM_INTPRIORITY_194 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3423. INTPRIORITY_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.273 VIM_INTPRIORITY_195 Register (Offset = 130Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h199

Long Description:

Return to Summary Table

Table 4-3424. Instance Table

Instance Name	Physical Address
VIM	50F0 130Ch

Figure 4-1644. VIM_INTPRIORITY_195 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3425. INTPRIORITY_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.274 VIM_INTPRIORITY_196 Register (Offset = 1310h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h200

Long Description:

Return to Summary Table

Table 4-3426. Instance Table

Instance Name	Physical Address
VIM	50F0 1310h

Figure 4-1645. VIM_INTPRIORITY_196 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3427. INTPRIORITY_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.275 VIM_INTPRIORITY_197 Register (Offset = 1314h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h201

Long Description:

Return to Summary Table

Table 4-3428. Instance Table

Instance Name	Physical Address
VIM	50F0 1314h

Figure 4-1646. VIM_INTPRIORITY_197 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3429. INTPRIORITY_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.276 VIM_INTPRIORITY_198 Register (Offset = 1318h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h202

Long Description:

Return to Summary Table

Table 4-3430. Instance Table

Instance Name	Physical Address
VIM	50F0 1318h

Figure 4-1647. VIM_INTPRIORITY_198 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3431. INTPRIORITY_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.277 VIM_INTPRIORITY_199 Register (Offset = 131Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h203

Long Description:

Return to Summary Table

Table 4-3432. Instance Table

Instance Name	Physical Address
VIM	50F0 131Ch

Figure 4-1648. VIM_INTPRIORITY_199 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3433. INTPRIORITY_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.278 VIM_INTPRIORITY_200 Register (Offset = 1320h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h204

Long Description:

Return to Summary Table

Table 4-3434. Instance Table

Instance Name	Physical Address
VIM	50F0 1320h

Figure 4-1649. VIM_INTPRIORITY_200 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3435. INTPRIORITY_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.279 VIM_INTPRIORITY_201 Register (Offset = 1324h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h205

Long Description:

Return to Summary Table

Table 4-3436. Instance Table

Instance Name	Physical Address
VIM	50F0 1324h

Figure 4-1650. VIM_INTPRIORITY_201 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3437. INTPRIORITY_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.280 VIM_INTPRIORITY_202 Register (Offset = 1328h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h206

Long Description:

Return to Summary Table

Table 4-3438. Instance Table

Instance Name	Physical Address
VIM	50F0 1328h

Figure 4-1651. VIM_INTPRIORITY_202 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3439. INTPRIORITY_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.281 VIM_INTPRIORITY_203 Register (Offset = 132Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h207

Long Description:

Return to Summary Table

Table 4-3440. Instance Table

Instance Name	Physical Address
VIM	50F0 132Ch

Figure 4-1652. VIM_INTPRIORITY_203 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3441. INTPRIORITY_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.282 VIM_INTPRIORITY_204 Register (Offset = 1330h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h208

Long Description:

Return to Summary Table

Table 4-3442. Instance Table

Instance Name	Physical Address
VIM	50F0 1330h

Figure 4-1653. VIM_INTPRIORITY_204 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3443. INTPRIORITY_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.283 VIM_INTPRIORITY_205 Register (Offset = 1334h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h209

Long Description:

Return to Summary Table

Table 4-3444. Instance Table

Instance Name	Physical Address
VIM	50F0 1334h

Figure 4-1654. VIM_INTPRIORITY_205 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3445. INTPRIORITY_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.284 VIM_INTPRIORITY_206 Register (Offset = 1338h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h210

Long Description:

Return to Summary Table

Table 4-3446. Instance Table

Instance Name	Physical Address
VIM	50F0 1338h

Figure 4-1655. VIM_INTPRIORITY_206 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3447. INTPRIORITY_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.285 VIM_INTPRIORITY_207 Register (Offset = 133Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h211

Long Description:

Return to Summary Table

Table 4-3448. Instance Table

Instance Name	Physical Address
VIM	50F0 133Ch

Figure 4-1656. VIM_INTPRIORITY_207 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3449. INTPRIORITY_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.286 VIM_INTPRIORITY_208 Register (Offset = 1340h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h212

Long Description:

Return to Summary Table

Table 4-3450. Instance Table

Instance Name	Physical Address
VIM	50F0 1340h

Figure 4-1657. VIM_INTPRIORITY_208 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3451. INTPRIORITY_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.287 VIM_INTPRIORITY_209 Register (Offset = 1344h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h213

Long Description:

Return to Summary Table

Table 4-3452. Instance Table

Instance Name	Physical Address
VIM	50F0 1344h

Figure 4-1658. VIM_INTPRIORITY_209 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3453. INTPRIORITY_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.288 VIM_INTPRIORITY_210 Register (Offset = 1348h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h214

Long Description:

Return to Summary Table

Table 4-3454. Instance Table

Instance Name	Physical Address
VIM	50F0 1348h

Figure 4-1659. VIM_INTPRIORITY_210 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3455. INTPRIORITY_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.289 VIM_INTPRIORITY_211 Register (Offset = 134Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h215

Long Description:

Return to Summary Table

Table 4-3456. Instance Table

Instance Name	Physical Address
VIM	50F0 134Ch

Figure 4-1660. VIM_INTPRIORITY_211 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3457. INTPRIORITY_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.290 VIM_INTPRIORITY_212 Register (Offset = 1350h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h216

Long Description:

Return to Summary Table

Table 4-3458. Instance Table

Instance Name	Physical Address
VIM	50F0 1350h

Figure 4-1661. VIM_INTPRIORITY_212 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3459. INTPRIORITY_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.291 VIM_INTPRIORITY_213 Register (Offset = 1354h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h217

Long Description:

Return to Summary Table

Table 4-3460. Instance Table

Instance Name	Physical Address
VIM	50F0 1354h

Figure 4-1662. VIM_INTPRIORITY_213 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3461. INTPRIORITY_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.292 VIM_INTPRIORITY_214 Register (Offset = 1358h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h218

Long Description:

Return to Summary Table

Table 4-3462. Instance Table

Instance Name	Physical Address
VIM	50F0 1358h

Figure 4-1663. VIM_INTPRIORITY_214 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3463. INTPRIORITY_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.293 VIM_INTPRIORITY_215 Register (Offset = 135Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h219

Long Description:

Return to Summary Table

Table 4-3464. Instance Table

Instance Name	Physical Address
VIM	50F0 135Ch

Figure 4-1664. VIM_INTPRIORITY_215 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3465. INTPRIORITY_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.294 VIM_INTPRIORITY_216 Register (Offset = 1360h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h220

Long Description:

Return to Summary Table

Table 4-3466. Instance Table

Instance Name	Physical Address
VIM	50F0 1360h

Figure 4-1665. VIM_INTPRIORITY_216 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3467. INTPRIORITY_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.295 VIM_INTPRIORITY_217 Register (Offset = 1364h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h221

Long Description:

Return to Summary Table

Table 4-3468. Instance Table

Instance Name	Physical Address
VIM	50F0 1364h

Figure 4-1666. VIM_INTPRIORITY_217 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3469. INTPRIORITY_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.296 VIM_INTPRIORITY_218 Register (Offset = 1368h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h222

Long Description:

Return to Summary Table

Table 4-3470. Instance Table

Instance Name	Physical Address
VIM	50F0 1368h

Figure 4-1667. VIM_INTPRIORITY_218 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3471. INTPRIORITY_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.297 VIM_INTPRIORITY_219 Register (Offset = 136Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h223

Long Description:

Return to Summary Table

Table 4-3472. Instance Table

Instance Name	Physical Address
VIM	50F0 136Ch

Figure 4-1668. VIM_INTPRIORITY_219 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3473. INTPRIORITY_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.298 VIM_INTPRIORITY_220 Register (Offset = 1370h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h224

Long Description:

Return to Summary Table

Table 4-3474. Instance Table

Instance Name	Physical Address
VIM	50F0 1370h

Figure 4-1669. VIM_INTPRIORITY_220 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3475. INTPRIORITY_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.299 VIM_INTPRIORITY_221 Register (Offset = 1374h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h225

Long Description:

Return to Summary Table

Table 4-3476. Instance Table

Instance Name	Physical Address
VIM	50F0 1374h

Figure 4-1670. VIM_INTPRIORITY_221 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3477. INTPRIORITY_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.300 VIM_INTPRIORITY_222 Register (Offset = 1378h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h226

Long Description:

Return to Summary Table

Table 4-3478. Instance Table

Instance Name	Physical Address
VIM	50F0 1378h

Figure 4-1671. VIM_INTPRIORITY_222 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3479. INTPRIORITY_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.301 VIM_INTPRIORITY_223 Register (Offset = 137Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h227

Long Description:

Return to Summary Table

Table 4-3480. Instance Table

Instance Name	Physical Address
VIM	50F0 137Ch

Figure 4-1672. VIM_INTPRIORITY_223 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3481. INTPRIORITY_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.302 VIM_INTPRIORITY_224 Register (Offset = 1380h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h228

Long Description:

Return to Summary Table

Table 4-3482. Instance Table

Instance Name	Physical Address
VIM	50F0 1380h

Figure 4-1673. VIM_INTPRIORITY_224 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3483. INTPRIORITY_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.303 VIM_INTPRIORITY_225 Register (Offset = 1384h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h229

Long Description:

Return to Summary Table

Table 4-3484. Instance Table

Instance Name	Physical Address
VIM	50F0 1384h

Figure 4-1674. VIM_INTPRIORITY_225 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3485. INTPRIORITY_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.304 VIM_INTPRIORITY_226 Register (Offset = 1388h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h230

Long Description:

Return to Summary Table

Table 4-3486. Instance Table

Instance Name	Physical Address
VIM	50F0 1388h

Figure 4-1675. VIM_INTPRIORITY_226 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3487. INTPRIORITY_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.305 VIM_INTPRIORITY_227 Register (Offset = 138Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h231

Long Description:

Return to Summary Table

Table 4-3488. Instance Table

Instance Name	Physical Address
VIM	50F0 138Ch

Figure 4-1676. VIM_INTPRIORITY_227 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3489. INTPRIORITY_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.306 VIM_INTPRIORITY_228 Register (Offset = 1390h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h232

Long Description:

Return to Summary Table

Table 4-3490. Instance Table

Instance Name	Physical Address
VIM	50F0 1390h

Figure 4-1677. VIM_INTPRIORITY_228 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3491. INTPRIORITY_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.307 VIM_INTPRIORITY_229 Register (Offset = 1394h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h233

Long Description:

Return to Summary Table

Table 4-3492. Instance Table

Instance Name	Physical Address
VIM	50F0 1394h

Figure 4-1678. VIM_INTPRIORITY_229 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3493. INTPRIORITY_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.308 VIM_INTPRIORITY_230 Register (Offset = 1398h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h234

Long Description:

Return to Summary Table

Table 4-3494. Instance Table

Instance Name	Physical Address
VIM	50F0 1398h

Figure 4-1679. VIM_INTPRIORITY_230 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3495. INTPRIORITY_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.309 VIM_INTPRIORITY_231 Register (Offset = 139Ch) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h235

Long Description:

Return to Summary Table

Table 4-3496. Instance Table

Instance Name	Physical Address
VIM	50F0 139Ch

Figure 4-1680. VIM_INTPRIORITY_231 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3497. INTPRIORITY_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.310 VIM_INTPRIORITY_232 Register (Offset = 13A0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h236

Long Description:

Return to Summary Table

Table 4-3498. Instance Table

Instance Name	Physical Address
VIM	50F0 13A0h

Figure 4-1681. VIM_INTPRIORITY_232 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3499. INTPRIORITY_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.311 VIM_INTPRIORITY_233 Register (Offset = 13A4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h237

Long Description:

Return to Summary Table

Table 4-3500. Instance Table

Instance Name	Physical Address
VIM	50F0 13A4h

Figure 4-1682. VIM_INTPRIORITY_233 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3501. INTPRIORITY_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.312 VIM_INTPRIORITY_234 Register (Offset = 13A8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h238

Long Description:

Return to Summary Table

Table 4-3502. Instance Table

Instance Name	Physical Address
VIM	50F0 13A8h

Figure 4-1683. VIM_INTPRIORITY_234 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3503. INTPRIORITY_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.313 VIM_INTPRIORITY_235 Register (Offset = 13ACh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h239

Long Description:

Return to Summary Table

Table 4-3504. Instance Table

Instance Name	Physical Address
VIM	50F0 13ACh

Figure 4-1684. VIM_INTPRIORITY_235 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3505. INTPRIORITY_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.314 VIM_INTPRIORITY_236 Register (Offset = 13B0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h240

Long Description:

Return to Summary Table

Table 4-3506. Instance Table

Instance Name	Physical Address
VIM	50F0 13B0h

Figure 4-1685. VIM_INTPRIORITY_236 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3507. INTPRIORITY_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.315 VIM_INTPRIORITY_237 Register (Offset = 13B4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h241

Long Description:

Return to Summary Table

Table 4-3508. Instance Table

Instance Name	Physical Address
VIM	50F0 13B4h

Figure 4-1686. VIM_INTPRIORITY_237 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3509. INTPRIORITY_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.316 VIM_INTPRIORITY_238 Register (Offset = 13B8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h242

Long Description:

Return to Summary Table

Table 4-3510. Instance Table

Instance Name	Physical Address
VIM	50F0 13B8h

Figure 4-1687. VIM_INTPRIORITY_238 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3511. INTPRIORITY_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.317 VIM_INTPRIORITY_239 Register (Offset = 13BCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h243

Long Description:

Return to Summary Table

Table 4-3512. Instance Table

Instance Name	Physical Address
VIM	50F0 13BCh

Figure 4-1688. VIM_INTPRIORITY_239 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3513. INTPRIORITY_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.318 VIM_INTPRIORITY_240 Register (Offset = 13C0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h244

Long Description:

Return to Summary Table

Table 4-3514. Instance Table

Instance Name	Physical Address
VIM	50F0 13C0h

Figure 4-1689. VIM_INTPRIORITY_240 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3515. INTPRIORITY_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.319 VIM_INTPRIORITY_241 Register (Offset = 13C4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h245

Long Description:

Return to Summary Table

Table 4-3516. Instance Table

Instance Name	Physical Address
VIM	50F0 13C4h

Figure 4-1690. VIM_INTPRIORITY_241 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3517. INTPRIORITY_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.320 VIM_INTPRIORITY_242 Register (Offset = 13C8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h246

Long Description:

Return to Summary Table

Table 4-3518. Instance Table

Instance Name	Physical Address
VIM	50F0 13C8h

Figure 4-1691. VIM_INTPRIORITY_242 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3519. INTPRIORITY_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.321 VIM_INTPRIORITY_243 Register (Offset = 13CCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h247

Long Description:

Return to Summary Table

Table 4-3520. Instance Table

Instance Name	Physical Address
VIM	50F0 13CCh

Figure 4-1692. VIM_INTPRIORITY_243 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3521. INTPRIORITY_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.322 VIM_INTPRIORITY_244 Register (Offset = 13D0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h248

Long Description:

Return to Summary Table

Table 4-3522. Instance Table

Instance Name	Physical Address
VIM	50F0 13D0h

Figure 4-1693. VIM_INTPRIORITY_244 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3523. INTPRIORITY_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.323 VIM_INTPRIORITY_245 Register (Offset = 13D4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h249

Long Description:

Return to Summary Table

Table 4-3524. Instance Table

Instance Name	Physical Address
VIM	50F0 13D4h

Figure 4-1694. VIM_INTPRIORITY_245 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3525. INTPRIORITY_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.324 VIM_INTPRIORITY_246 Register (Offset = 13D8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h250

Long Description:

Return to Summary Table

Table 4-3526. Instance Table

Instance Name	Physical Address
VIM	50F0 13D8h

Figure 4-1695. VIM_INTPRIORITY_246 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3527. INTPRIORITY_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.325 VIM_INTPRIORITY_247 Register (Offset = 13DCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h251

Long Description:

Return to Summary Table

Table 4-3528. Instance Table

Instance Name	Physical Address
VIM	50F0 13DCh

Figure 4-1696. VIM_INTPRIORITY_247 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3529. INTPRIORITY_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.326 VIM_INTPRIORITY_248 Register (Offset = 13E0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h252

Long Description:

Return to Summary Table

Table 4-3530. Instance Table

Instance Name	Physical Address
VIM	50F0 13E0h

Figure 4-1697. VIM_INTPRIORITY_248 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3531. INTPRIORITY_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.327 VIM_INTPRIORITY_249 Register (Offset = 13E4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h253

Long Description:

Return to Summary Table

Table 4-3532. Instance Table

Instance Name	Physical Address
VIM	50F0 13E4h

Figure 4-1698. VIM_INTPRIORITY_249 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3533. INTPRIORITY_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.328 VIM_INTPRIORITY_250 Register (Offset = 13E8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h254

Long Description:

Return to Summary Table

Table 4-3534. Instance Table

Instance Name	Physical Address
VIM	50F0 13E8h

Figure 4-1699. VIM_INTPRIORITY_250 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3535. INTPRIORITY_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.329 VIM_INTPRIORITY_251 Register (Offset = 13ECh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h255

Long Description:

Return to Summary Table

Table 4-3536. Instance Table

Instance Name	Physical Address
VIM	50F0 13ECh

Figure 4-1700. VIM_INTPRIORITY_251 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3537. INTPRIORITY_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.330 VIM_INTPRIORITY_252 Register (Offset = 13F0h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h256

Long Description:

Return to Summary Table

Table 4-3538. Instance Table

Instance Name	Physical Address
VIM	50F0 13F0h

Figure 4-1701. VIM_INTPRIORITY_252 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3539. INTPRIORITY_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.331 VIM_INTPRIORITY_253 Register (Offset = 13F4h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h257

Long Description:

Return to Summary Table

Table 4-3540. Instance Table

Instance Name	Physical Address
VIM	50F0 13F4h

Figure 4-1702. VIM_INTPRIORITY_253 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3541. INTPRIORITY_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.332 VIM_INTPRIORITY_254 Register (Offset = 13F8h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h258

Long Description:

Return to Summary Table

Table 4-3542. Instance Table

Instance Name	Physical Address
VIM	50F0 13F8h

Figure 4-1703. VIM_INTPRIORITY_254 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3543. INTPRIORITY_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.333 VIM_INTPRIORITY_255 Register (Offset = 13FCh) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32) h1000 + Q x h259

Long Description:

Return to Summary Table

Table 4-3544. Instance Table

Instance Name	Physical Address
VIM	50F0 13FCh

Figure 4-1704. VIM_INTPRIORITY_255 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES19												PRI			
RO												RW			
0												1111			

Access Types Legend

Table 4-3545. INTPRIORITY_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

4.30.334 VIM_INTVECTOR Register (Offset = 2000h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h4

Long Description:

Return to Summary Table

Table 4-3546. Instance Table

Instance Name	Physical Address
VIM	50F0 2000h

Figure 4-1705. VIM_INTVECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3547. INTVECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.335 VIM_INTVECTOR_1 Register (Offset = 2004h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h5

Long Description:

Return to Summary Table

Table 4-3548. Instance Table

Instance Name	Physical Address
VIM	50F0 2004h

Figure 4-1706. VIM_INTVECTOR_1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3549. INTVECTOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.336 VIM_INTVECTOR_2 Register (Offset = 2008h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h6

Long Description:

Return to Summary Table

Table 4-3550. Instance Table

Instance Name	Physical Address
VIM	50F0 2008h

Figure 4-1707. VIM_INTVECTOR_2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3551. INTVECTOR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.337 VIM_INTVECTOR_3 Register (Offset = 200Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h7

Long Description:

Return to Summary Table

Table 4-3552. Instance Table

Instance Name	Physical Address
VIM	50F0 200Ch

Figure 4-1708. VIM_INTVECTOR_3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3553. INTVECTOR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.338 VIM_INTVECTOR_4 Register (Offset = 2010h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h8

Long Description:

Return to Summary Table

Table 4-3554. Instance Table

Instance Name	Physical Address
VIM	50F0 2010h

Figure 4-1709. VIM_INTVECTOR_4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3555. INTVECTOR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.339 VIM_INTVECTOR_5 Register (Offset = 2014h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h9

Long Description:

Return to Summary Table

Table 4-3556. Instance Table

Instance Name	Physical Address
VIM	50F0 2014h

Figure 4-1710. VIM_INTVECTOR_5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3557. INTVECTOR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.340 VIM_INTVECTOR_6 Register (Offset = 2018h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h10

Long Description:

Return to Summary Table

Table 4-3558. Instance Table

Instance Name	Physical Address
VIM	50F0 2018h

Figure 4-1711. VIM_INTVECTOR_6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3559. INTVECTOR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.341 VIM_INTVECTOR_7 Register (Offset = 201Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h11

Long Description:

Return to Summary Table

Table 4-3560. Instance Table

Instance Name	Physical Address
VIM	50F0 201Ch

Figure 4-1712. VIM_INTVECTOR_7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3561. INTVECTOR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.342 VIM_INTVECTOR_8 Register (Offset = 2020h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h12

Long Description:

Return to Summary Table

Table 4-3562. Instance Table

Instance Name	Physical Address
VIM	50F0 2020h

Figure 4-1713. VIM_INTVECTOR_8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3563. INTVECTOR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.343 VIM_INTVECTOR_9 Register (Offset = 2024h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h13

Long Description:

Return to Summary Table

Table 4-3564. Instance Table

Instance Name	Physical Address
VIM	50F0 2024h

Figure 4-1714. VIM_INTVECTOR_9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3565. INTVECTOR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.344 VIM_INTVECTOR_10 Register (Offset = 2028h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h14

Long Description:

Return to Summary Table

Table 4-3566. Instance Table

Instance Name	Physical Address
VIM	50F0 2028h

Figure 4-1715. VIM_INTVECTOR_10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3567. INTVECTOR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.345 VIM_INTVECTOR_11 Register (Offset = 202Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h15

Long Description:

Return to Summary Table

Table 4-3568. Instance Table

Instance Name	Physical Address
VIM	50F0 202Ch

Figure 4-1716. VIM_INTVECTOR_11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3569. INTVECTOR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.346 VIM_INTVECTOR_12 Register (Offset = 2030h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h16

Long Description:

Return to Summary Table

Table 4-3570. Instance Table

Instance Name	Physical Address
VIM	50F0 2030h

Figure 4-1717. VIM_INTVECTOR_12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3571. INTVECTOR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.347 VIM_INTVECTOR_13 Register (Offset = 2034h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h17

Long Description:

Return to Summary Table

Table 4-3572. Instance Table

Instance Name	Physical Address
VIM	50F0 2034h

Figure 4-1718. VIM_INTVECTOR_13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3573. INTVECTOR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.348 VIM_INTVECTOR_14 Register (Offset = 2038h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h18

Long Description:

Return to Summary Table

Table 4-3574. Instance Table

Instance Name	Physical Address
VIM	50F0 2038h

Figure 4-1719. VIM_INTVECTOR_14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3575. INTVECTOR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.349 VIM_INTVECTOR_15 Register (Offset = 203Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h19

Long Description:

Return to Summary Table

Table 4-3576. Instance Table

Instance Name	Physical Address
VIM	50F0 203Ch

Figure 4-1720. VIM_INTVECTOR_15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3577. INTVECTOR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.350 VIM_INTVECTOR_16 Register (Offset = 2040h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h20

Long Description:

Return to Summary Table

Table 4-3578. Instance Table

Instance Name	Physical Address
VIM	50F0 2040h

Figure 4-1721. VIM_INTVECTOR_16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3579. INTVECTOR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.351 VIM_INTVECTOR_17 Register (Offset = 2044h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h21

Long Description:

Return to Summary Table

Table 4-3580. Instance Table

Instance Name	Physical Address
VIM	50F0 2044h

Figure 4-1722. VIM_INTVECTOR_17 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3581. INTVECTOR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.352 VIM_INTVECTOR_18 Register (Offset = 2048h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h22

Long Description:

Return to Summary Table

Table 4-3582. Instance Table

Instance Name	Physical Address
VIM	50F0 2048h

Figure 4-1723. VIM_INTVECTOR_18 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3583. INTVECTOR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.353 VIM_INTVECTOR_19 Register (Offset = 204Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h23

Long Description:

Return to Summary Table

Table 4-3584. Instance Table

Instance Name	Physical Address
VIM	50F0 204Ch

Figure 4-1724. VIM_INTVECTOR_19 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3585. INTVECTOR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.354 VIM_INTVECTOR_20 Register (Offset = 2050h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h24

Long Description:

Return to Summary Table

Table 4-3586. Instance Table

Instance Name	Physical Address
VIM	50F0 2050h

Figure 4-1725. VIM_INTVECTOR_20 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3587. INTVECTOR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.355 VIM_INTVECTOR_21 Register (Offset = 2054h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h25

Long Description:

Return to Summary Table

Table 4-3588. Instance Table

Instance Name	Physical Address
VIM	50F0 2054h

Figure 4-1726. VIM_INTVECTOR_21 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3589. INTVECTOR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.356 VIM_INTVECTOR_22 Register (Offset = 2058h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h26

Long Description:

Return to Summary Table

Table 4-3590. Instance Table

Instance Name	Physical Address
VIM	50F0 2058h

Figure 4-1727. VIM_INTVECTOR_22 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3591. INTVECTOR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.357 VIM_INTVECTOR_23 Register (Offset = 205Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h27

Long Description:

Return to Summary Table

Table 4-3592. Instance Table

Instance Name	Physical Address
VIM	50F0 205Ch

Figure 4-1728. VIM_INTVECTOR_23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3593. INTVECTOR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.358 VIM_INTVECTOR_24 Register (Offset = 2060h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h28

Long Description:

Return to Summary Table

Table 4-3594. Instance Table

Instance Name	Physical Address
VIM	50F0 2060h

Figure 4-1729. VIM_INTVECTOR_24 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3595. INTVECTOR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.359 VIM_INTVECTOR_25 Register (Offset = 2064h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h29

Long Description:

Return to Summary Table

Table 4-3596. Instance Table

Instance Name	Physical Address
VIM	50F0 2064h

Figure 4-1730. VIM_INTVECTOR_25 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3597. INTVECTOR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.360 VIM_INTVECTOR_26 Register (Offset = 2068h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h30

Long Description:

Return to Summary Table

Table 4-3598. Instance Table

Instance Name	Physical Address
VIM	50F0 2068h

Figure 4-1731. VIM_INTVECTOR_26 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3599. INTVECTOR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.361 VIM_INTVECTOR_27 Register (Offset = 206Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h31

Long Description:

Return to Summary Table

Table 4-3600. Instance Table

Instance Name	Physical Address
VIM	50F0 206Ch

Figure 4-1732. VIM_INTVECTOR_27 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3601. INTVECTOR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.362 VIM_INTVECTOR_28 Register (Offset = 2070h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h32

Long Description:

Return to Summary Table

Table 4-3602. Instance Table

Instance Name	Physical Address
VIM	50F0 2070h

Figure 4-1733. VIM_INTVECTOR_28 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3603. INTVECTOR_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.363 VIM_INTVECTOR_29 Register (Offset = 2074h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h33

Long Description:

Return to Summary Table

Table 4-3604. Instance Table

Instance Name	Physical Address
VIM	50F0 2074h

Figure 4-1734. VIM_INTVECTOR_29 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3605. INTVECTOR_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.364 VIM_INTVECTOR_30 Register (Offset = 2078h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h34

Long Description:

Return to Summary Table

Table 4-3606. Instance Table

Instance Name	Physical Address
VIM	50F0 2078h

Figure 4-1735. VIM_INTVECTOR_30 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3607. INTVECTOR_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.365 VIM_INTVECTOR_31 Register (Offset = 207Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h35

Long Description:

Return to Summary Table

Table 4-3608. Instance Table

Instance Name	Physical Address
VIM	50F0 207Ch

Figure 4-1736. VIM_INTVECTOR_31 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3609. INTVECTOR_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.366 VIM_INTVECTOR_32 Register (Offset = 2080h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h36

Long Description:

Return to Summary Table

Table 4-3610. Instance Table

Instance Name	Physical Address
VIM	50F0 2080h

Figure 4-1737. VIM_INTVECTOR_32 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3611. INTVECTOR_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.367 VIM_INTVECTOR_33 Register (Offset = 2084h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h37

Long Description:

Return to Summary Table

Table 4-3612. Instance Table

Instance Name	Physical Address
VIM	50F0 2084h

Figure 4-1738. VIM_INTVECTOR_33 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3613. INTVECTOR_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.368 VIM_INTVECTOR_34 Register (Offset = 2088h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h38

Long Description:

Return to Summary Table

Table 4-3614. Instance Table

Instance Name	Physical Address
VIM	50F0 2088h

Figure 4-1739. VIM_INTVECTOR_34 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3615. INTVECTOR_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.369 VIM_INTVECTOR_35 Register (Offset = 208Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h39

Long Description:

Return to Summary Table

Table 4-3616. Instance Table

Instance Name	Physical Address
VIM	50F0 208Ch

Figure 4-1740. VIM_INTVECTOR_35 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3617. INTVECTOR_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.370 VIM_INTVECTOR_36 Register (Offset = 2090h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h40

Long Description:

Return to Summary Table

Table 4-3618. Instance Table

Instance Name	Physical Address
VIM	50F0 2090h

Figure 4-1741. VIM_INTVECTOR_36 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3619. INTVECTOR_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.371 VIM_INTVECTOR_37 Register (Offset = 2094h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h41

Long Description:

Return to Summary Table

Table 4-3620. Instance Table

Instance Name	Physical Address
VIM	50F0 2094h

Figure 4-1742. VIM_INTVECTOR_37 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3621. INTVECTOR_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.372 VIM_INTVECTOR_38 Register (Offset = 2098h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h42

Long Description:

Return to Summary Table

Table 4-3622. Instance Table

Instance Name	Physical Address
VIM	50F0 2098h

Figure 4-1743. VIM_INTVECTOR_38 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3623. INTVECTOR_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.373 VIM_INTVECTOR_39 Register (Offset = 209Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h43

Long Description:

Return to Summary Table

Table 4-3624. Instance Table

Instance Name	Physical Address
VIM	50F0 209Ch

Figure 4-1744. VIM_INTVECTOR_39 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3625. INTVECTOR_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.374 VIM_INTVECTOR_40 Register (Offset = 20A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h44

Long Description:

Return to Summary Table

Table 4-3626. Instance Table

Instance Name	Physical Address
VIM	50F0 20A0h

Figure 4-1745. VIM_INTVECTOR_40 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3627. INTVECTOR_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.375 VIM_INTVECTOR_41 Register (Offset = 20A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h45

Long Description:

Return to Summary Table

Table 4-3628. Instance Table

Instance Name	Physical Address
VIM	50F0 20A4h

Figure 4-1746. VIM_INTVECTOR_41 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3629. INTVECTOR_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.376 VIM_INTVECTOR_42 Register (Offset = 20A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h46

Long Description:

Return to Summary Table

Table 4-3630. Instance Table

Instance Name	Physical Address
VIM	50F0 20A8h

Figure 4-1747. VIM_INTVECTOR_42 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3631. INTVECTOR_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.377 VIM_INTVECTOR_43 Register (Offset = 20ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h47

Long Description:

Return to Summary Table

Table 4-3632. Instance Table

Instance Name	Physical Address
VIM	50F0 20ACh

Figure 4-1748. VIM_INTVECTOR_43 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3633. INTVECTOR_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.378 VIM_INTVECTOR_44 Register (Offset = 20B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h48

Long Description:

Return to Summary Table

Table 4-3634. Instance Table

Instance Name	Physical Address
VIM	50F0 20B0h

Figure 4-1749. VIM_INTVECTOR_44 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3635. INTVECTOR_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.379 VIM_INTVECTOR_45 Register (Offset = 20B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h49

Long Description:

Return to Summary Table

Table 4-3636. Instance Table

Instance Name	Physical Address
VIM	50F0 20B4h

Figure 4-1750. VIM_INTVECTOR_45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3637. INTVECTOR_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.380 VIM_INTVECTOR_46 Register (Offset = 20B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h50

Long Description:

Return to Summary Table

Table 4-3638. Instance Table

Instance Name	Physical Address
VIM	50F0 20B8h

Figure 4-1751. VIM_INTVECTOR_46 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3639. INTVECTOR_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.381 VIM_INTVECTOR_47 Register (Offset = 20BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h51

Long Description:

Return to Summary Table

Table 4-3640. Instance Table

Instance Name	Physical Address
VIM	50F0 20BCh

Figure 4-1752. VIM_INTVECTOR_47 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3641. INTVECTOR_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.382 VIM_INTVECTOR_48 Register (Offset = 20C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h52

Long Description:

Return to Summary Table

Table 4-3642. Instance Table

Instance Name	Physical Address
VIM	50F0 20C0h

Figure 4-1753. VIM_INTVECTOR_48 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3643. INTVECTOR_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.383 VIM_INTVECTOR_49 Register (Offset = 20C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h53

Long Description:

Return to Summary Table

Table 4-3644. Instance Table

Instance Name	Physical Address
VIM	50F0 20C4h

Figure 4-1754. VIM_INTVECTOR_49 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3645. INTVECTOR_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.384 VIM_INTVECTOR_50 Register (Offset = 20C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h54

Long Description:

Return to Summary Table

Table 4-3646. Instance Table

Instance Name	Physical Address
VIM	50F0 20C8h

Figure 4-1755. VIM_INTVECTOR_50 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3647. INTVECTOR_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.385 VIM_INTVECTOR_51 Register (Offset = 20CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h55

Long Description:

Return to Summary Table

Table 4-3648. Instance Table

Instance Name	Physical Address
VIM	50F0 20CCh

Figure 4-1756. VIM_INTVECTOR_51 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3649. INTVECTOR_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.386 VIM_INTVECTOR_52 Register (Offset = 20D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h56

Long Description:

Return to Summary Table

Table 4-3650. Instance Table

Instance Name	Physical Address
VIM	50F0 20D0h

Figure 4-1757. VIM_INTVECTOR_52 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3651. INTVECTOR_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.387 VIM_INTVECTOR_53 Register (Offset = 20D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h57

Long Description:

Return to Summary Table

Table 4-3652. Instance Table

Instance Name	Physical Address
VIM	50F0 20D4h

Figure 4-1758. VIM_INTVECTOR_53 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3653. INTVECTOR_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.388 VIM_INTVECTOR_54 Register (Offset = 20D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h58

Long Description:

Return to Summary Table

Table 4-3654. Instance Table

Instance Name	Physical Address
VIM	50F0 20D8h

Figure 4-1759. VIM_INTVECTOR_54 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3655. INTVECTOR_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.389 VIM_INTVECTOR_55 Register (Offset = 20DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h59

Long Description:

Return to Summary Table

Table 4-3656. Instance Table

Instance Name	Physical Address
VIM	50F0 20DCh

Figure 4-1760. VIM_INTVECTOR_55 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3657. INTVECTOR_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.390 VIM_INTVECTOR_56 Register (Offset = 20E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h60

Long Description:

Return to Summary Table

Table 4-3658. Instance Table

Instance Name	Physical Address
VIM	50F0 20E0h

Figure 4-1761. VIM_INTVECTOR_56 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3659. INTVECTOR_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.391 VIM_INTVECTOR_57 Register (Offset = 20E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h61

Long Description:

Return to Summary Table

Table 4-3660. Instance Table

Instance Name	Physical Address
VIM	50F0 20E4h

Figure 4-1762. VIM_INTVECTOR_57 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3661. INTVECTOR_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.392 VIM_INTVECTOR_58 Register (Offset = 20E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h62

Long Description:

Return to Summary Table

Table 4-3662. Instance Table

Instance Name	Physical Address
VIM	50F0 20E8h

Figure 4-1763. VIM_INTVECTOR_58 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3663. INTVECTOR_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.393 VIM_INTVECTOR_59 Register (Offset = 20ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h63

Long Description:

Return to Summary Table

Table 4-3664. Instance Table

Instance Name	Physical Address
VIM	50F0 20ECh

Figure 4-1764. VIM_INTVECTOR_59 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3665. INTVECTOR_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.394 VIM_INTVECTOR_60 Register (Offset = 20F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h64

Long Description:

Return to Summary Table

Table 4-3666. Instance Table

Instance Name	Physical Address
VIM	50F0 20F0h

Figure 4-1765. VIM_INTVECTOR_60 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3667. INTVECTOR_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.395 VIM_INTVECTOR_61 Register (Offset = 20F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h65

Long Description:

Return to Summary Table

Table 4-3668. Instance Table

Instance Name	Physical Address
VIM	50F0 20F4h

Figure 4-1766. VIM_INTVECTOR_61 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3669. INTVECTOR_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.396 VIM_INTVECTOR_62 Register (Offset = 20F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h66

Long Description:

Return to Summary Table

Table 4-3670. Instance Table

Instance Name	Physical Address
VIM	50F0 20F8h

Figure 4-1767. VIM_INTVECTOR_62 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3671. INTVECTOR_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.397 VIM_INTVECTOR_63 Register (Offset = 20FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h67

Long Description:

Return to Summary Table

Table 4-3672. Instance Table

Instance Name	Physical Address
VIM	50F0 20FCh

Figure 4-1768. VIM_INTVECTOR_63 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3673. INTVECTOR_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.398 VIM_INTVECTOR_64 Register (Offset = 2100h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h68

Long Description:

Return to Summary Table

Table 4-3674. Instance Table

Instance Name	Physical Address
VIM	50F0 2100h

Figure 4-1769. VIM_INTVECTOR_64 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3675. INTVECTOR_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.399 VIM_INTVECTOR_65 Register (Offset = 2104h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h69

Long Description:

Return to Summary Table

Table 4-3676. Instance Table

Instance Name	Physical Address
VIM	50F0 2104h

Figure 4-1770. VIM_INTVECTOR_65 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3677. INTVECTOR_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.400 VIM_INTVECTOR_66 Register (Offset = 2108h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h70

Long Description:

Return to Summary Table

Table 4-3678. Instance Table

Instance Name	Physical Address
VIM	50F0 2108h

Figure 4-1771. VIM_INTVECTOR_66 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3679. INTVECTOR_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.401 VIM_INTVECTOR_67 Register (Offset = 210Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h71

Long Description:

Return to Summary Table

Table 4-3680. Instance Table

Instance Name	Physical Address
VIM	50F0 210Ch

Figure 4-1772. VIM_INTVECTOR_67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3681. INTVECTOR_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.402 VIM_INTVECTOR_68 Register (Offset = 2110h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h72

Long Description:

Return to Summary Table

Table 4-3682. Instance Table

Instance Name	Physical Address
VIM	50F0 2110h

Figure 4-1773. VIM_INTVECTOR_68 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3683. INTVECTOR_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.403 VIM_INTVECTOR_69 Register (Offset = 2114h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h73

Long Description:

Return to Summary Table

Table 4-3684. Instance Table

Instance Name	Physical Address
VIM	50F0 2114h

Figure 4-1774. VIM_INTVECTOR_69 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3685. INTVECTOR_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.404 VIM_INTVECTOR_70 Register (Offset = 2118h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h74

Long Description:

Return to Summary Table

Table 4-3686. Instance Table

Instance Name	Physical Address
VIM	50F0 2118h

Figure 4-1775. VIM_INTVECTOR_70 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3687. INTVECTOR_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.405 VIM_INTVECTOR_71 Register (Offset = 211Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h75

Long Description:

Return to Summary Table

Table 4-3688. Instance Table

Instance Name	Physical Address
VIM	50F0 211Ch

Figure 4-1776. VIM_INTVECTOR_71 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3689. INTVECTOR_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.406 VIM_INTVECTOR_72 Register (Offset = 2120h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h76

Long Description:

Return to Summary Table

Table 4-3690. Instance Table

Instance Name	Physical Address
VIM	50F0 2120h

Figure 4-1777. VIM_INTVECTOR_72 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3691. INTVECTOR_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.407 VIM_INTVECTOR_73 Register (Offset = 2124h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h77

Long Description:

Return to Summary Table

Table 4-3692. Instance Table

Instance Name	Physical Address
VIM	50F0 2124h

Figure 4-1778. VIM_INTVECTOR_73 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3693. INTVECTOR_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.408 VIM_INTVECTOR_74 Register (Offset = 2128h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h78

Long Description:

Return to Summary Table

Table 4-3694. Instance Table

Instance Name	Physical Address
VIM	50F0 2128h

Figure 4-1779. VIM_INTVECTOR_74 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3695. INTVECTOR_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.409 VIM_INTVECTOR_75 Register (Offset = 212Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h79

Long Description:

Return to Summary Table

Table 4-3696. Instance Table

Instance Name	Physical Address
VIM	50F0 212Ch

Figure 4-1780. VIM_INTVECTOR_75 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3697. INTVECTOR_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.410 VIM_INTVECTOR_76 Register (Offset = 2130h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h80

Long Description:

Return to Summary Table

Table 4-3698. Instance Table

Instance Name	Physical Address
VIM	50F0 2130h

Figure 4-1781. VIM_INTVECTOR_76 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3699. INTVECTOR_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.411 VIM_INTVECTOR_77 Register (Offset = 2134h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h81

Long Description:

Return to Summary Table

Table 4-3700. Instance Table

Instance Name	Physical Address
VIM	50F0 2134h

Figure 4-1782. VIM_INTVECTOR_77 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3701. INTVECTOR_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.412 VIM_INTVECTOR_78 Register (Offset = 2138h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h82

Long Description:

Return to Summary Table

Table 4-3702. Instance Table

Instance Name	Physical Address
VIM	50F0 2138h

Figure 4-1783. VIM_INTVECTOR_78 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3703. INTVECTOR_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.413 VIM_INTVECTOR_79 Register (Offset = 213Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h83

Long Description:

Return to Summary Table

Table 4-3704. Instance Table

Instance Name	Physical Address
VIM	50F0 213Ch

Figure 4-1784. VIM_INTVECTOR_79 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3705. INTVECTOR_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.414 VIM_INTVECTOR_80 Register (Offset = 2140h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h84

Long Description:

Return to Summary Table

Table 4-3706. Instance Table

Instance Name	Physical Address
VIM	50F0 2140h

Figure 4-1785. VIM_INTVECTOR_80 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3707. INTVECTOR_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.415 VIM_INTVECTOR_81 Register (Offset = 2144h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h85

Long Description:

Return to Summary Table

Table 4-3708. Instance Table

Instance Name	Physical Address
VIM	50F0 2144h

Figure 4-1786. VIM_INTVECTOR_81 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3709. INTVECTOR_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.416 VIM_INTVECTOR_82 Register (Offset = 2148h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h86

Long Description:

Return to Summary Table

Table 4-3710. Instance Table

Instance Name	Physical Address
VIM	50F0 2148h

Figure 4-1787. VIM_INTVECTOR_82 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3711. INTVECTOR_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.417 VIM_INTVECTOR_83 Register (Offset = 214Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h87

Long Description:

Return to Summary Table

Table 4-3712. Instance Table

Instance Name	Physical Address
VIM	50F0 214Ch

Figure 4-1788. VIM_INTVECTOR_83 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3713. INTVECTOR_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.418 VIM_INTVECTOR_84 Register (Offset = 2150h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h88

Long Description:

Return to Summary Table

Table 4-3714. Instance Table

Instance Name	Physical Address
VIM	50F0 2150h

Figure 4-1789. VIM_INTVECTOR_84 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3715. INTVECTOR_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.419 VIM_INTVECTOR_85 Register (Offset = 2154h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h89

Long Description:

Return to Summary Table

Table 4-3716. Instance Table

Instance Name	Physical Address
VIM	50F0 2154h

Figure 4-1790. VIM_INTVECTOR_85 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3717. INTVECTOR_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.420 VIM_INTVECTOR_86 Register (Offset = 2158h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h90

Long Description:

Return to Summary Table

Table 4-3718. Instance Table

Instance Name	Physical Address
VIM	50F0 2158h

Figure 4-1791. VIM_INTVECTOR_86 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3719. INTVECTOR_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.421 VIM_INTVECTOR_87 Register (Offset = 215Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h91

Long Description:

Return to Summary Table

Table 4-3720. Instance Table

Instance Name	Physical Address
VIM	50F0 215Ch

Figure 4-1792. VIM_INTVECTOR_87 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3721. INTVECTOR_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.422 VIM_INTVECTOR_88 Register (Offset = 2160h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h92

Long Description:

Return to Summary Table

Table 4-3722. Instance Table

Instance Name	Physical Address
VIM	50F0 2160h

Figure 4-1793. VIM_INTVECTOR_88 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3723. INTVECTOR_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.423 VIM_INTVECTOR_89 Register (Offset = 2164h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h93

Long Description:

Return to Summary Table

Table 4-3724. Instance Table

Instance Name	Physical Address
VIM	50F0 2164h

Figure 4-1794. VIM_INTVECTOR_89 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3725. INTVECTOR_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.424 VIM_INTVECTOR_90 Register (Offset = 2168h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h94

Long Description:

Return to Summary Table

Table 4-3726. Instance Table

Instance Name	Physical Address
VIM	50F0 2168h

Figure 4-1795. VIM_INTVECTOR_90 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3727. INTVECTOR_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.425 VIM_INTVECTOR_91 Register (Offset = 216Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h95

Long Description:

Return to Summary Table

Table 4-3728. Instance Table

Instance Name	Physical Address
VIM	50F0 216Ch

Figure 4-1796. VIM_INTVECTOR_91 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3729. INTVECTOR_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.426 VIM_INTVECTOR_92 Register (Offset = 2170h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h96

Long Description:

Return to Summary Table

Table 4-3730. Instance Table

Instance Name	Physical Address
VIM	50F0 2170h

Figure 4-1797. VIM_INTVECTOR_92 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3731. INTVECTOR_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.427 VIM_INTVECTOR_93 Register (Offset = 2174h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h97

Long Description:

Return to Summary Table

Table 4-3732. Instance Table

Instance Name	Physical Address
VIM	50F0 2174h

Figure 4-1798. VIM_INTVECTOR_93 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3733. INTVECTOR_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.428 VIM_INTVECTOR_94 Register (Offset = 2178h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h98

Long Description:

Return to Summary Table

Table 4-3734. Instance Table

Instance Name	Physical Address
VIM	50F0 2178h

Figure 4-1799. VIM_INTVECTOR_94 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3735. INTVECTOR_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.429 VIM_INTVECTOR_95 Register (Offset = 217Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h99

Long Description:

Return to Summary Table

Table 4-3736. Instance Table

Instance Name	Physical Address
VIM	50F0 217Ch

Figure 4-1800. VIM_INTVECTOR_95 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3737. INTVECTOR_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.430 VIM_INTVECTOR_96 Register (Offset = 2180h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h100

Long Description:

Return to Summary Table

Table 4-3738. Instance Table

Instance Name	Physical Address
VIM	50F0 2180h

Figure 4-1801. VIM_INTVECTOR_96 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3739. INTVECTOR_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.431 VIM_INTVECTOR_97 Register (Offset = 2184h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h101

Long Description:

Return to Summary Table

Table 4-3740. Instance Table

Instance Name	Physical Address
VIM	50F0 2184h

Figure 4-1802. VIM_INTVECTOR_97 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3741. INTVECTOR_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.432 VIM_INTVECTOR_98 Register (Offset = 2188h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h102

Long Description:

Return to Summary Table

Table 4-3742. Instance Table

Instance Name	Physical Address
VIM	50F0 2188h

Figure 4-1803. VIM_INTVECTOR_98 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3743. INTVECTOR_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.433 VIM_INTVECTOR_99 Register (Offset = 218Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h103

Long Description:

Return to Summary Table

Table 4-3744. Instance Table

Instance Name	Physical Address
VIM	50F0 218Ch

Figure 4-1804. VIM_INTVECTOR_99 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3745. INTVECTOR_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.434 VIM_INTVECTOR_100 Register (Offset = 2190h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h104

Long Description:

Return to Summary Table

Table 4-3746. Instance Table

Instance Name	Physical Address
VIM	50F0 2190h

Figure 4-1805. VIM_INTVECTOR_100 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3747. INTVECTOR_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.435 VIM_INTVECTOR_101 Register (Offset = 2194h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h105

Long Description:

Return to Summary Table

Table 4-3748. Instance Table

Instance Name	Physical Address
VIM	50F0 2194h

Figure 4-1806. VIM_INTVECTOR_101 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3749. INTVECTOR_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.436 VIM_INTVECTOR_102 Register (Offset = 2198h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h106

Long Description:

Return to Summary Table

Table 4-3750. Instance Table

Instance Name	Physical Address
VIM	50F0 2198h

Figure 4-1807. VIM_INTVECTOR_102 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3751. INTVECTOR_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.437 VIM_INTVECTOR_103 Register (Offset = 219Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h107

Long Description:

Return to Summary Table

Table 4-3752. Instance Table

Instance Name	Physical Address
VIM	50F0 219Ch

Figure 4-1808. VIM_INTVECTOR_103 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3753. INTVECTOR_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.438 VIM_INTVECTOR_104 Register (Offset = 21A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h108

Long Description:

Return to Summary Table

Table 4-3754. Instance Table

Instance Name	Physical Address
VIM	50F0 21A0h

Figure 4-1809. VIM_INTVECTOR_104 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3755. INTVECTOR_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.439 VIM_INTVECTOR_105 Register (Offset = 21A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h109

Long Description:

Return to Summary Table

Table 4-3756. Instance Table

Instance Name	Physical Address
VIM	50F0 21A4h

Figure 4-1810. VIM_INTVECTOR_105 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3757. INTVECTOR_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.440 VIM_INTVECTOR_106 Register (Offset = 21A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h110

Long Description:

Return to Summary Table

Table 4-3758. Instance Table

Instance Name	Physical Address
VIM	50F0 21A8h

Figure 4-1811. VIM_INTVECTOR_106 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3759. INTVECTOR_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.441 VIM_INTVECTOR_107 Register (Offset = 21ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h111

Long Description:

Return to Summary Table

Table 4-3760. Instance Table

Instance Name	Physical Address
VIM	50F0 21ACh

Figure 4-1812. VIM_INTVECTOR_107 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3761. INTVECTOR_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.442 VIM_INTVECTOR_108 Register (Offset = 21B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h112

Long Description:

Return to Summary Table

Table 4-3762. Instance Table

Instance Name	Physical Address
VIM	50F0 21B0h

Figure 4-1813. VIM_INTVECTOR_108 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3763. INTVECTOR_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.443 VIM_INTVECTOR_109 Register (Offset = 21B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h113

Long Description:

Return to Summary Table

Table 4-3764. Instance Table

Instance Name	Physical Address
VIM	50F0 21B4h

Figure 4-1814. VIM_INTVECTOR_109 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3765. INTVECTOR_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.444 VIM_INTVECTOR_110 Register (Offset = 21B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h114

Long Description:

Return to Summary Table

Table 4-3766. Instance Table

Instance Name	Physical Address
VIM	50F0 21B8h

Figure 4-1815. VIM_INTVECTOR_110 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3767. INTVECTOR_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.445 VIM_INTVECTOR_111 Register (Offset = 21BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h115

Long Description:

Return to Summary Table

Table 4-3768. Instance Table

Instance Name	Physical Address
VIM	50F0 21BCh

Figure 4-1816. VIM_INTVECTOR_111 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3769. INTVECTOR_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.446 VIM_INTVECTOR_112 Register (Offset = 21C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h116

Long Description:

Return to Summary Table

Table 4-3770. Instance Table

Instance Name	Physical Address
VIM	50F0 21C0h

Figure 4-1817. VIM_INTVECTOR_112 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3771. INTVECTOR_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.447 VIM_INTVECTOR_113 Register (Offset = 21C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h117

Long Description:

Return to Summary Table

Table 4-3772. Instance Table

Instance Name	Physical Address
VIM	50F0 21C4h

Figure 4-1818. VIM_INTVECTOR_113 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3773. INTVECTOR_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.448 VIM_INTVECTOR_114 Register (Offset = 21C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h118

Long Description:

Return to Summary Table

Table 4-3774. Instance Table

Instance Name	Physical Address
VIM	50F0 21C8h

Figure 4-1819. VIM_INTVECTOR_114 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3775. INTVECTOR_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.449 VIM_INTVECTOR_115 Register (Offset = 21CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h119

Long Description:

Return to Summary Table

Table 4-3776. Instance Table

Instance Name	Physical Address
VIM	50F0 21CCh

Figure 4-1820. VIM_INTVECTOR_115 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3777. INTVECTOR_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.450 VIM_INTVECTOR_116 Register (Offset = 21D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h120

Long Description:

Return to Summary Table

Table 4-3778. Instance Table

Instance Name	Physical Address
VIM	50F0 21D0h

Figure 4-1821. VIM_INTVECTOR_116 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3779. INTVECTOR_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.451 VIM_INTVECTOR_117 Register (Offset = 21D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h121

Long Description:

Return to Summary Table

Table 4-3780. Instance Table

Instance Name	Physical Address
VIM	50F0 21D4h

Figure 4-1822. VIM_INTVECTOR_117 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3781. INTVECTOR_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.452 VIM_INTVECTOR_118 Register (Offset = 21D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h122

Long Description:

Return to Summary Table

Table 4-3782. Instance Table

Instance Name	Physical Address
VIM	50F0 21D8h

Figure 4-1823. VIM_INTVECTOR_118 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3783. INTVECTOR_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.453 VIM_INTVECTOR_119 Register (Offset = 21DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h123

Long Description:

Return to Summary Table

Table 4-3784. Instance Table

Instance Name	Physical Address
VIM	50F0 21DCh

Figure 4-1824. VIM_INTVECTOR_119 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3785. INTVECTOR_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.454 VIM_INTVECTOR_120 Register (Offset = 21E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h124

Long Description:

Return to Summary Table

Table 4-3786. Instance Table

Instance Name	Physical Address
VIM	50F0 21E0h

Figure 4-1825. VIM_INTVECTOR_120 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3787. INTVECTOR_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.455 VIM_INTVECTOR_121 Register (Offset = 21E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h125

Long Description:

Return to Summary Table

Table 4-3788. Instance Table

Instance Name	Physical Address
VIM	50F0 21E4h

Figure 4-1826. VIM_INTVECTOR_121 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3789. INTVECTOR_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.456 VIM_INTVECTOR_122 Register (Offset = 21E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h126

Long Description:

Return to Summary Table

Table 4-3790. Instance Table

Instance Name	Physical Address
VIM	50F0 21E8h

Figure 4-1827. VIM_INTVECTOR_122 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3791. INTVECTOR_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.457 VIM_INTVECTOR_123 Register (Offset = 21ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h127

Long Description:

Return to Summary Table

Table 4-3792. Instance Table

Instance Name	Physical Address
VIM	50F0 21ECh

Figure 4-1828. VIM_INTVECTOR_123 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3793. INTVECTOR_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.458 VIM_INTVECTOR_124 Register (Offset = 21F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h128

Long Description:

Return to Summary Table

Table 4-3794. Instance Table

Instance Name	Physical Address
VIM	50F0 21F0h

Figure 4-1829. VIM_INTVECTOR_124 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3795. INTVECTOR_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.459 VIM_INTVECTOR_125 Register (Offset = 21F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h129

Long Description:

Return to Summary Table

Table 4-3796. Instance Table

Instance Name	Physical Address
VIM	50F0 21F4h

Figure 4-1830. VIM_INTVECTOR_125 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3797. INTVECTOR_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.460 VIM_INTVECTOR_126 Register (Offset = 21F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h130

Long Description:

Return to Summary Table

Table 4-3798. Instance Table

Instance Name	Physical Address
VIM	50F0 21F8h

Figure 4-1831. VIM_INTVECTOR_126 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3799. INTVECTOR_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.461 VIM_INTVECTOR_127 Register (Offset = 21FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h131

Long Description:

Return to Summary Table

Table 4-3800. Instance Table

Instance Name	Physical Address
VIM	50F0 21FCh

Figure 4-1832. VIM_INTVECTOR_127 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3801. INTVECTOR_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.462 VIM_INTVECTOR_128 Register (Offset = 2200h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h132

Long Description:

Return to Summary Table

Table 4-3802. Instance Table

Instance Name	Physical Address
VIM	50F0 2200h

Figure 4-1833. VIM_INTVECTOR_128 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3803. INTVECTOR_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.463 VIM_INTVECTOR_129 Register (Offset = 2204h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h133

Long Description:

Return to Summary Table

Table 4-3804. Instance Table

Instance Name	Physical Address
VIM	50F0 2204h

Figure 4-1834. VIM_INTVECTOR_129 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3805. INTVECTOR_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.464 VIM_INTVECTOR_130 Register (Offset = 2208h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h134

Long Description:

Return to Summary Table

Table 4-3806. Instance Table

Instance Name	Physical Address
VIM	50F0 2208h

Figure 4-1835. VIM_INTVECTOR_130 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3807. INTVECTOR_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.465 VIM_INTVECTOR_131 Register (Offset = 220Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h135

Long Description:

Return to Summary Table

Table 4-3808. Instance Table

Instance Name	Physical Address
VIM	50F0 220Ch

Figure 4-1836. VIM_INTVECTOR_131 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3809. INTVECTOR_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.466 VIM_INTVECTOR_132 Register (Offset = 2210h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h136

Long Description:

Return to Summary Table

Table 4-3810. Instance Table

Instance Name	Physical Address
VIM	50F0 2210h

Figure 4-1837. VIM_INTVECTOR_132 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3811. INTVECTOR_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.467 VIM_INTVECTOR_133 Register (Offset = 2214h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h137

Long Description:

Return to Summary Table

Table 4-3812. Instance Table

Instance Name	Physical Address
VIM	50F0 2214h

Figure 4-1838. VIM_INTVECTOR_133 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3813. INTVECTOR_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.468 VIM_INTVECTOR_134 Register (Offset = 2218h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h138

Long Description:

Return to Summary Table

Table 4-3814. Instance Table

Instance Name	Physical Address
VIM	50F0 2218h

Figure 4-1839. VIM_INTVECTOR_134 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3815. INTVECTOR_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.469 VIM_INTVECTOR_135 Register (Offset = 221Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h139

Long Description:

Return to Summary Table

Table 4-3816. Instance Table

Instance Name	Physical Address
VIM	50F0 221Ch

Figure 4-1840. VIM_INTVECTOR_135 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3817. INTVECTOR_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.470 VIM_INTVECTOR_136 Register (Offset = 2220h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h140

Long Description:

Return to Summary Table

Table 4-3818. Instance Table

Instance Name	Physical Address
VIM	50F0 2220h

Figure 4-1841. VIM_INTVECTOR_136 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3819. INTVECTOR_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.471 VIM_INTVECTOR_137 Register (Offset = 2224h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h141

Long Description:

Return to Summary Table

Table 4-3820. Instance Table

Instance Name	Physical Address
VIM	50F0 2224h

Figure 4-1842. VIM_INTVECTOR_137 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3821. INTVECTOR_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.472 VIM_INTVECTOR_138 Register (Offset = 2228h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h142

Long Description:

Return to Summary Table

Table 4-3822. Instance Table

Instance Name	Physical Address
VIM	50F0 2228h

Figure 4-1843. VIM_INTVECTOR_138 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3823. INTVECTOR_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.473 VIM_INTVECTOR_139 Register (Offset = 222Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h143

Long Description:

Return to Summary Table

Table 4-3824. Instance Table

Instance Name	Physical Address
VIM	50F0 222Ch

Figure 4-1844. VIM_INTVECTOR_139 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3825. INTVECTOR_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.474 VIM_INTVECTOR_140 Register (Offset = 2230h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h144

Long Description:

Return to Summary Table

Table 4-3826. Instance Table

Instance Name	Physical Address
VIM	50F0 2230h

Figure 4-1845. VIM_INTVECTOR_140 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3827. INTVECTOR_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.475 VIM_INTVECTOR_141 Register (Offset = 2234h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h145

Long Description:

Return to Summary Table

Table 4-3828. Instance Table

Instance Name	Physical Address
VIM	50F0 2234h

Figure 4-1846. VIM_INTVECTOR_141 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3829. INTVECTOR_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.476 VIM_INTVECTOR_142 Register (Offset = 2238h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h146

Long Description:

Return to Summary Table

Table 4-3830. Instance Table

Instance Name	Physical Address
VIM	50F0 2238h

Figure 4-1847. VIM_INTVECTOR_142 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3831. INTVECTOR_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.477 VIM_INTVECTOR_143 Register (Offset = 223Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h147

Long Description:

Return to Summary Table

Table 4-3832. Instance Table

Instance Name	Physical Address
VIM	50F0 223Ch

Figure 4-1848. VIM_INTVECTOR_143 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3833. INTVECTOR_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.478 VIM_INTVECTOR_144 Register (Offset = 2240h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h148

Long Description:

Return to Summary Table

Table 4-3834. Instance Table

Instance Name	Physical Address
VIM	50F0 2240h

Figure 4-1849. VIM_INTVECTOR_144 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3835. INTVECTOR_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.479 VIM_INTVECTOR_145 Register (Offset = 2244h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h149

Long Description:

Return to Summary Table

Table 4-3836. Instance Table

Instance Name	Physical Address
VIM	50F0 2244h

Figure 4-1850. VIM_INTVECTOR_145 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3837. INTVECTOR_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.480 VIM_INTVECTOR_146 Register (Offset = 2248h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h150

Long Description:

Return to Summary Table

Table 4-3838. Instance Table

Instance Name	Physical Address
VIM	50F0 2248h

Figure 4-1851. VIM_INTVECTOR_146 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3839. INTVECTOR_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.481 VIM_INTVECTOR_147 Register (Offset = 224Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h151

Long Description:

Return to Summary Table

Table 4-3840. Instance Table

Instance Name	Physical Address
VIM	50F0 224Ch

Figure 4-1852. VIM_INTVECTOR_147 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3841. INTVECTOR_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.482 VIM_INTVECTOR_148 Register (Offset = 2250h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h152

Long Description:

Return to Summary Table

Table 4-3842. Instance Table

Instance Name	Physical Address
VIM	50F0 2250h

Figure 4-1853. VIM_INTVECTOR_148 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3843. INTVECTOR_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.483 VIM_INTVECTOR_149 Register (Offset = 2254h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h153

Long Description:

Return to Summary Table

Table 4-3844. Instance Table

Instance Name	Physical Address
VIM	50F0 2254h

Figure 4-1854. VIM_INTVECTOR_149 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3845. INTVECTOR_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.484 VIM_INTVECTOR_150 Register (Offset = 2258h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h154

Long Description:

Return to Summary Table

Table 4-3846. Instance Table

Instance Name	Physical Address
VIM	50F0 2258h

Figure 4-1855. VIM_INTVECTOR_150 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3847. INTVECTOR_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.485 VIM_INTVECTOR_151 Register (Offset = 225Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h155

Long Description:

Return to Summary Table

Table 4-3848. Instance Table

Instance Name	Physical Address
VIM	50F0 225Ch

Figure 4-1856. VIM_INTVECTOR_151 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3849. INTVECTOR_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.486 VIM_INTVECTOR_152 Register (Offset = 2260h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h156

Long Description:

Return to Summary Table

Table 4-3850. Instance Table

Instance Name	Physical Address
VIM	50F0 2260h

Figure 4-1857. VIM_INTVECTOR_152 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3851. INTVECTOR_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.487 VIM_INTVECTOR_153 Register (Offset = 2264h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h157

Long Description:

Return to Summary Table

Table 4-3852. Instance Table

Instance Name	Physical Address
VIM	50F0 2264h

Figure 4-1858. VIM_INTVECTOR_153 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3853. INTVECTOR_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.488 VIM_INTVECTOR_154 Register (Offset = 2268h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h158

Long Description:

Return to Summary Table

Table 4-3854. Instance Table

Instance Name	Physical Address
VIM	50F0 2268h

Figure 4-1859. VIM_INTVECTOR_154 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3855. INTVECTOR_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.489 VIM_INTVECTOR_155 Register (Offset = 226Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h159

Long Description:

Return to Summary Table

Table 4-3856. Instance Table

Instance Name	Physical Address
VIM	50F0 226Ch

Figure 4-1860. VIM_INTVECTOR_155 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3857. INTVECTOR_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.490 VIM_INTVECTOR_156 Register (Offset = 2270h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h160

Long Description:

Return to Summary Table

Table 4-3858. Instance Table

Instance Name	Physical Address
VIM	50F0 2270h

Figure 4-1861. VIM_INTVECTOR_156 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3859. INTVECTOR_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.491 VIM_INTVECTOR_157 Register (Offset = 2274h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h161

Long Description:

Return to Summary Table

Table 4-3860. Instance Table

Instance Name	Physical Address
VIM	50F0 2274h

Figure 4-1862. VIM_INTVECTOR_157 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3861. INTVECTOR_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.492 VIM_INTVECTOR_158 Register (Offset = 2278h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h162

Long Description:

Return to Summary Table

Table 4-3862. Instance Table

Instance Name	Physical Address
VIM	50F0 2278h

Figure 4-1863. VIM_INTVECTOR_158 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3863. INTVECTOR_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.493 VIM_INTVECTOR_159 Register (Offset = 227Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h163

Long Description:

Return to Summary Table

Table 4-3864. Instance Table

Instance Name	Physical Address
VIM	50F0 227Ch

Figure 4-1864. VIM_INTVECTOR_159 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3865. INTVECTOR_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.494 VIM_INTVECTOR_160 Register (Offset = 2280h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h164

Long Description:

Return to Summary Table

Table 4-3866. Instance Table

Instance Name	Physical Address
VIM	50F0 2280h

Figure 4-1865. VIM_INTVECTOR_160 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3867. INTVECTOR_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.495 VIM_INTVECTOR_161 Register (Offset = 2284h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h165

Long Description:

Return to Summary Table

Table 4-3868. Instance Table

Instance Name	Physical Address
VIM	50F0 2284h

Figure 4-1866. VIM_INTVECTOR_161 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3869. INTVECTOR_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.496 VIM_INTVECTOR_162 Register (Offset = 2288h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h166

Long Description:

Return to Summary Table

Table 4-3870. Instance Table

Instance Name	Physical Address
VIM	50F0 2288h

Figure 4-1867. VIM_INTVECTOR_162 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3871. INTVECTOR_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.497 VIM_INTVECTOR_163 Register (Offset = 228Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h167

Long Description:

Return to Summary Table

Table 4-3872. Instance Table

Instance Name	Physical Address
VIM	50F0 228Ch

Figure 4-1868. VIM_INTVECTOR_163 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3873. INTVECTOR_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.498 VIM_INTVECTOR_164 Register (Offset = 2290h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h168

Long Description:

Return to Summary Table

Table 4-3874. Instance Table

Instance Name	Physical Address
VIM	50F0 2290h

Figure 4-1869. VIM_INTVECTOR_164 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3875. INTVECTOR_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.499 VIM_INTVECTOR_165 Register (Offset = 2294h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h169

Long Description:

Return to Summary Table

Table 4-3876. Instance Table

Instance Name	Physical Address
VIM	50F0 2294h

Figure 4-1870. VIM_INTVECTOR_165 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3877. INTVECTOR_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.500 VIM_INTVECTOR_166 Register (Offset = 2298h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h170

Long Description:

Return to Summary Table

Table 4-3878. Instance Table

Instance Name	Physical Address
VIM	50F0 2298h

Figure 4-1871. VIM_INTVECTOR_166 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3879. INTVECTOR_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.501 VIM_INTVECTOR_167 Register (Offset = 229Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h171

Long Description:

Return to Summary Table

Table 4-3880. Instance Table

Instance Name	Physical Address
VIM	50F0 229Ch

Figure 4-1872. VIM_INTVECTOR_167 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3881. INTVECTOR_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.502 VIM_INTVECTOR_168 Register (Offset = 22A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h172

Long Description:

Return to Summary Table

Table 4-3882. Instance Table

Instance Name	Physical Address
VIM	50F0 22A0h

Figure 4-1873. VIM_INTVECTOR_168 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3883. INTVECTOR_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.503 VIM_INTVECTOR_169 Register (Offset = 22A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h173

Long Description:

Return to Summary Table

Table 4-3884. Instance Table

Instance Name	Physical Address
VIM	50F0 22A4h

Figure 4-1874. VIM_INTVECTOR_169 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3885. INTVECTOR_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.504 VIM_INTVECTOR_170 Register (Offset = 22A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h174

Long Description:

Return to Summary Table

Table 4-3886. Instance Table

Instance Name	Physical Address
VIM	50F0 22A8h

Figure 4-1875. VIM_INTVECTOR_170 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3887. INTVECTOR_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.505 VIM_INTVECTOR_171 Register (Offset = 22ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h175

Long Description:

Return to Summary Table

Table 4-3888. Instance Table

Instance Name	Physical Address
VIM	50F0 22ACh

Figure 4-1876. VIM_INTVECTOR_171 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3889. INTVECTOR_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.506 VIM_INTVECTOR_172 Register (Offset = 22B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h176

Long Description:

Return to Summary Table

Table 4-3890. Instance Table

Instance Name	Physical Address
VIM	50F0 22B0h

Figure 4-1877. VIM_INTVECTOR_172 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3891. INTVECTOR_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.507 VIM_INTVECTOR_173 Register (Offset = 22B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h177

Long Description:

Return to Summary Table

Table 4-3892. Instance Table

Instance Name	Physical Address
VIM	50F0 22B4h

Figure 4-1878. VIM_INTVECTOR_173 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3893. INTVECTOR_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.508 VIM_INTVECTOR_174 Register (Offset = 22B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h178

Long Description:

Return to Summary Table

Table 4-3894. Instance Table

Instance Name	Physical Address
VIM	50F0 22B8h

Figure 4-1879. VIM_INTVECTOR_174 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3895. INTVECTOR_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.509 VIM_INTVECTOR_175 Register (Offset = 22BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h179

Long Description:

Return to Summary Table

Table 4-3896. Instance Table

Instance Name	Physical Address
VIM	50F0 22BCh

Figure 4-1880. VIM_INTVECTOR_175 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3897. INTVECTOR_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.510 VIM_INTVECTOR_176 Register (Offset = 22C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h180

Long Description:

Return to Summary Table

Table 4-3898. Instance Table

Instance Name	Physical Address
VIM	50F0 22C0h

Figure 4-1881. VIM_INTVECTOR_176 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3899. INTVECTOR_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.511 VIM_INTVECTOR_177 Register (Offset = 22C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h181

Long Description:

Return to Summary Table

Table 4-3900. Instance Table

Instance Name	Physical Address
VIM	50F0 22C4h

Figure 4-1882. VIM_INTVECTOR_177 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3901. INTVECTOR_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.512 VIM_INTVECTOR_178 Register (Offset = 22C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h182

Long Description:

Return to Summary Table

Table 4-3902. Instance Table

Instance Name	Physical Address
VIM	50F0 22C8h

Figure 4-1883. VIM_INTVECTOR_178 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3903. INTVECTOR_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.513 VIM_INTVECTOR_179 Register (Offset = 22CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h183

Long Description:

Return to Summary Table

Table 4-3904. Instance Table

Instance Name	Physical Address
VIM	50F0 22CCh

Figure 4-1884. VIM_INTVECTOR_179 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3905. INTVECTOR_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.514 VIM_INTVECTOR_180 Register (Offset = 22D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h184

Long Description:

Return to Summary Table

Table 4-3906. Instance Table

Instance Name	Physical Address
VIM	50F0 22D0h

Figure 4-1885. VIM_INTVECTOR_180 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3907. INTVECTOR_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.515 VIM_INTVECTOR_181 Register (Offset = 22D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h185

Long Description:

Return to Summary Table

Table 4-3908. Instance Table

Instance Name	Physical Address
VIM	50F0 22D4h

Figure 4-1886. VIM_INTVECTOR_181 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3909. INTVECTOR_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.516 VIM_INTVECTOR_182 Register (Offset = 22D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h186

Long Description:

Return to Summary Table

Table 4-3910. Instance Table

Instance Name	Physical Address
VIM	50F0 22D8h

Figure 4-1887. VIM_INTVECTOR_182 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3911. INTVECTOR_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.517 VIM_INTVECTOR_183 Register (Offset = 22DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h187

Long Description:

Return to Summary Table

Table 4-3912. Instance Table

Instance Name	Physical Address
VIM	50F0 22DCh

Figure 4-1888. VIM_INTVECTOR_183 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3913. INTVECTOR_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.518 VIM_INTVECTOR_184 Register (Offset = 22E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h188

Long Description:

Return to Summary Table

Table 4-3914. Instance Table

Instance Name	Physical Address
VIM	50F0 22E0h

Figure 4-1889. VIM_INTVECTOR_184 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3915. INTVECTOR_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.519 VIM_INTVECTOR_185 Register (Offset = 22E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h189

Long Description:

Return to Summary Table

Table 4-3916. Instance Table

Instance Name	Physical Address
VIM	50F0 22E4h

Figure 4-1890. VIM_INTVECTOR_185 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3917. INTVECTOR_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.520 VIM_INTVECTOR_186 Register (Offset = 22E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h190

Long Description:

Return to Summary Table

Table 4-3918. Instance Table

Instance Name	Physical Address
VIM	50F0 22E8h

Figure 4-1891. VIM_INTVECTOR_186 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3919. INTVECTOR_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.521 VIM_INTVECTOR_187 Register (Offset = 22ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h191

Long Description:

Return to Summary Table

Table 4-3920. Instance Table

Instance Name	Physical Address
VIM	50F0 22ECh

Figure 4-1892. VIM_INTVECTOR_187 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3921. INTVECTOR_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.522 VIM_INTVECTOR_188 Register (Offset = 22F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h192

Long Description:

Return to Summary Table

Table 4-3922. Instance Table

Instance Name	Physical Address
VIM	50F0 22F0h

Figure 4-1893. VIM_INTVECTOR_188 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3923. INTVECTOR_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.523 VIM_INTVECTOR_189 Register (Offset = 22F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h193

Long Description:

Return to Summary Table

Table 4-3924. Instance Table

Instance Name	Physical Address
VIM	50F0 22F4h

Figure 4-1894. VIM_INTVECTOR_189 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3925. INTVECTOR_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.524 VIM_INTVECTOR_190 Register (Offset = 22F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h194

Long Description:

Return to Summary Table

Table 4-3926. Instance Table

Instance Name	Physical Address
VIM	50F0 22F8h

Figure 4-1895. VIM_INTVECTOR_190 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3927. INTVECTOR_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.525 VIM_INTVECTOR_191 Register (Offset = 22FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h195

Long Description:

Return to Summary Table

Table 4-3928. Instance Table

Instance Name	Physical Address
VIM	50F0 22FCh

Figure 4-1896. VIM_INTVECTOR_191 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3929. INTVECTOR_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.526 VIM_INTVECTOR_192 Register (Offset = 2300h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h196

Long Description:

Return to Summary Table

Table 4-3930. Instance Table

Instance Name	Physical Address
VIM	50F0 2300h

Figure 4-1897. VIM_INTVECTOR_192 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3931. INTVECTOR_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.527 VIM_INTVECTOR_193 Register (Offset = 2304h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h197

Long Description:

Return to Summary Table

Table 4-3932. Instance Table

Instance Name	Physical Address
VIM	50F0 2304h

Figure 4-1898. VIM_INTVECTOR_193 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3933. INTVECTOR_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.528 VIM_INTVECTOR_194 Register (Offset = 2308h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h198

Long Description:

Return to Summary Table

Table 4-3934. Instance Table

Instance Name	Physical Address
VIM	50F0 2308h

Figure 4-1899. VIM_INTVECTOR_194 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3935. INTVECTOR_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.529 VIM_INTVECTOR_195 Register (Offset = 230Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h199

Long Description:

Return to Summary Table

Table 4-3936. Instance Table

Instance Name	Physical Address
VIM	50F0 230Ch

Figure 4-1900. VIM_INTVECTOR_195 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3937. INTVECTOR_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.530 VIM_INTVECTOR_196 Register (Offset = 2310h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h200

Long Description:

Return to Summary Table

Table 4-3938. Instance Table

Instance Name	Physical Address
VIM	50F0 2310h

Figure 4-1901. VIM_INTVECTOR_196 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3939. INTVECTOR_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.531 VIM_INTVECTOR_197 Register (Offset = 2314h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h201

Long Description:

Return to Summary Table

Table 4-3940. Instance Table

Instance Name	Physical Address
VIM	50F0 2314h

Figure 4-1902. VIM_INTVECTOR_197 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3941. INTVECTOR_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.532 VIM_INTVECTOR_198 Register (Offset = 2318h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h202

Long Description:

Return to Summary Table

Table 4-3942. Instance Table

Instance Name	Physical Address
VIM	50F0 2318h

Figure 4-1903. VIM_INTVECTOR_198 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3943. INTVECTOR_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.533 VIM_INTVECTOR_199 Register (Offset = 231Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h203

Long Description:

Return to Summary Table

Table 4-3944. Instance Table

Instance Name	Physical Address
VIM	50F0 231Ch

Figure 4-1904. VIM_INTVECTOR_199 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3945. INTVECTOR_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.534 VIM_INTVECTOR_200 Register (Offset = 2320h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h204

Long Description:

Return to Summary Table

Table 4-3946. Instance Table

Instance Name	Physical Address
VIM	50F0 2320h

Figure 4-1905. VIM_INTVECTOR_200 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3947. INTVECTOR_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.535 VIM_INTVECTOR_201 Register (Offset = 2324h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h205

Long Description:

Return to Summary Table

Table 4-3948. Instance Table

Instance Name	Physical Address
VIM	50F0 2324h

Figure 4-1906. VIM_INTVECTOR_201 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3949. INTVECTOR_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.536 VIM_INTVECTOR_202 Register (Offset = 2328h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h206

Long Description:

Return to Summary Table

Table 4-3950. Instance Table

Instance Name	Physical Address
VIM	50F0 2328h

Figure 4-1907. VIM_INTVECTOR_202 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3951. INTVECTOR_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.537 VIM_INTVECTOR_203 Register (Offset = 232Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h207

Long Description:

Return to Summary Table

Table 4-3952. Instance Table

Instance Name	Physical Address
VIM	50F0 232Ch

Figure 4-1908. VIM_INTVECTOR_203 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3953. INTVECTOR_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.538 VIM_INTVECTOR_204 Register (Offset = 2330h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h208

Long Description:

Return to Summary Table

Table 4-3954. Instance Table

Instance Name	Physical Address
VIM	50F0 2330h

Figure 4-1909. VIM_INTVECTOR_204 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3955. INTVECTOR_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.539 VIM_INTVECTOR_205 Register (Offset = 2334h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h209

Long Description:

Return to Summary Table

Table 4-3956. Instance Table

Instance Name	Physical Address
VIM	50F0 2334h

Figure 4-1910. VIM_INTVECTOR_205 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3957. INTVECTOR_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.540 VIM_INTVECTOR_206 Register (Offset = 2338h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h210

Long Description:

Return to Summary Table

Table 4-3958. Instance Table

Instance Name	Physical Address
VIM	50F0 2338h

Figure 4-1911. VIM_INTVECTOR_206 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3959. INTVECTOR_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.541 VIM_INTVECTOR_207 Register (Offset = 233Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h211

Long Description:

Return to Summary Table

Table 4-3960. Instance Table

Instance Name	Physical Address
VIM	50F0 233Ch

Figure 4-1912. VIM_INTVECTOR_207 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3961. INTVECTOR_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.542 VIM_INTVECTOR_208 Register (Offset = 2340h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h212

Long Description:

Return to Summary Table

Table 4-3962. Instance Table

Instance Name	Physical Address
VIM	50F0 2340h

Figure 4-1913. VIM_INTVECTOR_208 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3963. INTVECTOR_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.543 VIM_INTVECTOR_209 Register (Offset = 2344h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h213

Long Description:

Return to Summary Table

Table 4-3964. Instance Table

Instance Name	Physical Address
VIM	50F0 2344h

Figure 4-1914. VIM_INTVECTOR_209 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3965. INTVECTOR_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.544 VIM_INTVECTOR_210 Register (Offset = 2348h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h214

Long Description:

Return to Summary Table

Table 4-3966. Instance Table

Instance Name	Physical Address
VIM	50F0 2348h

Figure 4-1915. VIM_INTVECTOR_210 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3967. INTVECTOR_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.545 VIM_INTVECTOR_211 Register (Offset = 234Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h215

Long Description:

Return to Summary Table

Table 4-3968. Instance Table

Instance Name	Physical Address
VIM	50F0 234Ch

Figure 4-1916. VIM_INTVECTOR_211 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3969. INTVECTOR_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.546 VIM_INTVECTOR_212 Register (Offset = 2350h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h216

Long Description:

Return to Summary Table

Table 4-3970. Instance Table

Instance Name	Physical Address
VIM	50F0 2350h

Figure 4-1917. VIM_INTVECTOR_212 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3971. INTVECTOR_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.547 VIM_INTVECTOR_213 Register (Offset = 2354h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h217

Long Description:

Return to Summary Table

Table 4-3972. Instance Table

Instance Name	Physical Address
VIM	50F0 2354h

Figure 4-1918. VIM_INTVECTOR_213 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3973. INTVECTOR_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.548 VIM_INTVECTOR_214 Register (Offset = 2358h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h218

Long Description:

Return to Summary Table

Table 4-3974. Instance Table

Instance Name	Physical Address
VIM	50F0 2358h

Figure 4-1919. VIM_INTVECTOR_214 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3975. INTVECTOR_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.549 VIM_INTVECTOR_215 Register (Offset = 235Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h219

Long Description:

Return to Summary Table

Table 4-3976. Instance Table

Instance Name	Physical Address
VIM	50F0 235Ch

Figure 4-1920. VIM_INTVECTOR_215 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3977. INTVECTOR_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.550 VIM_INTVECTOR_216 Register (Offset = 2360h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h220

Long Description:

Return to Summary Table

Table 4-3978. Instance Table

Instance Name	Physical Address
VIM	50F0 2360h

Figure 4-1921. VIM_INTVECTOR_216 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3979. INTVECTOR_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.551 VIM_INTVECTOR_217 Register (Offset = 2364h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h221

Long Description:

Return to Summary Table

Table 4-3980. Instance Table

Instance Name	Physical Address
VIM	50F0 2364h

Figure 4-1922. VIM_INTVECTOR_217 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3981. INTVECTOR_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.552 VIM_INTVECTOR_218 Register (Offset = 2368h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h222

Long Description:

Return to Summary Table

Table 4-3982. Instance Table

Instance Name	Physical Address
VIM	50F0 2368h

Figure 4-1923. VIM_INTVECTOR_218 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3983. INTVECTOR_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.553 VIM_INTVECTOR_219 Register (Offset = 236Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h223

Long Description:

Return to Summary Table

Table 4-3984. Instance Table

Instance Name	Physical Address
VIM	50F0 236Ch

Figure 4-1924. VIM_INTVECTOR_219 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3985. INTVECTOR_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.554 VIM_INTVECTOR_220 Register (Offset = 2370h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h224

Long Description:

Return to Summary Table

Table 4-3986. Instance Table

Instance Name	Physical Address
VIM	50F0 2370h

Figure 4-1925. VIM_INTVECTOR_220 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3987. INTVECTOR_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.555 VIM_INTVECTOR_221 Register (Offset = 2374h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h225

Long Description:

Return to Summary Table

Table 4-3988. Instance Table

Instance Name	Physical Address
VIM	50F0 2374h

Figure 4-1926. VIM_INTVECTOR_221 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3989. INTVECTOR_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.556 VIM_INTVECTOR_222 Register (Offset = 2378h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h226

Long Description:

Return to Summary Table

Table 4-3990. Instance Table

Instance Name	Physical Address
VIM	50F0 2378h

Figure 4-1927. VIM_INTVECTOR_222 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3991. INTVECTOR_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.557 VIM_INTVECTOR_223 Register (Offset = 237Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h227

Long Description:

Return to Summary Table

Table 4-3992. Instance Table

Instance Name	Physical Address
VIM	50F0 237Ch

Figure 4-1928. VIM_INTVECTOR_223 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3993. INTVECTOR_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.558 VIM_INTVECTOR_224 Register (Offset = 2380h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h228

Long Description:

Return to Summary Table

Table 4-3994. Instance Table

Instance Name	Physical Address
VIM	50F0 2380h

Figure 4-1929. VIM_INTVECTOR_224 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3995. INTVECTOR_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.559 VIM_INTVECTOR_225 Register (Offset = 2384h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h229

Long Description:

Return to Summary Table

Table 4-3996. Instance Table

Instance Name	Physical Address
VIM	50F0 2384h

Figure 4-1930. VIM_INTVECTOR_225 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3997. INTVECTOR_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.560 VIM_INTVECTOR_226 Register (Offset = 2388h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h230

Long Description:

Return to Summary Table

Table 4-3998. Instance Table

Instance Name	Physical Address
VIM	50F0 2388h

Figure 4-1931. VIM_INTVECTOR_226 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-3999. INTVECTOR_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.561 VIM_INTVECTOR_227 Register (Offset = 238Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h231

Long Description:

Return to Summary Table

Table 4-4000. Instance Table

Instance Name	Physical Address
VIM	50F0 238Ch

Figure 4-1932. VIM_INTVECTOR_227 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4001. INTVECTOR_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.562 VIM_INTVECTOR_228 Register (Offset = 2390h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h232

Long Description:

Return to Summary Table

Table 4-4002. Instance Table

Instance Name	Physical Address
VIM	50F0 2390h

Figure 4-1933. VIM_INTVECTOR_228 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4003. INTVECTOR_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.563 VIM_INTVECTOR_229 Register (Offset = 2394h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h233

Long Description:

Return to Summary Table

Table 4-4004. Instance Table

Instance Name	Physical Address
VIM	50F0 2394h

Figure 4-1934. VIM_INTVECTOR_229 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4005. INTVECTOR_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.564 VIM_INTVECTOR_230 Register (Offset = 2398h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h234

Long Description:

Return to Summary Table

Table 4-4006. Instance Table

Instance Name	Physical Address
VIM	50F0 2398h

Figure 4-1935. VIM_INTVECTOR_230 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4007. INTVECTOR_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.565 VIM_INTVECTOR_231 Register (Offset = 239Ch) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h235

Long Description:

Return to Summary Table

Table 4-4008. Instance Table

Instance Name	Physical Address
VIM	50F0 239Ch

Figure 4-1936. VIM_INTVECTOR_231 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4009. INTVECTOR_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.566 VIM_INTVECTOR_232 Register (Offset = 23A0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h236

Long Description:

Return to Summary Table

Table 4-4010. Instance Table

Instance Name	Physical Address
VIM	50F0 23A0h

Figure 4-1937. VIM_INTVECTOR_232 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4011. INTVECTOR_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.567 VIM_INTVECTOR_233 Register (Offset = 23A4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h237

Long Description:

Return to Summary Table

Table 4-4012. Instance Table

Instance Name	Physical Address
VIM	50F0 23A4h

Figure 4-1938. VIM_INTVECTOR_233 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4013. INTVECTOR_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.568 VIM_INTVECTOR_234 Register (Offset = 23A8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h238

Long Description:

Return to Summary Table

Table 4-4014. Instance Table

Instance Name	Physical Address
VIM	50F0 23A8h

Figure 4-1939. VIM_INTVECTOR_234 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4015. INTVECTOR_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.569 VIM_INTVECTOR_235 Register (Offset = 23ACh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h239

Long Description:

Return to Summary Table

Table 4-4016. Instance Table

Instance Name	Physical Address
VIM	50F0 23ACh

Figure 4-1940. VIM_INTVECTOR_235 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4017. INTVECTOR_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.570 VIM_INTVECTOR_236 Register (Offset = 23B0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h240

Long Description:

Return to Summary Table

Table 4-4018. Instance Table

Instance Name	Physical Address
VIM	50F0 23B0h

Figure 4-1941. VIM_INTVECTOR_236 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4019. INTVECTOR_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.571 VIM_INTVECTOR_237 Register (Offset = 23B4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h241

Long Description:

Return to Summary Table

Table 4-4020. Instance Table

Instance Name	Physical Address
VIM	50F0 23B4h

Figure 4-1942. VIM_INTVECTOR_237 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4021. INTVECTOR_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.572 VIM_INTVECTOR_238 Register (Offset = 23B8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h242

Long Description:

Return to Summary Table

Table 4-4022. Instance Table

Instance Name	Physical Address
VIM	50F0 23B8h

Figure 4-1943. VIM_INTVECTOR_238 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4023. INTVECTOR_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.573 VIM_INTVECTOR_239 Register (Offset = 23BCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h243

Long Description:

Return to Summary Table

Table 4-4024. Instance Table

Instance Name	Physical Address
VIM	50F0 23BCh

Figure 4-1944. VIM_INTVECTOR_239 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4025. INTVECTOR_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.574 VIM_INTVECTOR_240 Register (Offset = 23C0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h244

Long Description:

Return to Summary Table

Table 4-4026. Instance Table

Instance Name	Physical Address
VIM	50F0 23C0h

Figure 4-1945. VIM_INTVECTOR_240 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4027. INTVECTOR_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.575 VIM_INTVECTOR_241 Register (Offset = 23C4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h245

Long Description:

Return to Summary Table

Table 4-4028. Instance Table

Instance Name	Physical Address
VIM	50F0 23C4h

Figure 4-1946. VIM_INTVECTOR_241 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4029. INTVECTOR_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.576 VIM_INTVECTOR_242 Register (Offset = 23C8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h246

Long Description:

Return to Summary Table

Table 4-4030. Instance Table

Instance Name	Physical Address
VIM	50F0 23C8h

Figure 4-1947. VIM_INTVECTOR_242 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4031. INTVECTOR_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.577 VIM_INTVECTOR_243 Register (Offset = 23CCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h247

Long Description:

Return to Summary Table

Table 4-4032. Instance Table

Instance Name	Physical Address
VIM	50F0 23CCh

Figure 4-1948. VIM_INTVECTOR_243 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4033. INTVECTOR_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.578 VIM_INTVECTOR_244 Register (Offset = 23D0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h248

Long Description:

Return to Summary Table

Table 4-4034. Instance Table

Instance Name	Physical Address
VIM	50F0 23D0h

Figure 4-1949. VIM_INTVECTOR_244 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4035. INTVECTOR_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.579 VIM_INTVECTOR_245 Register (Offset = 23D4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h249

Long Description:

Return to Summary Table

Table 4-4036. Instance Table

Instance Name	Physical Address
VIM	50F0 23D4h

Figure 4-1950. VIM_INTVECTOR_245 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4037. INTVECTOR_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.580 VIM_INTVECTOR_246 Register (Offset = 23D8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h250

Long Description:

Return to Summary Table

Table 4-4038. Instance Table

Instance Name	Physical Address
VIM	50F0 23D8h

Figure 4-1951. VIM_INTVECTOR_246 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4039. INTVECTOR_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.581 VIM_INTVECTOR_247 Register (Offset = 23DCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h251

Long Description:

Return to Summary Table

Table 4-4040. Instance Table

Instance Name	Physical Address
VIM	50F0 23DCh

Figure 4-1952. VIM_INTVECTOR_247 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4041. INTVECTOR_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.582 VIM_INTVECTOR_248 Register (Offset = 23E0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h252

Long Description:

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Table 4-4042. Instance Table

Instance Name	Physical Address
VIM	50F0 23E0h

Figure 4-1953. VIM_INTVECTOR_248 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4043. INTVECTOR_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.583 VIM_INTVECTOR_249 Register (Offset = 23E4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h253

Long Description:

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Table 4-4044. Instance Table

Instance Name	Physical Address
VIM	50F0 23E4h

Figure 4-1954. VIM_INTVECTOR_249 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4045. INTVECTOR_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.584 VIM_INTVECTOR_250 Register (Offset = 23E8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h254

Long Description:

Return to Summary Table

Table 4-4046. Instance Table

Instance Name	Physical Address
VIM	50F0 23E8h

Figure 4-1955. VIM_INTVECTOR_250 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4047. INTVECTOR_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.585 VIM_INTVECTOR_251 Register (Offset = 23ECh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h255

Long Description:

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Table 4-4048. Instance Table

Instance Name	Physical Address
VIM	50F0 23ECh

Figure 4-1956. VIM_INTVECTOR_251 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4049. INTVECTOR_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.586 VIM_INTVECTOR_252 Register (Offset = 23F0h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h256

Long Description:

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Table 4-4050. Instance Table

Instance Name	Physical Address
VIM	50F0 23F0h

Figure 4-1957. VIM_INTVECTOR_252 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4051. INTVECTOR_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.587 VIM_INTVECTOR_253 Register (Offset = 23F4h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h257

Long Description:

Return to Summary Table

Table 4-4052. Instance Table

Instance Name	Physical Address
VIM	50F0 23F4h

Figure 4-1958. VIM_INTVECTOR_253 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4053. INTVECTOR_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.588 VIM_INTVECTOR_254 Register (Offset = 23F8h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h258

Long Description:

Return to Summary Table

Table 4-4054. Instance Table

Instance Name	Physical Address
VIM	50F0 23F8h

Figure 4-1959. VIM_INTVECTOR_254 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4055. INTVECTOR_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.30.589 VIM_INTVECTOR_255 Register (Offset = 23FCh) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32) h2000 + Q x h259

Long Description:

Return to Summary Table

Table 4-4056. Instance Table

Instance Name	Physical Address
VIM	50F0 23FCh

Figure 4-1960. VIM_INTVECTOR_255 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR														RES20	
RW														RO	
0														0	

Access Types Legend

Table 4-4057. INTVECTOR_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

Table 4-4058. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.31 SOC_TSXBAR_INTR Registers

Table 4-4059. SOC_TIMESYNC_XBAR1, SOC_TIMESYNC_XBAR1_SOC_TIMESYNC_XBAR Registers, Base Address=52E0 4000H, Length=1

Offset	Length	Acronym	Register Name	SOC_TIMESYNC_XBAR1 Physical Address
0h	32	SOC_TIMESYNC_XBAR1_PID	Identification register	52E0 4000h
4h	16	SOC_TIMESYNC_XBAR1_MUXCNTL	Interrupt mux control register	52E0 4004h

4.31.1 SOC_TIMESYNC_XBAR1_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

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Table 4-4060. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4000h

Figure 4-1961. SOC_TIMESYNC_XBAR1_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
RO		RO		RO											
1		10		11010010100											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
RO					RO			RO		RO					
10000					1			0		0					

Access Types Legend

Table 4-4061. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	Ah	bu
27 - 16	FUNCTION	RO	2903F6BF4h	function
15 - 11	RTLVER	RO	2710h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

4.31.2 SOC_TIMESYNC_XBAR1_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-4062. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4004h

Figure 4-1962. SOC_TIMESYNC_XBAR1_MUXCNTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0							
7	6	5	4	3	2	1	0
RESERVED				ENABLE			
NONE				RW			
0				0			

Access Types Legend

Table 4-4063. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
3 - 0	ENABLE	RW	0h	Mux control for interrupt N

Table 4-4064. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined

4.32 TOP_ESM Registers

Table 4-4065. TOP_ESM, TOP_ESM_TOP_ESM Registers, Base Address=52D0 0000H, Length=1

Offset	Length	Acronym	Register Name	TOP_ESM Physical Address
0h	32	TOP_ESM_PID	The Revision Register contains the major and minor revisions for the module.	52D0 0000h
4h	32	TOP_ESM_INFO	The Info Register gives the configuration Inforrmation of this ESM.	52D0 0004h
8h	8	TOP_ESM_EN	The Global Enable Register has the master interrupt mask	52D0 0008h
Ch	8	TOP_ESM_SFT_RST	The Global Soft Reset Register controls the global clear for raw status and enables	52D0 000Ch
10h	8	TOP_ESM_ERR_RAW	Raw Status/Set Register for Configuration Errors	52D0 0010h
14h	8	TOP_ESM_ERR_STS	Config Error Enable and Clear Register	52D0 0014h
18h	8	TOP_ESM_ERR_EN_SET	Config Error Enable Set Register	52D0 0018h
1Ch	8	TOP_ESM_ERR_EN_CLR	Config Error Interrupt Enabled Clear register	52D0 001Ch
20h	32	TOP_ESM_LOW_PRI	Shows which is the highest priority outstanding low priority interrupt	52D0 0020h
24h	32	TOP_ESM_HI_PRI	Shows which is the highest priority outstanding high priority interrupt	52D0 0024h
28h	32	TOP_ESM_LOW	Shows which groups have oustanding low priority interrupts	52D0 0028h
2Ch	32	TOP_ESM_HI	Shows which groups have oustanding high priority interrupts	52D0 002Ch
30h	16	TOP_ESM_EOI	End of Interrupt Register	52D0 0030h
40h	8	TOP_ESM_PIN_CTRL	This register controls the error_pin_n output	52D0 0040h
44h	0	TOP_ESM_PIN_STS	This register reflects the status of the error_pin_n output	52D0 0044h
48h	24	TOP_ESM_PIN_CNTR	This register shows the current value of the error pin counter	52D0 0048h
4Ch	24	TOP_ESM_PIN_CNTR_PRE	This register contains the value that is loaded in to the Error Counter	52D0 004Ch
50h	24	TOP_ESM_PWMH_PIN_CNTR	This register shows the current value of the error pin PWM high counter	52D0 0050h
54h	24	TOP_ESM_PWMH_PIN_CNTR_PRE	This register contains the value that is loaded in to the Error PWM High Counter	52D0 0054h
58h	24	TOP_ESM_PWML_PIN_CNTR	This register shows the current value of the error pin PWM low counter	52D0 0058h

Table 4-4065. TOP_ESM, TOP_ESM_TOP_ESM Registers, Base Address=52D0 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	TOP_ESM Physical Address
5Ch	24	TOP_ESM_PWML_PIN_CNTR_PRE	This register contains the value that is loaded in to the Error PWM Low Counter	52D0 005Ch

4.32.1 TOP_ESM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description:

Return to Summary Table

Table 4-4066. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0000h

Figure 4-1963. TOP_ESM_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
RO		RO		RO											
1		10		111111100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1001					1			0		0					

Access Types Legend

Table 4-4067. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	FUNC	RO	19DEBCD660h	Module ID
15 - 11	RTL	RO	3E9h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	0h	Minor revision

4.32.2 TOP_ESM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this ESM.

Long Description:

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Table 4-4068. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0004h

Figure 4-1964. TOP_ESM_INFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LAST_RESET	RESERVED														
RO	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PULSE_GROUPS								GROUPS							
RO								RO							
1								11							

Access Types Legend

Table 4-4069. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	RO	0h	Indicates the Source of the last Reset
	RESERVED	NONE		Reserved
15 - 8	PULSE_GROUPS	RO	1h	Number of Pulse Error Groups
7 - 0	GROUPS	RO	Bh	Total number of Error Groups

4.32.3 TOP_ESM_EN Register (Offset = 8h) [reset = h]

Short Description: The Global Enable Register has the master interrupt mask

Long Description:

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Table 4-4070. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0008h

Figure 4-1965. TOP_ESM_EN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				RW			
0				0			

Access Types Legend

Table 4-4071. EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	RW	0h	Global Enable

4.32.4 TOP_ESM_SFT_RST Register (Offset = Ch) [reset = h]

Short Description: The Global Soft Reset Register controls the global clear for raw status and enables

Long Description:

Return to Summary Table

Table 4-4072. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 000Ch

Figure 4-1966. TOP_ESM_SFT_RST Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				WO			
0				0			

Access Types Legend

Table 4-4073. SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	WO	0h	Global Soft Reset

4.32.5 TOP_ESM_ERR_RAW Register (Offset = 10h) [reset = h]

Short Description: Raw Status/Set Register for Configuration Errors

Long Description:

Return to Summary Table

Table 4-4074. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0010h

Figure 4-1967. TOP_ESM_ERR_RAW Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						STS	
NONE						RW	
0						0	

Access Types Legend

Table 4-4075. ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	STS	RW	0h	This is the raw status for config errors

4.32.6 TOP_ESM_ERR_STS Register (Offset = 14h) [reset = h]

Short Description: Config Error Enable and Clear Register

Long Description:

Return to Summary Table

Table 4-4076. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0014h

Figure 4-1968. TOP_ESM_ERR_STS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						MSK	
NONE						RW	
0						0	

Access Types Legend

Table 4-4077. ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the masked status/clear for config errors

4.32.7 TOP_ESM_ERR_EN_SET Register (Offset = 18h) [reset = h]

Short Description: Config Error Enable Set Register

Long Description:

Return to Summary Table

Table 4-4078. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0018h

Figure 4-1969. TOP_ESM_ERR_EN_SET Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						MSK	
NONE						RW	
0						0	

Access Types Legend

Table 4-4079. ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable set for config errors

4.32.8 TOP_ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = h]

Short Description: Config Error Interrupt Enabled Clear register

Long Description:

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Table 4-4080. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 001Ch

Figure 4-1970. TOP_ESM_ERR_EN_CLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						MSK	
NONE						RW	
0						0	

Access Types Legend

Table 4-4081. ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable clear for config errors

4.32.9 TOP_ESM_LOW_PRI Register (Offset = 20h) [reset = h]

Short Description: Shows which is the highest priority outstanding low priority interrupt

Long Description:

Return to Summary Table

Table 4-4082. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0020h

Figure 4-1971. TOP_ESM_LOW_PRI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLS															
RO															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVL															
RO															
1111111111111111															

Access Types Legend

Table 4-4083. LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	3F28CB715 71C7h	This is the highest priority outstanding low priority pulse interrupt
15 - 0	LVL	RO	3F28CB715 71C7h	This is the highest priority outstanding low priority level interrupt

4.32.10 TOP_ESM_HI_PRI Register (Offset = 24h) [reset = h]

Short Description: Shows which is the highest priority outstanding high priority interrupt

Long Description:

Return to Summary Table

Table 4-4084. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0024h

Figure 4-1972. TOP_ESM_HI_PRI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLS															
RO															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVL															
RO															
1111111111111111															

Access Types Legend

Table 4-4085. HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	3F28CB715 71C7h	This is the highest priority outstanding high priority pulse interrupt
15 - 0	LVL	RO	3F28CB715 71C7h	This is the highest priority outstanding high priority level interrupt

4.32.11 TOP_ESM_LOW Register (Offset = 28h) [reset = h]

Short Description: Shows which groups have oustanding low priority interrupts

Long Description:

Return to Summary Table

Table 4-4086. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0028h

Figure 4-1973. TOP_ESM_LOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-4087. LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

4.32.12 TOP_ESM_HI Register (Offset = 2Ch) [reset = h]

Short Description: Shows which groups have oustanding high priority interrupts

Long Description:

Return to Summary Table

Table 4-4088. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 002Ch

Figure 4-1974. TOP_ESM_HI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS															
RO															
0															

Access Types Legend

Table 4-4089. HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

4.32.13 TOP_ESM_EOI Register (Offset = 30h) [reset = h]

Short Description: End of Interrupt Register

Long Description:

Return to Summary Table

Table 4-4090. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0030h

Figure 4-1975. TOP_ESM_EOI Name Register

15	14	13	12	11	10	9	8
RESERVED					KEY		
NONE					WO		
0					0		
7	6	5	4	3	2	1	0
KEY							
WO							
0							

Access Types Legend

Table 4-4091. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	KEY	WO	0h	This is the interrupt being serviced

4.32.14 TOP_ESM_PIN_CTRL Register (Offset = 40h) [reset = h]

Short Description: This register controls the error_pin_n output

Long Description:

Return to Summary Table

Table 4-4092. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0040h

Figure 4-1976. TOP_ESM_PIN_CTRL Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
PWM_EN				KEY			
RW				RW			
0				0			

Access Types Legend

Table 4-4093. PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	PWM_EN	RW	0h	PWM enable
3 - 0	KEY	RW	0h	Pin Control Key

4.32.15 TOP_ESM_PIN_STS Register (Offset = 44h) [reset = h]

Short Description: This register reflects the status of the error_pin_n output

Long Description:

Return to Summary Table

Table 4-4094. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0044h

Figure 4-1977. TOP_ESM_PIN_STS Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
VAL							
RO							
0							

Access Types Legend

Table 4-4095. PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	VAL	RO	0h	Value of the error_pin_n

4.32.16 TOP_ESM_PIN_CNTR Register (Offset = 48h) [reset = h]

Short Description: This register shows the current value of the error pin counter

Long Description:

Return to Summary Table

Table 4-4096. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0048h

Figure 4-1978. TOP_ESM_PIN_CNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RO															
0															

Access Types Legend

Table 4-4097. PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.32.17 TOP_ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error Counter

Long Description:

Return to Summary Table

Table 4-4098. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 004Ch

Figure 4-1979. TOP_ESM_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RW															
0															

Access Types Legend

Table 4-4099. PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.32.18 TOP_ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = h]

Short Description: This register shows the current value of the error pin PWM high counter

Long Description:

Return to Summary Table

Table 4-4100. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0050h

Figure 4-1980. TOP_ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RO															
0															

Access Types Legend

Table 4-4101. PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.32.19 TOP_ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM High Counter

Long Description:

Return to Summary Table

Table 4-4102. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0054h

Figure 4-1981. TOP_ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RW															
0															

Access Types Legend

Table 4-4103. PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.32.20 TOP_ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = h]

Short Description: This register shows the current value of the error pin PWM low counter

Long Description:

Return to Summary Table

Table 4-4104. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0058h

Figure 4-1982. TOP_ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RO															
0															

Access Types Legend

Table 4-4105. PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

4.32.21 TOP_ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM Low Counter

Long Description:

Return to Summary Table

Table 4-4106. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 005Ch

Figure 4-1983. TOP_ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
RW															
0															

Access Types Legend

Table 4-4107. PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

Table 4-4108. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

4.33 TPCC Registers

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
0h	32	HSM_TPCC0_PID	Peripheral ID Register	4702 0000h
4h	32	HSM_TPCC0_CCCFG	CC Configuration Register	4702 0004h
200h	32	HSM_TPCC0_QCHMAPN	QDMA Channel N Mapping Register	4702 0200h
240h	32	HSM_TPCC0_DMAQNUMN	DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.	4702 0240h
260h	32	HSM_TPCC0_QDMAQNUM	QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.	4702 0260h
280h	32	HSM_TPCC0_QUETCMAP	Queue to TC Mapping	4702 0280h
284h	32	HSM_TPCC0_QUEPRI	Queue Priority	4702 0284h
300h	32	HSM_TPCC0_EMR	Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	4702 0300h
304h	32	HSM_TPCC0_EMRH	Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	4702 0304h
308h	32	HSM_TPCC0_EMCR	Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	4702 0308h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
30Ch	32	HSM_TPCC0_EMCRH	Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	4702 030Ch
310h	32	HSM_TPCC0_QEMR	QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.	4702 0310h
314h	32	HSM_TPCC0_QEMCR	QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.	4702 0314h
318h	32	HSM_TPCC0_CCERR	CC Error Register	4702 0318h
31Ch	32	HSM_TPCC0_CCERRCLR	CC Error Clear Register	4702 031Ch
320h	32	HSM_TPCC0_EEVAL	Error Eval Register	4702 0320h
340h	32	HSM_TPCC0_DRAEM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.	4702 0340h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
344h	32	HSM_TPCC0_DRAEHM	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.	4702 0344h
380h	32	HSM_TPCC0_QRAEN	QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.	4702 0380h
400h	32	HSM_TPCC0_QNE0	Event Queue Entry Diagram for Queue n - Entry 0	4702 0400h
404h	32	HSM_TPCC0_QNE1	Event Queue Entry Diagram for Queue n - Entry 1	4702 0404h
408h	32	HSM_TPCC0_QNE2	Event Queue Entry Diagram for Queue n - Entry 2	4702 0408h
40Ch	32	HSM_TPCC0_QNE3	Event Queue Entry Diagram for Queue n - Entry 3	4702 040Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
410h	32	HSM_TPCC0_QNE4	Event Queue Entry Diagram for Queue n - Entry 4	4702 0410h
414h	32	HSM_TPCC0_QNE5	Event Queue Entry Diagram for Queue n - Entry 5	4702 0414h
418h	32	HSM_TPCC0_QNE6	Event Queue Entry Diagram for Queue n - Entry 6	4702 0418h
41Ch	32	HSM_TPCC0_QNE7	Event Queue Entry Diagram for Queue n - Entry 7	4702 041Ch
420h	32	HSM_TPCC0_QNE8	Event Queue Entry Diagram for Queue n - Entry 8	4702 0420h
424h	32	HSM_TPCC0_QNE9	Event Queue Entry Diagram for Queue n - Entry 9	4702 0424h
428h	32	HSM_TPCC0_QNE10	Event Queue Entry Diagram for Queue n - Entry 0	4702 0428h
42Ch	32	HSM_TPCC0_QNE11	Event Queue Entry Diagram for Queue n - Entry 11	4702 042Ch
430h	32	HSM_TPCC0_QNE12	Event Queue Entry Diagram for Queue n - Entry 12	4702 0430h
434h	32	HSM_TPCC0_QNE13	Event Queue Entry Diagram for Queue n - Entry 13	4702 0434h
438h	32	HSM_TPCC0_QNE14	Event Queue Entry Diagram for Queue n - Entry 14	4702 0438h
43Ch	32	HSM_TPCC0_QNE15	Event Queue Entry Diagram for Queue n - Entry 15	4702 043Ch
600h	32	HSM_TPCC0_QSTATN	QSTATn Register Set	4702 0600h
620h	32	HSM_TPCC0_QWMTHRA	Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.	4702 0620h
640h	32	HSM_TPCC0_CCSTAT	CC Status Register	4702 0640h
700h	32	HSM_TPCC0_AETCTL	Advanced Event Trigger Control	4702 0700h
704h	32	HSM_TPCC0_AETSTAT	Advanced Event Trigger Stat	4702 0704h
708h	32	HSM_TPCC0_AETCMD	AET Command	4702 0708h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1000h	32	HSM_TPCC0_ER	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.	4702 1000h
1004h	32	HSM_TPCC0_ERH	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.	4702 1004h
1008h	32	HSM_TPCC0_ECR	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.	4702 1008h
100Ch	32	HSM_TPCC0_ECRH	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.	4702 100Ch
1010h	32	HSM_TPCC0_ESR	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.	4702 1010h
1014h	32	HSM_TPCC0_ESRH	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.	4702 1014h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1018h	32	HSM_TPCC0_CER	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.	4702 1018h
101Ch	32	HSM_TPCC0_CERH	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.	4702 101Ch
1020h	32	HSM_TPCC0_EER	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.	4702 1020h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1024h	32	HSM_TPCC0_EERH	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.	4702 1024h
1028h	32	HSM_TPCC0_EECR	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..	4702 1028h
102Ch	32	HSM_TPCC0_EECRH	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..	4702 102Ch
1030h	32	HSM_TPCC0_EESR	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..	4702 1030h
1034h	32	HSM_TPCC0_EESRH	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..	4702 1034h
1038h	32	HSM_TPCC0_SER	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 1038h
103Ch	32	HSM_TPCC0_SERH	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 103Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1040h	32	HSM_TPCC0_SECR	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.	4702 1040h
1044h	32	HSM_TPCC0_SECRH	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.	4702 1044h
1050h	32	HSM_TPCC0_IER	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.	4702 1050h
1054h	32	HSM_TPCC0_IERH	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.	4702 1054h
1058h	32	HSM_TPCC0_IECR	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..	4702 1058h
105Ch	32	HSM_TPCC0_IECRH	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..	4702 105Ch
1060h	32	HSM_TPCC0_IESR	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..	4702 1060h
1064h	32	HSM_TPCC0_IESRH	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..	4702 1064h
1068h	32	HSM_TPCC0_IPR	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.	4702 1068h
106Ch	32	HSM_TPCC0_IPRH	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.	4702 106Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1070h	32	HSM_TPCC0_ICR	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.	4702 1070h
1074h	32	HSM_TPCC0_ICRH	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.	4702 1074h
1078h	32	HSM_TPCC0_IEVAL	Interrupt Eval Register	4702 1078h
1080h	32	HSM_TPCC0_QER	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.	4702 1080h
1084h	32	HSM_TPCC0_QEER	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.	4702 1084h
1088h	32	HSM_TPCC0_QEECR	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..	4702 1088h
108Ch	32	HSM_TPCC0_QEESR	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..	4702 108Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
1090h	32	HSM_TPCC0_QSER	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 1090h
1094h	32	HSM_TPCC0_QSECR	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..	4702 1094h
2000h	32	HSM_TPCC0_ER_RN	Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.	4702 2000h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
2004h	32	HSM_TPCC0_ERH_RN	Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.	4702 2004h
2008h	32	HSM_TPCC0_ECR_RN	Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.	4702 2008h
200Ch	32	HSM_TPCC0_ECRH_RN	Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.	4702 200Ch
2010h	32	HSM_TPCC0_ESR_RN	Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.	4702 2010h
2014h	32	HSM_TPCC0_ESRH_RN	Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.	4702 2014h
2018h	32	HSM_TPCC0_CER_RN	Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.	4702 2018h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
201Ch	32	HSM_TPCC0_CERH_RN	Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.	4702 201Ch
2020h	32	HSM_TPCC0_EER_RN	Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.	4702 2020h

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
2024h	32	HSM_TPCC0_EERH_RN	Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.	4702 2024h
2028h	32	HSM_TPCC0_EECR_RN	Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..	4702 2028h
202Ch	32	HSM_TPCC0_EECRH_RN	Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..	4702 202Ch
2030h	32	HSM_TPCC0_EESR_RN	Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..	4702 2030h
2034h	32	HSM_TPCC0_EESRH_RN	Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..	4702 2034h
2038h	32	HSM_TPCC0_SER_RN	Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 2038h
203Ch	32	HSM_TPCC0_SERH_RN	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 203Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
2040h	32	HSM_TPCC0_SECR_RN	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.	4702 2040h
2044h	32	HSM_TPCC0_SECRH_RN	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.	4702 2044h
2050h	32	HSM_TPCC0_IER_RN	Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.	4702 2050h
2054h	32	HSM_TPCC0_IERH_RN	Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.	4702 2054h
2058h	32	HSM_TPCC0_IECR_RN	Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..	4702 2058h
205Ch	32	HSM_TPCC0_IECRH_RN	Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..	4702 205Ch
2060h	32	HSM_TPCC0_IESR_RN	Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..	4702 2060h
2064h	32	HSM_TPCC0_IESRH_RN	Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..	4702 2064h
2068h	32	HSM_TPCC0_IPR_RN	Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.	4702 2068h
206Ch	32	HSM_TPCC0_IPRH_RN	Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.	4702 206Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
2070h	32	HSM_TPCC0_ICR_RN	Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.	4702 2070h
2074h	32	HSM_TPCC0_ICRH_RN	Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.	4702 2074h
2078h	32	HSM_TPCC0_IEVAL_RN	Interrupt Eval Register	4702 2078h
2080h	32	HSM_TPCC0_QER_RN	QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.	4702 2080h
2084h	32	HSM_TPCC0_QEER_RN	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/ latched in QER.En.	4702 2084h
2088h	32	HSM_TPCC0_QEECR_RN	QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..	4702 2088h
208Ch	32	HSM_TPCC0_QEESR_RN	QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..	4702 208Ch

Table 4-4109. HSM_TPCC0, HSM_TPCC0_HSM_TPCC Registers, Base Address=4702 0000H, Length=1 (continued)

Offset	Length	Acronym	Register Name	HSM_TPCC0 Physical Address
2090h	32	HSM_TPCC0_QSER_RN	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.	4702 2090h
2094h	32	HSM_TPCC0_QSECR_RN	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..	4702 2094h
4000h	32	HSM_TPCC0_OPT	Options Parameter	4702 4000h
4004h	32	HSM_TPCC0_SRC	Source Address	4702 4004h
4008h	32	HSM_TPCC0_ABCNT	A and B byte count	4702 4008h
400Ch	32	HSM_TPCC0_DST	Destination Address	4702 400Ch
4010h	32	HSM_TPCC0_BIDX	Register description is not available	4702 4010h
4014h	32	HSM_TPCC0_LNK	Link and Reload parameters	4702 4014h
4018h	32	HSM_TPCC0_CIDX	Register description is not available	4702 4018h
401Ch	32	HSM_TPCC0_CCNT	C byte count	4702 401Ch

4.33.1 HSM_TPCC0_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

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Table 4-4110. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0000h

Figure 4-1984. HSM_TPCC0_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RES1		FUNC											
RO		RO		RO											
1		0		1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
10101					11			0		0					

Access Types Legend

Table 4-4111. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
29 - 28	RES1	RO	0h	RESERVE FIELD
27 - 16	FUNC	RO	1h	Function indicates a software compatible module family.
15 - 11	RTL	RO	2775h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	0h	Minor Revision

4.33.2 HSM_TPCC0_CCCFG Register (Offset = 4h) [reset = h]

Short Description: CC Configuration Register

Long Description:

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Table 4-4112. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0004h

Figure 4-1985. HSM_TPCC0_CCCFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES2						MPEXIST	CHMAPEXIST	RES3		NUMREGN		RES4	NUMTC		
RO						RO	RO	RO		RO		RO	RO		
0						0	0	0		10		0	1		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES5	NUMPAENTRY			RES6	NUMINTCH			RES7	NUMQDMACH			RES8	NUMDMACH		
RO	RO			RO	RO			RO	RO			RO	RO		
0	11			0	100			0	100			0	101		

Access Types Legend

Table 4-4113. CCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RES2	RO	0h	RESERVE FIELD
25	MPEXIST	RO	0h	Memory Protection Existence MPEXIST = 0 : No memory protection. MPEXIST = 1 : Memory Protection logic included.
24	CHMAPEXIST	RO	0h	Channel Mapping Existence CHMAPEXIST = 0 : No Channel mapping. CHMAPEXIST = 1 : Channel mapping logic included.
23 - 22	RES3	RO	0h	RESERVE FIELD
21 - 20	NUMREGN	RO	Ah	Number of MP and Shadow regions
19	RES4	RO	0h	RESERVE FIELD
18 - 16	NUMTC	RO	1h	Number of Queues/Number of TCs
15	RES5	RO	0h	RESERVE FIELD
14 - 12	NUMPAENTRY	RO	Bh	Number of PaRAM entries
11	RES6	RO	0h	RESERVE FIELD
10 - 8	NUMINTCH	RO	64h	Number of Interrupt Channels
7	RES7	RO	0h	RESERVE FIELD
6 - 4	NUMQDMACH	RO	64h	Number of QDMA Channels
3	RES8	RO	0h	RESERVE FIELD
2 - 0	NUMDMACH	RO	65h	Number of DMA Channels

4.33.3 HSM_TPCC0_QCHMAPN Register (Offset = 200h) [reset = h]

Short Description: QDMA Channel N Mapping Register

Long Description:

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Table 4-4114. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0200h

Figure 4-1986. HSM_TPCC0_QCHMAPN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10		PAENTRY									TRWORD			RESERVED	
RO		RW									RW			NONE	
0		0									0			0	

Access Types Legend

Table 4-4115. QCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 14	RES10	RO	0h	RESERVE FIELD
13 - 5	PAENTRY	RW	0h	PaRAM Entry number for QDMA Channel N.
4 - 2	TRWORD	RW	0h	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized.
	RESERVED	NONE		Reserved

4.33.4 HSM_TPCC0_DMAQNUMN Register (Offset = 240h) [reset = h]

Short Description: DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

Long Description:

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Table 4-4116. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0240h

Figure 4-1987. HSM_TPCC0_DMAQNUMN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11		E7		RES12		E6		RES13		E5		RES14		E4	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15		E3		RES16		E2		RES17		E1		RES18		E0	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-4117. DMAQNUMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES11	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	DMA Queue Number for event #7
27	RES12	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	DMA Queue Number for event #6
23	RES13	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	DMA Queue Number for event #5
19	RES14	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	DMA Queue Number for event #4
15	RES15	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	DMA Queue Number for event #3
11	RES16	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	DMA Queue Number for event #2
7	RES17	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	DMA Queue Number for event #1
3	RES18	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	DMA Queue Number for event #0

4.33.5 HSM_TPCC0_QDMAQNUM Register (Offset = 260h) [reset = h]

Short Description: QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

Long Description:

Return to Summary Table

Table 4-4118. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0260h

Figure 4-1988. HSM_TPCC0_QDMAQNUM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES19		E7		RES20		E6		RES21		E5		RES22		E4	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES23		E3		RES24		E2		RES25		E1		RES26		E0	
RO		RW		RO		RW		RO		RW		RO		RW	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-4119. QDMAQNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES19	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	QDMA Queue Number for event #7
27	RES20	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	QDMA Queue Number for event #6
23	RES21	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	QDMA Queue Number for event #5
19	RES22	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	QDMA Queue Number for event #4
15	RES23	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	QDMA Queue Number for event #3
11	RES24	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	QDMA Queue Number for event #2
7	RES25	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	QDMA Queue Number for event #1
3	RES26	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	QDMA Queue Number for event #0

4.33.6 HSM_TPCC0_QUETCMAP Register (Offset = 280h) [reset = h]

Short Description: Queue to TC Mapping

Long Description:

Return to Summary Table

Table 4-4120. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0280h

Figure 4-1989. HSM_TPCC0_QUETCMAP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES27															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES27									TCNUMQ1			RES28	TCNUMQ0		
RO									RW			RO	RW		
0									1			0	0		

Access Types Legend

Table 4-4121. QUETCMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES27	RO	0h	RESERVE FIELD
6 - 4	TCNUMQ1	RW	1h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.
3	RES28	RO	0h	RESERVE FIELD
2 - 0	TCNUMQ0	RW	0h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.

4.33.7 HSM_TPCC0_QUEPRI Register (Offset = 284h) [reset = h]

Short Description: Queue Priority

Long Description:

Return to Summary Table

Table 4-4122. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0284h

Figure 4-1990. HSM_TPCC0_QUEPRI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES29									PRIQ1			RES30	PRIQ0		
RO									RW			RO	RW		
0									0			0	0		

Access Types Legend

Table 4-4123. QUEPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES29	RO	0h	RESERVE FIELD
6 - 4	PRIQ1	RW	0h	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.
3	RES30	RO	0h	RESERVE FIELD
2 - 0	PRIQ0	RW	0h	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.

4.33.8 HSM_TPCC0_EMR Register (Offset = 300h) [reset = h]

Short Description: Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-4124. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0300h

Figure 4-1991. HSM_TPCC0_EMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4125. EMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event Missed #31
30	E30	RO	0h	Event Missed #30
29	E29	RO	0h	Event Missed #29
28	E28	RO	0h	Event Missed #28
27	E27	RO	0h	Event Missed #27
26	E26	RO	0h	Event Missed #26
25	E25	RO	0h	Event Missed #25
24	E24	RO	0h	Event Missed #24
23	E23	RO	0h	Event Missed #23
22	E22	RO	0h	Event Missed #22
21	E21	RO	0h	Event Missed #21
20	E20	RO	0h	Event Missed #20
19	E19	RO	0h	Event Missed #19
18	E18	RO	0h	Event Missed #18
17	E17	RO	0h	Event Missed #17
16	E16	RO	0h	Event Missed #16
15	E15	RO	0h	Event Missed #15
14	E14	RO	0h	Event Missed #14
13	E13	RO	0h	Event Missed #13
12	E12	RO	0h	Event Missed #12
11	E11	RO	0h	Event Missed #11
10	E10	RO	0h	Event Missed #10
9	E9	RO	0h	Event Missed #9
8	E8	RO	0h	Event Missed #8

Table 4-4125. EMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1
0	E0	RO	0h	Event Missed #0

4.33.9 HSM_TPCC0_EMRH Register (Offset = 304h) [reset = h]

Short Description: Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-4126. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0304h

Figure 4-1992. HSM_TPCC0_EMRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4127. EMRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event Missed #63
30	E62	RO	0h	Event Missed #62
29	E61	RO	0h	Event Missed #61
28	E60	RO	0h	Event Missed #60
27	E59	RO	0h	Event Missed #59
26	E58	RO	0h	Event Missed #58
25	E57	RO	0h	Event Missed #57
24	E56	RO	0h	Event Missed #56
23	E55	RO	0h	Event Missed #55
22	E54	RO	0h	Event Missed #54
21	E53	RO	0h	Event Missed #53
20	E52	RO	0h	Event Missed #52
19	E51	RO	0h	Event Missed #51
18	E50	RO	0h	Event Missed #50
17	E49	RO	0h	Event Missed #49
16	E48	RO	0h	Event Missed #48
15	E47	RO	0h	Event Missed #47
14	E46	RO	0h	Event Missed #46
13	E45	RO	0h	Event Missed #45
12	E44	RO	0h	Event Missed #44
11	E43	RO	0h	Event Missed #43
10	E42	RO	0h	Event Missed #42
9	E41	RO	0h	Event Missed #41
8	E40	RO	0h	Event Missed #40

Table 4-4127. EMRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	E39	RO	0h	Event Missed #39
6	E38	RO	0h	Event Missed #38
5	E37	RO	0h	Event Missed #37
4	E36	RO	0h	Event Missed #36
3	E35	RO	0h	Event Missed #35
2	E34	RO	0h	Event Missed #34
1	E33	RO	0h	Event Missed #33
0	E32	RO	0h	Event Missed #32

4.33.10 HSM_TPCC0_EMCR Register (Offset = 308h) [reset = h]

Short Description: Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4128. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0308h

Figure 4-1993. HSM_TPCC0_EMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4129. EMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event Missed Clear #31
30	E30	WO	0h	Event Missed Clear #30
29	E29	WO	0h	Event Missed Clear #29
28	E28	WO	0h	Event Missed Clear #28
27	E27	WO	0h	Event Missed Clear #27
26	E26	WO	0h	Event Missed Clear #26
25	E25	WO	0h	Event Missed Clear #25
24	E24	WO	0h	Event Missed Clear #24
23	E23	WO	0h	Event Missed Clear #23
22	E22	WO	0h	Event Missed Clear #22
21	E21	WO	0h	Event Missed Clear #21
20	E20	WO	0h	Event Missed Clear #20
19	E19	WO	0h	Event Missed Clear #19
18	E18	WO	0h	Event Missed Clear #18
17	E17	WO	0h	Event Missed Clear #17
16	E16	WO	0h	Event Missed Clear #16
15	E15	WO	0h	Event Missed Clear #15
14	E14	WO	0h	Event Missed Clear #14
13	E13	WO	0h	Event Missed Clear #13
12	E12	WO	0h	Event Missed Clear #12
11	E11	WO	0h	Event Missed Clear #11
10	E10	WO	0h	Event Missed Clear #10
9	E9	WO	0h	Event Missed Clear #9
8	E8	WO	0h	Event Missed Clear #8
7	E7	WO	0h	Event Missed Clear #7

Table 4-4129. EMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

4.33.11 HSM_TPCC0_EMCRH Register (Offset = 30Ch) [reset = h]

Short Description: Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4130. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 030Ch

Figure 4-1994. HSM_TPCC0_EMCRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4131. EMCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event Missed Clear #63
30	E62	WO	0h	Event Missed Clear #62
29	E61	WO	0h	Event Missed Clear #61
28	E60	WO	0h	Event Missed Clear #60
27	E59	WO	0h	Event Missed Clear #59
26	E58	WO	0h	Event Missed Clear #58
25	E57	WO	0h	Event Missed Clear #57
24	E56	WO	0h	Event Missed Clear #56
23	E55	WO	0h	Event Missed Clear #55
22	E54	WO	0h	Event Missed Clear #54
21	E53	WO	0h	Event Missed Clear #53
20	E52	WO	0h	Event Missed Clear #52
19	E51	WO	0h	Event Missed Clear #51
18	E50	WO	0h	Event Missed Clear #50
17	E49	WO	0h	Event Missed Clear #49
16	E48	WO	0h	Event Missed Clear #48
15	E47	WO	0h	Event Missed Clear #47
14	E46	WO	0h	Event Missed Clear #46
13	E45	WO	0h	Event Missed Clear #45
12	E44	WO	0h	Event Missed Clear #44
11	E43	WO	0h	Event Missed Clear #43
10	E42	WO	0h	Event Missed Clear #42
9	E41	WO	0h	Event Missed Clear #41
8	E40	WO	0h	Event Missed Clear #40
7	E39	WO	0h	Event Missed Clear #39

Table 4-4131. EMCRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event Missed Clear #38
5	E37	WO	0h	Event Missed Clear #37
4	E36	WO	0h	Event Missed Clear #36
3	E35	WO	0h	Event Missed Clear #35
2	E34	WO	0h	Event Missed Clear #34
1	E33	WO	0h	Event Missed Clear #33
0	E32	WO	0h	Event Missed Clear #32

4.33.12 HSM_TPCC0_QEMR Register (Offset = 310h) [reset = h]

Short Description: QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-4132. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0310h

Figure 4-1995. HSM_TPCC0_QEMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES31								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4133. QEMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES31	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1
0	E0	RO	0h	Event Missed #0

4.33.13 HSM_TPCC0_QEMCR Register (Offset = 314h) [reset = h]

Short Description: QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4134. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0314h

Figure 4-1996. HSM_TPCC0_QEMCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES32															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES32								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4135. QEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES32	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event Missed Clear #7
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

4.33.14 HSM_TPCC0_CCERR Register (Offset = 318h) [reset = h]

Short Description: CC Error Register

Long Description:

Return to Summary Table

Table 4-4136. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0318h

Figure 4-1997. HSM_TPCC0_CCERR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES33															TCERR
RO															RO
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES34								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4137. CCERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES33	RO	0h	RESERVE FIELD
16	TCERR	RO	0h	Transfer Completion Code Error: TCCERR = 0 : Total number of allowed TCCs outstanding has not been reached. TCCERR = 1 : Total number of allowed TCCs has been reached. TCCERR can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors were previously clear) then an error will be signaled with TPCC error interrupt.
15 - 8	RES34	RO	0h	RESERVE FIELD
7	QTHRXCD7	RO	0h	Queue Threshold Error for Q7: QTHRXCD7 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD7 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
6	QTHRXCD6	RO	0h	Queue Threshold Error for Q6: QTHRXCD6 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD6 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
5	QTHRXCD5	RO	0h	Queue Threshold Error for Q5: QTHRXCD5 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD5 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD5 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

Table 4-4137. CCERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	QTHRXCD4	RO	0h	Queue Threshold Error for Q4: QTHRXCD4 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD4 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD4 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
3	QTHRXCD3	RO	0h	Queue Threshold Error for Q3: QTHRXCD3 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD3 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD3 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
2	QTHRXCD2	RO	0h	Queue Threshold Error for Q2: QTHRXCD2 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD2 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD2 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
1	QTHRXCD1	RO	0h	Queue Threshold Error for Q1: QTHRXCD1 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD1 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD1 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
0	QTHRXCD0	RO	0h	Queue Threshold Error for Q0: QTHRXCD0 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD0 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD0 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

4.33.15 HSM_TPCC0_CCERRCLR Register (Offset = 31Ch) [reset = h]

Short Description: CC Error Clear Register

Long Description:

Return to Summary Table

Table 4-4138. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 031Ch

Figure 4-1998. HSM_TPCC0_CCERRCLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES35															TCERR
RO															WO
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES36								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4139. CCERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES35	RO	0h	RESERVE FIELD
16	TCERR	WO	0h	Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect.
15 - 8	RES36	RO	0h	RESERVE FIELD
7	QTHRXCD7	WO	0h	Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect.
6	QTHRXCD6	WO	0h	Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect.
5	QTHRXCD5	WO	0h	Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect.
4	QTHRXCD4	WO	0h	Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect.
3	QTHRXCD3	WO	0h	Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect.
2	QTHRXCD2	WO	0h	Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect.
1	QTHRXCD1	WO	0h	Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect.
0	QTHRXCD0	WO	0h	Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect.

4.33.16 HSM_TPCC0_EEVAL Register (Offset = 320h) [reset = h]

Short Description: Error Eval Register

Long Description:

Return to Summary Table

Table 4-4140. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0320h

Figure 4-1999. HSM_TPCC0_EEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES37															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES37														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-4141. EEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES37	RO	0h	RESERVE FIELD
1	SET	WO	0h	Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect.
0	EVAL	WO	0h	Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect.

4.33.17 HSM_TPCC0_DRAEM Register (Offset = 340h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-4142. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0340h

Figure 4-2000. HSM_TPCC0_DRAEM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4143. DRAEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RW	0h	DMA Region Access enable for Region M bit #31
30	E30	RW	0h	DMA Region Access enable for Region M bit #30
29	E29	RW	0h	DMA Region Access enable for Region M bit #29
28	E28	RW	0h	DMA Region Access enable for Region M bit #28
27	E27	RW	0h	DMA Region Access enable for Region M bit #27
26	E26	RW	0h	DMA Region Access enable for Region M bit #26
25	E25	RW	0h	DMA Region Access enable for Region M bit #25
24	E24	RW	0h	DMA Region Access enable for Region M bit #24
23	E23	RW	0h	DMA Region Access enable for Region M bit #23
22	E22	RW	0h	DMA Region Access enable for Region M bit #22
21	E21	RW	0h	DMA Region Access enable for Region M bit #21
20	E20	RW	0h	DMA Region Access enable for Region M bit #20
19	E19	RW	0h	DMA Region Access enable for Region M bit #19
18	E18	RW	0h	DMA Region Access enable for Region M bit #18
17	E17	RW	0h	DMA Region Access enable for Region M bit #17
16	E16	RW	0h	DMA Region Access enable for Region M bit #16
15	E15	RW	0h	DMA Region Access enable for Region M bit #15
14	E14	RW	0h	DMA Region Access enable for Region M bit #14
13	E13	RW	0h	DMA Region Access enable for Region M bit #13
12	E12	RW	0h	DMA Region Access enable for Region M bit #12
11	E11	RW	0h	DMA Region Access enable for Region M bit #11
10	E10	RW	0h	DMA Region Access enable for Region M bit #10
9	E9	RW	0h	DMA Region Access enable for Region M bit #9

Table 4-4143. DRAEM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	E8	RW	0h	DMA Region Access enable for Region M bit #8
7	E7	RW	0h	DMA Region Access enable for Region M bit #7
6	E6	RW	0h	DMA Region Access enable for Region M bit #6
5	E5	RW	0h	DMA Region Access enable for Region M bit #5
4	E4	RW	0h	DMA Region Access enable for Region M bit #4
3	E3	RW	0h	DMA Region Access enable for Region M bit #3
2	E2	RW	0h	DMA Region Access enable for Region M bit #2
1	E1	RW	0h	DMA Region Access enable for Region M bit #1
0	E0	RW	0h	DMA Region Access enable for Region M bit #0

4.33.18 HSM_TPCC0_DRAEHM Register (Offset = 344h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-4144. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0344h

Figure 4-2001. HSM_TPCC0_DRAEHM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4145. DRAEHM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RW	0h	DMA Region Access enable for Region M bit #63
30	E62	RW	0h	DMA Region Access enable for Region M bit #62
29	E61	RW	0h	DMA Region Access enable for Region M bit #61
28	E60	RW	0h	DMA Region Access enable for Region M bit #60
27	E59	RW	0h	DMA Region Access enable for Region M bit #59
26	E58	RW	0h	DMA Region Access enable for Region M bit #58
25	E57	RW	0h	DMA Region Access enable for Region M bit #57
24	E56	RW	0h	DMA Region Access enable for Region M bit #56
23	E55	RW	0h	DMA Region Access enable for Region M bit #55
22	E54	RW	0h	DMA Region Access enable for Region M bit #54
21	E53	RW	0h	DMA Region Access enable for Region M bit #53
20	E52	RW	0h	DMA Region Access enable for Region M bit #52
19	E51	RW	0h	DMA Region Access enable for Region M bit #51
18	E50	RW	0h	DMA Region Access enable for Region M bit #50
17	E49	RW	0h	DMA Region Access enable for Region M bit #49
16	E48	RW	0h	DMA Region Access enable for Region M bit #48
15	E47	RW	0h	DMA Region Access enable for Region M bit #47
14	E46	RW	0h	DMA Region Access enable for Region M bit #46

Table 4-4145. DRAEHM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E45	RW	0h	DMA Region Access enable for Region M bit #45
12	E44	RW	0h	DMA Region Access enable for Region M bit #44
11	E43	RW	0h	DMA Region Access enable for Region M bit #43
10	E42	RW	0h	DMA Region Access enable for Region M bit #42
9	E41	RW	0h	DMA Region Access enable for Region M bit #41
8	E40	RW	0h	DMA Region Access enable for Region M bit #40
7	E39	RW	0h	DMA Region Access enable for Region M bit #39
6	E38	RW	0h	DMA Region Access enable for Region M bit #38
5	E37	RW	0h	DMA Region Access enable for Region M bit #37
4	E36	RW	0h	DMA Region Access enable for Region M bit #36
3	E35	RW	0h	DMA Region Access enable for Region M bit #35
2	E34	RW	0h	DMA Region Access enable for Region M bit #34
1	E33	RW	0h	DMA Region Access enable for Region M bit #33
0	E32	RW	0h	DMA Region Access enable for Region M bit #32

4.33.19 HSM_TPCC0_QRAEN Register (Offset = 380h) [reset = h]

Short Description: QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

Long Description:

Return to Summary Table

Table 4-4146. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0380h

Figure 4-2002. HSM_TPCC0_QRAEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES38															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES38								E7	E6	E5	E4	E3	E2	E1	E0
RO								RW	RW	RW	RW	RW	RW	RW	RW
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4147. QRAEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES38	RO	0h	RESERVE FIELD
7	E7	RW	0h	QDMA Region Access enable for Region M bit #7
6	E6	RW	0h	QDMA Region Access enable for Region M bit #6
5	E5	RW	0h	QDMA Region Access enable for Region M bit #5
4	E4	RW	0h	QDMA Region Access enable for Region M bit #4
3	E3	RW	0h	QDMA Region Access enable for Region M bit #3
2	E2	RW	0h	QDMA Region Access enable for Region M bit #2
1	E1	RW	0h	QDMA Region Access enable for Region M bit #1
0	E0	RW	0h	QDMA Region Access enable for Region M bit #0

4.33.20 HSM_TPCC0_QNE0 Register (Offset = 400h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-4148. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0400h

Figure 4-2003. HSM_TPCC0_QNE0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES39															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES39								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4149. QNE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES39	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.21 HSM_TPCC0_QNE1 Register (Offset = 404h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 1

Long Description:

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Table 4-4150. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0404h

Figure 4-2004. HSM_TPCC0_QNE1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES40								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4151. QNE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES40	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.22 HSM_TPCC0_QNE2 Register (Offset = 408h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 2

Long Description:

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Table 4-4152. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0408h

Figure 4-2005. HSM_TPCC0_QNE2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES41															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES41								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4153. QNE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES41	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.23 HSM_TPCC0_QNE3 Register (Offset = 40Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 3

Long Description:

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Table 4-4154. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 040Ch

Figure 4-2006. HSM_TPCC0_QNE3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES42															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES42								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4155. QNE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES42	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.24 HSM_TPCC0_QNE4 Register (Offset = 410h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 4

Long Description:

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Table 4-4156. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0410h

Figure 4-2007. HSM_TPCC0_QNE4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES43															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES43								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4157. QNE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES43	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.25 HSM_TPCC0_QNE5 Register (Offset = 414h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 5

Long Description:

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Table 4-4158. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0414h

Figure 4-2008. HSM_TPCC0_QNE5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES44															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES44								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4159. QNE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES44	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.26 HSM_TPCC0_QNE6 Register (Offset = 418h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 6

Long Description:

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Table 4-4160. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0418h

Figure 4-2009. HSM_TPCC0_QNE6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES45															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES45								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4161. QNE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES45	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.27 HSM_TPCC0_QNE7 Register (Offset = 41Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 7

Long Description:

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Table 4-4162. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 041Ch

Figure 4-2010. HSM_TPCC0_QNE7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES46															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES46								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4163. QNE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES46	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.28 HSM_TPCC0_QNE8 Register (Offset = 420h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 8

Long Description:

Return to Summary Table

Table 4-4164. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0420h

Figure 4-2011. HSM_TPCC0_QNE8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES47								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4165. QNE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES47	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.29 HSM_TPCC0_QNE9 Register (Offset = 424h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 9

Long Description:

Return to Summary Table

Table 4-4166. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0424h

Figure 4-2012. HSM_TPCC0_QNE9 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES48															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES48								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4167. QNE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES48	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.30 HSM_TPCC0_QNE10 Register (Offset = 428h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-4168. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0428h

Figure 4-2013. HSM_TPCC0_QNE10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES49								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4169. QNE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES49	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.31 HSM_TPCC0_QNE11 Register (Offset = 42Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 11

Long Description:

Return to Summary Table

Table 4-4170. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 042Ch

Figure 4-2014. HSM_TPCC0_QNE11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES50															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES50								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4171. QNE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES50	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.32 HSM_TPCC0_QNE12 Register (Offset = 430h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 12

Long Description:

Return to Summary Table

Table 4-4172. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0430h

Figure 4-2015. HSM_TPCC0_QNE12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES51															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES51								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4173. QNE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES51	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.33 HSM_TPCC0_QNE13 Register (Offset = 434h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 13

Long Description:

Return to Summary Table

Table 4-4174. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0434h

Figure 4-2016. HSM_TPCC0_QNE13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES52															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES52								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4175. QNE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES52	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.34 HSM_TPCC0_QNE14 Register (Offset = 438h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 14

Long Description:

Return to Summary Table

Table 4-4176. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0438h

Figure 4-2017. HSM_TPCC0_QNE14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES53															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES53								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4177. QNE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES53	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.35 HSM_TPCC0_QNE15 Register (Offset = 43Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 15

Long Description:

Return to Summary Table

Table 4-4178. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 043Ch

Figure 4-2018. HSM_TPCC0_QNE15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES54															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES54								ETYPE		ENUM					
RO								RO		RO					
0								0		0					

Access Types Legend

Table 4-4179. QNE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES54	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

4.33.36 HSM_TPCC0_QSTATN Register (Offset = 600h) [reset = h]

Short Description: QSTATn Register Set

Long Description:

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Table 4-4180. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0600h

Figure 4-2019. HSM_TPCC0_QSTATN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES55							THRXCD	RES56			WM				
RO							RO	RO			RO				
0							0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES57			NUMVAL					RES58			STRTPTR				
RO			RO					RO			RO				
0			0					0			0				

Access Types Legend

Table 4-4181. QSTATN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RES55	RO	0h	RESERVE FIELD
24	THRXCD	RO	0h	Threshold Exceeded: THRXCD = 0 : Threshold specified by QWMTHR(A B).Qn has not been exceeded. THRXCD = 1 : Threshold specified by QWMTHR(A B).Qn has been exceeded. QSTATn.THRXCD is cleared via CCERR.WMCLRn bit.
23 - 21	RES56	RO	0h	RESERVE FIELD
20 - 16	WM	RO	0h	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark (WM) was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 (empty) to 0x10 (full)
15 - 13	RES57	RO	0h	RESERVE FIELD
12 - 8	NUMVAL	RO	0h	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 (empty) to 0x10 (full)
7 - 4	RES58	RO	0h	RESERVE FIELD
3 - 0	STRTPTR	RO	0h	Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 (0th entry) to 0xF (15th entry)

4.33.37 HSM_TPCC0_QWMTHRA Register (Offset = 620h) [reset = h]

Short Description: Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

Long Description:

Return to Summary Table

Table 4-4182. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0620h

Figure 4-2020. HSM_TPCC0_QWMTHRA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES59															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES59			Q1					RES60			Q0				
RO			RW					RO			RW				
0			10000					0			10000				

Access Types Legend

Table 4-4183. QWMTHRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RES59	RO	0h	RESERVE FIELD
12 - 8	Q1	RW	2710h	Queue Threshold for Q1 value
7 - 5	RES60	RO	0h	RESERVE FIELD
4 - 0	Q0	RW	2710h	Queue Threshold for Q0 value

4.33.38 HSM_TPCC0_CCSTAT Register (Offset = 640h) [reset = h]

Short Description: CC Status Register

Long Description:

Return to Summary Table

Table 4-4184. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0640h

Figure 4-2021. HSM_TPCC0_CCSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES61								QUEACTV7	QUEACTV6	QUEACTV5	QUEACTV4	QUEACTV3	QUEACTV2	QUEACTV1	QUEACTV0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES62		COMPACTV						RES63			ACTV	RES64	TRACTV	QEVTACTV	EVTACTV
RO		RO						RO			RO	RO	RO	RO	RO
0		0						0			0	0	0	0	0

Access Types Legend

Table 4-4185. CCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RES61	RO	0h	RESERVE FIELD
23	QUEACTV7	RO	0h	Queue 7 Active QUEACTV7 = 0 : No Evts are queued in Q7. QUEACTV7 = 1 : At least one TR is queued in Q7.
22	QUEACTV6	RO	0h	Queue 6 Active QUEACTV6 = 0 : No Evts are queued in Q6. QUEACTV6 = 1 : At least one TR is queued in Q6.
21	QUEACTV5	RO	0h	Queue 5 Active QUEACTV5 = 0 : No Evts are queued in Q5. QUEACTV5 = 1 : At least one TR is queued in Q5.
20	QUEACTV4	RO	0h	Queue 4 Active QUEACTV4 = 0 : No Evts are queued in Q4. QUEACTV4 = 1 : At least one TR is queued in Q4.
19	QUEACTV3	RO	0h	Queue 3 Active QUEACTV3 = 0 : No Evts are queued in Q3. QUEACTV3 = 1 : At least one TR is queued in Q3.
18	QUEACTV2	RO	0h	Queue 2 Active QUEACTV2 = 0 : No Evts are queued in Q2. QUEACTV2 = 1 : At least one TR is queued in Q2.
17	QUEACTV1	RO	0h	Queue 1 Active QUEACTV1 = 0 : No Evts are queued in Q1. QUEACTV1 = 1 : At least one TR is queued in Q1.
16	QUEACTV0	RO	0h	Queue 0 Active QUEACTV0 = 0 : No Evts are queued in Q0. QUEACTV0 = 1 : At least one TR is queued in Q0.
15 - 14	RES62	RO	0h	RESERVE FIELD
13 - 8	COMPACTV	RO	0h	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV = 0 : No completion requests outstanding. COMPACTV = 1: Total of '1' completion request outstanding. ... COMPACTV = 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63.
7 - 5	RES63	RO	0h	RESERVE FIELD

Table 4-4185. CCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ACTV	RO	0h	Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy.
3	RES64	RO	0h	RESERVE FIELD
2	TRACTV	RO	0h	Transfer Request Active: TRACTV = 0 : Transfer Request processing/submission logic is inactive. TRACTV = 1 : Transfer Request processing/submission logic is active.
1	QEVTACTV	RO	0h	QDMA Event Active: QEVTACTV = 0 : No enabled QDMA Events are active within the CC. QEVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.
0	EVTACTV	RO	0h	DMA Event Active: EVTACTV = 0 : No enabled DMA Events are active within the CC. EVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.

4.33.39 HSM_TPCC0_AETCTL Register (Offset = 700h) [reset = h]

Short Description: Advanced Event Trigger Control

Long Description:

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Table 4-4186. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0700h

Figure 4-2022. HSM_TPCC0_AETCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	RES65														
RW	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES65		ENDINT						RES66	TYPE	STRTEVT					
RO		RW						RO	RW	RW					
0		0						0	0	0					

Access Types Legend

Table 4-4187. AETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	RW	0h	AET Enable: EN = 0 : AET event generation is disabled. EN = 1 : AET event generation is enabled.
30 - 14	RES65	RO	0h	RESERVE FIELD
13 - 8	ENDINT	RW	0h	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted (low)
7	RES66	RO	0h	RESERVE FIELD
6	TYPE	RW	0h	AET Event Type: TYPE = 0 : Event specified by STARTEVT applies to DMA Events (set by ER ESR or CER) TYPE = 1 : Event specified by STARTEVT applies to QDMA Events
5 - 0	STRTEVT	RW	0h	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted (high)

4.33.40 HSM_TPCC0_AETSTAT Register (Offset = 704h) [reset = h]

Short Description: Advanced Event Trigger Stat

Long Description:

Return to Summary Table

Table 4-4188. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0704h

Figure 4-2023. HSM_TPCC0_AETSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES67															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES67															STAT
RO															RO
0															0

Access Types Legend

Table 4-4189. AETSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES67	RO	0h	RESERVE FIELD
0	STAT	RO	0h	AET Status: AETSTAT = 0 : tpcc_aet is currently low. AETSTAT = 1 : tpcc_aet is currently high.

4.33.41 HSM_TPCC0_AETCMD Register (Offset = 708h) [reset = h]

Short Description: AET Command

Long Description:

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Table 4-4190. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 0708h

Figure 4-2024. HSM_TPCC0_AETCMD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES68															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES68															CLR
RO															WO
0															0

Access Types Legend

Table 4-4191. AETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES68	RO	0h	RESERVE FIELD
0	CLR	WO	0h	AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect..

4.33.42 HSM_TPCC0_ER Register (Offset = 1000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

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Table 4-4192. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1000h

Figure 4-2025. HSM_TPCC0_ER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4193. ER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4193. ER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.43 HSM_TPCC0_ERH Register (Offset = 1004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-4194. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1004h

Figure 4-2026. HSM_TPCC0_ERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4195. ERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4195. ERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.44 HSM_TPCC0_ECR Register (Offset = 1008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4196. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1008h

Figure 4-2027. HSM_TPCC0_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4197. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4197. ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.45 HSM_TPCC0_ECRH Register (Offset = 100Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4198. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 100Ch

Figure 4-2028. HSM_TPCC0_ECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4199. ECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4199. ECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.46 HSM_TPCC0_ESR Register (Offset = 1010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4200. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1010h

Figure 4-2029. HSM_TPCC0_ESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4201. ESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4201. ESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.47 HSM_TPCC0_ESRH Register (Offset = 1014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4202. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1014h

Figure 4-2030. HSM_TPCC0_ESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4203. ESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4203. ESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.48 HSM_TPCC0_CER Register (Offset = 1018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-4204. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1018h

Figure 4-2031. HSM_TPCC0_CER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4205. CER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4205. CER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.49 HSM_TPCC0_CERH Register (Offset = 101Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-4206. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 101Ch

Figure 4-2032. HSM_TPCC0_CERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4207. CERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4207. CERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.50 HSM_TPCC0_EER Register (Offset = 1020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-4208. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1020h

Figure 4-2033. HSM_TPCC0_EER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4209. EER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4209. EER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.51 HSM_TPCC0_EERH Register (Offset = 1024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-4210. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1024h

Figure 4-2034. HSM_TPCC0_EERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4211. EERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4211. EERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.52 HSM_TPCC0_EECR Register (Offset = 1028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4212. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1028h

Figure 4-2035. HSM_TPCC0_EECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4213. EECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4213. EECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.53 HSM_TPCC0_EECRH Register (Offset = 102Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4214. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 102Ch

Figure 4-2036. HSM_TPCC0_EECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4215. EECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4215. EECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.54 HSM_TPCC0_EESR Register (Offset = 1030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4216. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1030h

Figure 4-2037. HSM_TPCC0_EESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4217. EESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4217. EESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.55 HSM_TPCC0_EESRH Register (Offset = 1034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4218. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1034h

Figure 4-2038. HSM_TPCC0_EESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4219. EESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4219. EESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.56 HSM_TPCC0_SER Register (Offset = 1038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-4220. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1038h

Figure 4-2039. HSM_TPCC0_SER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4221. SER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7

Table 4-4221. SER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.57 HSM_TPCC0_SERH Register (Offset = 103Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-4222. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 103Ch

Figure 4-2040. HSM_TPCC0_SERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4223. SERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39

Table 4-4223. SERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.58 HSM_TPCC0_SECR Register (Offset = 1040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4224. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1040h

Figure 4-2041. HSM_TPCC0_SECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4225. SECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7

Table 4-4225. SECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.59 HSM_TPCC0_SECRH Register (Offset = 1044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4226. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1044h

Figure 4-2042. HSM_TPCC0_SECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4227. SECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39

Table 4-4227. SECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.60 HSM_TPCC0_IER Register (Offset = 1050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-4228. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1050h

Figure 4-2043. HSM_TPCC0_IER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4229. IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7

Table 4-4229. IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.33.61 HSM_TPCC0_IERH Register (Offset = 1054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-4230. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1054h

Figure 4-2044. HSM_TPCC0_IERH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4231. IERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39

Table 4-4231. IERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.33.62 HSM_TPCC0_IECR Register (Offset = 1058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4232. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1058h

Figure 4-2045. HSM_TPCC0_IECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4233. IECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4233. IECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.63 HSM_TPCC0_IECRH Register (Offset = 105Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4234. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 105Ch

Figure 4-2046. HSM_TPCC0_IECRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4235. IECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-4235. IECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.64 HSM_TPCC0_IESR Register (Offset = 1060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4236. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1060h

Figure 4-2047. HSM_TPCC0_IESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4237. IESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4237. IESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.65 HSM_TPCC0_IESRH Register (Offset = 1064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4238. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1064h

Figure 4-2048. HSM_TPCC0_IESRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4239. IESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-4239. IESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.66 HSM_TPCC0_IPR Register (Offset = 1068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-4240. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1068h

Figure 4-2049. HSM_TPCC0_IPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4241. IPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6

Table 4-4241. IPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.33.67 HSM_TPCC0_IPRH Register (Offset = 106Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-4242. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 106Ch

Figure 4-2050. HSM_TPCC0_IPRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4243. IPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38

Table 4-4243. IPRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.33.68 HSM_TPCC0_ICR Register (Offset = 1070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4244. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1070h

Figure 4-2051. HSM_TPCC0_ICR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4245. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4245. ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.69 HSM_TPCC0_ICRH Register (Offset = 1074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4246. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1074h

Figure 4-2052. HSM_TPCC0_ICRH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4247. ICRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39

Table 4-4247. ICRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.70 HSM_TPCC0_IEVAL Register (Offset = 1078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

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Table 4-4248. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1078h

Figure 4-2053. HSM_TPCC0_IEVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES69															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES69														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-4249. IEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES69	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

4.33.71 HSM_TPCC0_QER Register (Offset = 1080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

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Table 4-4250. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1080h

Figure 4-2054. HSM_TPCC0_QER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES70															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES70								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4251. QER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES70	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.72 HSM_TPCC0_QEER Register (Offset = 1084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

Return to Summary Table

Table 4-4252. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1084h

Figure 4-2055. HSM_TPCC0_QEER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES71															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES71								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4253. QEER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES71	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.73 HSM_TPCC0_QEECR Register (Offset = 1088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4254. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1088h

Figure 4-2056. HSM_TPCC0_QEECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES72															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES72								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4255. QEECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES72	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.74 HSM_TPCC0_QEESR Register (Offset = 108Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4256. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 108Ch

Figure 4-2057. HSM_TPCC0_QEESR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES73								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4257. QEESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES73	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.75 HSM_TPCC0_QSER Register (Offset = 1090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-4258. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1090h

Figure 4-2058. HSM_TPCC0_QSER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES74															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES74								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4259. QSER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES74	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.76 HSM_TPCC0_QSECR Register (Offset = 1094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4260. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 1094h

Figure 4-2059. HSM_TPCC0_QSECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES75															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES75								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4261. QSECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES75	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.77 HSM_TPCC0_ER_RN Register (Offset = 2000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

Return to Summary Table

Table 4-4262. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2000h

Figure 4-2060. HSM_TPCC0_ER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4263. ER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4263. ER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.78 HSM_TPCC0_ERH_RN Register (Offset = 2004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-4264. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2004h

Figure 4-2061. HSM_TPCC0_ERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4265. ERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4265. ERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.79 HSM_TPCC0_ECR_RN Register (Offset = 2008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4266. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2008h

Figure 4-2062. HSM_TPCC0_ECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4267. ECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4267. ECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.80 HSM_TPCC0_ECRH_RN Register (Offset = 200Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4268. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 200Ch

Figure 4-2063. HSM_TPCC0_ECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4269. ECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4269. ECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.81 HSM_TPCC0_ESR_RN Register (Offset = 2010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4270. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2010h

Figure 4-2064. HSM_TPCC0_ESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4271. ESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4271. ESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.82 HSM_TPCC0_ESRH_RN Register (Offset = 2014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4272. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2014h

Figure 4-2065. HSM_TPCC0_ESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4273. ESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4273. ESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.83 HSM_TPCC0_CER_RN Register (Offset = 2018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-4274. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2018h

Figure 4-2066. HSM_TPCC0_CER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4275. CER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4275. CER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.84 HSM_TPCC0_CERH_RN Register (Offset = 201Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-4276. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 201Ch

Figure 4-2067. HSM_TPCC0_CERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4277. CERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4277. CERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.85 HSM_TPCC0_EER_RN Register (Offset = 2020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-4278. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2020h

Figure 4-2068. HSM_TPCC0_EER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4279. EER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10

Table 4-4279. EER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.86 HSM_TPCC0_EERH_RN Register (Offset = 2024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-4280. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2024h

Figure 4-2069. HSM_TPCC0_EERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4281. EERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42

Table 4-4281. EERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.87 HSM_TPCC0_EECR_RN Register (Offset = 2028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4282. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2028h

Figure 4-2070. HSM_TPCC0_EECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4283. EECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4283. EECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.88 HSM_TPCC0_EECRH_RN Register (Offset = 202Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4284. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 202Ch

Figure 4-2071. HSM_TPCC0_EECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4285. EECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4285. EECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.89 HSM_TPCC0_EESR_RN Register (Offset = 2030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4286. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2030h

Figure 4-2072. HSM_TPCC0_EESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4287. EESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6

Table 4-4287. EESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.90 HSM_TPCC0_EESRH_RN Register (Offset = 2034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4288. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2034h

Figure 4-2073. HSM_TPCC0_EESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4289. EESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38

Table 4-4289. EESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.91 HSM_TPCC0_SER_RN Register (Offset = 2038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-4290. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2038h

Figure 4-2074. HSM_TPCC0_SER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4291. SER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7

Table 4-4291. SER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.92 HSM_TPCC0_SERH_RN Register (Offset = 203Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-4292. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 203Ch

Figure 4-2075. HSM_TPCC0_SERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4293. SERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39

Table 4-4293. SERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

4.33.93 HSM_TPCC0_SECR_RN Register (Offset = 2040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4294. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2040h

Figure 4-2076. HSM_TPCC0_SECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4295. SECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7

Table 4-4295. SECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.94 HSM_TPCC0_SECRH_RN Register (Offset = 2044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-4296. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2044h

Figure 4-2077. HSM_TPCC0_SECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4297. SECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39

Table 4-4297. SECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

4.33.95 HSM_TPCC0_IER_RN Register (Offset = 2050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-4298. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2050h

Figure 4-2078. HSM_TPCC0_IER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4299. IER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7

Table 4-4299. IER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.33.96 HSM_TPCC0_IERH_RN Register (Offset = 2054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-4300. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2054h

Figure 4-2079. HSM_TPCC0_IERH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4301. IERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39

Table 4-4301. IERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.33.97 HSM_TPCC0_IECR_RN Register (Offset = 2058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4302. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2058h

Figure 4-2080. HSM_TPCC0_IECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4303. IECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4303. IECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.98 HSM_TPCC0_IECRH_RN Register (Offset = 205Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4304. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 205Ch

Figure 4-2081. HSM_TPCC0_IECRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4305. IECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-4305. IECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.99 HSM_TPCC0_IESR_RN Register (Offset = 2060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4306. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2060h

Figure 4-2082. HSM_TPCC0_IESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4307. IESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4307. IESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.100 HSM_TPCC0_IESRH_RN Register (Offset = 2064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-4308. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2064h

Figure 4-2083. HSM_TPCC0_IESRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4309. IESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38

Table 4-4309. IESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.101 HSM_TPCC0_IPR_RN Register (Offset = 2068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-4310. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2068h

Figure 4-2084. HSM_TPCC0_IPR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4311. IPR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6

Table 4-4311. IPR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

4.33.102 HSM_TPCC0_IPRH_RN Register (Offset = 206Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-4312. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 206Ch

Figure 4-2085. HSM_TPCC0_IPRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4313. IPRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38

Table 4-4313. IPRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

4.33.103 HSM_TPCC0_ICR_RN Register (Offset = 2070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-4314. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2070h

Figure 4-2086. HSM_TPCC0_ICR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4315. ICR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6

Table 4-4315. ICR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

4.33.104 HSM_TPCC0_ICRH_RN Register (Offset = 2074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

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Table 4-4316. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2074h

Figure 4-2087. HSM_TPCC0_ICRH_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32
WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4317. ICRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39

Table 4-4317. ICRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

4.33.105 HSM_TPCC0_IEVAL_RN Register (Offset = 2078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

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Table 4-4318. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2078h

Figure 4-2088. HSM_TPCC0_IEVAL_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES76															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES76														SET	EVAL
RO														WO	WO
0														0	0

Access Types Legend

Table 4-4319. IEVAL_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES76	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

4.33.106 HSM_TPCC0_QER_RN Register (Offset = 2080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

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Table 4-4320. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2080h

Figure 4-2089. HSM_TPCC0_QER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES77															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES77								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4321. QER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES77	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.107 HSM_TPCC0_QEER_RN Register (Offset = 2084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

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Table 4-4322. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2084h

Figure 4-2090. HSM_TPCC0_QEER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES78															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES78								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4323. QEER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES78	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.108 HSM_TPCC0_QEECR_RN Register (Offset = 2088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

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Table 4-4324. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2088h

Figure 4-2091. HSM_TPCC0_QEECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES79															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES79								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4325. QEECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES79	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.109 HSM_TPCC0_QEESR_RN Register (Offset = 208Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

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Table 4-4326. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 208Ch

Figure 4-2092. HSM_TPCC0_QEESR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES80															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES80								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4327. QEESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES80	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.110 HSM_TPCC0_QSER_RN Register (Offset = 2090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

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Table 4-4328. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2090h

Figure 4-2093. HSM_TPCC0_QSER_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES81															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES81								E7	E6	E5	E4	E3	E2	E1	E0
RO								RO	RO	RO	RO	RO	RO	RO	RO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4329. QSER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES81	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

4.33.111 HSM_TPCC0_QSECR_RN Register (Offset = 2094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

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Table 4-4330. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 2094h

Figure 4-2094. HSM_TPCC0_QSECR_RN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES82															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES82								E7	E6	E5	E4	E3	E2	E1	E0
RO								WO	WO	WO	WO	WO	WO	WO	WO
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-4331. QSECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES82	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

4.33.112 HSM_TPCC0_OPT Register (Offset = 4000h) [reset = h]

Short Description: Options Parameter

Long Description:

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Table 4-4332. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4000h

Figure 4-2095. HSM_TPCC0_OPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRIV	RES83			PRIVID				ITCCHEN	TCCHEN	ITCINTEN	TCINTEN	WIMODE	RES84	TCC	
RO	RO			RO				RW	RW	RW	RW	RW	RO	RW	
0	0			0				0	0	0	0	0	0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				TCCMODE	FWID			RES85				STATIC	SYNCDIM	DAM	SAM
RW				RW	RW			RO				RW	RW	RW	RW
0				0	0			0				0	0	0	0

Access Types Legend

Table 4-4333. OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV	RO	0h	Privilege level: privilege level (supervisor vs. user) for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege
30 - 28	RES83	RO	0h	RESERVE FIELD
27 - 24	PRIVID	RO	0h	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.
23	ITCCHEN	RW	0h	Intermediate transfer completion chaining enable: 0: Intermediate transfer complete chaining is disabled. 1: Intermediate transfer complete chaining is enabled.
22	TCCHEN	RW	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled.
21	ITCINTEN	RW	0h	Intermediate transfer completion interrupt enable: 0: Intermediate transfer complete interrupt is disabled. 1: Intermediate transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
20	TCINTEN	RW	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
19	WIMODE	RW	0h	Backward compatibility mode: 0: Normal operation 1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission (0 means 1 1 means 2 ...) and forces ACNT to be treated as a word-count (left shifted by 2 by hardware to create byte cnt for TR submission)
18	RES84	RO	0h	RESERVE FIELD
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER (bit CER[TCC]) for chaining or in IER (bit IER[TCC]) for interrupts.

Table 4-4333. OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TCCMODE	RW	0h	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0: Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC (which was returned from the peripheral). 1: Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally .
10 - 8	FWID	RW	0h	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC.
7 - 4	RES85	RO	0h	RESERVE FIELD
3	STATIC	RW	0h	Static Entry: 0: Entry is updated as normal 1: Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed.
2	SYNCDIM	RW	0h	Transfer Synchronization Dimension: 0: A-Sync Each event triggers the transfer of ACNT elements. 1: AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements
1	DAM	RW	0h	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0: INCR Dst addressing within an array increments. Dst is not a FIFO. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0: INCR Src addressing within an array increments. Source is not a FIFO. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.33.113 HSM_TPCC0_SRC Register (Offset = 4004h) [reset = h]

Short Description: Source Address

Long Description:

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Table 4-4334. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4004h

Figure 4-2096. HSM_TPCC0_SRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRC															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC															
RW															
0															

Access Types Legend

Table 4-4335. SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SRC	RW	0h	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

4.33.114 HSM_TPCC0_ABCNT Register (Offset = 4008h) [reset = h]

Short Description: A and B byte count

Long Description:

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Table 4-4336. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4008h

Figure 4-2097. HSM_TPCC0_ABCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-4337. ABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 (64K-1 arrays). BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ...
15 - 0	ACNT	RW	0h	ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes (64K-1 bytes). ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation (to translate between a word count and a byte count) will dropthe 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT.

4.33.115 HSM_TPCC0_DST Register (Offset = 400Ch) [reset = h]

Short Description: Destination Address

Long Description:

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Table 4-4338. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 400Ch

Figure 4-2098. HSM_TPCC0_DST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DST															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST															
RW															
0															

Access Types Legend

Table 4-4339. DST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DST	RW	0h	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

4.33.116 HSM_TPCC0_BIDX Register (Offset = 4010h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-4340. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4010h

Figure 4-2099. HSM_TPCC0_BIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-4341. BIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value (2's complement) used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers.
15 - 0	SBIDX	RW	0h	Source 2nd Dimension Index: SBIDX is a 16-bit signed value (2's complement) used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.

4.33.117 HSM_TPCC0_LNK Register (Offset = 4014h) [reset = h]

Short Description: Link and Reload parameters

Long Description:

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Table 4-4342. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4014h

Figure 4-2100. HSM_TPCC0_LNK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNTRLD															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK															
RW															
0															

Access Types Legend

Table 4-4343. LNK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNTRLD	RW	0h	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT (conceptually) reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field.
15 - 0	LINK	RW	0h	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination (i.e. after count fields are decremented to '0') with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000 thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case (5-lsbs) behavior is undefined forthe user (i.e. don't have to test it). In the former case (2 msbs) user should be able to take advantage of this feature (i.e. do have to test it). If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field.

4.33.118 HSM_TPCC0_CIDX Register (Offset = 4018h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-4344. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 4018h

Figure 4-2101. HSM_TPCC0_CIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCIDX															
RW															
0															

Access Types Legend

Table 4-4345. CIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DCIDX	RW	0h	Destination Frame Index: DCIDX is a 16-bit signed value (2's complement) used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by DST address) to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame.
15 - 0	SCIDX	RW	0h	Source Frame Index: SCIDX is a 16-bit signed value (2's complement) used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by SRC address) to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame.

4.33.119 HSM_TPCC0_CCNT Register (Offset = 401Ch) [reset = h]

Short Description: C byte count

Long Description:

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Table 4-4346. Instance Table

Instance Name	Physical Address
HSM_TPCC0	4702 401Ch

Figure 4-2102. HSM_TPCC0_CCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES86															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT															
RW															
0															

Access Types Legend

Table 4-4347. CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES86	RO	0h	RESERVE FIELD
15 - 0	CCNT	RW	0h	CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 (64K-1 frames). CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no affect on CCNT operation.

Table 4-4348. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

4.34 TPTC Registers

Table 4-4349. HSM_TPTC00, HSM_TPTC00_HSM_TPTC Registers, Base Address=4704 0000H, Length=8

Offset	Length	Acronym	Register Name	HSM_TPTC00 Physical Address	HSM_TPTC01 Physical Address
0h	32	HSM_TPTC00_PID	Peripheral ID Register	4704 0000h	4706 0000h
4h	16	HSM_TPTC00_TCCFG	TC Configuration Register	4704 0004h	4706 0004h
100h	16	HSM_TPTC00_TCSTAT	TC Status Register	4704 0100h	4706 0100h
104h	8	HSM_TPTC00_INTSTAT	Interrupt Status Register	4704 0104h	4706 0104h
108h	8	HSM_TPTC00_INTEN	Interrupt Enable Register	4704 0108h	4706 0108h
10Ch	8	HSM_TPTC00_INTCLR	Interrupt Clear Register	4704 010Ch	4706 010Ch
110h	8	HSM_TPTC00_INTCMD	Interrupt Command Register	4704 0110h	4706 0110h
120h	8	HSM_TPTC00_ERRSTAT	Error Status Register	4704 0120h	4706 0120h
124h	8	HSM_TPTC00_ERREN	Error Enable Register	4704 0124h	4706 0124h
128h	8	HSM_TPTC00_ERRCLR	Error Clear Register	4704 0128h	4706 0128h
12Ch	24	HSM_TPTC00_ERRDET	Error Details Register	4704 012Ch	4706 012Ch
130h	8	HSM_TPTC00_ERRCMD	Error Command Register	4704 0130h	4706 0130h
140h	8	HSM_TPTC00_RDRATE	Read Rate Register	4704 0140h	4706 0140h
200h	32	HSM_TPTC00_POPT	Prog Set Options	4704 0200h	4706 0200h
204h	32	HSM_TPTC00_PSRC	Prog Set Src Address	4704 0204h	4706 0204h
208h	32	HSM_TPTC00_PCNT	Prog Set Count	4704 0208h	4706 0208h
20Ch	32	HSM_TPTC00_PDST	Prog Set Dst Address	4704 020Ch	4706 020Ch
210h	32	HSM_TPTC00_PBIDX	Prog Set B-Dim Idx	4704 0210h	4706 0210h
214h	16	HSM_TPTC00_PMPPRXY	Prog Set Mem Protect Proxy	4704 0214h	4706 0214h
240h	32	HSM_TPTC00_SAOPT	Src Actv Set Options	4704 0240h	4706 0240h
244h	32	HSM_TPTC00_SASRC	Src Actv Set Src Address	4704 0244h	4706 0244h
248h	24	HSM_TPTC00_SACNT	Src Actv Set A-Count	4704 0248h	4706 0248h
24Ch	32	HSM_TPTC00_SADST	Src Actv Set Dst Address	4704 024Ch	4706 024Ch
250h	32	HSM_TPTC00_SABIDX	Src Actv Set B-Dim Idx	4704 0250h	4706 0250h
254h	16	HSM_TPTC00_SAMPPRXY	Src Actv Set Mem Protect Proxy	4704 0254h	4706 0254h
258h	16	HSM_TPTC00_SACNTRLD	Src Actv Set Cnt Reload	4704 0258h	4706 0258h
25Ch	32	HSM_TPTC00_SASRCBREF	Src Actv Set Src Addr B-Reference	4704 025Ch	4706 025Ch
260h	32	HSM_TPTC00_SADSTBREF	Src Actv Set Dst Addr B-Reference	4704 0260h	4706 0260h
264h	16	HSM_TPTC00_SABCNT	Src Actv Set B-Count	4704 0264h	4706 0264h
280h	16	HSM_TPTC00_DFCNTRLD	Dst FIFO Set Cnt Reload	4704 0280h	4706 0280h
284h	32	HSM_TPTC00_DFSRCBREF	Dst FIFO Set Src Addr B-Reference	4704 0284h	4706 0284h
300h	32	HSM_TPTC00_DFOPT0	Dst FIFO Set Options	4704 0300h	4706 0300h
304h	32	HSM_TPTC00_DFSRC0	Dst FIFO Set Src Address	4704 0304h	4706 0304h
308h	24	HSM_TPTC00_DFACNT0	Dst FIFO Set A-Count	4704 0308h	4706 0308h

Table 4-4349. HSM_TPTC00, HSM_TPTC00_HSM_TPTC Registers, Base Address=4704 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name	HSM_TPTC00 Physical Address	HSM_TPTC01 Physical Address
30Ch	32	HSM_TPTC00_DFDST0	Dst FIFO Set Dst Address	4704 030Ch	4706 030Ch
310h	32	HSM_TPTC00_DFBIDX0	Dst FIFO Set B-Dim Idx	4704 0310h	4706 0310h
314h	16	HSM_TPTC00_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy	4704 0314h	4706 0314h
318h	16	HSM_TPTC00_DFBCNT0	Dst FIFO Set B-Count	4704 0318h	4706 0318h
340h	32	HSM_TPTC00_DFOPT1	Dst FIFO Set Options	4704 0340h	4706 0340h
344h	32	HSM_TPTC00_DFSRC1	Dst FIFO Set Src Address	4704 0344h	4706 0344h
348h	24	HSM_TPTC00_DFACNT1	Dst FIFO Set A-Count	4704 0348h	4706 0348h
34Ch	32	HSM_TPTC00_DFDST1	Dst FIFO Set Dst Address	4704 034Ch	4706 034Ch
350h	32	HSM_TPTC00_DFBIDX1	Dst FIFO Set B-Dim Idx	4704 0350h	4706 0350h
354h	16	HSM_TPTC00_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy	4704 0354h	4706 0354h
358h	16	HSM_TPTC00_DFBCNT1	Dst FIFO Set B-Count	4704 0358h	4706 0358h

Table 4-4350. HSM_TPTC01, HSM_TPTC01_HSM_TPTC Registers, Base Address=4706 0000H, Length=8

Offset	Length	Acronym	Register Name	HSM_TPTC00 Physical Address	HSM_TPTC01 Physical Address
0h	32	HSM_TPTC01_PID	Peripheral ID Register	4704 0000h	4706 0000h
4h	16	HSM_TPTC01_TCCFG	TC Configuration Register	4704 0004h	4706 0004h
100h	16	HSM_TPTC01_TCSTAT	TC Status Register	4704 0100h	4706 0100h
104h	8	HSM_TPTC01_INTSTAT	Interrupt Status Register	4704 0104h	4706 0104h
108h	8	HSM_TPTC01_INTEN	Interrupt Enable Register	4704 0108h	4706 0108h
10Ch	8	HSM_TPTC01_INTCLR	Interrupt Clear Register	4704 010Ch	4706 010Ch
110h	8	HSM_TPTC01_INTCMD	Interrupt Command Register	4704 0110h	4706 0110h
120h	8	HSM_TPTC01_ERRSTAT	Error Status Register	4704 0120h	4706 0120h
124h	8	HSM_TPTC01_ERREN	Error Enable Register	4704 0124h	4706 0124h
128h	8	HSM_TPTC01_ERRCLR	Error Clear Register	4704 0128h	4706 0128h
12Ch	24	HSM_TPTC01_ERRDET	Error Details Register	4704 012Ch	4706 012Ch
130h	8	HSM_TPTC01_ERRCMD	Error Command Register	4704 0130h	4706 0130h
140h	8	HSM_TPTC01_RDRATE	Read Rate Register	4704 0140h	4706 0140h
200h	32	HSM_TPTC01_POPT	Prog Set Options	4704 0200h	4706 0200h
204h	32	HSM_TPTC01_PSRC	Prog Set Src Address	4704 0204h	4706 0204h
208h	32	HSM_TPTC01_PCNT	Prog Set Count	4704 0208h	4706 0208h
20Ch	32	HSM_TPTC01_PDST	Prog Set Dst Address	4704 020Ch	4706 020Ch
210h	32	HSM_TPTC01_PBIDX	Prog Set B-Dim Idx	4704 0210h	4706 0210h
214h	16	HSM_TPTC01_PMPPRXY	Prog Set Mem Protect Proxy	4704 0214h	4706 0214h
240h	32	HSM_TPTC01_SAOPT	Src Actv Set Options	4704 0240h	4706 0240h
244h	32	HSM_TPTC01_SASRC	Src Actv Set Src Address	4704 0244h	4706 0244h
248h	24	HSM_TPTC01_SACNT	Src Actv Set A-Count	4704 0248h	4706 0248h
24Ch	32	HSM_TPTC01_SADST	Src Actv Set Dst Address	4704 024Ch	4706 024Ch
250h	32	HSM_TPTC01_SABIDX	Src Actv Set B-Dim Idx	4704 0250h	4706 0250h
254h	16	HSM_TPTC01_SAMPPRXY	Src Actv Set Mem Protect Proxy	4704 0254h	4706 0254h
258h	16	HSM_TPTC01_SACNTRLD	Src Actv Set Cnt Reload	4704 0258h	4706 0258h

Table 4-4350. HSM_TPTC01, HSM_TPTC01_HSM_TPTC Registers, Base Address=4706 0000H, Length=8 (continued)

Offset	Length	Acronym	Register Name	HSM_TPTC00 Physical Address	HSM_TPTC01 Physical Address
25Ch	32	HSM_TPTC01_SASRCBREF	Src Actv Set Src Addr B-Reference	4704 025Ch	4706 025Ch
260h	32	HSM_TPTC01_SADSTBREF	Src Actv Set Dst Addr B-Reference	4704 0260h	4706 0260h
264h	16	HSM_TPTC01_SABCNT	Src Actv Set B-Count	4704 0264h	4706 0264h
280h	16	HSM_TPTC01_DFCNTRLD	Dst FIFO Set Cnt Reload	4704 0280h	4706 0280h
284h	32	HSM_TPTC01_DFSRCBREF	Dst FIFO Set Src Addr B-Reference	4704 0284h	4706 0284h
300h	32	HSM_TPTC01_DFOPT0	Dst FIFO Set Options	4704 0300h	4706 0300h
304h	32	HSM_TPTC01_DFSRC0	Dst FIFO Set Src Address	4704 0304h	4706 0304h
308h	24	HSM_TPTC01_DFACNT0	Dst FIFO Set A-Count	4704 0308h	4706 0308h
30Ch	32	HSM_TPTC01_DFDST0	Dst FIFO Set Dst Address	4704 030Ch	4706 030Ch
310h	32	HSM_TPTC01_DFBIDX0	Dst FIFO Set B-Dim Idx	4704 0310h	4706 0310h
314h	16	HSM_TPTC01_DFMPPRXY0	Dst FIFO Set Mem Protect Proxy	4704 0314h	4706 0314h
318h	16	HSM_TPTC01_DFBCNT0	Dst FIFO Set B-Count	4704 0318h	4706 0318h
340h	32	HSM_TPTC01_DFOPT1	Dst FIFO Set Options	4704 0340h	4706 0340h
344h	32	HSM_TPTC01_DFSRC1	Dst FIFO Set Src Address	4704 0344h	4706 0344h
348h	24	HSM_TPTC01_DFACNT1	Dst FIFO Set A-Count	4704 0348h	4706 0348h
34Ch	32	HSM_TPTC01_DFDST1	Dst FIFO Set Dst Address	4704 034Ch	4706 034Ch
350h	32	HSM_TPTC01_DFBIDX1	Dst FIFO Set B-Dim Idx	4704 0350h	4706 0350h
354h	16	HSM_TPTC01_DFMPPRXY1	Dst FIFO Set Mem Protect Proxy	4704 0354h	4706 0354h
358h	16	HSM_TPTC01_DFBCNT1	Dst FIFO Set B-Count	4704 0358h	4706 0358h

4.34.1 HSM_TPTC00_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-4351. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0000h
HSM_TPTC01	4706 0000h

Figure 4-2103. HSM_TPTC00_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		NONE		RO											
1		0		0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
1				11				0		1					

Access Types Legend

Table 4-4352. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
	RESERVED	NONE		Reserved
27 - 16	FUNC	RO	0h	Function indicates a software compatible module family.
15 - 11	RTL	RO	1h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	1h	Minor Revision

4.34.2 HSM_TPTC00_TCCFG Register (Offset = 4h) [reset = h]

Short Description: TC Configuration Register

Long Description:

Return to Summary Table

Table 4-4353. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0004h
HSM_TPTC01	4706 0004h

Figure 4-2104. HSM_TPTC00_TCCFG Name Register

15	14	13	12	11	10	9	8
RESERVED						DREGDEPTH	
NONE						RO	
0						10	

7	6	5	4	3	2	1	0
RESERVED		BUSWIDTH		RESERVED	FIFOSIZE		
NONE		RO		NONE	RO		
0		10		0	100		

Access Types Legend

Table 4-4354. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 8	DREGDEPTH	RO	Ah	Dst Register FIFO Depth Parameterization
	RESERVED	NONE		Reserved
5 - 4	BUSWIDTH	RO	Ah	Bus Width Parameterization
	RESERVED	NONE		Reserved
2 - 0	FIFOSIZE	RO	64h	Fifo Size Parameterization

4.34.3 HSM_TPTC00_TCSTAT Register (Offset = 100h) [reset = h]

Short Description: TC Status Register

Long Description:

Return to Summary Table

Table 4-4355. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0100h
HSM_TPTC01	4706 0100h

Figure 4-2105. HSM_TPTC00_TCSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED		DFSTRTPTR		RESERVED			ACTV
NONE		RO		NONE			RO
0		0		0			1
7	6	5	4	3	2	1	0
RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE	RO			NONE	RO	RO	RO
0	0			0	0	0	0

Access Types Legend

Table 4-4356. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 12	DFSTRTPTR	RO	0h	Dst FIFO Start PointerRepresents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
	RESERVED	NONE		Reserved
8	ACTV	RO	1h	Channel ActiveChannel Active is a logical-OR of each of the BUSY/ ACTV signals. The ACTV bit must remain high through the life of a TR.ACTV = 0 : Channel is idle.ACTV = 1 : Channel is busy.
	RESERVED	NONE		Reserved
6 - 4	DSTACTV	RO	0h	Destination Active StateSpecifies the number of TRs that are resident in the Dst Register FIFO at a given instant.Legal values are constrained by the DSTREGDEPTH parameter.
	RESERVED	NONE		Reserved
2	WSACTV	RO	0h	Write Status ActiveWSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands.WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	RO	0h	Source Active StateSRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	RO	0h	Program Register Set BusyPROGBUSY = 0 : Prog set idle and is available for programming.PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

4.34.4 HSM_TPTC00_INTSTAT Register (Offset = 104h) [reset = h]

Short Description: Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-4357. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0104h
HSM_TPTC01	4706 0104h

Figure 4-2106. HSM_TPTC00_INTSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RO	RO
0						0	0

Access Types Legend

Table 4-4358. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RO	0h	TR Done Event Status:TRDONE = 0 : Condition not detected.TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	RO	0h	Program Set Empty Event Status:PROGEMPTY = 0 : Condition not detected.PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

4.34.5 HSM_TPTC00_INTEN Register (Offset = 108h) [reset = h]

Short Description: Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-4359. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0108h
HSM_TPTC01	4706 0108h

Figure 4-2107. HSM_TPTC00_INTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-4360. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RW	0h	TR Done Event Enable:INTEN.TRDONE = 0 : TRDONE Event is disabled.INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	RW	0h	Program Set Empty Event Enable:INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled.INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

4.34.6 HSM_TPTC00_INTCLR Register (Offset = 10Ch) [reset = h]

Short Description: Interrupt Clear Register

Long Description:

Return to Summary Table

Table 4-4361. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 010Ch
HSM_TPTC01	4706 010Ch

Figure 4-2108. HSM_TPTC00_INTCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4362. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	WO	0h	TR Done Event Clear:INTCLR.TRDONE = 0 : Writes of '0' have no effect.INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	WO	0h	Program Set Empty Event Clear:INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect.INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

4.34.7 HSM_TPTC00_INTCMD Register (Offset = 110h) [reset = h]

Short Description: Interrupt Command Register

Long Description:

Return to Summary Table

Table 4-4363. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0110h
HSM_TPTC01	4706 0110h

Figure 4-2109. HSM_TPTC00_INTCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4364. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC interrupt:Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC interruptWrite of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.Writes of '0' have no affect.

4.34.8 HSM_TPTC00_ERRSTAT Register (Offset = 120h) [reset = h]

Short Description: Error Status Register

Long Description:

Return to Summary Table

Table 4-4365. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0120h
HSM_TPTC01	4706 0120h

Figure 4-2110. HSM_TPTC00_ERRSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RO	RO	NONE	RO
0				0	0	0	0

Access Types Legend

Table 4-4366. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RO	0h	MMR Address Error:MMRAERR = 0 : Condition not detected.MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	RO	0h	TR Error:TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
	RESERVED	NONE		Reserved
0	BUSERR	RO	0h	Bus Error Event:BUSERR = 0: Condition not detected.BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

4.34.9 HSM_TPTC00_ERREN Register (Offset = 124h) [reset = h]

Short Description: Error Enable Register

Long Description:

Return to Summary Table

Table 4-4367. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0124h
HSM_TPTC01	4706 0124h

Figure 4-2111. HSM_TPTC00_ERREN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RW	RW	NONE	RW
0				0	0	0	0

Access Types Legend

Table 4-4368. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RW	0h	Interrupt enable for ERRSTAT.MMRAERR:ERREN.MMRAERR = 0 : BUSERR is disabled.ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	RW	0h	Interrupt enable for ERRSTAT.TRERR:ERREN.TRERR = 0 : BUSERR is disabled.ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
	RESERVED	NONE		Reserved
0	BUSERR	RW	0h	Interrupt enable for ERRSTAT.BUSERR:ERREN.BUSERR = 0 : BUSERR is disabled.ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

4.34.10 HSM_TPTC00_ERRCLR Register (Offset = 128h) [reset = h]

Short Description: Error Clear Register

Long Description:

Return to Summary Table

Table 4-4369. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0128h
HSM_TPTC01	4706 0128h

Figure 4-2112. HSM_TPTC00_ERRCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				WO	WO	NONE	WO
0				0	0	0	0

Access Types Legend

Table 4-4370. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	WO	0h	Interrupt clear for ERRSTAT.MMRAERR:ERRCLR.MMRAERR = 0 : Writes of '0' have no effect.ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	WO	0h	Interrupt clear for ERRSTAT.TRERR:ERRCLR.TRERR = 0 : Writes of '0' have no effect.ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
	RESERVED	NONE		Reserved
0	BUSERR	WO	0h	Interrupt clear for ERRSTAT.BUSERR:ERRCLR.BUSERR = 0 : Writes of '0' have no effect.ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

4.34.11 HSM_TPTC00_ERRDET Register (Offset = 12Ch) [reset = h]

Short Description: Error Details Register

Long Description:

Return to Summary Table

Table 4-4371. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 012Ch
HSM_TPTC01	4706 012Ch

Figure 4-2113. HSM_TPTC00_ERRDET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TCCHEN	TCINTEN								
NONE						RO	RO								
0						0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TCC						RESERVED				STAT			
NONE		RO						NONE				RO			
0		0						0				0			

Access Types Legend

Table 4-4372. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TCCHEN	RO	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	RO	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
13 - 8	TCC	RO	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
3 - 0	STAT	RO	0h	Transaction Status:Stores the non-zero status/error code that was detected on the read status or write status bus.MS-bit effectively serves as the read vs. write error code.If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.Encoding of errors matches the CBA spec.

4.34.12 HSM_TPTC00_ERRCMD Register (Offset = 130h) [reset = h]

Short Description: Error Command Register

Long Description:

Return to Summary Table

Table 4-4373. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0130h
HSM_TPTC01	4706 0130h

Figure 4-2114. HSM_TPTC00_ERRCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4374. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC error interrupt:Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC error interruptWrite of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.Writes of '0' have no affect.

4.34.13 HSM_TPTC00_RDRATE Register (Offset = 140h) [reset = h]

Short Description: Read Rate Register

Long Description:

Return to Summary Table

Table 4-4375. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0140h
HSM_TPTC01	4706 0140h

Figure 4-2115. HSM_TPTC00_RDRATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RDRATE		
NONE					RW		
0					0		

Access Types Legend

Table 4-4376. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RDRATE	RW	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

4.34.14 HSM_TPTC00_POPT Register (Offset = 200h) [reset = h]

Short Description: Prog Set Options

Long Description:

Return to Summary Table

Table 4-4377. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0200h
HSM_TPTC01	4706 0200h

Figure 4-2116. HSM_TPTC00_POPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-4378. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.15 HSM_TPTC00_PSRC Register (Offset = 204h) [reset = h]

Short Description: Prog Set Src Address

Long Description:

Return to Summary Table

Table 4-4379. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0204h
HSM_TPTC01	4706 0204h

Figure 4-2117. HSM_TPTC00_PSRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RW															
0															

Access Types Legend

Table 4-4380. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RW	0h	Source address for Program Register Set

4.34.16 HSM_TPTC00_PCNT Register (Offset = 208h) [reset = h]

Short Description: Prog Set Count

Long Description:

Return to Summary Table

Table 4-4381. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0208h
HSM_TPTC01	4706 0208h

Figure 4-2118. HSM_TPTC00_PCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-4382. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15 - 0	ACNT	RW	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.34.17 HSM_TPTC00_PDST Register (Offset = 20Ch) [reset = h]

Short Description: Prog Set Dst Address

Long Description:

Return to Summary Table

Table 4-4383. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 020Ch
HSM_TPTC01	4706 020Ch

Figure 4-2119. HSM_TPTC00_PDST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RW															
0															

Access Types Legend

Table 4-4384. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RW	0h	Destination address for Program Register Set

4.34.18 HSM_TPTC00_PBIDX Register (Offset = 210h) [reset = h]

Short Description: Prog Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4385. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0210h
HSM_TPTC01	4706 0210h

Figure 4-2120. HSM_TPTC00_PBIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-4386. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Dest B-Idx for Program Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RW	0h	Source B-Idx for Program Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.19 HSM_TPTC00_PMPPRXY Register (Offset = 214h) [reset = h]

Short Description: Prog Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4387. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0214h
HSM_TPTC01	4706 0214h

Figure 4-2121. HSM_TPTC00_PMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4388. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.20 HSM_TPTC00_SAOPT Register (Offset = 240h) [reset = h]

Short Description: Src Actv Set Options

Long Description:

Return to Summary Table

Table 4-4389. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0240h
HSM_TPTC01	4706 0240h

Figure 4-2122. HSM_TPTC00_SAOPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-4390. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.21 HSM_TPTC00_SASRC Register (Offset = 244h) [reset = h]

Short Description: Src Actv Set Src Address

Long Description:

Return to Summary Table

Table 4-4391. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0244h
HSM_TPTC01	4706 0244h

Figure 4-2123. HSM_TPTC00_SASRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4392. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address for Source Active Register Set

4.34.22 HSM_TPTC00_SACNT Register (Offset = 248h) [reset = h]

Short Description: Src Actv Set A-Count

Long Description:

Return to Summary Table

Table 4-4393. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0248h
HSM_TPTC01	4706 0248h

Figure 4-2124. HSM_TPTC00_SACNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4394. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.34.23 HSM_TPTC00_SADST Register (Offset = 24Ch) [reset = h]

Short Description: Src Actv Set Dst Address

Long Description:

Return to Summary Table

Table 4-4395. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 024Ch
HSM_TPTC01	4706 024Ch

Figure 4-2125. HSM_TPTC00_SADST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4396. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Source Active Register Set

4.34.24 HSM_TPTC00_SABIDX Register (Offset = 250h) [reset = h]

Short Description: Src Actv Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4397. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0250h
HSM_TPTC01	4706 0250h

Figure 4-2126. HSM_TPTC00_SABIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4398. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Source Active Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Source B-Idx for Source Active Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.25 HSM_TPTC00_SAMPPRXY Register (Offset = 254h) [reset = h]

Short Description: Src Actv Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4399. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0254h
HSM_TPTC01	4706 0254h

Figure 4-2127. HSM_TPTC00_SAMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4400. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.26 HSM_TPTC00_SACNTRLD Register (Offset = 258h) [reset = h]

Short Description: Src Actv Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-4401. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0258h
HSM_TPTC01	4706 0258h

Figure 4-2128. HSM_TPTC00_SACNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-4402. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.34.27 HSM_TPTC00_SASRCBREF Register (Offset = 25Ch) [reset = h]

Short Description: Src Actv Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4403. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 025Ch
HSM_TPTC01	4706 025Ch

Figure 4-2129. HSM_TPTC00_SASRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-4404. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Source Active Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.34.28 HSM_TPTC00_SADSTBREF Register (Offset = 260h) [reset = h]

Short Description: Src Actv Set Dst Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4405. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0260h
HSM_TPTC01	4706 0260h

Figure 4-2130. HSM_TPTC00_SADSTBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF															
RO															
0															

Access Types Legend

Table 4-4406. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDRBREF	RO	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

4.34.29 HSM_TPTC00_SABCNT Register (Offset = 264h) [reset = h]

Short Description: Src Actv Set B-Count

Long Description:

Return to Summary Table

Table 4-4407. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0264h
HSM_TPTC01	4706 0264h

Figure 4-2131. HSM_TPTC00_SABCNT Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4408. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Dimension count:Number of arrays to be transferred where each array is ACNT in length.Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

4.34.30 HSM_TPTC00_DFCNTRLD Register (Offset = 280h) [reset = h]

Short Description: Dst FIFO Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-4409. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0280h
HSM_TPTC01	4706 0280h

Figure 4-2132. HSM_TPTC00_DFCNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-4410. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.34.31 HSM_TPTC00_DFSRCBREF Register (Offset = 284h) [reset = h]

Short Description: Dst FIFO Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4411. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0284h
HSM_TPTC01	4706 0284h

Figure 4-2133. HSM_TPTC00_DFSRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-4412. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Destination FIFO Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.34.32 HSM_TPTC00_DFOPT0 Register (Offset = 300h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-4413. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0300h
HSM_TPTC01	4706 0300h

Figure 4-2134. HSM_TPTC00_DFOPT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-4414. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.33 HSM_TPTC00_DFSRC0 Register (Offset = 304h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-4415. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0304h
HSM_TPTC01	4706 0304h

Figure 4-2135. HSM_TPTC00_DFSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4416. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.34.34 HSM_TPTC00_DFACNT0 Register (Offset = 308h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-4417. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0308h
HSM_TPTC01	4706 0308h

Figure 4-2136. HSM_TPTC00_DFACNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4418. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.34.35 HSM_TPTC00_DFDST0 Register (Offset = 30Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-4419. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 030Ch
HSM_TPTC01	4706 030Ch

Figure 4-2137. HSM_TPTC00_DFDST0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4420. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.34.36 HSM_TPTC00_DFBIDX0 Register (Offset = 310h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4421. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0310h
HSM_TPTC01	4706 0310h

Figure 4-2138. HSM_TPTC00_DFBIDX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4422. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.37 HSM_TPTC00_DFMPPRXY0 Register (Offset = 314h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4423. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0314h
HSM_TPTC01	4706 0314h

Figure 4-2139. HSM_TPTC00_DFMPPRXY0 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4424. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.38 HSM_TPTC00_DFBCNT0 Register (Offset = 318h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-4425. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0318h
HSM_TPTC01	4706 0318h

Figure 4-2140. HSM_TPTC00_DFBCNT0 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4426. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.34.39 HSM_TPTC00_DFOPT1 Register (Offset = 340h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-4427. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0340h
HSM_TPTC01	4706 0340h

Figure 4-2141. HSM_TPTC00_DFOPT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-4428. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.40 HSM_TPTC00_DFSRC1 Register (Offset = 344h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-4429. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0344h
HSM_TPTC01	4706 0344h

Figure 4-2142. HSM_TPTC00_DFSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4430. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.34.41 HSM_TPTC00_DFACNT1 Register (Offset = 348h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-4431. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0348h
HSM_TPTC01	4706 0348h

Figure 4-2143. HSM_TPTC00_DFACNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4432. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.34.42 HSM_TPTC00_DFDST1 Register (Offset = 34Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-4433. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 034Ch
HSM_TPTC01	4706 034Ch

Figure 4-2144. HSM_TPTC00_DFDST1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4434. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.34.43 HSM_TPTC00_DFBIDX1 Register (Offset = 350h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4435. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0350h
HSM_TPTC01	4706 0350h

Figure 4-2145. HSM_TPTC00_DFBIDX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4436. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.44 HSM_TPTC00_DFMPPRXY1 Register (Offset = 354h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4437. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0354h
HSM_TPTC01	4706 0354h

Figure 4-2146. HSM_TPTC00_DFMPPRXY1 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4438. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.45 HSM_TPTC00_DFBCNT1 Register (Offset = 358h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-4439. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0358h
HSM_TPTC01	4706 0358h

Figure 4-2147. HSM_TPTC00_DFBCNT1 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4440. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.34.46 HSM_TPTC01_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-4441. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0000h
HSM_TPTC01	4706 0000h

Figure 4-2148. HSM_TPTC01_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		NONE		RO											
1		0		0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
1				11				0		1					

Access Types Legend

Table 4-4442. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
	RESERVED	NONE		Reserved
27 - 16	FUNC	RO	0h	Function indicates a software compatible module family.
15 - 11	RTL	RO	1h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	1h	Minor Revision

4.34.47 HSM_TPTC01_TCCFG Register (Offset = 4h) [reset = h]

Short Description: TC Configuration Register

Long Description:

Return to Summary Table

Table 4-4443. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0004h
HSM_TPTC01	4706 0004h

Figure 4-2149. HSM_TPTC01_TCCFG Name Register

15	14	13	12	11	10	9	8
RESERVED						DREGDEPTH	
NONE						RO	
0						10	
7	6	5	4	3	2	1	0
RESERVED		BUSWIDTH		RESERVED		FIFOSIZE	
NONE		RO		NONE		RO	
0		10		0		100	

Access Types Legend

Table 4-4444. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 8	DREGDEPTH	RO	Ah	Dst Register FIFO Depth Parameterization
	RESERVED	NONE		Reserved
5 - 4	BUSWIDTH	RO	Ah	Bus Width Parameterization
	RESERVED	NONE		Reserved
2 - 0	FIFOSIZE	RO	64h	Fifo Size Parameterization

4.34.48 HSM_TPTC01_TCSTAT Register (Offset = 100h) [reset = h]

Short Description: TC Status Register

Long Description:

Return to Summary Table

Table 4-4445. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0100h
HSM_TPTC01	4706 0100h

Figure 4-2150. HSM_TPTC01_TCSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED		DFSTRTPTR		RESERVED			ACTV
NONE		RO		NONE			RO
0		0		0			1
7	6	5	4	3	2	1	0
RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE	RO			NONE	RO	RO	RO
0	0			0	0	0	0

Access Types Legend

Table 4-4446. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 12	DFSTRTPTR	RO	0h	Dst FIFO Start PointerRepresents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
	RESERVED	NONE		Reserved
8	ACTV	RO	1h	Channel ActiveChannel Active is a logical-OR of each of the BUSY/ ACTV signals. The ACTV bit must remain high through the life of a TR.ACTV = 0 : Channel is idle.ACTV = 1 : Channel is busy.
	RESERVED	NONE		Reserved
6 - 4	DSTACTV	RO	0h	Destination Active StateSpecifies the number of TRs that are resident in the Dst Register FIFO at a given instant.Legal values are constrained by the DSTREGDEPTH parameter.
	RESERVED	NONE		Reserved
2	WSACTV	RO	0h	Write Status ActiveWSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands.WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	RO	0h	Source Active StateSRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	RO	0h	Program Register Set BusyPROGBUSY = 0 : Prog set idle and is available for programming.PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

4.34.49 HSM_TPTC01_INTSTAT Register (Offset = 104h) [reset = h]

Short Description: Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-4447. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0104h
HSM_TPTC01	4706 0104h

Figure 4-2151. HSM_TPTC01_INTSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RO	RO
0						0	0

Access Types Legend

Table 4-4448. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RO	0h	TR Done Event Status:TRDONE = 0 : Condition not detected.TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	RO	0h	Program Set Empty Event Status:PROGEMPTY = 0 : Condition not detected.PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

4.34.50 HSM_TPTC01_INTEN Register (Offset = 108h) [reset = h]

Short Description: Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-4449. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0108h
HSM_TPTC01	4706 0108h

Figure 4-2152. HSM_TPTC01_INTEN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						RW	RW
0						0	0

Access Types Legend

Table 4-4450. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RW	0h	TR Done Event Enable:INTEN.TRDONE = 0 : TRDONE Event is disabled.INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	RW	0h	Program Set Empty Event Enable:INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled.INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

4.34.51 HSM_TPTC01_INTCLR Register (Offset = 10Ch) [reset = h]

Short Description: Interrupt Clear Register

Long Description:

Return to Summary Table

Table 4-4451. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 010Ch
HSM_TPTC01	4706 010Ch

Figure 4-2153. HSM_TPTC01_INTCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4452. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	WO	0h	TR Done Event Clear:INTCLR.TRDONE = 0 : Writes of '0' have no effect.INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	WO	0h	Program Set Empty Event Clear:INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect.INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

4.34.52 HSM_TPTC01_INTCMD Register (Offset = 110h) [reset = h]

Short Description: Interrupt Command Register

Long Description:

Return to Summary Table

Table 4-4453. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0110h
HSM_TPTC01	4706 0110h

Figure 4-2154. HSM_TPTC01_INTCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4454. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC interrupt:Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC interruptWrite of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.Writes of '0' have no affect.

4.34.53 HSM_TPTC01_ERRSTAT Register (Offset = 120h) [reset = h]

Short Description: Error Status Register

Long Description:

Return to Summary Table

Table 4-4455. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0120h
HSM_TPTC01	4706 0120h

Figure 4-2155. HSM_TPTC01_ERRSTAT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RO	RO	NONE	RO
0				0	0	0	0

Access Types Legend

Table 4-4456. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RO	0h	MMR Address Error:MMRAERR = 0 : Condition not detected.MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	RO	0h	TR Error:TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
	RESERVED	NONE		Reserved
0	BUSERR	RO	0h	Bus Error Event:BUSERR = 0: Condition not detected.BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

4.34.54 HSM_TPTC01_ERREN Register (Offset = 124h) [reset = h]

Short Description: Error Enable Register

Long Description:

Return to Summary Table

Table 4-4457. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0124h
HSM_TPTC01	4706 0124h

Figure 4-2156. HSM_TPTC01_ERREN Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				RW	RW	NONE	RW
0				0	0	0	0

Access Types Legend

Table 4-4458. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RW	0h	Interrupt enable for ERRSTAT.MMRAERR:ERREN.MMRAERR = 0 : BUSERR is disabled.ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	RW	0h	Interrupt enable for ERRSTAT.TRERR:ERREN.TRERR = 0 : BUSERR is disabled.ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
	RESERVED	NONE		Reserved
0	BUSERR	RW	0h	Interrupt enable for ERRSTAT.BUSERR:ERREN.BUSERR = 0 : BUSERR is disabled.ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

4.34.55 HSM_TPTC01_ERRCLR Register (Offset = 128h) [reset = h]

Short Description: Error Clear Register

Long Description:

Return to Summary Table

Table 4-4459. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0128h
HSM_TPTC01	4706 0128h

Figure 4-2157. HSM_TPTC01_ERRCLR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				WO	WO	NONE	WO
0				0	0	0	0

Access Types Legend

Table 4-4460. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	WO	0h	Interrupt clear for ERRSTAT.MMRAERR:ERRCLR.MMRAERR = 0 : Writes of '0' have no effect.ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	WO	0h	Interrupt clear for ERRSTAT.TRERR:ERRCLR.TRERR = 0 : Writes of '0' have no effect.ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
	RESERVED	NONE		Reserved
0	BUSERR	WO	0h	Interrupt clear for ERRSTAT.BUSERR:ERRCLR.BUSERR = 0 : Writes of '0' have no effect.ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

4.34.56 HSM_TPTC01_ERRDET Register (Offset = 12Ch) [reset = h]

Short Description: Error Details Register

Long Description:

Return to Summary Table

Table 4-4461. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 012Ch
HSM_TPTC01	4706 012Ch

Figure 4-2158. HSM_TPTC01_ERRDET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TCCHEN	TCINTEN								
NONE						RO	RO								
0						0	0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TCC						RESERVED				STAT			
NONE		RO						NONE				RO			
0		0						0				0			

Access Types Legend

Table 4-4462. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TCCHEN	RO	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	RO	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
13 - 8	TCC	RO	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
3 - 0	STAT	RO	0h	Transaction Status:Stores the non-zero status/error code that was detected on the read status or write status bus.MS-bit effectively serves as the read vs. write error code.If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.Encoding of errors matches the CBA spec.

4.34.57 HSM_TPTC01_ERRCMD Register (Offset = 130h) [reset = h]

Short Description: Error Command Register

Long Description:

Return to Summary Table

Table 4-4463. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0130h
HSM_TPTC01	4706 0130h

Figure 4-2159. HSM_TPTC01_ERRCMD Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						WO	WO
0						0	0

Access Types Legend

Table 4-4464. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC error interrupt:Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC error interruptWrite of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.Writes of '0' have no affect.

4.34.58 HSM_TPTC01_RDRATE Register (Offset = 140h) [reset = h]

Short Description: Read Rate Register

Long Description:

Return to Summary Table

Table 4-4465. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0140h
HSM_TPTC01	4706 0140h

Figure 4-2160. HSM_TPTC01_RDRATE Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED					RDRATE		
NONE					RW		
0					0		

Access Types Legend

Table 4-4466. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RDRATE	RW	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

4.34.59 HSM_TPTC01_POPT Register (Offset = 200h) [reset = h]

Short Description: Prog Set Options

Long Description:

Return to Summary Table

Table 4-4467. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0200h
HSM_TPTC01	4706 0200h

Figure 4-2161. HSM_TPTC01_POPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-4468. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.60 HSM_TPTC01_PSRC Register (Offset = 204h) [reset = h]

Short Description: Prog Set Src Address

Long Description:

Return to Summary Table

Table 4-4469. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0204h
HSM_TPTC01	4706 0204h

Figure 4-2162. HSM_TPTC01_PSRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RW															
0															

Access Types Legend

Table 4-4470. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RW	0h	Source address for Program Register Set

4.34.61 HSM_TPTC01_PCNT Register (Offset = 208h) [reset = h]

Short Description: Prog Set Count

Long Description:

Return to Summary Table

Table 4-4471. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0208h
HSM_TPTC01	4706 0208h

Figure 4-2163. HSM_TPTC01_PCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BCNT															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RW															
0															

Access Types Legend

Table 4-4472. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15 - 0	ACNT	RW	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.34.62 HSM_TPTC01_PDST Register (Offset = 20Ch) [reset = h]

Short Description: Prog Set Dst Address

Long Description:

Return to Summary Table

Table 4-4473. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 020Ch
HSM_TPTC01	4706 020Ch

Figure 4-2164. HSM_TPTC01_PDST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RW															
0															

Access Types Legend

Table 4-4474. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RW	0h	Destination address for Program Register Set

4.34.63 HSM_TPTC01_PBIDX Register (Offset = 210h) [reset = h]

Short Description: Prog Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4475. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0210h
HSM_TPTC01	4706 0210h

Figure 4-2165. HSM_TPTC01_PBIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RW															
0															

Access Types Legend

Table 4-4476. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Dest B-Idx for Program Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RW	0h	Source B-Idx for Program Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.64 HSM_TPTC01_PMPPRXY Register (Offset = 214h) [reset = h]

Short Description: Prog Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4477. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0214h
HSM_TPTC01	4706 0214h

Figure 4-2166. HSM_TPTC01_PMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4478. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.65 HSM_TPTC01_SAOPT Register (Offset = 240h) [reset = h]

Short Description: Src Actv Set Options

Long Description:

Return to Summary Table

Table 4-4479. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0240h
HSM_TPTC01	4706 0240h

Figure 4-2167. HSM_TPTC01_SAOPT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-4480. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.66 HSM_TPTC01_SASRC Register (Offset = 244h) [reset = h]

Short Description: Src Actv Set Src Address

Long Description:

Return to Summary Table

Table 4-4481. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0244h
HSM_TPTC01	4706 0244h

Figure 4-2168. HSM_TPTC01_SASRC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4482. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address for Source Active Register Set

4.34.67 HSM_TPTC01_SACNT Register (Offset = 248h) [reset = h]

Short Description: Src Actv Set A-Count

Long Description:

Return to Summary Table

Table 4-4483. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0248h
HSM_TPTC01	4706 0248h

Figure 4-2169. HSM_TPTC01_SACNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4484. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

4.34.68 HSM_TPTC01_SADST Register (Offset = 24Ch) [reset = h]

Short Description: Src Actv Set Dst Address

Long Description:

Return to Summary Table

Table 4-4485. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 024Ch
HSM_TPTC01	4706 024Ch

Figure 4-2170. HSM_TPTC01_SADST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4486. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Source Active Register Set

4.34.69 HSM_TPTC01_SABIDX Register (Offset = 250h) [reset = h]

Short Description: Src Actv Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4487. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0250h
HSM_TPTC01	4706 0250h

Figure 4-2171. HSM_TPTC01_SABIDX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4488. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Source Active Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Source B-Idx for Source Active Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.70 HSM_TPTC01_SAMPPRXY Register (Offset = 254h) [reset = h]

Short Description: Src Actv Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4489. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0254h
HSM_TPTC01	4706 0254h

Figure 4-2172. HSM_TPTC01_SAMPPRXY Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4490. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.71 HSM_TPTC01_SACNTRLD Register (Offset = 258h) [reset = h]

Short Description: Src Actv Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-4491. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0258h
HSM_TPTC01	4706 0258h

Figure 4-2173. HSM_TPTC01_SACNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-4492. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.34.72 HSM_TPTC01_SASRCBREF Register (Offset = 25Ch) [reset = h]

Short Description: Src Actv Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4493. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 025Ch
HSM_TPTC01	4706 025Ch

Figure 4-2174. HSM_TPTC01_SASRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-4494. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Source Active Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.34.73 HSM_TPTC01_SADSTBREF Register (Offset = 260h) [reset = h]

Short Description: Src Actv Set Dst Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4495. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0260h
HSM_TPTC01	4706 0260h

Figure 4-2175. HSM_TPTC01_SADSTBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF															
RO															
0															

Access Types Legend

Table 4-4496. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDRBREF	RO	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

4.34.74 HSM_TPTC01_SABCNT Register (Offset = 264h) [reset = h]

Short Description: Src Actv Set B-Count

Long Description:

Return to Summary Table

Table 4-4497. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0264h
HSM_TPTC01	4706 0264h

Figure 4-2176. HSM_TPTC01_SABCNT Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4498. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Dimension count:Number of arrays to be transferred where each array is ACNT in length.Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

4.34.75 HSM_TPTC01_DFCNTRLD Register (Offset = 280h) [reset = h]

Short Description: Dst FIFO Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-4499. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0280h
HSM_TPTC01	4706 0280h

Figure 4-2177. HSM_TPTC01_DFCNTRLD Name Register

15	14	13	12	11	10	9	8
ACNTRLD							
RO							
0							
7	6	5	4	3	2	1	0
ACNTRLD							
RO							
0							

Access Types Legend

Table 4-4500. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

4.34.76 HSM_TPTC01_DFSRCBREF Register (Offset = 284h) [reset = h]

Short Description: Dst FIFO Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-4501. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0284h
HSM_TPTC01	4706 0284h

Figure 4-2178. HSM_TPTC01_DFSRCBREF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDRBREF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF															
RO															
0															

Access Types Legend

Table 4-4502. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Destination FIFO Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

4.34.77 HSM_TPTC01_DFOPT0 Register (Offset = 300h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-4503. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0300h
HSM_TPTC01	4706 0300h

Figure 4-2179. HSM_TPTC01_DFOPT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED		FWID		RESERVED		PRI		RESERVED		DAM	SAM
RW				NONE		RW		NONE		RW		NONE		RW	RW
0				0		0		0		0		0		0	0

Access Types Legend

Table 4-4504. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.78 HSM_TPTC01_DFSRC0 Register (Offset = 304h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-4505. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0304h
HSM_TPTC01	4706 0304h

Figure 4-2180. HSM_TPTC01_DFSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4506. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.34.79 HSM_TPTC01_DFACNT0 Register (Offset = 308h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-4507. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0308h
HSM_TPTC01	4706 0308h

Figure 4-2181. HSM_TPTC01_DFACNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4508. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.34.80 HSM_TPTC01_DFDST0 Register (Offset = 30Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-4509. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 030Ch
HSM_TPTC01	4706 030Ch

Figure 4-2182. HSM_TPTC01_DFDST0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4510. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.34.81 HSM_TPTC01_DFBIDX0 Register (Offset = 310h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4511. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0310h
HSM_TPTC01	4706 0310h

Figure 4-2183. HSM_TPTC01_DFBIDX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4512. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.82 HSM_TPTC01_DFMPPRXY0 Register (Offset = 314h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4513. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0314h
HSM_TPTC01	4706 0314h

Figure 4-2184. HSM_TPTC01_DFMPPRXY0 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4514. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.83 HSM_TPTC01_DFBCNT0 Register (Offset = 318h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-4515. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0318h
HSM_TPTC01	4706 0318h

Figure 4-2185. HSM_TPTC01_DFBCNT0 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4516. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.34.84 HSM_TPTC01_DFOPT1 Register (Offset = 340h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-4517. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0340h
HSM_TPTC01	4706 0340h

Figure 4-2186. HSM_TPTC01_DFOPT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		DBG_ID		RESERVED					TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE		RW		NONE					RW	NONE	RW	NONE		RW	
0		0		0					0	0	0	0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM
RW				NONE	RW			NONE	RW			NONE		RW	RW
0				0	0			0	0			0		0	0

Access Types Legend

Table 4-4518. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

4.34.85 HSM_TPTC01_DFSRC1 Register (Offset = 344h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-4519. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0344h
HSM_TPTC01	4706 0344h

Figure 4-2187. HSM_TPTC01_DFSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR															
RO															
0															

Access Types Legend

Table 4-4520. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

4.34.86 HSM_TPTC01_DFACNT1 Register (Offset = 348h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-4521. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0348h
HSM_TPTC01	4706 0348h

Figure 4-2188. HSM_TPTC01_DFACNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	ACNT														
NONE	RO														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACNT															
RO															
0															

Access Types Legend

Table 4-4522. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

4.34.87 HSM_TPTC01_DFDST1 Register (Offset = 34Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-4523. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 034Ch
HSM_TPTC01	4706 034Ch

Figure 4-2189. HSM_TPTC01_DFDST1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DADDR															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR															
RO															
0															

Access Types Legend

Table 4-4524. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

4.34.88 HSM_TPTC01_DFBIDX1 Register (Offset = 350h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-4525. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0350h
HSM_TPTC01	4706 0350h

Figure 4-2190. HSM_TPTC01_DFBIDX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DBIDX															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBIDX															
RO															
0															

Access Types Legend

Table 4-4526. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

4.34.89 HSM_TPTC01_DFMPPRXY1 Register (Offset = 354h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-4527. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0354h
HSM_TPTC01	4706 0354h

Figure 4-2191. HSM_TPTC01_DFMPPRXY1 Name Register

15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						RO	RO
0						0	0
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				RO			
0				0			

Access Types Legend

Table 4-4528. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

4.34.90 HSM_TPTC01_DFBCNT1 Register (Offset = 358h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-4529. Instance Table

Instance Name	Physical Address
HSM_TPTC00	4704 0358h
HSM_TPTC01	4706 0358h

Figure 4-2192. HSM_TPTC01_DFBCNT1 Name Register

15	14	13	12	11	10	9	8
BCNT							
RO							
0							
7	6	5	4	3	2	1	0
BCNT							
RO							
0							

Access Types Legend

Table 4-4530. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

Table 4-4531. Access Type Codes

Access Type	Code	Description
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

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