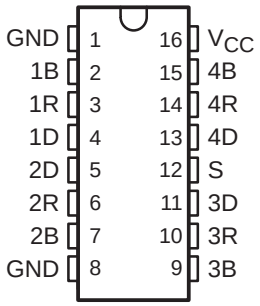
- **Schottky Circuitry for High Speed, Typical Propagation Delay Time . . . 12 ns**
- **Drivers Feature Open-Collector Outputs for Party-Line (Data Bus) Operation**
- **Driver Outputs Can Sink 100 mA at 0.8 V Maximum**
- **pnp Inputs for Minimal Input Loading**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26S10**

D OR N PACKAGE
(TOP VIEW)



description

The AM26S10C is a quadruple bus transceiver utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use pnp transistors to reduce the input loading.

The driver of the AM26S10C is inverting and has two ground connections for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10C is characterized for operation over the temperature range of 0°C to 70°C.

Function Tables

AM26S10C
(transmitting)

INPUTS		OUTPUTS	
S	**D**	**B**	**R**
L	H	L	H
L	L	H	L

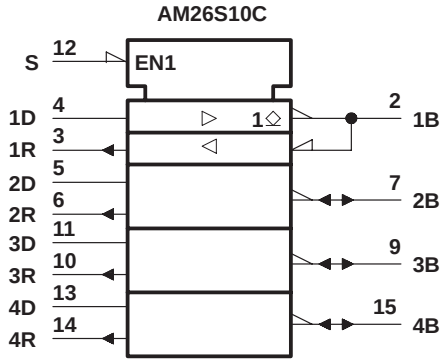
AM26S10C
(receiving)

INPUTS			OUTPUT
S	**B**	**D**	**R**
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

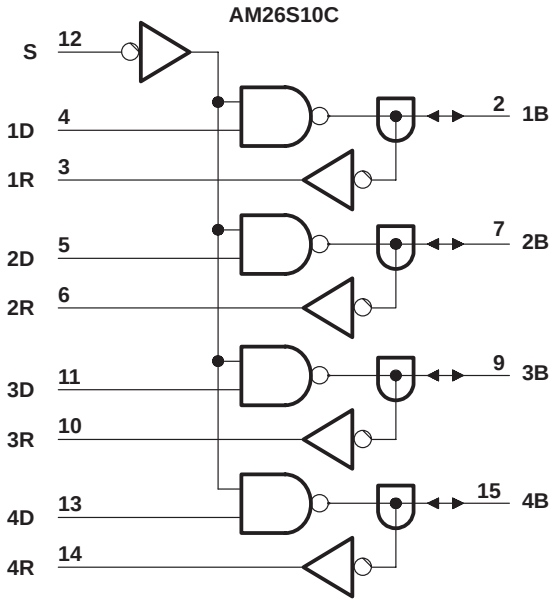
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†

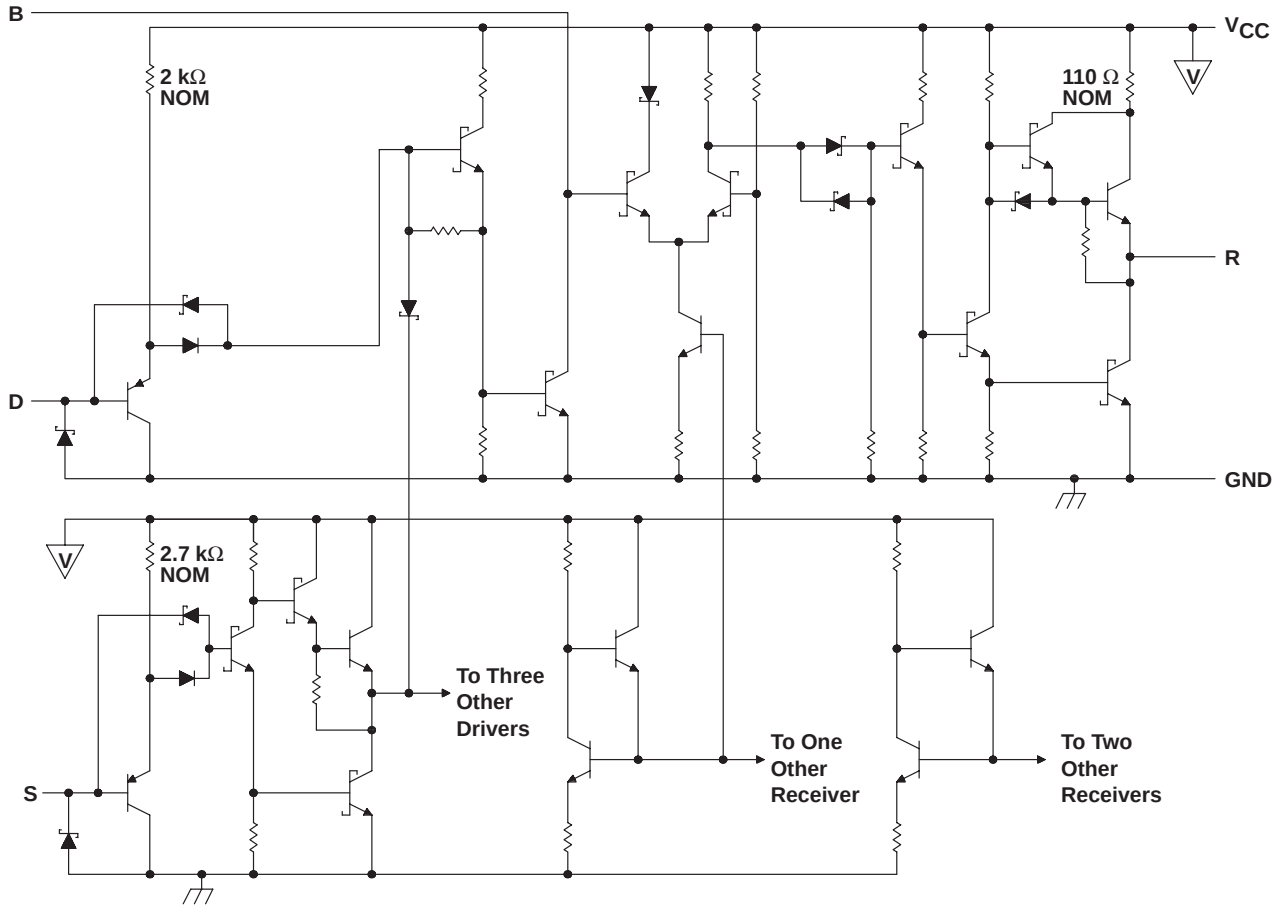


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Driver or strobe input voltage range, V_I . . . . . –0.5 V to 5.5 V
Bus voltage range, driver output off, V_O . . . . . –0.5 V to 5.25 V
Driver or strobe input current range, I_I . . . . . –30 mA to 5 mA
Driver output current, I_O . . . . . 200 mA
Receiver output current, I_O . . . . . 30 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-levael input voltage, V_{IH}	D or S	2			V
	B	2.25			
Low-level input voltage, V_{IL}	D or S			0.8	V
	B			1.75	
Receiver high-level output current, I_{OH}				–1	mA
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			20	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range

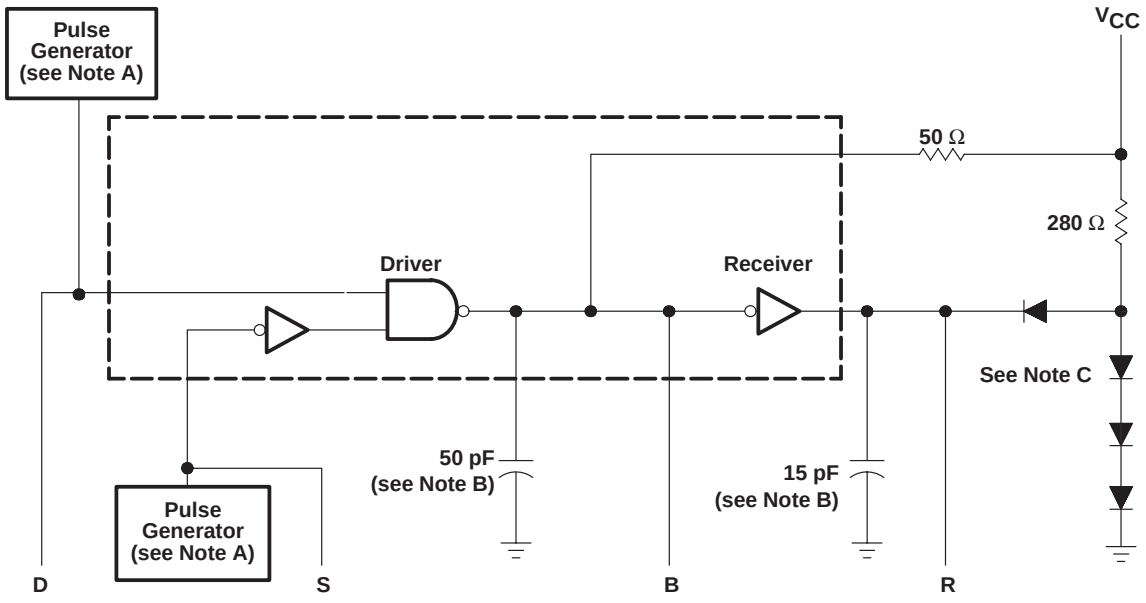
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D or S	V_{CC} = 4.75 V, I_I = –18 mA					–1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = 4.75 V, I_{OH} = –1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.7	3.4		V
V_{OH}	Low-level output voltage	R	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5	V
		B			I_{OL} = 40 mA		0.33	0.5	
					I_{OL} = 70 mA		0.42	0.7	
					I_{OL} = 100 mA		0.51	0.8	
$I_{O(off)}$	Off-stage output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 5.25 V,	V_O = 0.8 V			–50	μA
				V_{CC} = 5.25 V,	V_O = 4.5 V			100	
				V_{CC} = 0,	V_O = 4.5 V			100	
I_{IH}	High-level input current	D	V_{CC} = 5.25 V, V_I = 2.7 V					30	μA
		S						20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = 5.25 V, V_I = 5.5 V					100	μA
I_{IL}	Low-level input current	D	V_{CC} = 5.25 V, V_I = 0.4 V					–0.54	mA
		S						–0.36	
I_{OS}	Short-circuit output current‡	R	V_{CC} = 5.25 V			–18		–60	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, All driver outputs low	Strobe at 0 V,	No load,		45	70	mA
								80	

† All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

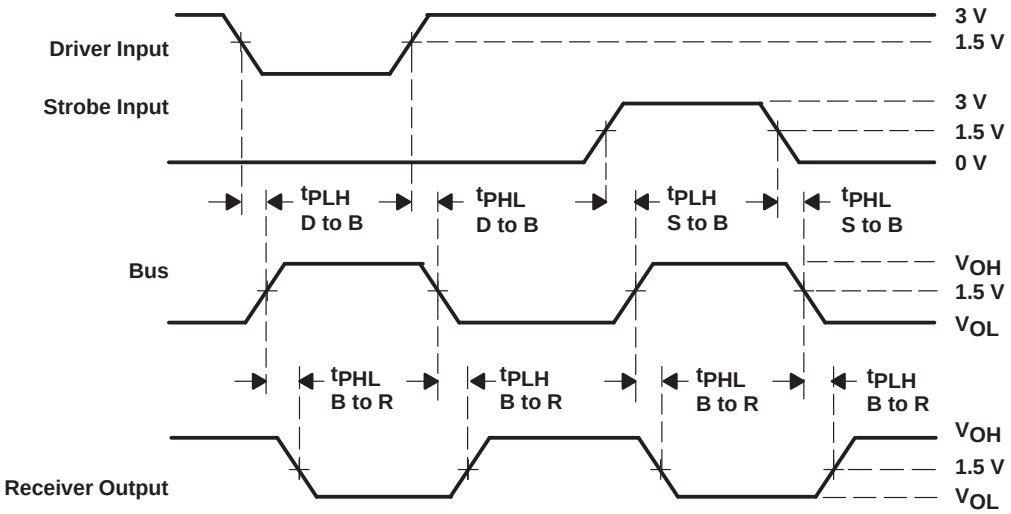
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	AM26S10C			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns.
B. Includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

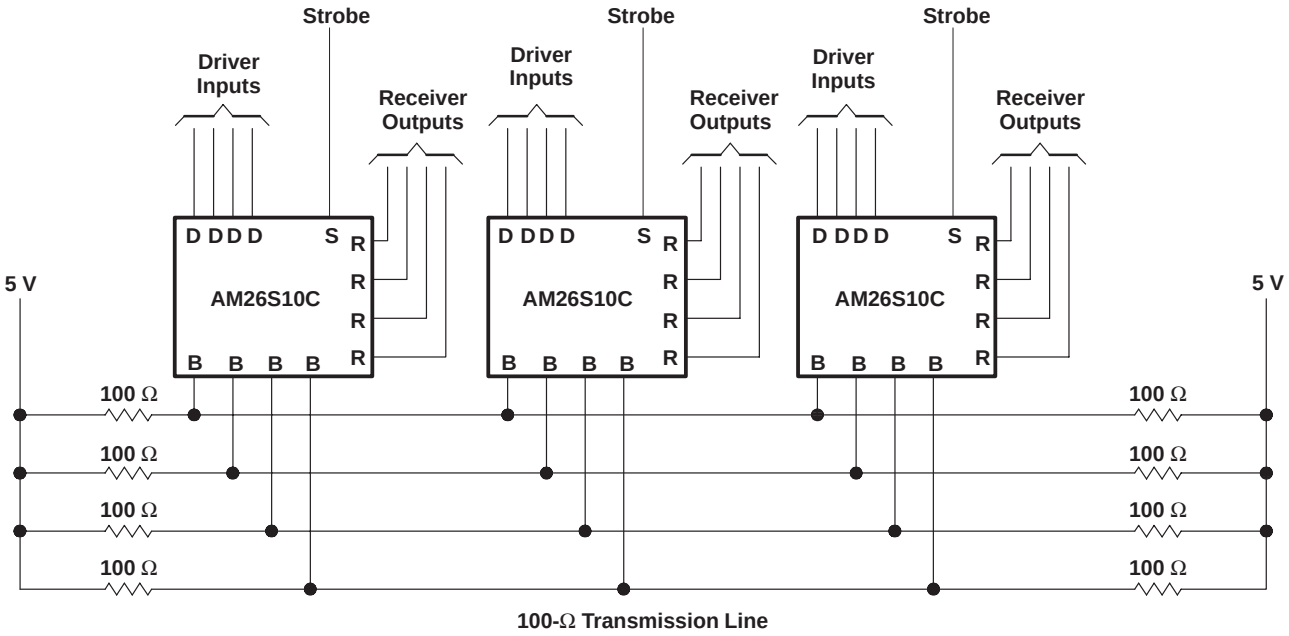


Figure 2. Party-Line System

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26S10CD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26S10C	Samples
AM26S10CDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26S10C	Samples
AM26S10CDRG4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70		Samples
AM26S10CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26S10CN	Samples
AM26S10CNE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26S10CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

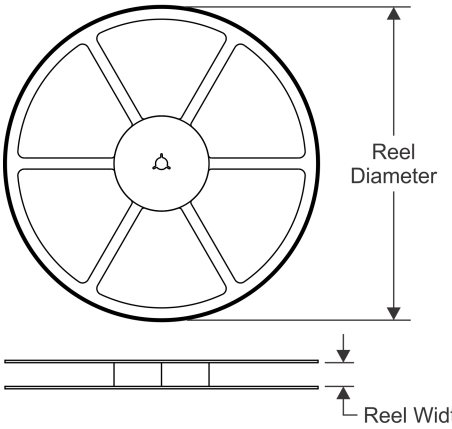
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

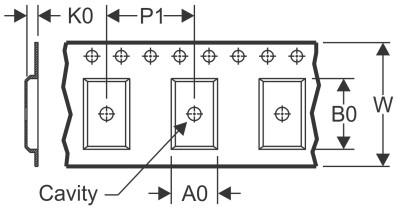
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

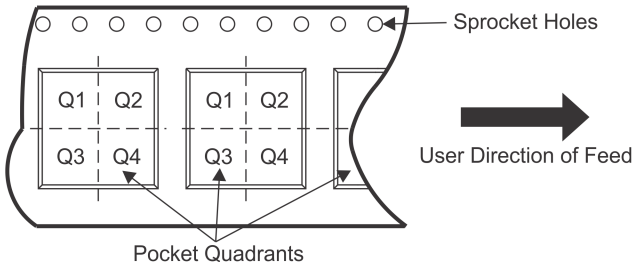


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

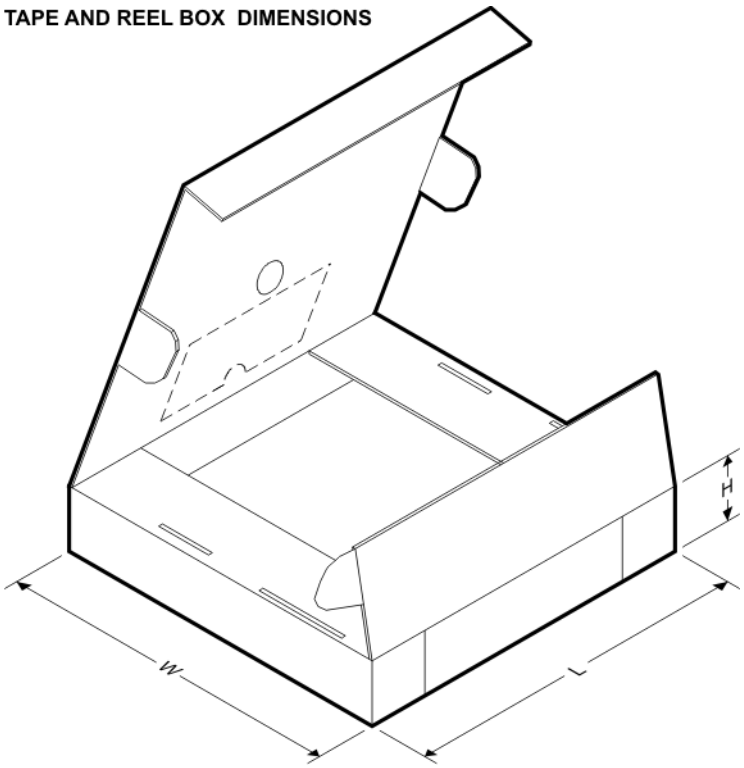
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26S10CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

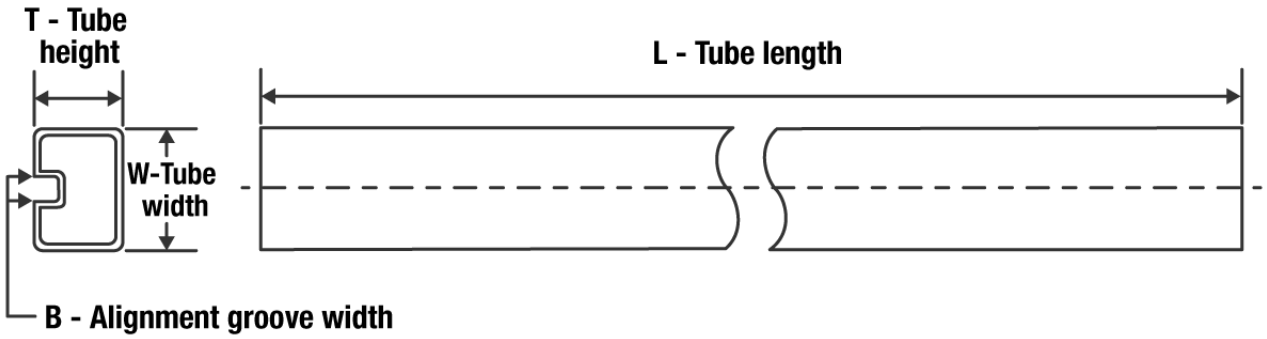
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26S10CDR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



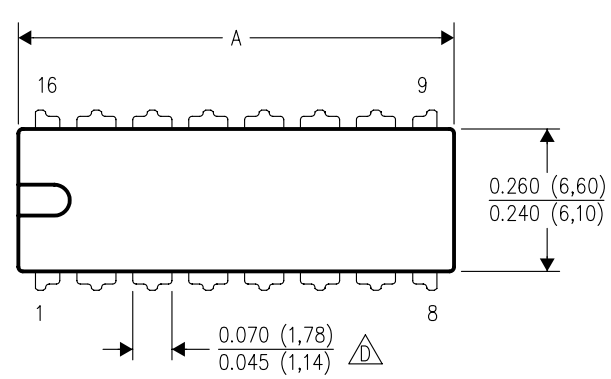
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AM26S10CD	D	SOIC	16	40	507	8	3940	4.32
AM26S10CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26S10CNE4	N	PDIP	16	25	506	13.97	11230	4.32

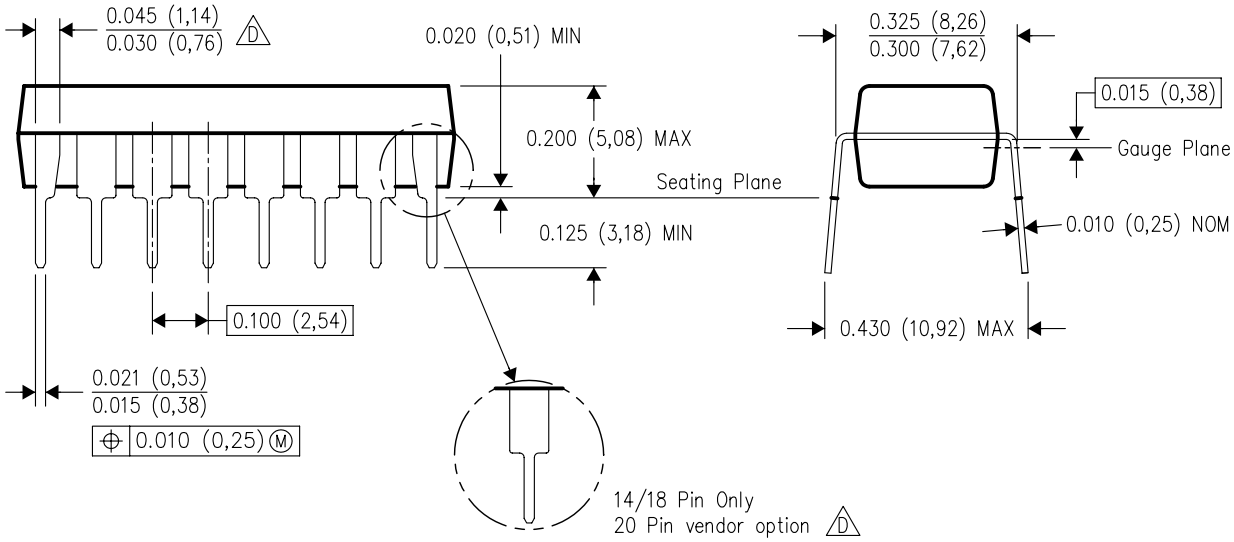
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



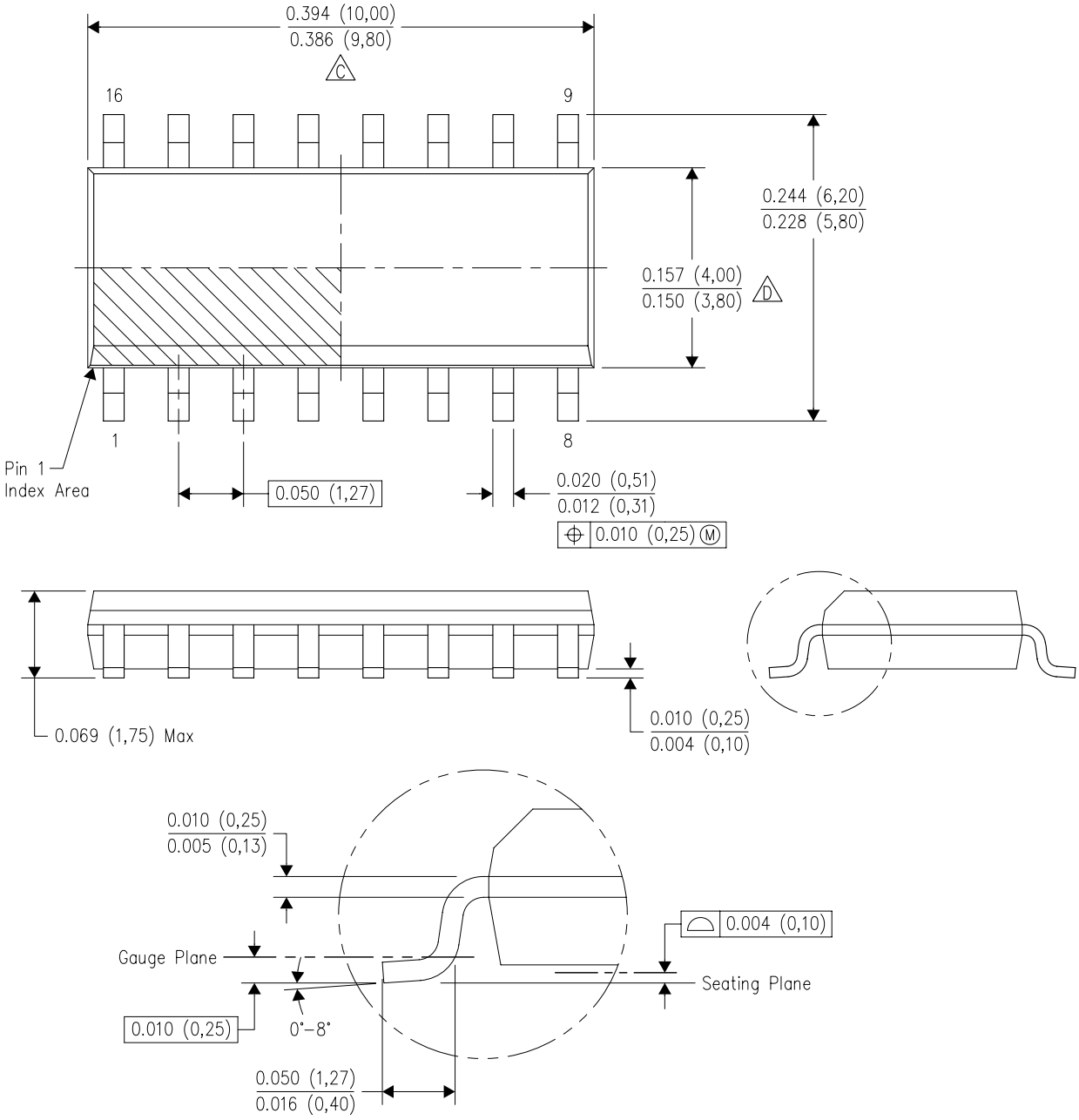
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

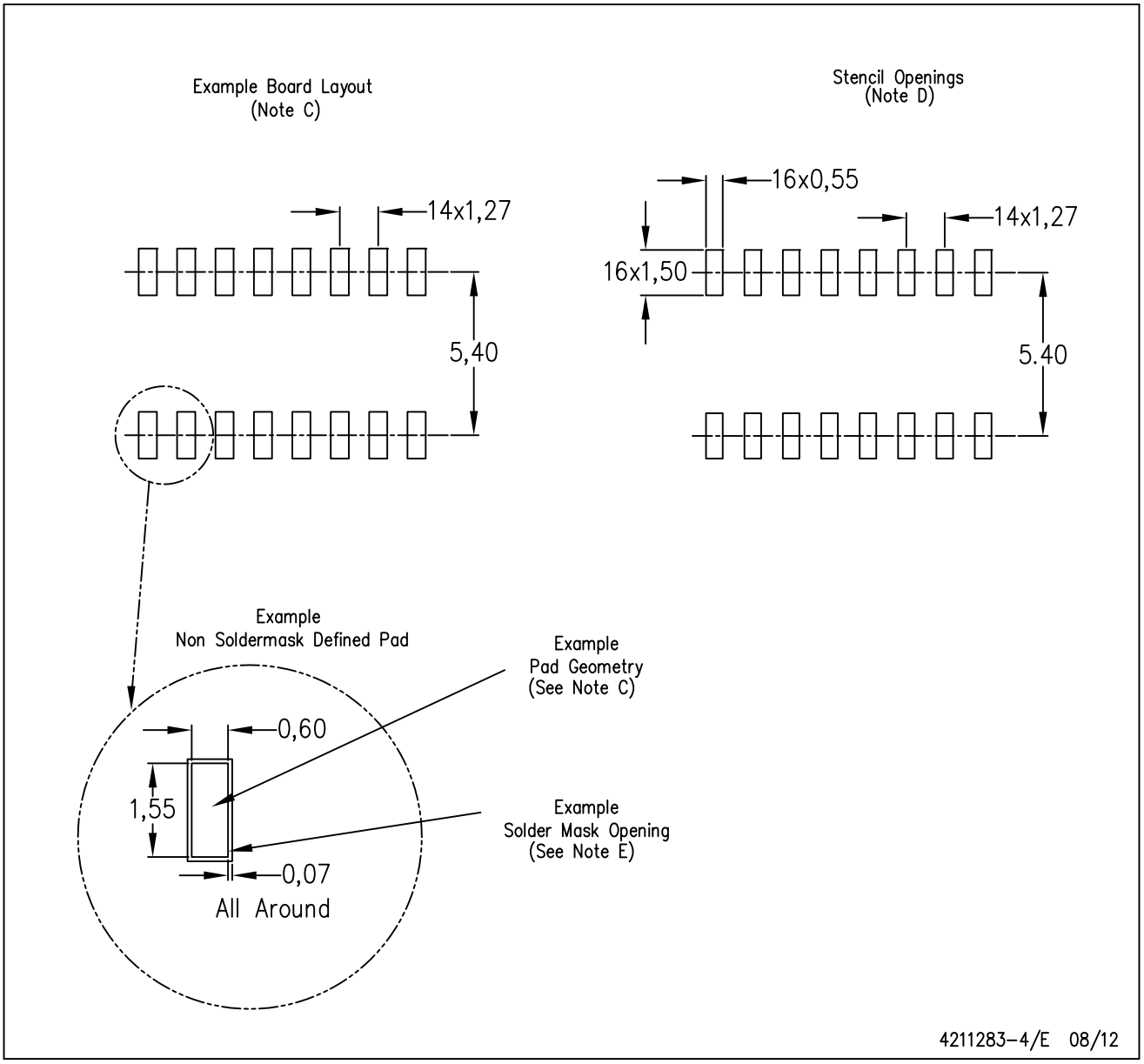
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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