Errata

AM273x Sitara Microcontrollers Silicon Revision 1.0

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories) of the AM273x microcontroller. This document may also contain usage notes. Usage notes decribe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

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1 Usage Notes and Advisories Matrices

Table 1-1 lists all usage notes and the applicable silicon revision(s). Table 1-2 lists all advisories, modules affected, and the applicable silicon revision(s).

Table 1-1. Usage Notes Matrix

NUMBER	TITLE	SILICON REVISIONS AFFECTED
		x.x
Aurora	i2293 - Aurora Interface does not operate at maximum rated frequency if Clock lane is required or in Bypass mode of operation	YES
DSP	i2295 - Memory filter protection within DSP cannot filter access based on PrivID	YES
ESM	i2300 - ESM: nerror gets asserted in safety-enabled test cases when warm reset is asserted multiple times	YES

Table 1-2. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM273x 1.0
Aurora	i2299 - Aurora IP first pattern should not be sync	YES
CSI	i2297 - CSI Careabouts	YES
DMM	i2315 - DMM Careabouts while in Trace mode	YES
	i2318 - DMM cannot write to region which only supports privilege mode writes	YES
DSP	i2298 - DSP PBIST Reset changing DSP L2 clock	YES
DSS	i2289 - Unaligned access from DSS CM4 could cause data integrity failure and hang	YES
EDMA	i2288 - EDMA transfer that spans M1+M2 memories of HWA could result in data corruption	YES
L3	i2294 - Subsequent memory initialisation configuration of L3 Bank D will not trigger a memory initialisation	YES
MDO	i2301 - MDO: SW marker inserted at FIFO threshold location gets missed	YES
	i2302 - MDO: Issue seen in potential interoperability with receiver supporting on Strict Alignment User Flow Control Stripping during overflow message transmission in Aurora 64B/66B Protocol.	YES
	i2309 - MDO: HWA vbusm2ram sniffer address allocation logic is incorrect	YES

Devices Supported

This document supports the following devices:

- AM273x

2 Silicon Revision *1.0* Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

Silicon Revision *1.0* Usage Notes

i2293 ***Aurora Interface does not operate at Max rated frequency if Clock lane is required or in Bypass mode of operation***

Details Below is the Max frequency and Skew

Mode	Value
Aurora - No Clock Lane	Max datarate : 900Mbps Multi lane skew between lanes : 600 ps
Aurora + Clock Lane	Max datarate : 625 Mbps Skew between Data and Clock lane : 230 ps
Bypass + Clock + Frame Clock Lane	Max datarate : 450Mbps Skew between Data/Frame Clock and Clock Lane : 230 ps

Workaround None

i2295 ***Memory filter protection within DSP cannot filter access based on PrivID***

Details Because these bits are tied to 0x0 internally, there is no option to use these signals as attributes for the transfer in memory protection within the DSP.

Workaround None

i2300 ***ESM: nerror gets asserted in safety-enabled test cases when warm reset is asserted multiple times.***

Details Glitches are observed on some ESM error lines just after warm reset is asserted. These glitches get captured in the ESM status registers as valid errors. After de-asserting warm reset, these errors are still pending, since these registers are cleared on power-on reset. When nerror is unmasked, these errors are seen at the nerror PAD.

Workaround To avoid this issue, the safety enable sequence should clear all the ESM status registers at the start.

Silicon Revision *1.0* Advisories

i2288 ***EDMA transfer that spans M1+M2 memories of HWA could result in data corruption***

Details Any EDMA transfer that spans M1+M2 memories of HWA may result in data corruption without any notification of error from the SoC.

As per TPTC IP Spec, a TR is supposed to access a single slave end point. M0/M1 memory banks of HWA are available via single slave point and M2/M3 memory banks of HWA are available as another slave point (different from that of M0/M1). Hence if a single TR is used to access a buffer spanning M1 and M2 memories of the HWA (i.e. a single buffer spanning 2 different slave points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement.

Workaround Split the access into 2 TRs so that a single TR does not span M1+M2. The 2 TRs can be chained.

i2289 ***Unaligned access from DSS CM4 could cause data integrity failure and hang***

Details

The DSS HWA CM4 cannot perform an access to an address space outside its subsystem, which is:

- Not aligned to the 32 bit boundary OR
- Not a multiple of 32 bit such 8/16 bit access

This includes and is not limited to DSP L2, DSS L3, and MSS L2 spaces.

Workaround

Ensure address is 32 bit aligned and accessed in multiples of 32 bit.

DMA the data from L2/L3 to a location inside the HWA CM4 Subsystem and then access from CM4.

i2294 ***Subsequent memory initialisation configuration of L3 Bank D will not trigger a memory initialisation***

Details

Memory initialization for DSS_L3 Bank D is not a write pulse high but read-write bit DSS_CTRL::DSS_L3RAM_MEMINIT_START::L3RAM3_MEMINIT_START

Workaround

To trigger a subsequent memory initialization, write 0x0 to the field before writing 0x1 to trigger memory initialization.

1. Write 0x0 to DSS_CTRL::DSS_L3RAM_MEMINIT_START::L3RAM3_MEMINIT_START
2. Write 0x1 to DSS_CTRL::DSS_L3RAM_MEMINIT_START::L3RAM3_MEMINIT_START

i2297 ***CSI Careabouts***

Details

Data corruption can occur when CSI attempts to make writes to PCR/HWA/HSM/DMM, which are not 8 byte aligned.

Workaround

CSI2 to DMM transfer should be with 1 line ping-pong enabled when DMM is operating in CSI2 mode.

Access from CSI2 to any PCR or HWA or HSM space needs to have 1 of the following constraints:

- CSI2 payload size per line should be multiple of 8 bytes.
- CSI2 should operate in 1-line ping-pong configuration.

i2298 ***DSP PBIST Reset changing DSP L2 clock***

Details

During self-test operation of DSS subsystem by DSP, L2 memories are in functional mode and clock should not be disturbed. PBIST_ST_KEY register has to be set to access PBIST controller. MMR registers are for configuration of memory self-test and control for the select line of the clock mux added on L2 clock path.

Configuring the register will create the glitch at the L2 clock mux as it dynamically switches the select line while both clocks are active.

Workaround

DSP PBIST is done by MSS.

i2299 ***Aurora IP first pattern should not be sync***

Details

Aurora has a feature called sync compression, where one can compress the number of sync patterns sent based on a configuration register value. If the very first frame is a sequence of sync pattern, and the sync pattern compression is configured to n (as

i2299 (continued) ***Aurora IP first pattern should not be sync***

example), then ideally aurora should output only n sync patterns. Due to the bug, only one sync pattern will go as output.

Workaround None

i2301 ***MDO sw marker inserted at FIFO threshold location gets missed***

Details Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the AM273x device and transmit outside over LVDS (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The corresponding sniffer module sniffs a bus interface and accumulates data in the FIFO. When a FIFO threshold is reached, the data is sent out to the aggregator as a burst transfer.

An MDO source can also inject a marker indicator along with its data for tracking or other related purpose. If a marker is inserted such that it is a part of the last element of the FIFO threshold location, it will be missed.

This happens only when a sniffer other than *Sniffer 0* is used for transfer.

Workaround Multiple back to back markers (>1) can be sent out by the user to ensure at least one of them is registered by the receiver. The same sniffer configurations should be programmed to Sniffer 0 registers. This way the markers would be sent out and registered by the receiver. This workaround is only beneficial where Sniffer 0 is not in use and is idle for replicating other sniffer configurations.

Note

These workarounds are only required when using markers in operation. There are no restrictions on the sniffers when markers are not in use.

i2302 ***MDO: Issue seen in potential interoperability with receiver supporting on Strict Alignment User Flow Control Stripping during overflow message transmission in Aurora 64B/66B Protocol.***

Details Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the AM273x device and transmit outside over Aurora LVDS Interface (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The MDO sniffer module is responsible for monitoring the hardware interfaces in the chip and capturing the transactions on the bus which are within the configured addressing region of interest.

Data loss due to overflow can occur at the sniffer. This overflow information is sent as an interrupt to the CPU and the Aurora Tx IP. A User-Flow-Control (UFC) packet is generated by the Aurora TX IP in case of a data overflow condition in order to notify the user of this error condition. This is an error scenario and is not expected to occur in normal transfer functionality. At this stage, the data integrity is already comprised.

Aurora IP only supports UFC packet generation as per Section 6.6 of Aurora 64B/66B Protocol Specification, i.e. the UFC header block precedes the UFC data blocks. Strict Alignment User Flow Control Stripping (refer to Section 6.7 of Aurora 64B/66B Protocol Specification) is currently not supported.

Workaround The input data rate for the MDO should be less than the output data rate so as to keep the effective data rate within the limits to avoid any overflow condition.

i2309 ***MDO - HWA vbusm2ram sniffer address allocation logic is incorrect***

Details For MDO, while sniffing the 128 kB HWA memory, the address allocation for sniffer logic is incorrect, since the address is translated by 512 kB whenever 32kB boundary is crossed:

0 -32KB	no translation
32KB-64KB	address is translated by 512KB [22:19] = [18:15]
64KB-96KB	address is translated by 512KB [22:19] = [18:15]
96KB to 128KB	address is translated by 512KB [22:19] = [18:15]

Workaround While programming the address, snif_waddr[18:15] must be the same as snif_waddr[22:19].

START :END WORKAROUND START :END

0 -32KB 0x00000000:0x00007FFF 0x00000000:0x00007FFF

32KB-64KB 0x00008000: 0x0008FFFF 0x00088000: 0x0008FFFF

64KB-96KB 0x00010000:0x00017FFF 0x00110000:0x00117FFF

96KB to 128KB 0x00018000:0x0001FFFF 0x00198000:0x0019FFFF

i2315 ***DMM Careabouts while in Trace mode***

Details DMM can only support 32 bit/64 bit writes as master on interconnect.

Workaround None

i2318 ***DMM cannot write to region which only supports privilege mode writes***

Details All DMM writes are user-mode writes. DMM cannot write to a region which only supports privilege mode writes. This is applicable for both Trace mode and Direct Data mode.

Workaround None

Trademarks

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2021	Base	Initial Release

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