TEXAS INSTRUMENTS

Application Report
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Thermal Design Guide for DSP and ARM Application Processors

Catalog Processors

ABSTRACT

This application report has been compiled to provide specific information and considerations regarding thermal design requirements for all DSP and ARM-based single and multi-core processors (collectively referred to as “processors”, “System-on-chip”, or “SoC”). The information contained within this document is intended to provide a minimum level of understanding with regards to the thermal requirements and thermal management necessary to assure proper operation of the processor. Failure to establish and maintain the minimum requirements identified within this document (and the related data sheet) can reduce the life, reliability, or performance of the processor. Under certain conditions, exceeding the thermal requirement can permanently damage the processor. In all cases, if the thermal requirements identified in this document and the device-specific data sheets are not met, any warranty - implied or otherwise stated - will be null and void.

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1 Introduction

The processors and application (system) reliability, as well as electrical functionality and performance, is in part determined by the operating temperature under which all logic functions. As process nodes continue to shrink, processors become more complex and power increases, the control of variables such as component temperatures has become more critical to successful designs. Complex and more accurate calculations are performed using common Computational Fluid Dynamic (CFD) tools are strongly recommended by Texas Instruments, especially for complex systems.

2 Thermal Considerations

When designing a system with a high-performance SoC, the following items must be considered during design:

- Maximum power consumption
- Maximum case temperature specification
- Typical thermal resistance from junction-to-ambient (Theta-JA, is normally defined in the device-specific data sheet)
- Understanding that effective Theta-JA can be significantly higher depending on factors such airflow, component orientation, humidity and altitude
- For more information, see the processor-specific power and thermal reports.

2.1 Thermal Metrics

Thermal metrics are provided in the processor data sheet (for example, θ_{JA}, θ_{JC}, θ_{JB} to Ψ_{JB}). These thermal metrics are the result of characterization in accordance with (EIA/JEDEC) standards. Applicable standards and measurement conditions are specified in the data sheet.

For a complete definition and proper application of each thermal metric, see the Semiconductor and IC Package Thermal Metrics.

Thermal metrics in the processor data sheet provide a first-level approximation of system thermal performance. However, first-level approximations cannot replace actual thermal modeling of the system that includes operating environment constraints including but not limited to: projected maximum operating conditions, regulatory requirements, airflow, and so forth.

Processors with special thermal considerations may have specific thermal characterization reports that include data acquired over processor loading schemes at different ambient conditions. These processors generally require thermal considerations as part of the overall system design.

For more information regarding thermal design techniques and terminology if concepts in this document are not clear, see http://www.ti.com/thermal.

3 Thermal Models

Thermal models come in various configurations. Model selection depends on selection criteria and can be limited by the tools available. Models range from a simple 1R (one resistor) model to a more complex multi-resistor model commonly referred to as a network compact or Delphi model. As model complexity increases towards the network compact model, it is typically assumed that the performance and accuracy of the model also increases.

The following section provides an overview of the models commonly provided by TI. Although Texas Instruments recommends and intends to provide Network Compact Thermal models (Delphi) for all Sitara and KeyStone processors and beyond, it is important to understand the relationship and complexities of other common models, especially when constructing a system level simulation model.

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3.1 2R Model

A 2-R (2R or two resistor) model typically incorporates a junction point with two accompanying end points as illustrated in Figure 1. In some cases a 2R model may not include the transistor junction point; this construction typically is reserved for independent analysis of case and or heat sink constructions. For use with the processor and throughout the remainder of this document, a 2R model incorporate a junction point. A 2R model is considered to be a basic model when performing a first approximation thermal analysis.

Figure 1 is provided as a graphical representation for common 2R thermal models.

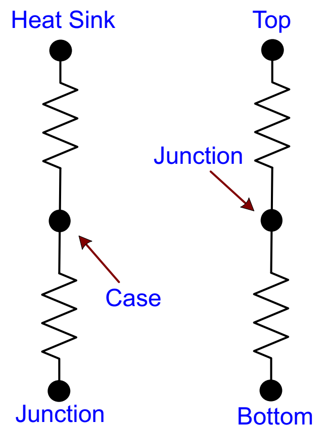

Figure 1. 2R Thermal Resistance Models

3.2 Delphi Compact Network Thermal Resistor Model

Unlike the 2-R model, most network compact models like the Delphi model are mathematical constructs, and not thermal resistances. A Delphi or compact model does not correspond to a specific physical thermal resistance between the two nodes. All Delphi models are designed around vendor (Texas Instruments) internal analysis. The Delphi model is designed to be used with common resistor network solvers, CFD tools, and other system level thermal simulation tools. The Delphi compact model is typically the best representative mode for the processor and typically includes a representation of all the heat conduction paths.

Delphi compact models are what Texas Instruments intends to offer to support processor thermal analysis. With this in mind understanding Delphi models and inherent constraints is necessary. All surface nodes on the Delphi model are by definition associated with only one temperature. Lastly, the Delphi models offered by Texas Instruments will closely approximate the effect on the environment of the actual package.

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Figure 2 is provided as a graphical representation for a common processor Delphi thermal resistance model. This model represents a fully packaged or encapsulated processor.

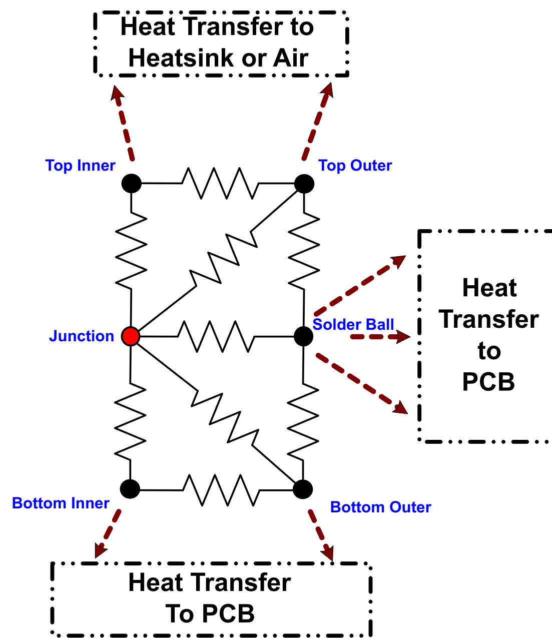

Figure 2. Delphi Compact Thermal Model

4 Tools

There are two basic classifications of thermal modeling tools, each with their own set of limitations and benefits. These include:

- Network calculator tools
- Three dimensional modeling tools

4.1 *Network Calculators*

A network calculator tool uses resistors as network links to develop the entire system. Surface or Top nodes are connected to appropriate nodes within the environment. This is defined in greater detail in the JEDEC Standard, JESD15-3 (*Two-Resistor Compact Thermal Model Guideline*). A network calculator (as with all tools discussed) require you to properly and correctly determine and implement variable factors including environmental conditions and heat capacity of the ambient air to the top node of the model.

4.2 *Three Dimensional Modeling and Simulators*

The second class of tools is referred to as 3D modeling tools. This class is generally defined by both Computational Fluid Dynamics (CFD) and Conduction Modeling (CM) (or non-CFD) tools. Other tools within this class do exist but are not as widely used. This group of tools focuses on heat transfer based on equations in a 3D field using differential equations. Models used within these tools include the Texas Instruments recommended Delphi compact thermal resistance model, which is also further defined in JESD15-4.

Conduction modeling tools are used to solve defining equations for conduction heat transfer within the solid portions of the system. Airflow effects are solved indirectly; they are applied as an equivalent heat transfer coefficient to the solid air (exposed) interfaces of the model (top and sides). Any surface (of the model) in contact with the system board (PCB) or heat sink are managed within the conduction heat transfer calculation.

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CFD tools work to solve both the air and solid portions of the system directly. Heat transfer and fluid flow calculations are based on the Navier-Stokes equations for the exposed sides. As with the conduction modeling tools, any node that contacts a solid utilizes the conduction heat transfer equations and calculations to derive a result. Most all quality CFD tools support transfer analysis for radiation, conduction, and convection of heat. CFD tools, although typically more precise, require correct physical geometries for discrete devices and systems to be accurate.

5 Thermal Variables

Multiple variables directly affect proper thermal measurements and calculations, and these need to be considered. The following sections discuss several of the independent factors to also consider.

5.1 Ambient Temperatures

Theta-JA changes with respect to ambient (surrounding air) temperature changes. This is due to density, viscosity, and heat capacity of the ambient air.

5.2 Power Dissipation

Processor package design also affects the convection, conduction, or radiated energy loss from the BGA package. In general, the higher the temperature on the BGA package surface gets, the more efficient convection, conduction, and radiation heat loss to the ambient environment becomes. As the device power consumption increases, the theta-JA of the implemented solution must get lower to prevent device overheating.

5.3 Altitude

Altitude of the operated product can have a significant effect on theta-JA measurements. Average static air pressure is reduced as the altitude increases, which results in reduced cooling efficiency. Therefore, the higher the altitude, the higher the measured temperature of a like application running under identical conditions. Prior research conducted (by IBM) resulted in a de-rating factor to be applied when operating at various altitudes. The following altitude and multiplication factors shown in Table 1 should also be taken into consideration when operating at various elevations.

Table 1. Multiplication Factor

Altitude (ft/(m))	Multiplication Factor
0 (0)	1.0
3000 (914.4)	1.1
5000 (1524)	1.14
7000 (2133.6)	1.17
8350 (2545.08)	1.2

5.4 Environmental Conditions

The environment surrounding the system is important. Variations in the environment affect the ability to exchange heat originating from the processor and the surrounding circuits. Therefore, the environment surrounding a product can dramatically impact the overall system thermal performance. Care should be taken to design the system for the intended environmental conditions.

5.5 System PCB Design

PCB design can have a large impact on processor thermal management. Design topologies that place complementary components in close proximity to the processor can also contribute to higher junction temperatures. The ability of the processor to properly dissipate power (in the form of heat) through the processor and into the environment as well as through the lid utilizing conduction or convection methods is critical to all designs. For additional detailed information regarding PCB design recommendations, see Section 7.

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5.6 Processor Cooling

The processor can be cooled using one of three common methods:

- Conduction
- Convection
- Radiation

Radiation is the simplest and typically the least effective. A processor resting in place will naturally radiate heat into the environment (assuming the environment is a lower temperature than the processor) until such a time thermal equilibrium is obtained. Radiation as defined and used in this document is the natural radiation or transfer of heat from the processor to the ambient environment. This differs slightly when applying conduction or convection techniques.

Conduction, unlike radiation utilizes an interconnecting object (heat sink, thermal posts, thermal conductive material, and so forth) to conduct heat away from the processor. The most commonly used conduction method is a heat sink. Heat sinks vary in size, construction and attach methods - each will play a large role in defining how well a conduction method works. A heat sink applied directly to the individual processor may not be adequate enough to transfer the necessary amount of heat away. Limiting factors when using strictly conduction include the number and size of heat sink fins, thermal attach material and ambient temperature.

Other common methods of thermal conduction used within processor applications include lid attach and thermally conductive (electrically insulated) materials. Lid attach typically implies an extruded or molded lid that directly comes in contact with the processor and draws heat away from the processor to the external ambient environment. These extruded or molded lid attach devices are rigid. This method typically works well but has several design limitations that must be considered. The thermally conductive lid, depending on tolerances and PCB planarity, can crush the processor. Dissimilar materials have different rates of expansion and contraction - also adding to the potential risk. Alternately, a lid attach design can use an electrically isolated thermally conductive elastomer between the processor and conductive source. This same elastometric material can be used between the processor and the standard thermally conductive lid (non-extruded), but may yield worse results than a direct coupled (with a small thermal pad) lid attach method.

Forced convection, or, natural convection with forced air, typically produces the best results. System enclosures should be designed with airflow in mind, ideally with clear paths for exhaust and inlet air. The PCB should be designed such that forced air is allowed to freely move over the processors for maximum reduction of junction temperature. In a forced convection cooling system, the amount of air flow, internal and external ambient temperatures and static pressure play a large role in determining the junction temperature of the processor. When designing a forced convection cooling system, CFD tools should always be used to determine the optimum design and placement of components. A suitable plenum for air to move with little resistance over the processors provides the best efficiency in a design. Thermal management solutions utilizing forced convection must evaluate fan airflow (CFM) and noise (SPL) on a case-by-case basis to balance design goals and thermal maximum of the processor.

To some degree conduction and radiation are always present in a design, power in the form of heat is conducted away from the processor into the board, and the power or heat within the PCB or processor is naturally radiated into the surrounding environment. The best solution (in an ideal configuration) is a combination of all three methods.

5.6.1 Heat Transfer

There exists several methods for meeting the thermal requirements of the processor, the two most common methods are conduction and convection.

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5.6.1.1 Conduction

Conduction heat transfer refers to the conduction or direct contact between two surfaces resulting in a thermal transfer from one surface (higher temperature) to another (lower temperature). When referring to the cooling of the processor in an application/system this usually involves the direct contact of a heat sink (attached or possibly part of the system enclosure. The thermal heat generated by the processor is transferred to an attached heat sink/outer enclosure thereby reducing the heat (conducting it away) on the processor. In all conduction methods, the material used, compression forces, and ambient temperatures affect the transfer rates. Table 2 defines various material used today and the relative thermal coefficients of each.

Table 2. Thermal Coefficient of Common Materials

Material	Thermal Conductivity W / mK
Air	0.026
Aramide / Epoxy	0.20 - 0.30
Thermal Grease	0.20 - 0.70
Polyimide / E Glass	0.2 - 0.4
E-Glass Fiber	0.3 - 0.4
FR4 / E Glass	0.3 - 0.4
PTFE Ceramic (RO3000)	0.5 - 0.66
Thermal transfer tape	0.6
Non PTFE Ceramic (RO4000)	0.6 - 0.65
Thermally Conductive Silicon Pad	1.6
Thermally Conductive Elastomer	1.1 - 1.9
Doped Thermal Grease	1.68 - 2.58
Thermally Conductive Acrylic Pad	2.0 - 3.0
Soft Thermally Conductive Silicon Pad	3.1
Thermally Conductive Silicon/Ceramic Pad	1.0 - 4.1
Natural Graphite Thermal Pad	6 - 10
Low Modulus Carbon Fiber	8 - 12
Natural Graphite Thermal Pad + Polymer	16
High Modulus Carbon Fiber	300 - 325
Heavy Copper	385-400

5.6.1.2 Convection

Convection refers to the thermal transfer of heat from one object (processor) to the ambient environment typically by means of air movement (fan). Convection or air movement can be pulled or pushed across the processor depending on the application. If a fan is attached to the processor, the direction is usually to force the air away from the processor; whereas; if the system or application board includes external cooling fans, the air direction can be either direction (push or pull). Air movement in any enclosure in involves a plenum whether intended or not, it is always best to optimize the air movement to maximize the effects and minimize any excessive back pressure on the fan (to maximize fan life and reduce noise).

6 Thermal Equations

The following is a summary of equations used to approximate relative junction temperatures of the processor.

For more complete thermal metric application and calculation methods, see Semiconductor and IC Package Thermal Metrics.

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A simplified representation of the thermal path from the junction of the die through both the top and bottom of the package is given. As shown in Figure 3, the thermal path can be modeled as an equivalent electrical circuit. In this approach, power in watts is equivalent to current in amps, temperature delta in degrees is equivalent to Voltage drop, and thermal resistance in C/W is equivalent to electrical resistance in Ω. Therefore, a thermal resistance can be calculated as the temperature delta between node X and node Y, divided by the power.

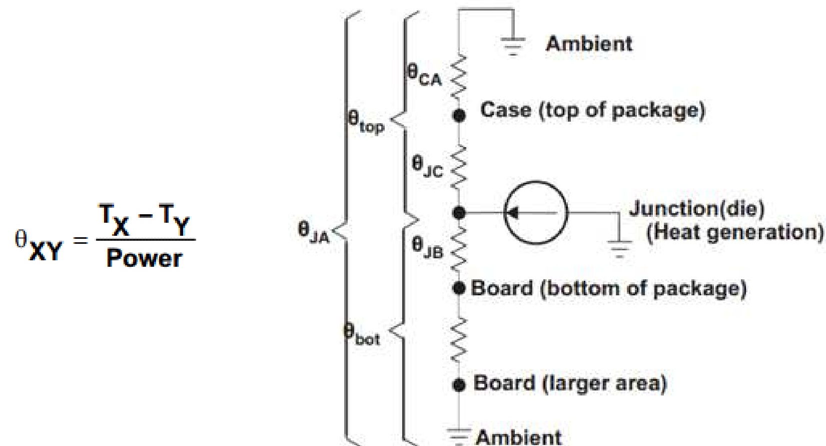

Figure 3. Thermal Path

The resistances of Figure 3 relate to the thermal resistances of the package and system as follows:

- $\theta_{JA,effective}$, : Total resistance of the whole system from die (junction) to ambient air
- Total thermal resistance through the top (θ_{top}) of processor to environment (including heat sink if used)
- Total thermal resistance through the bottom (θ_{bot}) of processor and PCB to environment
- θ_{CA} : Resistance from top of processor through air or heat sink to environment
- θ_{JC} : Resistance from die (junction) to the top of the package (case)
- θ_{JB} : Resistance from die (junction) to the board (near the processor), as defined by JESD 51-8. The resistances θ_{top},

The resistances θ_{top}, θ_{bot}, and θ_{CA} are not defined in the device-specific data manual but are mentioned here because they are useful in heat sink calculations.

6.1 θ_{JC} – Improved Junction Temperature With Heat Sink

Junction Temperature - Simple System Calculation With Heat Sink

$$T_{JUNCTION} = T_{AMBIENT} + (\theta_{JC} + \theta_{CS} + \theta_{SA}) \times Power \quad (1)$$

- ***Theta-CS (θ_{CS})***

  Theta-CS is the thermal resistance of the thermal interface material (TIM) between the processor case/ lid and heatsink.

- ***Theta-SA (θ_{SA})***

  Theta-SA is the thermal resistance of the heat sink. This value should come from your heat sink manufacturer (this value is highly dependent on airflow rate).

This calculation represents the preferred equation to be used when performing simple calculations on junction temperatures where a heat sink exists. This equation is recommended and most accurate for packages where θ_{JC} is small compared to θ_{JA}. This equation is recommended for processor applications where the majority of the heat can be dissipated through the lid of the package when an efficient heat sink is utilized.

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6.2 θ_{JC} – Improved Junction Temperature With Heat Sink – Complex Systems

Junction Temperature - Complex System Calculations With Heat Sinks

$$T_{FUNCTION} \cong T_{AMBIENT} + \left(\frac{\theta_{JA} \times (\theta_{JC} + \theta_{CS}\ \theta_{SA})}{\theta_{JA} + \theta_{JC} + \theta_{CS}\ \theta_{SA}} \right) \times Power \quad (2)$$

6.3 Ψ_{JT}

Calculated thermal resistance model:

$$T_{JUNCTION} = T_{CASE} + (\Psi_{JT} * Power) \quad (3)$$

Psi-JT or Ψ_{JT} is the thermal characterization parameter between junction to top. Top (or T_{TOP}) is the temperature at the top center of the package. The term power refers to total heat dissipated from the processor through any thermal path and not just the lid or case. Equation 4 can also be substituted when using the Psi-JT method:

$$\Psi_{JT} = (T_J - T_{TOP}) / Power \quad (4)$$

6.4 Ψ_{JB}

Calculated thermal resistance model:

$$T_{JUNCTION} = T_{BOARD} + (\Psi_{JB} * Power) \quad (5)$$

Psi_{JB} or Ψ_{JB} is the thermal characterization parameter between junction to board. Board refers to the temperature at the bottom center of the mounting surface. The term power refers to total heat dissipated from the processor through any thermal path and not just the lid or case. Equation 6 can also be substituted when using the Psi-JT method:

$$\Psi_{JB} = (T_J - T_{BOARD}) / Power \quad (6)$$

7 PCB Thermal Design Considerations

Processors and application (system) reliability, as well as electrical functionality and performance, is in part determined by the operating temperature under which all logic functions. As process nodes continue to shrink, processors become more complex and power increases, the control of variables such as component temperatures has become more critical to successful designs.

Independent variables (factors) that can be controlled and impact the processor temperature include: operating power, surrounding air flow, heat sources (peripheral components), orientation, internal and external system ambient temperatures, layout topologies and assembly board material (PCB or PWB). Printed circuit board design factors would include the width and thickness of the copper (Cu) trace contacting each of the component pins (balls, legs, pad, and so forth), the number and area of copper planes that connect to each, thermal vias that may be designed between them and the spreading planes, and the proximity of other components or heat generating sources.

Proper thermal design to control processor temperature requires consideration and implementation of factors that promote energy flow. It is impossible to reduce the requirements for proper thermal management to a single formula given all the possible variables and design permutations. The complex interactions between constraints and variables requires application level software programs and 3-D models to be constructed in order to get to an accurate approximation.

7.1 PCB Material Used as a Heat Sink

The printed circuit board or PCB can be thought of as a heat sink to which is soldered the individual processor balls or the legs (leads). The PCB construction, and the design and layout of your PCB, can significantly impact its efficiency as a heat sink. Figure 4 illustrates a typical application, whereby, a processor is mounted on the top of the PCB and connected via solder balls and a process is mounted on the bottom of the PCB via soldered legs. Figure 4 illustrates how heat is generated and transferred from the processor to the PCB. Conversely heat can travel from the PCB to the processor depending on where the larger thermal mass lies. Heat is generated as current flows through electrical resistances on the active surface of the processor die. A thermal gradient is established as the surface temperature rises.

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Heat in the form of thermal energy migrates from areas of higher temperature to areas of lower temperatures. In Figure 4, higher temperatures from either of the processor dies would transfer to the PCB. In the event the PCB (or surrounding components) were higher in temperature, the thermal transfer would be between the PCB to the processor. In a typical configuration (where the processor is the highest temperature), heat would flow from the processor die through the bumps (die attach), then through the copper metal substrate (in the package), through the solder balls (solder joints connecting the BGA package) to the PCB. In a proper thermal designed PCB, thermal conduction would occur between the BGA solder balls (or legs if applicable) onto the PCB and spread out over the entire area of the PCB, allowing for a potentially efficient form of convection, conduction, and radiation into the environment. Design of the PCB with minimal heat transfer paths will insulate the processor resulting in an increase in processor temperature.

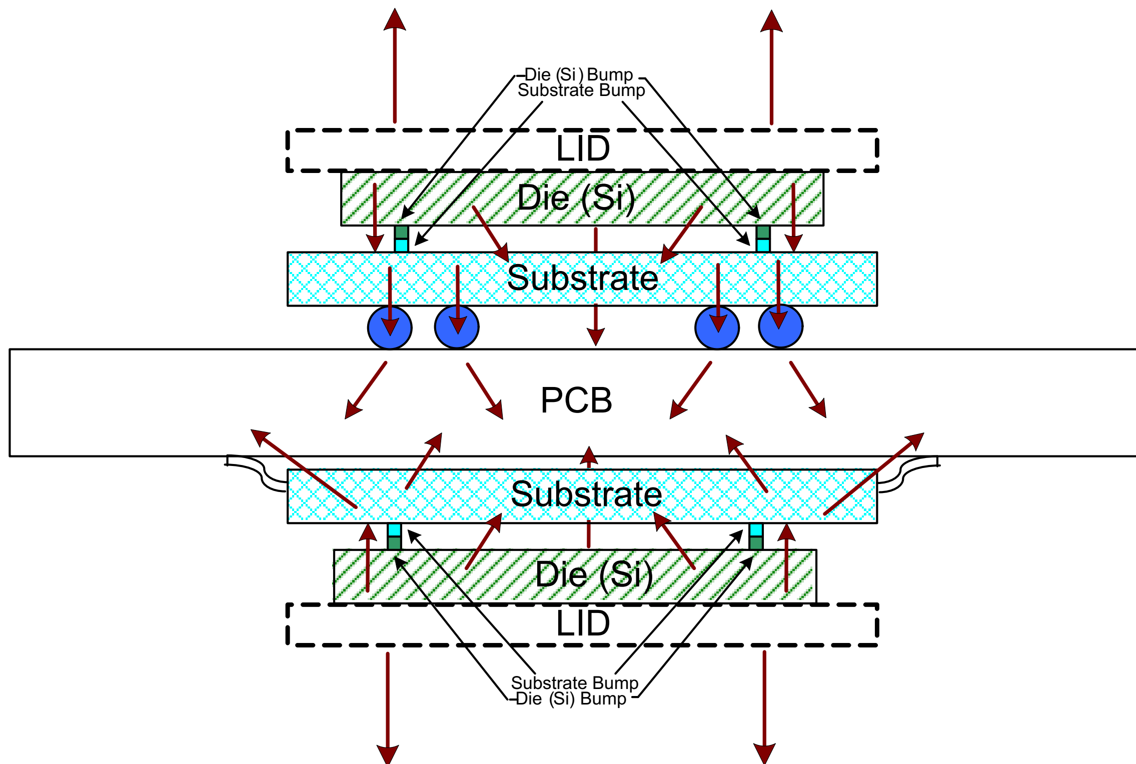

Figure 4. Processor to PCB Thermal Paths

In applications without a heatsink, proper design of the PCB is paramount to good thermal management of the application system. As PCB system designs vary, it is estimated that as much as 95%[1] of thermal energy can be dissipated by the PCB. Obtaining such thermal (transfer) performance can be achieved by following strict requirements, including but not limited to the following:

- Large spreading planes (*conduct heat away from the processor and components*)
- Sparsely populated PCBs with large areas for convection and radiation (*not typically possible*)
- Long[2] traces interconnecting the components, again to conduct heat away from the components (*Practical within reason*)
- Sufficient spacing of PCBs in a system rack to enable adequate convection

[1] From PCB Design for Thermal Performance

[2] Long traces should be used where not constrained by other routing requirements.

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A proper understanding of the thermal characteristics of the processor is critical for proper design of the application board and system. The maximum rated temperature of the device must not be exceeded, which requires adequate heat dispersion through a heat sink (or alternate sufficient cooling) to be a part of the thermal design. For acceptable operating temperature ranges, see the device-specific data sheet. Exceeding the recommended operating temperatures will decrease the processor reliability and may cause premature failure. Additionally, operating outside the recommended operating ranges may have an effect on timing and performance.

7.2 Trace Layout and Considerations

When considering trace layout for signal integrity, it is also important to take into account thermal (power) dissipation capability. Figure 5 provides the relative power dissipation for various trace widths (in inches) as compared to trace lengths (in inches). For this example, a 1 oz., 62.5 mil FR4 PCB was selected with a 25°C ambient temperature and a 50°C temperature rise. The information is provided to illustrate the advantages of wider traces when connecting to the solder balls (pins) of the processor.

Examining the results for a 2" trace, 10 mils in width, calculates to approximately 0.50W dissipated through or over the trace, whereas, the same length trace but only 4 mils in width calculates to only dissipate approximately 0.33W (34% lower power dissipation with the narrower trace).

Further examination for a 0.5" trace, 10 mils in width, calculates to approximately 0.12W dissipated through or over the trace, whereas, a 0.5" trace 4 mils in width calculates to only dissipate approximately 0.08W (34% lower power dissipation with the narrower trace).

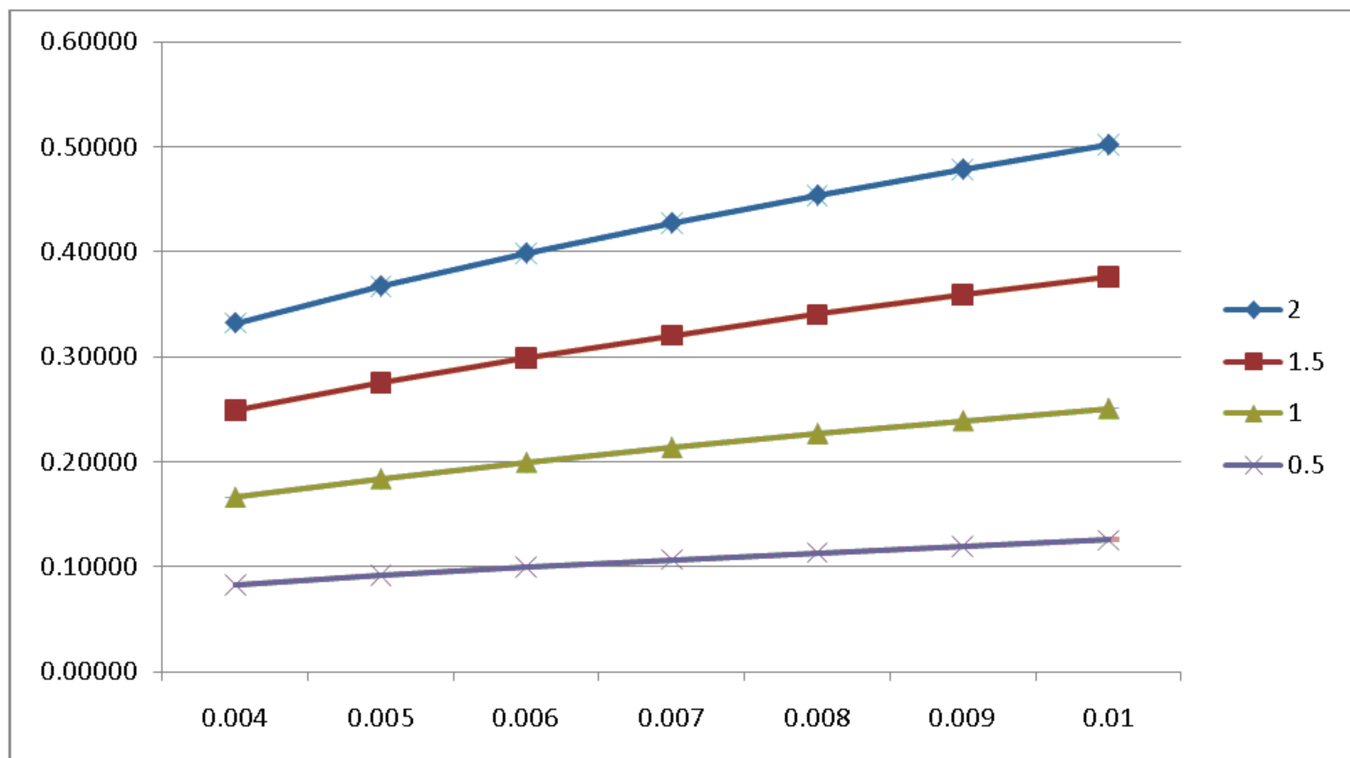

Figure 5. Trace Length vs Trace Width - Pwr Dissipation

Where possible, it is recommended that added copper be laid for traces and especially power pads for relative power supplies as recommended in each device-specific data sheet. As a further example, a 1.5" 1.5" 1oz. copper pad under a device (and directly coupled) is theoretically capable of dissipating 1.03 watts.

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NOTE: This graph and discussion only shows relative heat dissipation of various copper track sizes (lengths and widths). Actual dissipation will also be affected by other factors as discussed in this document.

7.2.1 PCB Size

PCB size has an impact on the thermal design of the end system, unfortunately most industries have predefined application form factors that must be followed. Inherently a larger PCB relates to more mass (copper) thus resulting in better heat dissipation. For academic purposes, note that a larger PCB improves the overall thermal characteristics (this is assuming good engineering design practices are applied).

7.3 Mechanical Compression

Mechanical compression, especially where conduction cooling is concerned is important. Excessive compression may improve thermal transfer but also increases the risk of damage to the processor or inducing added electrical shorts between BGA balls on the application hardware. Excessive mechanical compression is typically noted when using BGA sockets or interfacing a heat sink/enclosure indirect contact with the processor. For more information, see the device-specific data sheet and all relevant application reports regarding mechanical compression and BGA assembly.

7.4 PCB Material Selection

Proper printed circuit board (PCB) material (also referred to as PWB - printed wiring board) has a large impact on the overall system design. Materials range from low-cost FR4 to high-end ceramic material with other variations in between. Unfortunately what works well for a high performance application where signal integrity and propagation delays are important does not work as well as a thermal transfer medium.

Table 3 illustrates the tradeoff between thermal dissipation and propagation delays for several commonly used materials. Basic calculations were performed using a microstrip topology. Stripline configurations will have faster propagation times.

Table 3. Er versus Dk for Common PCB Materials

Material	Model	Er	T_{PD} Per Inch (pS)	Thermal Conductivity W/mK
Air	N/A	1	90.95	0.024
PTFE/Glass		2.2	111.31	–
2000	ULTRALAM	2.4 - 2.6	114.36	–
3070	RO3730	3.0	123.03	0.45
3000	RO3003	3.0	123.03	0.50
IS680	IS680	2.8	120.21	0.32
7000	SYRON	3.4	128.49	0.35
IS620	IS620	3.54 - 3.59	130.34	0.35
4000	RO4000	3.55	130.48	0.64
GETEK	GETEK	3.5 - 3.8	129.82	0.4
250HR	FR250	3.90 - 4.0	135.00	0.4 - 0.5
FR408	FR4	3.75 - 3.81	133.08	0.4
FR406	FR4	3.92 - 4.0	135.25	0.3 - 0.4
GI-180 BT/Epoxy	FR4	3.5 - 3.6	129.82	0.35
FR254	FRP-254	4.2 - 4.3	138.76	0.4 - 0.5
FR402	FR4	4.25 - 4.26	139.38	0.36

Materials that satisfy both conditions tend to be more costly and not used in mass production of recently evaluated processor application hardware. Selection of material is paramount to a successful design. Special attention must also be kept when evaluating a material for internal or external traces/planes.

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7.5 PCB Copper Weight

Proper copper thickness (referred to as planes) is important to the overall impedance, thermal management, and current carrying capabilities of the design. During the examination and review of all application hardware it is important to consider each of these variables.

As a general rule of thumb, the inner layers or planes of most PCBs are typically 1 oz. copper while the outer layers are 0.5 oz. copper. Outer layers receive solder masking which in the finished product is usually similar to the 1 oz. inner copper weight. Table 4 provides basic information regarding copper weight, thickness and current carrying capabilities (other factors can positively or negatively affect these specifications).

Table 4. Trace Width to Current Specifications

Cu Weight	Cu Thickness (mils)	Cu Thickness (mm)
2.0 oz	2.8	0.07112
1.0 oz	1.4	0.03556
½ oz	0.7	0.01778

Figure 6 illustrates the relationship between trace width, copper thickness (1 oz. shown) and current carrying capability.

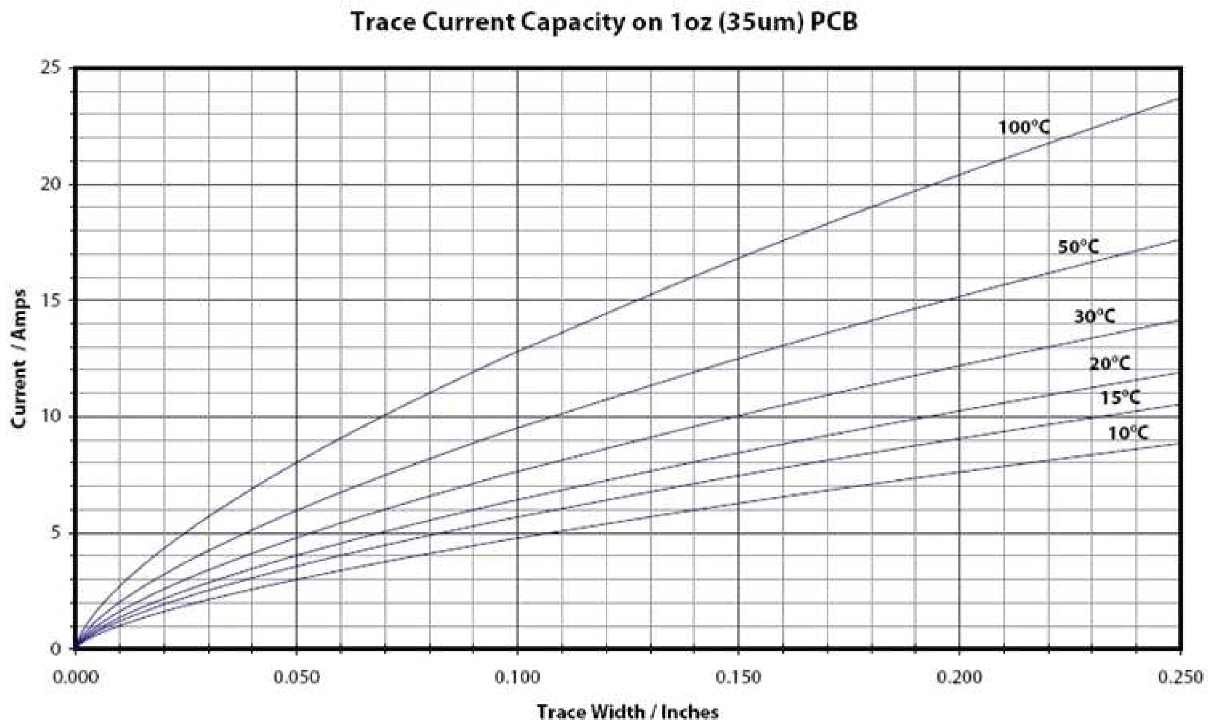

Figure 6. Trace Width to Current Specifications

It is important to properly match the weight of the internal layers against the power requirements, thermal needs, and impedance stack up.

8 General Requirements and Considerations

The information contained in this document is only intended to provide a general background to thermal management for the processor. Ultimately it is the integrator, intermediate application developer, or the end user that must evaluate the system as it pertains to proper thermal management of Texas Instruments processors.

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Each end application is different, regardless of whether or not the application is designed for the same market space. Design topologies, components, and materials as described briefly in this document account for many of the independent conditions required to properly evaluate the thermal design. It is your responsibility to correctly apply the variables including environmental conditions to the specific surface nodes of the Delphi compact model. You can elect to define environmental conditions based on modeling (of the environment) or by establishing boundary conditions in terms of specific heat transfer coefficients. Ultimately, the constraints and variables used will be limited by the tools available and time allotted for the analysis. Certain classes of simulation and modeling tools offer better accuracy and are always recommended.

Texas Instruments recommends the use of Network Compact Models like the Delphi model and intend to supply such a model for all new processors. Thermal models are typically provided in the processor's product folder on ti.com.

9 Case Temperature Measurement

Once the system has been finalized and manufactured, a case temperature measurement may be performed to ensure that the maximum case temperature specification of the processor has not been exceeded.

9.1 Case Temperature Measurement Without a Heatsink

Case temperature is defined as the hottest temperature on the top of the device and should be measured at the center of the top/lid of the device. The case temperature measurement can be performed with (in order of accuracy) an IR camera, a fluoroptic probe, a thermocouple, or IR gun (maximum field view of 4 mm diameter) just to name a few techniques. When a thermocouple is chosen as the technique to perform the measurement, a fine gauge wire (36 to 40 gauge, J or K wire) should be used to minimize the local cooling from the thermocouple.

If using a thermocouple, it should be attached to the center of the package surface (± 1 mm) with a bead of thermally conductive epoxy no larger than 2x2 mm on a side. Taping the thermocouple to the package surface is not recommended. To minimize the heat sinking nature of the thermocouple, the wire should be dressed along the diagonal of the package, down to the PCB surface, and over a minimum distanced of 25mm before lifting from the PCB. The thermocouple wire can be tacked to the PCB for this routing purpose with tape. Use of improper thermocouple wire gauge can create errors in the measurements of 5%-50%.

When using either an IR camera or IR gun, be sure to correct the reading for the emissivity of the surface being investigated, especially when the processor has a metal lid. See your instrument's documentation for details.

9.2 Case Temperature Measurement With a Heatsink

Measuring case temperatures with heat sinks applied represents special challenges since the heat sink covers the surface to be measured. If the user wishes to measure the case temperature with a heat sink applied, the following procedure is recommended.

1. Drill a hole with a diameter of 1mm or less in heat sink such that the hole will be at the center of the package when the heat sink is attached. Be sure to drill the hole through the heat sink before attaching the heat sink to the package. If a pressure sensitive adhesive is used to attach the heat sink, drill through this adhesive. Be sure there are no burrs or other material which would interfere with the mating surfaces.
2. Attach the heat sink to the package. If an epoxy will be used for the heat sink attach, fill the hole drilled in step 1 with a wax, foam, or other material which will insure the hole is not filled by the epoxy. Be careful not to contaminate the heat sink attach surface with this material.
3. Fill the hole with thermal grease. If the hole was plugged to avoid epoxy filling, be sure to unplug the hole.
4. Thread a fine gauge thermocouple of the type described above into the hole and secure with a drop of epoxy or tape.

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9.3 Case Temperature Measurement: Accounting for Leakage Variations

As noted above, the resulting case temperature of the processor that is measured in the finalized system is dependent on the power consumption of the processor in this specific application. To determine the maximum case temperature measurement, the worst case power consumption of the processor for the finalized product must be accounted for.

The power consumption of the processor can be broken down into the sum of two components, active power and static (also called leakage) power. The active power component is essentially dependent upon application activity and voltage. For a given application and constant voltage, it can be assumed that active power remains the same. Static power varies across voltage, temperature and manufacturing process. The processor power consumption summary spreadsheet takes into account the static power consumption from the strong units (representative of maximum end of static power consumption on production units). The spreadsheet may be used to estimate the worst case static power consumption for a given case temperature. The obtained value may then be used to calculate the final worst case total power consumption.

The following method describes the procedure to account for worst case static power in the case temperature measurement.

1. Measure the case temperature using the method described above.
2. Measure ambient temperature (outside of the enclosure).
3. Measure total power consumption of the processor in the finalized application.
4. Measure the static power consumption of the processor at the case temperature measured in step 1.
5. Calculate the active power consumption of the processor in the finalized application.
   Activepower = Total power -Static power
6. Calculate $\theta_{JA,effective}$ of the finalized system using the following equation:
   $$\theta_{\text{JA,effective}} \approx \frac{T_C - T_A}{\text{TotalPower}}$$
7. Use the power application spreadsheet to estimate the maximum static power consumption at the case temperature measured in step 1.
8. Recalculate the maximum total power consumption of the processor.
   Max TotalPower = ActivePower (step5) + Max Static power (step7)
9. Recalculate the case temperature, accounting for maximum total power consumption.
   $T_C \approx T_A$ (step2) + (TotalPower(step8) × $\theta_{JA,effective}$ (step6))

NOTE: The max case temperature measurement should account for worst case ambient conditions for the specific application.

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10 Sample Calculations

To make first-order junction temperature calculations, several pieces of data are needed:

- Power and thermal characterization data (TI provided, or experimentally derived from EVM)
- Thermal resistance characteristics from the device-specific data manual

For this example, the following thermal resistance characteristics will be used from an actual Texas Instruments processor:

Table 5. AM5728 Thermal Resistance Characteristics (ABC Package)

Parameter	Description	°C/W(1)	Air Flow (m/s)(2)
θ_{JC}	Junction-to-case	0.82	N/A
θ_{JB}	Junction-to-board	3.78	N/A
θ_{JA}	Junction-to-free air	11.1	0
	Junction-to-moving air	8.8	1
		8.0	2
		7.5	3
Ψ_{JT}	Junction-to-package top	0.62	0
		0.66	1
		0.66	2
		0.66	3
Ψ_{JB}	Junction-to-board	3.43	0
		3.22	1
		3.12	2
		3.04	3

10.1 Calculations With Theta Parameters

Estimating junction temperature using Theta parameters provides a reasonable approximation of junction temperature. Because Theta parameters are based on a processor mounted to a JEDEC defined test board, and will be different in an actual system, thermal calculations using Theta parameters are not a substitute for actual thermal modeling and system testing.

The following calculation uses data collected using actual silicon (nominal), on a production evaluation board, fitted with a low-cost heatsink attached to the processor lid with adhesive thermal interface material. Ambient temperature was controlled by placing the entire system in a thermal chamber.

CPU was loaded with the Dhrystone benchmark. The processor tested contains two ARM cores, so two instances of the benchmark were running. Power and thermal measurements were taken after 10 minutes of continues benchmarking.

Dhrystone benchmark (2-cores, 1.0 GHz, Linux 4.1), typical silicon	
Ambient temperature: 40°C Reported junction temperature (1) 64°C Total SoC Power (2): 2.4 W	θ_{JC} (3) = 0.82°C/W θ_{CS} (4) = 0.8°C/W θ_{SA} (4),(5) ≈= 20°C/W θ_{JA} (7) ≈= $\theta_{JC} + \theta_{CS} + \theta_{SA}$ = 21.62°C/W

(1) Junction temperature reported by on-chip MPU domain thermal sensor
(2) Total SoC power includes IO power, un-optimized for any application
(3) θ_{JC} (junction-to-case resistance) - from the device-specific data sheet
(4) θ_{CS} (case-to-heatsink) – from the heat sink data sheet
(5) Heatsink used is CTS p/n BDN10-3CB/A01
(6) θ_{SA} (heatsink-to-ambient) extrapolated, based on 0.3m/s airflow inside thermal chamber
(7) θ_{JA} (junction-to-ambient) assumes most power is dissipated through heat sink

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Calculated Junction Temperature

$$T_{JUNCTION} \cong T_{AMBIENT} + \left(\frac{\theta_{JA} \times (\theta_{JC} + \theta_{CS} + \theta_{SA})}{\theta_{JA} + \theta_{JC} + \theta_{CS} + \theta_{SA}} \right) \times Power \tag{7}$$

$$T_J \approx 40°C + \left(\frac{21.62 \times (0.82 + 0.8 + 20)}{21.62 + 0.82 + 0.8 + 20} \right) \times 2.4W$$

$$T_J \approx 66°C\ (estimated) \tag{8}$$

10.2 Calculations With PSI-JT Parameter

Psi-JT (Ψ_{JT}) is defined as the difference in junction temperature to case temperature at the top center of the package divided by the operating power. Ψ_{JT} is measured when the package is mounted only on the test PCB, which allows power to partition itself into any path that it wants to take. For more information regarding the definition and proper application of Ψ_{JT}, see Semiconductor and IC Package Thermal Metrics.

The following calculation uses data collected using typical silicon (nominal process), without a heatsink, on an orderable evaluation board and published thermal resistance values. For a complete set of processor thermal resistances, see Table 1. Test conditions were on a lab bench, in still air; natural convection thermal resistance numbers are used for Ψ_{JT}. A K type thermocouple (40 gauge) was embedded in a small bead of thermal grease, and held in place with a minimum amount of Kapton tape.

Linux kernel 4.4, OS Idle (scheduler and background tasks running)	
Ambient temperature: 40°C Reported junction temperature ([1]): 59°C Measured T_{CASE}:[2] 57°C	Total SoC power [2]: 2.2W Ψ_{JT} = 0.62°C/W

(1) Junction temperature reported by on-chip MPU domain thermal sensor

(2) Total SoC power includes IO power, un-optimized for any particular application

$$T_{JUNCTION} = T_{CASE} + (\Psi_{JT} * Power) \tag{9}$$

$$T_{JUNCTION} = T_{CASE} + (\Psi_{JT} * Power)$$

$$T_{JUNCTION} \cong 57^{\circ}C + (0.62 * 2.2W)$$

$$T_{JUNCTION} \cong 58.4^{\circ}C\ (calculated) \tag{10}$$

Linux kernel 4.4 Dual Dhrystone (2-cores running Dhrystone)	
Ambient temperature: 27°C Reported junction temperature ([1]): 86°C Measured T_{CASE}: 82°C	Total SoC Power ([2]): 6.3W Ψ_{JT} = 0.62°C/W

(1) Junction temperature reported by on-chip MPU domain thermal sensor

(2) Total SoC power includes IO power, and has not been optimized for any particular application

$$T_{JUNCTION} = T_{CASE} + (\Psi_{JT} * Power) \tag{11}$$

$$T_{JUNCTION} = T_{CASE} + (\Psi_{JT} * Power)$$

$$T_{JUNCTION} \cong 82^{\circ}C + (0.62. * 6.3W)$$

$$T_{JUNCTION} \cong 85.49^{\circ}C\ (calculated) \tag{12}$$

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10.3 Calculations With PSI-JB Parameter

Psi-JB (Ψ_{JB}) is very similar to Ψ_{JT} in concept. It refers to the measurement of the difference between the junction temperature and the center package pin temperature, divided by the power dissipation of the device. Ψ_{JB} is the thermal characterization parameter used to more accurately estimate in-use junction temperatures from a measured board temperature. For more information regarding the definition and proper application of Ψ_{JB}, see Semiconductor and IC Package Thermal Metrics.

The following calculation uses data collected using typical silicon (nominal process), without a heatsink, on an orderable evaluation board and published thermal resistance values. For complete set of processor thermal resistances, see Table 1). Test conditions were on a lab bench, in still air; natural convection thermal resistance numbers are used for Ψ_{JB}.

Linux kernel 4.4, OS Idle (scheduler and background tasks running)	
Ambient temperature: 26°C Reported junction temperature ([1]): 59°C Measured T_{BOARD}: 51°C	Total SoC Power ([2]): 2.2W Ψ_{JB} = 3.43°C/W

(1) Junction temperature reported by on-chip MPU domain thermal sensor
(2) Total SoC power includes IO power, and has not been optimized for any particular application

$$T_{JUNCTION} = T_{BOARD} + (\Psi_{JB} * Power) \tag{13}$$

$$T_{JUNCTION} = T_{BOARD} + (\Psi_{JB} * Power)$$
$$T_{JUNCTION} \cong 51^{\circ}C + (3.43 * 2.2W)$$
$$T_{JUNCTION} \cong 58.5^{\circ}C\ (calculated) \tag{14}$$

Linux kernel 4.4, dual Dhrystone (2-cores running Dhrystone)	
Ambient temperature: 27°C Reported junction temperature ([1]): 86°C Measured T_{BOARD}: 63°C	Total SoC Power ([2]): 6.3W Ψ_{JB} = 3.43°C/W

(1) Junction temperature reported by on-chip MPU domain thermal sensor
(2) Total SoC power includes IO power, and has not been optimized for any particular application

$$T_{JUNCTION} = T_{BOARD} + (\Psi_{JB} * Power) \tag{15}$$

$$T_{JUNCTION} = T_{BOARD} + (\Psi_{JB} * Power)$$
$$T_{JUNCTION} \cong 86^{\circ}C + (3.43 * 6.3W)$$
$$T_{JUNCTION} \cong 84.6^{\circ}C\ (calculated) \tag{16}$$

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2016) to B Revision	Page
• Added new Section 9.	14

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