TEXAS INSTRUMENTS

Application Report
SPRABY8–October 2015

AM572x GP EVM Power Simulations

Embedded Processors

ABSTRACT

The purpose of this application report is to present the flow, the environment settings and TI requirements used to perform the analysis of critical power nets of a platform using an application processor. The Power Delivery Network (PDN) performance is measured by extracting and analyzing three printed circuit board (PCB) parameters: DC resistivity, capacitor loop inductance, and broadband target impedance. To conclude each parameter section, PDN extraction results of the AM572x General-Purpose Evaluation Module (GP EVM) processor board with some general layout recommendations are presented.

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1 Requirements for Power Delivery Network (PDN)

PDN performance was not considered as a major criteria in the early days of printed circuit board (PCB) design. However, in today's platforms utilizing lower voltage, higher current, and reduced voltage noise margins, PDN performance must be modeled early in the PCB design process and then optimized to meet the specified device requirements with an overall objective of supplying a noise-free and stable voltage to the application processor. Figure 1 presents a break-down model of a complete PDN network from the Voltage Resource Manager (VRM) to the application processor.

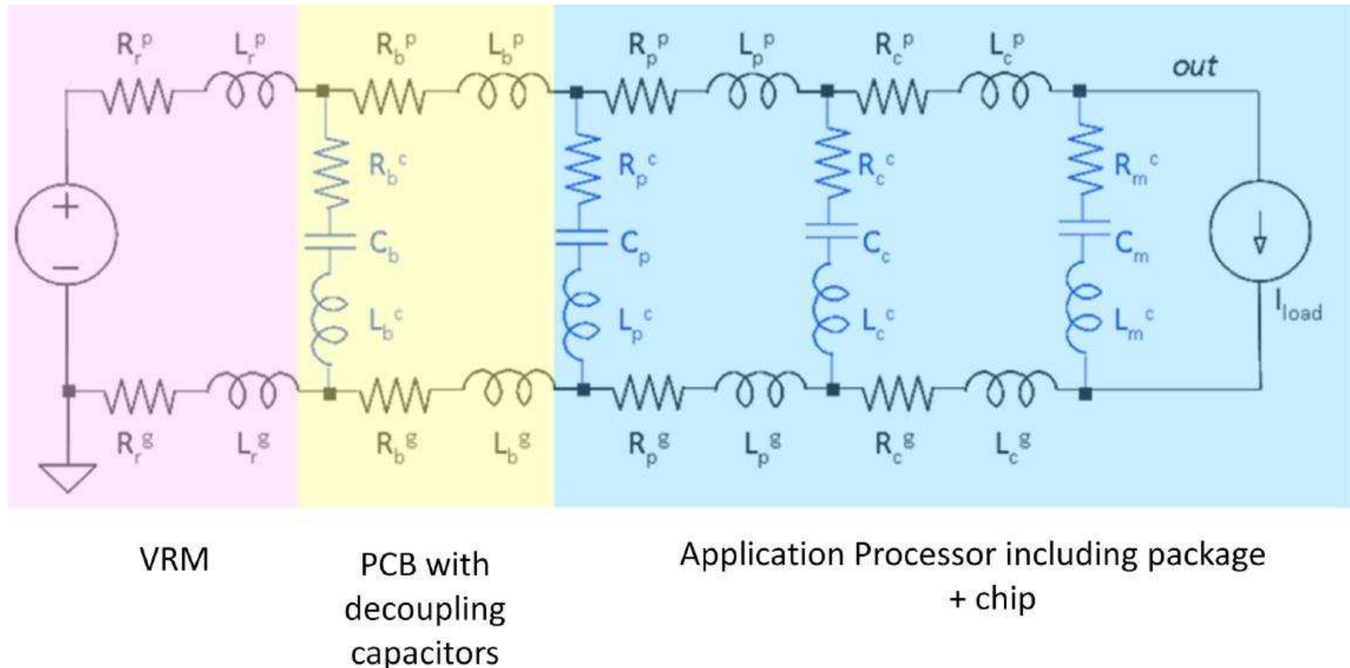

Figure 1. Power Delivery Network Model

Factors such as component selection, board manufacturing, assembly issues, ambient temperature, and other variables, can also cause power supply issues, but not all possible issues are discussed in this document. Nonetheless, every new board design should carefully consider the layout of each of the power supplies since some may be stressed more than others depending on the specific needs of each application.

Note that only the main power rails are discussed in this analysis:

- VDD_DDR
- VDD_CORE
- VDD_MPU
- VDD_DSP
- VDD_3V3
- VDD_1V8

The power requirements for the AM572x power rails can be found in the *AM572x Embedded Applications Processor Data Manual* (SPRS915). For details and requirements for each of these power supplies to the AM572x, see the data manual. Several simulations were run to determine the electrical characteristics of the AM572x GP EVM processor board. These simulations verify the basic electrical characteristics of the power delivery networks of these critical power supplies to the processor.

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2 Simulations to Run

- **Loop resistance** – provides details on IR drop, resultant voltage drop, and current density.

  The loop resistance is the primary portion of the trace impedance and directly affects the DC power delivery. This characteristic of the PCB design is especially important to ensure that power supplies remain within allowable ranges.

  Due to shape geometry complexity, vias, and multi-layer routing, it is difficult to manually calculate the DC resistance of the various circuits present on the PCB. Numerous signal integrity (SI) or layout EDA tools extract the DC resistance from the board design files.

  To extract DC resistance, you will need:

  – Platform Schematic
  – PCB Layout
  – PCB Stack-up
  – DC resistance extracting tool.

  Figure 2 describes the flow used by most tools to extract DC resistance. In TI PDN analysis, the lumped methodology is preferred; each of the power and GND pins of VRM and AP are grouped to shorten the simulation run time.

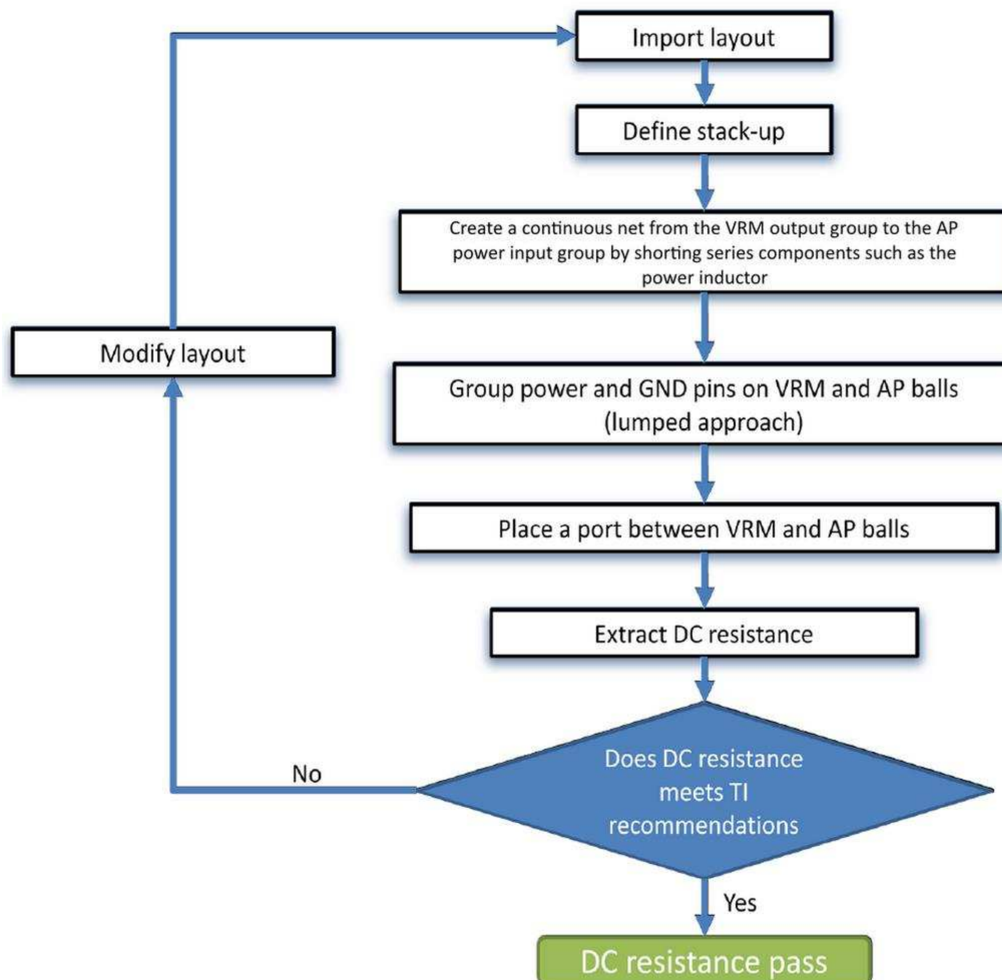

Figure 2. DC Resistance Extraction Flow

- **Loop inductance value** – provides information that helps analyze the decoupling capacitor placement and routing

  The loop distance is important for determining the inductance value of the power net. Each length of

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trace increases the inductance of the decoupling path (power side and return side.) A smaller loop distance from the processor to the decoupling capacitor helps reduce the loop inductance value, which in turn allows better filtering of power supply noise before the power reaches the processor's power pins.

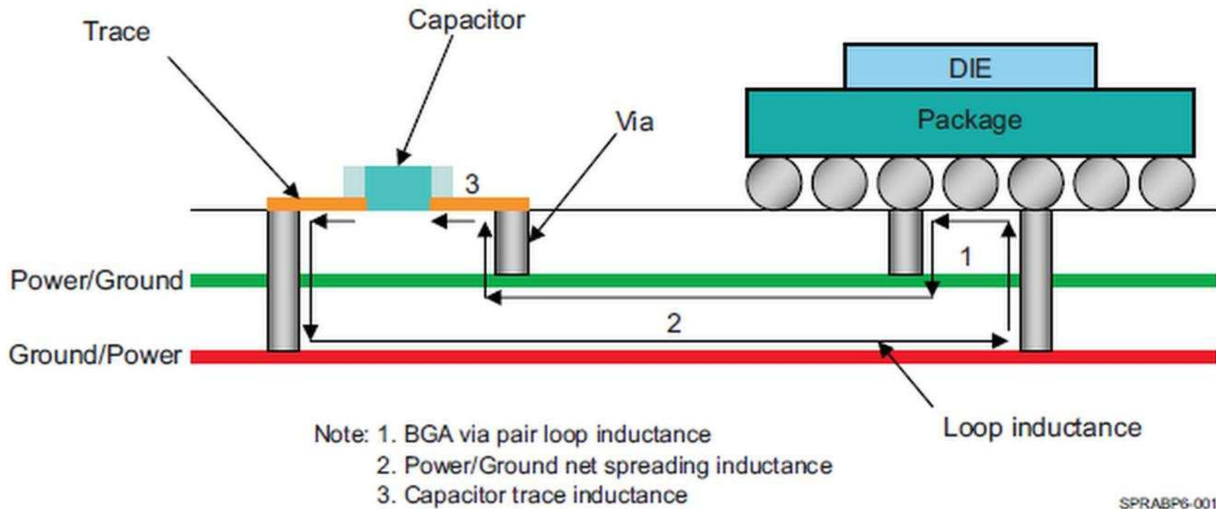

Figure 3. Cap Loop

- **Power trace impedance**

  Lumped analysis mode was performed first to simplify the initial simulations. As seen from the results, this board yields PDN simulation results so as not to necessitate distributed analysis for the main processor power nets.

- **Via placement and power distribution**

  Via placement is analyzed and current density simulations are reviewed to determine if plane layer changes (or power traces when routed within the processor ball array) cause insufficient power levels.

3 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85°C are shown in Table 1.

Table 1. Commercial Applications Representative Decoupling Capacitors Characteristics

Value	Voltage [V]	Package	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	Reference
22 µF	6,3	0603	X5R	±20%	-55 to 85	±15	GRM188R60J226MEA0L
10 µF	4,0	0402	X5R	±20%	-55 to 85	±15	GRM155R60G106ME44
4.7 µF	6,3	0402	X5R	±20%	-55 to 85	±15	GRM155R60J475ME95
2.2 µF	6,3	0402	X5R	±20%	-55 to 85	±15	GRM155R60J225ME95
1 µF	6,3	0201	X5R	±20%	-55 to 85	±15	GRM033R60J105MEA2
470 nF	6,3	0201	X5R	±20%	-55 to 85	±15	GRM033R60G474ME90
220 nF	6,3	0201	X5R	±20%	-55 to 85	±15	GRM033R60J224ME90
100 nF	6,3	0201	X5R	±20%	-55 to 85	±15	GRM033R60J104ME19

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Table 2. Recommended PDN and Decoupling Characteristics [1][2][3][4][5]

PDN Analysis:	Static	Dynamic		Number of Recommended Decoupling Capacitors per Supply							
Supply	Max R_{eff} [7] [mΩ]	Dec. Cap. Max LL [6][8] [nH]	Impedance [mΩ]	100 nF[6]	220 nF	470 nF	1µF	2.2 µF	4.7 µF	10 µF	22 µF
vdd_mpu	10	2	57	12	2	2	3	1	1		1
vdd_dspeve	13	2.5	54	8	1	1	2	1	1	1	
vdd	27	2	87	6	1	1	1	1	1		
vdd_gpu	18	2.5	207	6	1	1	1	1	1		
vdd_iva	48	2	800	5		1			1		
vdds_ddr1	10	2.5	200	8	4		2		2		1
vdds_ddr2	10	2.5	200	8	4		2		2		1
cap_vbbldo_dspeve	N/A	6	N/A								
cap_vbbldo_gpu	N/A	6	N/A								
cap_vbbldo_iva	N/A	6	N/A								
cap_vbbldo_mpu	N/A	6	N/A								
cap_vddram_core1	N/A	6	N/A								
cap_vddram_core2	N/A	6	N/A								
cap_vddram_core3	N/A	6	N/A								
cap_vddram_core4	N/A	6	N/A								
cap_vddram_core5	N/A	6	N/A								
cap_vddram_dspeve1	N/A	6	N/A								
cap_vddram_dspeve2	N/A	6	N/A								
cap_vddram_gpu	N/A	6	N/A								
cap_vddram_iva	N/A	6	N/A								
cap_vddram_mpu1	N/A	6	N/A								
cap_vddram_mpu2	N/A	6	N/A								

(1) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table of the *Specifications* chapter in the *AM572x Embedded Applications Processor Data Manual* (SPRS915).

(2) Capacitor ESL must be as low as possible and must not exceed 0.5 nH.

(3) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table of the *Specifications* chapter in the *AM572x Embedded Applications Processor Data Manual* (SPRS915).

(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC and the processor power balls.

(5) Assuming that the PMIC (power IC) feedback sense is taken close to processor power balls.

(6) This limit only applies to the lowest value capacitor present in the design.

(7) Maximum R_{eff} from SMPS to Processor.

(8) Maximum Loop Inductance for each decoupling capacitor.

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4 Models

The models to be used for the board components are key to ensuring that the simulation results provide realistic values as they relate to each particular board design. Table 3 lists the necessary models for this PDN study.

Table 3. Models for GP EVM PDN Study

Component	Reference Designator	Part Number	Model Name
Inductor	L5	Vishay IHLP-1616ABER1R0M11	Modeled as a short in simulation
Capacitor	C167	TDK C0603X5R0J224M030BB	C0603X5R0J224M030BB.s2p
Capacitor	VDD_MPU(C77,C82-C93)|VDD_DDRn(C156-C184) |VDD_CORE(C54-C72)|VDD_DSP(C51-C53, C57,C59,C61,C63,C64,C68-C70,C73-C76,C78-C80) |VDD_3V3(C113-C139,C15,C263,C268, C269,C30,C339,C50,C81)	TDK C0603X5R0J104M030BC	C0603X5R0J104M030BC.s2p
Resistor	R(all)		Modeled as a short in simulation

5 VDD_MPU

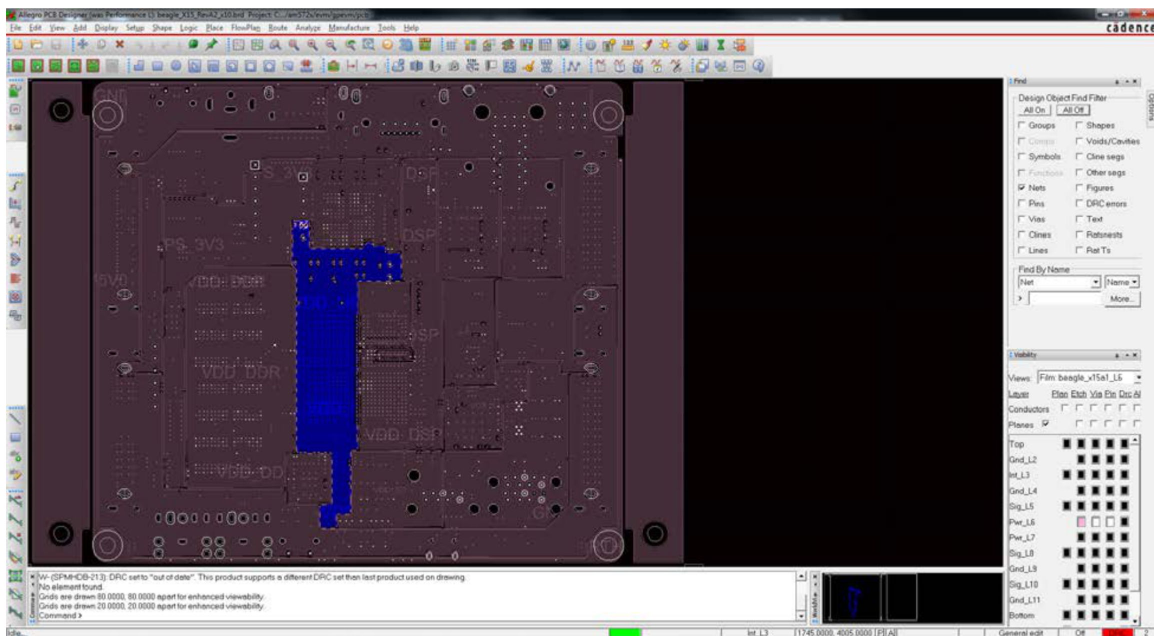

Figure 4. VDD_MPU Example (Layer 6)

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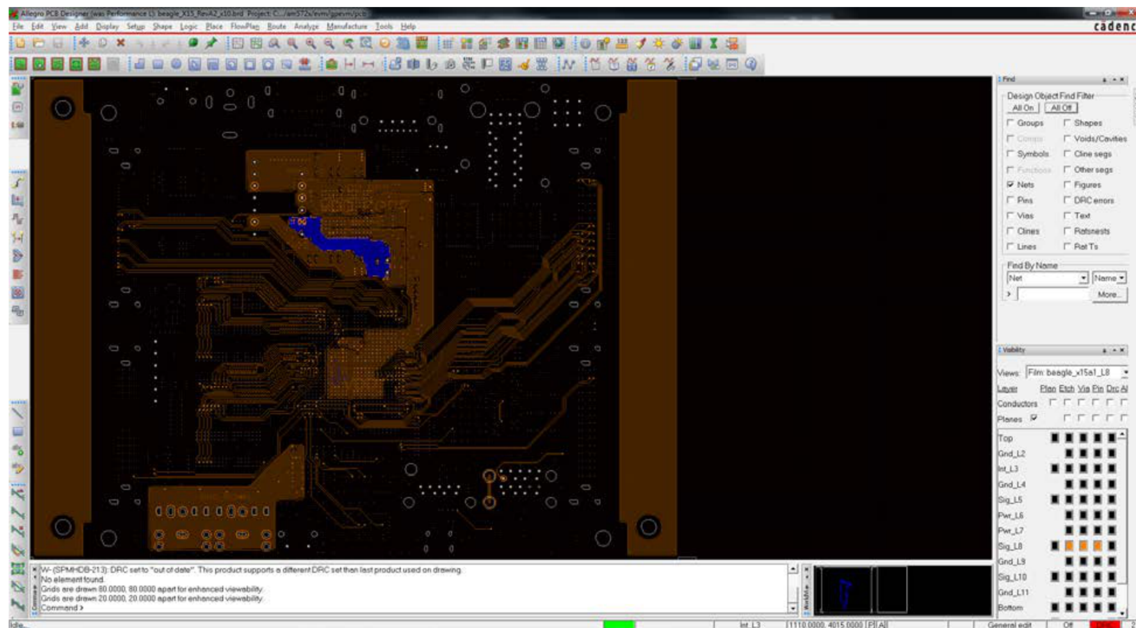

Figure 5. VDD_MPU Example (Layer 8)

5.1 IR Drop

Loop resistance = 0.2870 mΩ

VDD_MPU max drop due to trace resistance = 1.4 mV. With VDD_MPU sourced at 1.10 V nominal from the power management control IC (PMIC), the worst case level at System-on-Chip (SOC) is 1.0986 V.

5.2 Voltage Drop (resultant)

Figure 6 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_MPU power net.

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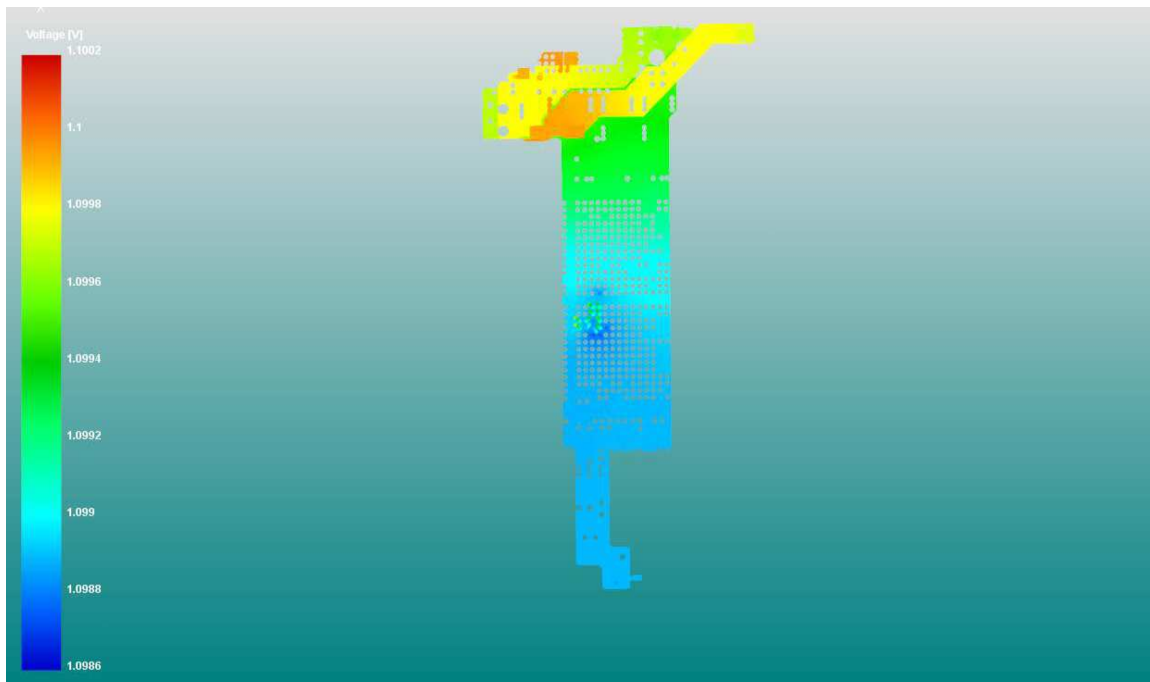

Figure 6. VDD_MPU Voltage Drop (resultant)

5.3 Current Density

Figure 7 shows the current density within the power trace. To determine the amount of current in any portion of the trace, see the color scale on the left side. Areas of high current density would benefit from additional copper to provide increased current availability.

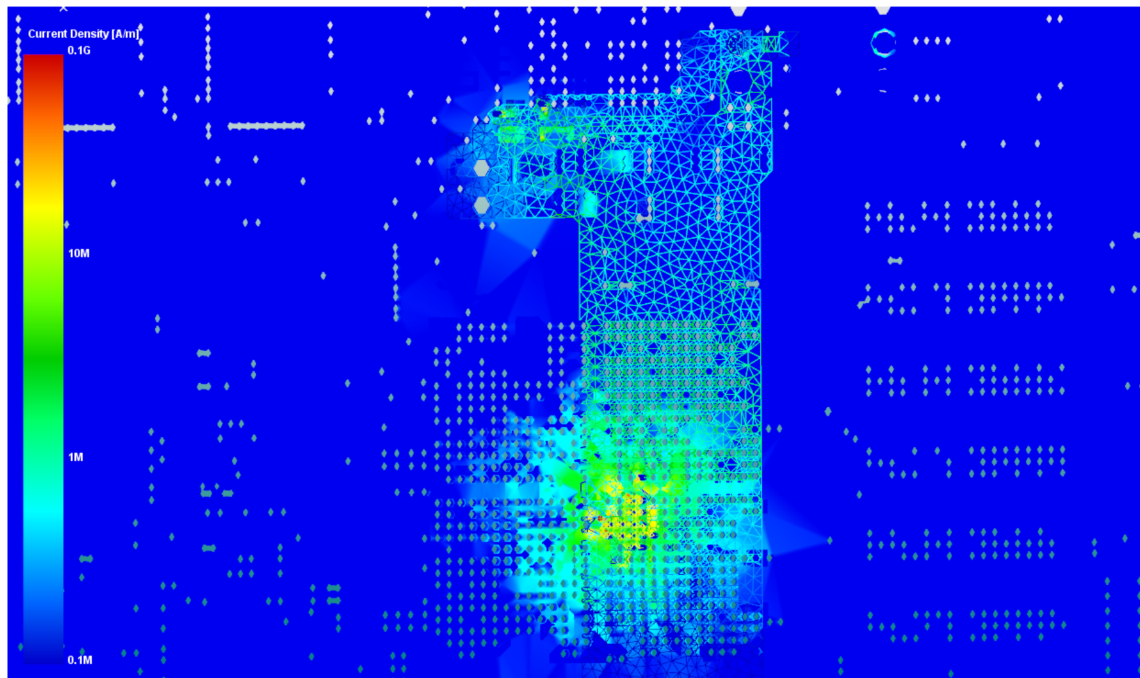

Figure 7. VDD_MPU Current Density

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5.4 Loop Inductance Value

Simulation was done to check the loop inductance values of each capacitor on the VDD_MPU power net. These are listed in Figure 8 and Table 4. These values are taken at 50 kHz.

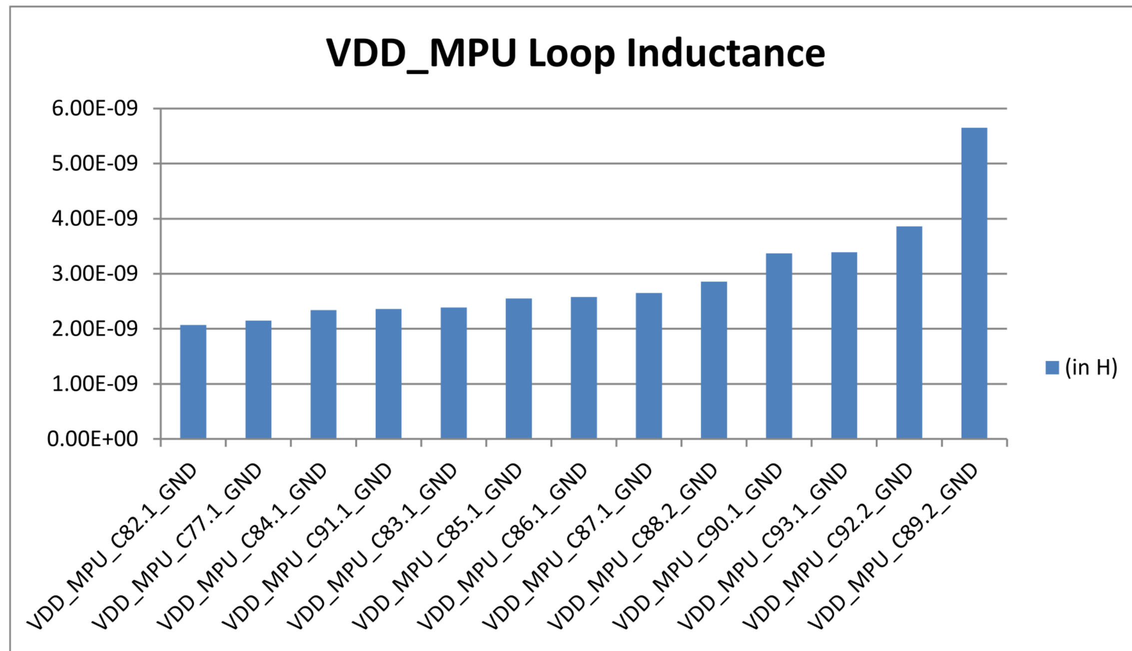

Figure 8. VDD_MPU Loop Inductance

Table 4. VDD_MPU Loop Inductance Table

VDD_MPU_C77.1_GND	2.15E-09
VDD_MPU_C82.1_GND	2.07E-09
VDD_MPU_C83.1_GND	2.39E-09
VDD_MPU_C84.1_GND	2.34E-09
VDD_MPU_C85.1_GND	2.55E-09
VDD_MPU_C86.1_GND	2.58E-09
VDD_MPU_C87.1_GND	2.65E-09
VDD_MPU_C88.2_GND	2.86E-09
VDD_MPU_C89.2_GND	5.65E-09
VDD_MPU_C90.1_GND	3.37E-09
VDD_MPU_C91.1_GND	2.36E-09
VDD_MPU_C92.2_GND	3.86E-09
VDD_MPU_C93.1_GND	3.39E-09

Space is limited for placing power decoupling capacitors on AM572x-based designs that place a premium on low-cost, reduced footprint PCBs. However, care was taken to place the bulk and decoupling capacitors in optimal locations that provide sufficient filtering of the input power to the processor. This is a tradeoff between processor power nets since there is not enough physical room to place all of the capacitors (for all power nets) close to the processor itself.

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5.5 Decoupling Capacitor Placement

Figure 9 shows the physical placement of the decoupling capacitors on the VDD_MPU power net.

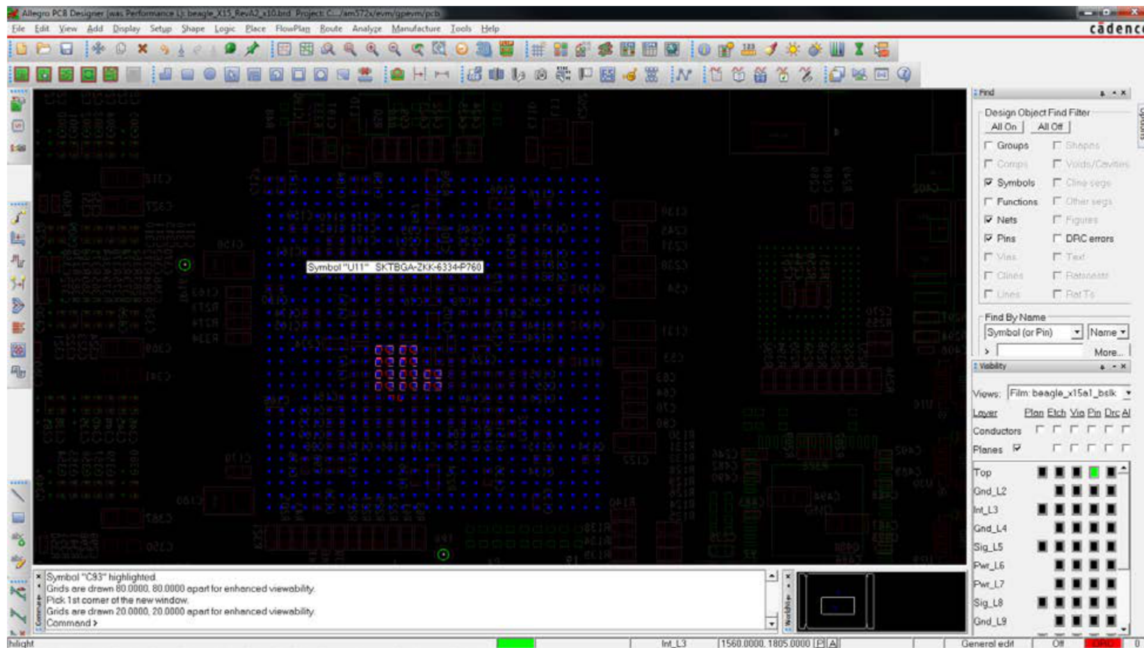

Figure 9. VDD_MPU Decoupling Capacitor Placement

5.6 Power Trace Impedance

Trace Impedance @ 50 MHz = 86.6 mohms

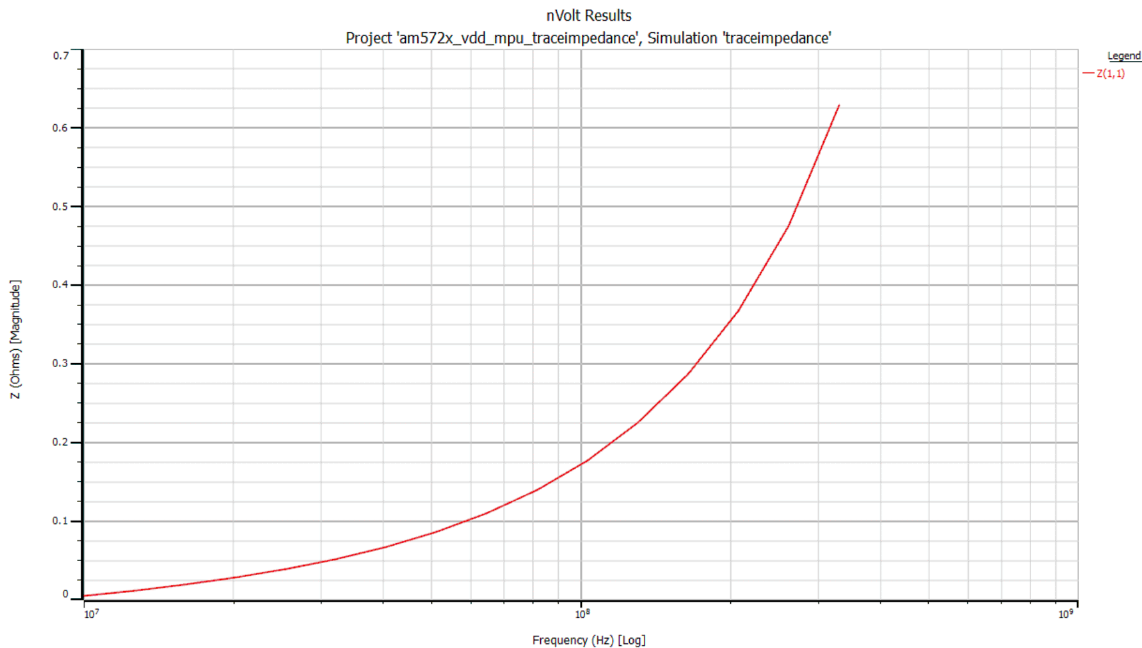

Figure 10. VDD_MPU Power Trace Impedance

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6 VDD_DDR

Power planes of the VDD_DDR1 and VDD_DDR2 power buses.

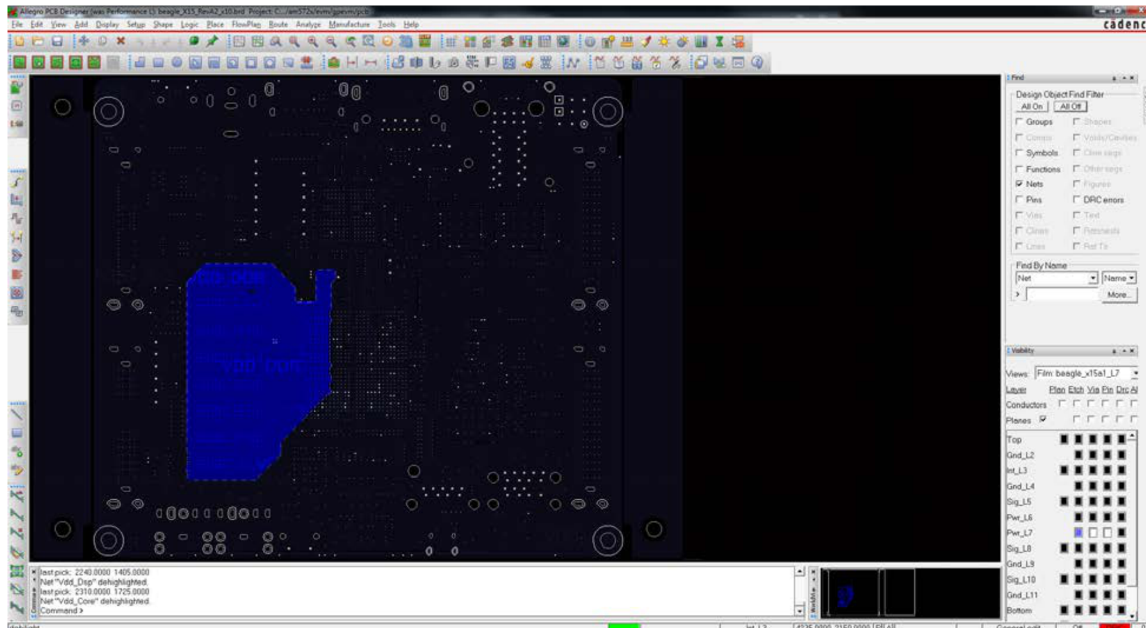

Figure 11. VDD_DDR Example (Layer 7)

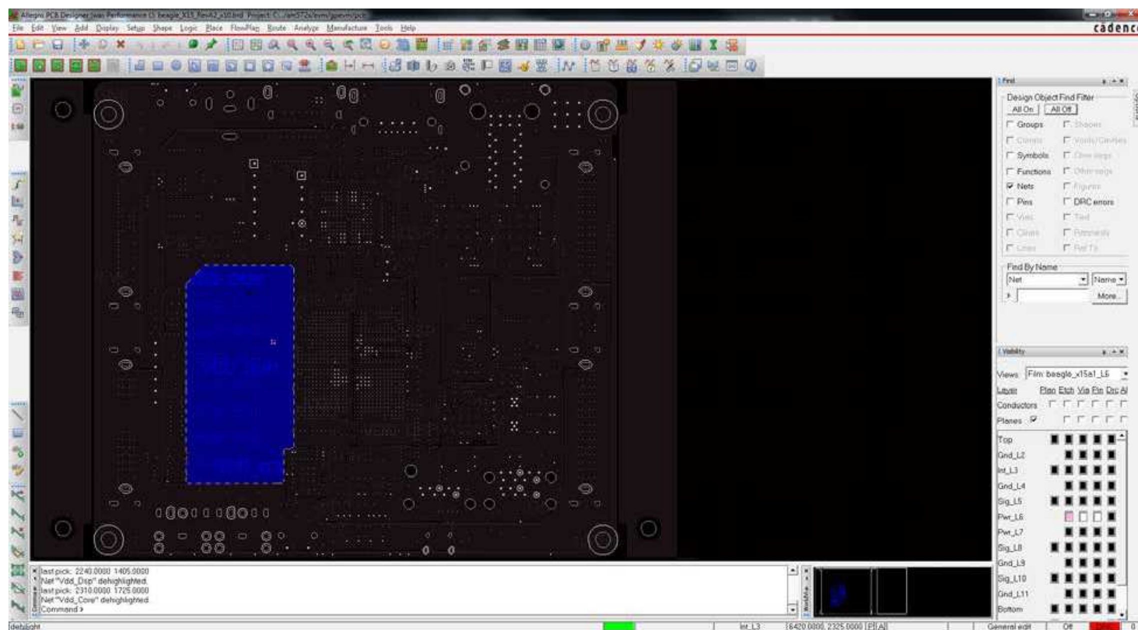

Figure 12. VDD_DDR Example (Layer 6)

6.1 Ir Drop

Loop resistance = 0.1581 mohm

VDD_DDR max drop due to trace resistance = 0.300 mV. With VDD_DDR sourced at 1.06 V from the PMIC, the worst case level at SOC is 1.0597 V.

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6.2 Voltage Drop (resultant)

Figure 13 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_DDR power net.

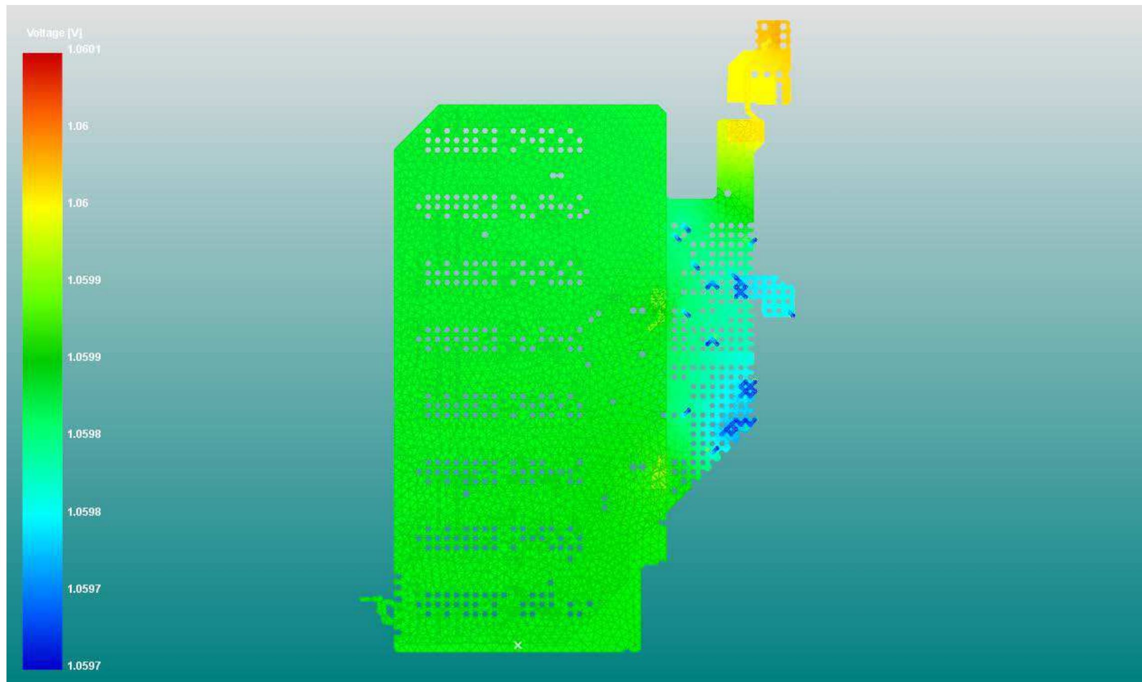

Figure 13. VDD_DDR Voltage Drop (resultant)

6.3 Current Density

Figure 14 shows the current density within the power trace. To determine the amount of current in any portion of the trace, see the color scale map on the left side.

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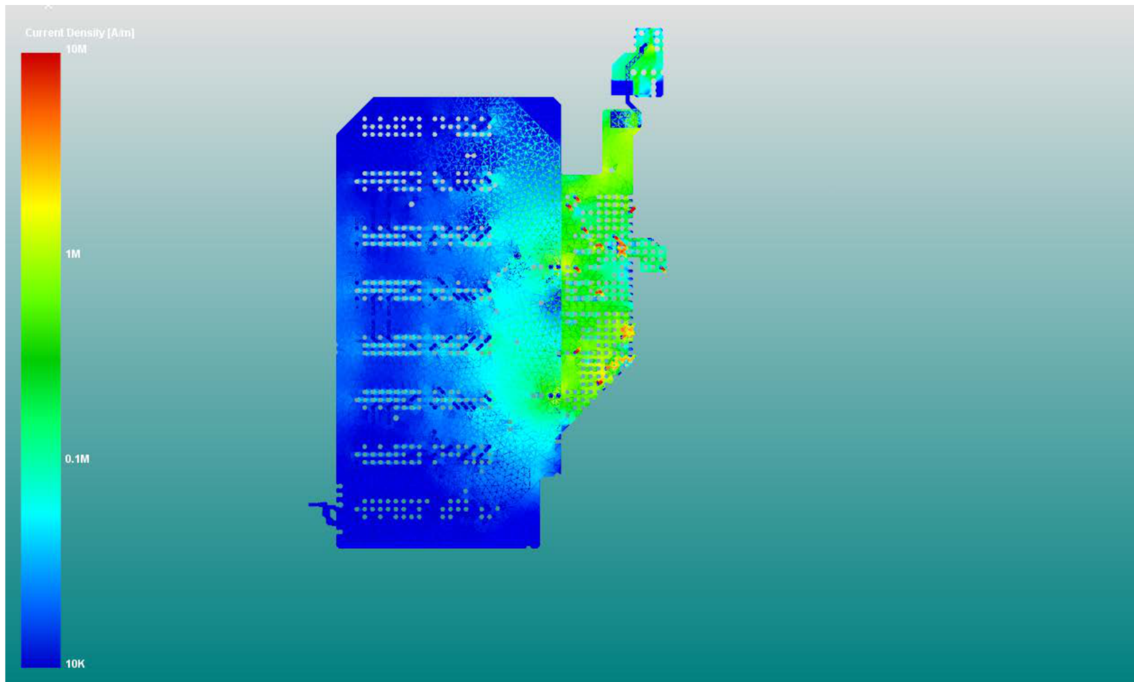

Figure 14. VDD_DDR Current Density

6.4 Loop Inductance Value

Estimations of the decoupling capacitor loop inductance values help to show whether the capacitor placement and routing is acceptable for each power net. Minimizing the loop inductance for each decoupling capacitor is important, within reason, in order to lower the overall inductance that the processor power pins see to the decoupling capacitors.

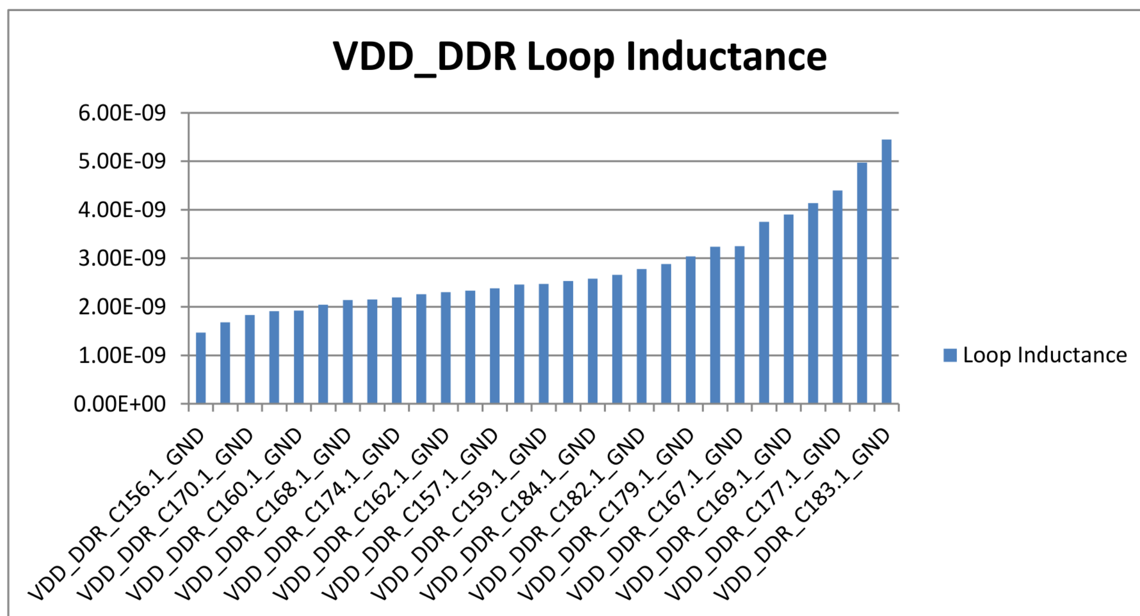

Figure 15. VDD_DDR Loop Inductance Value

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Table 5. Loop Inductance Value Table

VDD_DDR_C156.1_GND	1.47E-09
VDD_DDR_C157.1_GND	2.38E-09
VDD_DDR_C158.1_GND	2.66E-09
VDD_DDR_C159.1_GND	2.47E-09
VDD_DDR_C160.1_GND	1.92E-09
VDD_DDR_C161.1_GND	2.04E-09
VDD_DDR_C162.1_GND	2.30E-09
VDD_DDR_C163.1_GND	2.53E-09
VDD_DDR_C164.1_GND	2.15E-09
VDD_DDR_C165.1_GND	1.91E-09
VDD_DDR_C166.1_GND	2.88E-09
VDD_DDR_C167.1_GND	3.25E-09
VDD_DDR_C168.1_GND	2.14E-09
VDD_DDR_C169.1_GND	3.90E-09
VDD_DDR_C170.1_GND	1.83E-09
VDD_DDR_C171.1_GND	4.97E-09
VDD_DDR_C172.1_GND	2.33E-09
VDD_DDR_C173.1_GND	2.46E-09
VDD_DDR_C174.1_GND	2.19E-09
VDD_DDR_C175.1_GND	3.24E-09
VDD_DDR_C176.1_GND	3.75E-09
VDD_DDR_C177.1_GND	4.40E-09
VDD_DDR_C178.1_GND	2.26E-09
VDD_DDR_C179.1_GND	3.04E-09
VDD_DDR_C180.1_GND	1.68E-09
VDD_DDR_C181.1_GND	4.14E-09
VDD_DDR_C182.1_GND	2.78E-09
VDD_DDR_C183.1_GND	5.45E-09
VDD_DDR_C184.1_GND	2.58E-09

Space is limited for placing power decoupling capacitors on AM572x-based designs that place a premium on low-cost, reduced footprint PCBs. However, care was taken to place the bulk and decoupling capacitors in optimal locations that provide sufficient filtering of the input power to the processor. This is a tradeoff between processor power nets since there is not enough physical room to place all of the capacitors (for all power nets) close to the processor itself.

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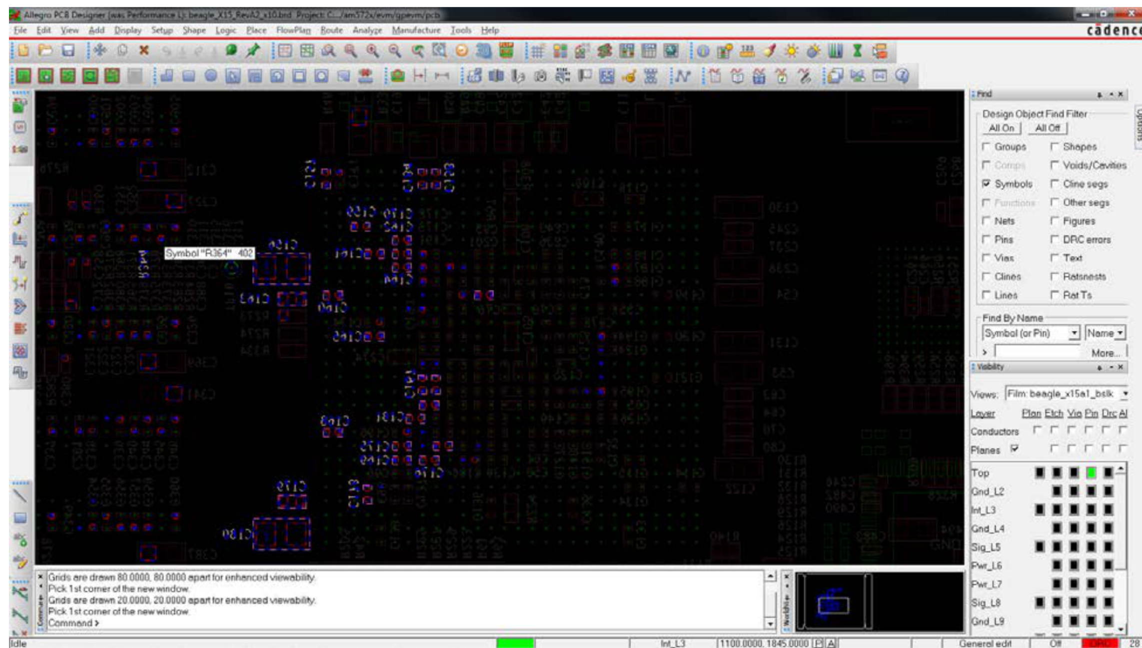

Figure 16. VDD_DDR Loop Inductance Value

6.5 Power Trace Impedance

Trace Impedance @ 50 MHz = 36.0 mohms

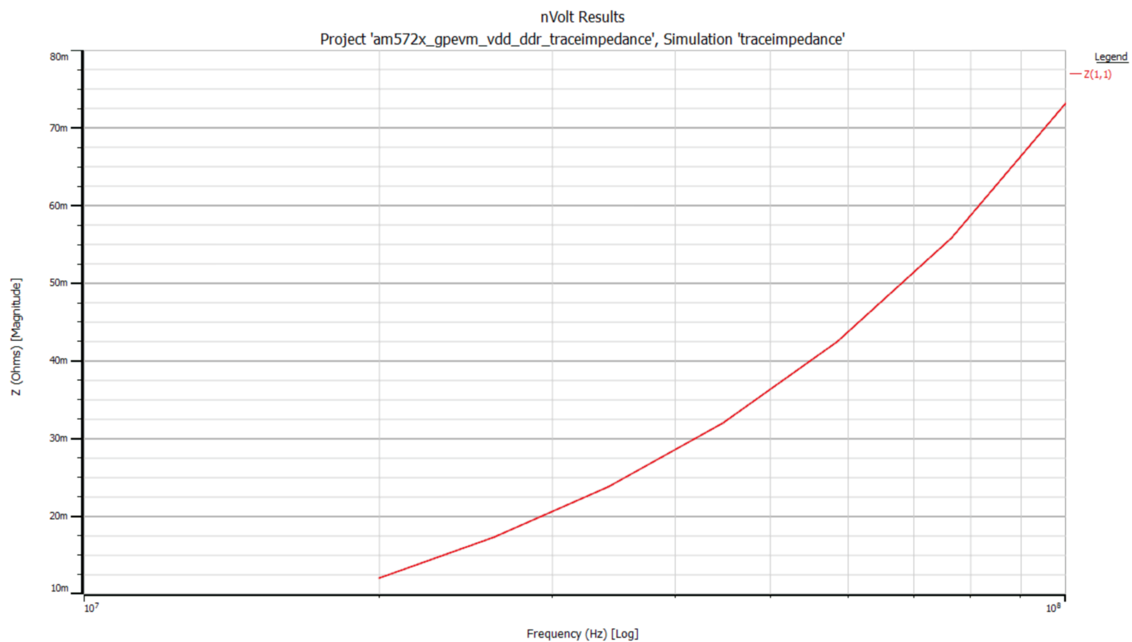

Figure 17. VDD_DDR Power Trace Impedance

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7 VDD_CORE

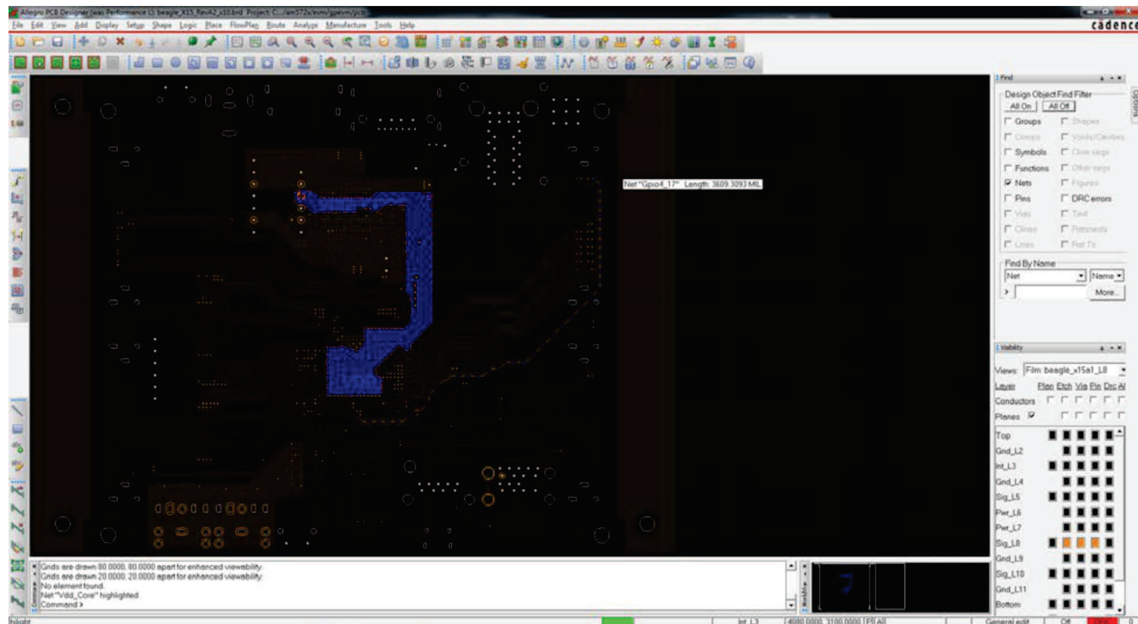

Figure 18. VDD_CORE Example (Layer 8)

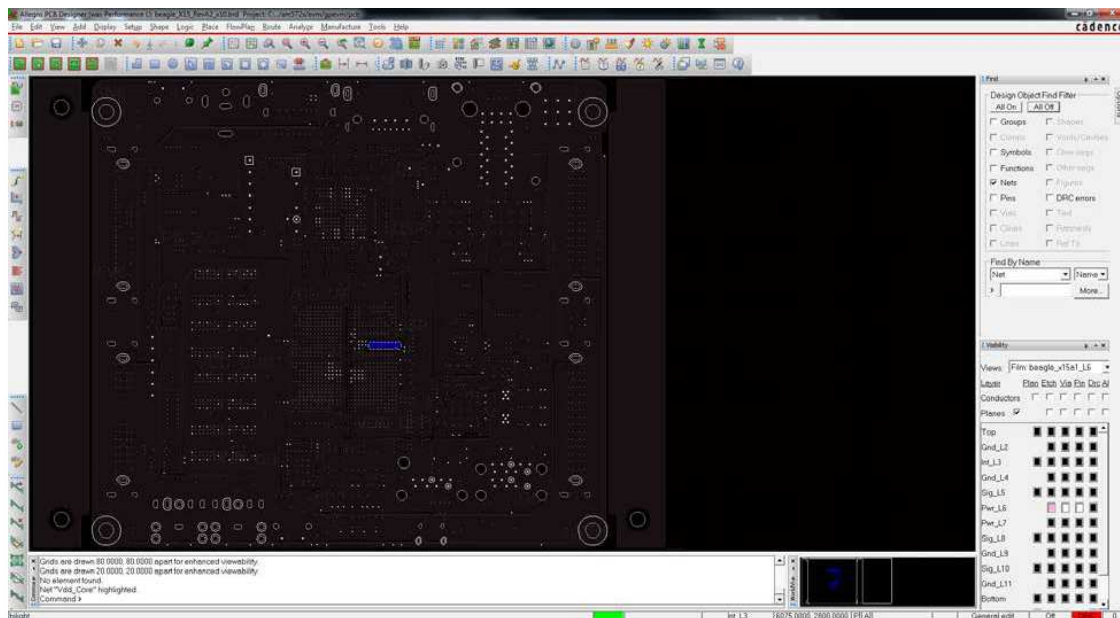

Figure 19. VDD_CORE Example (Layer 6)

7.1 Ir Drop

The loop resistance is 0.2174 mohm.

VDD_CORE max drop due to trace resistance = 0.420 mV. With VDD_CORE sourced at 1.03 V from the PMIC, the worst case voltage level at SOC is 1.02958 V.

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7.2 Voltage Drop (resultant)

Figure 20 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_CORE power net.

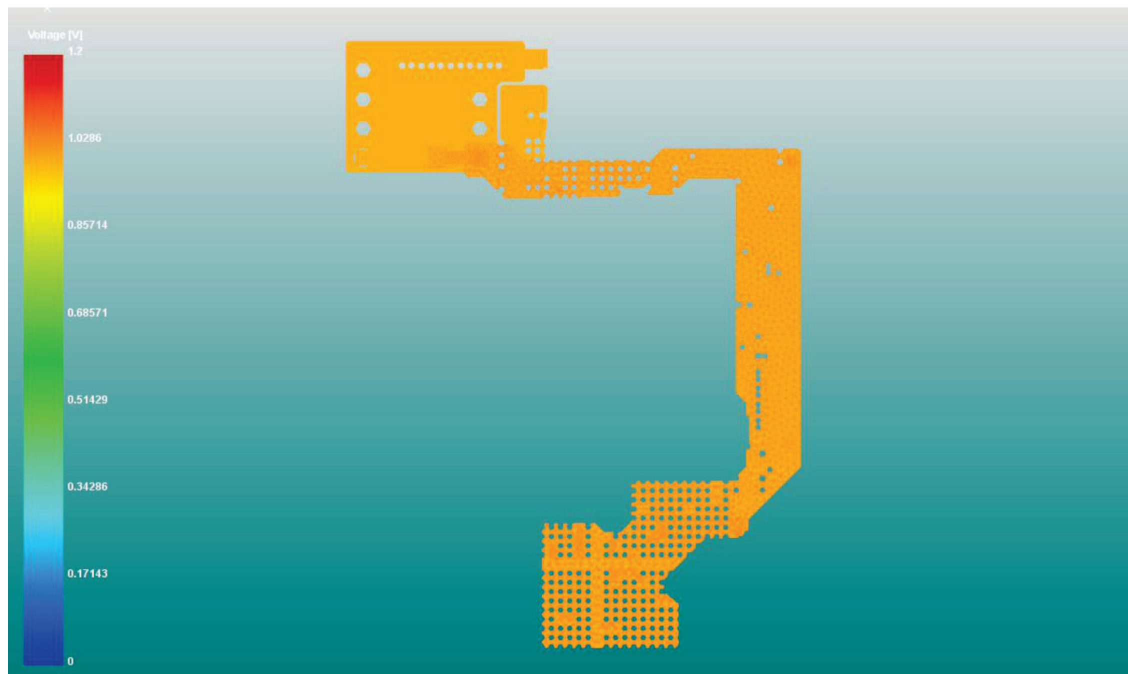

Figure 20. VDD_CORE Voltage Drop (resultant)

7.3 Current Density

Figure 21 shows the current density within the power trace. To determine the amount of current in any portion of the trace, see the color scale map on the left side.

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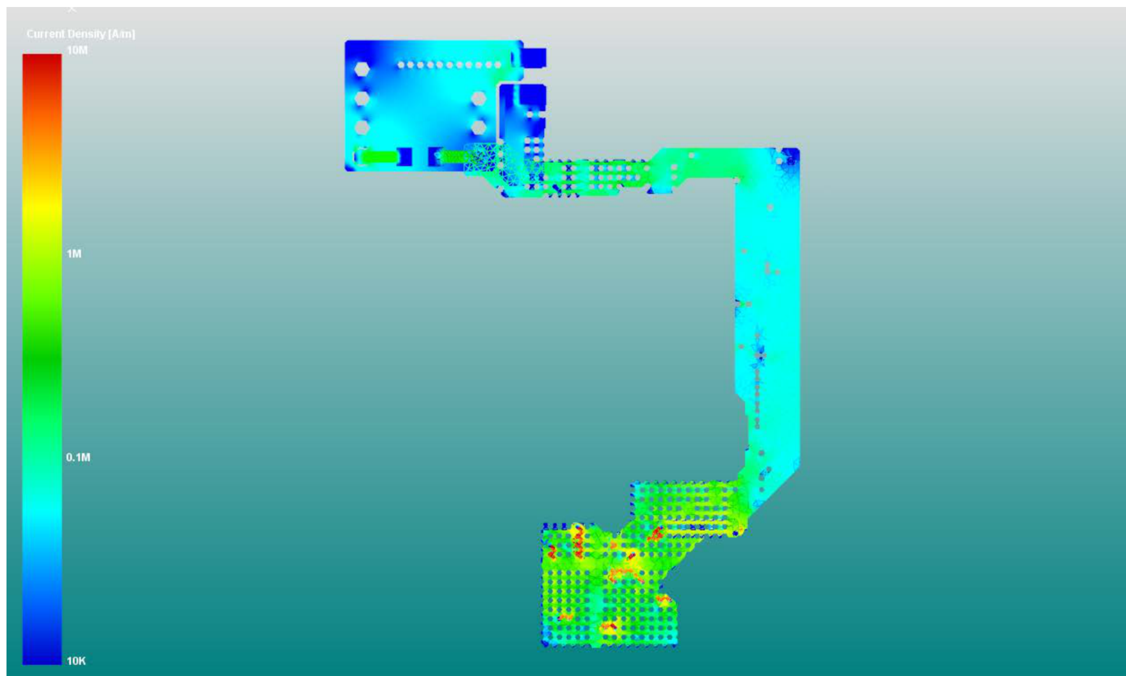

Figure 21. VDD_CORE Current Density

7.4 Loop Inductance Value

Estimations of the decoupling capacitor loop inductance values helps to show whether the capacitor placement and routing is acceptable for each power net. Minimizing the loop inductance for each decoupling capacitor is important, within reason, in order to lower the overall inductance that the processor power pins present to the decoupling capacitors.

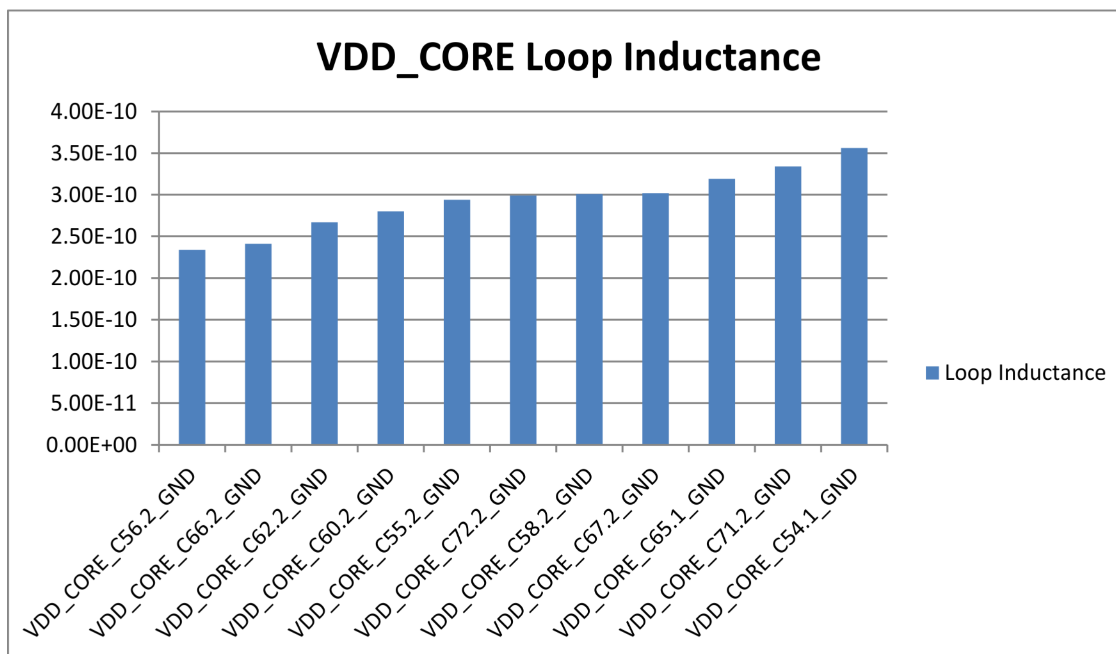

Figure 22. VDD_CORE Loop Inductance

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Table 6. VDD_CORE Loop Inductance Table

VDD_CORE_C54.1_GND	3.56E-10
VDD_CORE_C55.2_GND	2.94E-10
VDD_CORE_C56.2_GND	2.34E-10
VDD_CORE_C58.2_GND	3.01E-10
VDD_CORE_C60.2_GND	2.80E-10
VDD_CORE_C62.2_GND	2.67E-10
VDD_CORE_C65.1_GND	3.19E-10
VDD_CORE_C66.2_GND	2.41E-10
VDD_CORE_C67.2_GND	3.02E-10
VDD_CORE_C71.2_GND	3.34E-10
VDD_CORE_C72.2_GND	2.99E-10

7.5 Decoupling Capacitor Placement

Space is limited for placing power decoupling capacitors on AM572x-based designs that place a premium on low-cost, reduced footprint PCBs. However, care was taken to place the bulk and decoupling capacitors in optimal locations that provide sufficient filtering of the input power to the processor. This is a tradeoff between processor power nets since there is not enough physical room to place all of the capacitors (for all power nets) close to the processor itself.

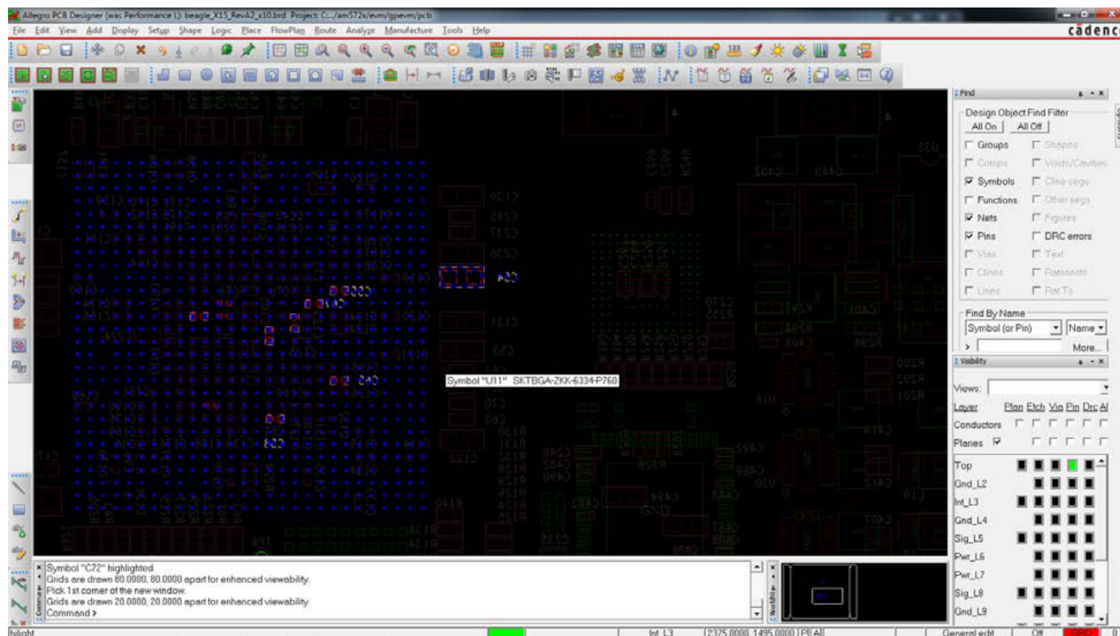

Figure 23. VDD_CORE Decoupling Capacitor Placement

7.6 Power Trace Impedance

Trace Impedance @ 50 MHz = 55.02 mohms

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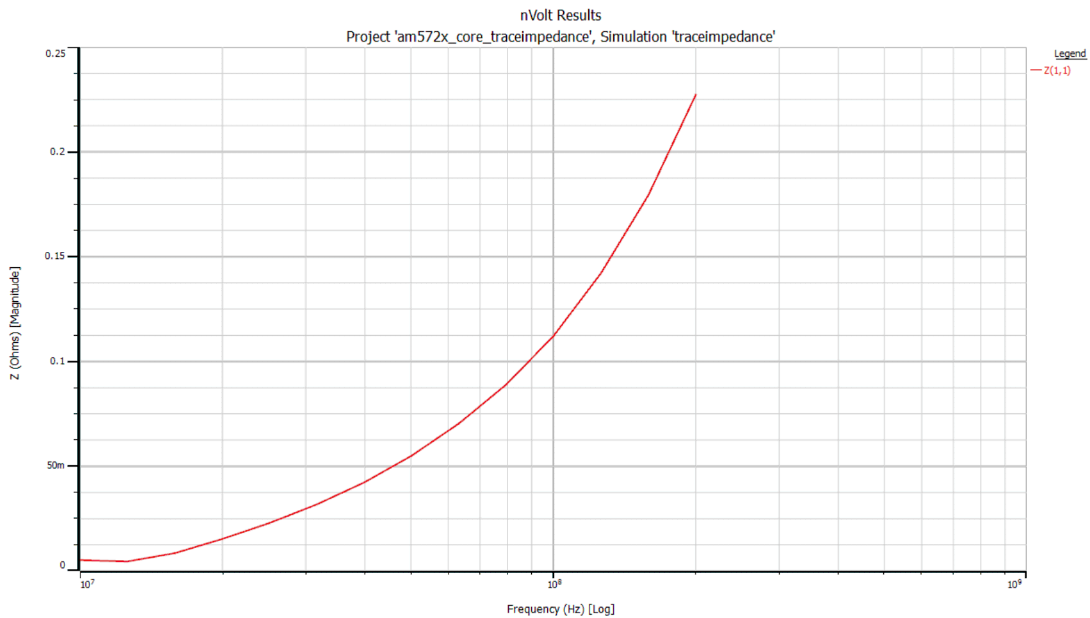

Figure 24. Trace Impedance

8 VDD_DSP

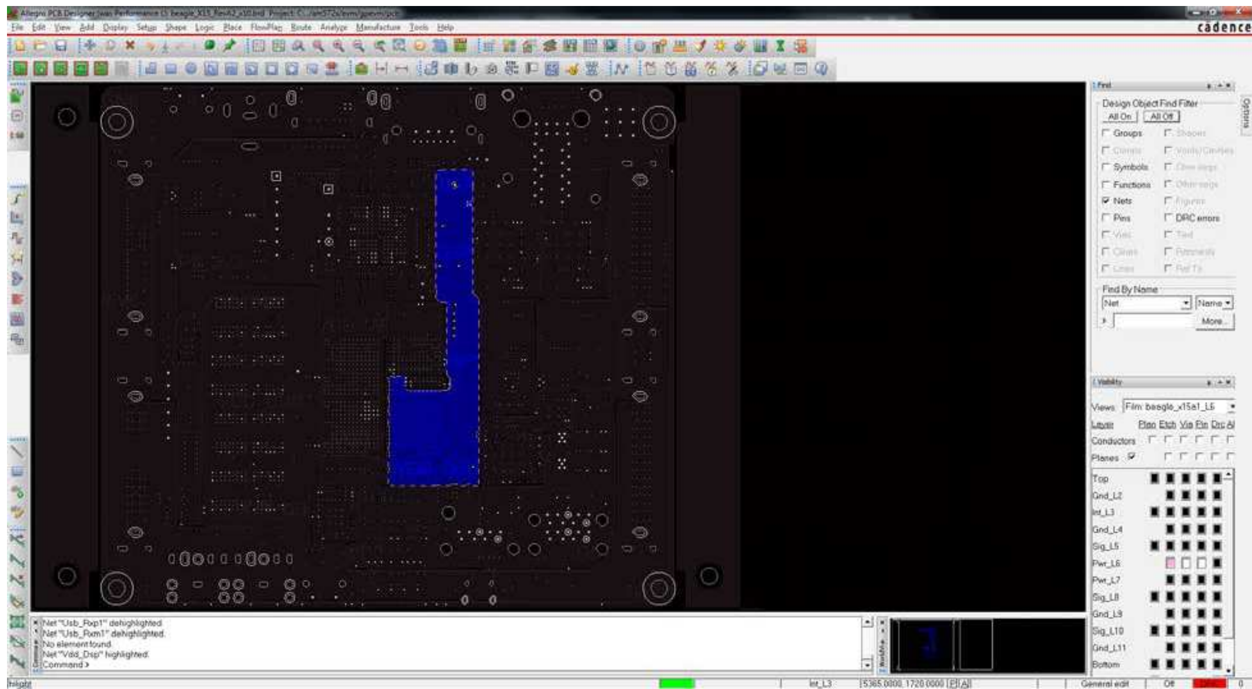

Figure 25. VDD_DSP Example (Layer 6)

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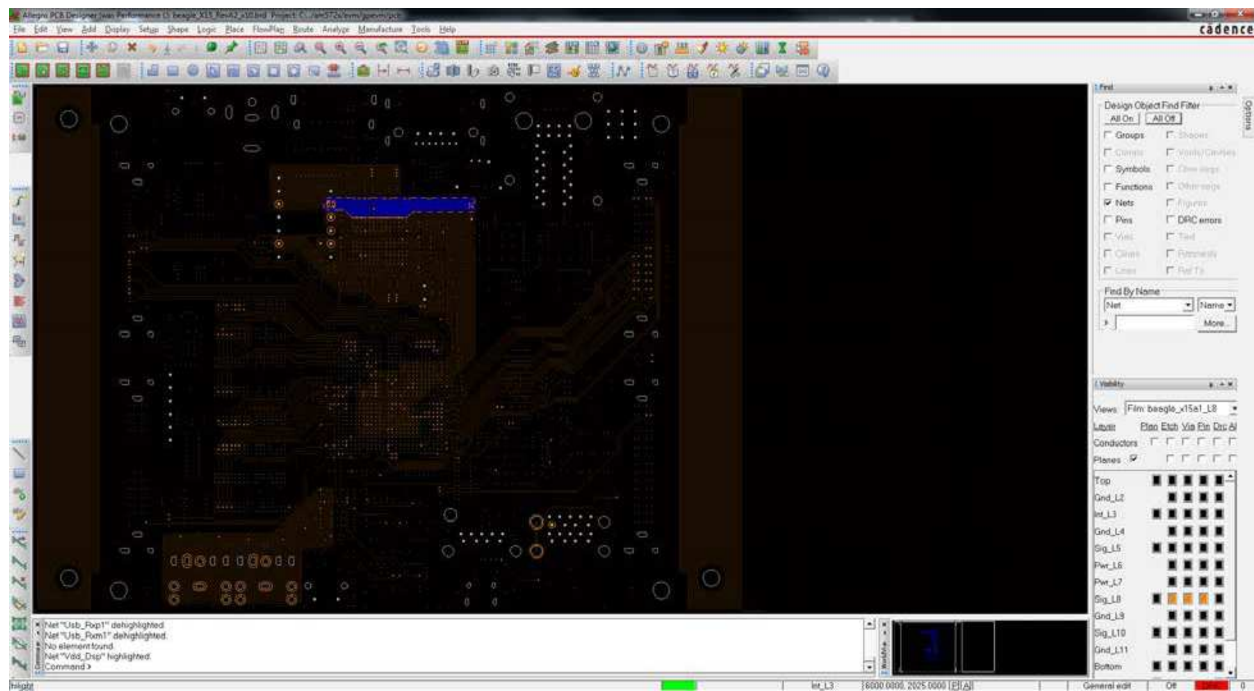

Figure 26. VDD_DSP (Layer 8)

Figure 27. VDD_DSP Example (Layer 9)

8.1 Ir Drop

The loop resistance = 0.3142 mohm.

VDD_DSP max drop due to trace resistance = 1.4 mV. With VDD_DSP sourced at 1.06 V from the PMIC, the worst case level at SOC is 1.0586 V.

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8.2 Voltage Drop (resultant)

Figure 28 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_DSP power net.

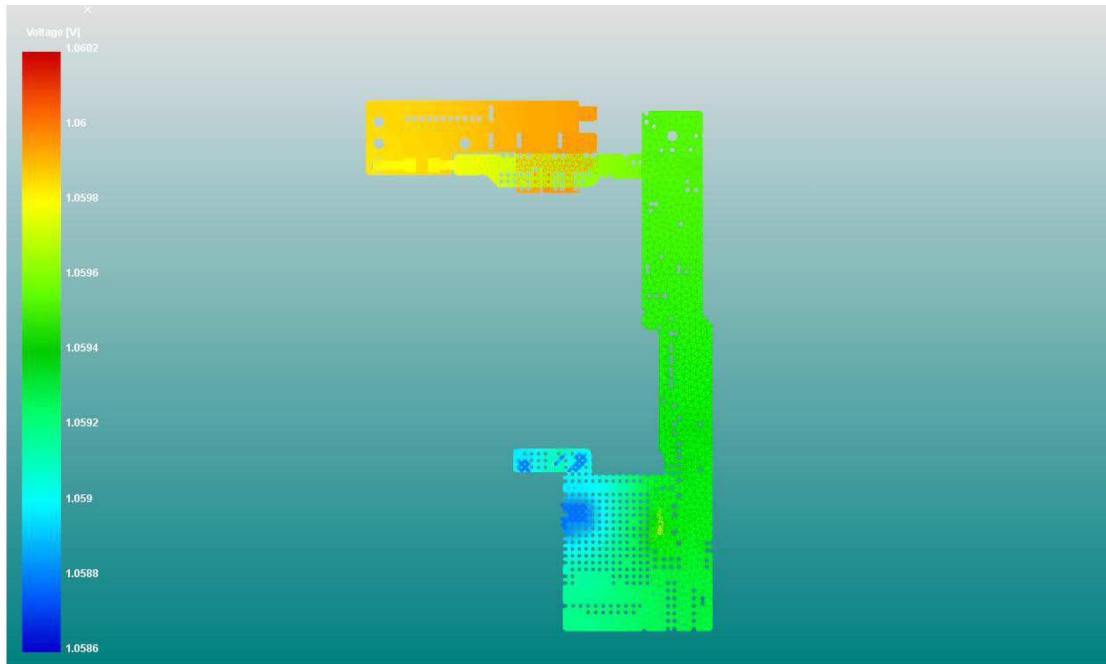

Figure 28. VDD_DSP Voltage Drop (resultant)

8.3 Current Density

Figure 29 shows the current density within the power trace. To determine the amount of current in any portion of the trace, see the color scale map on the left side.

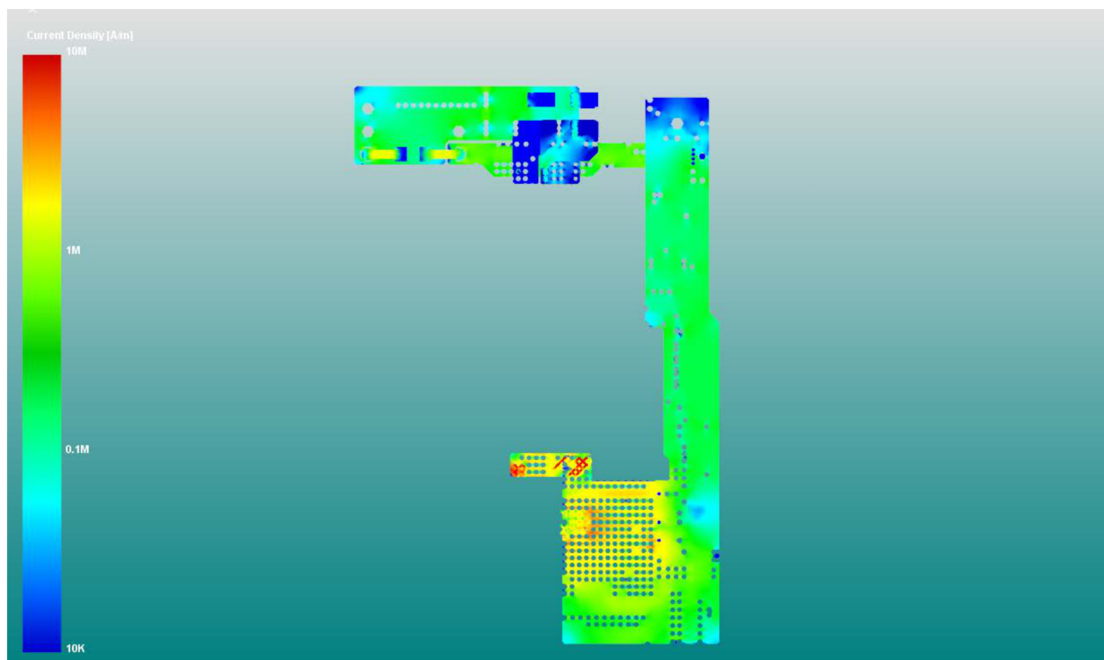

Figure 29. VDD_DSP Current Density

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8.4 Loop Inductance Value

Estimations of the decoupling capacitor loop inductance values helps to show whether the capacitor placement and routing is acceptable for each power net. Minimizing the loop inductance for each decoupling capacitor is important, within reason, in order to lower the overall inductance that the processor power pins present to the decoupling capacitors.

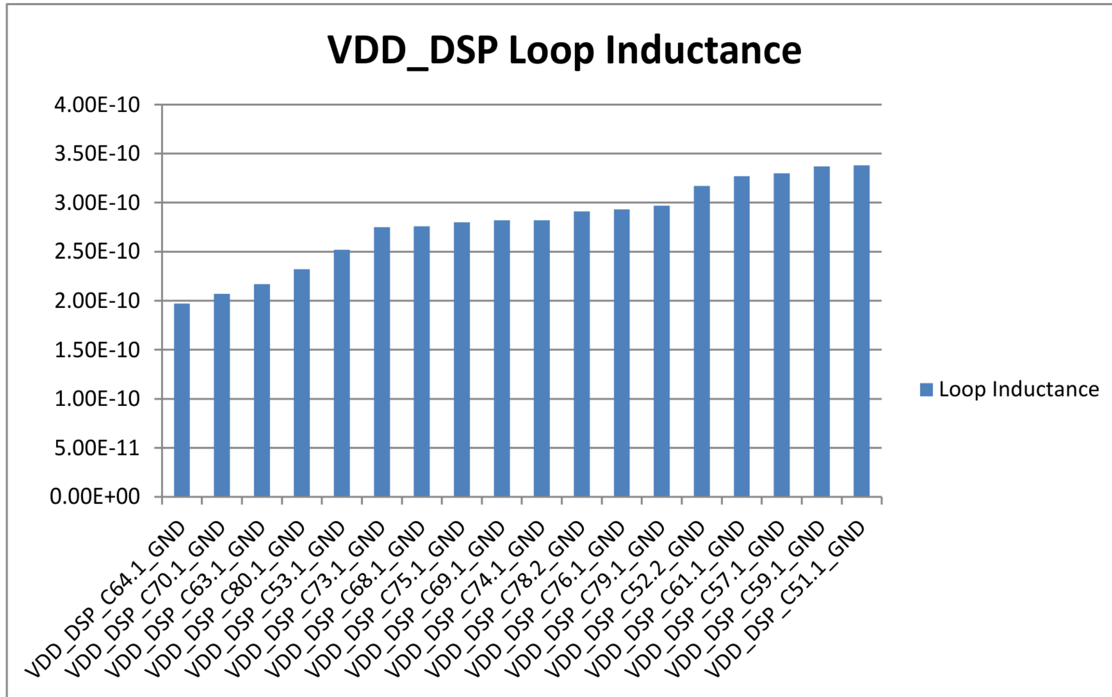

Figure 30. VDD_DSP Loop Inductance

Table 7. VDD_DSP Loop Inductance Table

Loop Inductance	50 MHz
VDD_DSP_C51.1_GND	3.38E-10
VDD_DSP_C52.2_GND	3.17E-10
VDD_DSP_C53.1_GND	2.52E-10
VDD_DSP_C57.1_GND	3.30E-10
VDD_DSP_C59.1_GND	3.37E-10
VDD_DSP_C61.1_GND	3.27E-10
VDD_DSP_C63.1_GND	2.17E-10
VDD_DSP_C64.1_GND	1.97E-10
VDD_DSP_C68.1_GND	2.76E-10
VDD_DSP_C69.1_GND	2.82E-10
VDD_DSP_C70.1_GND	2.07E-10
VDD_DSP_C73.1_GND	2.75E-10
VDD_DSP_C74.1_GND	2.82E-10
VDD_DSP_C75.1_GND	2.80E-10
VDD_DSP_C76.1_GND	2.93E-10
VDD_DSP_C78.2_GND	2.91E-10
VDD_DSP_C79.1_GND	2.97E-10
VDD_DSP_C80.1_GND	2.32E-10

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8.5 Decoupling Capacitor Placement

Space is limited for placing power decoupling capacitors on AM572x-based designs that place a premium on low-cost, reduced footprint PCBs. However, care was taken to place the bulk and decoupling capacitors in optimal locations that provide sufficient filtering of the input power to the processor. This is a tradeoff between processor power nets since there is not enough physical room to place all of the capacitors (for all power nets) close to the processor itself.

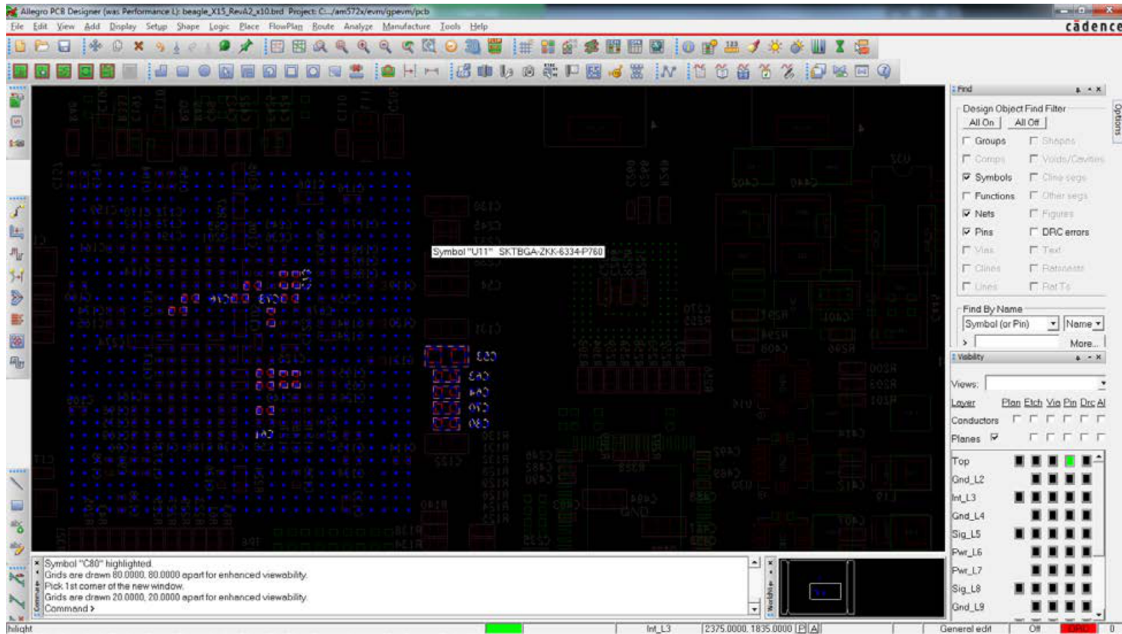

Figure 31. VDD_DSP Decoupling Capacitor Placement

8.6 Power Trace Impedance

Trace Impedance @ 50 MHz = 51.0 mohms

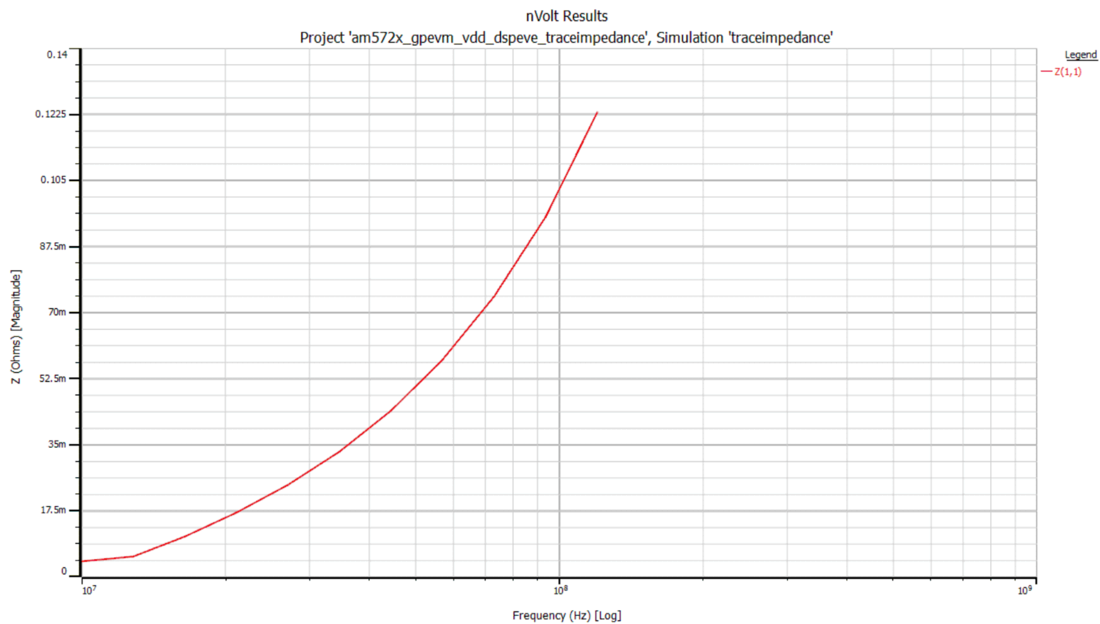

Figure 32. VDD_DSP Power Trace Impedance

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9 VDD_3V3

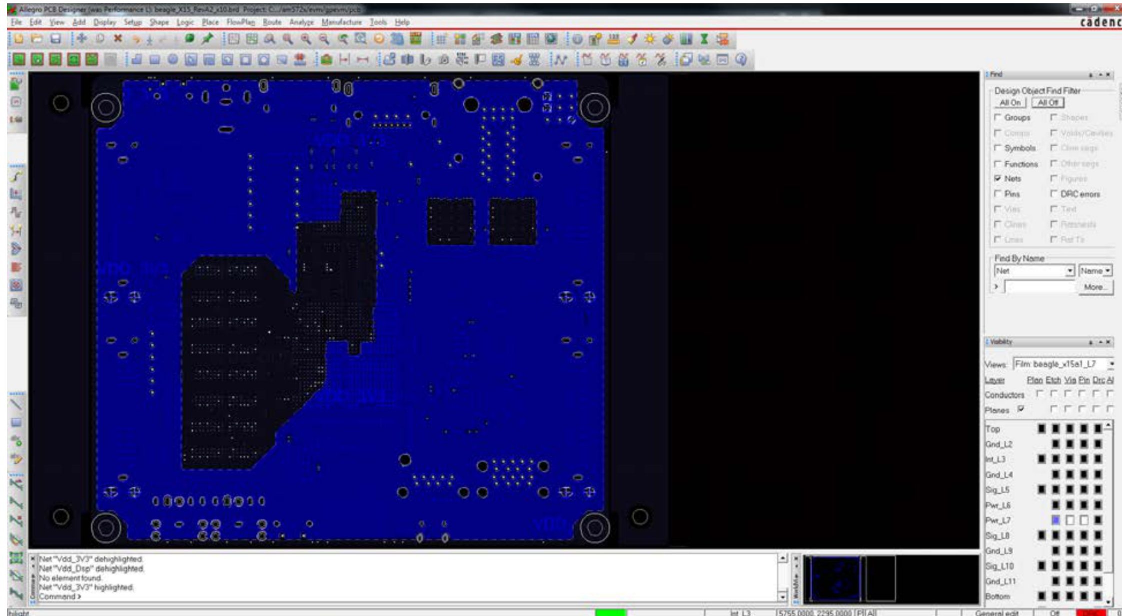

Figure 33. VDD_3V3

9.1 *Ir Drop*

Loop resistance = 0.1267 mohm

9.2 *Voltage Drop (resultant)*

Figure 34 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_3V3 power net.

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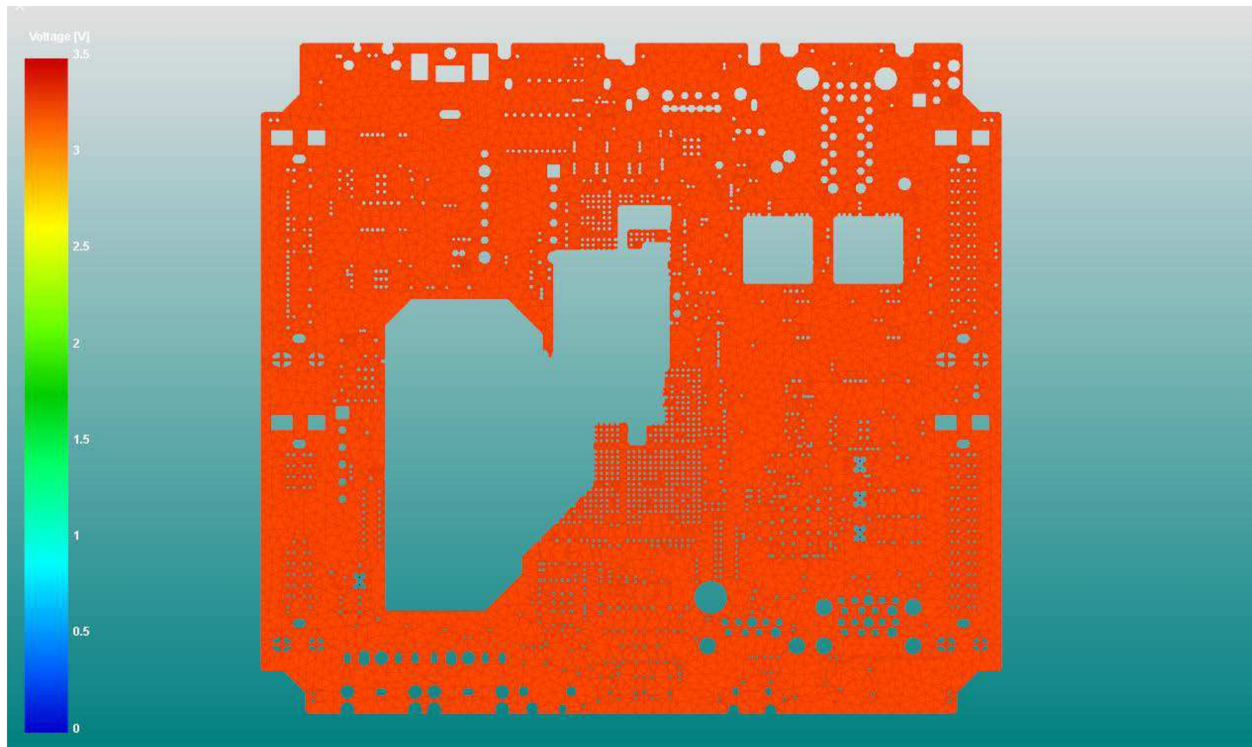

Figure 34. Voltage Drop (resultant)

9.3 Loop Inductance Value

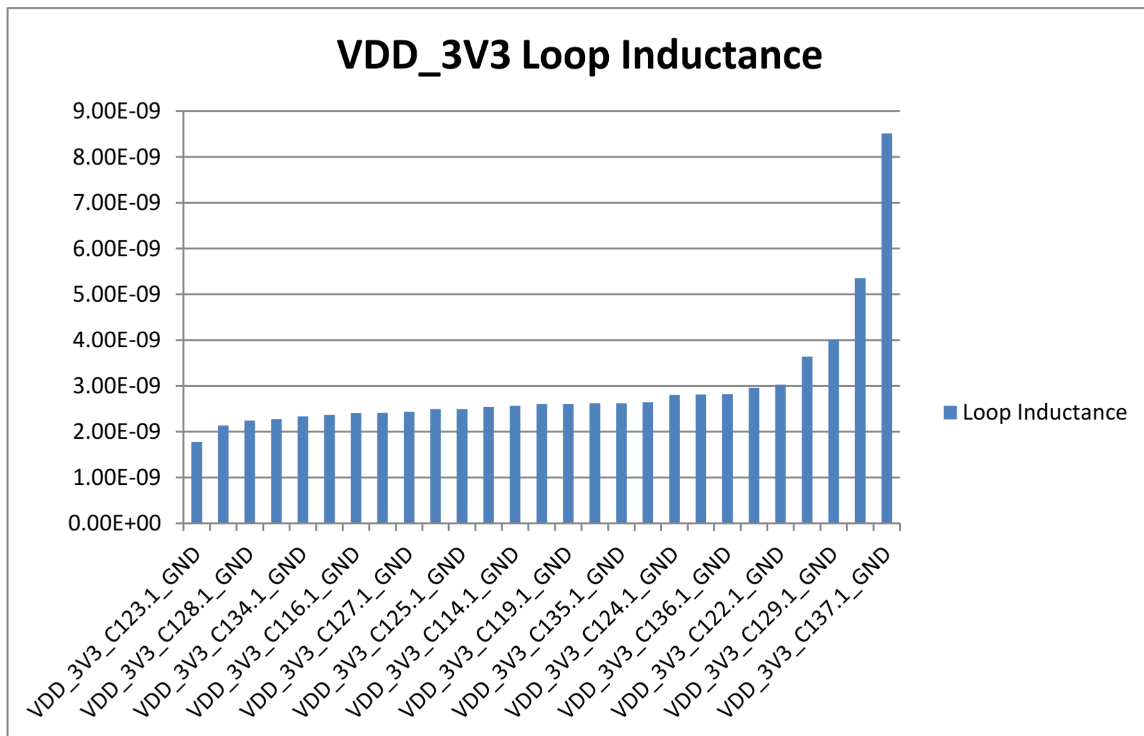

Figure 35. VDD_3V3 Loop Inductance

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Table 8. VDD_3V3 Loop Inductance Table

VDD_3V3_C113.1_GND	5.35E-09
VDD_3V3_C114.1_GND	2.56E-09
VDD_3V3_C115.1_GND	2.60E-09
VDD_3V3_C116.1_GND	2.40E-09
VDD_3V3_C117.1_GND	2.49E-09
VDD_3V3_C118.1_GND	2.62E-09
VDD_3V3_C119.1_GND	2.60E-09
VDD_3V3_C120.1_GND	2.41E-09
VDD_3V3_C121.1_GND	2.64E-09
VDD_3V3_C122.1_GND	3.02E-09
VDD_3V3_C123.1_GND	1.77E-09
VDD_3V3_C124.1_GND	2.80E-09
VDD_3V3_C125.1_GND	2.49E-09
VDD_3V3_C126.1_GND	2.54E-09
VDD_3V3_C127.1_GND	2.43E-09
VDD_3V3_C128.1_GND	2.24E-09
VDD_3V3_C129.1_GND	4.01E-09
VDD_3V3_C130.1_GND	3.64E-09
VDD_3V3_C131.1_GND	2.95E-09
VDD_3V3_C132.1_GND	2.27E-09
VDD_3V3_C133.1_GND	2.13E-09
VDD_3V3_C134.1_GND	2.33E-09
VDD_3V3_C135.1_GND	2.62E-09
VDD_3V3_C136.1_GND	2.82E-09
VDD_3V3_C137.1_GND	8.51E-09
VDD_3V3_C138.1_GND	2.36E-09
VDD_3V3_C139.1_GND	2.81E-09
VDD_3V3_C15.1_GND	6.67E-09
VDD_3V3_C263.2_GND	4.37E-09
VDD_3V3_C268.1_GND	2.81E-09
VDD_3V3_C269.1_GND	3.63E-09
VDD_3V3_C30.1_GND	4.86E-09
VDD_3V3_C389.1_GND	3.84E-09
VDD_3V3_C50.1_GND	3.99E-09
VDD_3V3_C81.1_GND	2.81E-09

9.4 Decoupling Capacitor Placement

Space is limited for placing power decoupling capacitors on AM572x-based designs that place a premium on low-cost, reduced footprint PCBs. However, care was taken to place the bulk and decoupling capacitors in optimal locations that provide sufficient filtering of the input power to the processor. This is a tradeoff between processor power nets since there is not enough physical room to place all of the capacitors (for all power nets) close to the processor itself.

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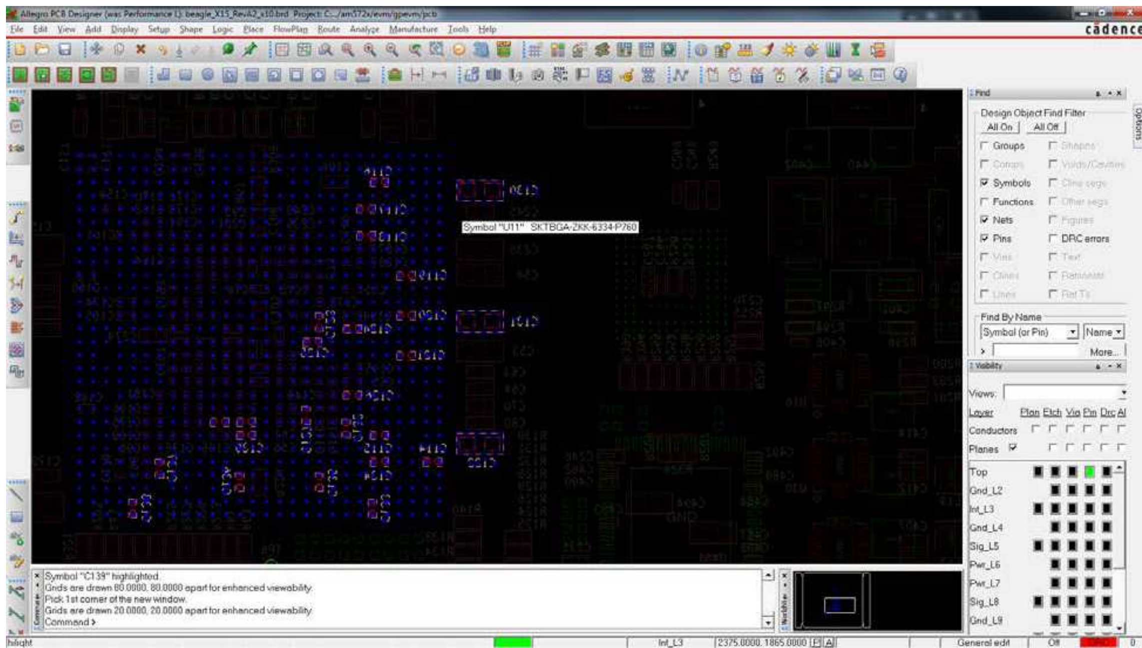

Figure 36. VDD_3V3 Decoupling Capacitor Placement

9.5 Power Trace Impedance

Trace Impedance @ 50 MHz = 45.5 mohms

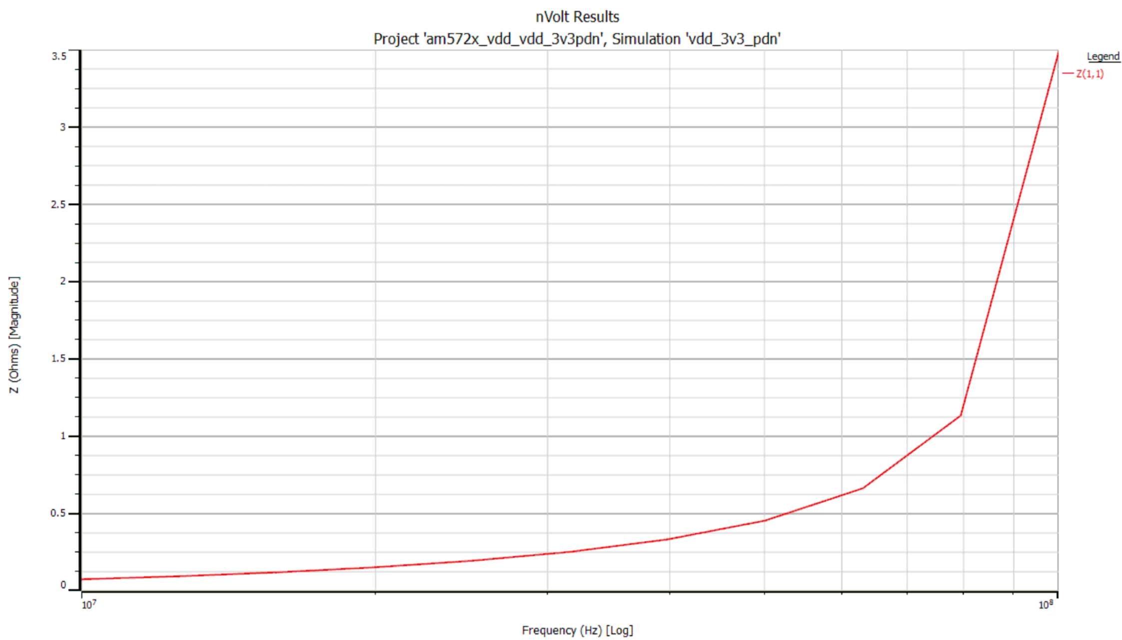

Figure 37. VDD_3V3 Power Trace Impedance

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10 VDD_1V8

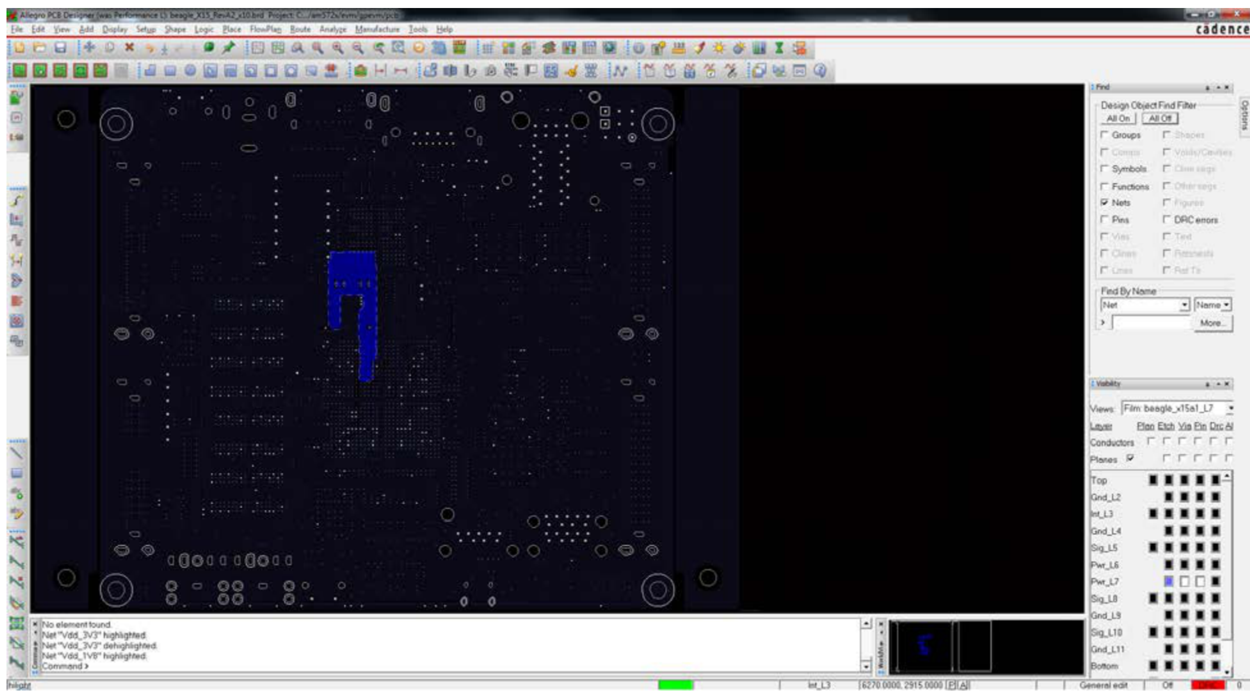

Figure 38. VDD_1V8 Example (Layer 7)

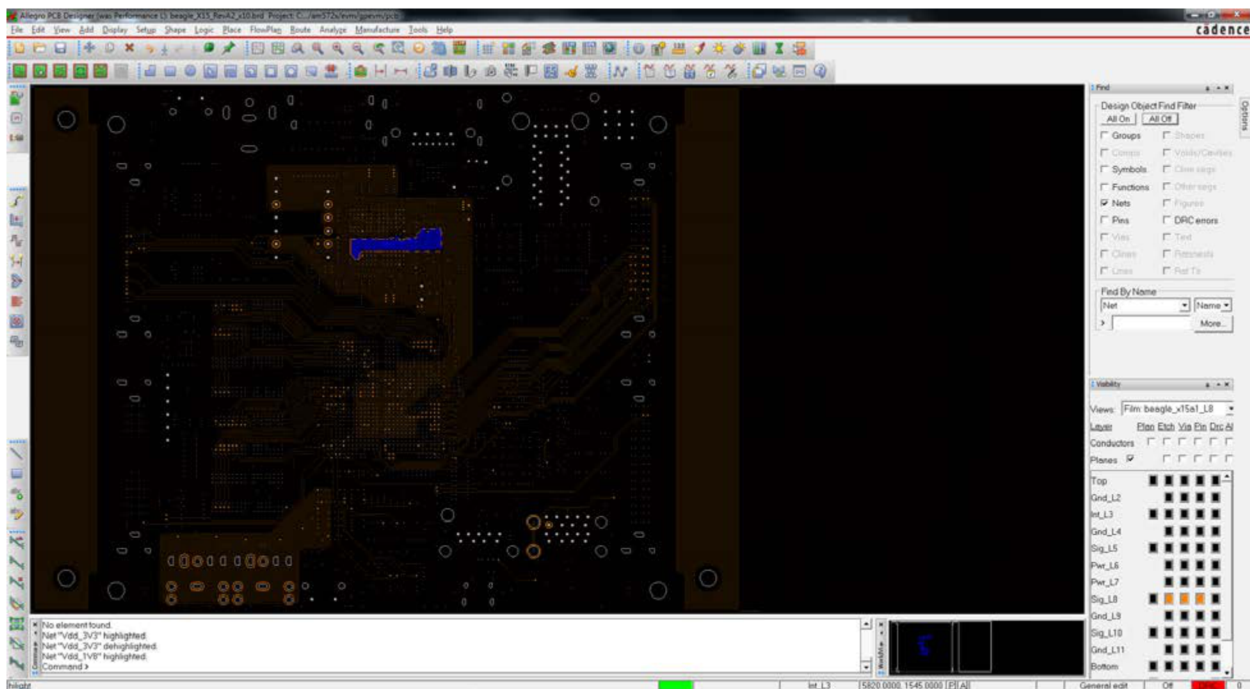

Figure 39. VDD_1V8 Example (Layer 8)

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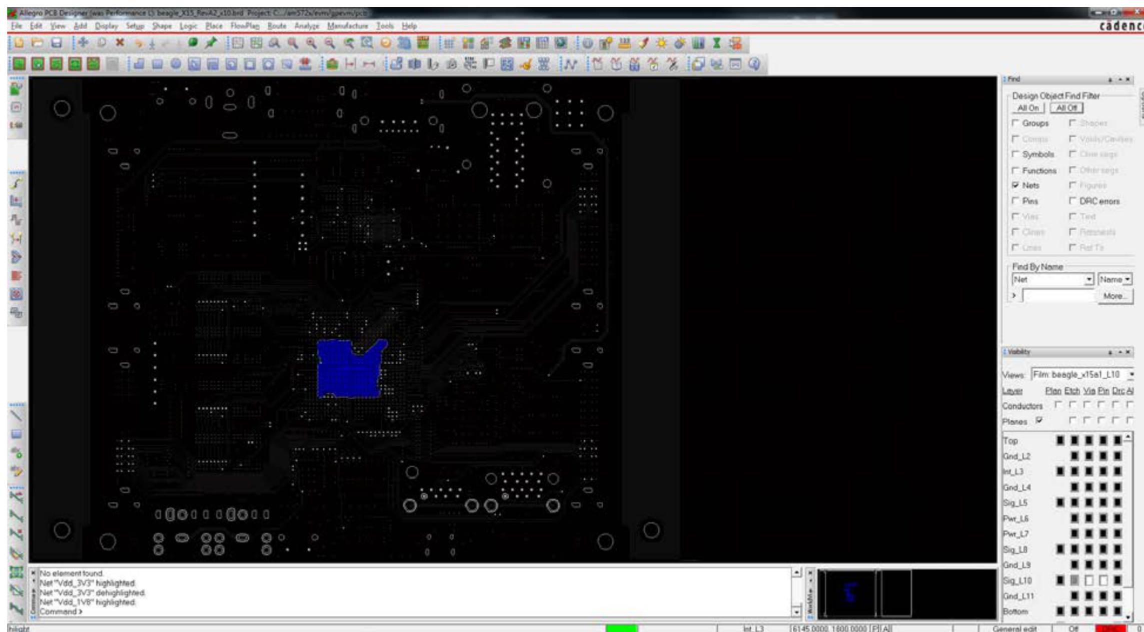

Figure 40. VDD_1V8 Example (Layer 10)

10.1 Ir Drop

Loop Resistance = 0.3624 mohm

1.79972 V

10.2 Voltage Drop (resultant)

Figure 41 shows the voltage drop from the PMIC to the processor pads. To decode the voltage value at each point on the power plane, see the color scale map on the left. This plot is a 2D view of all pertinent layers that contain the VDD_1V8 power net.

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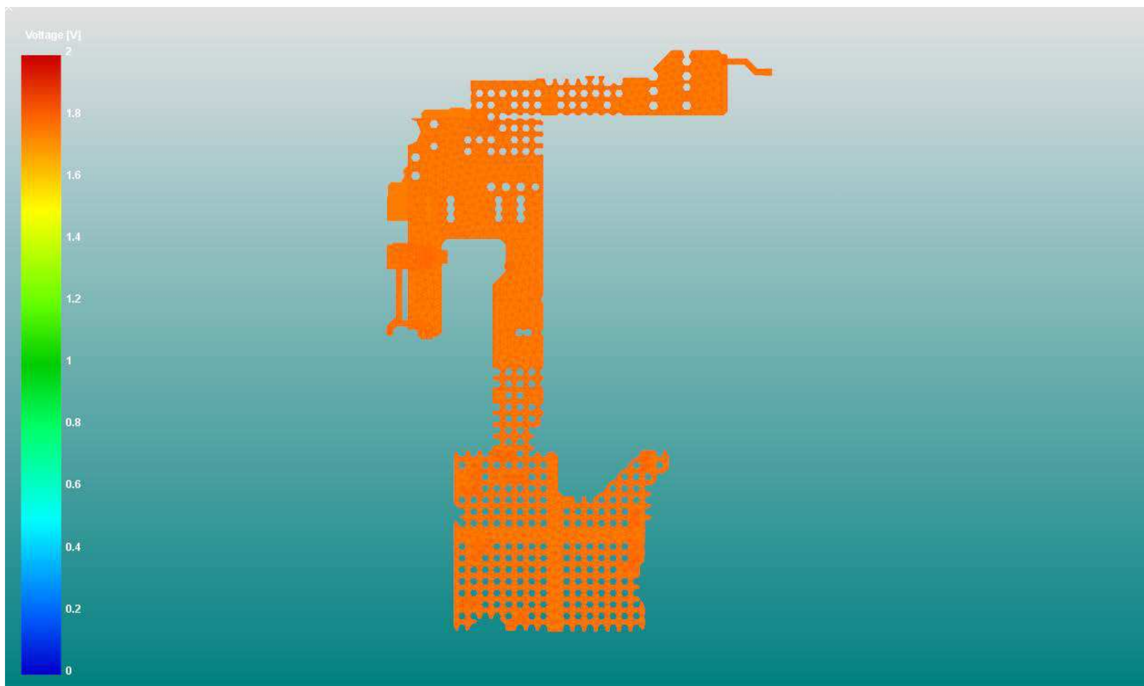

Figure 41. VDD_1V8 Voltage Drop (resultant)

10.3 Current Density

Figure 42 shows the current density within the power trace. To determine the amount of current in any portion of the trace, see the color scale map on the left side.

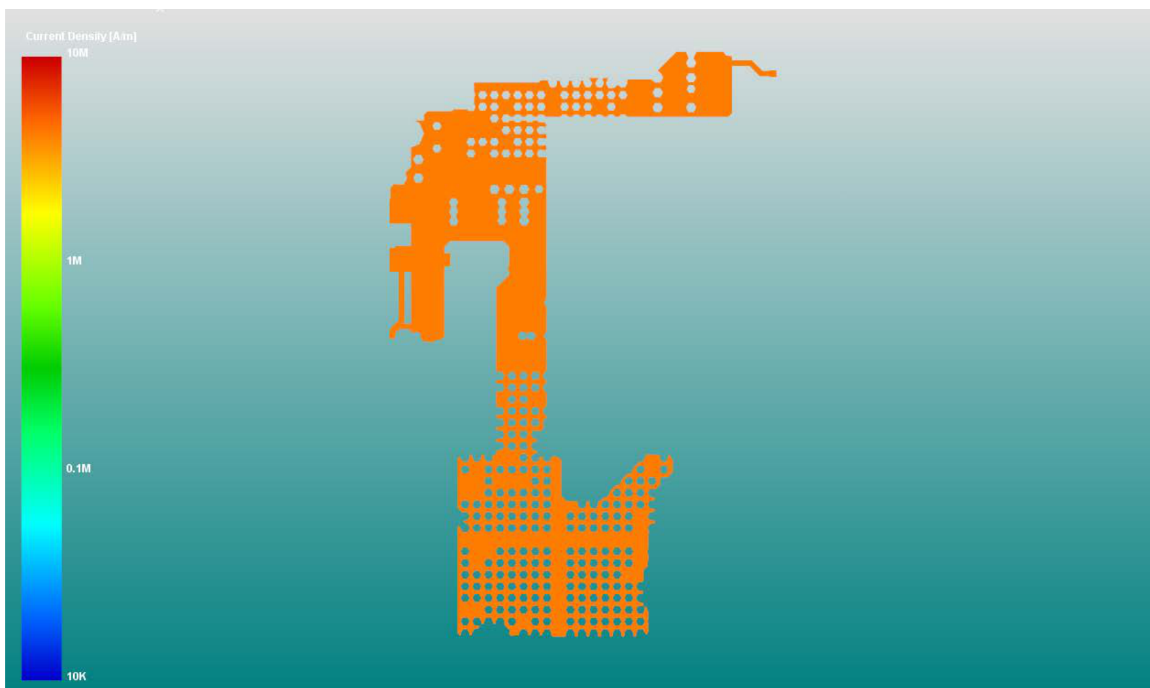

Figure 42. VDD_1V8 Current Density

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10.4 Power Trace Impedance

Trace Impedance @ 50 MHz = 63.5 mohms

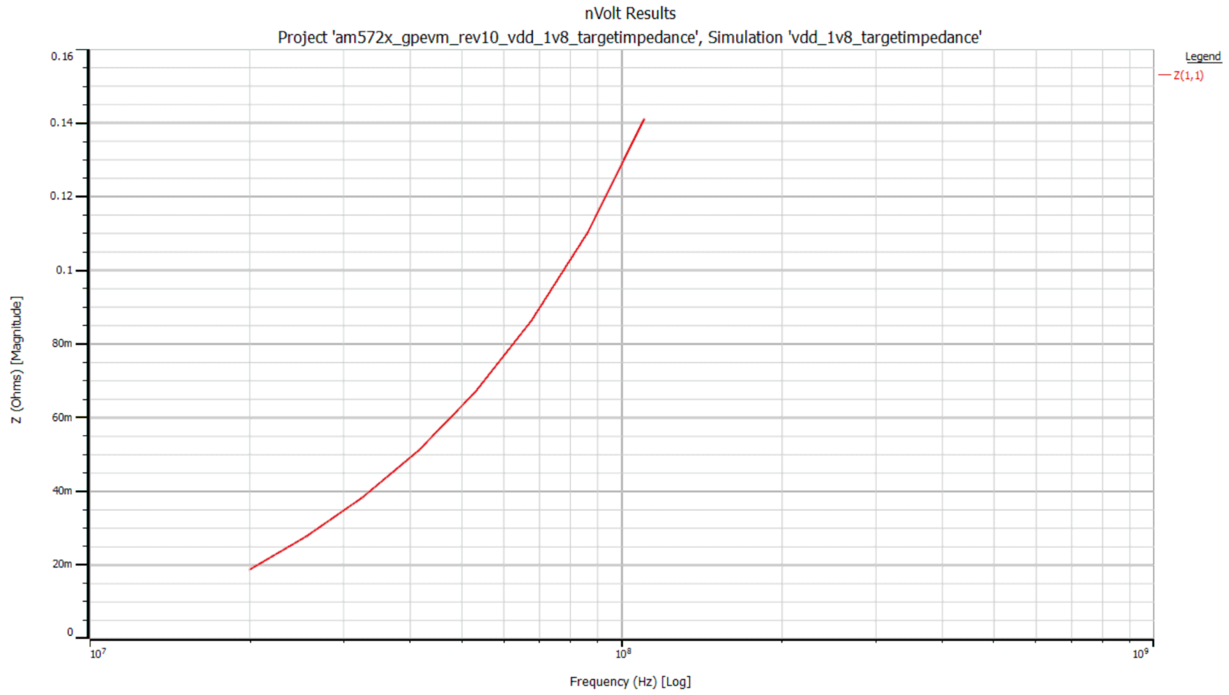

Figure 43. VDD_1V8 Trace Impedance

11 References

- *AM572x Embedded Applications Processor Data Manual* (SPRS915)

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