Application Report
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AM57xx BGA PCB Design

Catalolg Processors

ABSTRACT

This application report is designed to help customers understand what is involved with PCB design for AM57xx BGAs.

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Trademarks

1 Introduction

The AM57xx family of processors are housed in a 23 mm x 23 mm package which has a 0.80 mm pitch ball array of 28 x 28. To minimize cost, this ball grid is nearly a solid array. There are some open ball positions. Also, customer designs will normally have unused balls. The gaps created by the open ball positions, unused balls and the power and ground balls in the outer ball rows can be considered open via channels to simplify BGA breakout and routing if blind or buried vias are used. This ball map is not a true Via Channel Array.

Every PCB design is different in the BGA signal escape requirements. There are many different ways to escape the BGA for routing effectiveness. Considerations for PCB fabrication cost must be balanced against signal integrity requirements. For an example of BGA escape using simple through-hole vias, see the *PCB Layout* for the *AM572x General Purpose EVM Hardware* [2]. For an example of BGA escape using buried vias and micro vias in an HDI stack-up, see the PCB layout for the *AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware User's Guide* [3].

2 BGA Ball Pad Size

One of the most common questions we get is about what ball pad size to use. Optimal BGA ball pad size is easily found by referencing the IPC.org specifications for ball pad sizing. The IPC is an organization that is made up of hundreds of PCB manufacturers and assemblers worldwide working together to determine the optimal specifications for high PCB yield and reliability including BGA ball pads.

The IPC has a specification called IPC-7351A. This specification provides recommendations for all known BGA ball sizes. Table 1 shows the optimal ball pad size for any BGA design.

Table 1. IPC-7351A for NSMD Pads

Nominal Ball Diameter (1)	Reduction	Land Pattern Density Level	Nominal Land Diameter	Land Variation
0.75	25%	A	0.55	0.60-0.50
0.65	25%	A	0.50	0.55-0.45
0.6	25%	A	0.45	0.50-0.40
0.55	25%	A	0.40	0.45-0.35
0.5	20%	B	0.40	0.45-0.35
0.45	20%	B	0.35	0.40-0.30
0.4	20%	B	0.30	0.35-0.25
0.35	20%	B	0.30	0.35-0.25
0.3	20%	B	0.25	0.25-0.20
0.25	20%	B	0.20	0.20-0.17
0.2	15%	C	0.17	0.20-0.14

(1) Nominal ball diameter can be found on the mechanical package section near the end of the device-specific data sheet.

The mechanical package is shown in the *Mechanical Packaging and Orderable Information* section of *AM572x Sitara Processor Data Manual* (SPRS915).

The mechanical drawing for the AM572x package shows that the nominal ball diameter is 0.5mm. Find 0.5mm on the left hand column and follow that to the column that says "Nominal Land Diameter". The recommendation for the ball pad size is 0.4mm.

The far left column shows acceptable manufacturing variances, not allowable design targets (all manufacturing has tolerances). You must use the "Nominal Land Diameter" column to determine the correct BGA ball pad design target size.

3 Solder Mask Defined Pads Versus Non-solder Mask Defined Pads

ince the AM572x BGA has 0.80 mm ball pitch, it is recommended that non-solder-mask-defined (NSMD) PCB pads be used for mounting the device to the board. With the NSMD method, the opening in the solder mask is slightly larger than the copper pad, providing a small clearance between the edge of the solder mask and the pad.

While the size control is dependent on copper etching and is not as accurate as the solder mask defined method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. NSMD lands are recommended for small-pitch BGA packages because more space is left between the copper lands for signal traces. For more details on this topic, see the *Flip Chip Ball Grid Array Package Reference Guide* [4].

4 Ball Pattern Array Types

For embedded processors, TI makes two types of BGAs:

- Standard BGA arrays. These are characterized by the standard footprint which is usually either a full array (fully populated), or an array with a "moat" (a square of depopulated balls in the array that separates the inner array, which is mostly power and ground balls, from the outer array of signals, which primarily contains signal balls).
- Via Channel arrays. These are BGA arrays that have sections, or channels, of depopulated balls. When viewed from above, the ball pattern looks like an explosion or snowflake pattern. These arrays are specifically designed to reduce PCB cost by allowing large PCB feature sizes and reduced PCB layers. If a part uses a Via Channel BGA array, it is mentioned on the bulleted list on the first few pages of the *AM437x Sitara™ Processors Data Manual* [5] and there should be a PCB layout application report like *OMAP35x 0.65mm Pitch Layout Methods* [6]. Only TI makes Via Channel parts.

4.1 What is Via Channel?

Via Channel is a TI feature specifically designed to reduce PCB manufacturing cost by placing the BGA balls in patterns specifically designed for optimal via and trace placement. This feature uses a special BGA array design to allow two major advantages:

- Large PCB feature sizes (such as via, pad and trace widths) regardless of ball pitch
- Reduced PCB layer count (ball pattern enables increased layer efficiency)

Via Channel BGA arrays are designed to use standard PCB manufacturing processes (no micro vias or other HDI structures required) regardless of ball pitch, and they have reduced PCB layer requirements. Via Channel designs can be implemented in four total PCB layers (see the Via Channel PCB layer section below) with proper via and trace placement.

To learn more about this unique design feature, the following short slide set graphically explains how Via Channel works:

- "What is Via Channel" Presentation
  - "What is Via Channel" Presentation [1]

Below is an application report showing Via Channel routing for the OMAP 3530:

- *OMAP35x 0.65mm Pitch Layout Methods* [6]

4.2 PCB Feature Sizes For Standard BGAs

As stated previously, standard BGA arrays have tightly arranged balls. Therefore, this ball pattern dictates the PCB feature sizes and required number of signal routing layers. These figures can be arrived at with a calculator. However, be careful to make sure a line of the specified width can be used in between vias of the specified width. Just because a 16 mil via can be used on a 0.65 mm pitch part does not mean it's possible to route a 4 mil trace in between the vias.

Table 2. PCB Typical Feature Sizes For Standard (non-Via Channel) BGA Arrays

Ball Pitch	Via Diameter	Via Hole Trace Size	Trace Size	Clearance	Micro Vias?
0.8 mm pitch	18 mil	10-8 mil	4-5 mil	4 mil	No
0.65 mm pitch	16 mil (1) 12 mill	8 mil (1) 6 mill	4 mill (1) 4 mil	4 mill (1) 4 mil	No Yes
0.5 mm pitch	10 mil	5 mil	3 mil	3 mil	Yes
0.4 mm pitch	10-8 mil	5-4 mil	3 mil	3 mil	Yes

(1) 16 mil diameter/8 mil hole vias are only possible if done in a creative way that puts traces only in between every other via. In other words, 16/8 vias, when placed between the balls, will move enough to allow one 4 mil trace per pair, but not one 4 mil trace per via, so for some designs like the DM365 and DM355, 16/8 mil vias should be possible in your application since there are some areas to place vias in the array. However, for LC138, since it is a full array, it is not possible to use 16/8 vias unless only every other pin is not used (not likely). 16/8 vias are uncommon in the PCB fab world but some companies can do them without micro vias.

4.3 PCB Layer Count For Standard BGAs

The minimum number of signal routing layers required to route a particular design can be easily estimated once the signals and location of those signals is known. Assuming that the above required PCB feature sizes for that pitch are used, the PCB layers will be used as follows:

The first two rows will route on the top layer

The second two rows will route on a second layer

An additional PCB signal layer will be required for every row of signal balls in past the first 4.

So, if "Rows_in" equals the maximum number of signal ball rows in (from the outside of the BGA array) the centermost signal is located, then:

2 Rows_in = 1 PCB signal layer

3 Rows_in = 2 PCB signal layers

4 Rows_in = 2 PCB signal layers

5 Rows_in = 3 PCB signal layers

6 Rows_in = 4 PCB signal layers

7 Rows_in = 5 PCB signal layers

This assumes that all balls are routed because their signals are needed in the board design. If some signals are not needed, then those corresponding ball escape lanes are free for other signals. In this regard, less layers may be needed if the required signals have enough viable routing lanes.

So if a signal called I2C_CLK was required in the design, and it was located five rows in from the outside (counting all rows), then it would require three PCB signal layers, plus at least two PCB layers for power and ground, so that's 5 PCB layers total (actually 6 layers since boards are always constructed with an even number of layers for symmetry to minimize warpage).

4.4 PCB Feature sizes for Via Channel BGAs

If the Via Channel part, is used it has been specifically designed to reduce PCB costs. The PCB feature sizes are now independent of the ball pitch since the vias no longer have to be placed in between four balls. Via Channel also routes more signals out on lower layers. Where standard array trace density on lower PCB layers is limited by via interference of the traces, Via Channel designs are mostly free of this restriction, so more traces can be routed on fewer layers thereby reducing the number of PCB layers required. Most Via Channel board designs can be implemented in a four layer PCB (minimum).

Table 3. PCB Typical Feature Sizes For Via Channel BGA Arrays

Ball Pitch	Via Diameter	Via Hole Trace Size	Trace Size	Clearance	Micro Vias?
0.8 mm pitch	20 mil 18 mil	10-12 mil 10-8 mil	5 mil 4 mil	5 mil 4 mil	No
0.65 mm pitch	20 mil 18 mill	12-10 mil 10-8mill	4 mill 4 mil	4 mill 4 mil	No Yes
0.4 mm pitch	18 mil	10 mil	4 mil	4 mil	Yes

4.5 PCB Layer Count For Via Channel BGAs

Via Channel BGAs are specifically designed to require only four total PCB layers. Depending on the power requirements and the power signal routing, an additional power layer may be required bringing the PCB layer count to 6. With careful design this should be able to be avoided.

4.6 BGA Breakout for the AM57xx Devices

As stated previously, the AM57xx BGA package is a hybrid between a Standard BGA Array and a Via Channel Array. It only has a small number of open ball positions. Therefore, if using a through-hole via stack-up, the limitations and feature sizes discussed above will apply to the PCB design. However, if using the micro vias or some other type of blind and buried via technology, the open balls combined with unused ball positions and the power and ground ball positions can result in open via channels such that Via Channel Array routing techniques can be used. The design team must balance the layer count versus manufacturing complexity. Signal integrity requirements may also impact this decision since the AM572x devices have many high performance interfaces.

4.7 BGA Escape Routing Guidance

The following wiki page link provides specific guidance for BGA escape routing. It also contains images from the AM572 IDK to help designers implement their board layout.

- *General hardware design/BGA PCB design/BGA decoupling* [7]

5 BGA Decoupling (Bypass) Capacitor Selection and Placement

It is important to perform a power analysis on the board design to make sure the PCB can supply adequate current to the main power rails of the AM572x. Similarly, it is critical to properly implement power supply decoupling capacitors. For more information, see the *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

6 BGA Solder Reflow Profile

The solder reflow temperature and duration profile is critical to success in the IC mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder. Finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out or the temperature rises too fast to allow it to evaporate, many negative things happen. These range from solder-particle splatter to trapped gases, which can cause voids and embrittlement. A significant number of reliability problems with solder joints can be solved with a proper warm-up step, so this needs careful attention.

The second key point that successful reflow cycles have in common is uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming may lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package. Heating the paste too hot, too quickly before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

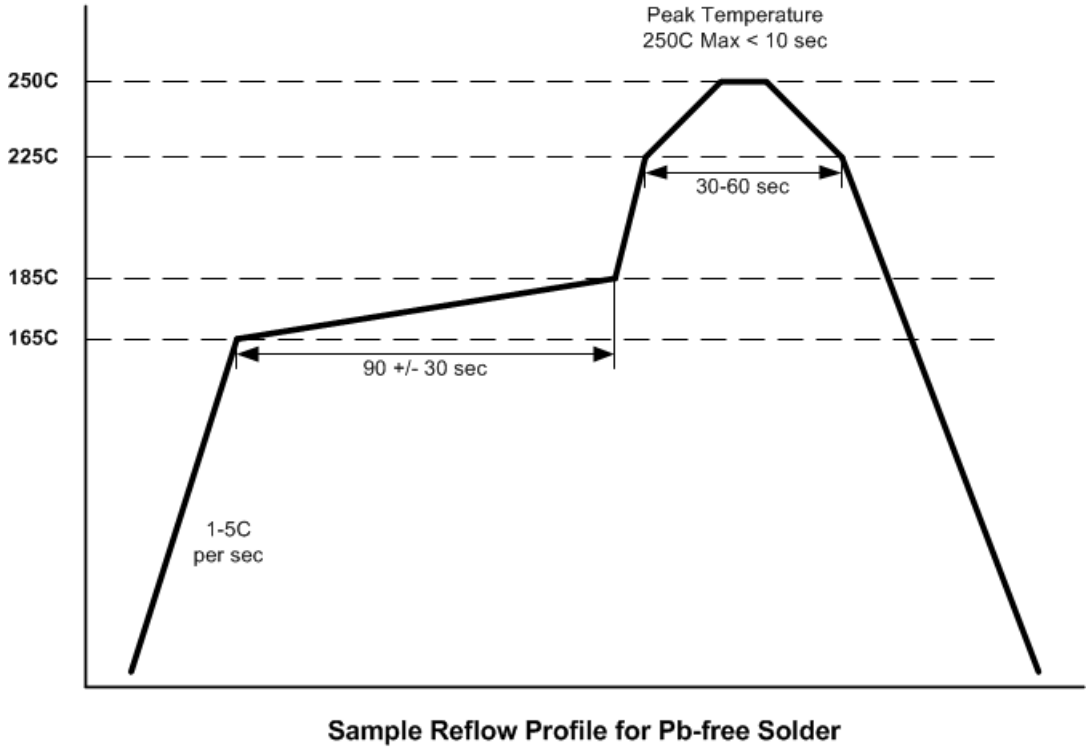

Figure 1. Sample Reflow Profile for Pb-Free Solder

7 Support Information

7.1 BGA PCB Feature Definitions (for the purposes of this page)

- Ball pads - Also known as BGA "lands". This is the copper that the BGA ball solders to.
- NSMD pad - Non-Solder Mask Defined ball pad. This kind of pad has an opening that is defined only by the size of the ball pad. The solder mask is applied around the ball pad and does not cover it. This kind of pad is more popular lately and has the advantage of increased ball adhesion because the ball flows around the sides of the ball pad and grips on the top and the sides. This kind of pad is usually recommended for BGA designs 0.5mm and above.
- SMD pad - Solder Mask Defined ball pad. This kind of pad has a large copper area, but the solder mask covers the edges, so the opening is known as solder mask defined. This kind of pad is sometimes best for very small pitch pads where ball shorting is an issue.
- Via diameter - the full width of the via annular ring
- Micro via - a via that is laser drilled.
- HDI - High Density Interconnect. This is the type of board that uses very small vias like micro vias. When a board uses micro vias it is called an HDI board.
- Blind via - a conductive plated via that begins on one surface but does not continue on through the entire board stack.
- Buried via - a conductive plated via that does not connect to either surface of the PCB. It is only between two inner layers of the PCB.
- Throughhole via - a conductive plated drilled hole (via) that starts on one surface of the board and continues through the internal layers to the opposite surface of the board.

7.2 Conversion Between mm and mils

- 0.075 mm = 3 mils (0.003”)
- 0.1 mm = 4 mils (0.004”)
- 0.125 mm = 5 mils (0.005”)
- 0.2 mm = 8 mils (0.008”)
- 0.4 mm = 16 mils (0.016”)
- 0.45 mm = 18 mils (0.018”)
- 0.5 mm = 20 mils (0.020”)

8 References

1. *TI Via Channel™ Array*
2. *AM572x General Purpose EVM Hardware*
3. *AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware User's Guide*
4. *Flip Chip Ball Grid Array Package Reference Guide* (SPRS915)
5. *AM437x Sitara™ Processors Data Manual*
6. *OMAP35x 0.65mm Pitch Layout Methods*
7. *General hardware design/BGA PCB design/BGA decoupling* wiki
8. *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*

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