Application Report
SPRACF8A–May 2018–Revised March 2019

AM571x/AM572x/AM574x PCB Escape Routing

ABSTRACT

This document provides a sample PCB escape routing for the AM571x, AM572x, and AM574x SoCs. This escape document is based on the AM572x IDK EVM and the pinmux defined for that design.

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Trademarks

1 Introduction

This document provides a sample PCB escape routing for the AM571x, AM572x, and AM574x SoCs. These components have consistent pin placement for the functions assigned to each pin. The AM572x and AM574x provide multiple functions on each pin, and it would be impossible to provide an escape for all permutations of the pinmux selection. This escape document is based on the AM572x IDK EVM and the pinmux defined for that design.

1.1 Stackup

The PCB layout designer must balance many different requirements when starting a PCB layout. The first is the board stackup. The AM571x/AM572x/AM574x family of devices have a 23-mm × 23-mm package, which has a 0.80-mm pitch ball array of 28×28. To minimize cost, this ball grid is nearly a solid array. Due to the number of rows of signal balls around the periphery, designs must have 4 routing layers, not including the top and bottom layers, which can also contain some signal routes. In addition, due to the number of power supply rails, the stackup requires two layers dedicated to power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. This design example routes out all the signal balls, and requires a 12-layer stackup similar to that listed in Table 1.

Table 1. Layer Stackup

PCB Layer	Layer Routing, Planes, or Pours
Layer 1	Component pads and signal routing
Layer 2	Ground
Layer 3	Signal routing(1)
Layer 4	Signal routing(1)
Layer 5	Ground
Layer 6	Power
Layer 7	Power
Layer 8	Ground
Layer 9	Signal routing(1)
Layer 10	Signal routing(1)
Layer 11	Ground
Layer 12	Component pads (including most decoupling) and signal routing

(1) Tracks are assumed to be perpendicular. Broadside coupling must be minimized to prevent crosstalk problems. Else, additional Ground planes must be inserted between the signal routing layers.

A 12-layer stack-up such as the one discussed above is needed for a relatively dense PCB layout. Alternately, the layer count can be reduced, assuming one or more of the following exist:

- The PCB is not crowded around the AM571x/AM572x/AM574x device. This allows for more routing away from the device on the top and bottom layers, which can reduce layer congestion.
- Many of the signal balls are unused. Many designs will not use all of the interfaces, resulting in unused signal balls. This also reduces routing congestion.
- The PCB layout team has time to carefully place the routes. This can be very time consuming.

It is not acceptable to violate routing rules simply to save money on reduced PCB layers or due to limited routing time. All requirements must still be met. Also, creative routing increases design validation time – both in simulation and bench testing. This can be minimized if the layout is similar to one of the TI EVM designs.

The AM572 IDK EVM is implemented in a 12-layer stack-up similar to the one described above. This design has nearly every signal ball routed to circuitry or a connector. This drives the requirement for the full number of layers. Additionally, this board is designed for optimum signal integrity on the high speed interfaces while limiting the board size. To accomplish this, the design team chose to implement a High Density Interconnect (HDI) board using micro vias on both the top 2 and bottom 2 layers. This provided optimum routing for the SERDES interfaces and the DDR3 routes on layers 3 and 10, as well as the bottom and top layers, because there is no via stub. It also allowed layers 4 and 9 to contain DDR3 routes with very little via stub. The HDI stack-up adds cost, but it results in excellent signal integrity and simplified routing.

1.2 Floorplan Component Placement

Optimum trace routing has routes as short as possible with a minimum of cross-over. This requires careful placement of the components around the AM571x/AM572x/AM574x device. Figure 1 shows the default arrangement of the signal balls, as well as the power and ground balls. Some of the interfaces can move to other locations due to pin multiplex choices, and there are other interfaces not listed that are exposed through pin multiplex choices. The PCB layout team must analyze the locations of the interfaces used and the associated components and connectors.

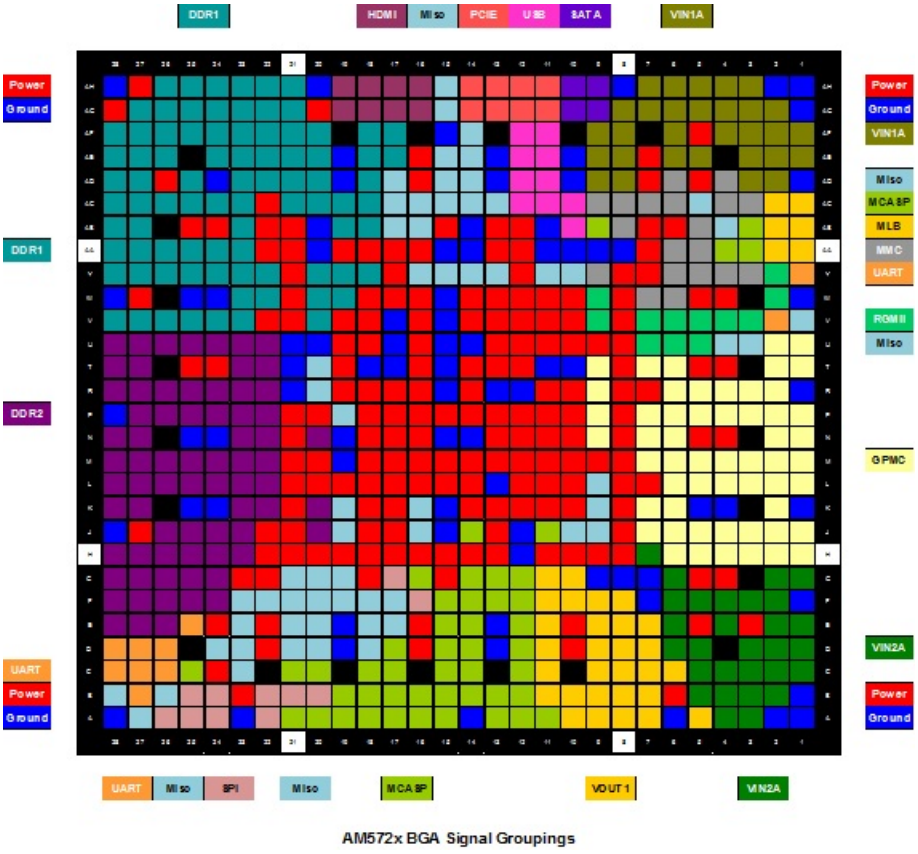

Figure 1. BGA Signal Grouping

1.3 Critical Interfaces Impact Placement

Placement of the AM571x, AM572x, or AM574x device and some of the components or connectors is also dictated by some of the highest performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

1.3.1 Critical Interfaces Routing

As indicated earleir, critical interfaces affect component placement options. When routing begins, these critical interfaces must be routed first. The design team must establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

Table 2 lists a recommended priority order for interfaces contained on the AM571x, AM572x, and AM574x family of devices. Individual design requirements may cause this list to change slightly, but this provides a good baseline.

Table 2. Routing Priority

Interface	Routing Priority
USB3	10 (Highest Priority)
SATA	9
PCIe	9
HDMI	8
DDR3	7
USB2	6
Power distribution	6
RGMII	6
QSPI	6
Parallel Video	5
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog audio	3
GPMC	2
GPIO	1
UART	1
I2C	1 (Lowest Priority)

The placement of most of these should be clear. The multi-gigabit SERDES interfaces are the most critical, due to their data rate and loss concerns. USB3 is at the top because it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the USB3 connector and the AM571x/AM572x/AM574x device. If the distance is too great, a USB3 repeater device may need to be added.

The asynchronous and low speed interfaces are at the bottom of the table. This leaves the synchronous and source-synchronous interfaces in the center, prioritized by their data rate. The one surprise may be power distribution, which is often left to last. This usually results in poor decoupling performance, current starvation, or excessive power supply noise due to insufficient copper required to carry the power and ground currents. PCB board space for the copper and decoupling must be allocated before routing the middle and low priority interfaces.

1.3.2 SERDES Interface Routing

The SERDES interfaces must always be routed first. SERDES routing should follow the guidelines provided in the appropriate data manual and in the *High-Speed Interface Layout Guidelines* (SPRAAR7) application note.

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. Most of the SERDES interfaces (SATA, PCIe Lane 0, and HDMI) are all located on the outer rows to allow these to route away from the device without requiring vias. Figure 2 shows the routing of the PCIe Lane 0 and HDMI signals on the AM572 IDK on the top layer.

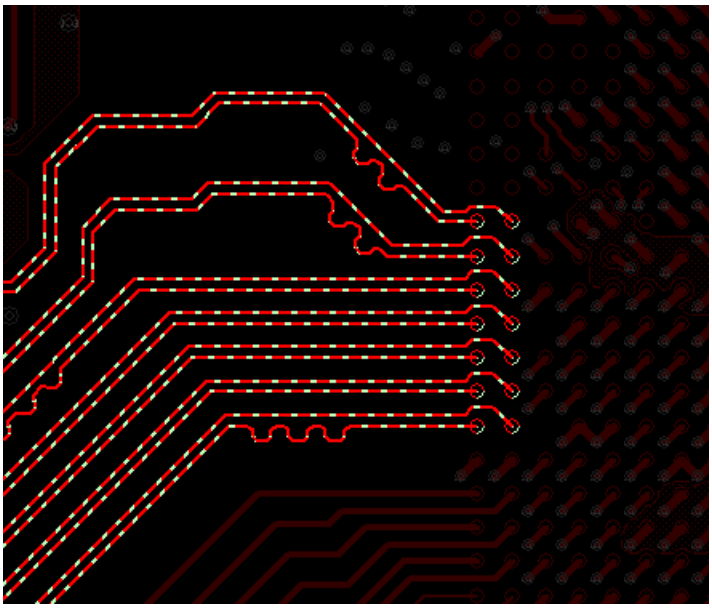

Figure 2. SERDES Top Layer Signal Escape

The multiplexed pins for PCIe Lane 1 and USB3 are not on the outer two rows requiring vias. Figure 3 shows the routing of these as USB3 on the AM572 IDK on the third layer. The AM572 IDK design is an HDI stack-up using micro vias, which allows the USB3 traces to be routed on layer 3 without any via stubs. Figure 3 also shows the USB2 traces for both port 0 and port 1. If HDI is not used, via stubs should be avoided. Using a through board via allows the routing of these signals to be transferred to the bottom of the board.

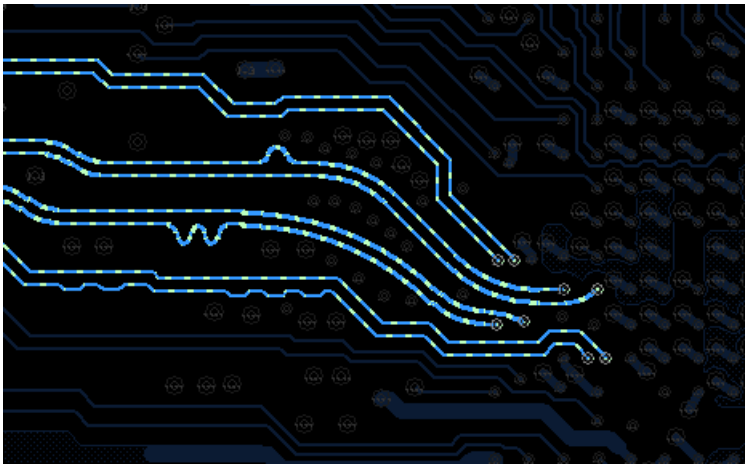

Figure 3. SERDES Layer 3 Signal Escape

1.4 DDR3 Signal Routing

The DDR3 signals must be routed next. Refer to the *AM572x Data Manual* (SPRS915) and the *AM574x Data Manual* (SPRS982) for detailed recommendations for DDR3 routing. The figures below show the BGA breakout for the first DDR3 port, but the same technique must be used for the second DDR3 port.

The DDR3 SDRAM memory devices should be arranged so that the data group balls are closest to the AM572x device. This lets the data group nets have the shortest possible routing. The Address, Command, and Control signals operate at half the bandwidth of the data, so they are expected to be longer.

1.4.1 Data Group Routes

Figure 4, Figure 5, and Figure 6 show the data group routing for the first DDR3 port. The PCB layout designer grouped all 11 nets for each byte group on a single layer. This is not a requirement, but it is strongly recommended as this simplifies the signal length and delay matching requirements.

Figure 4 shows Data Group 1 and Data Group 3. These signals break out on the top layer and are then routed on layer 3. Due to the use of micro vias, there is no via stub on these routes.

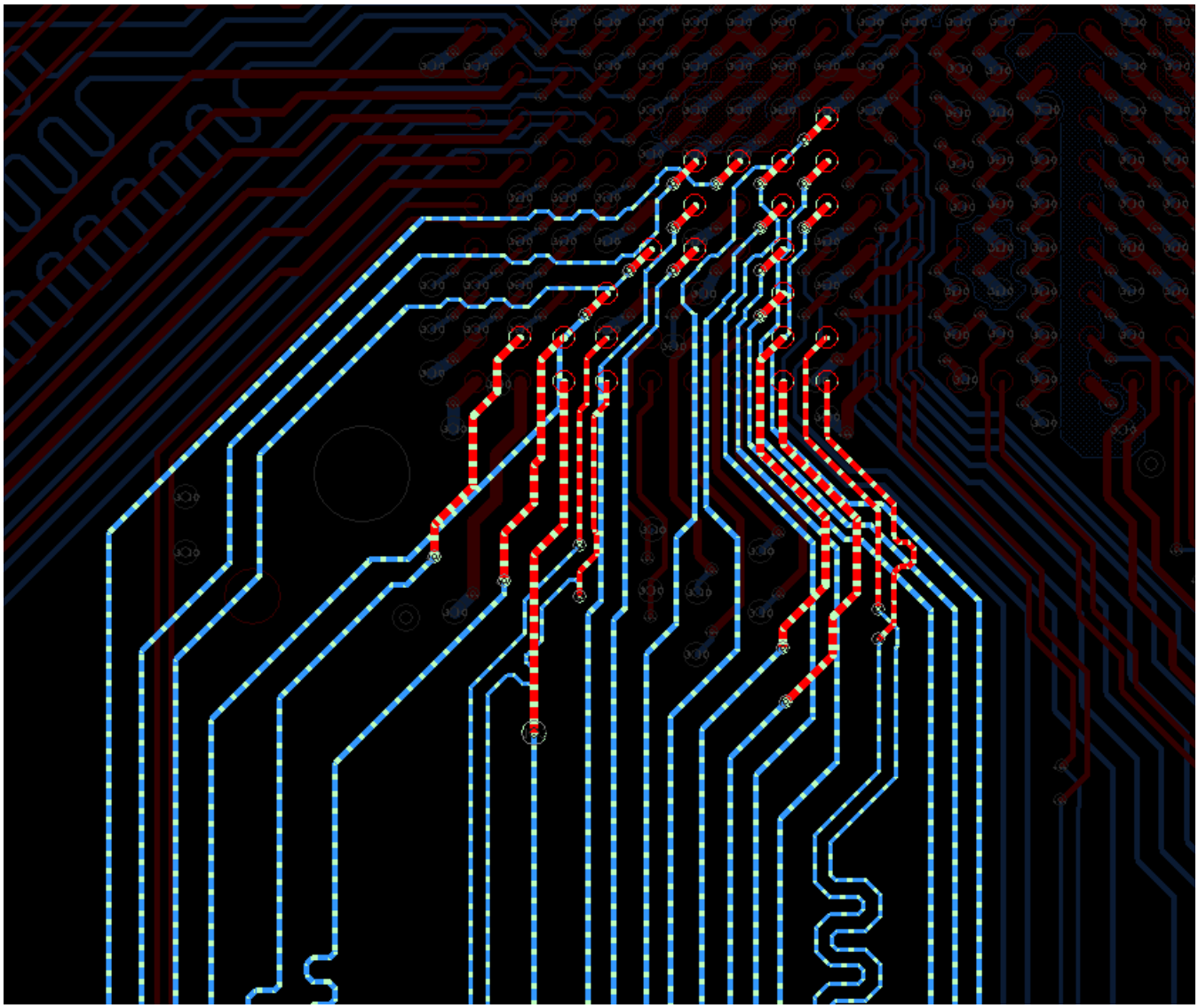

Figure 4. DDR3 Data Group 1 and 3 Routing

Figure 5 shows Data Group 0 and Data Group 2. These signals break out on the top layer and are then routed on layer 10. Due to the use of micro vias, there is no via stub on these routes.

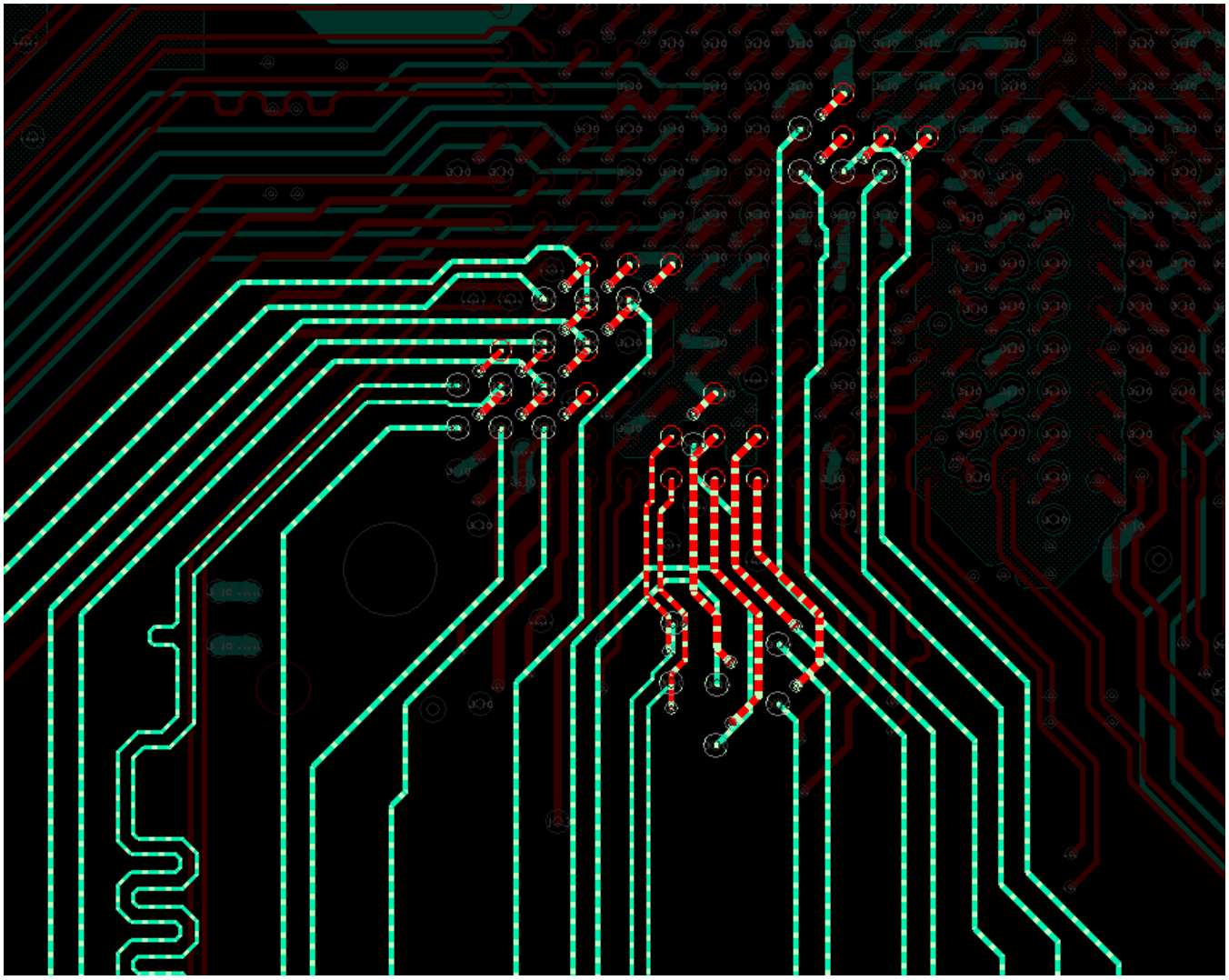

Figure 5. DDR3 Data Group 0 and 2 Routing

Figure 6 shows the ECC Data Group. These signals break out on the top layer and are then routed on layer 3. Due to the use of micro vias, there is no via stub on these routes.

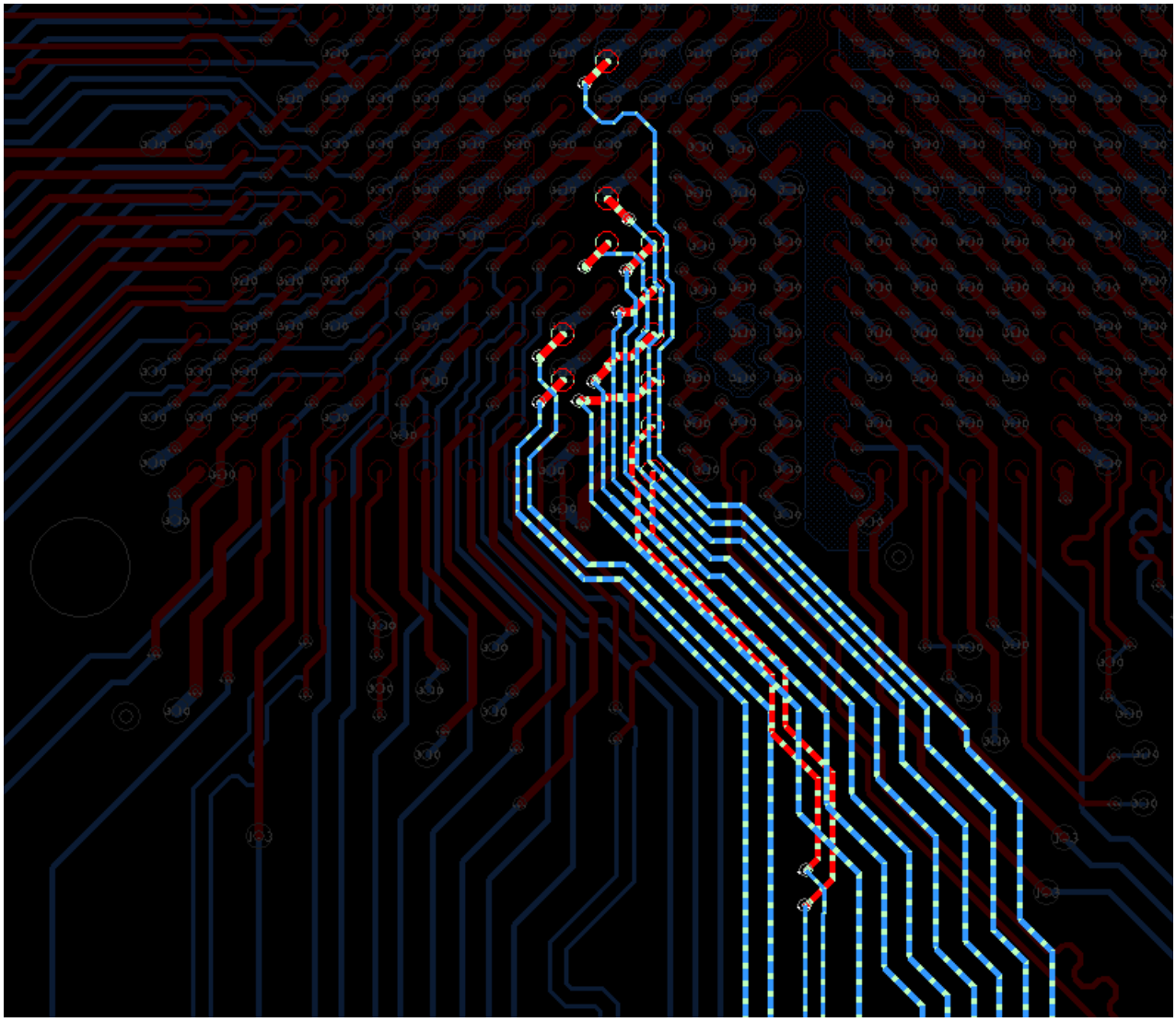

Figure 6. DDR3 ECC Data Group Routing

1.4.2 Address, Command, Control ,and Clock Group Routes

The next four figures show the Address, Command, Control, and Clock (ACCC) group routing for the first DDR3 port. Figure 7 is an overlay showing these routes on layers 1, 3, and 10. The following images show each layer separately.

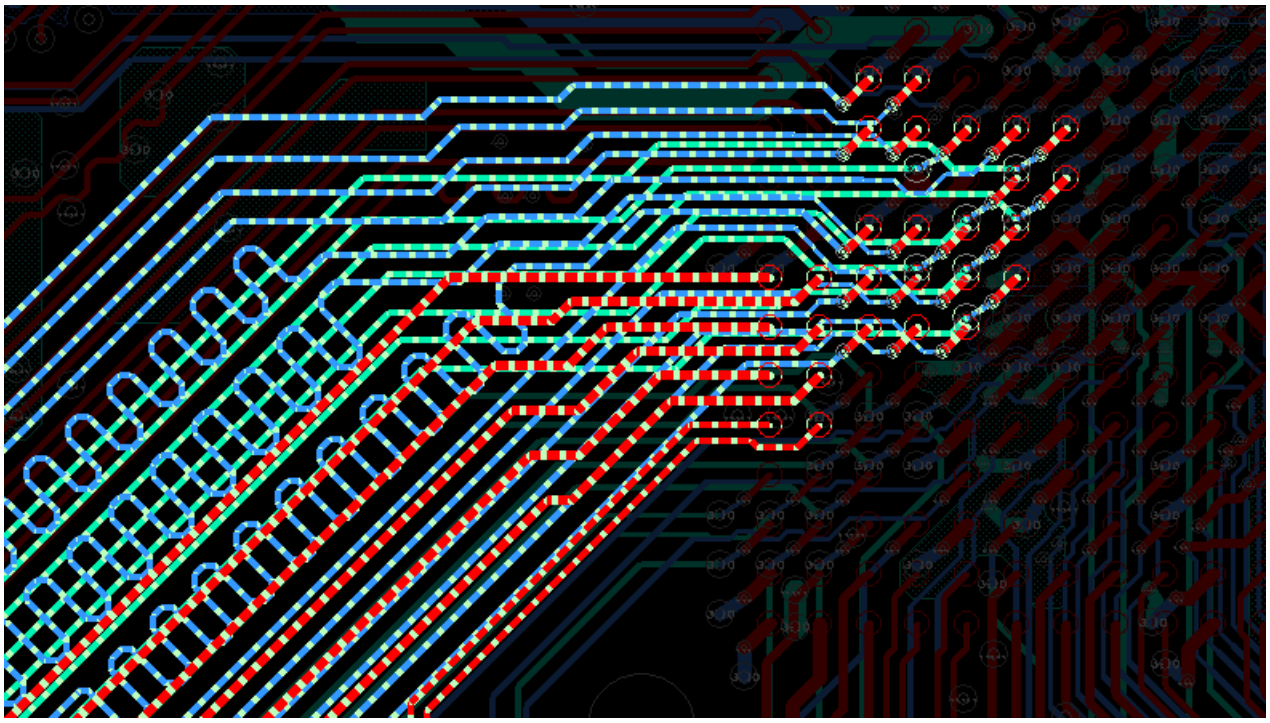

Figure 7. Overlay of Address, Command, Control, and Clock Group Routing

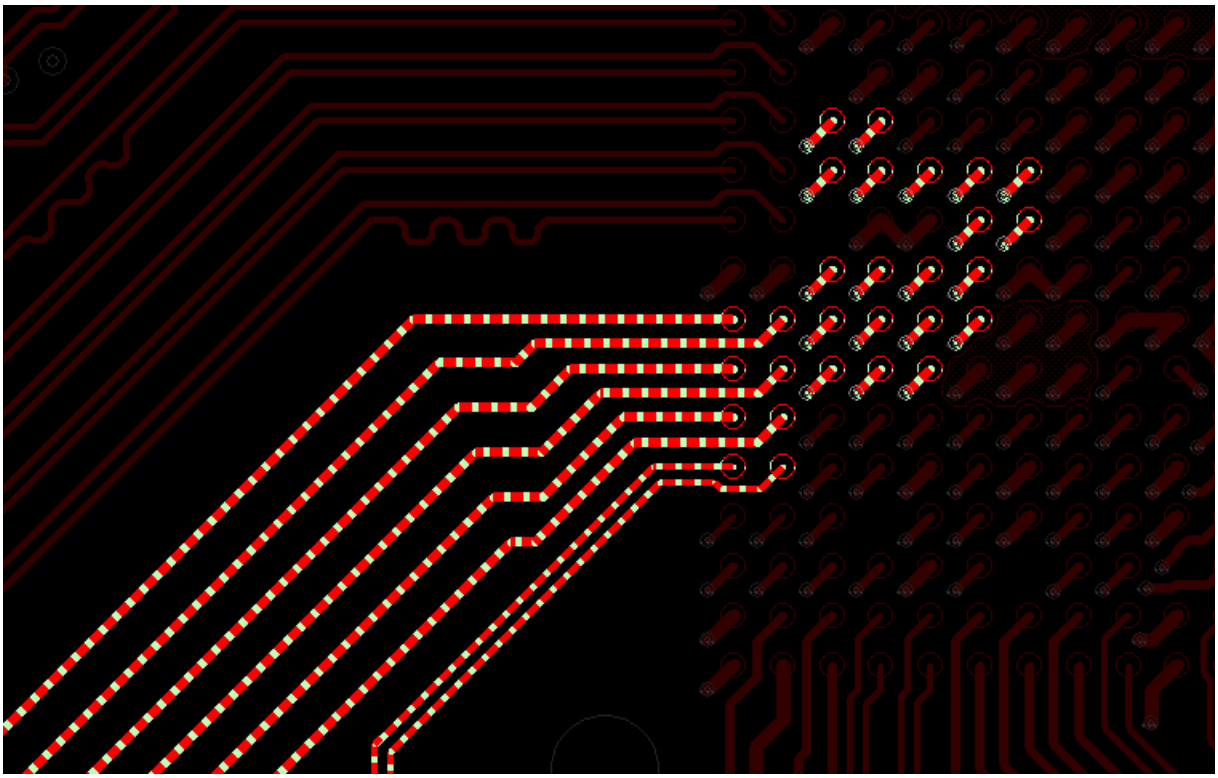

Figure 8. Top Layer Routing of Address, Command, Control, and Clock Group

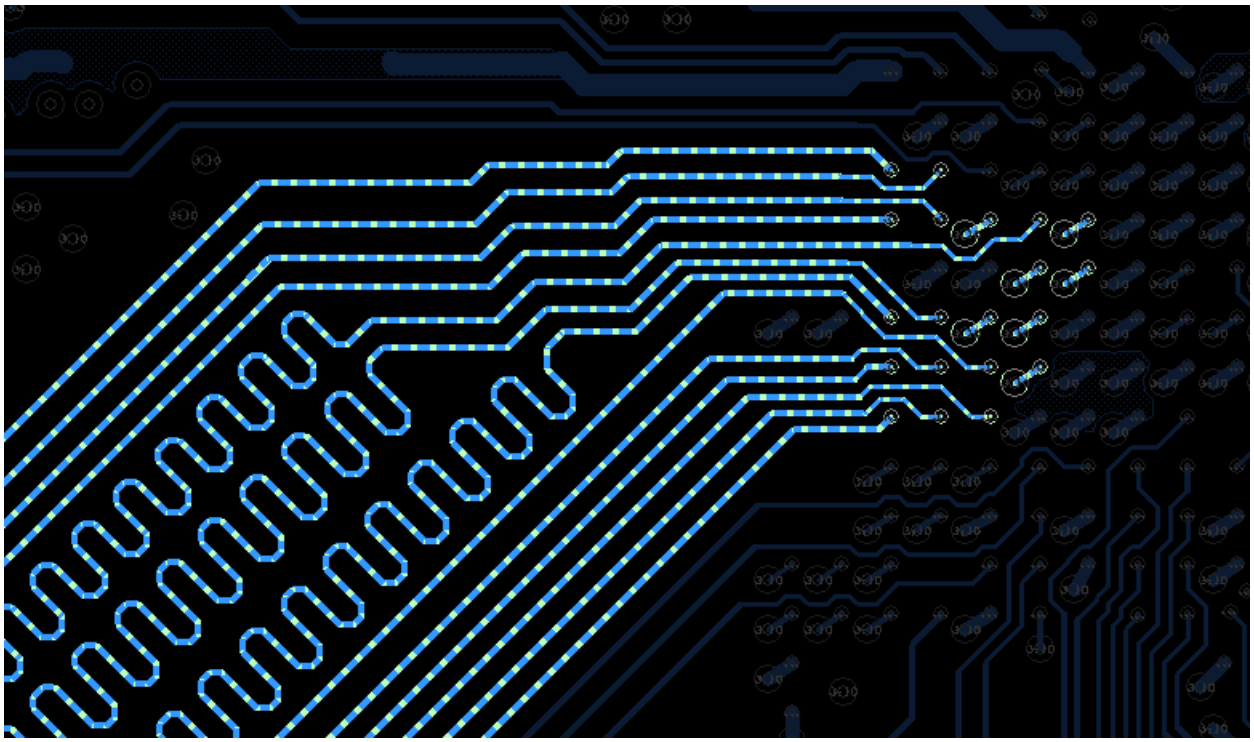

Figure 9. Layer 3 Routing of Address, Command, Control, and Clock Group

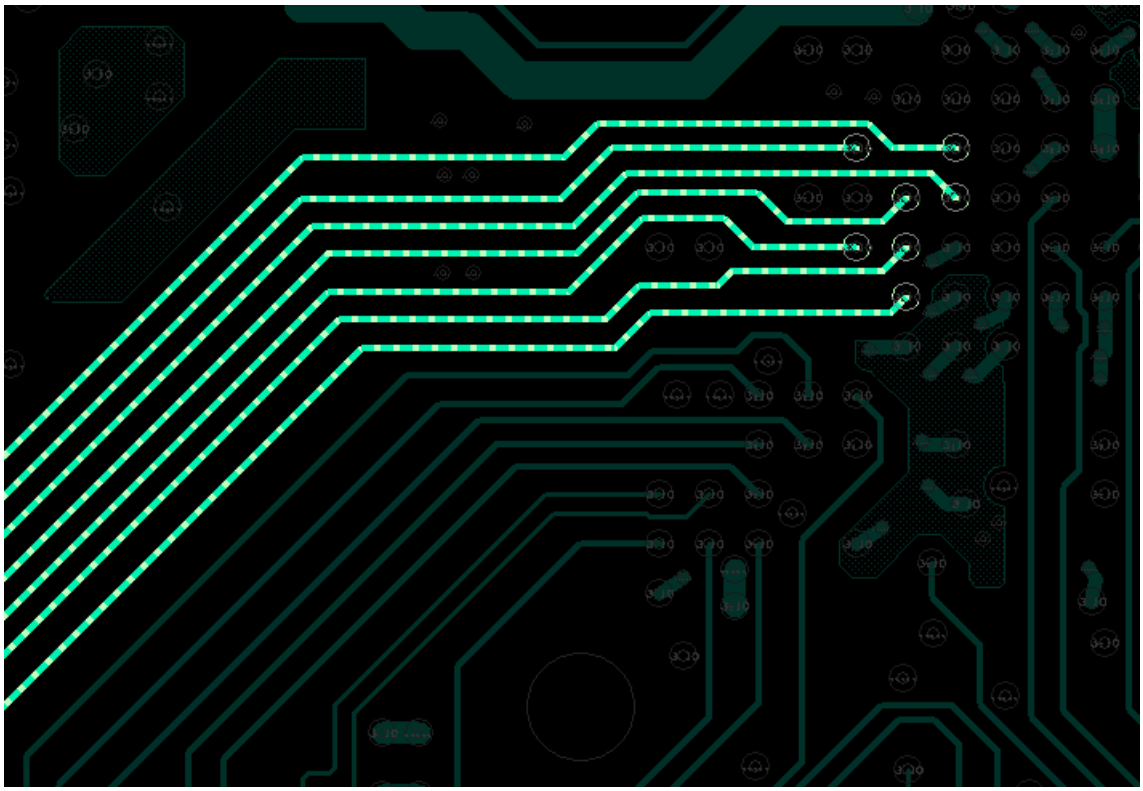

Figure 10. Layer 10 Routing of Address, Command, Control, and Clock Group

1.5 Power Planes and Decoupling Routing

The middle priority interfaces and the power distribution planes and pours should be routed following the SERDES and DDR3 interfaces. TI strongly recommends completing all SERDES and DDR3 routing before continuing with other interfaces. The power distribution planes, pours, and all of the decoupling should be placed before PCB simulations are executed for the SERDES and DDR3 routes. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation. If so, these must be completed at this time.

1.6 Lowest Priority Interface Routing

When both the length matching and simulations of the highest priority interfaces, as well as the Power Distribution Network (PDN) analysis, have been completed, the layout can continue with the medium priority interfaces followed by the lower priority interfaces.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2018) to A Revision	Page
• Added AM571x information throughout document.	1

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