Application Note

Powering the AM62x with the TPS65219 PMIC

ABSTRACT

This application note can be used as a guide for integrating the TPS65219 Power Management IC (PMIC) into non-automotive systems powering the Industrial AM62x Sitara Processor. An orderable part number comparison table details the configurations of several factory programmed TPS65219 variants that can support different AM62x use cases. Example power maps are provided to assist the design process.

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1 Introduction

The TPS65219 PMIC is a cost and space optimized solution specially designed to power the AM62x processor and its principal peripherals. TPS65219 has flexible mapping and comes in several factory programmed variants to support different AM62x use cases. A hardware solution is readily available with the AM62x SK EVM. The AM62x is the latest in the Sitara™ family of Arm® processors, built with features to support embedded 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options. To be used in applications from Human Machine Interfaces (HMI) to 3D Point Cloud, this processor provides powerful computing while supporting power management features designed for portable or power-sensitive systems. Powering a processor such as the AM62x family demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing.

The AM62x processor requires at minimum, power for seven main rails. These include the core supply rails (VDD_CORE and VDDR_CORE), DDR IO supply (VDDS_DDR), and 1.8 V and 3.3 V digital and analog IO rails (VDDSHVx, VDDSHV_MCU, VDDSHVy, VDDA_MCU). This application note discusses the TPS65219 power management IC (PMIC) and its full feature-set, specifically designed to power the AM62 Sitara™ processor and its principal peripherals.

2 TPS65219 Overview

The TPS65219 PMIC contains seven regulators, 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) are configurable for load switch and bypass mode to support dynamic SD card voltages, while LDO3 and LDO4 (2×300 mA) are configurable as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. For systems that may require an extended temperature range, the TPS65219 is characterized for either -40°C to +105°C ambient temperature. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65219 PMIC provides the full power package to supply the AM62x SoC, as well as many other SoCs.

Table 2-1. TPS65219 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5 V - 5.5 V	0.6 V - 3.4 V	3.5 A	• 2.3 MHz quasi-fixed frequency. • Low IQ/auto-PFM and Forced PWM modes supported. • Dynamic voltage scaling • Programmable power sequencing and default voltages • Integrated voltage supervisor for undervoltage
BUCK2	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
BUCK3	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
LDO1	1.5 V - 5.5 V	0.6 V - 3.4 V	400 mA	• Configurable as load switch and bypass-mode supporting SD-Card • Integrated voltage supervisor for undervoltage
LDO2	1.5 V - 5.5 V	0.6 V - 3.4 V	400 mA	
LDO3	2.5 V - 5.5 V	1.2 V - 3.3 V	300 mA	• Configurable as load switch • Integrated voltage supervisor for undervoltage
LDO4	2.5 V - 5.5 V	1.2 V - 3.3 V	300 mA	

2.1 TPS65219 Functional Block Diagram

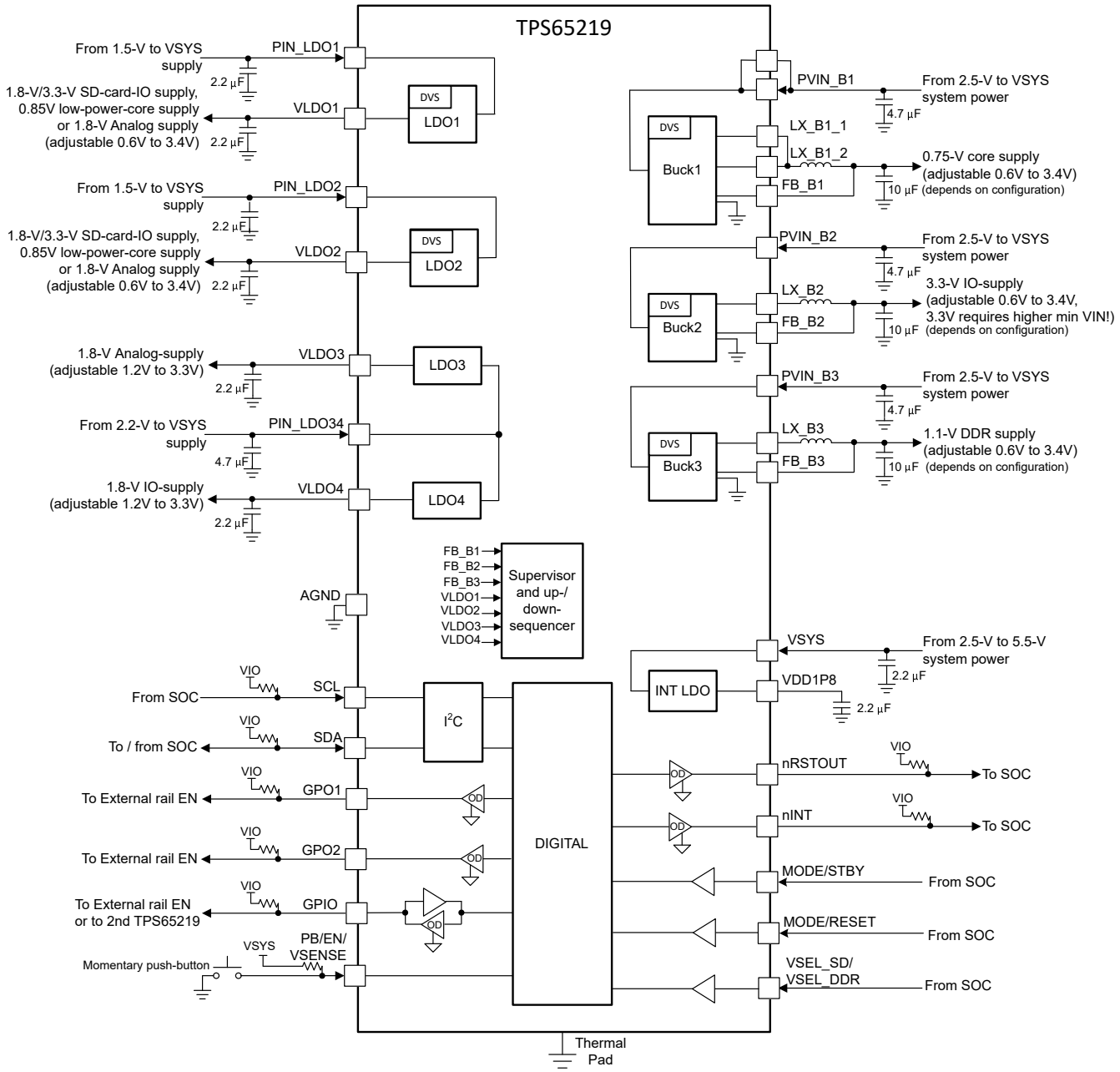


Figure 2-1. TPS65219 Functional Block Diagram

3 TPS65219 Variants

There are four different orderable part number (OPN) variants of the TPS65219 PMIC that come factory programmed to power the AM62x processor. Selecting the right OPN will be based on the application use case and design requirements. Table 3-1 compares the NVM configurations from the output voltages on each rail to the configuration of the digital pins as well as the package options. This table also includes the reference hardware that is available to support new designs. For additional detailed information, please refer to the device data sheet and technical reference manual (TRM) available at Ti.com.

Table 3-1. TPS65219 Comparison Table

		TPS6521901 Section 4.1	**TPS6521902** Section 4.2	**TPS6521903** Section 4.3	**TPS6521904** Section 4.4
Use Case	Vsys	5 V	3.3 V	3.3 V	3.3 V
	External Memory Support	DDR4	LPDDR4	DDR4	DDR4
BUCK1	Vout	0.75 V	0.75 V	0.75 V	0.85 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
BUCK2	Vout	3.3 V	1.8 V	1.8 V	1.8 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
BUCK3	Vout	1.2 V	1.1 V	1.2 V	1.2 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
LDO1	Vout	3.3 V (Bypass)	3.3 V (Bypass)	3.3 V (Bypass)	3.3 V (Bypass)
LDO2	Vout	0.85 V	0.85 V	0.85 V	1.8 V (Bypass)
LDO3	Vout	1.8 V	1.8 V	1.8 V	1.8 V
LDO4	Vout	2.5 V	2.5 V	2.5 V	2.5 V
GPIO	GPO1	Enabled	Disabled	Disabled	Disabled
	GPO2	Disabled	Enabled	Enabled	Enabled
	GPIO	Disabled	Disabled	Disabled	Disabled
	Multi-Device	Disabled	Disabled	Disabled	Disabled
MODE_RESET	Config	RESET	RESET	RESET	RESET
MODE_STANDBY	Config	Mode and Standby	Mode and Standby	Mode and Standby	Mode and Standby
VSEL_SD_DDR	Config	SD	SD	SD	SD
	Polarity	High = VOUT Low = 1.8 V	High = VOUT Low = 1.8 V	High = VOUT Low = 1.8 V	High = VOUT Low = 1.8 V
	Rail	LDO1	LDO1	LDO1	LDO1
EN_PB_VSENSE	Config	Enable	Push-button	Push-button	Push-button
First Supply detection [1]	FSD config	Enabled	Enabled	Enabled	Enabled
Orderable Part Number	Package size 5 x 5 mm	TPS6521901RHBR	TPS6521902RHBR	TPS6521903RHBR	TPS6521904RHBR
	Package size 4 x 4 mm	TPS6521901RSMR	TPS6521902RSMR	TPS6521903RSMR	TPS6521904RSMR
Design Resources	Reference Hardware	TPS65219EVM (PMIC only. Does not include processor)	SK-AM62-P1 AM62x EVM LPDDR4 variation	SK-AM62-P1 AM62x EVM	SK-AM62-P1 AM62x EVM VDD_CORE variation
	Reference Hardware Availability	Boards and design files available now on Ti.com.	Design files can be re-used from the SK-AM62-P1 EVM Design Files. Changes must be implemented to support LPDDR4 memory.	SK-AM62-P1 EVM Design Files available now. Boards will be available on Ti.com starting September 2022.	Design files can be re-used from the SK-AM62-P1 EVM Design Files. Changes must be implemented to support VDD_CORE and VDDR_CORE with 0.85V from Buck1.

[1] First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.

4 Power Block Diagrams

There are several considerations to take into account when designing the TPS65219 to power the AM62 processor and its peripherals. Will the application be using LPDDR4 or DDR4 memory? Does an SD card need to be supported? What will the system supply voltage be? Are there any external discrete ICs that will require fully controlled sequencing? Does system application prioritize highest integration or lowest power consumption? Each of these questions impact the design, configuration, setup, among others, of the power block diagram and plays a role designing the most robust power solution. Figure 4-1 outlines some of the common design considerations that may come up when pairing the TPS65219 PMIC to the AM62 SoC rails.

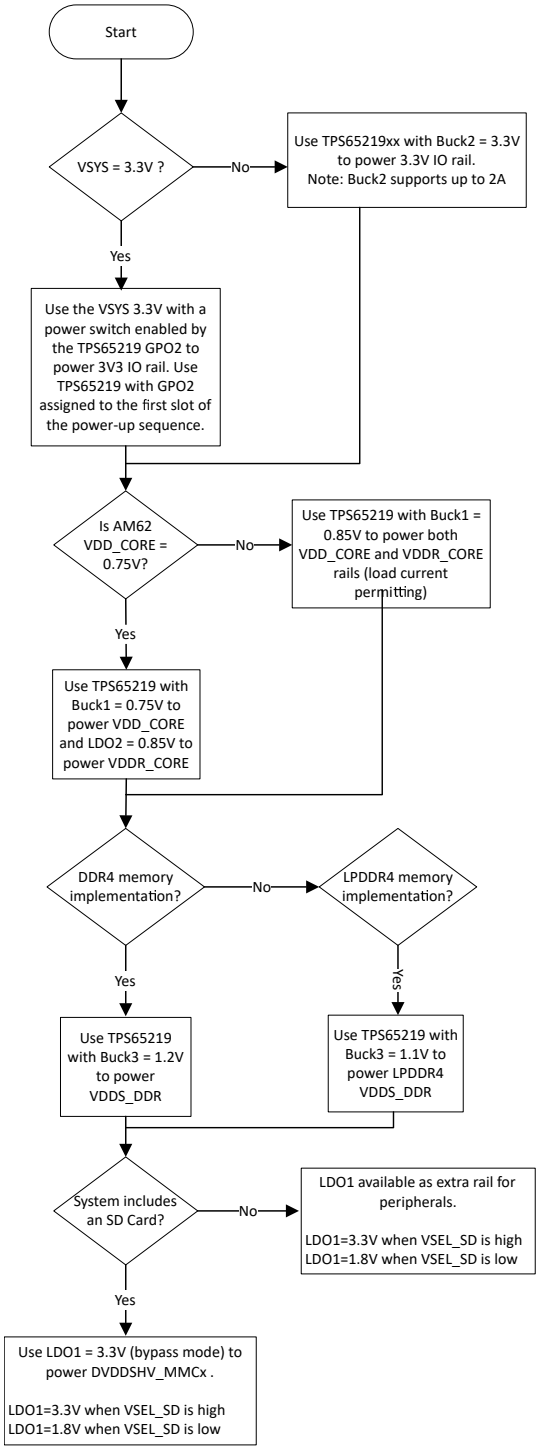


Figure 4-1. TPS65219 Power Map Decision Tree

4.1 TPS6521901 Powering AM62x

Use case: VSYS=5V, DDR4 Memory

Figure 4-2 shows the TPS6521901 variant powering the AM62x processor on a system with 5 V input supply and DDR4 memory. The 5 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx). Buck1, Buck2 and Buck3 are used to supply VDD_CORE at 0.75 V, 3.3 V VDDSHVx IO and DDR IO respectively. Since Buck2 (3.3 V PMIC rail) is programmed to ramp up first in the power-up sequence, it can be used as the input supply for some of the LDOs to minimize power dissipation. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is used to supply the VDDR_CORE. LDO3 supports the 1.8 V analog domain and LDO4 supports the 2.5 V VPP for the DDR4 memory. This power solution requires an external discrete buck regulator to supply the 1.8 V VDDSHV IO domain. This external discrete can be enabled using the GPO1 of the PMIC. TPS6521901 comes pre-programmed to enable GPO1 in the second slot of the power-up sequence with a duration of 10 ms. The external discrete must ramp up and reach a stable output voltage within the 10 ms duration of the second slot (before the PMIC starts the 3rd slot of the power-up sequence). The remaining two general purpose pins (GPIO and GPO2) are free digital resources that are disabled by default but can be enabled through I2C after the PMIC completes the power-up sequence. Figure 4-3 and Figure 4-4 shows the power-up and power-down sequence programmed on TPS6521901.

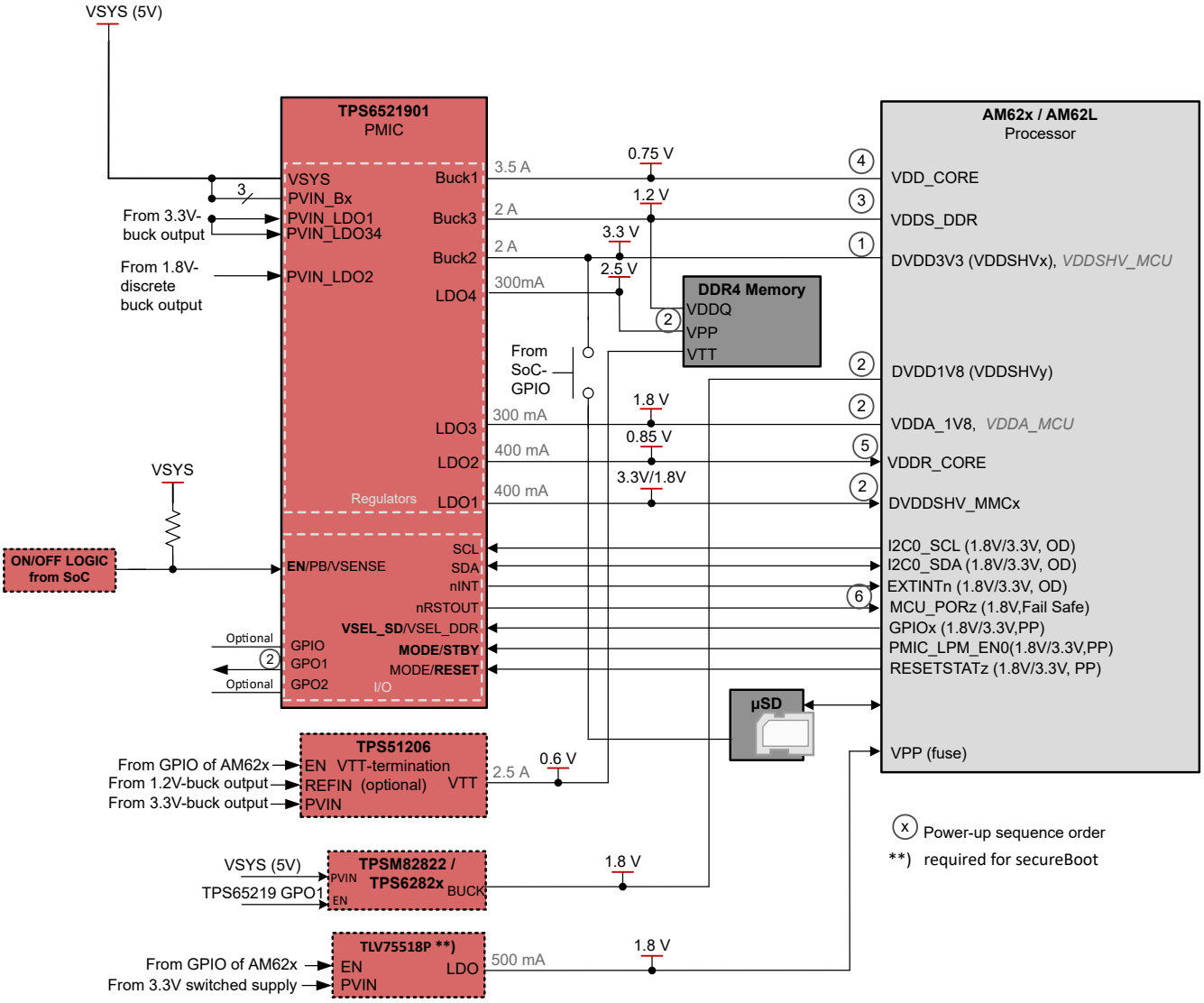


Figure 4-2. TPS6521901 Powering AM62

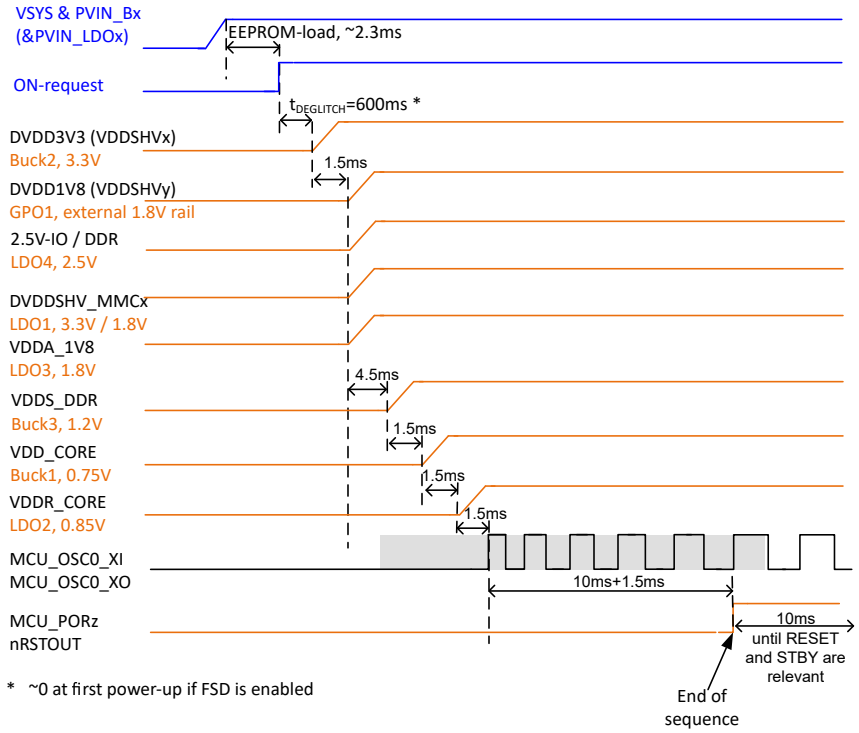
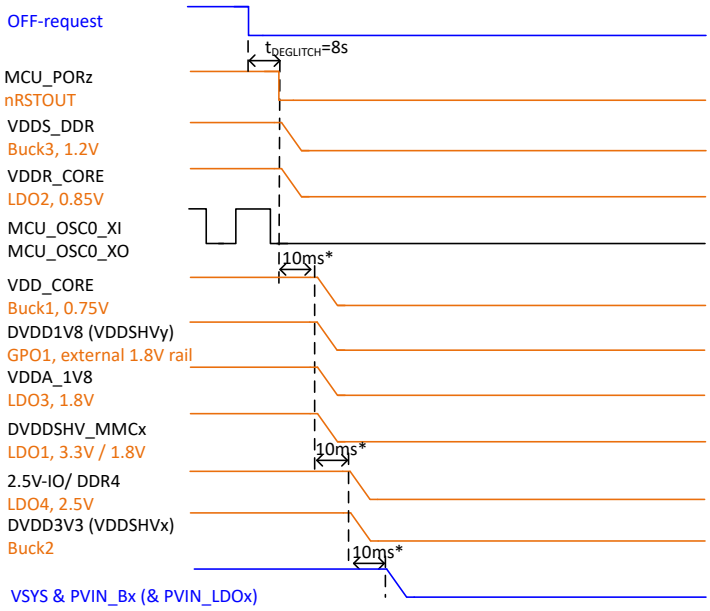


Figure 4-3. TPS6521901 Power-Up Sequence



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 4-4. TPS6521901 Power-Down Sequence

4.2 TPS6521902 Powering AM62x

Use case: VSYS=3.3V, LDDR4 Memory

Figure 4-5 shows the TPS6521902 variant powering the AM62x processor on a system with 3.3 V input supply and LDDR4 memory. Buck1, LDO3, LDO2, and LDO1 are used to supply the same AM62x domains that were described in the previous block diagram. The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 DVDDSH IO domain. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence. Buck3 and Buck2 supports the 1.1 V and 1.8 V required by VDDS_DDR and the 1.8 V DVDD3V3 IO domain. They are also used to support the required voltages on the LPDDR4 memory. LDO4 is a free 2.5 V power resource that can be used for external peripherals like the Ethernet PHY. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed. Figure 4-6 and Figure 4-7 shows the power-up and power-down sequence programmed on TPS6521902.

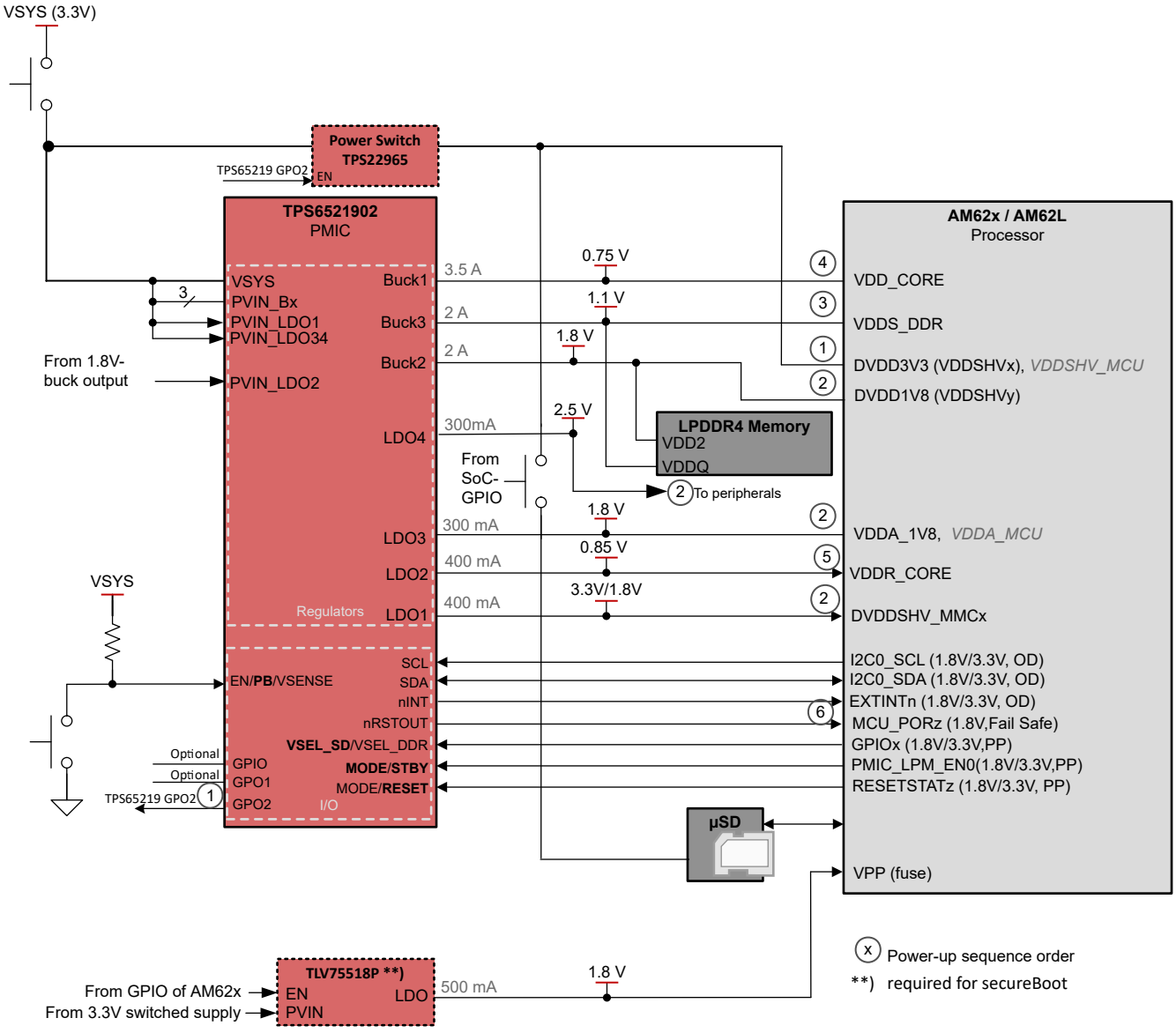


Figure 4-5. TPS6521902 Powering AM62

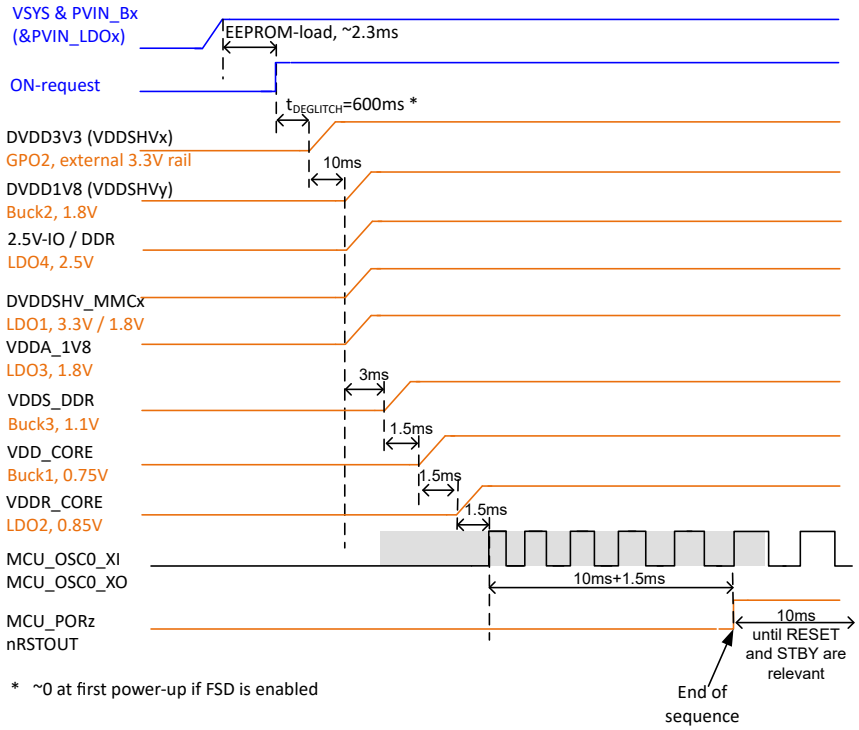
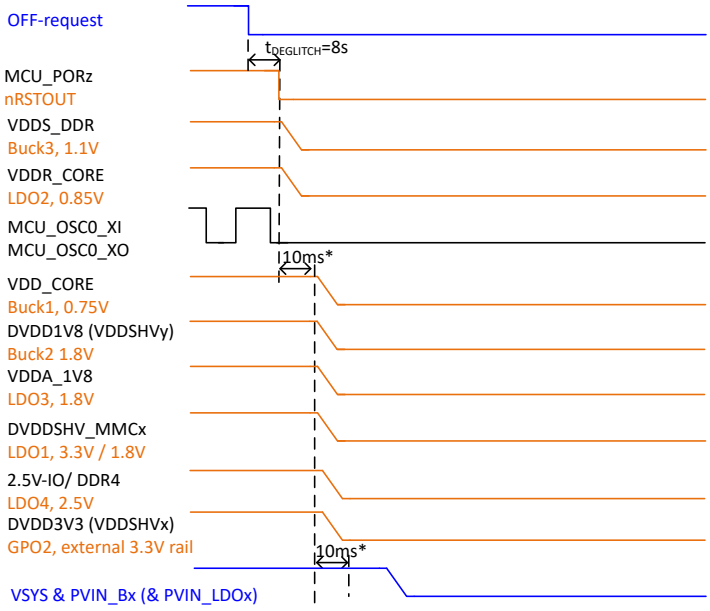


Figure 4-6. TPS6521902 Power-Up Sequence



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 4-7. TPS6521902 Power-Down Sequence

4.3 TPS6521903 Powering AM62x

Use case: VSYS=3.3V, DDR4 Memory

Figure 4-8 shows the TPS6521903 variant powering the AM62x processor on a system with 3.3 V input supply and DDR4 memory. Buck1, Buck2, LDO3, LDO2, LDO1, and GPO2 are used to power/enable the same domains that were described in the previous power block diagrams. The 3.3 V, coming from the pre-regulator, can be combined with a power switch to supply the 3.3 DVDDSH IO domain. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence. Buck3 is used to supply the VDDS_DDR and together with the 1.8 V on Buck2 they support the voltages needed for the DDR4 memory. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed. This variant is used on the SK-AM62-P1 EVM and design files are available to be leveraged for new designs. Figure 4-9 and Figure 4-10 shows the power-up and power-down sequence programmed on TPS6521903.

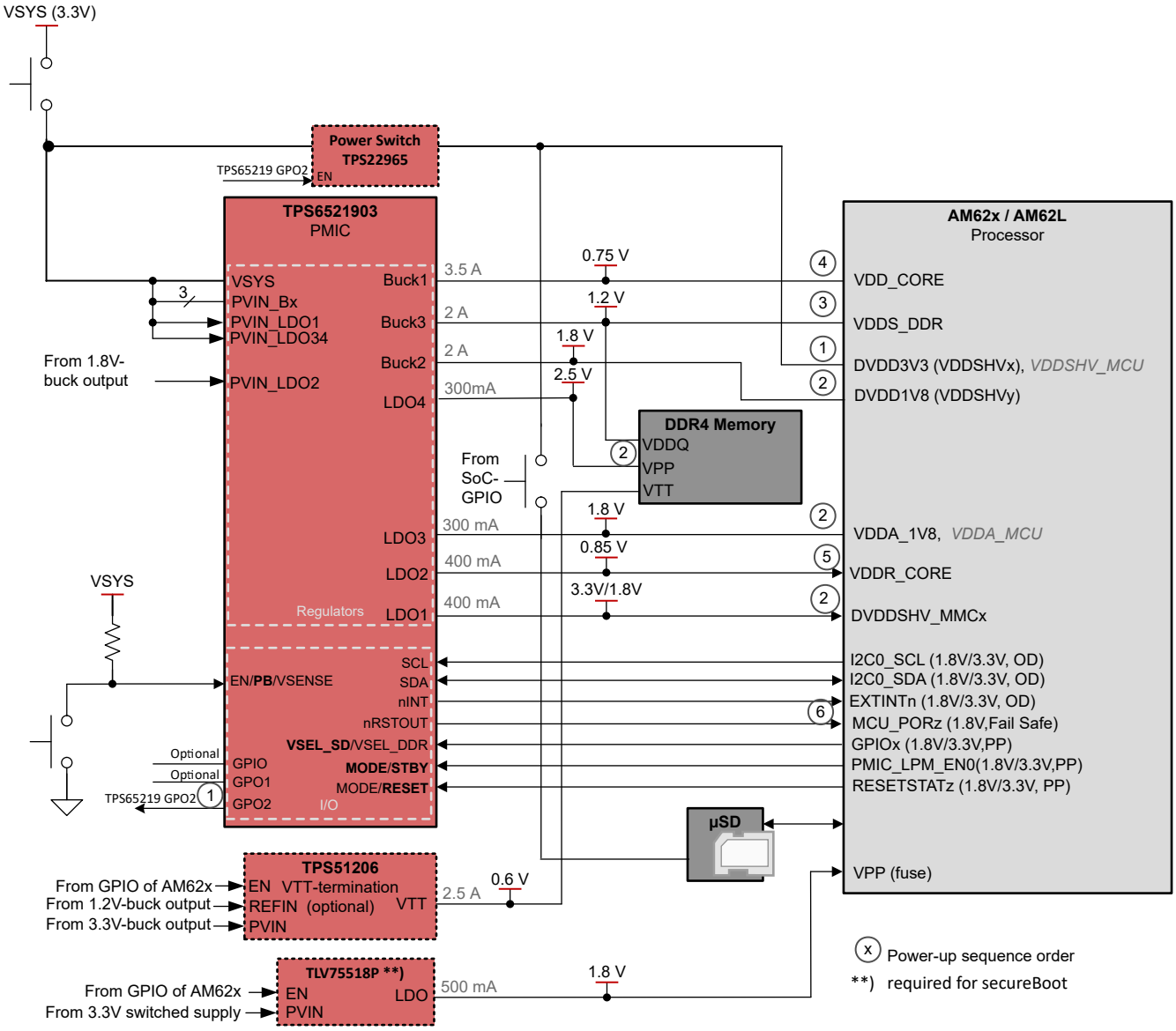


Figure 4-8. TPS6521903 Powering AM62x

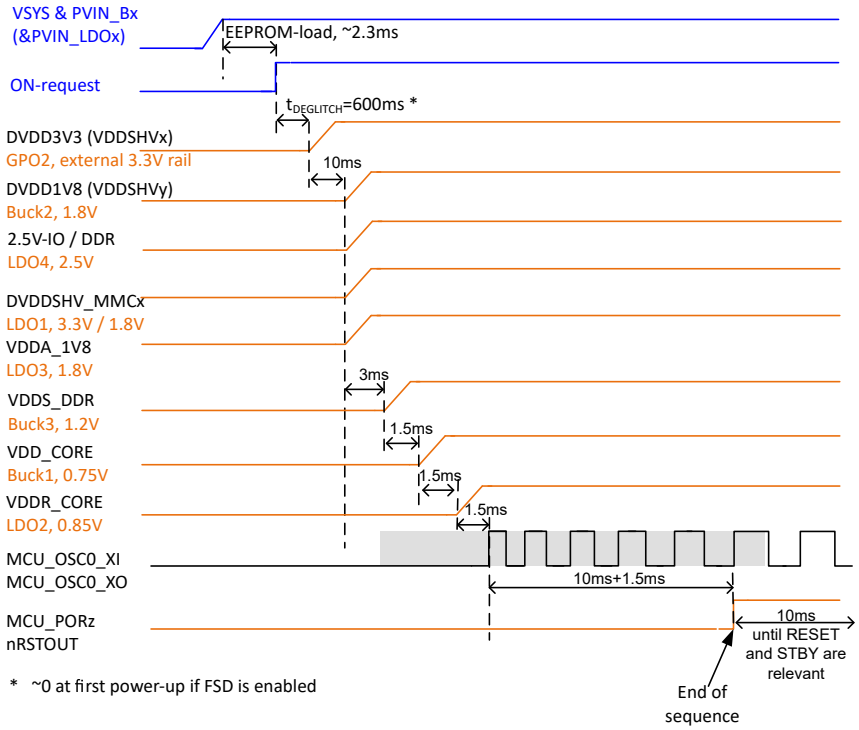
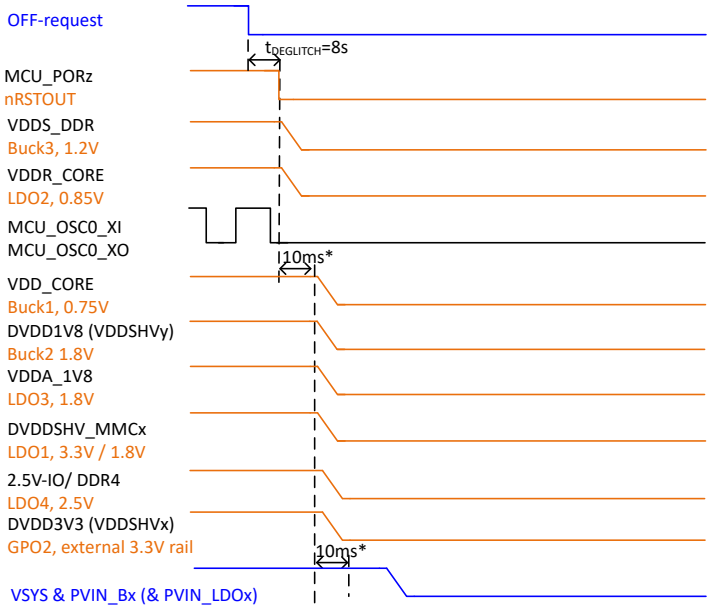


Figure 4-9. TPS6521903 Power-Up Sequence



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 4-10. TPS6521903 Power-Down Sequence

4.4 TPS6521904 Powering AM62x

Use case: VSYS=3.3V, DDR4 Memory, VDD_CORE=0.85V

Figure 4-11 shows the TPS6521904 variant powering the AM62x processor on a system with 3.3 V input supply and DDR4. This configuration is similar to the TPS6521903 but in this scenario, VDD_CORE is operated at 0.85 V instead of 0.75 V. As stated on the AM62x data sheet, "VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85 V". This requirement on the processor allows to have both, VDD_CORE and VDDR_CORE supplied by the same PMIC rail (Buck1). LDO2 is a free power resource pre-programmed for 1.8V output which can be used to supply external peripherals. Similarly to the TPS6521903, this configuration also has GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. The configuration can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence). Figure 4-12 and Figure 4-13 shows the power-up and power-down sequence programmed on TPS6521904.

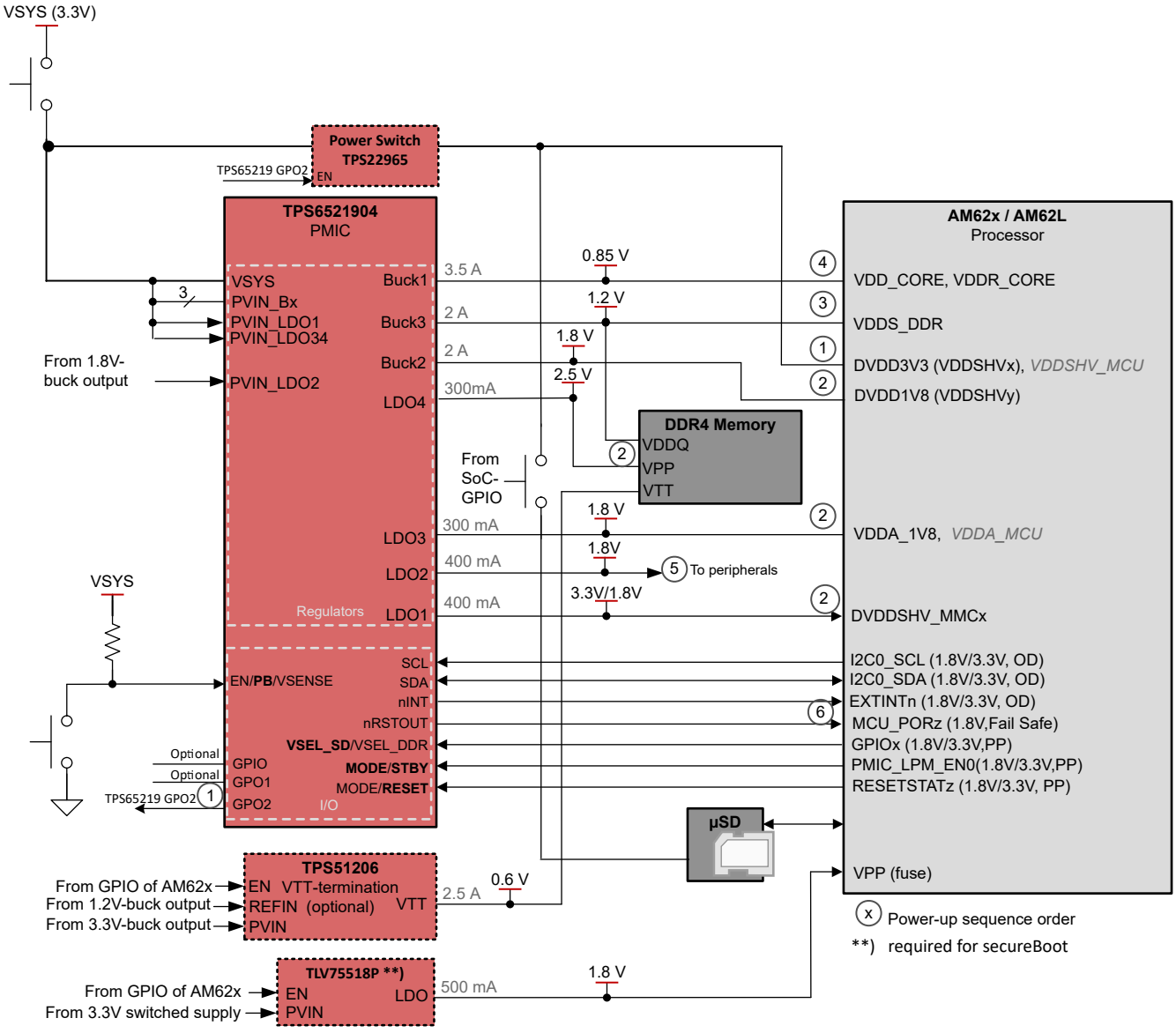


Figure 4-11. TPS6521904 Powering AM62x

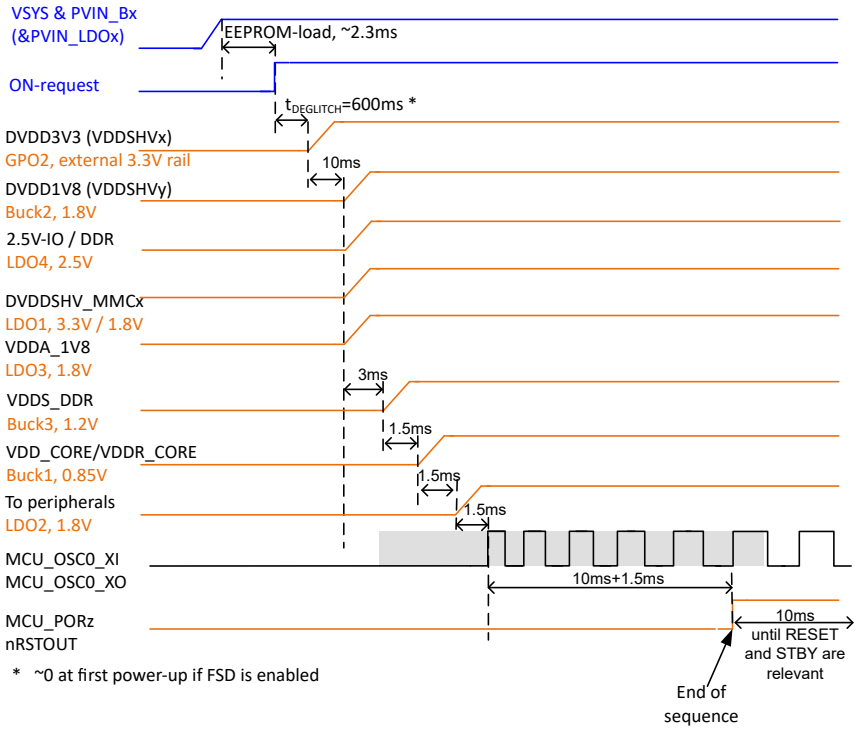
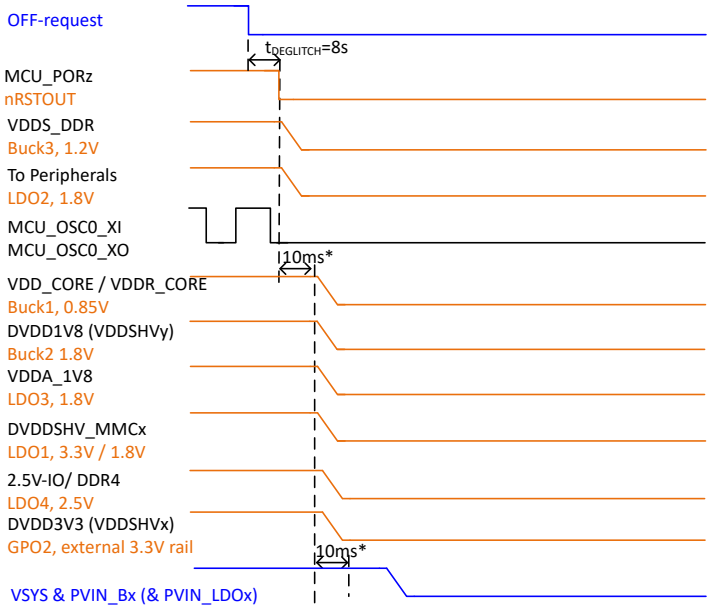


Figure 4-12. TPS6521904 Power-Up Sequence



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 4-13. TPS6521904 Power-Down Sequence

5 References

1. Texas Instruments, TPS65219 Integrated Power Management IC for ARM Cortex—A53 Processors and FPGAs data sheet.
2. Texas Instruments, AM62x Sitara™ Processors data sheet.

6 Revision History

Changes from Revision * (May 2022) to Revision A (June 2022)	Page
• Added link to TPS65219EVM design files	4
• Updated *AM62x SK E5 EM* with *SK-AM62-P1* and added hyperlink to the design files	4
• Deleted sample availability	4
• Added hyperlink to SK-AM62-P1	10

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